EIGEN
ENGINEERING, INC

PRELIMINARY RESULTS

Test Of CCU/CSU Interface Devices

For

Data Acquisition System (ANATEC)

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Prepared For: Sacramento Municipal Utility District
Rancho Seco Nuclear Generating Station

Prepared By: Timothy E. Estes
Senior Engineer

3150 ALMADEN EXPRESSWAY, SUITE 233 • SAN JOSE, CALIFORNIA 95118 • (408) 978-8113

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1.0 INTRODUCTION

This document presents in summary form, the preliminary results of testing of the following Anatec Data Acquisition System, CCU to CSU interface associated components:

A. 120 ohm, 1/4 W. resistor to +5 VDC power supply
B. 180 ohm, 1/4 W. resistor to +5 VDC power supply
C. 47 ohm, 1/4 W. resistor to +8.5 VDC power supply
D. Transistor/Resistor network to +8.5 VDC and +5 VDC power supplies.

The following section will provide the Maximum Credible Voltage (MCV) values, point of application, output values, functionality of the device after testing, for each isolation device tested. All signals were recorded on a 8 channel strip chart recorder. Test inputs were applied for 1 to 2 seconds.

2.0 TEST SUMMARY

2.1 120 and 180 Ohm, 1/4 W. Resistors (Figure 1)

Each resistor was tested using a High-Level Analog Input Multiplexer (MUX) circuit board to provide the +5 VDC for testing. The normal DC source for the interface components comes from a power supply contained on the same circuit board as these components. The MUX circuit board was used to determine the effects of an applied MCV on that board 5 VDC power supply and the +8.5 VDC feeding it. The resistor (120 or 180 ohm) was effectively inserted across the +5 VDC to common gound. The MCV of at least 120 VAC RMS was applied between the resistor and ground.

2.1 120 and 180 Ohm, 1/4 W. Resistors (Continued)

Test results show the following:

A. When the MCV was applied between the test resistor and ground, the test resistor opened due to overcurrent within 10 milliseconds or less. This resulted in sharp voltage spikes, of the same duration, being felt in the +5 VDC and +8.5 VDC power supplies. The on-board +5 VDC or the +8.5 VDC power supply were not effected by this surge. After the resistor opened, the power supplies returned to normal levels. A 0.1 volt peak-to-peak ripple, found on strip chart traces of the +5 VDC and +8.5 VDC afterwards, is felt to be the result of induced voltages from the test leads used. The ripple disappears when the 120 VAC MCV is turned off.

B. For the 120 ohm resistor test, the maximum voltage spike felt on the +5 VDC was 2.2 volts peak-to-peak and of 10 millisecond duration. For the +8.5 VDC, the maximum spike was 1.2 volts peak-to-peak and of 5 millisecond duration. (See Table 1)

C. For the 180 ohm resistor test, the maximum voltage spike seen on +5 VDC was 2.5 volts peak-to-peak and 10 millisecond duration. The maximum spike on the +8.5 VDC power supply was 1.3 volts peak-to-peak and of 5 millisecond duration. (See Table 2)

D. A six minute run, using a 180 ohm resistor, with MCV applied, showed no deterioration of +5 VDC and +8.5 VDC power supplies over the run period.

2.2 47 ohm, 1/4 W. Resistor (Figure 3)

For this test, a 47 ohm resistor was essentially placed across a +8.5 VDC power supply output. A MCV of at least 120 VAC was input between the test resistor and common ground.

Test results show the following:

A. When 120 VAC was applied, the 47 ohm resistor opened within 15 milliseconds. This caused the +8.5 power supply to see a maximum 2.0 volt peak-to-peak fluctuation lasting for 0.2 seconds. The +8.5 VDC then returned to normal level. (See Table 3)

B. A 0.25 volt peak-to-peak ripple, seen on the +8.5 VDC level after the resistor opened, appears to be induced into the circuit by test leads used. It disappears when the MCV is turned off.

2.3 Transistor/Resistor Network (Figure 2)

A bread-board circuit was fabricated to simulate this interface circuitry. An MCV of 120 VAC or greater was applied between the transistor collector and common ground. The effects of the MCV was monitored at the +5 VDC and +8.5 VDC power supplies, transistor base voltage, the voltage drop across the 47 ohm resistor, and the logic input line to the circuit inverter.

2.3 Transistor/Resistor Network (Continued)

Test results show the following:

A. The 47 and 160 ohm resistors opened or effectively opened within 5 milliseconds of the MCV application.

B. The transistor shorted internally between collector, emitter and base within the above 5 milliseconds.

C. The maximum spike felt by the +5 VDC power supply was a 0.5 volt peak-to-peak fluctuation of 5 millisecond duration. The +8.5 VDC power supply felt a 0.7 volt peak-to-peak fluctuation of 5 millisecond duration. Both power supplies return to normal levels after the fluctuations. (See Table 4)

D. The 750 ohm resistor opened after 1.02 seconds with some signs of overheating.

E. During this 1.02 second period, the logic input to the inverter experienced a 1.5 volt peak-to-peak spike for 5 milliseconds and then a 0.45 volt peak-to-peak sine wave of 60 Hz for the remainder of the 1.02 seconds. This ended when the 750 ohm resistor opened.

TABLE 1

Preliminary CCR/CSU Interface Test Results

Test Resistor: 120 Ohms

Date: 6/15/87

Figure No.: 1

Time: 0716

Test#	Input Voltage P-P	Input Current P-P/DUR	+8.5 VDC Voltage P-P/DUR	+5 VDC Voltage P-P/DUR
1	333	1.5A/.015 sec	0.5V/.01 sec.	1V/.01 sec
2	355	1.3A/.005 sec	0.3V/.005 sec	1.8V/.005 sec
3	342	0.5A/.005 sec	0.6V/.002 sec	0.4V/.005 sec
4	344	1.0A/.01 sec	1.2V/.005 sec	0.6V/.01 sec
5	344	1.35A/.01 sec	0.7V/.01 sec	2.2V/.01 sec

Comments: The 120 ohm resistor opens within the input current spike duration period.

TABLE 2

Preliminary CCR/CEU Interface Test Results

Test Resistor: 180 Ohms

Date: 6/15/87

Figure No.: 1

Time: 0735

Test#	Input Voltage P-P	Input Current P-P/DUR	+8.5 VDC Voltage P-P/DUR	+5 VDC Voltage P-P/DUR
1	344V	2A/.015sec	0.6V/.005sec	2.5V/.01sec
2	344V	1.1A/.007sec	0.7V/.005sec	0.2V/.007sec
3	344V	1.72A/.015sec	1.3V/.005sec	0.8V/.01sec
4	335V	2A/.03sec	0.6V/.01sec	2.0V/.02sec
5	335V	1.65A/.025sec	1.2V/.01sec	0.55V/.02sec

Comments: The 180 ohm resistor opens within the input current spike time duration period.

TABLE 3

Preliminary CCR/CSU Interface Test Results

Test Resistor: 47 Ohms Date: 6/16/87

Figure No.: 3 Time: 1205

Test#	Input Voltage P-P	Input Current P-P/DUR	+8.5 VDC Voltage P-P/DUR	+5 VDC Voltage P-P/DUR
1	335	1.5 A / .015 sec	1.5V / .25 sec	N/A /
2	315	1.7A / .01sec	2.0V / .20 sec	N/A /
		/	/	/
		/	/	/
		/	/	/

Comments: The 47 ohm resistor opens within the input current spike pulse duration.

TABLE 4

Preliminary CCR/CSU Interface Test Results

Test Device : Transistor/Resistor Network Date: 6/17/87

Figure No.: 2 Time: 0952

Test#	Input Voltage P-P	Input Current P-P/DUR	+8.5 VDC Voltage P-P/DUR	+5 VDC Voltage P-P/DUR
1	337	1.5A/.005 SEC	0.7V/.005 SEC	0.5V/.005 SEC
		/.	/.	/.
		/.	/.	/.
		/.	/.	/.
		/.	/.	/.

Comments: Transistor shorted internally, base to emitter to collector; 47 and 750 ohm resistors opened; 160 ohm resistor effectively open at 1.51 megohms; Logic input terminal (TP-1) received a 0.45 V peak to peak signal at 60 Hz until the 750 ohm resistor opened after 1.02 seconds

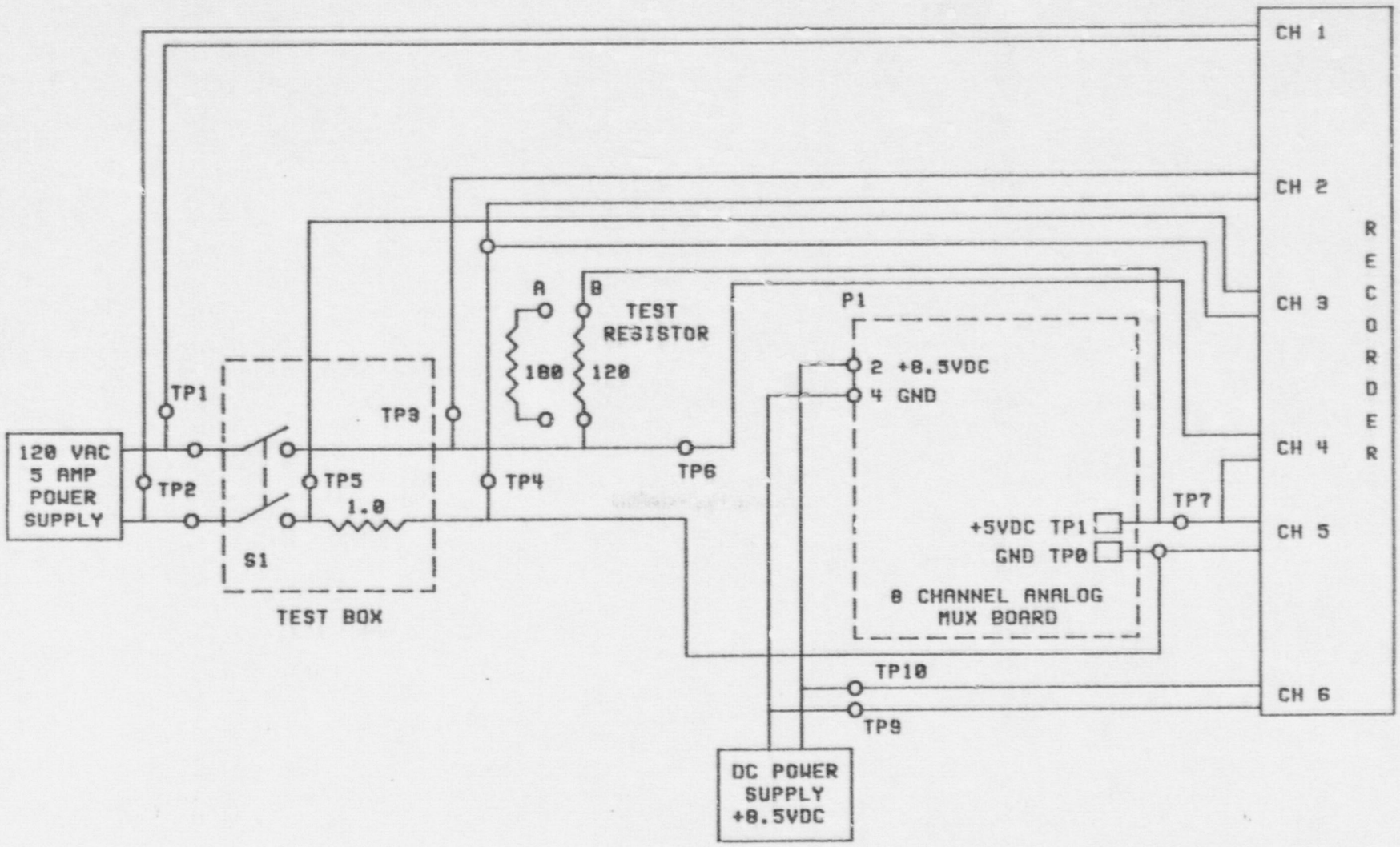

FIGURE 1

EIGEN ENGINEERING, INC. 3150 ALMADEN EXPRESSWAY, SAN JOSE, CA			
TITLE: TEST SETUP FOR MCV TEST OF 120 & 180 OHM RESISTOR INTERFACE			
DWG. NO.: SMD-1035-87-001 SH 1 OF 1			
REVISION	PREPARED BY	APPROVED BY	DATE
A	TEE		

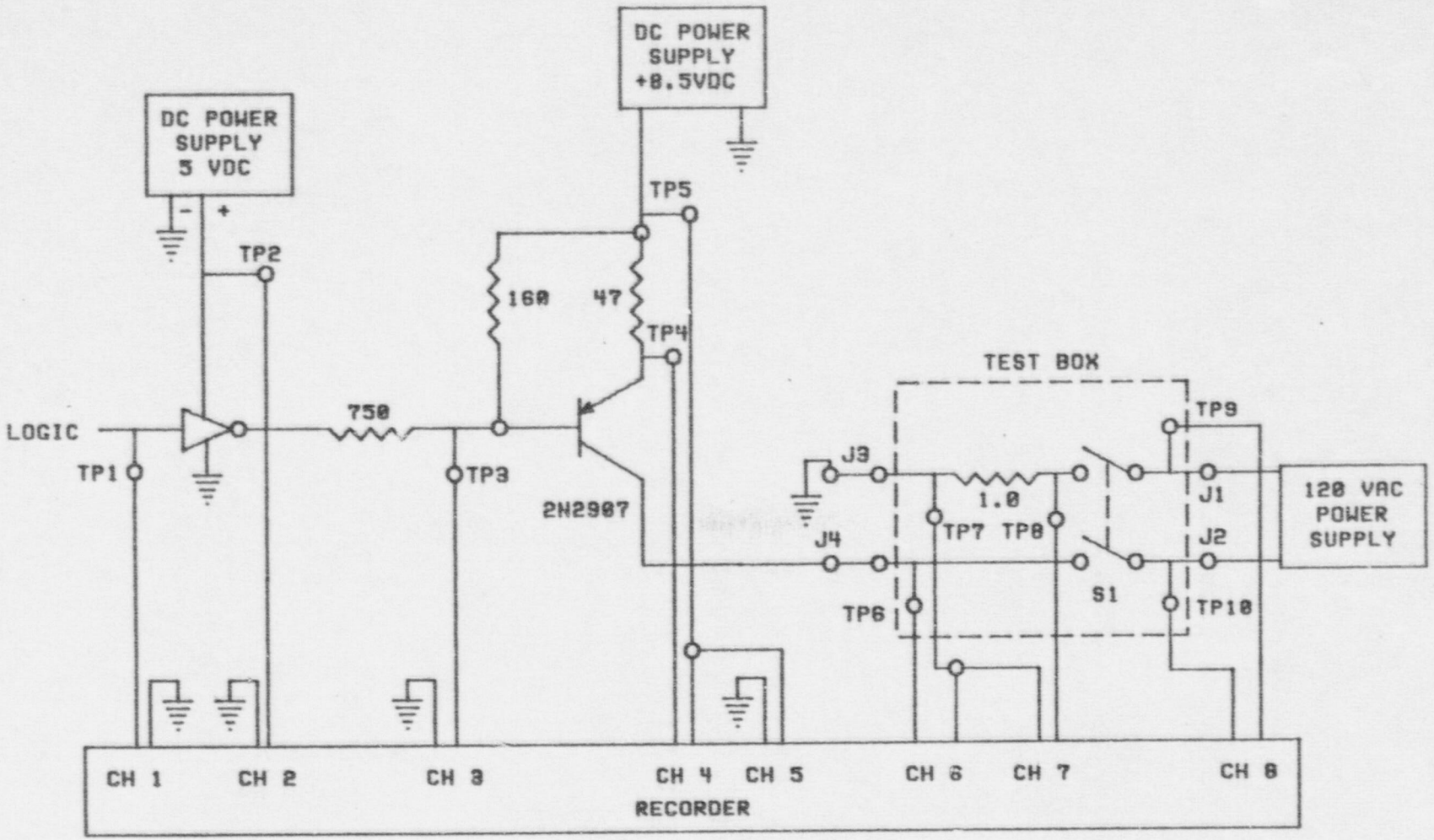

FIGURE 2

EIGEN ENGINEERING, INC. 3150 ALMADEN EXPRESSWAY, SAN JOSE, CA			
TITLE: TEST SETUP FOR MCV TEST OF TRANSISTOR/RESISTOR INTERFACE			
DWG. NO.: SMD-1035-87-002 SH 1 OF 1			
REVISION	PREPARED BY	APPROVED BY	DATE
A	TEE		

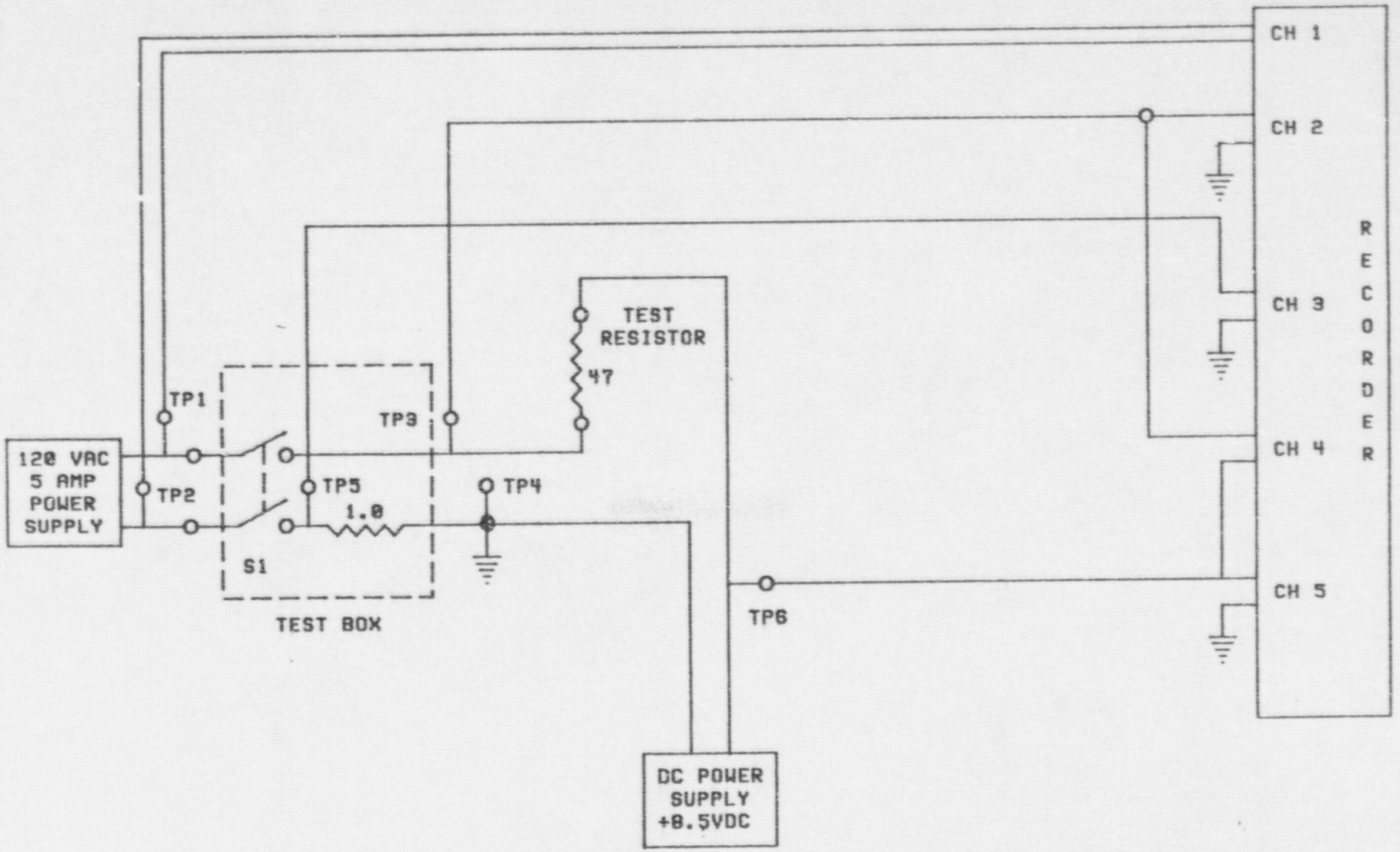

FIGURE 3

EIGEN ENGINEERING, INC. 3150 ALMADEN EXPRESSWAY, SAN JOSE, CA			
TITLE: TEST SETUP FOR MCV TEST OF 47 OHM RESISTOR INTERFACE			
DWG. NO.: SMD-1035-87-003 SH 1 OF 1			
REVISION	PREPARED BY	APPROVED BY	DATE
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