

ATTACHMENT 3
BG&E 32500-EX
NUS DA8827

REMOTE I/O EQUIPMENT
HARDWARE ACCEPTANCE TEST
PROCEDURE for
NUS CORP. /
BALTIMORE GAS and ELECTRIC
CALVERT CLIFFS
DATA ACQUISITION SYSTEM

AT C.P.I. (FORT LAUDERDALE)
20 February 1984

 **Computer Products, Inc.**
Measurement & Control Systems Division

*Unit 4
Cab. 1*

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P PDR

COMPUTER PRODUCTS, INCORPORATED
MEASUREMENT & CONTROL SYSTEMS DIVISION

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PROCEDURE APPROVED BY: Steve Kelly DATE 2/27/84
(B.G.E.) TITLE: Engineer

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/20/84

This revision of the Remote I/O Hardware Acceptance Test Procedure,
dated 2/20/84, includes the following pages :

- Page 1 dated 20 February 1984,
- Page 2 dated 2/2/84,
- Page 2a dated 2/20/84,
- Page 3 through 78 dated 2/2/84,
- Pages 79 through 80 dated 2/20/84,
- Pages 81 through 88 dated 2/2/84,
- Pages 89 through 90 dated 2/20/84, and
- Pages 91 through 116 dated 2/2/84.

Revision 2/20/84 approved by :

(C.P.I.)	<u><i>[Signature]</i></u>	DATE	<u>2/28/84</u>
(N.U.S.)	<u><i>[Signature]</i></u>	DATE	<u>2/28/84</u>
(B.G.E.)	<u><i>[Signature]</i></u>	DATE	<u>2/28/84</u>

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BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
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UNIT # 11

SYSTEM CABINET ID: SRA Cabinet # 1

TEST CONDUCTOR : Robert Lega

NUS REPRESENTATIVE : B.W. BUZAK

BGE REPRESENTATIVE : MICHAEL S. JONES

Procedure copy complete : Initials : RL / /

DATE TEST STARTED : 3/7/84

LOG BOOK PAGES: 11 _____

TEST COMPLETED BY: Robert Lega DATE 3/16/84

(C.P.I.) TITLE: Service Center Manager

TEST WITNESSED BY: [Signature] DATE 3/16/84

(N.G.S.) TITLE: Director Quality Assurance

TEST WITNESSED BY: NOT AVAILABLE WJD DATE _____

(B.G.E.) TITLE: _____

1. GENERAL DESCRIPTION

The purpose of this document is to provide a procedure for the performance of a customer acceptance test of the remote input/output equipment hardware purchased by NUS Corporation by purchase order number DA 8827-1 and sold by Computer Products Incorporated, Measurement and Control Systems Division by sales order numbers 28334 (Unit I) and 28335 (Unit II) at the Fort Lauderdale plant of CPI. This equipment is destined to be installed in the Baltimore Gas and Electric Calvert Cliffs power generation plant.

The equipment is broken into two 'units', 'Unit 1' and 'Unit 2'. Each unit is divided into two 'channels', 'Channel A' and 'Channel B'. The channels are composed of the following 'subsystems': 'Safety Related A', 'Safety Related B', 'Non-Safety Related A', 'Non-Safety Related B', 'Shared A-B', 'Data Concentrator / Maintenance Panel A', and 'Data Concentrator / Maintenance Panel B'. Each subsystem may be composed of one or more cabinets containing the I/O equipment.

The testing of the remote I/O equipment at this level does not include the Data Concentrator equipment nor the Data Concentrator remote links, the Intelligent Remote Control Units.

Testing will be performed on a per cabinet basis with one copy of this procedure assigned to each cabinet. Each type of product in a cabinet will be tested as a group before proceeding to the next type of equipment.

Cabinets in the Non-Safety Related and the Shared subsystems have wiring that source or terminate in another cabinet within its subsystem and due to this inter-cabinet and inter-chassis wiring, some connections and measurements will be made at cabinets or controllers other than the one under test.

2. TABLE OF CONTENTS / SCOPE OF TESTS

SECTION 3. - Dispositioning and Test Data Recording

The dispositioning of the tested product and the recording of test results is described in this section.

SECTION 4. - Test Equipment Requirements

The equipment required to perform this acceptance test is listed in this section.

SECTION 5. - Reference Documents

Documents referenced by the procedure and the documents associated with the equipment under test and the test equipment are listed.

SECTION 6. - Configuration of Equipment for Testing

This section describes the special configurations of the test equipment and the equipment to be tested for the performance of the tests.

SECTION 7. - Equipment Under Test Configuration Verification

The correspondance of the configuration of the equipment in the cabinet to the equipment configuration drawings will be verified.

SECTION 8. - AC Power Distribution/Indicator Panel and Power Supply Validation

The AC Power Distribution and Indicator Panel and the power supplies will be validated as operational and the corresponding power wiring will be validated to be accurate.

SECTION 9. - Optically Isolated Digital Input Module Validation

Each Optically Isolated Digital Input Module and the corresponding signal conditioning module will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 10. - O.I.D.I. Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected Optically Isolated Digital Inputs in the cabinet under test will be validated as operational in compliance with IEEE standard § 472.

SECTION 11. - Change of State Digital Input Module Validation

Each Change of State Digital Input Module and the corresponding signal conditioning module will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 12. - C.O.S.D.I. Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected Change of State Digital Inputs in the cabinet under test will be validated as operational in compliance with IEEE standard § 472.

SECTION 13. - Quad Pulse Counter Module Validation

Each Quad Pulse Counter Module and the corresponding signal conditioning module will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 14. - Quad Pulse Counter Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected Quad Pulse Counters in the cabinet under test will be validated as operational in compliance with IEEE standard § 472.

SECTION 15. - Up/Down Pulse Counter Module Validation

Each Up/Down Pulse Counter Module and the corresponding signal conditioning module will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 16. - Up/Down Pulse Counter Module Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected Up/Down Pulse Counters in the cabinet under test will be validated as operational in compliance with IEEE standard # 472.

SECTION 17. - Digital and Analog Loopback and Calibration Module and Analog to Digital Converter Module Validation.

Each Digital and Analog Loopback and Calibration Module and Analog to Digital Converter Module will be validated as operational and accurate; the temperature sensing transducers will be validated as operational and accurate; and the associated cabling will be associated to be accurate.

SECTION 18. - Power Supply Monitoring Analog Inputs Validation

Each analog input gate module monitoring the cabinet power supplies, the RTD SCM power supplies, and the contact sense power supplies will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 19. - Voltage Sensing Analog Input Gate Module Validation

Each voltage sensing analog input gate module and the corresponding signal conditioning module will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 20. - Voltage Sensing Analog Input Gate Module Accuracy, Common Mode Voltage Rejection, and Surge Withstand Capability Validation

The common mode voltage rejection and the accuracy of a sample of up to five percent (or at least one) of the voltage sensing analog input gate modules in the cabinet will be validated. Then a surge will be applied to the sample in compliance with IEEE standard # 472. The common mode voltage rejection and accuracy of the sample will then be revalidated to validate the operation of the surge protection circuitry.

SECTION 21. - Resistive Sensing Analog Input Gate Module Validation

Each resistive sensing analog input gate module and the corresponding signal conditioning module(s) will be validated as operational, and the associated cabling will be validated as accurate.

SECTION 22. - Resistive Sensing Analog Input Gate Module Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected resistive sensing analog inputs in the cabinet under test will be validated as operational in compliance with IEEE standard § 472.

SECTION 23. - Voltage Sensing Analog Input Gate Module Stability Validation

The voltage sensing analog input gate modules selected for validation of common mode voltage rejection, accuracy, and surge withstand capability will be validated to be stable.

APPENDIX A. - Test and Repair Log Book Format

The format of the log book used to document records of the testing and any anomalies or non-conformances found is illustrated in this appendix.

APPENDIX B. - CPI RTP Control Panel Description and Operating Instructions

This appendix contains a description and instructions on the operation of the CPI RTP Control Panel, one of the primary pieces of test equipment used to perform the test.

APPENDIX C. - Slot/Address Cross Reference Table for UI/OC and RAUI/OC

This is a table cross referencing the physical slot number of the option card slots of the Universal I/O Controllers with their programming addresses.

APPENDIX D. - Operating Instructions and Test Configuration for Velonex Transient Surge Transient Generator

The operation and configuration of the Velonex Surge Transient Generator, used to test the surge withstand capabilities of the equipment in compliance with IEEE standard # 472 is described in this appendix.

ATTACHMENT 1. - Test Configuration Drawings

This attachment contains drawings depicting the configurations of test equipment used for the various tests.

ATTACHMENT 2. - Equipment Configuration Drawings

This attachment contains the drawings of the configuration of the equipment in the cabinet as the equipment will be tested.

3. DISPOSITIONING AND TEST DATA RECORDING

The acceptance test will be performed using a copy of this procedure stamped 'Controlled Document' with the required signatures on the approval signature page (page 2).

At the beginning of the test :

- 1) The test conductor and the representatives from NUS and BGE will print their names on the test performance signature page (page 3) of the copy of the test procedure; (All entries made on all documents will be made in black ink.)
- 2) The copy will be verified to assure that there is one and only one copy of each page of the procedure included; The test performance signature page will then be initialed;
- 3) An entry will be made to the 'Test and Repair Log' using the format illustrated in Appendix A, to mark the commencement of the test on a cabinet;
- 4) The unique identification of the cabinet under test will be entered on the test performance signature page;
- 5) The page number of any and all pages of the log book associated with the cabinet under test will also be recorded on the test performance signature page; and
- 6) The CPI identification numbers, where applicable, of the test equipment used to perform this acceptance test will be noted in the required test equipment section (Section 4.) of the copy of the procedure.

A module identifier block appears in each verification/ validation section of this procedure. Successful completion of applicable steps of the procedure on an individual product or product set shall be indicated by entering the location identifier of the module in the controller and the controller's identifier and initialed by the test conductor and a witness.

A signature block appears at the end of each verification/ validation section of this procedure. Successful completion of an applicable section on all products specified by the procedure shall be indicated by the signatures of the appropriate representatives of CPI, NUS, and BGE (where applicable).

When a section of the procedure is NOT applicable to a cabinet, 'N/A' will be entered on the signature lines and will be initialed by the appropriate representatives.

Anomalies or non-conformances encountered during the performance of the test shall be handled as follows:

- 1) An entry is made in the Test and Repair Log describing the non-conformance;
- 2) The non-conformance will be documented on a Non-Conforming Material Report (NCRM) form (reference: AQ 5.01);
- 3) The non-conformance is corrected;
- 4) The corrective action is documented in the Test and Repair Log;
- 5) The corrective action is documented on the NCRM form;
- 6) The applicable validation steps are repeated and successful completion is indicated by the signature of the representatives on the signature block.

Note that if a non-conformance is encountered during the performance of one of the validations of a five percent sample, the steps above will be performed and in addition another sample is selected and tested.

4. TEST EQUIPMENT REQUIRED

The equipment required to perform this acceptance test is as listed below:

(All electronic test equipment shall be in compliance with C.P.I. Quality Assurance procedure AQ 8.02 - 'Calibration Control System'.)

- 4.1 Digital multimeter :
Hewlett Packard Co. Model # 3468B CPI ID # 5541
- 4.2 Programmable DC Voltage Source :
Electronic Development Corp. Model # 501-J CPI ID # 5572
- 4.3 AC/DC V-A Source :
RPL Industries, Inc. Model No. 828 CPI ID # 5571
- 4.4 Surge Transient Generator :
Velonex Model No. 510 CPI ID # 5455
- 4.5 Digital Thermometer :
Omega Engineering Inc. Model No. 2166A CPI ID # 5519
- 4.6 CPI Analog Input System Test Computer : LSI-11 based
(See the 'Description and Operating Instructions for the CPI Analog Input Test Computer and Analog Input Test Programs')
- 4.7 CPI RTP Control Panels , 2 ea.
(CPI # 070-0044-001)
- 4.8 CPI Universal I/O Controller
(CPI # 070-0004-003)
- 4.9 CPI Special Relay Output Module with contact protection
(CPI # 000-7066-000)
- 4.10 CPI Special Pulsing Relay Output Module with contact protection
(CPI # 000-7067-000)
- 4.11 CPI I/O Bus Termination Module
(CPI # 021-0004-000)
- 4.12 CPI RTP I/O Bus Cables
(CPI # 314-0001-010 1 each and
CPI # 314-0001-020 1 each)
- 4.13 CPI 12 Volt Power Supply, panel mounted
(CPI # 070-0008-000)

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- 4.14 CPI BTSCA (25 inch, 48 pin) to Test Cable/Connector Adapter
(CPI # 000-7077-000)
- 4.15 CPI Digital Input Surge Protection Test Connector
(CPI # 000-7078-000)
- 4.16 CPI Pulse Counter Surge Protection Test Connector
(CPI # 000-7097-000)
- 4.17 CPI Analog Input Unbalanced (1 Kohm) Test Termination/Connector
(CPI # 000-7079-000)
- 4.18 CPI Digital Test Cable
(CPI # 000-7080-000)
- 4.19 CPI Analog Input Test Divider/Connector for BTSCAs
(CPI # 000-7081-000)
- 4.20 CPI Analog Input Parallel Input Test Connector
(CPI # 000-7082-000)
- 4.21 CPI Analog Input Test Divider/Connector for UTRPs
(CPI # 000-7085-000)
- 4.22 CPI RTD Resistor Termination: Platinum 200 ohm, 32 : 350 F
(CPI # 000-7086-000)
- 4.23 CPI RTD Resistor Termination: Platinum 200 ohm, 32 : 850 F
(CPI # 000-7087-000)
- 4.24 CPI RTD Resistor Termination: Platinum 200 ohm, 32 : 110 F
(CPI # 000-7088-000)
- 4.25 CPI RTD Resistor Termination: Copper 10 ohm, -10 : 209 C
(CPI # 000-7089-000)
- 4.26 CPI Up/Down Pulse Counters Test Headers w/ diodes
(CPI # 000-7098-000, -001, -002, -003)
- 4.27 AC Power Receptacle Tester :
Ideal Industries, Inc. Model No. 6I-035

5. REFERENCE DOCUMENTS

This section lists the documents referenced by the procedure and the documents associated with the equipment under test and the test equipment. Other documents may be referred to by the documents listed in this section.

5.1 CPI Univ. A.D.C. Card and Univ. A.I. Card Set (# 021-0211)

- 5.1.1 Parts List (CPI # AP 020-0211)
- 5.1.2 Parts List (CPI # AP 021-0211)
- 5.1.3 Schematic (CPI # CS 021-0211)
- 5.1.4 Assembly Dwg. (CPI # CA 021-0211)
- 5.1.5 Technical Manual (CPI # 980-0021-211)
- 5.1.6 Engineering Specification (CPI # AE 021-0211)
- 5.1.7 Test Procedure (CPI # AT 021-0211)

5.2 CPI Digital Input Card (# 021-5227)

- 5.2.1 Parts List (CPI # AP 020-5227)
- 5.2.2 Parts List (CPI # AP 021-5227)
- 5.2.3 Schematic (CPI # CS 021-5227)
- 5.2.4 Assembly Dwg. (CPI # CA 021-5227)
- 5.2.5 Technical Manual (CPI # 980-0021-227)
- 5.2.6 Engineering Specification (CPI # AE 021-5227)
- 5.2.7 Test Procedure (CPI # AT 021-5227)

5.3 CPI Optically Isolated Digital Input Card (# 021-5230)

- 5.3.1 Parts List (CPI # AP 020-5230)
- 5.3.2 Parts List (CPI # AP 021-5230)
- 5.3.3 Schematic (CPI # CS 021-5230)
- 5.3.4 Assembly Dwg. (CPI # CA 021-5230)
- 5.3.5 Technical Manual (CPI # 980-0021-230)
- 5.3.6 Engineering Specification (CPI # AE 021-5230)
- 5.3.7 Test Procedure (CPI # AT 021-5230)

5.4 CPI Universal B.S.W.R. Analog Input Gate Card (# 021-5234)

- 5.4.1 Parts List (CPI # AP 020-5234)
- 5.4.2 Parts List (CPI # AP 021-5234)
- 5.4.3 Schematic (CPI # CS 021-5234)
- 5.4.4 Assembly Dwg. (CPI # CA 021-5234)
- 5.4.5 Technical Manual (CPI # 980-0021-211)
- 5.4.6 Engineering Specification (CPI # AE 021-5234)
- 5.4.7 Engineering Specification (CPI # AE 021-0211)
- 5.4.8 Test Procedure (CPI # AT 021-5234)
- 5.4.9 Test Procedure (CPI # AT 021-0211)

5.5 CPI Digital and Analog Loopback and Cal. Card (# 021-5271)

- 5.5.1 Parts List (CPI # AP 021-5271)
- 5.5.2 Schematic (CPI # CS 021-5271)
- 5.5.3 Assembly Dwg. (CPI # CA 021-5271)
- 5.5.4 Engineering Specification (CPI # AE 021-5271)
- 5.5.5 Test Procedure (CPI # AT 021-5271)

5.6 CPI Quad Pulse Counter Card (# 021-5278)

- 5.6.1 Parts List (CPI # AP 021-5278)
- 5.6.2 Schematic (CPI # CS 021-5278)
- 5.6.3 Assembly Dwg. (CPI # CA 021-5278)
- 5.6.4 Engineering Specification (CPI # AE 021-5278)
- 5.6.5 Test Procedure (CPI # AT 021-5278)

5.7 CPI Change of State Digital Input Card (# 038-5064)

- 5.7.1 Parts List (CPI # AP 038-5064)
- 5.7.2 Schematic (CPI # CS 038-5064)
- 5.7.3 Assembly Dwg. (CPI # CA 038-5064)
- 5.7.4 Engineering Specification (CPI # AE 038-5064)
- 5.7.5 Test Procedure (CPI # AT 038-5064)

5.8 CPI Analog Input Signal Conditioning Module (# 038-5097)

- 5.8.1 Parts List (CPI # AP 038-5097)
- 5.8.2 Schematic (CPI # CS 038-5097)
- 5.8.3 Assembly Dwg. (CPI # CA 038-5097)
- 5.8.4 Engineering Specification (CPI # AE 038-5097)
- 5.8.5 Test Procedure (CPI # AT 038-5097)

5.9 CPI Digital Input Signal Conditioning Module (# 038-5098)

- 5.9.1 Parts List (CPI # AP 038-5098)
- 5.9.2 Schematic (CPI # CS 038-5098)
- 5.9.3 Assembly Dwg. (CPI # CA 038-5098)
- 5.9.4 Engineering Specification (CPI # AE 038-5098)
- 5.9.5 Test Procedure (CPI # AT 038-5098)

5.10 CPI C.O.S. D.I. Signal Conditioning Module (# 038-5099)

- 5.10.1 Parts List (CPI # AP 038-5099)
- 5.10.2 Schematic (CPI # CS 038-5099)
- 5.10.3 Assembly Dwg. (CPI # CA 038-5099)
- 5.10.4 Engineering Specification (CPI # AE 038-5099)
- 5.10.5 Test Procedure (CPI # AT 038-5099)

5.17 CPI U-16 Universal I/O Controller (# 040-5462)

- 5.17.1 Parts List (CPI # AP 040-5462)
- 5.17.2 Logic Dwg. (CPI # CL 070-5073)
- 5.17.3 Assembly Dwg. (CPI # CA 040-5462)
- 5.17.4 Technical Manual (CPI # 980-0070-004)
- 5.17.5 Engineering Specification (CPI # AE 040-5462)
- 5.17.6 Test Procedure (CPI # AT 070-5073)
- 5.17.7 Wiring Diagram (CPI # CW 318-5010)

5.18 CPI Reversed RTD Signal Conditioning Chassis (# 040-5467)

- 5.18.1 Parts List (CPI # AP 040-5467)
- 5.18.2 Assembly Dwg. (CPI # CA 040-5467)
- 5.18.3 Engineering Specification (CPI # AE 040-5467)
- 5.18.4 Test Procedure (CPI # AT 040-5467)
- 5.18.5 Wiring Diagram (CPI # CW 040-5467)
- 5.18.6 Technical Manual (CPI # 980-0040-213)

5.19 CPI Redundant +/-15 Volt/ 2.25 Amp Power Supply (# 040-5482)

- 5.19.1 Parts List (CPI # AP 040-5482)
- 5.19.2 Assembly Dwg. (CPI # CA 040-5482)
- 5.19.3 Engineering Specification (CPI # AE 040-5482)
- 5.19.4 Test Procedure (CPI # AT 040-5482)
- 5.19.5 Wiring Diagram (CPI # CW 040-5482)

5.20 CPI Redundant 5 Volt/ 30 Amp Power Supply (# 040-5483)

- 5.20.1 Parts List (CPI # AP 040-5483)
- 5.20.2 Assembly Dwg. (CPI # CA 040-5483)
- 5.20.3 Engineering Specification (CPI # AE 040-5483)
- 5.20.4 Test Procedure (CPI # AT 040-5483)
- 5.20.5 Wiring Diagram (CPI # CW 040-5483)

5.21 CPI Redundant +/-15 Volt/ 4.5 Amp Power Supply (# 040-5484)

- 5.21.1 Parts List (CPI # AP 040-5484)
- 5.21.2 Assembly Dwg. (CPI # CA 040-5484)
- 5.21.3 Engineering Specification (CPI # AE 040-5484)
- 5.21.4 Test Procedure (CPI # AT 040-5484)
- 5.21.5 Wiring Diagram (CPI # CW 040-5484)

5.22 CPI Redundant 5 Volt/ 60 Amp Power Supply (# 040-5485)

- 5.22.1 Parts List (CPI # AP 040-5485)
- 5.22.2 Assembly Dwg. (CPI # CA 040-5485)
- 5.22.3 Engineering Specification (CPI # AE 040-5485)
- 5.22.4 Test Procedure (CPI # AT 040-5485)
- 5.22.5 Wiring Diagram (CPI # CW 040-5485)

5.23 CPI Redundant +/-15 Volt/ 9.0 Amp Power Supply (# 040-5486)

- 5.23.1 Parts List (CPI # AP 040-5486)
- 5.23.2 Assembly Dwg. (CPI # CA 040-5486)
- 5.23.3 Engineering Specification (CPI # AE 040-5486)
- 5.23.4 Test Procedure (CPI # AT 040-5486)
- 5.23.5 Wiring Diagram (CPI # CW 040-5486)

5.24 CPI Redundant 5 Volt/ 120 Amp Power Supply (# 040-5487)

- 5.24.1 Parts List (CPI # AP 040-5487)
- 5.24.2 Assembly Dwg. (CPI # CA 040-5487)
- 5.24.3 Engineering Specification (CPI # AE 040-5487)
- 5.24.4 Test Procedure (CPI # AT 040-5487)
- 5.24.5 Wiring Diagram (CPI # CW 040-5487)

5.25 CPI A.I. Gate Card to RTD Sig. Cond. Mod. Cable (# 040-5505)

- 5.25.1 Parts List (CPI # AP 040-5505)
- 5.25.2 Assembly Dwg. (CPI # CA 040-5505)
- 5.25.3 Engineering Specification (CPI # AE 040-5505)
- 5.25.4 Wire List (CPI # AW 040-5505)

5.26 CPI Redundant 125 Volt/ 1.0 Amp Power Supply (# 040-5509)

- 5.26.1 Parts List (CPI # AP 040-5509)
- 5.26.2 Assembly Dwg. (CPI # CA 040-5509)
- 5.26.3 Engineering Specification (CPI # AE 040-5509)
- 5.26.4 Test Procedure (CPI # AT 040-5509)
- 5.26.5 Wiring Diagram (CPI # CW 040-5509)

5.27 CPI AC Power Distribution / Indicator Panel (# 040-5511)

- 5.27.1 Parts List (CPI # AP 040-5511)
- 5.27.2 Assembly Dwg. (CPI # CA 040-5511)
- 5.27.3 Engineering Specification (CPI # AE 040-5511)
- 5.27.4 Test Procedure (CPI # AT 040-5511)
- 5.27.5 Wiring Diagram (CPI # CW 040-5511)

- 5.28 CPI Pulse Counter Card to S.C.M. Cable (# 040-5517)
 - 5.28.1 Parts List (CPI # AP 040-5517)
 - 5.28.2 Assembly Dwg. (CPI # CA 040-5517)
 - 5.28.3 Engineering Specification (CPI # AE 040-5517)
 - 5.28.4 Wire List (CPI # AW 040-5517)

- 5.29 CPI Up/Down Pulse Counter Card to S.C.M. Cable (# 040-5518)
 - 5.29.1 Parts List (CPI # AP 040-5518)
 - 5.29.2 Assembly Dwg. (CPI # CA 040-5518)
 - 5.29.3 Engineering Specification (CPI # AE 040-5518)
 - 5.29.4 Wire List (CPI # AW 040-5518)

- 5.30 CPI Digital Barrier Terminal Strip Cable Assembly (# 040-5519)
 - 5.30.1 Parts List (CPI # AP 040-5519)
 - 5.30.2 Assembly Dwg. (CPI # CA 040-5519)
 - 5.30.3 Engineering Specification (CPI # AE 040-5519)
 - 5.30.4 Wire List (CPI # AW 040-5519-0)
 - 5.30.5 Wire List (CPI # AW 040-5519-1)

- 5.31 CPI Analog Barrier Terminal Strip Cable Assembly (# 040-5520)
 - 5.31.1 Parts List (CPI # AP 040-5520)
 - 5.31.2 Assembly Dwg. (CPI # CA 040-5520)
 - 5.31.3 Engineering Specification (CPI # AE 040-5520)
 - 5.31.4 Wire List (CPI # AW 040-5520)

- 5.32 CPI RTD S.C.M. Barrier Terminal Strip Cable Ass'y (# 040-5521)
 - 5.32.1 Parts List (CPI # AP 040-5521)
 - 5.32.2 Assembly Dwg. (CPI # CA 040-5521)
 - 5.32.3 Engineering Specification (CPI # AE 040-5521)
 - 5.32.4 Wire List (CPI # AW 040-5521)

- 5.33 CPI Uniform Temperature Reference Plate (# 040-5522)
 - 5.33.1 Parts List (CPI # AP 040-5522)
 - 5.33.2 Assembly Dwg. (CPI # CA 040-5522)
 - 5.33.3 Engineering Specification (CPI # AE 040-5522)
 - 5.33.4 Wire List (CPI # AW 040-5522)
 - 5.33.5 Technical Manual (CPI # 980-0070-052)

5.34 CPI Redundant Access Universal I/O Controller (# 070-5083)

- 5.34.1 Parts List (CPI # AP 070-5083)
- 5.34.2 Parts List (CPI # AP 069-5083)
- 5.34.3 Logic Dwg. (CPI # CL 070-5076)
- 5.34.4 Assembly Dwg. (CPI # CA 070-5083)
- 5.34.5 Assembly Dwg. (CPI # CA 069-5083)
- 5.34.6 Technical Manual (CPI # 980-0070-004)
- 5.34.7 Engineering Specification (CPI # AE NEQ070-5083)
- 5.34.8 Engineering Specification (CPI # AE 070-5076)
- 5.34.9 Test Procedure (CPI # AT 070-5076)

5.35 CPI Analog Barrier Terminal Strip Cable Assembly (# 075-0053)

- 5.35.1 Parts List (CPI # AP 075-0053)
- 5.35.2 Assembly Dwg. (CPI # CA 075-0053)
- 5.35.3 Engineering Specification (CPI # AE 075-0053)
- 5.35.4 Wire List (CPI # AW 075-0053)

5.36 CPI Digital Barrier Terminal Strip Cable Assembly (# 075-5227)

- 5.36.1 Parts List (CPI # AP 075-5227)
- 5.36.2 Assembly Dwg. (CPI # CA 075-5227)
- 5.36.3 Engineering Specification (CPI # AE 075-5227)
- 5.36.4 Wire List (CPI # AW 075-5227)
- 5.36.5 Technical Manual (CPI # 980-0075-227)

5.37 CPI DALCAL Card Barrier Terminal Strip Cable Ass'y (# 075-5271)

- 5.37.1 Parts List (CPI # AP 075-5271)
- 5.37.2 Assembly Dwg. (CPI # CA 075-5271)
- 5.37.3 Engineering Specification (CPI # AE 075-5271)
- 5.37.4 Wire List (CPI # AW 075-5271)

5.38 CPI I/O Bus Cable (# 314-5043)

- 5.38.1 Parts List (CPI # AP 314-5043)
- 5.38.2 Assembly Dwg. (CPI # CA 314-5043)
- 5.38.3 Engineering Specification (CPI # AE 314-5043)

5.39 CPI Current Source Temperature Transducer (# 559-5002)

- 5.39.1 Parts List (CPI # AP 559-5002)
- 5.39.2 Assembly Dwg. (CPI # AA 559-5002)

5.40 CPI Universal I/O Controller (# 070-0004)

- 5.40.1 Parts List (CPI # AP 070-0004)
- 5.40.2 Parts List (CPI # AP 069-0004)
- 5.40.3 Logic Dwg. (CPI # CL 070-0004)
- 5.40.4 Assembly Dwg. (CPI # CA 070-0004)
- 5.40.5 Assembly Dwg. (CPI # CA 069-0004)
- 5.40.6 Technical Manual (CPI # 980-0070-004)
- 5.40.7 Engineering Specification (CPI # AE 070-0004)
- 5.40.8 Test Procedure (CPI # AT 070-0004)

5.41 CPI RTP Control Panel (# 070-0044)

- 5.41.1 Parts List (CPI # AP 070-0044)
- 5.41.2 Logic Dwg. (CPI # CL 070-0044)
- 5.41.3 Assembly Dwg. (CPI # CA 070-0044)
- 5.41.4 Technical Manual (CPI # 980-0070-044)
- 5.41.5 Engineering Specification (CPI # AE 070-0044)
- 5.41.6 Test Procedure (CPI # AT 070-0044)

5.42 CPI 12 V Power Supply, panel mounted (# 070-0008)

- 5.42.1 Parts List (CPI # AP 070-0008)
- 5.42.2 Assembly Dwg. (CPI # CA 070-0008)
- 5.42.3 Technical Manual (CPI # 980-0070-008)
- 5.42.4 Engineering Specification (CPI # AE 070-0008)
- 5.42.5 Test Procedure (CPI # AT 070-0008)

5.43 CPI Special Relay Out. Card w/ Contact Prot. (# 000-7066)

- 5.43.1 Parts List (CPI # AP 000-7066/7067)
- 5.43.2 Schematic (CPI # CS 000-7066/7067)
- 5.43.3 Assembly Dwg. (CPI # CA 000-7066/7067)
- 5.43.4 Technical Manual (CPI # 980-0021-232)
- 5.43.5 Engineering Specification (CPI # AE 021-5232)
- 5.43.6 Test Procedure (CPI # AT 021-5232)

5.44 CPI Spec. Pulsing Relay Out. Card w/ Contact Prot. (# 000-7067)

- 5.44.1 Parts List (CPI # AP 000-7066/7067)
- 5.44.2 Schematic (CPI # CS 000-7066/7067)
- 5.44.3 Assembly Dwg. (CPI # CA 000-7066/7067)
- 5.44.4 Technical Manual (CPI # 980-0021-232)
- 5.44.5 Engineering Specification (CPI # AE 021-5232)
- 5.44.6 Test Procedure (CPI # AT 021-5232)

- 5.45 CPI BTSCA (25 inch, 48 pin) to Test Cable/Connector Adapter
(CPI # 000-7077)
 - 5.45.1 Assembly Dwg. (CPI # AA 000-7077)
 - 5.45.2 Wire List (CPI # AW 000-7077)
- 5.46 CPI Digital Input Surge Protection Test Connector
(CPI # 000-7078)
 - 5.46.1 Schematic (CPI # AS 000-7078)
- 5.47 CPI Pulse Counter Surge Protection Test Connector
(CPI # 000-7097)
 - 5.47.1 Schematic (CPI # AS 000-7097)
- 5.48 CPI Analog Input Unbalanced (1 Kohm) Test Termination/Connector
(CPI # 000-7079)
 - 5.48.1 Schematic (CPI # AS 000-7079)
- 5.49 CPI Digital Test Cable (CPI # 000-7080)
 - 5.49.1 Schematic (CPI # AS 000-7080)
- 5.50 CPI Analog Input Test Divider/Connector for BTSCAs
(CPI # 000-7081)
 - 5.50.1 Schematic (CPI # AS 000-7081)
- 5.51 CPI Analog Input Parallel Input Test Connector (CPI # 000-7082)
 - 5.51.1 Schematic (CPI # AS 000-7082)
- 5.52 CPI Analog Input Test Divider/Connector for UTRPs
(CPI # 000-7085)
 - 5.52.1 Schematic (CPI # AS 000-7085)

5.53 CPI RTD Resistor Terminations

5.53.1 Platinum 200 ohm, 32 ± 350 F (CPI # 000-7086)

5.53.1.1 Information Dwg. (CPI # AH 000-7086)

5.53.2 Platinum 200 ohm, 32 ± 850 F (CPI # 000-7087)

5.53.2.1 Information Dwg. (CPI # AH 000-7087)

5.53.3 Platinum 200 ohm, 32 ± 110 F (CPI # 000-7088)

5.53.3.1 Information Dwg. (CPI # AH 000-7088)

5.53.4 Copper 10 ohm, -10 ± 209 C (CPI # 000-7089)

5.53.4.1 Information Dwg. (CPI # AH 000-7089)

- 5.54 CPI Quality Assurance Procedure (CPI # AQ 8.02) -
'Calibration Control System'
- 5.55 CPI Quality Assurance Procedure (CPI # AQ 5.01) -
'Non-Conforming Material Control System'
- 5.56 CPI 'Description and Operating Instructions for the CPI Analog
Input Test Computer and Analog Input Test Programs'
- 5.57 IEEE Standard # 472-1974 - 'Guide for Surge Withstand
Capability (SWC) Testing'
- 5.58 Hewlett Packard Co. 'Operator's Manual for 3468A/B Multimeter'
- 5.59 Velonex 'Instruction Manual for Model 510 Surge Transient
Generator'
- 5.60 Electronic Development Corp. 'Operator's Manual for Model 501
Programmable DC Voltage Standard'
- 5.61 Omega Engineering, Inc. 'Instruction Manual for Model 2166A
Multipoint Digital Thermometer'
- 5.62 RFL Industries, Inc. 'Instruction Manual for Model 828 AC/DC
V-A Source'

6. CONFIGURATION OF EQUIPMENT FOR TESTING

Specific or special configurations of the test equipment shall be as follows:

- 6.1 One RTP Control Panel (070-0044-001), with Device Address Select switches set for '111111', shall be labelled '#1'.
- 6.2 The test Universal I/O Controller (070-0004-003), with First Device Code set for '111111', shall contain:
 - 6.2.1 a I/O Bus Termination module (021-0004) in slot 2;
 - 6.2.2 a Special Relay Output Module (000-7066) with contact protection in slot 6; and
 - 6.2.3 a Special Pulsing Relay Output Module (000-7067) with contact protection in slot 7.
- 6.3 One RTP I/O Bus Cable (314-0001-020) shall connect the Control Panel #1 (slot 5) to the test Universal I/O Controller (slot 1).
- 6.4 The output of the panel mounted 12 volt power supply shall be wired terminal block TB 1 of the test universal I/O controller to supply the 12 volts necessary to drive the relay output modules.
- 6.5 The other RTP Control Panel (070-0044-001) shall be labelled '#2';
- 6.6 One RTP I/O Bus Cable (314-0001-001) shall be connected to Control Panel #2 (slot 5) with the other end to be connected to the equipment in the cabinet under test.
- 6.7 The AC/DC V-A Source shall be configured to output 600 Volts AC RMS, 60 Hertz.
- 6.8 The Surge Transient Generator shall be configured as described in Appendix D.

- 6.9 Connect the I/O Bus Cable (314-0001-010) from Control Panel #2 to the 'first' I/O controller (slot 1 of standard Universal I/O Controllers (040-5462) or slot 4 of Redundant Access Universal I/O Controllers (070-5083)) in I/O daisy-chain of the cabinet set under test.
- 6.10 Set the first device code of the 'first' I/O controller in the cabinet set daisy-chain to '110000' (binary) (48 (decimal)) and the second device code of the first controller to '110001' (binary) (49 (decimal)). Set the devices codes of the successive controllers in the daisy-chain as follows:

DEVICE CODE

	FIRST		SECOND	
	(binary)	(decimal)	(binary)	(decimal)
second controller	'110010'	50	'110011'	51
third controller	'110100'	52	'110101'	53
fourth controller	'110110'	54	'110111'	55
fifth controller	'111000'	56	'111001'	57
sixth controller	'111010'	58	'111011'	59
seventh controller	'111100'	60	'111101'	61
eighth controller	'111110'	62	'111111'	63

- 6.11 Set the 'One Device Code/Two Device Code' switch on all I/O controllers to 'Two Device Codes'.
- 6.12 Install the Up/Down Pulse Counters Test Headers (000-7098) on any Up/Down Pulse Counters (038-5115) in the cabinet under test (-000 for counter #0 (DS2), -001 for counter #1 (DS1), -002 for counter #2 (DS3), and -003 for counter #3 (DS4)).

7. EQUIPMENT UNDER TEST CONFIGURATION VERIFICATION

Verify that the configuration of the equipment in the cabinet corresponds to the equipment cabinet configuration drawings of Attachment 2.

If a non-conformance is noted during the configuration verification, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the verification of the configuration will continue with the item found to be non-conforming.

EQUIPMENT
UNDER TEST
CONFIGURATION
VERIFICATION

PERFORMED BY: *Robert Lagan* C.P.I.
APPROVED BY: *[Signature]* 2/7/84 N.U.S.
APPROVED BY: *Michael [Signature]* 2/7/84 B.G.E.

8. AC POWER DISTRIBUTION/ INDICATOR PANEL AND POWER SUPPLY VALIDATION

The purpose of this test is to validate the operation of the the power supplies (040-5482, 040-5483, 040-5485, 040-5486, 040-5487, 040-5509); to validate the accuracy of the power supply to chassis cabling; to validate the functionality of the AC Power Distribution/ Indicator Panel (040-5511).

The validation of the AC Distribution/ Indicator Panel is accomplished by validating the presence of contact closures at the circuit breaker indicator points with a multimeter, then applying AC power and validating the presence of AC voltage at the AC power distribution receptacles with a AC power receptacle tester and the closure of the relay contacts indicating the presence of the AC power with a multimeter. Then one of the circuit breakers is turned off and the presence or absence of AC voltage at the appropriate distribution receptacles will be validated. This is then repeated for the other circuit.

The validation of the power supplies is accomplished by measuring the voltages at the voltage inputs to the I/O controllers in the cabinet subsystem under test with a digital multimeter and validating that the measured voltage is within the specifications of the power supply plus a tolerance for voltage loss in the length of the power supply to chassis cabling.

(Note that in this section and other sections of the procedure, the individual power supplies of the redundant power supply assemblies are differentiated with the designations 'A' and 'B' which are not to be confused with unit subdivisions 'Channel A' and 'Channel B'.)

AC PWER DISTRIBUTION/ INDICATOR PANEL VALIDATION

- 8.1 Remove all AC power plugs from the distribution receptacles of the AC Power Distribution/ Indicator Panel.
- 8.2 Turn both circuit breakers (S1 and S2) ON.
- 8.3 Using the digital multimeter, validate the presence of contact closures (less than one ohm resistance) between the following points:
 - TB3-3 to TB3-4 (Circuit Breaker A)
 - TB3-8 to TB3-9 (Circuit Breaker B)
- 8.4 Using the digital multimeter, validate the absence of contact closures (more than one megaohm resistance) between the following points:
 - TB3-1 to TB3-2 (AC Monitor Relay A)
 - TB3-6 to TB3-7 (AC Monitor Relay B)

8.5 Plug power cord 'A' (connected to the AC Distribution/ Indicator Panel) into a source of AC power.

8.6 Using the digital multimeter, validate the presence of contact closures (less than one ohm resistance) between the following points:

TB3-1 to TB3-2 (AC Monitor Relay A)
TB3-3 to TB3-4 (Circuit Breaker A)
TB3-8 to TB3-9 (Circuit Breaker B)

8.7 Using the digital multimeter, validate the absence of contact closures (more than one megaohm resistance) between the following points:

TB3-6 to TB3-7 (AC Monitor Relay B)

8.8 Plug power cord 'B' (connected to the AC Distribution/ Indicator Panel) into a source of AC power.

8.9 Using the digital multimeter, validate the presence of contact closures (less than one ohm resistance) between the following points:

TB3-1 to TB3-2 (AC Monitor Relay A)
TB3-3 to TB3-4 (Circuit Breaker A)
TB3-6 to TB3-7 (AC Monitor Relay B)
TB3-8 to TB3-9 (Circuit Breaker B)

8.10 Plug power cord 'C' (connected to the AC Distribution/ Indicator Panel) into a source of AC power.

8.11 Using the AC power receptacle tester, validate that the AC power at all receptacles (J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, and J12) is ON (indicates 'CORRECT WIRING').

8.12 Turn the 'A' circuit breaker (S1) OFF. Validate that the AC power is ON or OFF (no lamps lighted on tester) at the receptacles per the following table:

J1 OFF	J2 OFF	J3 OFF	J4 OFF
J5 ON	J6 ON	J7 ON	J8 ON
J9 ON	J10 ON	J11 ON	J12 ON

8.13 Turn the 'A' circuit breaker (S1) ON and the 'B' circuit breaker (S2) OFF. Validate that the AC power is ON or OFF at the receptacles per the following table:

J1 ON	J2 ON	J3 ON	J4 ON
J5 ON	J6 ON	J7 ON	J8 ON
J9 OFF	J10 OFF	J11 OFF	J12 OFF

8.14 Turn both circuit breakers OFF. Validate that the AC power is ON or OFF at the receptacles per the following table:

J1 OFF	J2 OFF	J3 OFF	J4 OFF
J5 ON	J6 OFF	J7 OFF	J8 OFF
J9 OFF	J10 OFF	J11 OFF	J12 OFF

8.15 Install the AC power plugs into the AC Distribution/ Indicator Panel per Attachment 2.

8.16 Validate that the cabinet blower is operational.

8.17 Turn both circuit breakers ON.

AC DISTRIBUTION/
INDICATOR PANEL
VALIDATION

PERFORMED BY: *Robert Leggs* C.P.I.

WITNESSED BY: *[Signature]* N.U.S.

If a non-conformance is noted during the validation of the AC Distribution/ Indicator Panel, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the AC Distribution/ Indicator Panel will be repeated (steps 8.2 to 8.17).

+15 VOLT POWER SUPPLY VALIDATION

8.19 Using the digital multimeter, validate that the +15VDC at each of the I/O controllers (terminal block points 6 (ground) and 7 (+15 volts)) wired for +15 volts per Attachment 2 measures +(14.7 : 15.3) volts. Record the chassis ID number and voltage below:

CHASSIS ID NO.:	<u>I[-15]</u>	VOLTAGE:	<u>15.09V</u>	INITIALS:	<u>RL /</u>
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____

+15 VOLT POWER SUPPLY VALIDATION PERFORMED BY: [Signature] C.P.I.
WITNESSED BY: [Signature] N.U.S.

If a non-conformance is noted during the validation of the +15 Volt Power Supply, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the +15 Volt Power Supply will be repeated (step 8.19).

-15 VOLT POWER SUPPLY VALIDATION

8.20 Using the digital multimeter, validate that the -15VDC at each of the I/O controllers (terminal block points 8 (ground) and 9 (-15 volts)) wired for -15 volts per Attachment 2 measures -(14.7 : 15.3) volts. Record chassis ID number and voltage below:

CHASSIS ID NO.:	<u>II-1F1</u>	VOLTAGE:	<u>-15.11</u>	INITIALS:	<u>RL /</u>
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____
CHASSIS ID NO.:	_____	VOLTAGE:	_____	INITIALS:	____/____

-15 VOLT
POWER SUPPLY
VALIDATION

PERFORMED BY: Robert Leger C.P.I.
WITNESSED BY: [Signature] N.U.S.

If a non-conformance is noted during the validation of the -15 Volt Power Supply, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the -15 Volt Power Supply will be repeated (step 8.20).

125 VOLT POWER SUPPLY VALIDATION

8.21 Using the digital multimeter, validate that the 125VDC at the power supply assembly (040-5509; (terminal blocks TB 4 (+125 volts) points 1-8 and TB 5 (ground) points 1-8) measure +(112.5 : 137.5) volts. Record the voltage below:

TB4-1/TB5-1:	VOLTAGE: _____	INITIALS: <u>N/A /</u>
TB4-2/TB5-2:	VOLTAGE: _____	INITIALS: _____/_____
TB4-3/TB5-3:	VOLTAGE: _____	INITIALS: _____/_____
TB4-4/TB5-4:	VOLTAGE: _____	INITIALS: _____/_____
TB4-5/TB5-5:	VOLTAGE: _____	INITIALS: _____/_____
TB4-6/TB5-6:	VOLTAGE: _____	INITIALS: _____/_____
TB4-7/TB5-7:	VOLTAGE: _____	INITIALS: _____/_____
TB4-8/TB5-8:	VOLTAGE: _____	INITIALS: _____/_____

125 VOLT
POWER SUPPLY
VALIDATION

PERFORMED BY: N/A *Robert Legh* C.P.I.

WITNESSED BY: *[Signature]* N.U.S.

IF a non-conformance is noted during the validation of the 125 Volt Power Supply, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the 125 Volt Power Supply will be repeated (step 8.21).

9. OPTICALLY ISOLATED DIGITAL INPUT MODULE VALIDATION

The purpose of this test is to validate the operation of the Optically Isolated Digital Input modules (021-5230) and their associated signal conditioning circuits (038-5098) and to validate the accuracy of the input module to signal conditioning module cabling (040-5456) and the signal conditioning module to terminal strip cabling (040-5519).

This validation is accomplished by using a control panel to control a relay output module in a test I/O controller to simulate 'contacts' on the terminal strip which sources the input module. The simulated data is monitored by a second control panel connected to the I/O controllers in the cabinet under test. (Reference Figure I of Attachment 1)

- 9.1 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.
- 9.2 Connect the 'Digital Test Cable' (000-7080) between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/Connector Adapter'.
- 9.3 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, and WAIT TEST UP

COMMAND WORD : to select random mode, disable interrupts, and to address the 'Special Relay Output Module' (address '0')

INSTRUCTION RATE : 50K range - vernier midrange

- 9.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Optically Isolated Digital Input Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, WAIT TEST and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50K range - vernier midrange

9.5 RESET both control panels.

9.6 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #1, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #1. Validate the operation of each bit.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

9.7 Repeat steps 9.1 to 9.6 for all Optically Isolated Digital Input Modules in the cabinet under test.

OPTICALLY ISOLATED DIGITAL INPUT VALIDATION PERFORMED BY: Red Lopez N/A C.F.I
 WITNESSED BY: [Signature] N.U.S

If a non-conformance is noted during the Optically Isolated Digital Input Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the O.I.D.I. will be repeated on the module/ cable set where the non-conformance was noted.

10. OPTICALLY ISOLATED DIGITAL INPUT MODULE SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate a sample of the surge withstand capability provided by the signal conditioning modules (038-5098) by simulating contacts on the input terminal; to the digital input module under test, then applying a surge to the inputs while monitoring the data input from the module under test with a control panel to validate that no data changes during the application of the surge. Each bit of the module tested will then be revalidated for functionality as per Section 9. (Reference Figure 2 of Attachment 1)

- 10.1 Select a sample of up to five percent or at least one of the surge protected Optically Isolated Digital Input Modules (021-5230 / 038-5098) in the cabinet under test to have the surge withstand capability tested.
- 10.2 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.
- 10.3 Connect the 'Digital Input Surge Test Connector' (000-7078) to the 'BTSCA to Test Cable/Connector Adapter'. Connect the red lead of the surge transient generator cable to the test connector. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.
- 10.4 Configure Control Panel #2 as follows:
 - DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Optically Isolated Digital Input Module under test per Attachment 2, Section 6, and Appendix B.
 - INSTRUCTION SELECT : COM, WAIT TEST and IN UP
 - COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.
 - INSTRUCTION RATE : 50K range - vernier midrange
- 10.5 RESET Control Panel #2.
- 10.6 Ready the surge transient generator to output a surge per Appendix D.

10.7 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

10.8 Repeat steps 10.2 to 10.7 on all of the Optically Isolated Digital Input modules in the selected sample.

10.9 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment: 2.

10.10 Connect the 'Digital Test Cable' (000-7080) between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/Connector Adapter'.

10.11 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Optically Isolated Digital Input Module under test per Attachment 2, Section 3, and Appendix B.

INSTRUCTION SELECT : COM, WAIT TEST and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50K range - vernier midrange

10.12 RESET both control panels.

10.13 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #1, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #1. Validate the operation of each bit.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

10.14 Repeat steps 10.9 to 10.13 for each of the Optically Isolated Digital Input Modules selected for surge withstand capability testing.

OPTICALLY ISOLATED	PERFORMED BY:	<u>Robert Lopez</u>	N/A	C.P.I.
DIGITAL INPUT	APPROVED BY:	<u>[Signature]</u>		N.U.S.
SURGE WITHSTAND	APPROVED BY:	<u>[Signature]</u>		N.U.S.
CAPABILITY	APPROVED BY:	<u>[Signature]</u>		N.U.S.
VALIDATION	APPROVED BY:	<u>NOT AVAILABLE</u>		B.G.E.

If a non-conformance is noted during the Optically Isolated Digital Input Surge Withstand Capability Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Optically Isolated Digital Input Surge Withstand Capability will be repeated on the module/ cabling set where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one, of the Optically Isolated Digital Inputs with surge protection will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

II. CHANGE OF STATE DIGITAL INPUT VALIDATION

The purpose of this test is to validate the operation of the Change of State Digital Input modules (038-5064) and their associated signal conditioning circuits (038-5099) and to validate the accuracy of the input module to signal conditioning module cabling (040-5456) and the signal conditioning module to terminal strip cabling (040-5519).

This validation is accomplished by using a control panel to control a relay output module in a test I/O controller to simulate 'contacts' on the terminal strip which sources the input module. The simulated data is monitored by a second control panel connected to the I/O controllers in the cabinet under test. (Reference Figure 3 of Attachment 1)

11.1 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

11.2 Connect the 'Digital Test Cable' (000-7080) between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/Connector Adapter'.

11.3 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, and WAIT TEST UP

COMMAND WORD : to select random mode, disable interrupts, and to address the 'Special Relay Output Module' (address '0')

INSTRUCTION RATE : 50K range - vernier midrange

11.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Change of State Digital Input Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, INT QRY, and IN UP,
WAIT INT DOWN

COMMAND WORD : to select random mode, enable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50 range - vernier midrange

11.5 RESET both control panels.

11.6 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #1, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #1. Validate that the interrupt request display of Control Panel #2 flashes ON then OFF when a bit is toggled. Validate that the interrupt vector displayed corresponds to the controller first device address and the module slot address. Validate the operation of each bit.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

11.7 Repeat steps 11.1 to 11.6 for all Change of State Digital Input modules in the cabinet under test.

CHANGE OF STATE
 DIGITAL INPUT
 VALIDATION

PERFORMED BY: N/A/ Palatka C.P.I.

WITNESSED BY: [Signature] N.U.S.

If a non-conformance is noted during the Change of State Digital Input Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the C.O.S.D.I. will be repeated on the module/ cabling set where the non-conformance was noted.

12. CHANGE OF STATE DIGITAL INPUT MODULE SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate a sample of the surge withstand capability provided by the signal conditioning modules (03C-5099) by simulating contacts on input terminals to the digital input module under test, then applying a surge to the inputs while monitoring the data input from the module under test with a control panel to validate that no data shall change during the application of the surge. Each bit of the module tested will then be revalidated for functionality as per Section 11. (Reference Figure 4 of Attachment 1)

- 12.1 Select a sample of up to five percent or at least one of the surge protected Change of State Digital Input modules (038-5064 / 038-5099) in the cabinet under test to have the surge withstand capability tested.
- 12.2 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.
- 12.3 Connect the 'Digital Input Surge Test Connector' (000-7078) to the 'BTSCA to Test Cable/Connector Adapter'. Connect the red lead of the surge transient generator cable to the test connector. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.
- 12.4 Configure Control Panel #2 as follows:
- DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Change of State Digital Input Module under test per Attachment 2, Section 6, and Appendix B.
- INSTRUCTION SELECT : COM, INT QRY, and IN UP,
WAIT INT DOWN
- COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.
- INSTRUCTION RATE : 50K range - vernier midrange
- 12.5 RESET Control Panel #2.
- 12.6 Ready the surge transient generator to output a surge per Appendix D.

12.7 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____

12.8 Repeat steps 12.2 to 12.7 on all of the Change Of State Digital Input modules in the selected sample.

12.9 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

12.10 Connect the 'Digital Test Cable' (000-7080) between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/Connector Adapter'.

12.11 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Change of State Digital Input Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, INT QRY, and IN UP,
 WAIT INT DOWN

COMMAND WORD : to select random mode, enable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50 range ~ vernier midrange

12.12 RESET both control panels.

12.13 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #1, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #1. Validate that the interrupt request display of Control Panel #2 flashes on then off when a bit is toggled. Validate that the interrupt vector displayed corresponds to the controller first device address and the module slot address. Validate the operation of each bit.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	<u>N/A</u> / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____

12.14 Repeat steps 12.9 to 12.13 on the Change of State Digital Input modules selected for surge withstand capability testing.

CHANGE OF STATE	PERFORMED BY:	<u>N/A</u> <i>Robert Jegan</i>	C.P.I.
DIGITAL INPUT	APPROVED BY:	<i>[Signature]</i>	N.U.S.
SURGE WITHSTAND	APPROVED BY:	<u>NOT AVAILABLE</u>	B.G.E.
CAPABILITY			
VALIDATION			

If a non-conformance is noted during the Change of State Digital Input Surge Withstand Capability Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Change of State Digital Input Surge Withstand Capability will be repeated on the module/ cabling set where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one, of the Change of State Digital Input with surge protection will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

13. QUAD PULSE COUNTER MODULE VALIDATION

The purpose of this test is to validate that the Quad Pulse Counter modules (021-5278) and their associated signal conditioning circuits (038-5099) are operational and to validate the accuracy of the counter module to signal conditioning module cabling (040-5517) and the signal conditioning module to terminal strip cabling (040-5519).

This is accomplished by using a control panel to control a relay output module in a test I/O controller to simulate 'contacts' pulses on the terminal strip which sources the input module. The simulated data is monitored by a second control panel connected to the I/O controllers in the cabinet under test. (Reference Figure 5 of Attachment I)

- 13.1 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.
- 13.2 Connect the 'Digital Test Cable' (000-7080) between the 'Special Pulsing Relay Output Module' (000-7067) in the test I/O controller (slot 7) and the 'BTSCA to Test Cable/Connector Adapter'.
- 13.3 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the 'Special Pulsing Relay Output Module' (address '1')

INSTRUCTION RATE : 50 range - vernier midrange

OUTPUT WORD : '0000 0000 0000 0000'

- 13.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Quad Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

- 13.5 RESET both control panels.
- 13.6 Initialize the four counters of the module under test to zero counts from the Output Word of Control Panel #2. Set the Output Word to all zeros.
- 13.7 Validate that counter #0 (Data Word Display of Control Panel #2) indicates a count of zero (all LEDs OFF).
- 13.8 Select counter #1 from Control Panel #2 Output Word and validate that counter #1 indicates a count of zero.
- 13.9 Select counter #2 and validate that counter #2 indicates a count of zero.
- 13.10 Select counter #3 and validate that counter #3 indicates a count of zero.
- 13.11 Select counter #0 from Control Panel #2 Output Word.
- 13.12 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #0 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.
- 13.13 Validate that the Data Word Display of Control Panel #2 increments. Using the Output Word of Control Panel #2, select counters #1, #2, and #3 and validate that these counters are not incrementing.
- 13.14 Reset the bit set in the Output Word of Control Panel #1.
- 13.15 Select counter #1.
- 13.16 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #1 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.
- 13.17 Validate that counter #1 increments. Validate that counters #0, #2, and #3 do not increment.
- 13.18 Reset the bit set in the Output Word of Control Panel #1.
- 13.19 Select counter #2.
- 13.20 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #2 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.

- 13.21 Validate that counter #2 increments. Validate that counters #0, #1, and #3 do not increment.
- 13.22 Reset the bit set in the Output Word of Control Panel #1.
- 13.23 Select counter #3.
- 13.24 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #3 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.
- 13.25 Validate that counter #3 increments. Validate that counters #0, #1, and #2 do not increment.
- 13.26 Reset the bit set in the Output Word of Control Panel #1.

HOOD of 040-5517 PI/SCM CABLE on MODULE UNDER TEST	COUNTER NUMBER			
	#0	#1	#2	#3
HOOD P1	0	1	2	3
HOOD P2	4	5	6	7
HOOD P3	8	9	10	11
HOOD P4	12	13	14	15

Output Word bit set on Control Panel #1 to control pulsing relay

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

- 13.27 Repeat steps 13.1 to 13.26 for all Quad Pulse Counter modules in the cabinet under test.

QUAD PULSE COUNTER MODULE VALIDATION PERFORMED BY: N/A [Signature] C.P.I.
 WITNESSED BY: [Signature] N.U.S.

If a non-conformance is noted during the Quad Pulse Counter Module Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Quad Pulse Counters will be repeated on the module/ cabling set where the non-conformance was noted.

14 QUAD PULSE COUNTER MODULE SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate a sample of the surge withstand capability provided by the signal conditioning modules (038-5099) by applying a surge to the terminals that source the input module while monitoring the data input from the module under test with a control panel to validate that the data shall not change during the application of the surge. The module tested will then be revalidated for functionality as per Section 13. (Reference Figure 6 of Attachment 1)

- 14.1 Select a sample of up to five percent or at least one of the surge protected Quad Pulse Counter Modules (021-5278 / 038-5099) in the cabinet to have the surge withstand capability tested.
- 14.2 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.
- 14.3 Connect the 'Pulse Counter Surge Test Connector' (000-7097) to the 'BTSCA to Test Cable/Connector Adapter'. Connect the red lead of the surge transient generator cable to the point on the test connector marked with the number on the hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) installed on the module to be tested. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.

14.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Quad Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

- 14.5 RESET Control Panel #2.
- 14.6 Initialize the four counters of the module under test to zero counts from the Output Word of Control Panel #2. Validate that counters #0, #1, #2, and #3 all indicate counts of zero.

- 14.7 Ready the surge transient generator to output a surge per Appendix D.
- 14.8 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.
- 14.9 Validate that counters #0, #1, #2, and #3 all indicate counts of zero.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

- 14.10 Repeat steps 14.2 to 14.9 on all of the Quad Pulse Counter modules in the selected sample.
- 14.11 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.
- 14.12 Connect the 'Digital Test Cable' (000-7080) between the 'Special Pulsing Relay Output Module' (000-7067) in the test I/O controller (slot 7) and the 'BTSCA to Test Cable/Connector Adapter'.
- 14.13 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Quad Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

- 14.14 RESET both control panels.

- 14.15 Select counter #0 from Control Panel #2 Output Word.
- 14.16 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #0 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.
- 14.17 Validate that the Data Word Display of Control Panel #2 increments.
- 14.18 Reset the bit set in the Output Word of Control Panel #1.
- 14.19 Select counter #1.
- 14.20 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #1 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.
- 14.21 Validate that counter #1 increments.
- 14.22 Reset the bit set in the Output Word of Control Panel #1.
- 14.23 Select counter #2.
- 14.24 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #2 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.
- 14.25 Validate that counter #2 increments.
- 14.26 Reset the bit set in the Output Word of Control Panel #1.
- 14.27 Select counter #3.
- 14.28 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #3 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.
- 14.29 Validate that counter #3 increments.
- 14.30 Reset the bit set in the Output Word of Control Panel #1.

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
 BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
 at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

HOOD of 040-5517 PI/SCM CABLE on MODULE UNDER TEST	COUNTER NUMBER			
	#0	#1	#2	#3
HOOD P1	0	1	2	3
HOOD P2	4	5	6	7
HOOD P3	8	9	10	11
HOOD P4	12	13	14	15

Output Word bit set on
Control Panel #1 to
control pulsing relay

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____

14.31 Repeat steps 14.11 to 14.30 on the Quad Pulse Counter modules selected for surge withstand capability testing.

QUAD PULSE	PERFORMED BY:	<u>N/A Robert Lopez</u>	C.P.I.
COUNTER SURGE	APPROVED BY:	<u>[Signature]</u>	N.U.S.
WITHSTAND	APPROVED BY:	<u>NOT AVAILABLE</u>	B.G.E.
CAPABILITY			
VALIDATION			

If a non-conformance is noted during the Quad Pulse Counter Surge Withstand Capability Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Quad Pulse Counter Surge Withstand Capability will be repeated on the module/ cabling set where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one, of the Quad Pulse Counters with surge protection will be selected and tested. This will be repeated if an another non-conformance is identified in the second sample.

15. UP/DOWN PULSE COUNTER MODULE VALIDATION

The purpose of this test is to validate that the Up/Down Pulse Counter Modules (038-5115) and their associated signal conditioning circuits (038-5099) are operational and to validate the accuracy of the counter module to signal conditioning module cabling (040-5456 or 040-5518) and the signal conditioning module to terminal strip cabling (040-5519).

This is accomplished by using a control panel to control a relay output module in a test I/O controller to simulate 'contact' pulses on the terminal strip which sources the counter module. The simulated data is monitored by a second control panel connected to the I/O controllers in the cabinet under test. (Reference Figure 7 of Attachment 1)

Note that the 'Channel A' Up/Down Pulse Counters are configured differently than the 'Channel B' Up/Down Pulse Counters. The 'Channel B' counters have their 16 inputs conditioned/ sourced by one signal conditioning module/ terminal strip. The 'Channel A' counters have their 16 inputs conditioned/ sourced by two signal conditioning modules/ terminal strips (the UP, DOWN, and SET inputs by one SCM/TS, and the RESET inputs by another SCM/TS).

Also note that the counters can be set to a count determined by a customer selected configuration of diodes on the module. The modules are normally factory configured for a count of zero. This creates a problem in testing in that the SET input yields the same count as the RESET input. For the purpose of this acceptance test, the modules are configured to give counts of 119 (decimal) ('01110111' binary), 187 (decimal) ('10111011' binary), 221 (decimal) ('11011101' binary), and 238 (decimal) ('11101110' binary) for counters #0, #1, #2, and #3 respectively on a SET input. Prior to shipment, the normal factory configured diodes will be installed on the modules.

15.1 Install the 'BTSCA to Test Cable/ Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2 for 'Channel B' counters or on each of the selected BTSCAs for the 'Channel A' counters.

15.2 Connect the 'Digital Test Cable' (000-7080) between the 'Special Pulsing Relay Output Module' (000-7067) in the test I/O controller (slot 7) and the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA for 'Channel B' counters or on the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the UP, DOWN, and SET inputs to the 'Channel A' counters. For 'Channel A' counters, connect a second 'Digital Test Cable' between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the RESET inputs to the 'Channel A' counters.

15.3 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable
interrupts, and to address the
'Special Pulsing Relay Output Module'
(address '1')

INSTRUCTION RATE : 50 range - vernier midrange

OUTPUT WORD : '0000 0000 0000 0000'

15.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the
I/O Controller containing the Up/Down
Pulse Counter Module under test per
Attachment 2, Section 6, and
Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable
interrupts, and to address the module
under test using Attachment 2,
Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

15.5 RESET both control panels.

15.6 Set the counter #0 of the module under test to a count of
'10000000' (binary) from the Output Word of Control Panel #2.

15.7 Validate that counter #0 indicates a count of '10000000' in the
Data Word Display of Control Panel #2.

15.8 Set counter #1 to a count of '10000000' .

15.9 Validate that counter #1 indicates a count of '10000000' .

15.10 Set counter #2 to a count of '10000000' .

15.11 Validate that counter #2 indicates a count of '10000000' .

15.12 Set counter #3 to a count of '10000000' .

15.13 Validate that counter #3 indicates a count of '10000000' .

For 'Channel A' Up/Down Pulse Counters, proceed with steps 15.14 to 15.31, then continue with step 15.48 .

For 'Channel B' Up/Down Pulse Counters, proceed with steps 15.32 to 15.47, then continue with step 15.48 .

'CHANNEL A' COUNTERS ONLY (15.14 to 15.31)

- 15.14 Set the COMMAND WORD of Control Panel #1 to address the 'Special Relay Output Module' (address '0').
- 15.15 Select counter #0 from Control Panel #2 Output Word.
- 15.16 Set bit 0, 4, 8, or 12, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #0.
- 15.17 Reset the bit set in the Output Word of Control Panel #1.
- 15.18 Validate that counter #0 indicates a count of '00000000' in the Data Word Display of Control Panel #2.
- 15.19 Select counter #1 from Control Panel #2 Output Word.
- 15.20 Set bit 1, 5, 9, or 13, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #1.
- 15.21 Reset the bit set in the Output Word of Control Panel #1.
- 15.22 Validate that counter #1 indicates a count of '00000000' in the Data Word Display of Control Panel #2.
- 15.23 Select counter #2 from Control Panel #2 Output Word.
- 15.24 Set bit 2, 6, 10, or 14, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #2.
- 15.25 Reset the bit set in the Output Word of Control Panel #1.
- 15.26 Validate that counter #2 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

- 15.27 Select counter #3 from Control Panel #2 Output Word.
- 15.28 Set bit 3, 7, 11, or 15, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #3.
- 15.29 Reset the bit set in the Output Word of Control Panel #1.
- 15.30 Validate that counter #3 indicates a count of '00000000' in the Data Word Display of Control Panel #2.
- 15.31 Set the COMMAND WORD of Control Panel #1 to address the 'Special Pulsing Relay Output Module' (address '1').

POSITION OF MODULE ON 040-5518 CABLE	COUNTER #				
	0	1	2	3	
FIRST CARD	0	1	2	3	Output Word bit set on Control Panel #1 to control pulsing relay on RESET inputs of Channel A counters
SECOND CARD	4	5	6	7	
THIRD CARD	8	9	10	11	
FOURTH CARD	12	13	14	15	

'CHANNEL B' COUNTERS ONLY (15.32 to 15.47)

- 15.32 Select counter #0 from Control Panel #2 Output Word.
- 15.33 Set bit 2 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #0.
- 15.34 Reset the bit set in the Output Word of Control Panel #1.
- 15.35 Validate that counter #0 indicates a count of '00000000' in the Data Word Display of Control Panel #2.
- 15.36 Select counter #1 from Control Panel #2 Output Word.
- 15.37 Set bit 6 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #1.
- 15.38 Reset the bit set in the Output Word of Control Panel #1.
- 15.39 Validate that counter #1 indicates a count of '00000000' .
- 15.40 Select counter #2 from Control Panel #2 Output Word.
- 15.41 Set bit 10 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #2.
- 15.42 Reset the bit set in the Output Word of Control Panel #1.
- 15.43 Validate that counter #2 indicates a count of '00000000' .
- 15.44 Select counter #3 from Control Panel #2 Output Word.
- 15.45 Set bit 14 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #3.
- 15.46 Reset the bit set in the Output Word of Control Panel #1.
- 15.47 Validate that counter #3 indicates a count of '00000000' .

'CHANNEL A' and 'CHANNEL B' COUNTERS

- 15.48 Select counter #0 from Control Panel #2 Output Word.
- 15.49 Set bit 3 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #0.
- 15.50 Reset the bit set in the Output Word of Control Panel #1.
- 15.51 Validate that counter #0 indicates a count of '01110111' in the Data Word Display of Control Panel #2.
- 15.52 Select counter #1 from Control Panel #2 Output Word.
- 15.53 Set bit 7 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #1.
- 15.54 Reset the bit set in the Output Word of Control Panel #1.
- 15.55 Validate that counter #1 indicates a count of '10111011' .
- 15.56 Select counter #2 from Control Panel #2 Output Word.
- 15.57 Set bit 11 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #2.
- 15.58 Reset the bit set in the Output Word of Control Panel #1.
- 15.59 Validate that counter #2 indicates a count of '11011101' .
- 15.60 Select counter #3 from Control Panel #2 Output Word.
- 15.61 Set bit 15 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #3.
- 15.62 Reset the bit set in the Output Word of Control Panel #1.
- 15.63 Validate that counter #3 indicates a count of '11101110' .

- 15.64 Select counter #0 from Control Panel #2 Output Word.
- 15.65 Set bit 0 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #0.
- 15.66 Validate that counter #0 (the Data Word Display of Control Panel #2) increments.
- 15.67 Reset the bit set in the Output Word of Control Panel #1.
- 15.68 Set bit 1 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #0.
- 15.69 Validate that counter #0 (the Data Word Display of Control Panel #2) decrements.
- 15.70 Reset the bit set in the Output Word of Control Panel #1.
- 15.71 Select counter #1 from Control Panel #2 Output Word.
- 15.72 Set bit 4 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #1.
- 15.73 Validate that counter #1 (the Data Word Display of Control Panel #2) increments.
- 15.74 Reset the bit set in the Output Word of Control Panel #1.
- 15.75 Set bit 5 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #1.
- 15.76 Validate that counter #1 (the Data Word Display of Control Panel #2) decrements.
- 15.77 Reset the bit set in the Output Word of Control Panel #1.

- 15.78 Select counter #2 from Control Panel #2 Output Word.
- 15.79 Set bit 8 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #2.
- 15.80 Validate that counter #2 (the Data Word Display of Control Panel #2) increments.
- 15.81 Reset the bit set in the Output Word of Control Panel #1.
- 15.82 Set bit 9 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #2.
- 15.83 Validate that counter #2 (the Data Word Display of Control Panel #2) decrements.
- 15.84 Reset the bit set in the Output Word of Control Panel #1.
- 15.85 Select counter #3 from Control Panel #2 Output Word.
- 15.86 Set bit 12 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #3.
- 15.87 Validate that counter #3 (the Data Word Display of Control Panel #2) increments.
- 15.88 Reset the bit set in the Output Word of Control Panel #1.
- 15.89 Set bit 13 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #3.
- 15.90 Validate that counter #3 (the Data Word Display of Control Panel #2) decrements.
- 15.91 Reset the bit set in the Output Word of Control Panel #1.

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MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

15.92 Repeat steps 15.1 to 15.91 for all Up/Down Counter modules in the cabinet.

UP/DOWN PULSE PERFORMED BY: N/A [Signature] C.P.I.
 COUNTER MODULE WITNESSED BY: [Signature] R.U.S.
 VALIDATION

If a non-conformance is noted during the Up/Down Pulse Counter Module Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Up/Down Pulse Counters will be repeated on the module/ cabling set where the non-conformance was noted.

16. UP/DOWN PULSE COUNTER MODULE SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate a sample of the surge withstand capability provided by the signal conditioning modules (038-5099) by applying a surge to the Up/Down Pulse Counter terminals that source the input modules while monitoring the data input from the module under test with a control panel to validate that the data shall not change during the application of the surge. The module tested will then be revalidated for functionality as per Section 15. [Reference Figure 8 of Attachment I]

- 16.1 Select a sample of up to five percent or at least one of the surge protected Up/Down Counter modules (038-5115 / 038-5099) in the cabinet to have the surge withstand capability tested.
- 16.2 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2 for 'Channel B' counters or on each of the selected BTSCAs for the 'Channel A' counters.
- 16.3 Connect the 'Digital Input Surge Test Connector' (000-7078) to the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA for 'Channel B' counters or on the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the UP, DOWN, and SET inputs to the 'Channel A' counters. For 'Channel A' counters, connect the 'Pulse Counter Surge Test Connector' (000-7097) to the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the RESET inputs to the 'Channel A' counters.
- 16.4 Connect the red lead of the surge transient generator cable to the 'Digital Input Surge Test Connector' on the BTSCA for 'Channel B' counters or on the BTSCA which sources the UP, DOWN, and SET inputs to the 'Channel A' counters. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.
- 16.5 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Up/Down Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

- 16.6 RESET Control Panel #2.
- 16.7 Set counter #0 of the module under test to a count of '10000000' (binary) from the Output Word of Control Panel #2.
- 16.8 Validate that counter #0 indicates a count of '10000000' in the Data Word Display of Control Panel #2.
- 16.9 Set counter #1 to a count of '10000000' .
- 16.10 Validate that counter #1 indicates a count of '10000000' .
- 16.11 Set counter #2 to a count of '10000000' .
- 16.12 Validate that counter #2 indicates a count of '10000000' .
- 16.13 Set counter #3 to a count of '10000000' .
- 16.14 Validate that counter #3 indicates a count of '10000000' .
- 16.15 Select counter #0.
- 16.16 Ready the surge transient generator to output a surge per Appendix D.
- 16.17 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.
- 16.18 Validate that counter #0 indicates a count of '10000000' in the Data Word Display of Control Panel #2.
- 16.19 Validate that counter #1 indicates a count of '10000000' .
- 16.20 Validate that counter #2 indicates a count of '10000000' .
- 16.21 Validate that counter #3 indicates a count of '10000000' .

PERFORM STEPS 16.22 TO 16.28 for 'CHANNEL A' COUNTERS ONLY

- 16.22 Connect the red lead of the surge transient generator cable to the 'Pulse Counter Surge Test Connector' on the BTSCA which sources the RESET inputs to the 'Channel A' counters. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.

- 16.23 Ready the surge transient generator to output a surge per Appendix D.
- 16.24 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.
- 16.25 Validate that counter #0 indicates a count of '10000000' in the Data Word Display of Control Panel #2.
- 16.26 Validate that counter #1 indicates a count of '10000000' .
- 16.27 Validate that counter #2 indicates a count of '10000000' .
- 16.28 Validate that counter #3 indicates a count of '10000000' .

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A	_____	_____	____/____
_____	_____	____/____	_____	_____	____/____
_____	_____	____/____	_____	_____	____/____
_____	_____	____/____	_____	_____	____/____
_____	_____	____/____	_____	_____	____/____

- 16.29 Repeat steps 16.2 to 16.28 (as applicable) on all of the Up/Down Pulse Counter modules in the sample selected.

16.30 Install the 'BTSCA to Test Cable/ Connector Adapter' (J00-7077) on the selected BTSCA in the cabinet under test per Attachment 2 for 'Channel B' counters or on each of the selected BTSCAs for the 'Channel A' counters.

16.31 Connect the 'Digital Test Cable' (000-7080) between the 'Special Pulsing Relay Output Module' (000-7067) in the test I/O controller (slot 7) and the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA for 'Channel B' counters or on the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the UP, DOWN, and SET inputs to the 'Channel A' counters. For 'Channel A' counters, connect a second 'Digital Test Cable' between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the RESET inputs to the 'Channel A' counters.

16.32 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the 'Special Pulsing Relay Output Module' (address '1')

INSTRUCTION RATE : 50 range - vernier midrange

OUTPUT WORD : '0000 0000 0000 0000'

16.33 Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Up/Down Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

- 16.34 RESET both control panels.
- 16.35 Set the counter #0 of the module under test to a count of '10000000' (binary) from the Output Word of Control Panel #2.
- 16.36 Validate that counter #0 indicates a count of '10000000' in the Data Word Display of Control Panel #2.
- 16.37 Set counter #1 to a count of '10000000' .
- 16.38 Validate that counter #1 (Data Word Display of Control Panel #2) indicates a count of '10000000' .
- 16.39 Set counter #2 to a count of '10000000' .
- 16.40 Validate that counter #2 (Data Word Display of Control Panel #2) indicates a count of '10000000' .
- 16.41 Set counter #3 to a count of '10000000' .
- 16.42 Validate that counter #3 (Data Word Display of Control Panel #2) indicates a count of '10000000' .

For 'Channel A' Up/Down Pulse Counters, proceed with steps 16.43 to 16.60, then continue with step 16.77 .

For 'Channel B' Up/Down Pulse Counters, proceed with steps 16.61 to 16.76, then continue with step 16.77 .

'CHANNEL A' COUNTERS ONLY (16.43 to 16.60)

- 16.43 Set the COMMAND WORD of Control Panel #1 to address the 'Special Relay Output Module' (address '0').
- 16.44 Select counter #0 from Control Panel #2 Output Word.
- 16.45 Set bit 0, 4, 8, or 12, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #0.
- 16.46 Reset the bit set in the Output Word of Control Panel #1.
- 16.47 Validate that counter #0 indicates a count of '00000000' in the Data Word Display of Control Panel #2.
- 16.48 Select counter #1 from Control Panel #2 Output Word.
- 16.49 Set bit 1, 5, 9, or 13, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #1.
- 16.50 Reset the bit set in the Output Word of Control Panel #1.
- 16.51 Validate that counter #1 indicates a count of '00000000' in the Data Word Display of Control Panel #2.
- 16.52 Select counter #2 from Control Panel #2 Output Word.
- 16.53 Set bit 2, 6, 10, or 14, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #2.
- 16.54 Reset the bit set in the Output Word of Control Panel #1.
- 16.55 Validate that counter #2 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

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- 16.56 Select counter #3 from Control Panel #2 Output Word.
- 16.57 Set bit 3, 7, 11, or 15, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #3.
- 16.58 Reset the bit set in the Output Word of Control Panel #1.
- 16.59 Validate that counter #3 indicates a count of '00000000' in the Data Word Display of Control Panel #2.
- 16.60 Set the COMMAND WORD of Control Panel #1 to address the 'Special Pulsing Relay Output Module' (address '1').

POSITION OF MODULE ON 040-5518 CABLE	COUNTER #				
=====+====+====+====+====	0	1	2	3	Output Word bit set on Control Panel #1 to control pulsing relay on RESET inputs of Channel A counters
FIRST CARD	0	1	2	3	
-----+-----+-----+-----+-----	4	5	6	7	
SECOND CARD	4	5	6	7	
-----+-----+-----+-----+-----	8	9	10	11	
THIRD CARD	8	9	10	11	
-----+-----+-----+-----+-----	12	13	14	15	
FOURTH CARD	12	13	14	15	

CHANNEL B COUNTERS ONLY (16.61 to 16.76)

- 16.61 Select counter #0 from Control Panel #2 Output Word.
- 16.62 Set bit 2 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #0.
- 16.63 Reset the bit set in the Output Word of Control Panel #1.
- 16.64 Validate that counter #0 indicates a count of '00000000' in the Data Word Display of Control Panel #2.
- 16.65 Select counter #1 from Control Panel #2 Output Word.
- 16.66 Set bit 6 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #1.
- 16.67 Reset the bit set in the Output Word of Control Panel #1.
- 16.68 Validate that counter #1 (Data Word Display of Control Panel #2) indicates a count of '00000000'.
- 16.69 Select counter #2 from Control Panel #2 Output Word.
- 16.70 Set bit 10 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #2.
- 16.71 Reset the bit set in the Output Word of Control Panel #1.
- 16.72 Validate that counter #2 (Data Word Display of Control Panel #2) indicates a count of '00000000'.
- 16.73 Select counter #3 from Control Panel #2 Output Word.
- 16.74 Set bit 14 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #3.
- 16.75 Reset the bit set in the Output Word of Control Panel #1.
- 16.76 Validate that counter #3 (Data Word Display of Control Panel #2) indicates a count of '00000000'.

'CHANNEL A' and 'CHANNEL B' COUNTERS

- 16.77 Select counter #0 from Control Panel #2 Output Word.
- 16.78 Set bit 3 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #0.
- 16.79 Reset the bit set in the Output Word of Control Panel #1.
- 16.80 Validate that counter #0 indicates a count of '01110111' in the Data Word Display of Control Panel #2.
- 16.81 Select counter #1 from Control Panel #2 Output Word.
- 16.82 Set bit 7 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #1.
- 16.83 Reset the bit set in the Output Word of Control Panel #1.
- 16.84 Validate that counter #1 (Data Word Display of Control Panel #2) indicates a count of '10111011' .
- 16.85 Select counter #2 from Control Panel #2 Output Word.
- 16.86 Set bit 11 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #2.
- 16.87 Reset the bit set in the Output Word of Control Panel #1.
- 16.88 Validate that counter #2 (Data Word Display of Control Panel #2) indicates a count of '11011101' .
- 16.89 Select counter #3 from Control Panel #2 Output Word.
- 16.90 Set bit 15 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #3.
- 16.91 Reset the bit set in the Output Word of Control Panel #1.
- 16.92 Validate that counter #3 (Data Word Display of Control Panel #2) indicates a count of '11101110' .

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- 16.93 Select counter #0 from Control Panel #2 Output Word.
- 16.94 Set bit 0 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #0.
- 16.95 Validate that counter #0 (Data Word Display of Control Panel #2) increments.
- 16.96 Reset the bit set in the Output Word of Control Panel #1.
- 16.97 Set bit 1 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #0.
- 16.98 Validate that counter #0 (Data Word Display of Control Panel #2) decrements.
- 16.99 Reset the bit set in the Output Word of Control Panel #1.
- 16.100 Select counter #1 from Control Panel #2 Output Word.
- 16.101 Set bit 4 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #1.
- 16.102 Validate that counter #1 (Data Word Display of Control Panel #2) increments.
- 16.103 Reset the bit set in the Output Word of Control Panel #1.
- 16.104 Set bit 5 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #1.
- 16.105 Validate that counter #1 (Data Word Display of Control Panel #2) decrements.
- 16.106 Reset the bit set in the Output Word of Control Panel #1.

- 16.107 Select counter #2 from Control Panel #2 Output Word.
- 16.108 Set bit 8 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #2.
- 16.109 Validate that counter #2 (Data Word Display of Control Panel #2) increments.
- 16.110 Reset the bit set in the Output Word of Control Panel #1.
- 16.111 Set bit 9 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #2.
- 16.112 Validate that counter #2 (Data Word Display of Control Panel #2) decrements.
- 16.113 Reset the bit set in the Output Word of Control Panel #1.
- 16.114 Select counter #3 from Control Panel #2 Output Word.
- 16.115 Set bit 12 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #3.
- 16.116 Validate that counter #3 (Data Word Display of Control Panel #2) increments.
- 16.117 Reset the bit set in the Output Word of Control Panel #1.
- 16.118 Set bit 13 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #3.
- 16.119 Validate that counter #3 (Data Word Display of Control Panel #2) decrements.
- 16.120 Reset the bit set in the Output Word of Control Panel #1.

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MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____

16.121 Repeat steps 16.30 to 16.120 on the remaining Up/Down Pulse Counters selected for surge withstand capability testing.

UP/DOWN PULSE	PERFORMED BY:	<u>N/A [Signature]</u>	C.P.I.
COUNTER MODULE	APPROVED BY:	<u>[Signature]</u>	N.U.S.
SURGE WITHSTAND	APPROVED BY:	<u>NOT AVAILABLE</u>	B.G.E.
CAPABILITY			
VALIDATION			

If a non-conformance is noted during the Up/Down Pulse Counter Surge Withstand Capability Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Up/Down Pulse Counter Surge Withstand Capability will be repeated on the module/ cabling set where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one, of the Up/Down Pulse Counters with surge protection will be selected and tested. This will be repeated if an another non-conformance is identified in the second sample.

17. DIGITAL and ANALOG LOOPBACK and CALIBRATION MODULE VALIDATION

The purpose of this test is to validate the operation of the different functional blocks of the Digital and Analog Loopback and Calibration modules (021-5271) where applicable; to validate the accuracy of the DALCAL module to terminal strip cabling (075-5271) where applicable; and to validate the functionality of the temperature transducer (559-5002) within the cabinet where applicable.

The Universal Analog to Digital Converter module (021-0211) is also validated when configured in a controller containing a DALCAL module.

The digital loopback functional block validation is accomplished by using a control panel to output data to the module under test and validating that the data input from the module echos the data output.

The analog loopback/ calibration functional block validation is accomplished by using a test computer system (see the CPI Description and Operating Instructions for the CPI Analog Input Test Computer and Programs) to run a test program to acquire analog data from the DALCAL / Universal A/D Converter module pair under test and validate the data acquired per data derived from the specifications of the Universal A/D Converter module (AE 021-0211) and the DALCAL module (AE 021-5271).

The temperature transducer monitoring functional block validation is accomplished by using the test computer system to run the test program to acquire analog data from the DALCAL / Universal A/D Converter module pair sensing the output of the temperature transducer. The test program displays the raw analog data and also converts the data to the corresponding temperature. The temperature measured is compared to the temperature measured by a digital thermometer and the data is validated per data derived from the specifications of the Universal A/D Converter module, the DALCAL module, the temperature transducer, and the test digital thermometer.

DALCAL MODULE DIGITAL LOOPBACK VALIDATION

17.1 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O controller containing the DALCAL Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

17.2 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #2, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #2. Validate the operation of each bit.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
II-1F1	10	RL/			/
		/			/

17.3 Repeat steps 17.1 to 17.2 for all DALCAL modules in the cabinet under test.

DALCAL MODULE DIGITAL LOOPBACK VALIDATION PERFORMED BY: Robert Logan C.P.I.
 WITNESSED BY: [Signature] N.U.S.

If a non-conformance is noted during the DALCAL module digital loopback validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the DALCAL module digital loopback will be repeated on the module where the non-conformance was noted.

DALCAL MODULE ANALOG LOOPBACK VALIDATION

- 17.4 Load the DALCAL module test program into the Analog Input Test Computer per the CPI Description and Operating Instructions for the Analog Input Test Computer.
- 17.5 Use information from the operating instructions, Attachment 2, Appendix C, Section 6, and the following steps to answer the program prompts to run the DALCAL test program on the DALCAL module / Analog to Digital Converter Module pair under test.
- 17.6 Run an offset test at gain code 0 for 100 scans and validate an offset within $(-0.050 \pm +0.050)V$.
- 17.7 Run an offset test at gain code 1 for 100 scans and validate an offset within $(-0.025 \pm +0.025)V$.
- 17.8 Run an offset test at gain code 2 for 100 scans and validate an offset within $(-0.0125 \pm +0.0125)V$.
- 17.9 Run an offset test at gain code 3 for 100 scans and validate an offset within $(-0.00625 \pm +0.00625)V$.
- 17.10 Run a positive full scale test at gain code 0 for 100 scans and validate a voltage within $(+9.950 \pm +10.050)V$.
- 17.11 Run a positive full scale test at gain code 1 for 100 scans and validate a voltage within $(+4.975 \pm +5.025)V$.
- 17.12 Run a positive full scale test at gain code 2 for 100 scans and validate a voltage within $(+2.4875 \pm +2.5125)V$.
- 17.13 Run a positive full scale test at gain code 3 for 100 scans and validate a voltage within $(+1.24375 \pm +1.25625)V$.
- 17.14 Run a negative full scale test at gain code 0 for 100 scans and validate a voltage within $(-9.950 \pm -10.050)V$.
- 17.15 Run a negative full scale test at gain code 1 for 100 scans and validate a voltage within $(-4.975 \pm -5.025)V$.
- 17.16 Run a negative full scale test at gain code 2 for 100 scans and validate a voltage within $(-2.4875 \pm -2.5125)V$.
- 17.17 Run a negative full scale test at gain code 3 for 100 scans and validate a voltage within $(-1.24375 \pm -1.25625)V$.

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MODULE PAIRS TESTED:

CHASSIS #	DALCAL / SLOT #	A.D.C SLOT #	INITIALS
<u>II-1F1</u>	<u>10</u>	<u>11</u>	<u>RV/</u>
_____	_____	_____	<u>/</u>
_____	_____	_____	<u>/</u>
_____	_____	_____	<u>/</u>

17.18 Repeat steps 17.5 to 17.17 on all DALCAL modules configured with Analog to Digital Converter cards in the cabinet under test.

DALCAL MODULE	PERFORMED BY: <u>Robert Legon</u>	C.P.I.
ANALOG LOOPBACK/ CALIBRATION	APPROVED BY: <u>[Signature]</u>	N.U.S.
VALIDATION	APPROVED BY: <u>NOT AVAILABLE</u>	B.G.E.

If a non-conformance is noted during the DALCAL module analog loopback validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the DALCAL module analog loopback will be repeated on the module where the non-conformance was noted.

DALCAL MODULE TEMPERATURE MONITORING VALIDATION

- 17.19 Using the Digital Thermometer, measure the temperature (in Celsius) at the temperature transducer (559-5002) monitored by the DALCAL module in the cabinet under test. Record the temperature measured below.
- 17.20 Use information from the operating instructions, Attachment 2, Appendix C, Section 7, and the following steps to answer the program prompts to run the DALCAL test program on the DALCAL modules configured to measure the cabinet temperature.
- 17.21 Run the system monitor test for 100 scans and validate that the DALCAL modules configured to measure cabinet temperature indicate a temperature within 3 degrees Celsius of the temperature measured with the digital thermometer.

MODULES TESTED:

CHASSIS # SLOT # INITIALS

II-1E1 10 RV/

CABINET TEMPERATURE USING DIGITAL THERMOMETER : 24°C

CABINET TEMPERATURE USING DALCAL : 23.973°C

CHASSIS # SLOT # INITIALS

_____ / _____

CABINET TEMPERATURE USING DIGITAL THERMOMETER : _____

CABINET TEMPERATURE USING DALCAL : _____

- 17.22 Repeat steps 17.19 to 17.21 on all DALCAL modules configured to measure cabinet temperature.

DALCAL MODULE
TEMPERATURE
MONITORING
VALIDATION

PERFORMED BY: Robert Logan C.P.I.

WITNESSED BY: [Signature] N.U.S.

If a non-conformance is noted during the DALCAL module temperature monitoring validation, the non-conformance will be dispositioned per Section I., the non-conformance will be corrected, and the validation of the DALCAL module temperature monitoring will be repeated on the module where the non-conformance was noted.

18. POWER SUPPLY MONITORING VALIDATION

The purpose of this test is to validate the gross operation of the analog input modules (02I-5234) monitoring cabinet power supplies and the RTD signal conditioning module power supplies; to validate the accuracy of the input module to terminal strip cabling (075-0053) and the terminal strip to power supply dividers or terminal strip to RTD SCM power supply cabling; and to validate the operation of the digital input module (02I-5227) monitoring the contact sense (125 Volt) power supply and the accuracy of the input module to terminal strip cabling (075-5227) and any other associated cabling.

The validation of the analog inputs monitoring the power supplies is accomplished by using the test computer system to run a test program to acquire analog data from the analog input gate module under test and validating that the data acquired represents voltages representative of the outputs from the power supply dividers. Then Each power supply will be powered down and the corresponding data must indicate a loss of power supply.

The validation of the digital inputs monitoring the contact sense (125 Volt) power supply is accomplished by using a control panel to monitor the digital input module under test, removing the source of 125 Volts to the module under test and validating that the appropriate digital bit changes state.

CABINET POWER SUPPLY MONITOR VALIDATION

- 18.1 Use information from the analog input test computer operating instructions, Attachment 2, Appendix C, Section 6, and the following steps to answer the program prompts to run the analog input test program on the analog input gate module that is wired to monitor cabinet power supplies.
- 18.2 Validate that the channels monitoring the +5 volt power supplies, where applicable, measure (4.0 : 6.0) volts.
- 18.3 Validate that the channels monitoring the +15 volt power supplies, where applicable, measure (4.0 : 6.0) volts.
- 18.4 Validate that the channels monitoring the -15 volt power supplies, where applicable, measure (-4.0 : -6.0) volts.
- 18.5 Validate that the channels monitoring the +125 volt power supplies, where applicable, measure (4.0 : 6.0) volts.

- 18.6 Unplug the 'A' power cord of the 5 volt power supply monitored by the analog input module under test, where applicable, from its AC panel.
- 18.7 Rerun the analog input test program and validate that the channel monitoring the 'A' 5 volt power supply indicates a voltage between (0.0 : 1.0) volts.
- 18.8 Reinstall the 'A' power cord in the AC panel and unplug the 'B' power cord.
- 18.9 Rerun the analog input test program and validate that the channel monitoring the 'B' 5 volt power supply indicates a voltage between (0.0 : 1.0) volts.
- 18.10 Reinstall the 'B' power cord in the AC panel.
- 18.11 Unplug the 'A' power cord of the +15 volt power supply monitored by the analog input module under test, where applicable, from its AC panel.
- 18.12 Rerun the analog input test program and validate that the channel monitoring the 'A' +15 volt power supply indicates a voltage between (0.0 : 1.0) volts.
- 18.13 Reinstall the 'A' power cord in the AC panel and unplug the 'B' power cord.
- 18.14 Rerun the analog input test program and validate that the channel monitoring the 'B' +15 volt power supply indicates a voltage between (0.0 : 1.0) volts.
- 18.15 Reinstall the 'B' power cord in the AC panel.
- 18.16 Unplug the 'A' power cord of the -15 volt power supply monitored by the analog input module under test, where applicable, from its AC panel.
- 18.17 Rerun the analog input test program and validate that the channel monitoring the 'A' -15 volt power supply indicates a voltage of between (0.0 : -1.0) volts.
- 18.18 Reinstall the 'A' power cord in the AC panel and unplug the 'B' power cord.
- 18.19 Rerun the analog input test program and validate that the channel monitoring the 'B' -15 volt power supply indicates a voltage of between (0.0 : -1.0) volts.
- 18.20 Reinstall the 'B' power cord in the AC panel.

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- 18.21 Unplug the 'A' power cord of the 125 volt power supply monitored by the analog input module under test, where applicable, from its AC panel.
- 18.22 Rerun the analog input test program and validate that the channel monitoring the 'A' 125 volt power supply indicates a voltage between (0.0 ± 1.0) volts.
- 18.23 Reinstall the 'A' power cord in the AC panel and unplug the 'B' power cord.
- 18.24 Rerun the analog input test program and validate that the channel monitoring the 'B' 125 volt power supply indicates a voltage between (0.0 ± 1.0) volts.
- 18.25 Reinstall the 'B' power cord in the AC panel.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
<u>II-1F1</u>	<u>17</u>	<u>RL /</u>	_____	_____	_____ / _____
_____	_____	_____ / _____	_____	_____	_____ / _____

- 18.26 Repeat steps 18.1 to 18.25 for all analog inputs in the cabinet wired to monitor cabinet power supplies.

CABINET
 POWER SUPPLY
 MONITORING
 VALIDATION

PERFORMED BY: *Robert Legon* C.P.I.
 WITNESSED BY: *BWIS* N.U.S.

If a non-conformance is noted during the cabinet power supply monitoring validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the cabinet power supply monitoring will be repeated on the module where the non-conformance was noted.

RTD SCM POWER SUPPLY MONITORING VALIDATION

- 18.27 Use information from the analog input test computer operating instructions, Attachment 2, Appendix C, Section 6, and the following steps to answer the program prompts to run the analog input test program on the analog input gate module that is wired to monitor RTD Signal Conditioning Module power supplies.
- 18.28 Validate that the channels monitoring RTD SCM power supplies, where applicable, measure (+9.9 : +10.1) volts.
- 18.29 Remove the first RTD signal conditioning module from its backplane connector with its hood still attached.
- 18.30 Allow thirty seconds or more to allow the filter capacitors of the analog input module monitoring the RTD SCM power supply to settle.
- 18.31 Rerun the analog input test program and verify that the channel monitoring the power supply of the RTD SCM removed from the backplane indicates a voltage of less than 1.0 volts.
- 18.32 Repeat steps 18.29 to 18.31 on each of the RTD SCMs monitored by the analog input module under test.
- 18.33 Unplug the power cord of the RTD signalling conditioning chassis from the AC panel and reinstall the RTD SCMs removed from the backplane then reinstall the power cord.

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MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A/	_____	_____	/
_____	_____	/	_____	_____	/

18.34 Repeat steps 18.27 to 18.33 for all analog inputs in the cabinet under test wired to monitor RTD SCM power supplies.

RTD SCM
 POWER SUPPLY
 MONITORING
 VALIDATION

PERFORMED BY:
 WITNESSED BY:

N/A Solatbey
BW B K

C.P.I.
 N.U.S.

If a non-conformance is noted during the RTD SCM power supply monitoring validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the RTD SCM power supply monitoring will be repeated on the module where the non-conformance was noted.

CONTACT SENSE VOLTAGE MONITORING VALIDATION

18.35 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O controller containing the digital input module monitoring the 125 volts under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, WAIT TEST, AND IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50K range - vernier midrange

18.36 RESET the control panel.

18.37 Validate that the bits, in the control panel Data Word Display, associated with the contact sense voltage are ON.

18.38 For input modules monitoring the contact sense voltage of 'Channel B' Up/ Down Pulse Counters, unplug both power cords of the 125 volt power supply supplying the contact sense voltage being monitored by the input module under test and validate that the bits, in the control panel data word display, associated these pulse counter modules are OFF.

18.39 For input modules monitoring the contact sense voltage of modules other than the 'Channel B' Up/ Down Pulse Counters, remove the hood from the 300/400 side of the signal conditioning module and validate that the bit associated with the module whose hood was disconnected is OFF. Repeat this for all modules monitored by the module under test.

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MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	N/A/	_____	_____	/
_____	_____	/	_____	_____	/

18.40 Repeat steps 18.35 to 18.39 for all digital inputs in the cabinet under test wired to monitor contact sense voltage.

CONTACT SENSE	PERFORMED BY:	<u>N/A Suletiga</u>	C.P.I.
MONITORING	WITNESSED BY:	<u>[Signature]</u>	N.O.S.
DIGITAL INPUT			
VALIDATION			

If a non-conformance is noted during the contact sense voltage monitoring validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the contact sense voltage monitoring will be repeated on the module where the non-conformance was noted.

19. VOLTAGE SENSING ANALOG INPUT GATE MODULE VALIDATION

The purpose of this test is to validate the gross operation of the Universal High Speed Wide Range Analog Input modules (021-5234) and their associated signal conditioning circuits (038-5097) and to validate the accuracy of the input module to signal conditioning module (040-5455) and the signal conditioning module to terminal strip (040-5520) or Uniform Temperature Reference Plate cabling (040-5522). It is not intended to validate the accuracy of the analog input cards.

This validation is accomplished by connecting a voltage divider network to the terminals sourcing the analog input module, and applying a voltage to the divider. Then data is read from the analog input module using the Analog Input Test Computer and test programs. This data is validated against a table of voltages derived from the divider network and the voltage applied. (Reference Figure 9 of Attachment 1)

- 19.1 Set the programmable DC voltage standard to zero volts.
- 19.2 Install the 'BTSCA to Test Cable/ Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test for those analog inputs terminated with BTSCAs.
- 19.3 Connect the Analog Input Test Divider/ Connector for BTSCAs (000-7081) to the BTSCA to Test Cable/ Connector Adapter for BTSCA terminated analog inputs. Connect the Analog Input Test Divider/ Connector for UTRPs (000-7085) to the UTRP terminals for UTRP terminated analog inputs.
- 19.4 Connect the output of the programmable DC voltage standard to the test divider inputs corresponding to the module under test.
- 19.5 Set the programmable DC voltage standard to +4.070 volts (voltage standard switch setting : 65C00 hexadecimal).
- 19.6 Use information from the analog input test computer operating instructions, Attachment 2, Appendix C, Section 6, and the following steps to answer the program prompts to run the analog input test program on the analog input gate module under test.
- 19.7 Run the Analog Input Test Program on the selected module for 100 scans at Gain Code 8. Validate that the mean voltages of each channel scanned are within the following voltages :

CH 0 = +(38 : 42) mV	CH 4 = +(18 : 22) mV
CH 1 = +(33 : 37) mV	CH 5 = +(13 : 17) mV
CH 2 = +(28 : 32) mV	CH 6 = +(8 : 12) mV
CH 3 = +(23 : 27) mV	CH 7 = +(3 : 7) mV

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MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
II-1F1	12	RL/			/
II-1F1	13	RL/			/
II-1F1	14	RL/			/
II-1F1	15	RL/			/
II-1F1	16	RL/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/

19.8 Repeat steps 19.1 to 19.7 for all analog input modules with voltage sense inputs in the cabinet under test.

ANALOG INPUT
(with voltage
sense inputs)
VALIDATION

PERFORMED BY: Robert Logan C.P.I.
WITNESSED BY: [Signature] N.U.S.

If a non-conformance is noted during the voltage sensing analog input module validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the voltage sense analog input monitoring will be repeated on the module where the non-conformance was noted.

20. VOLTAGE SENSING ANALOG INPUT GATE MODULE ACCURACY, COMMON MODE REJECTION, and SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate that the accuracy and common mode rejection of a sample of the analog to digital converter module/ analog input gate module (021-0211 / 021-5234) pairs and associated signal conditioning circuitry (038-5097) and cabling are within the published CPI specifications for the products being tested. Also validated is the surge withstand capability of this sample of the signal conditioning modules (038-5097). The drift/stability of this sample will also be validated in section 23.

The validation of the accuracy and common mode rejection are accomplished by using the analog input test computer to run the analog input test program to acquire data from the analog input module sets. First the module set will be run with zero common mode voltage to record the baseline noise on the inputs, then a common mode voltage source will be connected to the inputs to the gate module and the test program will be rerun to record the input noise with common mode voltage applied. The two runs will be compared and the difference between the baseline noise and the noise with common mode voltage applied must be less than specifications derived from the specifications of the module set. Then a precision voltage standard will be used to excite the inputs of the gate module in parallel and the test program will be run to record baseline offset in the channels then the precision voltage will be applied and the program will be rerun. The difference between the offset run and the voltage applied must be within specifications derived from the specifications of the module set. (Reference Figures 10 and 11 of Attachment 1)

The validation of the surge withstand capability is accomplished by simulating transducers with one kilohm resistors between the HIGH and LOW input terminals to the module. Then a surge is applied to one side of the resistors. Data is not acquired from the analog input module during the surge application. After the surge has been applied, the accuracy and common mode rejection of the module set will be retested to validate that the surge did not affect the performance of the module set. (Reference Figure 12 of Attachment 1)

- 20.1 Select up to five percent or at least one of the surge protected analog inputs modules with voltage sense BTSCA terminations in the cabinet to have common mode rejection, accuracy, surge withstand capability and drift/stability (in section 23.) validation performed on them.
- 20.2 Install the 'BTSCA to Test Cable/ Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.
- 20.3 Install the 'Analog Input Unbalanced Test Termination/ Connector' (000-7079) on the 'BTSCA to Test Cable/ Connector Adapter'.

- 20.4 Connect the output of the AC/DC V-A Source between the bussed inputs (red/high lead) corresponding to the module under test on the unbalanced test termination/ connector and the surge ground bus bar (black/low lead) in the cabinet under test.
- 20.5 With the AC/DC V-A source at zero volts, run the Analog Input Test Program on the selected module for 100 scans at Gain Code 8. This is to record the baseline noise on the channels of the module under test.
- 20.6 Set the AC/DC V-A source to 600 volts RMS (1697 V P-P), 60 HZ.
- 20.7 Run the Analog Input Test Program on the selected module for 100 scans at Gain Code 8. This is to record the increase in noise due to the common mode voltage not rejected.
- 20.8 Set the common mode voltage source to zero.
- 20.9 Validate that the peak to peak noise with the common mode voltage applied does not increase more than 2.7 millivolts for 021-5234-002 analog input gate modules, or more than 540 microvolts for 021-5234-003 analog input gate modules.
- 20.10 Set the programmable DC voltage standard to output zero volts.
- 20.11 Replace the 'Analog Input Unbalanced Test Terminator/ Connector' with the 'Analog Input Parallel Input Test Connector' (000-7082) on the 'BTSCA to Test Cable/ Connector Adapter'.
- 20.12 Connect the output of the programmable DC voltage standard to the input on the 'Analog Input Parallel Input Test Connector' corresponding to the module under test.
- 20.13 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.
- 20.14 With the programmable DC voltage standard at zero volts, run the Analog Input Test Program on the selected module for 100 scans at Gain Code 8. This is to record the baseline offset on the channels of the module under test.
- 20.15 Set the programmable DC voltage standard for +0.070 volts (programmable DC voltage standard setting : 01C00 hexadecimal).
- 20.16 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

- 20.17 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 8.
- 20.18 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.14 is within +(69.91 : 70.09) millivolts.
- 20.19 Set the programmable DC voltage standard for -0.070 volts.
- 20.20 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.
- 20.21 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 8.
- 20.22 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.14 is within -(69.91 : 70.09) millivolts.
- 20.23 Set the programmable DC voltage standard to output zero volts.
- 20.24 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.
- 20.25 Run the Analog Input Test Program on the selected module for 100 scans at Gain Code 4. This is to record the baseline offset on the channels of the module under test.
- 20.26 Set the programmable DC voltage standard for +0.560 volts (programmable DC voltage standard setting : 0E000 hexadecimal).
- 20.27 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.
- 20.28 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 4.
- 20.29 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.25 is within +(559.30 : 560.70) millivolts.
- 20.30 Set the programmable DC voltage standard for -0.560 volts.
- 20.31 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

- 20.32 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 4.
- 20.33 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.25 is within $-(559.30 : 560.70)$ millivolts.
- 20.34 Set the programmable DC voltage standard to output zero volts.
- 20.35 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.
- 20.36 Run the Analog Input Test Program on the selected module for 100 scans at Gain Code 0. This is to record the baseline offset on the channels of the module under test.
- 20.37 Set the programmable DC voltage standard for +8.960 volts (programmable DC voltage standard setting : E0000 hexadecimal).
- 20.38 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.
- 20.39 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 0.
- 20.40 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.36 is within $+(8.950 : 8.970)$ volts.
- 20.41 Set the programmable DC voltage standard for -8.960 volts.
- 20.42 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.
- 20.43 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 0.
- 20.44 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.36 is within $-(8.950 : 8.970)$ volts.
- 20.45 Set the programmable DC voltage standard to output zero volts.

- 20.46 Replace the 'Analog Input Parallel Input Test Connector' with the 'Analog Input Unbalanced Test Terminator/ Connector' on the 'BTSCA to Test Cable/ Connector Adapter'.
- 20.47 Connect the red lead of the surge transient generator cable to the the bussed inputs on the test connector corresponding to the module under test. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.
- 20.48 Ready the surge transient generator to output a surge per Appendix D.
- 20.49 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds.
- 20.50 Repeat steps 20.3 to 20.45 to validate that the module set under test continues to meet specifications.

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
 BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
 at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
IL-151	16	RV/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/

20.51 Repeat steps 20.2 to 20.50 on all of the modules in the selected sample.

VOLTAGE SENSING
 ANALOG INPUT
 COMMON MODE
 REJECTION,
 ACCURACY, and
 SURGE WITHSTAND
 VALIDATION

PERFORMED BY: Robert Lagon C.P.I.
 APPROVED BY: [Signature] N.U.S.
 APPROVED BY: NOT AVAILABLE B.G.E.

If a non-conformance is noted during the voltage sensing analog input common mode rejection, accuracy, and surge withstand capability validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the voltage sensing analog input common mode rejection, accuracy, and surge withstand capability will be repeated on the module where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one of the voltage sensing analog input modules (with BTSCA terminations) will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

21. RESISTIVE SENSING ANALOG INPUT GATE MODULE VALIDATION

The purpose of this test is to validate the gross operation of the analog input modules (021-5234) whose inputs are conditioned with resistive thermal device bridge completion circuits (038-5108); to validate the accuracy of the analog input gate module to RTD signal conditioning module cabling (040-5505) and the RTD signal conditioning module to terminal strip cabling (040-5521); and to validate the gross operation of the resistive thermal device in the uniform temperature reference plate (040-5522) and the accuracy of the associated cabling.

The validation of the analog inputs is accomplished by simulating resistive thermal devices with resistors on the terminal strip sourcing the input circuitry, then monitoring the data read from the analog input modules with the test computer and validating that the data read corresponds to the expected voltage from the RTD SCM per a table of voltage output versus resistance applied. (Reference Figure 13 of Attachment 1)

The validation of the resistive thermal device is accomplished by monitoring the data read from the analog input modules with the test computer and validating that the data read corresponds to a voltage corresponding to room temperature (assuming a room temperature range of 70F to 85F).

- 21.1 Connect the appropriate RTD Resistor Terminations (000-7086 for 038-5108-100, 200 ohm Pt, 32-350F; 000-7087 for 038-5108-101, 200 ohm Pt, 32-850F; 000-7088 for 038-5108-102, 200 ohm Pt, 32-110F; 000-7089 for 038-5108-103, 10 ohm Cu, -10-209C) to the appropriate points on the selected RTD BTSCA in the cabinet under test per Attachment 2 except on the channels wired to monitor the UTR RTD.

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

21.2 Run the Analog Input Test Program on the selected module set for 100 scans at gain code 4. Validate that the analog inputs indicate voltages within the voltage range in the following table: (all values in millivolts)

(Each RTD bridge completion module has circuits for the conditioning of four analog channels. Thus the eight channel gate modules require two RTD bridge completion modules, one for the first four channels, and another for the second four channels. This necessitates that the test program be run twice and the data from the SCM not being tested be ignored.)

(Note that some analog input gate modules are conditioned with only four channels of RTD conditioning, thus the other four channels are unterminated and their data must be ignored).

(The channels (of the 038-5108-100) wired to monitor the UTR RTD must indicate a voltage corresponding to the temperature of the uniform temperature reference plate which is assumed to be at room temperature of between 70F (19 millivolts) and 85F (27 millivolts).)

RTD TYPE =	200 Ohm Pt	200 Ohm Pt	200 Ohm Pt	10 Ohm Cu
TEMP =	32 : 350 F	32 : 850 F	32 : 110 F	-10 : 209 C
P/N :	038-5108-100	038-5108-101	038-5108-102	038-5108-103
CH 0 =	+32 : +48	+64 : +96	+6 : +14	+2.0 : +3.0
CH 1 =	+72 : +88	+144 : +176	+16 : +24	+4.5 : +5.5
CH 2 =	+112 : +128	+224 : +256	+26 : +34	+7.0 : +8.0
CH 3 =	+152 : +168	+304 : +336	+36 : +44	+9.5 : +10.5

VOLTAGES (millivolts) OUTPUT FROM RTD BRIDGE COMPLETION CIRCUITS

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
 BALTIMORE GAS and ELECTRIC CALVERT CLIPPS DATA ACQUISITION SYSTEM
 at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

MODULES TESTED:

GATE MODULE		CH 0-3 RTD SCM		CH 4-7 RTD SCM		INITIALS
CHASSIS #	SLOT #	CHASSIS #	SLOT #	CHASSIS #	SLOT #	
_____	_____	_____	_____	_____	_____	N/A
_____	_____	_____	_____	_____	_____	/
_____	_____	_____	_____	_____	_____	/
_____	_____	_____	_____	_____	_____	/
_____	_____	_____	_____	_____	_____	/
_____	_____	_____	_____	_____	_____	/
_____	_____	_____	_____	_____	_____	/
_____	_____	_____	_____	_____	_____	/

21.3 Repeat steps 21.1 to 21.2 for all analog input gate modules with resistive thermal device signal conditioning in the cabinet under test.

ANALOG INPUT
 (with resistive
 sense inputs)
 VALIDATION

PERFORMED BY: N. A. B. [Signature] C.P.I.
 WITNESSED BY: [Signature] N.U.S.

If a non-conformance is noted during the resistive sensing analog input validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the resistive sensing analog input modules will be repeated on the module where the non-conformance was noted.

22. RESISTIVE SENSING ANALOG INPUT GATE MODULE SURGE WITHSTAND
CAPABILITY VALIDATION

The purpose of this test is to validate the surge withstand capability of a sample of the RTD signal conditioning modules (038-5108). This is accomplished by simulating RTD inputs on the input terminals to the module set, and first acquiring baseline/ reference data from the analog input module. A surge is then applied to the inputs. Data is not acquired during the surge application. Data is again acquired from the analog input module after the surge application and the data is validated as not changing by more than a predefined limit. (Reference Figure 14 of Attachment 1)

- 22.1 Select up to five percent or at least one of the surge protected Analog Inputs with RTD signal conditioning (021-5234 / 038-5108) to have the surge withstand capability tested. Since two RTD SCMs are required to condition one analog input gate module, two RTD SCMs will be surge tested for every analog input gate selected.
- 22.2 Connect the appropriate RTD Resistor Terminations (000-7086 for 038-5108-100, 200 ohm Pt, 32-350F; 000-7087 for 038-5108-101, 200 ohm Pt, 32-850F; 000-7088 for 038-5108-102, 200 ohm Pt, 32-110F; 000-7089 for 038-5108-103, 10 ohm Cu, -10-209C) to the appropriate points on the selected RTD BTSCA in the cabinet under test per Attachment 2 except on the channels wired to monitor the UTR RTD.
- 22.3 Run the Analog Input Test Program on the selected module set for 100 scans at gain code 4. Validate that the analog inputs indicate voltages within the voltage range in the following table: (all values in millivolts)
- (Each RTD bridge completion module has circuits for the conditioning of four analog channels. Thus the eight channel gate modules require two RTD bridge completion modules, one for the first four channels, and another for the second four channels. This necessitates that the test program be run twice and the data from the SCM not being tested be ignored.)
- (Note that some analog input gate modules are conditioned with only four channels of RTD conditioning, thus the other four channels are unterminated and their data must be ignored).
- (The channels (of the 038-5108-100) wired to monitor the UTR RTD must indicate a voltage corresponding to the temperature of the uniform temperature reference plate which is assumed to be at room temperature of between 70F (19 millivolts) and 85F (27 millivolts).)

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
 BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
 at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

RTD TYPE =	200 Ohm Pt	200 Ohm Pt	200 Ohm Pt	10 Ohm Cu
TEMP =	32 : 350 F	32 : 850 F	32 : 110 F	-10 : 209 C
P/N :	038-5108-100	038-5108-101	038-5108-102	038-5108-103
CH 0 =	+32 : +48	+64 : +96	+6 : +14	+2.0 : +3.0
CH 1 =	+72 : +88	+144 : +176	+16 : +24	+4.5 : +5.5
CH 2 =	+112 : +128	+224 : +256	+25 : +34	+7.0 : +8.0
CH 3 =	+152 : +168	+304 : +336	+36 : +44	+9.5 : +10.5

VOLTAGES (millivolts) OUTPUT FROM RTD BRIDGE COMPLETION CIRCUITS

- 22.4 Connect the red lead of the surge transient generator cable to the RTD test termination on the selected BTSCA. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.
- 22.5 Ready the surge transient generator to output a surge per Appendix D.
- 22.6 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds.
- 22.7 Rerun the Analog Input Test Program on the selected module set for 100 scans at gain code 4. Validate that the analog inputs indicate voltages within the voltage range in the table above (all values in millivolts).
- 22.8 Validate that the means of the channels on the analog input module conditioned with the selected RTD SCM do not change by more than 1 bit between the pre-surge sample and the post-surge sample.
- 22.9 Validate that the peak to peak noise of the channels on the selected module does not increase by more than 2 bits peak to peak between the pre-surge sample and the post-surge sample.

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

MODULES SELECTED and TESTED:

GATE MODULE		CH 0-3 RTD SCM		CH 4-7 RTD SCM		INITIALS
CHASSIS #	SLOT #	CHASSIS #	SLOT #	CHASSIS #	SLOT #	
_____	_____	_____	_____	_____	_____	N/A/
_____	_____	_____	_____	_____	_____	/
_____	_____	_____	_____	_____	_____	/
_____	_____	_____	_____	_____	_____	/
_____	_____	_____	_____	_____	_____	/

22.10 Repeat steps 22.2 to 22.9 on all of the analog input/ RTU signal conditioning modules in the selected sample.

RESISTIVE SENSING	PERFORMED BY: <u>Robert Logan</u>	C.P.I.
ANALOG INPUT	APPROVED BY: <u>BWFEK</u>	N.U.S.
SURGE WITHSTAND	APPROVED BY: <u>NOT AVAILABLE</u>	B.G.E.
CAPABILITY		
VALIDATION		

Note that, due to design constraints, the inputs to the resistive thermal device bridge completion circuits are not surge protected, but the output of the circuits is surge protected and will protect the analog input gate module.

If a non-conformance is noted during the resistive sensing analog input surge withstand capability validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the resistive sensing analog input surge withstand capability will be repeated on the module where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one of the resistive sensing analog input modules will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

23. ANALOG INPUT DRIFT/STABILITY TEST

The purpose of this test is to validate that the sample of voltage sense analog input modules selected for common mode rejection, accuracy, and surge withstand capability validation are within the CPI published specifications for drift/stability.

- 23.1 Using bus wire, short the input terminals of the voltage sense analog input modules selected for common mode rejection, accuracy, and surge withstand capability testing. Connect the shorted channels to the surge ground bus bar in the cabinet under test.
- 23.2 Allow the cabinet (cabinet subsystem) to stabilize for a minimum of 2 hours.
- 23.3 Run the Analog Input Test Program on the selected modules for 100 scans at Gain Code 11.
- 23.4 Using the digital thermometer, record the temperature at the temperature transducer inside the cabinet under test.
- 23.5 Repeat steps 23.3 to 23.4 at two hour intervals four times.

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

3/9/84

INITIAL SCAN: TIME: 9 41am TEMP: 24°C

(Enter mean voltage from scan below)

MODULE TESTED: CHASSIS # II-1F1 SLOT # 16 INITIALS: RL /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
-4.321	-2.820W	-1.501W	-2.759W	-1.001W	1.245W	-0.489W	-4.736

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
 BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
 at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

SECOND SCAN: TIME: 3/12/84
8:29 TEMP: 30°C

(Enter mean voltage from scan below and deviation from initial scan under mean)

MODULE TESTED: CHASSIS # II-1F1 SLOT # 16 INITIALS: RL /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
-5.615mV	-3.003mV	-2.379mV	-2.345mV	-1.929mV	1.738mV	-1.709mV	-6.470mV
-0.294	-0.183	-1.038	-0.586	-0.928	0.513	-1.221	-1.734

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # SLOT # INITIALS: /

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

3/12/84

THIRD SCAN: TIME: 11:15:00 TEMP: 29°C

(Enter mean voltage from scan below and deviation from initial scan under mean)

MODULE TESTED: CHASSIS # II-1F1 SLOT # 16 INITIALS: RL/

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
-6.079 μ V	-3.113 μ V	-2.698 μ V	-4.285 μ V	-2.563 μ V	1.099 μ V	-2.002 μ V	-6.885 μ V
-1.758	-0.293	-1.197	-1.526	-1.522	-0.246	-1.514	-2.149

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

3/12/84

FOURTH SCAN: TIME: 2:27 TEMP: 28°C

(Enter mean voltage from scan below and deviation from initial scan under mean)

MODULE TESTED: CHASSIS # II-1E1 SLOT # 16 INITIALS: RL

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
- 5.452 μ V	- 2.828 μ V	- 2.417 μ V	- 3.284 μ V	- 1.794 μ V	1.892 μ V	- 1.453 μ V	- 6.299 μ V
1.111	- 0.036	- 0.916	- 0.525	- 0.793	- 0.647	- 0.965	- 1.563

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
 BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
 at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

3/12/84
 FIFTH SCAN: TIME: 4:240M TEMP: 29°C

(Enter mean voltage from scan below and deviation from initial scan under mean)

MODULE TESTED: CHASSIS # II-1F1 SLOT # 16 INITIALS: RL/

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7
-5.688 μ V	-2.893 μ V	-2.209 μ V	-3.149 μ V	-1.721 μ V	2.161 μ V	-1.531 μ V	-6.067 μ V
-1.367	-0.073	-.708	-0.390	-0.720	+0.916	-1.050	-1.331

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _____ SLOT # _____ INITIALS: _____/

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

23.6 Determine the channel with the most deviation from the initial scan for for each successive scan.

SECOND SCAN : CHASSIS # II-1F1 SLOT # 16
CHAN # 7 MAX. DEVIATION -1.734

THIRD SCAN : CHASSIS # II-1F1 SLOT # 16
CHAN # 7 MAX. DEVIATION -2.149

FOURTH SCAN : CHASSIS # II-1F1 SLOT # 16
CHAN # 7 MAX. DEVIATION -1.563 μ V

FIFTH SCAN : CHASSIS # II-1F1 SLOT # 16
CHAN # 1 MAX. DEVIATION -1.367 μ V

23.7 Validate that the maximum deviation for each sampling is within
+/- 10 microvolts plus +/- 0.5 microvolts per degree C change
in ambient temperature of the initial reading.

Second reading : temp change 6° C

maximum allowable deviation =

$$(\text{temp change } \underline{6^\circ} \text{ C} \times 0.5 \text{ uV/C}) + 10 \text{ uV} = \underline{13.0} \text{ uV}$$

maximum measured deviation : -1.734 μ V

Third reading : temp change 5° C

maximum allowable deviation =

$$(\text{temp change } \underline{5^\circ} \text{ C} \times 0.5 \text{ uV/C}) + 10 \text{ uV} = \underline{12.5} \text{ uV}$$

maximum measured deviation : -2.149 μ V

Fourth reading : temp change 4° C

maximum allowable deviation =

$$(\text{temp change } \underline{4^\circ} \text{ C} \times 0.5 \text{ uV/C}) + 10 \text{ uV} = \underline{12.0} \text{ uV}$$

maximum measured deviation : -1.583 μ V

Fifth reading : temp change 5° C

maximum allowable deviation =

$$(\text{temp change } \underline{5^\circ} \text{ C} \times 0.5 \text{ uV/C}) + 10 \text{ uV} = \underline{12.5} \text{ uV}$$

maximum measured deviation : -1.367 μ V

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

ANALOG INPUT	PERFORMED BY:	<u>Robert Ligo</u>	C.P.I.
DRIFT/ STABILITY TEST	APPROVED BY:	<u>[Signature]</u>	N.U.S.
	APPROVED BY:	<u>NOT AVAILABLE</u>	B.G.E.

If a non-conformance is noted during the voltage sensing analog input drift/ stability validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the voltage sensing analog input drift/ stability will be repeated on the module where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one of the voltage sensing analog input modules (with BTSCA terminations) will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

APPENDIX A

TEST AND REPAIR LOG BOOK FORMAT

The Test and Repair Log is used to record any and all acceptance testing of the data acquisition system supplied by Computer Products, Inc. to NUS Corp. and Baltimore Gas and Electric for the Calvert Cliffs power generation plant. It is also used to record any and all anomalies noted during this testing and the corrective action taken to correct the anomalies.

Entries (in black ink) are to be made in the log as follows:

Identification of Cabinet under test :

Unit # (I or II), CPI cabinet # (1 - 11);

Title of test procedure used for testing

(or 'Continuation of Anomalies of Unit X Cabinet X' if an additional page is required to list the anomalies);

Date test started;

Date test completed;

Name of test conductor printed and signed;

Name of the witness printed and signed;

If no anomalies are noted during the test, then NONE is checked in the anomalies noted section;

If anomalies are noted, then a description of the anomaly is entered and the action taken to correct the anomaly is described. The last anomaly is followed by 'End of Anomalies'.

The following are sample pages of the log with typical responses.

***** THE FOLLOWING IS A SAMPLE ONLY. *****

TEST and REPAIR LOG for
NUS / BALTIMORE GAS and ELECTRIC CALVERT CLIFFS
DATA ACQUISITION SYSTEM supplied by COMPUTER PRODUCTS, INC.

UNIT # I CPI CABINET # -3

TESTED PER

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE dated 1/29/84
(procedure used for testing)

DATE STARTED: I MARCH 1984 DATE COMPLETED: 3 MARCH 1984

PERFORMED BY: (conductor's name) (conductor's sign.)
(printed) (signed)

WITNESSED BY: (auditor's name) (auditor's sign.)
(printed) (signed)

=====

ANOMALIES NOTED and CORRECTIVE ACTION TAKEN: (NONE:(X))

***** THE PRECEDING IS A SAMPLE ONLY. *****

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (PT. LAUDERDALE) 2/2/84

***** THE FOLLOWING IS A SAMPLE ONLY. *****

TEST and REPAIR LOG for
NUS / BALTIMORE GAS and ELECTRIC CALVERT CLIFFS
DATA ACQUISITION SYSTEM supplied by COMPUTER PRODUCTS, INC

UNIT # II CPI CABINET # 9

TESTED PER

(CONTINUATION OF ANOMALIES NOTED)

(procedure used for testing)

DATE STARTED: _____ DATE COMPLETED: _____

PERFORMED BY: _____ (printed) _____ (signed)

WITNESSED BY: _____ (printed) _____ (signed)

=====

ANOMALIES NOTED and CORRECTIVE ACTION TAKEN: (NONE:(),

5) Section 17. : Analog to Digital Converter (9F3-11) (P/N 021-0211-008

S/N C0099) out of calibration. Recalibrated ADC per AT 021-0211

and test rerun.

(END OF ANOMALIES)

***** THE PRECEDING IS A SAMPLE ONLY. *****

APPENDIX B

CPI RTP CONTROL PANEL DESCRIPTION AND OPERATING INSTRUCTION SUMMARY

The following is a condensed description and summary of operation of the CPI RTP7505/05 Control Panel (P/N 070-0044) required for the performance of this acceptance test. For more information refer to CPI Technical Manual # 980-0070-044.

The RTP7505/05 Control Panel is used to provide an easy to use method of exercising the various inputs and outputs of equipment connected via the RTP bus. Connection to the bus is through a ribbon cable connected from slot #5 of the control panel to the 'I/O Bus In' slot of the first chassis in the I/O string. A computer may be connected to slot #1 of the control panel allowing either the computer or the control panel to access the peripheral equipment attached to the RTP I/O bus.

The following controls and indicators are used on the Control Panel:

1. MAN/COMP (Manual/Computer) switch
2. DATA WORD DISPLAY
3. INTERRUPT VECTOR DISPLAY
4. OUTPUT WORD SELECT switches
5. COMMAND WORD SELECT switches
6. CONTROL DISPLAY
7. INSTRUCTION RATE controls
8. DEVICE ADDRESS SELECT switches
9. INSTRUCTION SELECT switches
10. RESET switch

APPENDIX B cont'd

The MAN/COMP (MANual/COMPUter) switch is a two position switch which is used to select the operating mode of the RTP Control Panel. When the switch is placed in the MANual position, the control panel is set to the manual mode of operation and the computer is disconnected from the RTP peripheral devices connected to the control panel. When the switch is placed in the COMPUter position, the computer is connected thru the control panel to the peripheral devices on the RTP I/O bus.

The DATA WORD DISPLAY provides a visual display of the data loaded into the input buffer. Sixteen light emitting diodes (LED's), represent the 16 data bits. Each data bit will light in the presence of a '1', and be dark in the presence of a '0'. The MAN/COMP switch selects the source of the data to be loaded and displayed. In the MANual mode, the data displayed is the result of a transfer from the selected peripheral device by an input transfer function from the control panel. In the COMPUter mode, the data displayed is from the computer.

The INTERRUPT VECTOR DISPLAY provides a visual display of the data bits representing the address of the current interrupt vector from the selected peripheral. Ten light emitting diodes (LED's), represent the 10 data bits. Each data bit will light in the presence of a '1', and be dark in the presence of a '0'. The data displayed is the result of a transfer from the selected peripheral device by an Interrupt Query (INT QRY) instruction from the control panel.

The OUTPUT WORD SELECT consists of 16 two position toggle switches, representing the 16 data bits, which are used to format an output data word. In the MANual mode, the data word is transferred to the selected peripheral. In the COMPUter mode, the data word is transferred to the computer during a DATA INPUT instruction addressed to the first device address of the control panel. The UP position of each switch represents a '1', and the DOWN position represents a '0'.

The COMMAND WORD SELECT consists of 16 two position toggle switches, representing the 16 data bits, which are used to format a command data word. In the MANual mode, the data word is transferred to the selected peripheral. In the COMPUter mode, the switches perform no function. The UP position of each switch represents a '1', and the DOWN position represents a '0'.

APPENDIX B cont'd

The CONTROL WORD DISPLAY provides a visual display of the status of various functions using 6 light emitting diodes (LED's), to represent the 6 functions as follows:

DEV SEL - The DEVICE SElect display, when lighted, indicates that the device address switches in one of the RTP peripheral devices connected to the control panel is set to the address corresponding to the setting of the DEVICE ADDRESS SELECT switches. This display is only active in the MANUAL mode.

INT - The INTerrupt request display, when lighted, indicates that one or more RTP peripheral devices connected to the control panel are requesting interrupt service. The priority of the interrupts is determined by the electrical proximity of the devices to the control panel. Interrupt requests are always reset by an INTERRUPT QUERY instruction, and depending on the type of device, by either an INPUT, OUTPUT, or COMMAND instruction or Master Reset. This display is only active in the MANUAL mode.

DATA RDY - The DATA Ready display, when lighted, indicates that the peripheral device being addressed is in a ready state. Note: the DATA RDY indicator actually monitors the RTP TEST RETURN line. This display is only active in the MANUAL mode.

RUN - The RUN display, when lighted, indicates that an instruction is in the instruction register and is being executed.

MAN - The MANUAL display, when lighted, indicates that the control panel is in the manual mode.

COMP - The COMPuter display, when lighted, indicates that the control panel is in the computer mode.

The INSTRUCTION RATE controls consist of a six position rotary switch designated RANGE and a potentiometer designated VERNIER. The overall instruction rate can be varied, using the two controls, over the total range of about 0.5 to 500,000 instructions per second.

RANGE - The RANGE selector switch is designated 5, 50, 500, 5K (5000), 50K (50,000), and 500K (500,000) which define the nominal instruction rate per second for each range.

VERNIER - The VERNIER potentiometer varies the instruction rate within each range from the maximum rate down to the minimum rate for that range.

APPENDIX B cont'd

The DEVICE ADDRESS SELECT consists of 6 two position toggle switches representing the 6 data bits, which are used to format the DEVICE ADDRESS lines on the RTP I/O bus. These switches are only active in the MANUAL mode and are designated 32, 16, 8, 4, 2, and 1. The UP position of each switch represents a '1', and the DOWN position represents a '0'.

The INSTRUCTION SELECT consists of 5 three position toggle switches with an LED indicator associated with each switch. The five switches are used to select MANUAL mode instructions to be executed and have no function in the COMPUTER mode.

Four switches, COMMAND, OUTPUT, INTERRUPT QUERY, and INPUT each have three positions: UP - (locked) allows continuous execution; CENTER - skip execution (or no execution); and DOWN - (momentary contact with spring return) single cycle execution.

The WAIT TEST/WAIT INT switch is also a three position switch. The UP position (WAIT TEST) causes a wait in the execution sequence until the test return line tests 'ready'. The CENTER position causes a skip or no execution, and the DOWN position causes a wait in the execution sequence until an interrupt request is initiated from one of the RTP peripheral devices.

Any of the four instructions COMMAND, OUTPUT, INTERRUPT QUERY, or INPUT, can be single cycle executed in any order manually. When any of the instruction select switches are set to the up position (continuous execution), the instructions are executed in the following order: COMMAND, OUTPUT, WAIT TEST / WAIT INTERRUPT, INTERRUPT QUERY, INPUT. When the last selected instruction is executed, the sequence starts over and continues until it is stopped or the switches are changed.

Each switch has a LED associated with it which lights during execution of that particular instruction.

The RESET switch is a momentary contact with spring return switch, which when depressed, resets the logic circuitry in the RTP Control Panel and also causes an I/O Reset to all peripheral devices on the RTP I/O bus. This switch is only active in the MANUAL mode.

APPENDIX C

PHYSICAL SLOT NUMBER to SLOT ADDRESS CROSS REFERENCE TABLE

UNIVERSAL I/O CONTROLLERS (070-0004 & 040-5462)			REDUNDANT ACCESS UNIVERSAL I/O CONTROLLERS (070-5083)		
SLOT	ADDRESS (binary) (decimal)		SLOT	ADDRESS (binary) (decimal)	
6	0000	00	10	0000	00
7	0001	01	11	0001	01
8	0010	02	12	0010	02
9	0011	03	13	0011	03
10	0100	04	14	0100	04
11	0101	05	15	0101	05
12	0110	06	16	0110	06
13	0111	07	17	0111	07
14	1000	08			
15	1001	09			
16	1010	10			
17	1011	11			
18	1100	12			
19	1101	13			
20	1110	14			
21	1111	15			

These addresses (binary) represent data bits 12 - 15 of the Command Word when used to address an option card.

APPENDIX D

OPERATING INSTRUCTIONS AND CONFIGURATION FOR TEST
of the
VELONEX SURGE TRANSIENT GENERATOR

THIS GENERATOR IS CAPABLE OF OUTPUTTING VOLTAGES THAT ARE LETHAL.

USE EXTREME CAUTION AT ALL TIMES WHEN USING THIS GENERATOR.

This piece of test equipment is used to generate surge transients. The surge transient required for this test is defined by IEEE Standard # 472 ('Surge Withstand Capability Testing'). Configure the generator as follows to generate the required surge transient.

Set the BURST MODE selector switch to '2X LINE FREQUENCY'; set the OUTPUT TIMER MODE selector switch to 'TIMED OUTPUT'; set the OUTPUT TIMER DURATION control to '2 seconds'; and set the SOURCE IMPEDANCE selector switch to '150 OHMS'. The settings of the BURST FREQUENCY and BURST PHASE controls are ignored in this operating mode.

Install a connector on the LOW OUTPUT terminal to connect the LOW OUTPUT to the chassis ground (connected internally to the connector).

Install a 'HV connector to alligator clip cable' to the HIGH OUTPUT terminal.

Depress the white POWER ON pushbutton to put the generator in standby mode.

To ready the generator for generating a surge transient, connect the output cable to the item to be tested (black to the surge ground reference and red to the point(s) to be tested); depress the two red HV ON pushbuttons simultaneously; adjust the OUTPUT AMPLITUDE control to the full clockwise position.

To apply the surge transient, depress the START pushbutton. will cause a dangerous high voltage to be present at the output. the generator for two seconds. USE CAUTION.

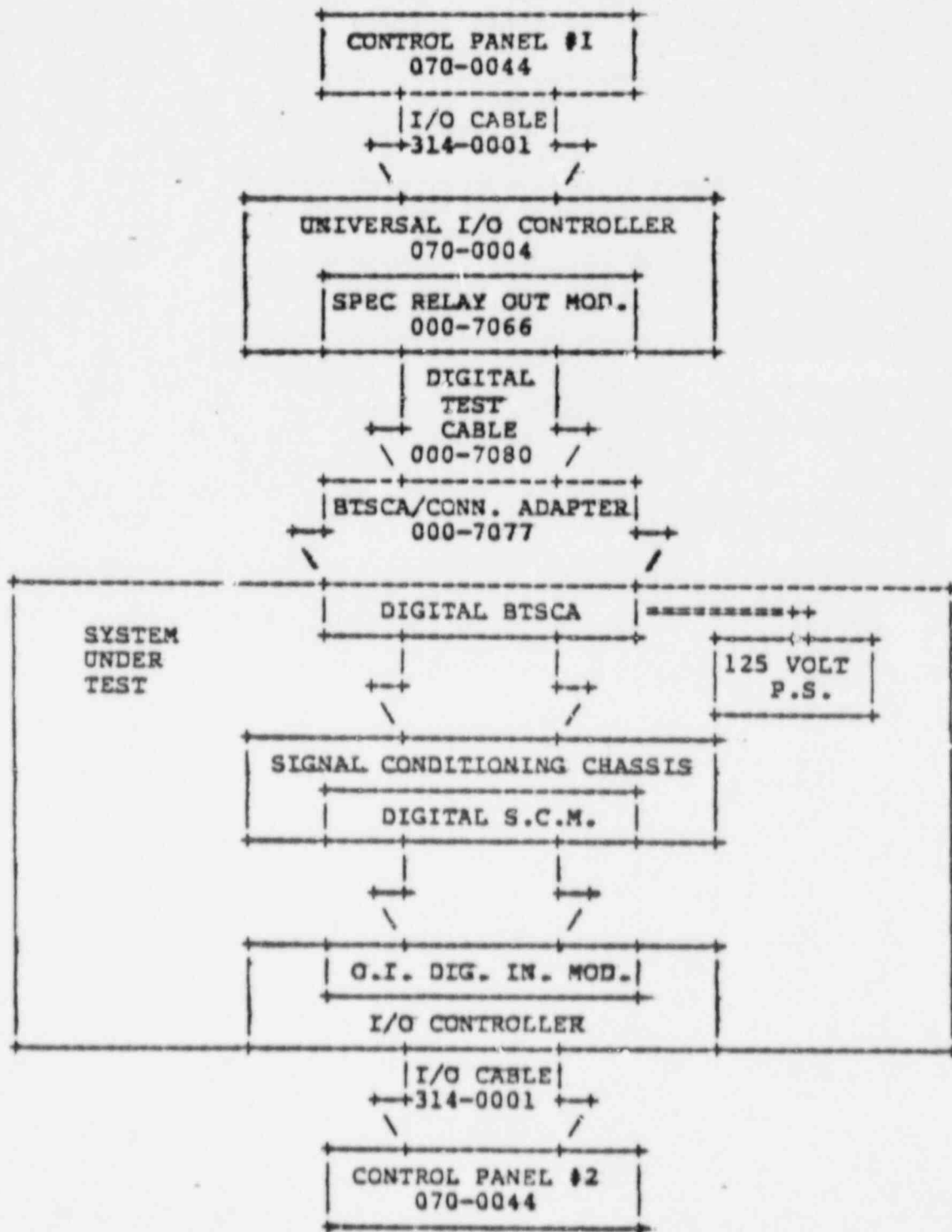
To put the generator back into standby mode, push one of the red HV ON pushbuttons.

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (PT. LAUDERDALE) 2/2/84

ATTACHMENT 1

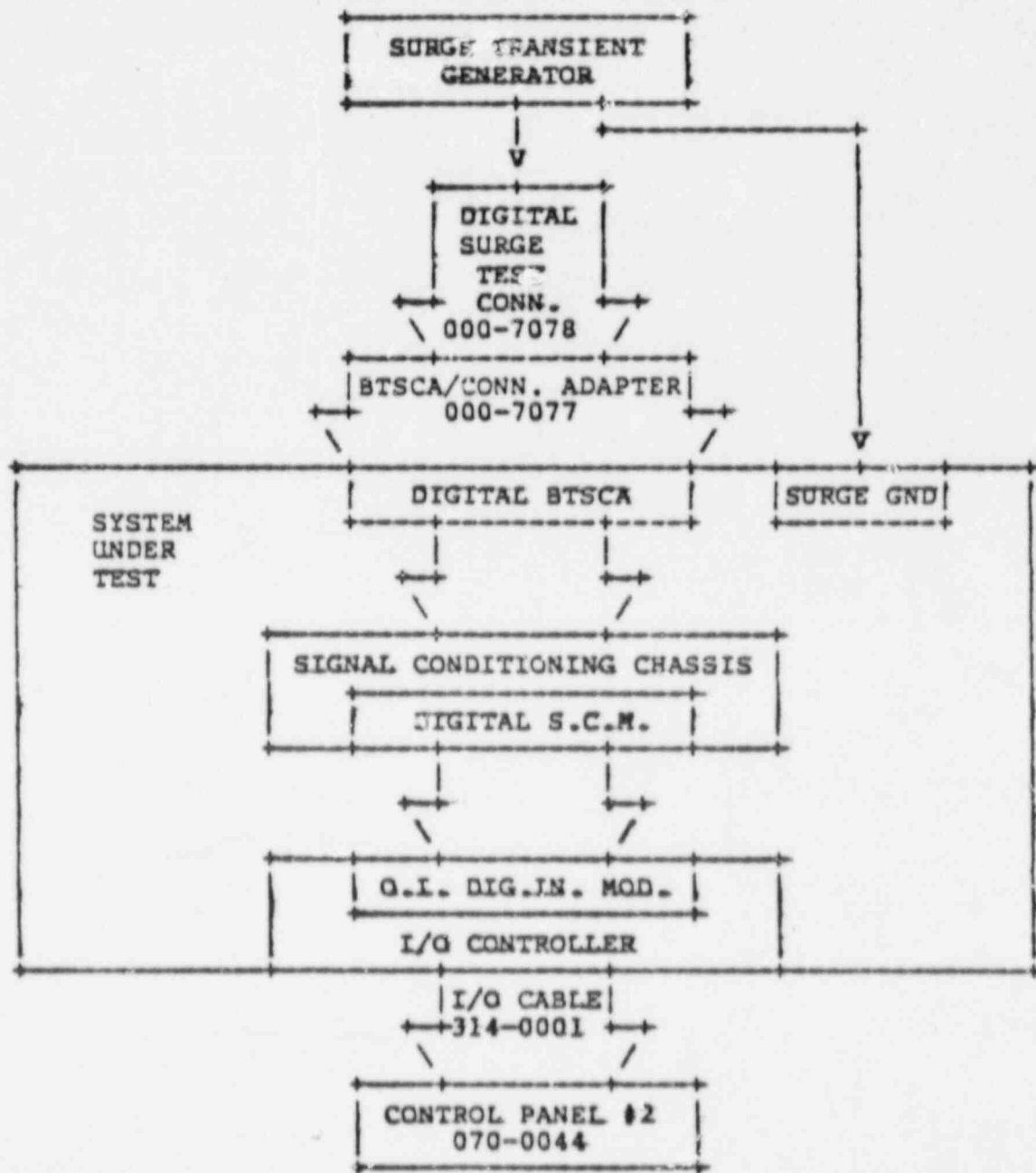
TEST CONFIGURATION DRAWINGS

The following figures are drawings depicting the configuration of test equipment used to perform the different sections of the procedure.



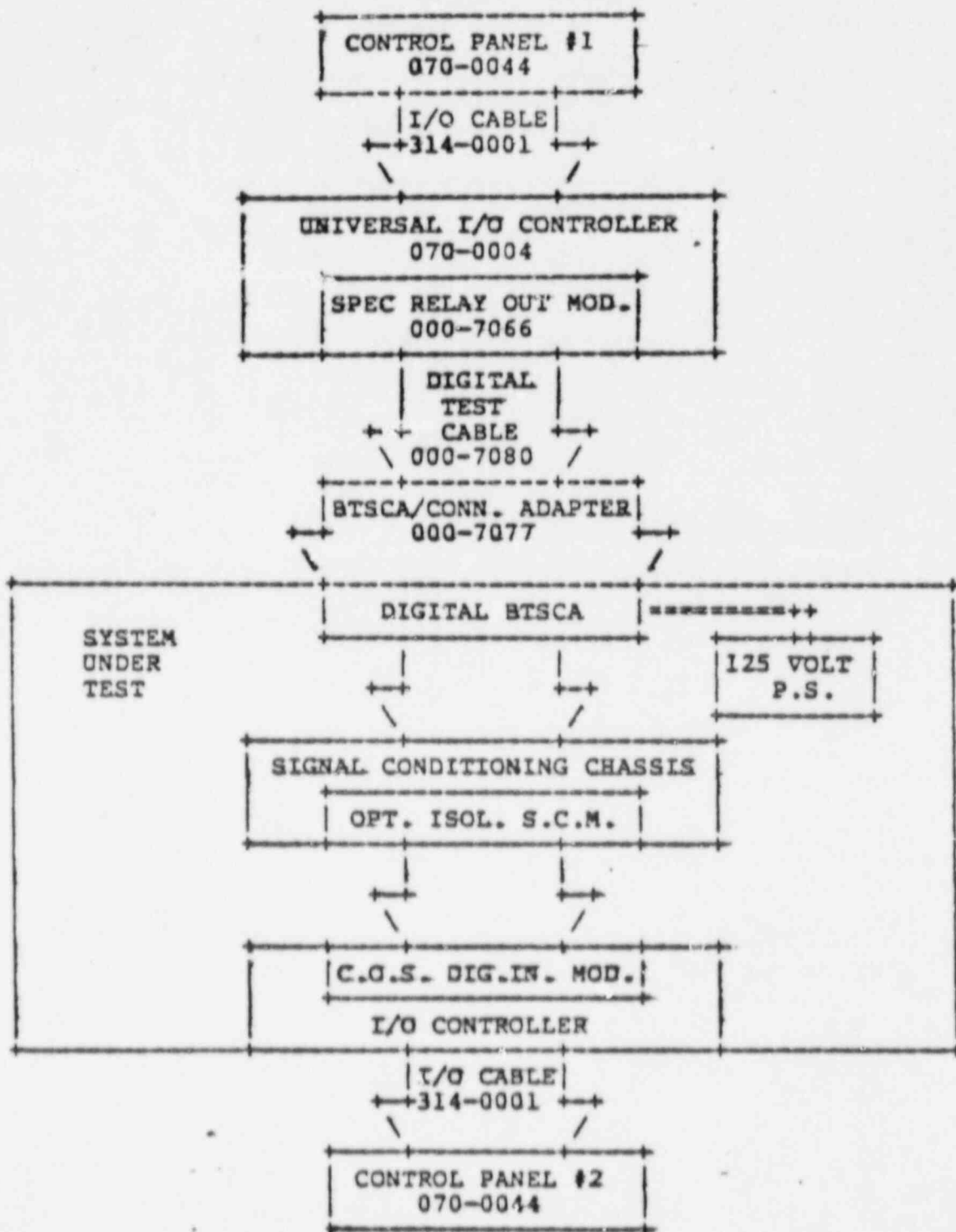
OPTICALLY ISOLATED DIGITAL INPUT VALIDATION

FIGURE 1



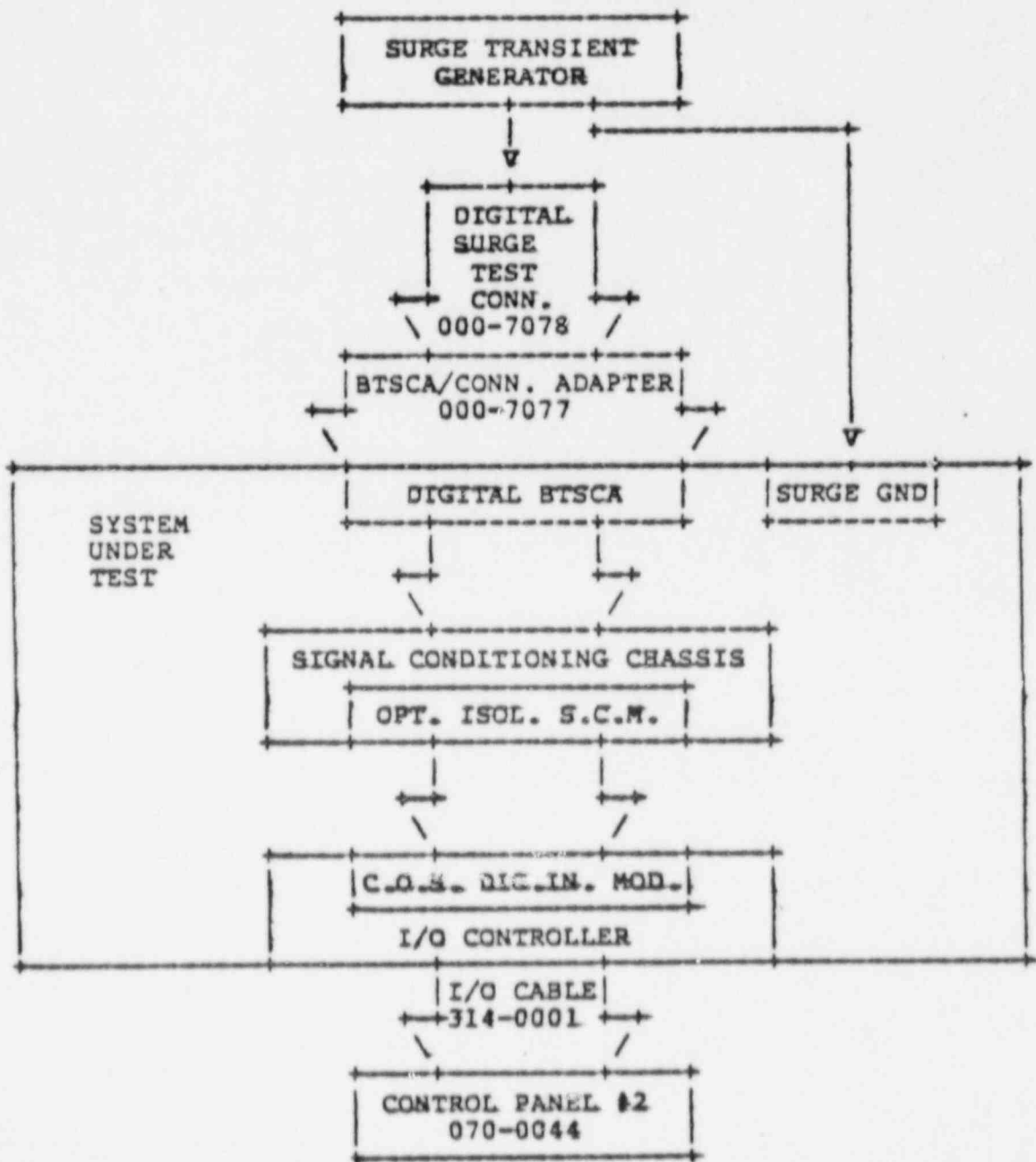
OPTICALLY ISOLATED DIGITAL INPUT
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 2



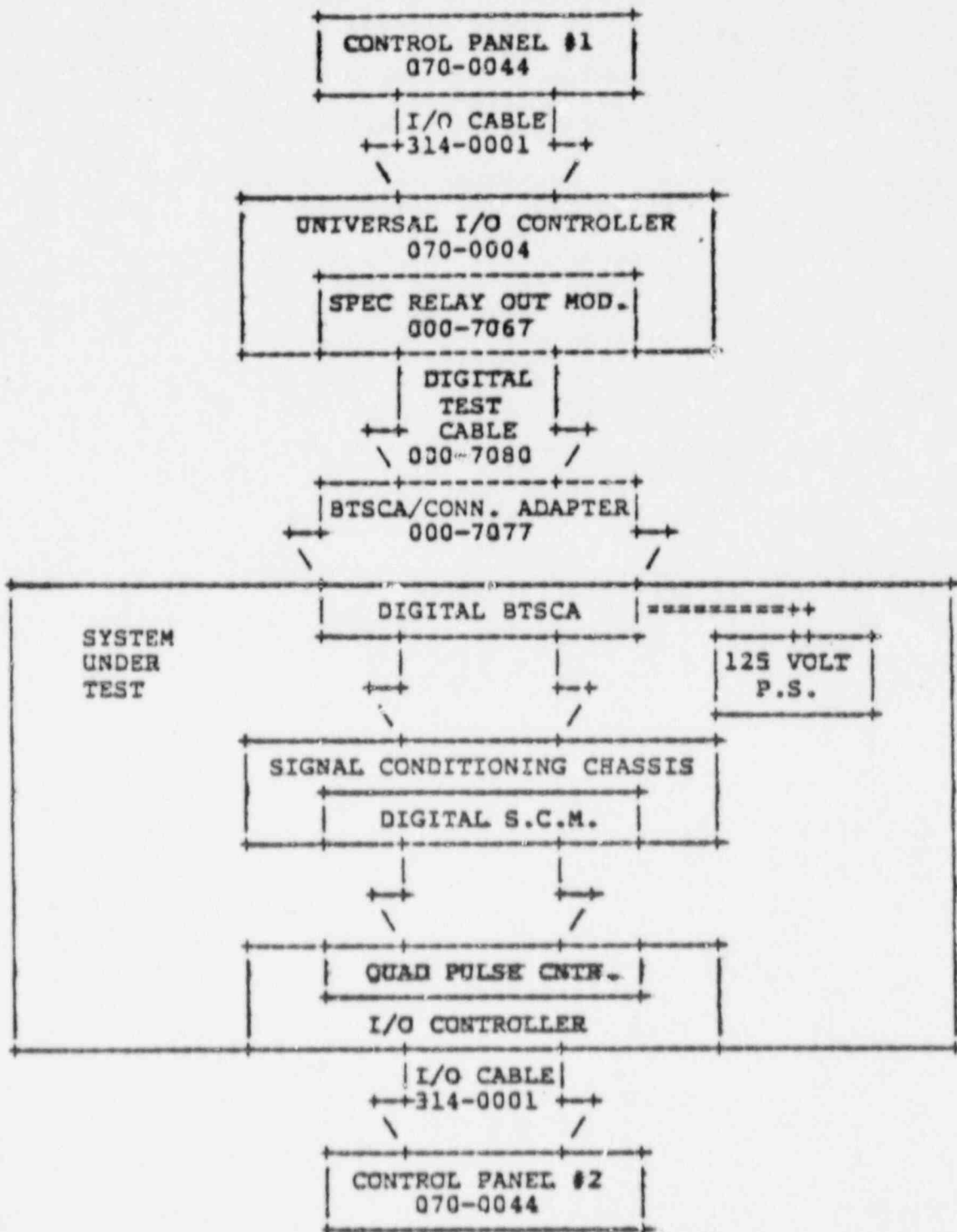
CHANGE OF STATE DIGITAL INPUT VALIDATION

FIGURE 1



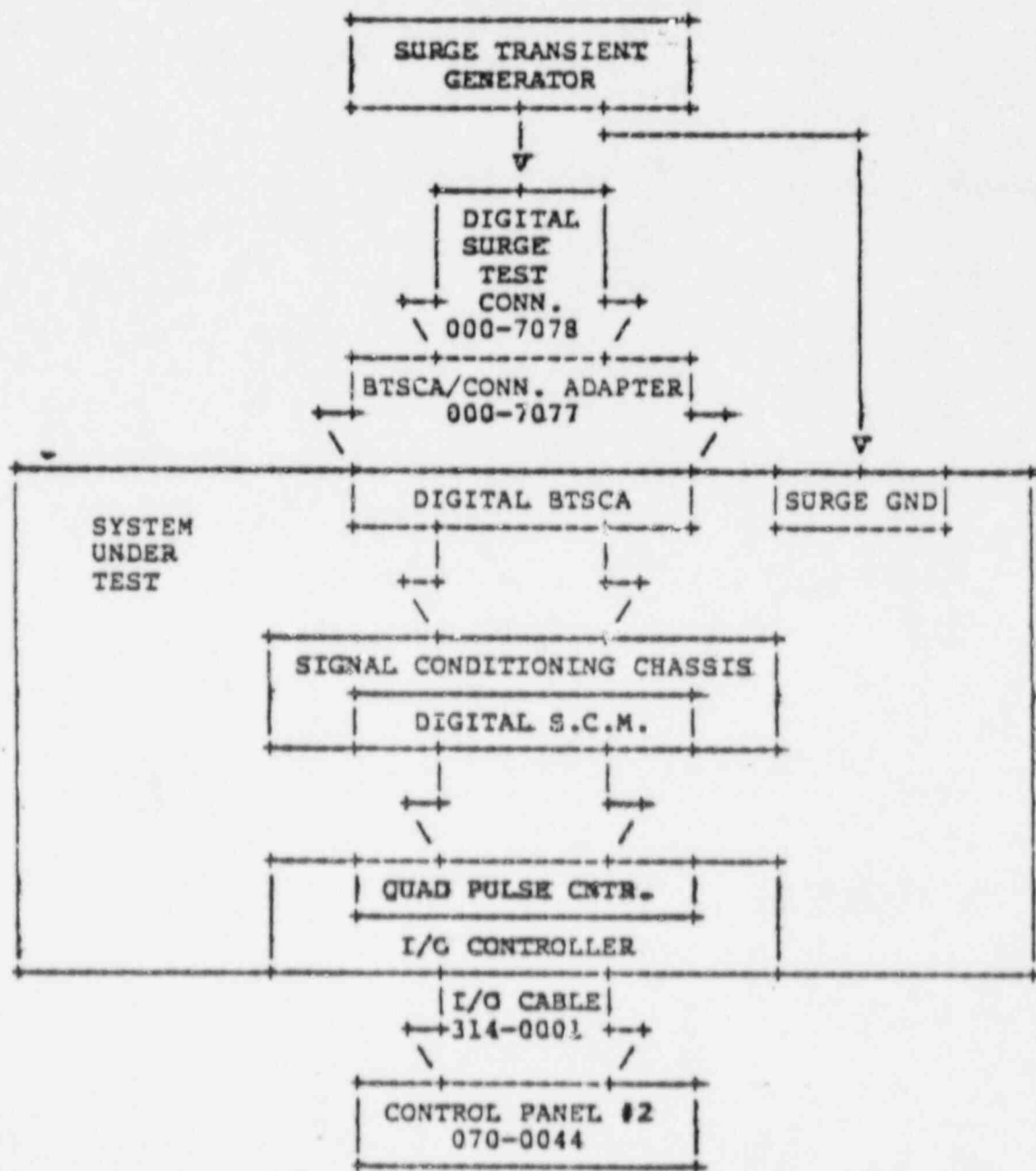
CHANGE OF STATE DIGITAL INPUT
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 4



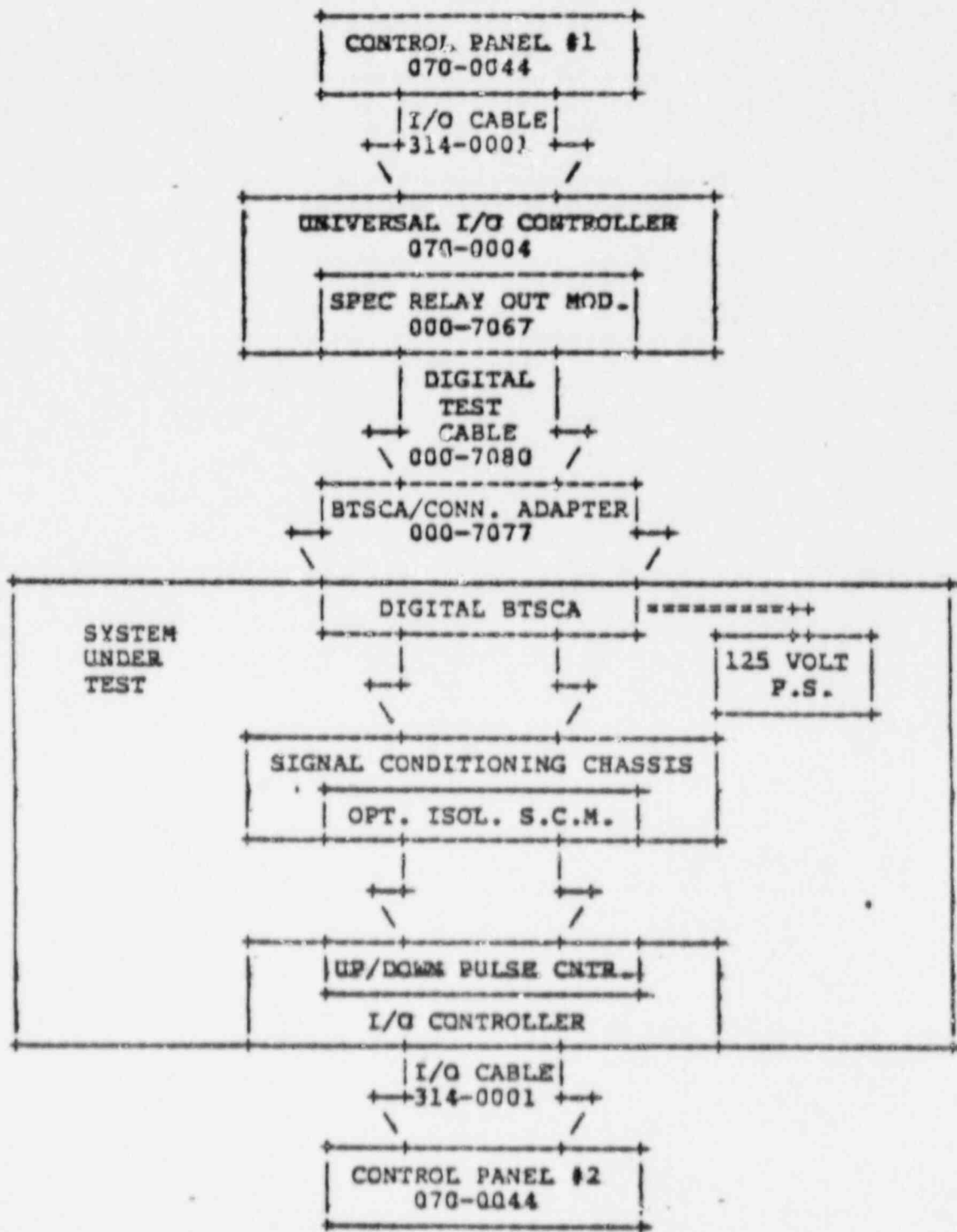
QUAD PULSE COUNTER VALIDATION

FIGURE 5



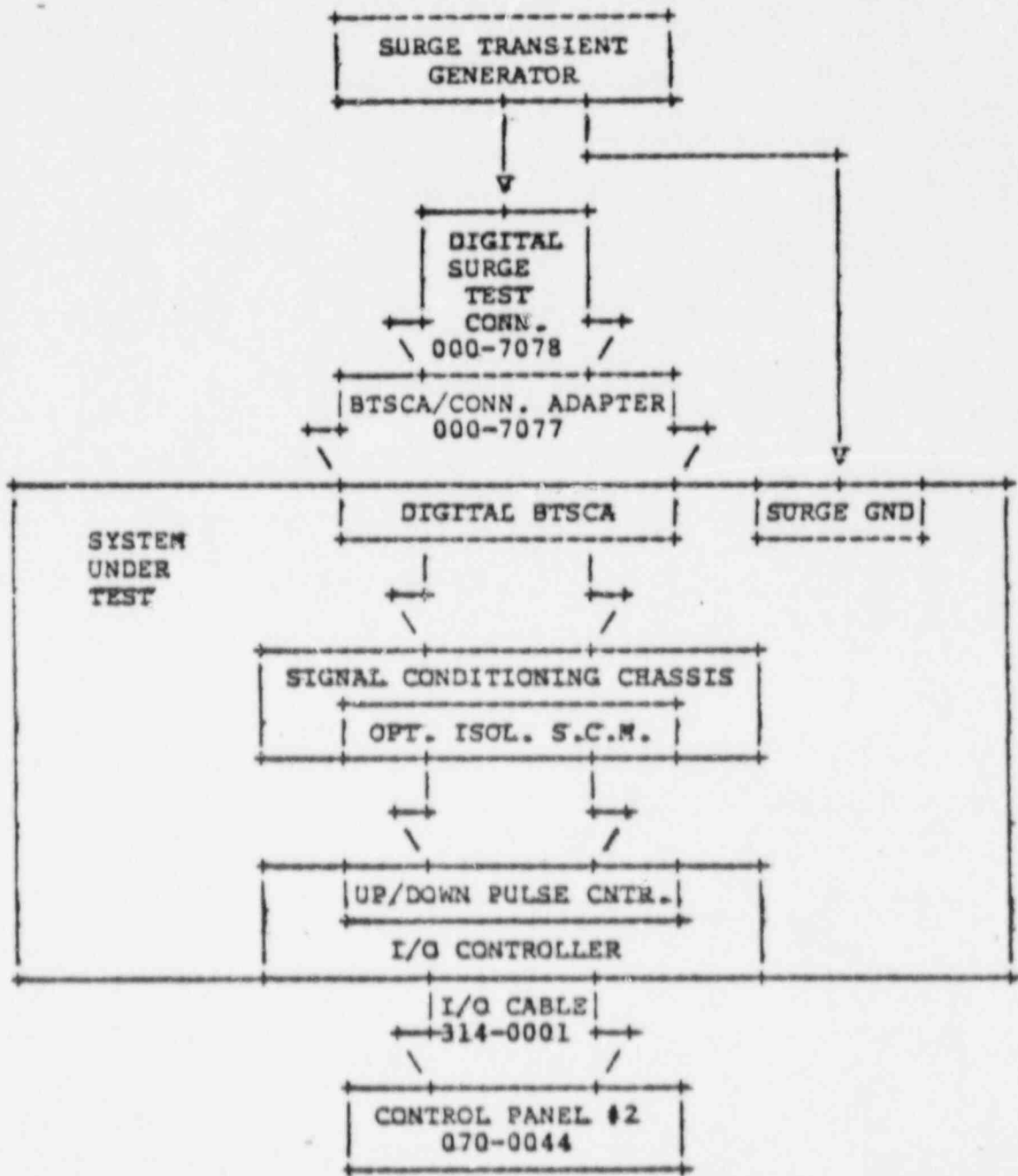
QUAD PULSE COUNTER
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 6



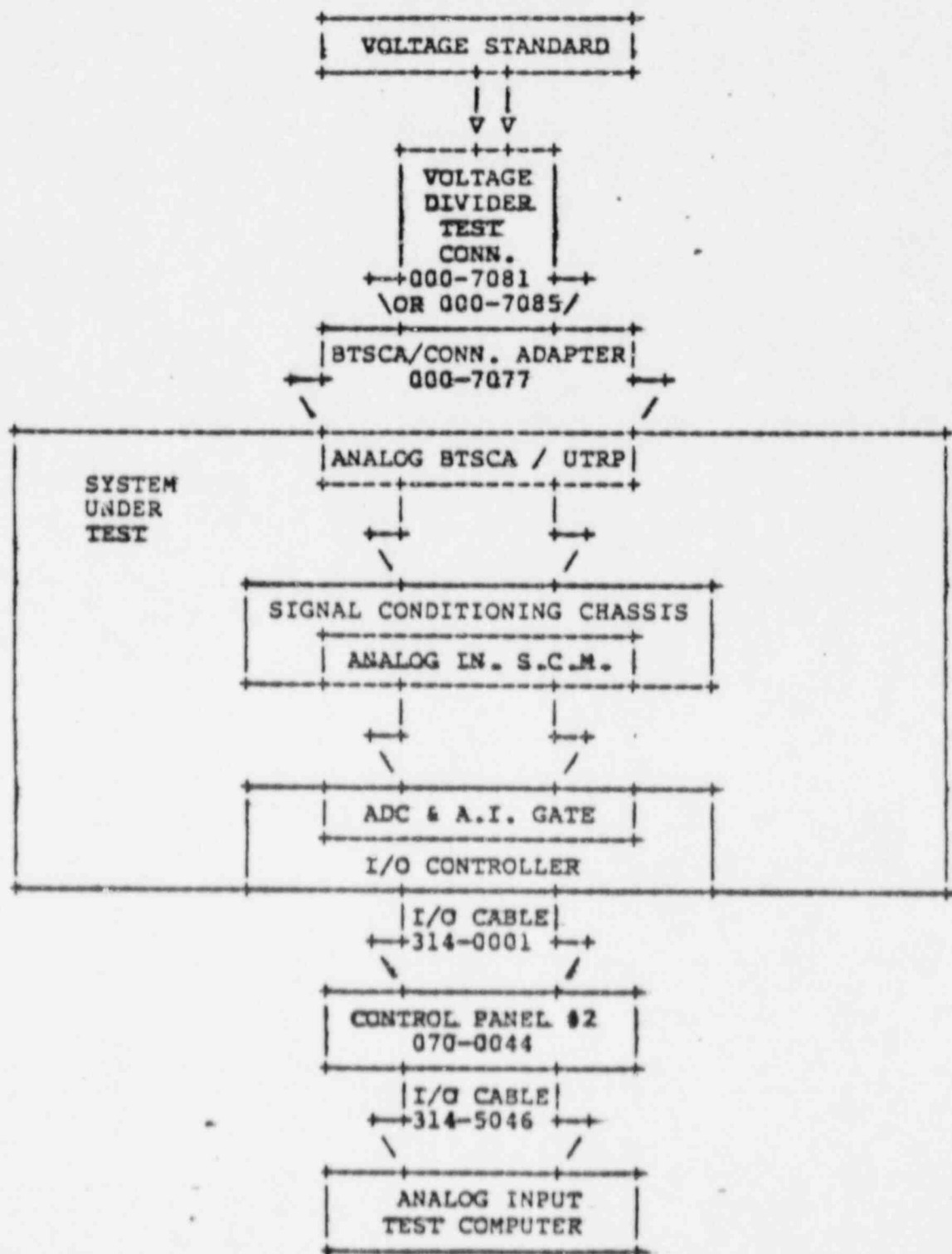
UP/DOWN PULSE COUNTER VALIDATION

FIGURE 7



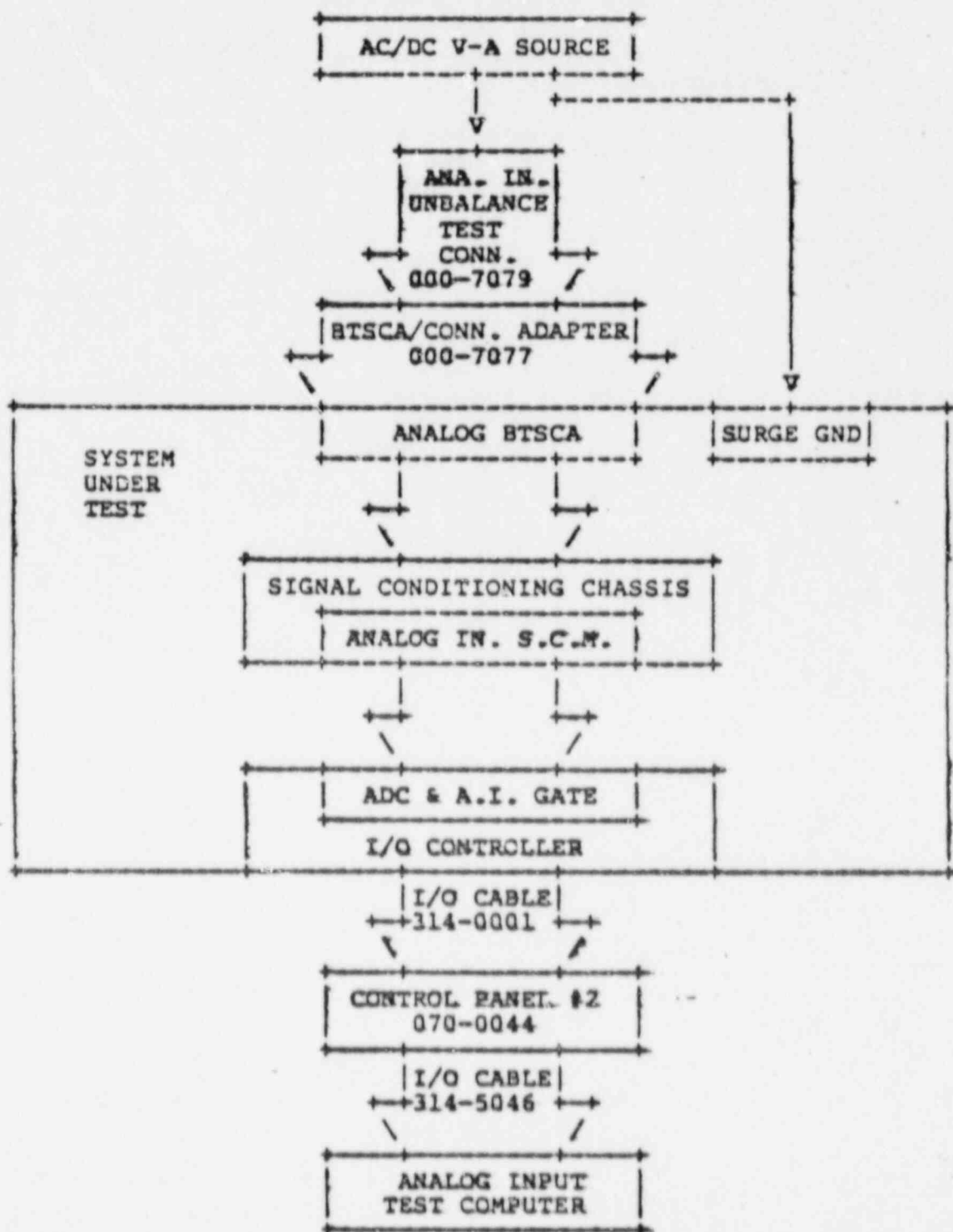
UP/DOWN PULSE COUNTER
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 8



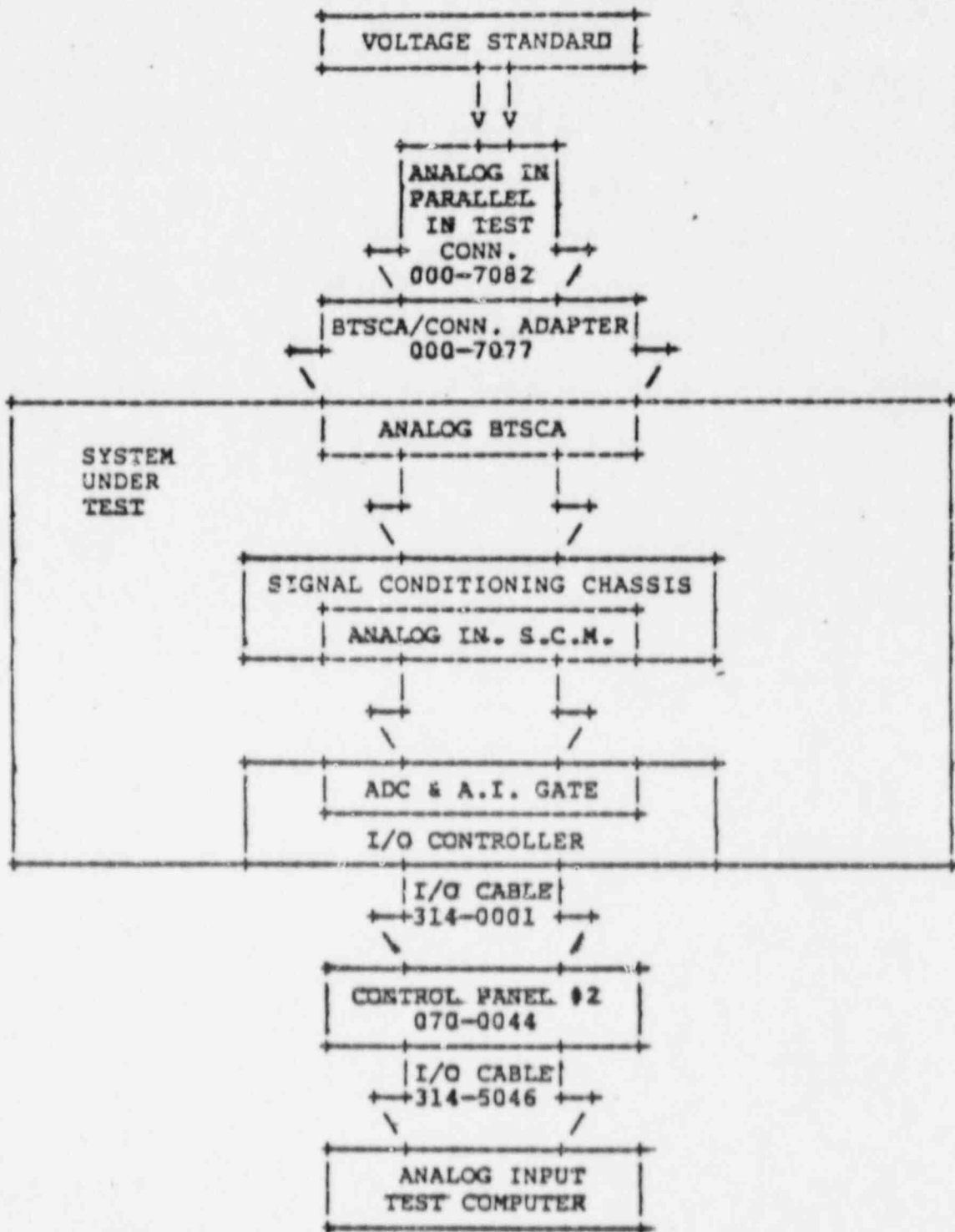
VOLTAGE SENSING ANALOG INPUT GATE VALIDATION

FIGURE 9



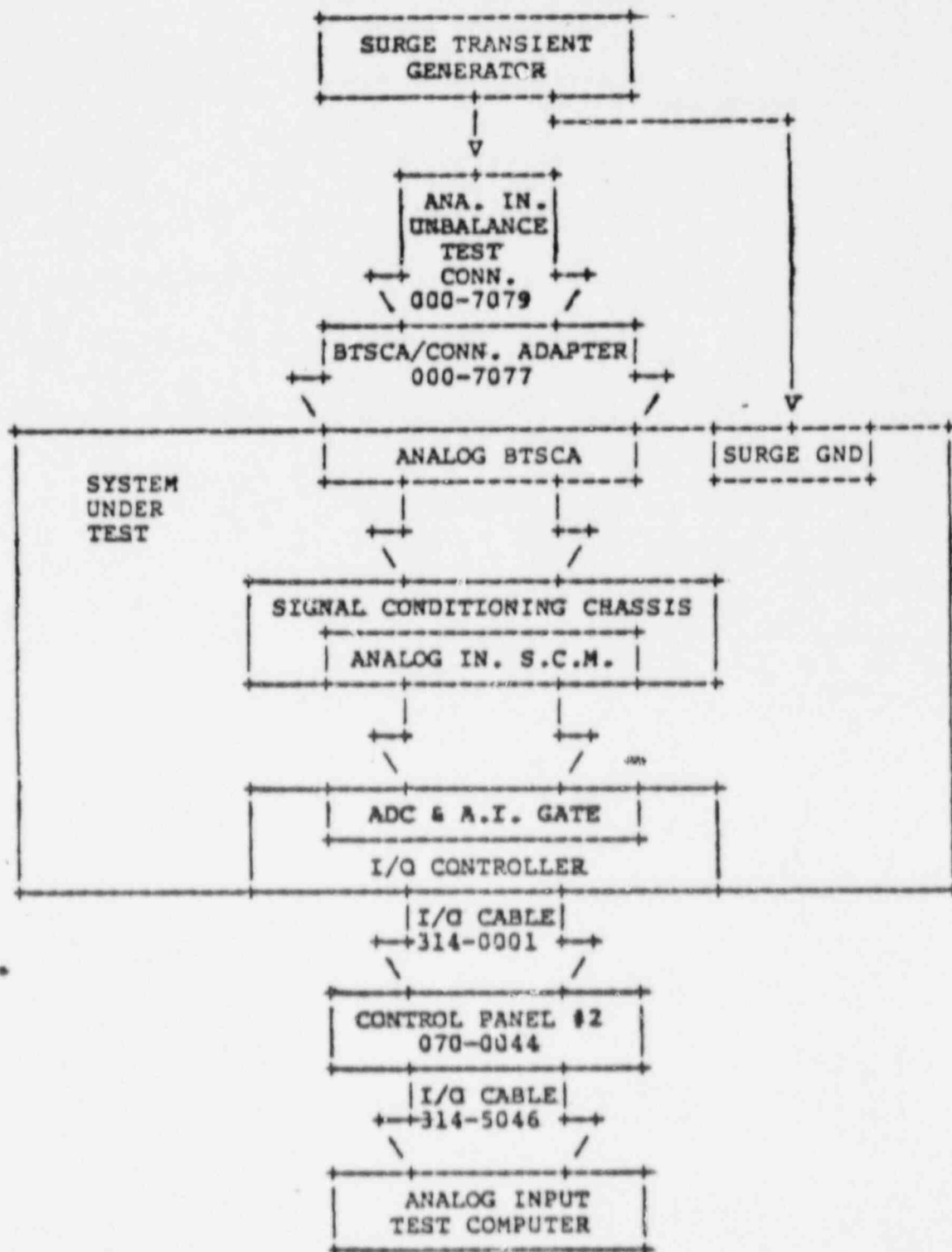
VOLTAGE SENSING ANALOG INPUT
COMMON MODE REJECTION VALIDATION

FIGURE 10



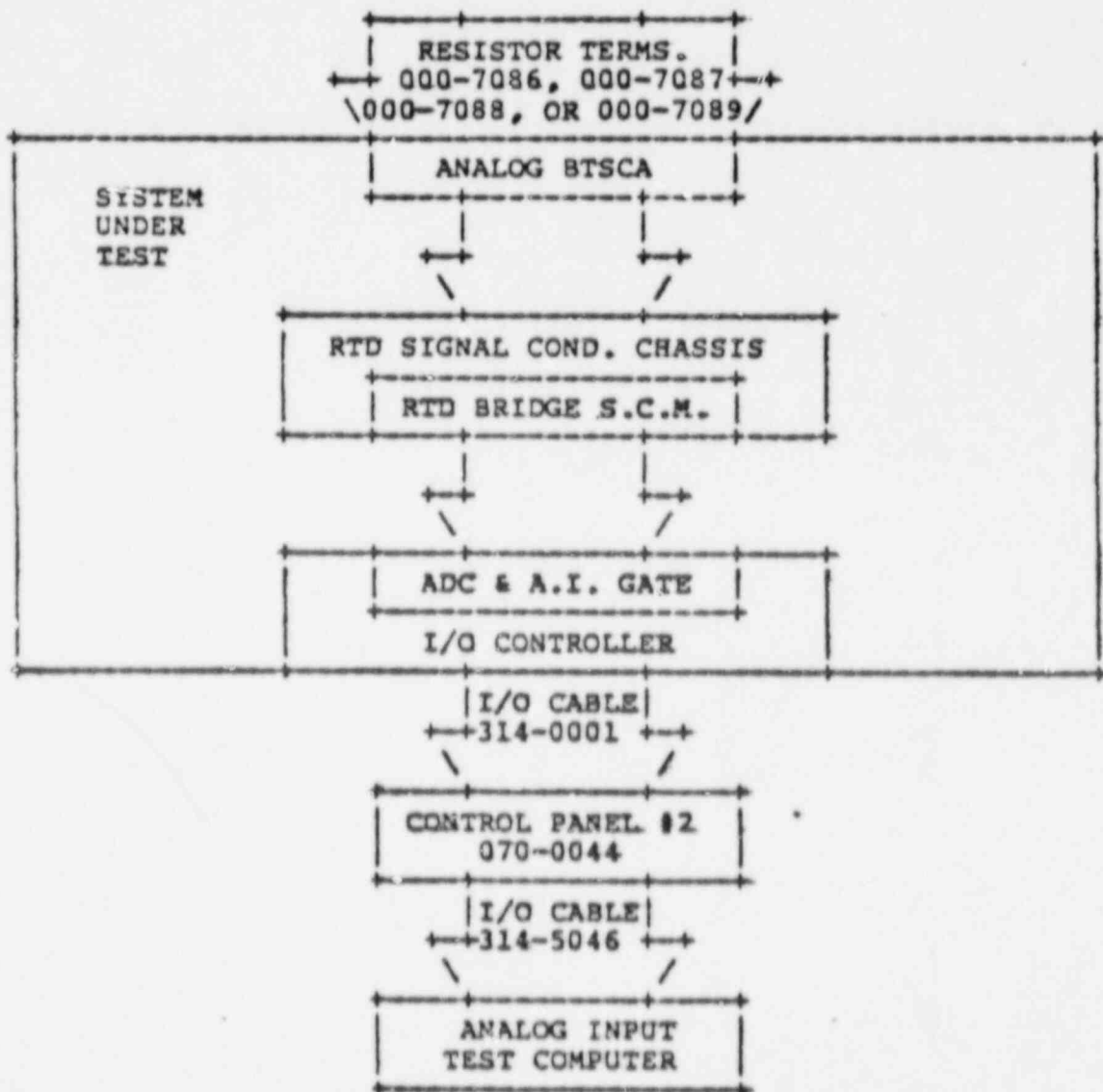
VOLTAGE SENSING ANALOG INPUT
ACCURACY VALIDATION

FIGURE 11



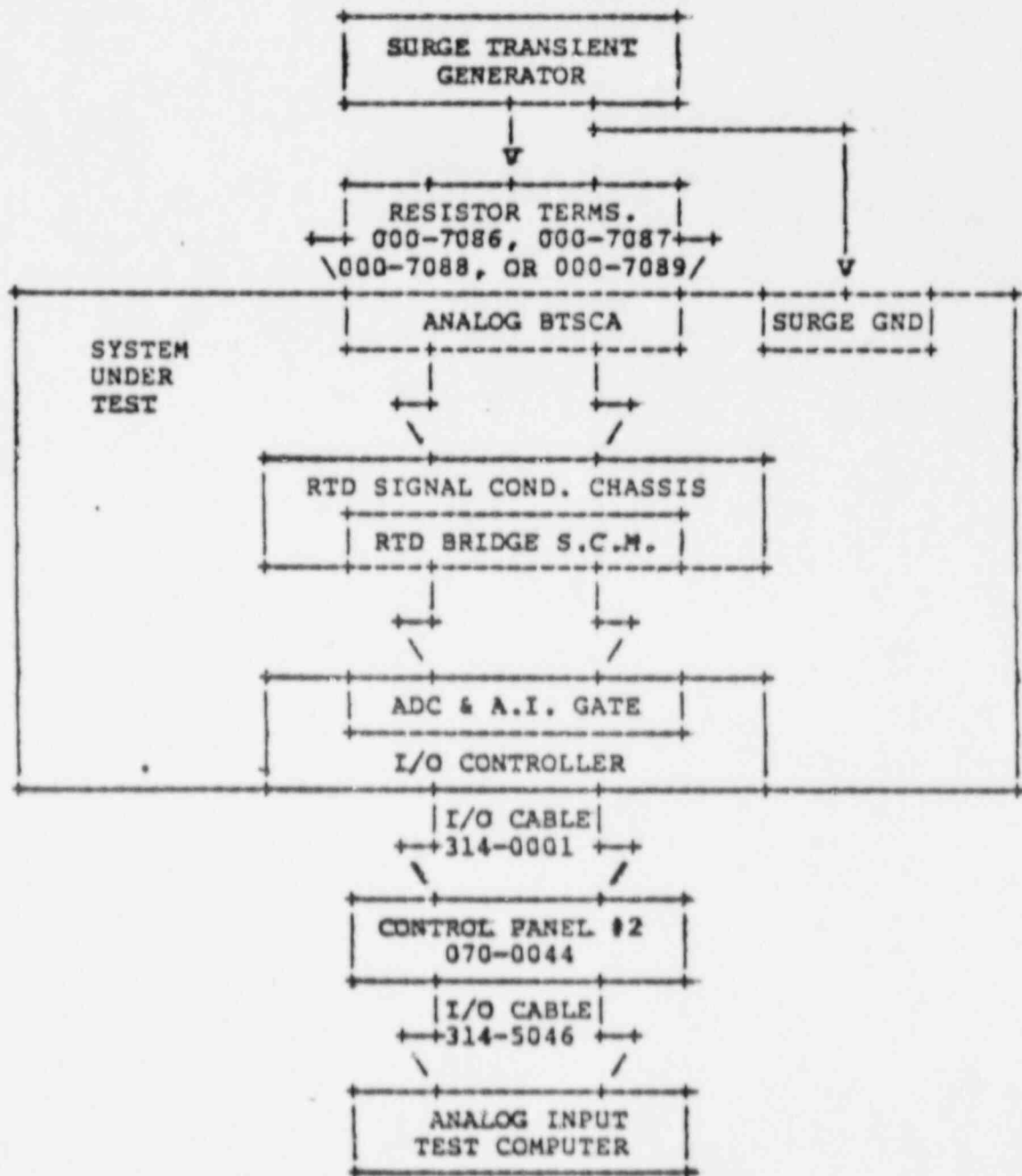
VOLTAGE SENSING ANALOG INPUT
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 12



RESISTIVE SENSING ANALOG INPUT VALIDATION

FIGURE 13



RESISTIVE SENSING ANALOG INPUT
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 14

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP./
BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM
at COMPUTER PRODUCTS, INC. (FT. LAUDERDALE) 2/2/84

ATTACHMENT 2

CABINET CONFIGURATION DRAWINGS

(TO BE SUPPLIED PRIOR TO TESTING)

date printed 3/6/84

UNIT	MODEL		PART NUMBER	DESCRIPTION	ASSEMBLY USED ON	
	NUMBER	NUMBER			CHASSIS	CARDS
1F1	C0002	NEQ	070-5083-000A	REDUNDANT ACCESS UNIVERSAL I/O CONT.		
1F2	C0036	NEQ	075-5271-005A	BTSCA, DALCAL (CASH)	1F1	10
1F3	C0037	NEQ	040-5454-000B	16 SLOT SIGNAL CONDITIONING CHASSIS		
1F4	C0027	NEQ	075-0053-005P	BTSCA, ANALOG	1F1	17
1F5	C0012	NEQ	040-5511-000A	DUAL SOURCE AC DISTRIBUTION AND IND.		
1F6	C0003	NEQ	040-5483-001A	DUAL 5V POWER SUPPLY FOR TWO U-16'S		
1F7	C0003	NEQ	040-5482-001A	DUAL +/-15V P.S. FOR ONE U-16		
1R1				RESERVED POSITION		
1R2	C0015	NEQ	040-5523-000A	BTSCA, SPARE TERMINALS		
1R3	C0063	NEQ	040-5520-005A	BTSCA, ANALOG	1F3	1-P1, 2-P2
1R4	C0033	NEQ	040-5520-005A	BTSCA, ANALOG	1F3	3-P1, 4-P2
1R5	C0065	NEQ	040-5520-005A	BTSCA, ANALOG	1F3	5-P1, 6-P2
1R6	C0013	NEQ	204-0003-000B	CABINET BLOWER		
1X1	C0012	NEQ	559-5002-000A	TEMPERATURE DETECTOR		
NOTES :				RELEASED ENG :	DATE	COMPUTER PRODUCTS FORT LAUDERDALE, FLORIDA
				RELEASED MFG :	DATE	TITLE :
				DRAWN : F. LEMKA	DATE 11/11/83	CABINET LAYOUT
				CHECKED :	DATE	SR-A
				ENGINEER :	DATE	UNIT 2
				APPROVED:	DATE	DRAWING NUMBER AP 283350
						REV E
						SHEET 1 OF 23 SHEETS

CHASSIS NUMBER : 1F1 JOB NUMBER : MCS-283350 CUSTOMER : BALTIMORE GAS & ELECTRIC / NUS
 LOCATION : SAFETY RELATED A , UNIT 2 CHASSIS TYPE : REDUNDANT ACCESS UNIVERSAL I/O CONTROLLER

CARD LOCATION	CARD PART NUMBER	CARD MODEL NUMBER	CARD DESCRIPTION	BTSCA PART NUMBER	BTSCA LOCATION
1			NOT USED		
2	C0012	NEQ 021-5258-000A1	7420/60-000 HIGH SPEED OPTICAL MODEM		
3			NOT USED		
4	C0013	NEQ 022-5002-000A	7411/60-000 INTELLIGENT REMOTE CONT. UNIT		
5			NOT USED		
6	C0035	NEQ 021-0004-000E	7411/60-000 RESISTOR/TERMINATOR		
7	C0058	NEQ 021-0008-001H	I/O BUS DRIVER TERMINATOR		
8	C0058	NEQ 021-0016-000S	STANDARD RTP INTERFACE		
9	C0044	NEQ 021-0032-000S	CHANNEL SELECT		
10	C0016	NEQ 021-5271-000A	7436/10-000 DALCAL (CASH) CARD	075-5271-005	1F2
11	C0038	NEQ 021-0211-008G	7436/21-000 BIPOLAR 14 BIT ADC		
12	C0188	NEQ 021-5234-003C	7436/50-003 H.S.W.R. GATE CARD	040-5455-013	1F3-5
13	C0189	NEQ 021-5234-003C	7436/50-003 H.S.W.R. GATE CARD	040-5455-013	1F3-6
14	C0190	NEQ 021-5234-003C	7436/50-003 H.S.W.R. GATE CARD	040-5455-012	1F3-7
15	C0191	NEQ 021-5234-003C	7436/50-003 H.S.W.R. GATE CARD	040-5455-012	1F3-8
16	C0192	NEQ 021-5234-003C	7436/50-003 H.S.W.R. GATE CARD	040-5455-011	1F3-9
17	C0193	NEQ 021-5234-003C	7436/50-003 H.S.W.R. GATE CARD	075-0053-005	1F4

REV	DESCRIPTION	CHKD	APPD	DATE	DRAWN : F. LEMKA	DATE	SR-A
B				11/19/83	CHECKED :	DATE	UNIT 2
C				12/08/83	ENGINEER :	DATE	CARD LAYOUT
D				12/23/83			DRAWING NUMBER
E				01/02/84	APPROVED :	DATE	AD 283350
							REV F
							SHEET 1 OF 47 SHEETS

CARD LOCATION		CARD PART NUMBER	CARD MODEL NUMBER	CARD DESCRIPTION	BTSCA PART NUMBER	BTSCA LOCATION
1				NOT USED		
2				NOT USED		
3				NOT USED		
4				NOT USED		
5	C0238	NEQ 038-5097-000B1		SURGE PROTECTION CARD (AI)	040-5520-005	1R3(P1)
6	C0091	NEQ 038-5097-000B1		SURGE PROTECTION CARD (AI)	040-5520-005	1R3(P2)
7	C0195	NEQ 038-5097-000B1		SURGE PROTECTION CARD (AI)	040-5520-005	1R4(P1)
8	C0075	NEQ 038-5097-000B1		SURGE PROTECTION CARD (AI)	040-5520-005	1R4(P2)
9	C0106	NEQ 038-5097-000B1		SURGE PROTECTION CARD (AI)	040-5520-005	1R5(P1)
10				NOT USED	040-5520-005	1R5(P2)
11				NOT USED		
12				NOT USED		
13				NOT USED		
14				NOT USED		
15				NOT USED		
16				NOT USED		

REV	DESCRIPTION	CHKD	APPD	DATE	DRAWN : F. LEMKA	DATE	SR-A
F				01/13/84	CHECKED :	11/11/83	UNIT 2
					ENGINEER :	DATE	CARD LAYOUT
					APPROVED :	DATE	DRAWING NUMBER
							AD 283350
							REV
							F
							SHEET 2 OF 47 SHEETS

SOURCE		DESTINATION		CABLE MODEL NUMBER	ROUTING AND PART NUMBER	TERMINATOR LOCATION	DESCRIPTION AND NOTES
1F3	5	1F1	12		040-5455-013B		CABLE, SURGE PROTECTION CARD TO ANALOG INPUT CARD C0167
1F3	6	1F1	13		040-5455-013B		CABLE, SURGE PROTECTION CARD TO ANALOG INPUT CARD C0193
1F3	7	1F1	14		040-5455-012B		CABLE, SURGE PROTECTION CARD TO ANALOG INPUT CARD C0195
1F3	8	1F1	15		040-5455-012B		CABLE, SURGE PROTECTION CARD TO ANALOG INPUT CARD C0202
1F3	9	1F1	16		040-5455-011B		CABLE, SURGE PROTECTION CARD TO ANALOG INPUT CARD C0183
1F1	6			7411/60-000	021-0004-000E		RESISTOR TERMINATOR CARD C0035

NOTES :					RELEASED ENG :	DATE	COMPUTER PRODUCTS FORT LAUDERDALE, FLORIDA	
					RELEASED MFG :	DATE	TITLE :	
					DRAWN : F. LENKA	DATE 11/11/83	SYSTEM I/O CABLE CONFIGURATION	
REV	DESCRIPTION			CHKD	APPD	DATE	CHECKED :	DATE UNIT 2
B						11/19/83	ENGINEER :	DATE
C						12/20/83	APPROVED :	DATE
D						01/02/84		DRAWING NUMBER AV 283350
E						01/13/84		REV E
								SHEET 1 OF 100 SHEETS

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (0) : 1
 Enter the Bit Resolution of the A/D card. < 12, 14> (12) : 14
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) : 0
 Enter the slot address of the first card. < 0, 15> (0) : 0
 Enter the number of cards to be scanned. < 1, 15> (1) :
 SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR
 Select SCAN TYPE. < 0, 3> (0) : 0
 Enter the gain code for the desired system gain. < 0, 3> (1) : 0
 Enter the desired number of scans. < 1, 32767> (100) :
 Return the RTP Control Panel to the COMP mode. RETURN to continue ?

Dalcard
II-171
SLOT 12

A/D
II-171
SLOT 4

CARD CHANNEL	MEAN	P-P
0	0	150.000 uV 1.250 mV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (1) : 2
 Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (1) :
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the slot address of the first card. < 0, 15> (0) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR
 Select SCAN TYPE. < 0, 3> (0) : 0
 Enter the gain code for the desired system gain. < 0, 3> (1) : 1
 Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P
0	0	0.000 uV 0.000 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) : 0
 #q1>

Execution Aborted!
 DALCAL Card TEST PROGRAM for B. G. E. ACCEPTANCE - Version 10-JAN-84

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (1) :
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the slot address of the first card. < 0, 15> (0) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR
 Select SCAN TYPE. < 0, 3> (0) : 0
 Enter the gain code for the desired system gain. < 0, 3> (1) : 2

II-1
Att. 3, p. 1

Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P
0	0 -143.750 uV	312.500 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (0) : 2
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the slot address of the first card. < 0, 15> (0) :
Enter the number of cards to be scanned. < 1, 15> (1) :
SCAN Types - (0) = OFFSET
(1) = PLUS POLARITY
(2) = MINUS POLARITY
(3) = SYSTEM MONITOR

Select SCAN TYPE. < 0, 3> (0) : 0
Enter the gain code for the desired system gain. < 0, 3> (1) : 3
Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P
0	0 -156.250 uV	0.000 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) : 2
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the slot address of the first card. < 0, 15> (0) :
Enter the number of cards to be scanned. < 1, 15> (1) :
SCAN Types - (0) = OFFSET
(1) = PLUS POLARITY
(2) = MINUS POLARITY
(3) = SYSTEM MONITOR

Select SCAN TYPE. < 0, 3> (0) : 1
Select (0) = FULLSCALE, (1) = HALFSCALE. < 0, 1> (0) :
Enter the gain code for the desired system gain. < 0, 3> (1) :
Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P
0	0 5.001 uV	0.000 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) :
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the slot address of the first card. < 0, 15> (0) :
Enter the number of cards to be scanned. < 1, 15> (1) :
SCAN Types - (0) = OFFSET
(1) = PLUS POLARITY
(2) = MINUS POLARITY
(3) = SYSTEM MONITOR

Select SCAN TYPE. < 0, 3> (0) : 1
Select (0) = FULLSCALE, (1) = HALFSCALE. < 0, 1> (0) :
Enter the gain code for the desired system gain. < 0, 3> (1) : 0
Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL MEAN P-P
0 0 10.001 V 0.000 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) : 2
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the slot address of the first card. < 0, 15> (0) :
Enter the number of cards to be scanned. < 1, 15> (1) :
SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR
Select SCAN TYPE. < 0, 3> (0) : 1
Select (0) = FULLSCALE, (1) = HALFSCALE. < 0, 1> (0) :
Enter the gain code for the desired system gain. < 0, 3> (1) : 2
Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL MEAN P-P
0 0 2.500 V 312.500 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) : 2
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the slot address of the first card. < 0, 15> (0) :
Enter the number of cards to be scanned. < 1, 15> (1) :
SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR
Select SCAN TYPE. < 0, 3> (0) : 1
Select (0) = FULLSCALE, (1) = HALFSCALE. < 0, 1> (0) :
Enter the gain code for the desired system gain. < 0, 3> (1) : 3
Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL MEAN P-P
0 0 1.250 V 312.500 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) : 2
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the slot address of the first card. < 0, 15> (0) :
Enter the number of cards to be scanned. < 1, 15> (1) :
SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR
Select SCAN TYPE. < 0, 3> (0) : 2
Select (0) = FULLSCALE, (1) = HALFSCALE. < 0, 1> (0) :
Enter the gain code for the desired system gain. < 0, 3> (1) : 0
Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL MEAN P-P

0 0 -10.000 V 0.000 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) : 2
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the slot address of the first card. < 0, 15> (0) :
Enter the number of cards to be scanned. < 1, 15> (1) :
SCAN Types - (0) = OFFSET
(1) = PLUS POLARITY
(2) = MINUS POLARITY
(3) = SYSTEM MONITOR
Select SCAN TYPE. < 0, 3> (0) : 2
Select (0) = FULLSCALE, (1) = HALFSCALE. < 0, 1> (0) :
Enter the gain code for the desired system gain. < 0, 3> (1) : 1
Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P
0	0 -5.001 V	625.000 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) : 2
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the slot address of the first card. < 0, 15> (0) :
Enter the number of cards to be scanned. < 1, 15> (1) :
SCAN Types - (0) = OFFSET
(1) = PLUS POLARITY
(2) = MINUS POLARITY
(3) = SYSTEM MONITOR
Select SCAN TYPE. < 0, 3> (0) : 2
Select (0) = FULLSCALE, (1) = HALFSCALE. < 0, 1> (0) :
Enter the gain code for the desired system gain. < 0, 3> (1) : 2
Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P
0	0 -2.500 V	312.500 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) : 2
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the slot address of the first card. < 0, 15> (0) :
Enter the number of cards to be scanned. < 1, 15> (1) :
SCAN Types - (0) = OFFSET
(1) = PLUS POLARITY
(2) = MINUS POLARITY
(3) = SYSTEM MONITOR
Select SCAN TYPE. < 0, 3> (0) : 2
Select (0) = FULLSCALE, (1) = HALFSCALE. < 0, 1> (0) :
Enter the gain code for the desired system gain. < 0, 3> (1) : 3
Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P
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0 0 -1.250 V 156.250 uV

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) :

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Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (1) :
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the slot address of the first card. < 0, 15> (0) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR

Section 17
 Dual
 Temperature
 II-1F1
 Slot 10
 A/D
 Slot 11

Select SCAN TYPE. < 0, 3> (0) : 3
 Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P	FUNCTION	NOMINAL
0	1.006 V	625.000 uV	+15 volts	+1 volt
0	-1.007 V	0.000 uV	-15 volts	-1 volt
0	996.844 mV	1.250 mV	+5 volts	+1 volt
0	418.606 mV	625.000 uV	+12 volts	+1 volt
0	-625.000 uV	0.000 uV	48/125 volts	+1 volt
0	-625.000 uV	0.000 uV	48/125 volts	+1 volt
0	23.973 C	0.063 C	TEMP A	
0	-273.212 C	0.000 C	TEMP B	

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) :

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U.A.I.C.S. TEST PROGRAM for B. G. E. ACCEPTANCE - Version 12-JAN-84

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) : II-1F1
 Enter the slot address of the A/D card. < 0, 15> (0) : 1
 Enter the Bit Resolution of the A/D card. < 12, 14> (12) : 14
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the desired system sample rate in hertz. < 1, 200> (100) : 50
 Enter the slot address of the first gate card. < 0, 511> (0) : 7
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (0) :
 Enter the desired number of scans. < 1, 32767> (1) : 100
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = 1003.330 Bits, 1.254 V
 Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 7, Channel 0.
 Channel - Channel OFFSET = 8134.090 Bits, 10.168 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
7	0	4010.020 Bits	1 Bits	5.013 V	1.250 mV	0.140
7	1	3999.580 Bits	1 Bits	4.999 V	1.250 mV	0.494
7	2	4059.180 Bits	1 Bits	5.074 V	1.250 mV	0.384
7	3	-4050.220 Bits	1 Bits	-5.063 V	1.250 mV	0.414
7	4	4068.000 Bits	0 Bits	5.085 V	0.000 uV	0.000
7	5	-4066.090 Bits	1 Bits	-5.083 V	1.250 mV	0.286
7	6	38.170 Bits	1 Bits	47.712 mV	1.250 mV	0.376
7	7	-32.000 Bits	0 Bits	-40.000 mV	0.000 uV	0.000

Average MEAN = 1003.330 Bits, 1.254 V
 Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 7, Channel 0.
 Channel - Channel OFFSET = 8134.090 Bits, 10.168 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 499.794 Bits, 624.742 mV
 Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 7, Channel 1.
 Channel - Channel OFFSET = 8139.850 Bits, 10.175 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
7	0	3.000 Bits	0 Bits	3.750 mV	0.000 uV	0.000
7	1	4000.060 Bits	1 Bits	5.000 V	1.250 mV	0.237
7	2	4059.220 Bits	1 Bits	5.074 V	1.250 mV	0.414
7	3	-4071.890 Bits	1 Bits	-5.090 V	1.250 mV	0.313
7	4	4067.960 Bits	1 Bits	5.085 V	1.250 mV	0.196
7	5	-4066.160 Bits	1 Bits	-5.083 V	1.250 mV	0.367
7	6	38.160 Bits	1 Bits	47.700 mV	1.250 mV	0.367
7	7	-32.000 Bits	0 Bits	-40.000 mV	0.000 uV	0.000

Average MEAN = 499.794 Bits, 624.742 mV
 Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 7, Channel 1.
 Channel - Channel OFFSET = 8139.850 Bits, 10.175 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 500.960 Bits, 626.200 mV
 Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 7, Channel 0.
 Channel - Channel OFFSET = 8140.230 Bits, 10.175 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
7	0	4008.990 Bits	1 Bits	5.011 V	1.250 mV	0.099
7	1	3.500 Bits	1 Bits	4.375 mV	1.250 mV	0.500
7	2	4059.460 Bits	1 Bits	5.074 V	1.250 mV	0.498
7	3	-4072.230 Bits	1 Bits	-5.090 V	1.250 mV	0.421
7	4	4038.000 Bits	0 Bits	5.085 V	0.000 uV	0.000
7	5	-4066.170 Bits	1 Bits	-5.083 V	1.250 mV	0.376
7	6	38.130 Bits	1 Bits	47.662 mV	1.250 mV	0.336
7	7	-32.000 Bits	0 Bits	-40.000 mV	0.000 uV	0.000

Average MEAN = 500.960 Bits, 626.200 mV
 Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 7, Channel 0.
 Channel - Channel OFFSET = 8140.230 Bits, 10.175 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 1004.669 Bits, 1.256 V
 Maximum PEAK to PEAK = 98 Bits, 122.500 mV on Card 7, Channel 2.
 Channel - Channel OFFSET = 8133.180 Bits, 10.166 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
7	0	4009.300 Bits	1 Bits	5.012 V	1.250 mV	0.458
7	1	4000.020 Bits	1 Bits	5.000 V	1.250 mV	0.140
7	2	474.550 Bits	98 Bits	593.187 mV	122.500 mV	28.492
7	3	-453.650 Bits	93 Bits	-567.062 mV	116.250 mV	27.315
7	4	4067.130 Bits	1 Bits	5.084 V	1.250 mV	0.336
7	5	-4066.050 Bits	1 Bits	-5.083 V	1.250 mV	0.218
7	6	38.050 Bits	1 Bits	47.562 mV	1.250 mV	0.218
7	7	-32.000 Bits	0 Bits	-40.000 mV	0.000 uV	0.000

Average MEAN = 1004.669 Bits, 1.256 V
 Maximum PEAK to PEAK = 98 Bits, 122.500 mV on Card 7, Channel 2.
 Channel - Channel OFFSET = 8133.180 Bits, 10.166 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 990.750 Bits, 1.238 V
 Maximum PEAK to PEAK = 49 Bits, 61.250 mV on Card 7, Channel 5.
 Channel - Channel OFFSET = 8130.610 Bits, 10.163 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
7	0	4009.990 Bits	1 Bits	5.012 V	1.250 mV	0.099
7	1	4000.010 Bits	1 Bits	5.000 V	1.250 mV	0.099
7	2	4058.560 Bits	1 Bits	5.073 V	1.250 mV	0.496
7	3	-4072.050 Bits	1 Bits	-5.090 V	1.250 mV	0.218
7	4	219.810 Bits	37 Bits	274.762 mV	46.250 mV	10.952
7	5	-296.430 Bits	49 Bits	-370.537 mV	61.250 mV	14.372
7	6	38.110 Bits	1 Bits	47.638 mV	1.250 mV	0.313

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7 7 -32.000 Bits 0 Bits -40.000 mV 0.000 uV 0.000

Average MEAN = 990.750 Bits, 1.238 V
Maximum PEAK to PEAK = 49 Bits, 61.250 mV on Card 7, Channel 5.
Channel - Channel OFFSET = 8130.610 Bits, 10.163 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 1000.525 Bits, 1.251 V
Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 7, Channel 0.
Channel - Channel OFFSET = 8138.100 Bits, 10.173 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
7	0	4009.990 Bits	1 Bits	5.012 V	1.250 mV	0.099
7	1	4000.000 Bits	0 Bits	5.000 V	0.000 uV	0.000
7	2	4059.000 Bits	0 Bits	5.074 V	0.000 uV	0.000
7	3	-4072.030 Bits	1 Bits	-5.090 V	1.250 mV	0.171
7	4	4066.070 Bits	1 Bits	5.083 V	1.250 mV	0.255
7	5	-4065.000 Bits	0 Bits	-5.081 V	0.000 uV	0.000
7	6	38.130 Bits	1 Bits	47.662 mV	1.250 mV	0.336
7	7	-31.960 Bits	1 Bits	-39.950 mV	1.250 mV	0.196

Average MEAN = 1000.525 Bits, 1.251 V
Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 7, Channel 0.
Channel - Channel OFFSET = 8138.100 Bits, 10.173 V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) :

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) :

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3	0	4095.550 Bits	2 Bits	39.996 mV	19.531 uV	0.589
3	1	3582.010 Bits	1 Bits	34.981 mV	9.766 uV	0.099
3	2	3071.180 Bits	1 Bits	29.992 mV	9.766 uV	0.384
3	3	2563.030 Bits	1 Bits	25.030 mV	9.766 uV	0.171
3	4	2051.840 Bits	1 Bits	20.038 mV	9.766 uV	0.367
3	5	1536.110 Bits	2 Bits	15.001 mV	19.531 uV	0.343
3	6	1028.080 Bits	2 Bits	10.040 mV	19.531 uV	0.337
3	7	516.940 Bits	1 Bits	5.048 mV	9.766 uV	0.237

Average MEAN = 1155.369 Bits, 11.283 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 3, Channel 0.
 Channel - Channel OFFSET = 4091.580 Bits, 39.957 mV

Enter (1)=PRINTOUT, (2)=PESCAN, (3)=RESTART. < 0, 3> (1) : 3
 Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (1) :
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the desired system sample rate in hertz. < 1, 200> (50) :
 Enter the slot address of the first gate card. < 0, 511> (2) : 4
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (2) :
 Enter the gain code for the desired system gain. < 0, 11> (8) :
 Enter the desired number of scans. < 1, 32767> (100) :
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = 1144.526 Bits, 11.177 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 4, Channel 5.
 Channel - Channel OFFSET = 4096.630 Bits, 40.006 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
4	0	4082.970 Bits	1 Bits	39.873 mV	9.766 uV	0.171
4	1	3578.000 Bits	0 Bits	34.942 mV	0.000 uV	0.000
4	2	3067.040 Bits	1 Bits	29.952 mV	9.766 uV	0.196
4	3	2549.380 Bits	1 Bits	24.896 mV	9.766 uV	0.485
4	4	2043.590 Bits	1 Bits	19.957 mV	9.766 uV	0.492
4	5	1528.000 Bits	2 Bits	14.922 mV	19.531 uV	0.141
4	6	1023.000 Bits	0 Bits	9.990 mV	0.000 uV	0.000
4	7	507.090 Bits	1 Bits	4.952 mV	9.766 uV	0.286
5	0	-13.660 Bits	1 Bits	-133.399 uV	9.766 uV	0.474
5	1	-7.160 Bits	1 Bits	-69.922 uV	9.766 uV	0.367
5	2	-7.400 Bits	1 Bits	-72.266 uV	9.766 uV	0.490
5	3	-11.070 Bits	1 Bits	-108.106 uV	9.766 uV	0.255
5	4	-5.260 Bits	1 Bits	-51.367 uV	9.766 uV	0.439
5	5	-6.990 Bits	2 Bits	-68.262 uV	19.531 uV	0.264
5	6	-9.060 Bits	1 Bits	-88.477 uV	9.766 uV	0.237
5	7	-6.060 Bits	1 Bits	-59.180 uV	9.766 uV	0.237

Average MEAN = 1144.526 Bits, 11.177 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 4, Channel 5.
 Channel - Channel OFFSET = 4096.630 Bits, 40.006 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 1147.159 Bits, 11.203 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 4, Channel 5.

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) : *Section 19*
 Enter the slot address of the A/D card. < 0, 15> (1) :
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) : *II-1F1*
 Enter the desired system sample rate in hertz. < 1, 200> (50) : *5KTS*
 Enter the slot address of the first gate card. < 0, 511> (7) : *2 12-16*
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) : 2
 Enter the gain code for the desired system gain. < 0, 11> (0) : 8
 Enter the desired number of scans. < 1, 32767> (100) :
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = 1155.403 Bits, 11.283 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 3, Channel 0.
 Channel - Channel OFFSET = 4096.660 Bits, 40.007 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
2	0	4097.650 Bits	1 Bits	40.016 mV	9.766 uV	0.477
2	1	3585.000 Bits	0 Bits	35.010 mV	0.000 uV	0.000
2	2	3074.530 Bits	1 Bits	30.025 mV	9.766 uV	0.499
2	3	2564.100 Bits	1 Bits	25.040 mV	9.766 uV	0.300
2	4	2052.350 Bits	1 Bits	20.043 mV	9.766 uV	0.477
2	5	1540.740 Bits	1 Bits	15.046 mV	9.766 uV	0.439
2	6	1028.950 Bits	1 Bits	10.048 mV	9.766 uV	0.218
2	7	517.170 Bits	1 Bits	5.051 mV	9.766 uV	0.376
3	0	3.990 Bits	2 Bits	38.965 uV	19.531 uV	0.173
3	1	0.990 Bits	2 Bits	9.668 uV	19.531 uV	0.173
3	2	3.840 Bits	1 Bits	37.500 uV	9.766 uV	0.367
3	3	2.900 Bits	1 Bits	28.320 uV	9.766 uV	0.300
3	4	4.000 Bits	0 Bits	39.063 uV	0.000 uV	0.000
3	5	2.230 Bits	1 Bits	21.777 uV	9.766 uV	0.421
3	6	4.000 Bits	2 Bits	39.063 uV	19.531 uV	0.283
3	7	4.010 Bits	1 Bits	39.160 uV	9.766 uV	0.099

Average MEAN = 1155.403 Bits, 11.283 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 3, Channel 0.
 Channel - Channel OFFSET = 4096.660 Bits, 40.007 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 1155.369 Bits, 11.283 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 3, Channel 0.
 Channel - Channel OFFSET = 4091.580 Bits, 39.957 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
2	0	5.750 Bits	1 Bits	56.153 uV	9.766 uV	0.433
2	1	3.970 Bits	1 Bits	38.770 uV	9.766 uV	0.171
2	2	5.750 Bits	1 Bits	56.153 uV	9.766 uV	0.433
2	3	5.470 Bits	1 Bits	53.418 uV	9.766 uV	0.499
2	4	4.380 Bits	1 Bits	42.774 uV	9.766 uV	0.485
2	5	5.640 Bits	1 Bits	55.078 uV	9.766 uV	0.480
2	6	4.940 Bits	1 Bits	48.242 uV	9.766 uV	0.237
2	7	5.260 Bits	1 Bits	51.367 uV	9.766 uV	0.439

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Channel - Channel OFFSET = 4087.270 Bits, 39.915 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
4 0	-5.290 Bits	1 Bits	-51.660 uV	9.766 uV	0.454
4 1	-1.080 Bits	1 Bits	-10.547 uV	9.766 uV	0.271
4 2	-1.020 Bits	1 Bits	-9.961 uV	9.766 uV	0.140
4 3	-5.250 Bits	1 Bits	-51.270 uV	9.766 uV	0.433
4 4	-2.130 Bits	1 Bits	-20.601 uV	9.766 uV	0.336
4 5	-4.040 Bits	2 Bits	-39.453 uV	19.531 uV	0.242
4 6	-0.230 Bits	1 Bits	-2.246 uV	9.766 uV	0.421
4 7	-2.340 Bits	1 Bits	-22.852 uV	9.766 uV	0.474
5 0	4081.980 Bits	1 Bits	39.863 mV	9.766 uV	0.140
5 1	3576.050 Bits	1 Bits	34.922 mV	9.766 uV	0.218
5 2	3063.810 Bits	1 Bits	29.920 mV	9.766 uV	0.392
5 3	2553.000 Bits	0 Bits	24.932 mV	0.000 uV	0.000
5 4	2044.050 Bits	1 Bits	19.961 mV	9.766 uV	0.218
5 5	1530.990 Bits	1 Bits	14.951 mV	9.766 uV	0.099
5 6	1017.170 Bits	1 Bits	9.933 mV	9.766 uV	0.376
5 7	508.870 Bits	1 Bits	4.969 mV	9.766 uV	0.336

Average MEAN = 1147.159 Bits, 11.203 mV

Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 4, Channel 5.

Channel - Channel OFFSET = 4087.270 Bits, 39.915 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 3

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :

Enter the slot address of the A/D card. < 0, 15> (1) :

Enter the Bit Resolution of the A/D card. < 12, 14> (14) :

Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :

Enter the desired system sample rate in hertz. < 1, 200> (50) :

Enter the slot address of the first gate card. < 0, 511> (4) : 6

Enter the number of channels per card. < 4, 8> (8) :

Enter the number of cards to be scanned. < 1, 15> (2) : 1

Enter the gain code for the desired system gain. < 0, 11> (8) :

Enter the desired number of scans. < 1, 32767> (100) :

Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = 2301.299 Bits, 22.474 mV

Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 5.

Channel - Channel OFFSET = 3576.920 Bits, 34.931 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6 0	4089.600 Bits	1 Bits	39.938 mV	9.766 uV	0.490
6 1	3575.080 Bits	1 Bits	34.913 mV	9.766 uV	0.271
6 2	3069.000 Bits	0 Bits	29.971 mV	0.000 uV	0.000
6 3	2556.960 Bits	1 Bits	24.970 mV	9.766 uV	0.196
6 4	2049.090 Bits	1 Bits	20.011 mV	9.766 uV	0.286
6 5	1532.990 Bits	2 Bits	14.971 mV	19.531 uV	0.173
6 6	1024.990 Bits	1 Bits	10.010 mV	9.766 uV	0.099
6 7	512.680 Bits	1 Bits	5.007 mV	9.766 uV	0.466

Average MEAN = 2301.299 Bits, 22.474 mV

Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 5.

Channel - Channel OFFSET = 3576.920 Bits, 34.931 mV

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Att. 3, p.

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (1) :
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the desired system sample rate in hertz. < 1, 200> (50) :
 Enter the slot address of the first gate card. < 0, 511> (6) :
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (8) :
 Enter the desired number of scans. < 1, 32767> (100) :
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (2) : 1

Section 20
II-1#10
SLOT 16
CM acc.
Surge
CM acc

Average MEAN = 0.160 Bits, 1.563 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 1.690 Bits, 16.504 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-0.340 Bits	1 Bits	-3.320 uV	9.766 uV	0.474
6	1	-0.900 Bits	2 Bits	-8.789 uV	19.531 uV	0.332
6	2	0.490 Bits	2 Bits	4.785 uV	19.531 uV	0.520
6	3	-0.010 Bits	2 Bits	-0.098 uV	19.531 uV	0.332
6	4	0.780 Bits	1 Bits	7.617 uV	9.766 uV	0.414
6	5	0.410 Bits	2 Bits	4.004 uV	19.531 uV	0.512
6	6	0.790 Bits	1 Bits	7.715 uV	9.766 uV	0.407
6	7	0.060 Bits	2 Bits	0.586 uV	19.531 uV	0.420

Average MEAN = 0.160 Bits, 1.563 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 1.690 Bits, 16.504 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 7165.735 Bits, 69.978 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 0.
 Channel - Channel OFFSET = 1.050 Bits, 10.257 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	7166.000 Bits	2 Bits	69.981 mV	19.531 uV	0.245
6	1	7165.030 Bits	2 Bits	69.971 mV	19.531 uV	0.263
6	2	7166.050 Bits	2 Bits	69.981 mV	19.531 uV	0.296
6	3	7165.200 Bits	1 Bits	69.973 mV	9.766 uV	0.400
6	4	7166.050 Bits	2 Bits	69.981 mV	19.531 uV	0.260
6	5	7165.470 Bits	1 Bits	69.975 mV	9.766 uV	0.499
6	6	7166.080 Bits	2 Bits	69.981 mV	19.531 uV	0.306
6	7	7166.000 Bits	2 Bits	69.981 mV	19.531 uV	0.316

Average MEAN = 7165.735 Bits, 69.978 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 0.
 Channel - Channel OFFSET = 1.050 Bits, 10.257 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = -7165.779 Bits, -69.979 mV
 Maximum PEAK to PEAK = 3 Bits, 29.297 uV on Card 6, Channel 0.

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Att. 3, p. 14

Channel - Channel OFFSET = 2.240 Bits, 21.873 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-7167.130 Bits	3 Bits	-69.992 mV	29.297 uV	0.523
6	1	-7167.000 Bits	3 Bits	-69.990 mV	29.297 uV	0.600
6	2	-7165.330 Bits	2 Bits	-69.974 mV	19.531 uV	0.549
6	3	-7165.610 Bits	2 Bits	-69.977 mV	19.531 uV	0.581
6	4	-7165.160 Bits	2 Bits	-69.972 mV	19.531 uV	0.418
6	5	-7164.960 Bits	3 Bits	-69.971 mV	29.297 uV	0.546
6	6	-7164.890 Bits	2 Bits	-69.970 mV	19.531 uV	0.508
6	7	-7166.150 Bits	3 Bits	-69.982 mV	29.297 uV	0.433

Average MEAN = -7165.779 Bits, -69.979 mV

Maximum PEAK to PEAK = 3 Bits, 29.297 uV on Card 6, Channel 0.

Channel - Channel OFFSET = 2.240 Bits, 21.873 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 3

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :

Enter the slot address of the A/D card. < 0, 15> (1) :

Enter the Bit Resolution of the A/D card. < 12, 14> (14) :

Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :

Enter the desired system sample rate in hertz. < 1, 200> (50) :

Enter the slot address of the first gate card. < 0, 511> (6) :

Enter the number of channels per card. < 4, 8> (8) :

Enter the number of cards to be scanned. < 1, 15> (1) :

Enter the gain code for the desired system gain. < 0, 11> (8) : 4

Enter the desired number of scans. < 1, 32767> (100) :

Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = 0.161 Bits, 12.598 uV

Maximum PEAK to PEAK = 1 Bits, 78.125 uV on Card 6, Channel 0.

Channel - Channel OFFSET = 0.510 Bits, 39.844 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	0.020 Bits	1 Bits	1.562 uV	78.125 uV	0.140
6	1	0.010 Bits	1 Bits	0.781 uV	78.125 uV	0.099
6	2	0.050 Bits	1 Bits	3.906 uV	78.125 uV	0.218
6	3	0.130 Bits	1 Bits	10.156 uV	78.125 uV	0.336
6	4	0.310 Bits	1 Bits	24.219 uV	78.125 uV	0.462
6	5	0.170 Bits	1 Bits	13.281 uV	78.125 uV	0.376
6	6	0.520 Bits	1 Bits	40.625 uV	78.125 uV	0.500
6	7	0.080 Bits	1 Bits	6.250 uV	78.125 uV	0.271

Average MEAN = 0.161 Bits, 12.598 uV

Maximum PEAK to PEAK = 1 Bits, 78.125 uV on Card 6, Channel 0.

Channel - Channel OFFSET = 0.510 Bits, 39.844 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 7165.710 Bits, 559.821 mV

Maximum PEAK to PEAK = 2 Bits, 156.250 uV on Card 6, Channel 1.

Channel - Channel OFFSET = 0.950 Bits, 74.196 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6 0	7166.090 Bits	1 Bits	559.851 mV	78.125 uV	0.286
6 1	7165.990 Bits	2 Bits	559.843 mV	156.250 uV	0.264
6 2	7166.040 Bits	1 Bits	559.847 mV	78.125 uV	0.196
6 3	7165.170 Bits	1 Bits	559.779 mV	78.125 uV	0.376
6 4	7165.630 Bits	2 Bits	559.815 mV	156.250 uV	0.523
6 5	7165.140 Bits	1 Bits	559.777 mV	78.125 uV	0.347
6 6	7165.550 Bits	2 Bits	559.809 mV	156.250 uV	0.536
6 7	7166.070 Bits	1 Bits	559.849 mV	78.125 uV	0.255

Average MEAN = 7165.710 Bits, 559.821 mV
 Maximum PEAK to PEAK = 2 Bits, 156.250 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 0.950 Bits, 74.196 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = -7164.448 Bits, -559.722 mV
 Maximum PEAK to PEAK = 2 Bits, 156.250 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 1.090 Bits, 85.182 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6 0	-7165.120 Bits	1 Bits	-559.775 mV	78.125 uV	0.325
6 1	-7164.880 Bits	2 Bits	-559.756 mV	156.250 uV	0.407
6 2	-7164.290 Bits	2 Bits	-559.710 mV	156.250 uV	0.475
6 3	-7164.100 Bits	1 Bits	-559.695 mV	78.125 uV	0.300
6 4	-7164.130 Bits	1 Bits	-559.698 mV	78.125 uV	0.336
6 5	-7164.030 Bits	2 Bits	-559.690 mV	156.250 uV	0.263
6 6	-7164.100 Bits	1 Bits	-559.695 mV	78.125 uV	0.300
6 7	-7164.930 Bits	2 Bits	-559.760 mV	156.250 uV	0.281

Average MEAN = -7164.448 Bits, -559.722 mV
 Maximum PEAK to PEAK = 2 Bits, 156.250 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 1.090 Bits, 85.182 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 3
 Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (1) :
 Enter the bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the desired system sample rate in hertz. < 1, 200> (50) :
 Enter the slot address of the first gate card. < 0, 511> (6) :
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (4) : 0
 Enter the desired number of scans. < 1, 32767> (100) :
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = 0.264 Bits, 329.687 uV
 Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 6, Channel 0.
 Channel - Channel OFFSET = 0.270 Bits, 337.500 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6 0	0.210 Bits	1 Bits	262.500 uV	1.250 mV	0.407
6 1	0.260 Bits	1 Bits	325.000 uV	1.250 mV	0.439

6	2	0.430 Bits	1 Bits	537.500 uV	1.250 mV	0.495
6	3	0.160 Bits	1 Bits	300.000 uV	1.250 mV	0.367
6	4	0.350 Bits	1 Bits	437.500 uV	1.250 mV	0.477
6	5	0.180 Bits	1 Bits	225.000 uV	1.250 mV	0.384
6	6	0.360 Bits	1 Bits	450.000 uV	1.250 mV	0.480
6	7	0.160 Bits	1 Bits	200.000 uV	1.250 mV	0.367

Average MEAN = 0.264 Bits, 329.687 uV
 Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 6, Channel 0.
 Channel - Channel OFFSET = 0.270 Bits, 337.500 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 7167.740 Bits, 8.960 V
 Maximum PEAK to PEAK = 2 Bits, 2.500 mV on Card 6, Channel 0.
 Channel - Channel OFFSET = 1.510 Bits, 1.887 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	7168.510 Bits	2 Bits	8.961 V	2.500 mV	0.520
6	1	7168.070 Bits	1 Bits	8.960 V	1.250 mV	0.255
6	2	7167.000 Bits	0 Bits	8.959 V	0.000 uV	0.000
6	3	7167.950 Bits	1 Bits	8.960 V	1.250 mV	0.218
6	4	7168.130 Bits	1 Bits	8.960 V	1.250 mV	0.336
6	5	7167.050 Bits	1 Bits	8.959 V	1.250 mV	0.218
6	6	7167.040 Bits	1 Bits	8.959 V	1.250 mV	0.196
6	7	7168.170 Bits	1 Bits	8.960 V	1.250 mV	0.376

Average MEAN = 7167.740 Bits, 8.960 V
 Maximum PEAK to PEAK = 2 Bits, 2.500 mV on Card 6, Channel 0.
 Channel - Channel OFFSET = 1.510 Bits, 1.887 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = -7167.612 Bits, -8.960 V
 Maximum PEAK to PEAK = 2 Bits, 2.500 mV on Card 6, Channel 2.
 Channel - Channel OFFSET = 2.900 Bits, 3.625 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-7168.280 Bits	1 Bits	-8.960 V	1.250 mV	0.449
6	1	-7168.300 Bits	1 Bits	-8.960 V	1.250 mV	0.458
6	2	-7167.660 Bits	2 Bits	-8.960 V	2.500 mV	0.620
6	3	-7166.100 Bits	1 Bits	-8.958 V	1.250 mV	0.300
6	4	-7166.400 Bits	1 Bits	-8.958 V	1.250 mV	0.490
6	5	-7168.150 Bits	1 Bits	-8.960 V	1.250 mV	0.357
6	6	-7167.010 Bits	2 Bits	-8.959 V	2.500 mV	0.173
6	7	-7169.000 Bits	0 Bits	-8.961 V	0.000 uV	0.000

Average MEAN = -7167.612 Bits, -8.960 V
 Maximum PEAK to PEAK = 2 Bits, 2.500 mV on Card 6, Channel 2.
 Channel - Channel OFFSET = 2.900 Bits, 3.625 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 3

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :

Enter the slot address of the A/D Card. < 0, 15> (1) :

Enter the Bit Resolution of the A/D card. < 12, 14> (14) :

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Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the desired system sample rate in hertz. < 1, 200> (50) :
 Enter the slot address of the first gate card. < 0, 511> (6) :
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (0) : 8
 Enter the desired number of scans. < 1, 32767> (100) :
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) : 2
 Enter the applied common mode voltage (P-P). < 1, 1700> (1697) :

Average MEAN = -7.525 Bits, -73.487 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 4.680 Bits, 45.703 uV
 Minimum Common Mode Rejection = 158.78dB on Card 6, Channel 1.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-8.330 Bits	1 Bits	-81.348 uV	9.766 uV	0.470
6	1	-8.570 Bits	2 Bits	-83.692 uV	19.531 uV	0.534
6	2	-6.720 Bits	2 Bits	-65.625 uV	19.531 uV	0.511
6	3	-8.480 Bits	1 Bits	-82.813 uV	9.766 uV	0.500
6	4	-6.230 Bits	1 Bits	-60.840 uV	9.766 uV	0.421
6	5	-10.030 Bits	2 Bits	-97.950 uV	19.531 uV	0.298
6	6	-5.350 Bits	1 Bits	-52.246 uV	9.766 uV	0.477
6	7	-6.490 Bits	1 Bits	-63.379 uV	9.766 uV	0.500

Average MEAN = -7.525 Bits, -73.487 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 4.680 Bits, 45.703 uV
 Minimum Common Mode Rejection = 158.78dB on Card 6, Channel 1.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = -5.749 Bits, -56.140 uV
 Maximum PEAK to PEAK = 5 Bits, 48.828 uV on Card 6, Channel 0.
 Channel - Channel OFFSET = 4.910 Bits, 47.949 uV
 Minimum Common Mode Rejection = 150.82dB on Card 6, Channel 0.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-5.940 Bits	5 Bits	-58.008 uV	48.828 uV	1.271
6	1	-7.020 Bits	4 Bits	-68.555 uV	39.063 uV	1.131
6	2	-4.750 Bits	5 Bits	-46.387 uV	48.828 uV	1.268
6	3	-6.600 Bits	4 Bits	-64.453 uV	39.063 uV	1.208
6	4	-4.440 Bits	5 Bits	-43.360 uV	48.828 uV	1.169
6	5	-8.420 Bits	5 Bits	-82.227 uV	48.828 uV	1.218
6	6	-3.510 Bits	4 Bits	-34.277 uV	39.063 uV	1.153
6	7	-5.310 Bits	4 Bits	-51.856 uV	39.063 uV	1.206

Average MEAN = -5.749 Bits, -56.140 uV
 Maximum PEAK to PEAK = 5 Bits, 48.828 uV on Card 6, Channel 0.
 Channel - Channel OFFSET = 4.910 Bits, 47.949 uV
 Minimum Common Mode Rejection = 150.82dB on Card 6, Channel 0.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 3
 Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (1) :

Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the desired system sample rate in hertz. < 1, 200> (50) :
 Enter the slot address of the first gate card. < 0, 511> (6) :
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (8) :
 Enter the desired number of scans. < 1, 32767> (100) :
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (2) : 1

Return the RTP Control Panel to the COMP mode. RETURN to continue ?

Average MEAN = -1.121 Bits, -10.950 uV
 Maximum PEAK to PEAK = 1 Bits, 9.766 uV on Card 6, Channel 0.
 Channel - Channel OFFSET = 1.520 Bits, 14.844 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-1.610 Bits	1 Bits	-15.723 uV	9.766 uV	0.488
6	1	-1.780 Bits	1 Bits	-17.383 uV	9.766 uV	0.414
6	2	-0.960 Bits	1 Bits	-9.375 uV	9.766 uV	0.196
6	3	-1.130 Bits	1 Bits	-11.035 uV	9.766 uV	0.336
6	4	-0.550 Bits	1 Bits	-5.371 uV	9.766 uV	0.497
6	5	-1.690 Bits	1 Bits	-16.504 uV	9.766 uV	0.462
6	6	-0.260 Bits	1 Bits	-2.539 uV	9.766 uV	0.439
6	7	-0.990 Bits	1 Bits	-9.668 uV	9.766 uV	0.099

Average MEAN = -1.121 Bits, -10.950 uV
 Maximum PEAK to PEAK = 1 Bits, 9.766 uV on Card 6, Channel 0.
 Channel - Channel OFFSET = 1.520 Bits, 14.844 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = -0.916 Bits, -8.948 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 6.
 Channel - Channel OFFSET = 1.370 Bits, 13.379 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-1.260 Bits	1 Bits	-12.305 uV	9.766 uV	0.439
6	1	-1.480 Bits	1 Bits	-14.453 uV	9.766 uV	0.500
6	2	-0.820 Bits	1 Bits	-8.008 uV	9.766 uV	0.384
6	3	-1.090 Bits	1 Bits	-10.645 uV	9.766 uV	0.286
6	4	-0.330 Bits	1 Bits	-3.223 uV	9.766 uV	0.470
6	5	-1.290 Bits	1 Bits	-12.598 uV	9.766 uV	0.454
6	6	-0.110 Bits	2 Bits	-1.074 uV	19.531 uV	0.371
6	7	-0.950 Bits	1 Bits	-9.277 uV	9.766 uV	0.218

Average MEAN = -0.916 Bits, -8.948 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 6.
 Channel - Channel OFFSET = 1.370 Bits, 13.379 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 7165.809 Bits, 69.979 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.

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 Att. 3, p. 19

Channel - Channel OFFSET = 1.580 Bits, 15.430 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6 0	7165.850 Bits	1 Bits	69.979 mV	9.766 uV	0.357
6 1	7165.230 Bits	2 Bits	69.973 mV	19.531 uV	0.444
6 2	7166.200 Bits	2 Bits	69.983 mV	19.531 uV	0.424
6 3	7165.100 Bits	1 Bits	69.972 mV	9.766 uV	0.300
6 4	7166.520 Bits	1 Bits	69.986 mV	9.766 uV	0.509
6 5	7164.940 Bits	1 Bits	69.970 mV	9.766 uV	0.237
6 6	7166.480 Bits	1 Bits	69.985 mV	9.766 uV	0.500
6 7	7166.150 Bits	1 Bits	69.982 mV	9.766 uV	0.357

Average MEAN = 7165.809 Bits, 69.979 mV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 1.580 Bits, 15.430 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = -7166.447 Bits, -69.985 mV
 Maximum PEAK to PEAK = 3 Bits, 29.297 uV on Card 6, Channel 2.
 Channel - Channel OFFSET = 3.580 Bits, 25.196 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : Invalid escape sequ

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0

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6 0	-7167.730 Bits	2 Bits	-69.998 mV	19.531 uV	0.691
6 1	-7167.470 Bits	2 Bits	-69.995 mV	19.531 uV	0.640
6 2	-7166.120 Bits	3 Bits	-69.982 mV	29.297 uV	0.431
6 3	-7166.350 Bits	2 Bits	-69.984 mV	19.531 uV	0.517
6 4	-7165.310 Bits	2 Bits	-69.974 mV	19.531 uV	0.484
6 5	-7166.810 Bits	2 Bits	-69.989 mV	19.531 uV	0.560
6 6	-7165.150 Bits	1 Bits	-69.972 mV	9.766 uV	0.357
6 7	-7166.640 Bits	2 Bits	-69.987 mV	19.531 uV	0.520

Average MEAN = -7166.447 Bits, -69.985 mV
 Maximum PEAK to PEAK = 3 Bits, 29.297 uV on Card 6, Channel 2.
 Channel - Channel OFFSET = 3.580 Bits, 25.196 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 1

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6 0	-7167.730 Bits	2 Bits	-69.998 mV	19.531 uV	0.691
6 1	-7167.470 Bits	2 Bits	-69.995 mV	19.531 uV	0.640
6 2	-7166.120 Bits	3 Bits	-69.982 mV	29.297 uV	0.431
6 3	-7166.350 Bits	2 Bits	-69.984 mV	19.531 uV	0.517
6 4	-7165.310 Bits	2 Bits	-69.974 mV	19.531 uV	0.484
6 5	-7166.810 Bits	2 Bits	-69.989 mV	19.531 uV	0.560
6 6	-7165.150 Bits	1 Bits	-69.972 mV	9.766 uV	0.357
6 7	-7166.640 Bits	2 Bits	-69.987 mV	19.531 uV	0.520

Average MEAN = -7166.447 Bits, -69.985 mV
 Maximum PEAK to PEAK = 3 Bits, 29.297 uV on Card 6, Channel 2.
 Channel - Channel OFFSET = 3.580 Bits, 25.196 uV

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Att. 3, p. 2

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < \, 3> (1) : 3
 Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (1) :
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the desired system sample rate in hertz. < 1, 200> (50) :
 Enter the slot address of the first gate card. < 0, 511> (6) :
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (8) : 4
 Enter the desired number of scans. < 1, 32767> (100) :
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = 0.105 Bits, 8.203 μ V
 Maximum PEAK to PEAK = 1 Bits, 78.125 μ V on Card 6, Channel 1.
 Channel - Channel OFFSET = 0.320 Bits, 15.000 μ V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	0.000 Bits	0 Bits	0.000 μ V	0.000 μ V	0.000
6	1	0.030 Bits	1 Bits	2.344 μ V	78.125 μ V	0.171
6	2	0.120 Bits	1 Bits	9.375 μ V	78.125 μ V	0.325
6	3	0.030 Bits	1 Bits	2.344 μ V	78.125 μ V	0.171
6	4	0.260 Bits	1 Bits	20.312 μ V	78.125 μ V	0.439
6	5	0.000 Bits	0 Bits	0.000 μ V	0.000 μ V	0.000
6	6	0.320 Bits	1 Bits	25.000 μ V	78.125 μ V	0.466
6	7	0.080 Bits	1 Bits	6.250 μ V	78.125 μ V	0.271

Average MEAN = 0.105 Bits, 8.203 μ V
 Maximum PEAK to PEAK = 1 Bits, 78.125 μ V on Card 6, Channel 1.
 Channel - Channel OFFSET = 0.320 Bits, 25.000 μ V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 7165.550 Bits, 559.809 mV
 Maximum PEAK to PEAK = 2 Bits, 156.250 μ V on Card 6, Channel 1.
 Channel - Channel OFFSET = 0.930 Bits, 72.670 μ V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	7166.020 Bits	1 Bits	559.845 mV	78.125 μ V	0.140
6	1	7165.620 Bits	2 Bits	559.814 mV	156.250 μ V	0.525
6	2	7165.980 Bits	2 Bits	559.842 mV	156.250 μ V	0.244
6	3	7165.120 Bits	1 Bits	559.775 mV	78.125 μ V	0.325
6	4	7165.310 Bits	1 Bits	559.790 mV	78.125 μ V	0.462
6	5	7165.090 Bits	1 Bits	559.773 mV	78.125 μ V	0.386
6	6	7165.250 Bits	1 Bits	559.785 mV	78.125 μ V	0.433
6	7	7166.010 Bits	2 Bits	559.844 mV	156.250 μ V	0.264

Average MEAN = 7165.550 Bits, 559.809 mV
 Maximum PEAK to PEAK = 2 Bits, 156.250 μ V on Card 6, Channel 1.
 Channel - Channel OFFSET = 0.930 Bits, 72.670 μ V

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = -7164.586 Bits, -559.733 mV

II-1
 Att. 3, p. 2

Maximum PEAK to PEAK = 2 Bits, 156.250 uV on Card 6, Channel 1.
Channel - Channel OFFSET = 0.990 Bits, 77.324 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-7165.110 Bits	1 Bits	-559.774 mV	78.125 uV	0.313
6	1	-7165.010 Bits	2 Bits	-559.766 mV	156.250 uV	0.264
6	2	-7164.880 Bits	2 Bits	-559.756 mV	156.250 uV	0.407
6	3	-7164.120 Bits	1 Bits	-559.697 mV	78.125 uV	0.325
6	4	-7164.220 Bits	1 Bits	-559.705 mV	78.125 uV	0.414
6	5	-7164.180 Bits	1 Bits	-559.702 mV	78.125 uV	0.384
6	6	-7164.140 Bits	1 Bits	-559.698 mV	78.125 uV	0.347
6	7	-7165.030 Bits	2 Bits	-559.768 mV	156.250 uV	0.222

Average MEAN = -7164.586 Bits, -559.733 mV
Maximum PEAK to PEAK = 2 Bits, 156.250 uV on Card 6, Channel 1.
Channel - Channel OFFSET = 0.990 Bits, 77.324 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 3
Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
Enter the slot address of the A/D card. < 0, 15> (1) :
Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
Enter the desired system sample rate in hertz. < 1, 200> (50) :
Enter the slot address of the first gate card. < 0, 511> (6) :
Enter the number of channels per card. < 4, 8> (8) :
Enter the number of cards to be scanned. < 1, 15> (1) :
Enter the gain code for the desired system gain. < 0, 1> (4) : 0
Enter the desired number of scans. < 1, 32767> (10) :
Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = 0.053 Bits, 65.625 uV
Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 6, Channel 0.
Channel - Channel OFFSET = 0.060 Bits, 75.000 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	0.050 Bits	1 Bits	62.500 uV	1.250 mV	0.218
6	1	0.070 Bits	1 Bits	87.500 uV	1.250 mV	0.255
6	2	0.060 Bits	1 Bits	75.000 uV	1.250 mV	0.237
6	3	0.080 Bits	1 Bits	100.000 uV	1.250 mV	0.271
6	4	0.020 Bits	1 Bits	25.000 uV	1.250 mV	0.140
6	5	0.040 Bits	1 Bits	50.000 uV	1.250 mV	0.196
6	6	0.040 Bits	1 Bits	50.000 uV	1.250 mV	0.196
6	7	0.060 Bits	1 Bits	75.000 uV	1.250 mV	0.237

Average MEAN = 0.053 Bits, 65.625 uV
Maximum PEAK to PEAK = 1 Bits, 1.250 mV on Card 6, Channel 0.
Channel - Channel OFFSET = 0.060 Bits, 75.000 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 7168.886 Bits, 8.961 uV
Maximum PEAK to PEAK = 2 Bits, 2.500 mV on Card 6, Channel 0.
Channel - Channel OFFSET = 1.300 Bits, 1.625 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

II-1
Att. 3, p. 2

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6 0	7169.330 Bits	2 Bits	8.962 V	2.500 mV	0.491
6 1	7169.180 Bits	1 Bits	8.961 V	1.250 mV	0.384
6 2	7168.130 Bits	1 Bits	8.960 V	1.250 mV	0.336
6 3	7169.130 Bits	1 Bits	8.961 V	1.250 mV	0.336
6 4	7169.170 Bits	1 Bits	8.961 V	1.250 mV	0.376
6 5	7168.030 Bits	1 Bits	8.960 V	1.250 mV	0.171
6 6	7169.030 Bits	1 Bits	8.961 V	1.250 mV	0.171
6 7	7169.080 Bits	1 Bits	8.961 V	1.250 mV	0.271

Average MEAN = 7168.886 Bits, 8.961 V
 Maximum PEAK to PEAK = 2 Bits, 2.500 mV on Card 6, Channel 0.
 Channel - Channel OFFSET = 1.300 Bits, 1.625 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = -7168.328 Bits, -8.960 V
 Maximum PEAK to PEAK = 2 Bits, 2.500 mV on Card 6, Channel 3.
 Channel - Channel OFFSET = 1.790 Bits, 2.238 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6 0	-7169.000 Bits	0 Bits	-8.961 V	0.000 uV	0.000
6 1	-7169.000 Bits	0 Bits	-8.961 V	0.000 uV	0.000
6 2	-7168.870 Bits	1 Bits	-8.961 V	1.250 mV	0.336
6 3	-7167.210 Bits	2 Bits	-8.959 V	2.500 mV	0.475
6 4	-7167.360 Bits	2 Bits	-8.959 V	2.500 mV	0.575
6 5	-7168.440 Bits	1 Bits	-8.961 V	1.250 mV	0.496
6 6	-7167.740 Bits	2 Bits	-8.960 V	2.500 mV	0.559
6 7	-7169.000 Bits	0 Bits	-8.961 V	0.000 uV	0.000

Average MEAN = -7168.328 Bits, -8.960 V
 Maximum PEAK to PEAK = 2 Bits, 2.500 mV on Card 6, Channel 3.
 Channel - Channel OFFSET = 1.790 Bits, 2.238 mV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) :

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) : *Section 2c*
 Enter the slot address of the A/D card. < 0, 15> (1) : *II-1F1*
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) : *SMT16*
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) : *Common Mode*
 Enter the desired system sample rate in hertz. < 1, 200> (50) :
 Enter the slot address of the first gate card. < 0, 511> (6) :
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (8) :
 Enter the desired number of scans. < 1, 32767> (100) :
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) : 2
 Enter the applied common mode voltage (P-P). < 1, 1700> (1) : 1697

Average MEAN = -0.076 Bits, -0.745 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 4.730 Bits, 46.192 uV
 Minimum Common Mode Rejection = 158.78dB on Card 6, Channel 1.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (3) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-0.990 Bits	1 Bits	-9.668 uV	9.766 uV	0.099
6	1	-3.000 Bits	2 Bits	-29.297 uV	19.531 uV	0.245
6	2	0.460 Bits	2 Bits	4.492 uV	19.531 uV	0.537
6	3	-0.470 Bits	1 Bits	-4.590 uV	9.766 uV	0.499
6	4	1.730 Bits	1 Bits	16.895 uV	9.766 uV	0.444
6	5	-0.650 Bits	1 Bits	-6.348 uV	9.766 uV	0.477
6	6	1.400 Bits	1 Bits	13.672 uV	9.766 uV	0.490
6	7	0.910 Bits	1 Bits	8.887 uV	9.766 uV	0.286

Average MEAN = -0.076 Bits, -0.745 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 4.730 Bits, 46.192 uV
 Minimum Common Mode Rejection = 158.78dB on Card 6, Channel 1.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 0.040 Bits, 0.391 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 4.070 Bits, 39.746 uV
 Minimum Common Mode Rejection = 158.78dB on Card 6, Channel 1.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-0.910 Bits	1 Bits	-8.887 uV	9.766 uV	0.286
6	1	-2.450 Bits	2 Bits	-23.926 uV	19.531 uV	0.536
6	2	0.630 Bits	2 Bits	6.152 uV	19.531 uV	0.533
6	3	-0.350 Bits	1 Bits	-3.418 uV	9.766 uV	0.477
6	4	1.620 Bits	1 Bits	15.820 uV	9.766 uV	0.485
6	5	-0.490 Bits	1 Bits	-4.785 uV	9.766 uV	0.500
6	6	1.390 Bits	1 Bits	13.574 uV	9.766 uV	0.488
6	7	0.820 Bits	1 Bits	8.594 uV	9.766 uV	0.325

Average MEAN = 0.040 Bits, 0.391 uV
 Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 1.
 Channel - Channel OFFSET = 4.070 Bits, 39.746 uV
 Minimum Common Mode Rejection = 158.78dB on Card 6, Channel 1.

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Att. 3, p. 24

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 0.076 Bits, 0.745 uV
Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 6.
Channel - Channel OFFSET = 3.610 Bits, 35.254 uV
Minimum Common Mode Rejection = 158.78dB on Card 6, Channel 6.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	-0.770 Bits	1 Bits	-7.520 uV	9.766 uV	0.421
6	1	-2.170 Bits	1 Bits	-21.191 uV	9.766 uV	0.376
6	2	0.620 Bits	1 Bits	6.055 uV	9.766 uV	0.485
6	3	-0.310 Bits	1 Bits	-3.027 uV	9.766 uV	0.462
6	4	1.440 Bits	1 Bits	14.063 uV	9.766 uV	0.496
6	5	-0.280 Bits	1 Bits	-2.734 uV	9.766 uV	0.449
6	6	1.250 Bits	2 Bits	12.207 uV	19.531 uV	0.456
6	7	0.830 Bits	1 Bits	8.105 uV	9.766 uV	0.376

Average MEAN = 0.076 Bits, 0.745 uV
Maximum PEAK to PEAK = 2 Bits, 19.531 uV on Card 6, Channel 6.
Channel - Channel OFFSET = 3.610 Bits, 35.254 uV
Minimum Common Mode Rejection = 158.78dB on Card 6, Channel 6.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 2

Average MEAN = 0.104 Bits, 1.013 uV
Maximum PEAK to PEAK = 5 Bits, 48.828 uV on Card 6, Channel 6.
Channel - Channel OFFSET = 3.600 Bits, 35.156 uV
Minimum Common Mode Rejection = 150.82dB on Card 6, Channel 6.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD	CHANNEL	MEAN	P-P	MEAN	P-P	STD. DEV.
6	0	0.000 Bits	4 Bits	0.000 uV	39.063 uV	1.158
6	1	-2.100 Bits	3 Bits	-20.508 uV	29.297 uV	1.054
6	2	0.580 Bits	4 Bits	5.664 uV	39.063 uV	1.201
6	3	-0.130 Bits	4 Bits	-1.270 uV	39.063 uV	1.074
6	4	1.140 Bits	4 Bits	11.133 uV	39.063 uV	1.200
6	5	-0.480 Bits	3 Bits	-4.688 uV	29.297 uV	0.995
6	6	1.500 Bits	5 Bits	14.648 uV	48.828 uV	1.187
6	7	0.320 Bits	3 Bits	3.125 uV	29.297 uV	1.232

Average MEAN = 0.104 Bits, 1.013 uV
Maximum PEAK to PEAK = 5 Bits, 48.828 uV on Card 6, Channel 6.
Channel - Channel OFFSET = 3.600 Bits, 35.156 uV
Minimum Common Mode Rejection = 150.82dB on Card 6, Channel 6.

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) :

Section 2

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) : U.A.I.C.S. TE 84

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (0) : 1
 Enter the Bit Resolution of the A/D card. < 12, 14> (12) : 14
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) : 0
 Enter the desired system sample rate in hertz. < 1, 200> (100) : 50
 Enter the slot address of the first gate card. < 0, 511> (0) : 6
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (0) : 11
 Enter the desired number of scans. < 1, 32767> (1) : 100
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Reading #1

II-1F1
SLOT 6

Average MEAN = -1.678 Bits, -2.048 uV
 Maximum PEAK to PEAK = 10 Bits, 12.207 uV on Card 6, Channel 2.
 Channel - Channel OFFSET = 4.900 Bits, 5.981 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 1

CARD	CHANNEL	MEAN	P-P	MEAN #1	P-P	STD. DEV.
6	0	-3.540 Bits	8 Bits	-4.321 uV	9.766 uV	1.545
6	1	-2.310 Bits	8 Bits	-2.820 uV	9.766 uV	1.598
6	2	-1.230 Bits	10 Bits	-1.501 uV	12.207 uV	1.624
6	3	-2.260 Bits	6 Bits	-2.759 uV	7.324 uV	1.301
6	4	-0.820 Bits	8 Bits	-1.001 uV	9.766 uV	1.465
6	5	1.020 Bits	9 Bits	1.245 uV	10.986 uV	1.643
6	6	-0.400 Bits	6 Bits	-0.488 uV	7.324 uV	1.334
6	7	-3.880 Bits	8 Bits	-4.736 uV	9.766 uV	1.423

Average MEAN = -1.678 Bits, -2.048 uV
 Maximum PEAK to PEAK = 10 Bits, 12.207 uV on Card 6, Channel 2.
 Channel - Channel OFFSET = 4.900 Bits, 5.981 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) :

DALCAL Card TEST PROGRAM for B. G. E. ACCEPTANCE - Version 10-JAN-84

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (0) : 1
 Enter the Bit Resolution of the A/D card. < 12, 14> (12) : 14
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the slot address of the first card. < 0, 15> (0) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR
 Select SCAN TYPE. < 0, 3> (0) : 3
 Enter the desired number of scans. < 1, 32767> (100) :

CARD	CHANNEL	MEAN	P-P	FUNCTION	NOMINAL
0	0	1.006 V	625.000 uV	+15 volts	+1 volt
0	1	-1.009 V	625.000 uV	-15 volts	-1 volt
0	2	996.794 mV	1.250 mV	+5 volts	+1 volt
0	3	418.444 mV	625.000 uV	+12 volts	+1 volt

II-1
Att. 3, p. 26

0	4	-637.500 uV	625.000 uV	48/125 volts	+1 volt
0	5	-637.500 uV	625.000 uV	48/125 volts	+1 volt
0	6	24.414 C	0.125 C	TEMP A	#)
0	7	-273.212 C	0.000 C	TEMP B	

Select (1) = RETEST, (2) = NEWTEST. < 0, 2 > (1) :

II-1
Att. 3 p. 2

Section 23
 Reading #2
 II-1F1
 56T16

U.A.I.C.S. TEST PROGRAM for B. G. E. ACCEPTANCE - Version 12-JAN-84

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (0) : 1
 Enter the Bit Resolution of the A/D card. < 12, 14> (12) : 14
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the desired system sample rate in hertz. < 1, 200> (100) : 50
 Enter the slot address of the first gate card. < 0, 511> (0) : 6
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (0) : 11
 Enter the desired number of scans. < 1, 32767> (1) : 100
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = -2.340 Bits, -2.856 uV
 Maximum PEAK to PEAK = 9 Bits, 10.986 uV on Card 6, Channel 0.
 Channel - Channel OFFSET = 6.740 Bits, 8.228 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1 : 1

CARD	CHANNEL	MEAN	P-P	MEAN #2	P-P	STD. DEV.
6	0	-4.600 Bits	9 Bits	-5.615 uV	10.986 uV	1.503
6	1	-2.460 Bits	9 Bits	-3.003 uV	10.986 uV	1.565
6	2	-2.080 Bits	8 Bits	-2.539 uV	9.766 uV	1.707
6	3	-2.740 Bits	8 Bits	-3.345 uV	9.766 uV	1.671
6	4	-1.580 Bits	8 Bits	-1.929 uV	9.766 uV	1.680
6	5	1.440 Bits	9 Bits	1.758 uV	10.986 uV	1.657
6	6	-1.400 Bits	7 Bits	-1.709 uV	8.545 uV	1.685
6	7	-5.300 Bits	7 Bits	-6.470 uV	8.545 uV	1.338

Average MEAN = -2.340 Bits, -2.856 uV
 Maximum PEAK to PEAK = 9 Bits, 10.986 uV on Card 6, Channel 0.
 Channel - Channel OFFSET = 6.740 Bits, 8.228 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) :

DALCAL Card TEST PROGRAM for B. G. E. ACCEPTANCE - Version 10-JAN-84

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (0) : 1
 Enter the Bit Resolution of the A/D card. < 12, 14> (12) : 14
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the slot address of the first card. < 0, 15> (0) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR
 Select SCAN TYPE. < 0, 3> (0) : 3
 Enter the desired number of scans. < 1, 32767> (100) :

CARD	CHANNEL	MEAN	P-P	FUNCTION	NOMINAL
0	0	1.006 V	625.000 uV	+15 volts	+1 volt
0	1	-1.009 V	625.000 uV	-15 volts	-1 volt
0	2	996.862 mV	1.250 mV	+5 volts	+1 volt
0	3	418.687 mV	625.000 uV	+12 volts	+1 volt
0	4	-1.231 mV	625.000 uV	48/125 volts	+1 volt
0	5	-1.231 mV	625.000 uV	48/125 volts	+1 volt
0	6	27.981 C	0.125 C	TEMP A #2	
0	7	-273.254 C	0.063 C	TEMP B	

II-1
 Att. 3, p. 28

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) : Section 23
 Enter the slot address of the A/D card. < 0, 15> (1) : Reading #3
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type. (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) : II-1F1
 Enter the desired system sample rate in hertz. < 1, 200> (50) :
 Enter the slot address of the first gate card. < 0, 511> (4) : 6 Slot 16
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (11) :
 Enter the desired number of scans. < 1, 32767> (100) :
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = -2.716 Bits, -3.316 uV
 Maximum PEAK to PEAK = 10 Bits, 12.207 uV on Card 6, Channel 5.
 Channel - Channel OFFSET = 6.540 Bits, 7.983 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (2) : 1

CARD CHANNEL	MEAN	P-P	MEAN #3	P-P	STD. DEV.
6 0	-4.980 Bits	8 Bits	-6.079 uV	9.766 uV	1.649
6 1	-2.990 Bits	8 Bits	-3.113 uV	9.766 uV	1.621
6 2	-2.210 Bits	8 Bits	-2.698 uV	9.766 uV	1.796
6 3	-3.510 Bits	9 Bits	-4.285 uV	10.986 uV	1.775
6 4	-2.100 Bits	7 Bits	-2.563 uV	8.545 uV	1.658
6 5	0.900 Bits	10 Bits	1.099 uV	12.207 uV	1.900
6 6	-1.640 Bits	7 Bits	-2.007 uV	8.545 uV	1.786
6 7	-5.640 Bits	8 Bits	-6.885 uV	9.766 uV	1.507

Average MEAN = -2.716 Bits, -3.316 uV
 Maximum PEAK to PEAK = 10 Bits, 12.207 uV on Card 6, Channel 5.
 Channel - Channel OFFSET = 6.540 Bits, 7.983 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) :
 DALCAL Card TEST PROGRAM for B. G. E. ACCEPTANCE - Version 10-JAN-84

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (0) : 1
 Enter the Bit Resolution of the A/D card. < 12, 14> (12) : 14
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the slot address of the first card. < 0, 15> (0) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR
 Select SCAN TYPE. < 0, 3> (0) : 3
 Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P	FUNCTION	NOMINAL
0 0	1.006 V	1.250 mV	+15 volts	+1 volt
0 1	-1.009 V	625.000 uV	-15 volts	-1 volt
0 2	996.444 mV	625.000 uV	+5 volts	+1 volt
0 3	418.381 mV	625.000 uV	+12 volts	+1 volt
0 4	-1.250 mV	0.000 uV	48/125 volts	+1 volt
0 5	-1.225 mV	625.000 uV	48/125 volts	+1 volt
0 6	27.277 C	0.125 C	TEMP A #3	
0 7	-273.256 C	0.063 C	TEMP B	

II-1
 Att. 3, p.29

6	3	-2.690 Bits	8 Bits	-3.284 uV	9.766 uV	1.566
6	4	-1.470 Bits	7 Bits	-1.794 uV	8.545 uV	1.539
6	5	1.550 Bits	9 Bits	1.892 uV	10.986 uV	1.774
6	6	-1.190 Bits	9 Bits	-1.453 uV	10.986 uV	1.604
6	7	-5.160 Bits	8 Bits	-6.299 uV	9.766 uV	1.515

Average MEAN = -2.216 Bits, -2.705 uV #4
 Maximum PEAK to PEAK = 10 Bits, 12.207 uV on Card 6, Channel 0.
 Channel - Channel OFFSET = 6.710 Bits, 1.191 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) :

2
 Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (1) :
 Enter the Bit Resolution of the A/D card. < 12, 14> (14) :
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the slot address of the first card. < 0, 15> (0) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 SCAN Types - (0) = OFFSET
 (1) = PLUS POLARITY
 (2) = MINUS POLARITY
 (3) = SYSTEM MONITOR

Section 23
 II-1F1
 Slot 16
 Reading #5

Select SCAN TYPE. < 0, 3> (0) : 3
 Enter the desired number of scans. < 1, 32767> (100) :

CARD CHANNEL	MEAN	P-P	FUNCTION	NOMINAL	
0	0	1.006 V	625.000 uV	+15 volts	+1 volt
0	1	-1.009 V	625.000 uV	-15 volts	-1 volt
0	2	996.500 mV	625.000 uV	+5 volts	+1 volt
0	3	418.406 mV	625.000 uV	+12 volts	+1 volt
0	4	-1.231 mV	625.000 uV	48/125 volts	+1 volt
0	5	-1.225 mV	625.000 uV	48/125 volts	+1 volt
0	6	27.592 C	0.063 C	TEMP A	#5
0	7	-273.256 C	0.063 C	TEMP B	

Select (1) = RETEST, (2) = NEWTEST. < 0, 2> (2) :
 U.A.I.C.S. TEST PROGRAM for B. G. E. ACCEPTANCE - Version 12-JAN-84

Enter the 1st DEVICE CODE of the I/O Controller. < 48, 63> (48) :
 Enter the slot address of the A/D card. < 0, 15> (0) : 1
 Enter the Bit Resolution of the A/D card. < 12, 14> (12) : 14
 Select the A/D type, (0)=BIPOLAR, (1)=UNIPOLAR. < 0, 1> (0) :
 Enter the desired system sample rate in hertz. < 1, 200> (100) : 50
 Enter the slot address of the first gate card. < 0, 511> (0) : 6
 Enter the number of channels per card. < 4, 8> (8) :
 Enter the number of cards to be scanned. < 1, 15> (1) :
 Enter the gain code for the desired system gain. < 0, 11> (0) : 11
 Enter the desired number of scans. < 1, 32767> (1) : 100
 Select (1)=NORMAL SCAN, (2)=COMMON MODE SCAN. < 1, 2> (1) :

Average MEAN = -2.161 Bits, -2.638 uV
 Maximum PEAK to PEAK = 11 Bits, 13.428 uV on Card 6, Channel 4.
 Channel - Channel OFFSET = 6.740 Bits, 8.228 uV

Enter (1)=PRINTOUT, (2)=RESCAN, (3)=RESTART. < 0, 3> (1) : 1

CARD CHANNEL	MEAN	P-P	MEAN #5	P-P	STD. DEV.	
6	0	-4.660 Bits	10 Bits	-5.688 uV	12.207 uV	1.485
6	1	-2.370 Bits	8 Bits	-2.893 uV	9.766 uV	1.695
6	2	-1.810 Bits	9 Bits	-2.209 uV	10.986 uV	1.953
6	3	-2.580 Bits	8 Bits	-3.149 uV	9.766 uV	1.686
6	4	-1.410 Bits	11 Bits	-1.721 uV	13.428 uV	1.778
6	5	1.770 Bits	9 Bits	2.161 uV	10.986 uV	1.886
6	6	-1.260 Bits	8 Bits	-1.538 uV	9.766 uV	1.759
6	7	-4.970 Bits	9 Bits	-6.067 uV	10.986 uV	1.634

Average MEAN = -2.161 Bits, -2.638 uV
 Maximum PEAK to PEAK = 11 Bits, 13.428 uV on Card 6, Channel 4.
 Channel - Channel OFFSET = 6.740 Bits, 8.228 uV

II-1
 Att. 3, p. 3

DRAWING CHANGE NOTICE

DCN NO. 60277-2A

SH. 2 OF 3

BALTIMORE GAS & ELECTRIC COMPANY
NUCLEAR ENGINEERING SERVICES DEPARTMENT

KWJ	JB	KWJ	JB	RMS	THP	7/10/87
DWN	CHK	DSGN	CHK	DE	APP'D	DATE

CALVERT CLIFFS UNIT - 1#2

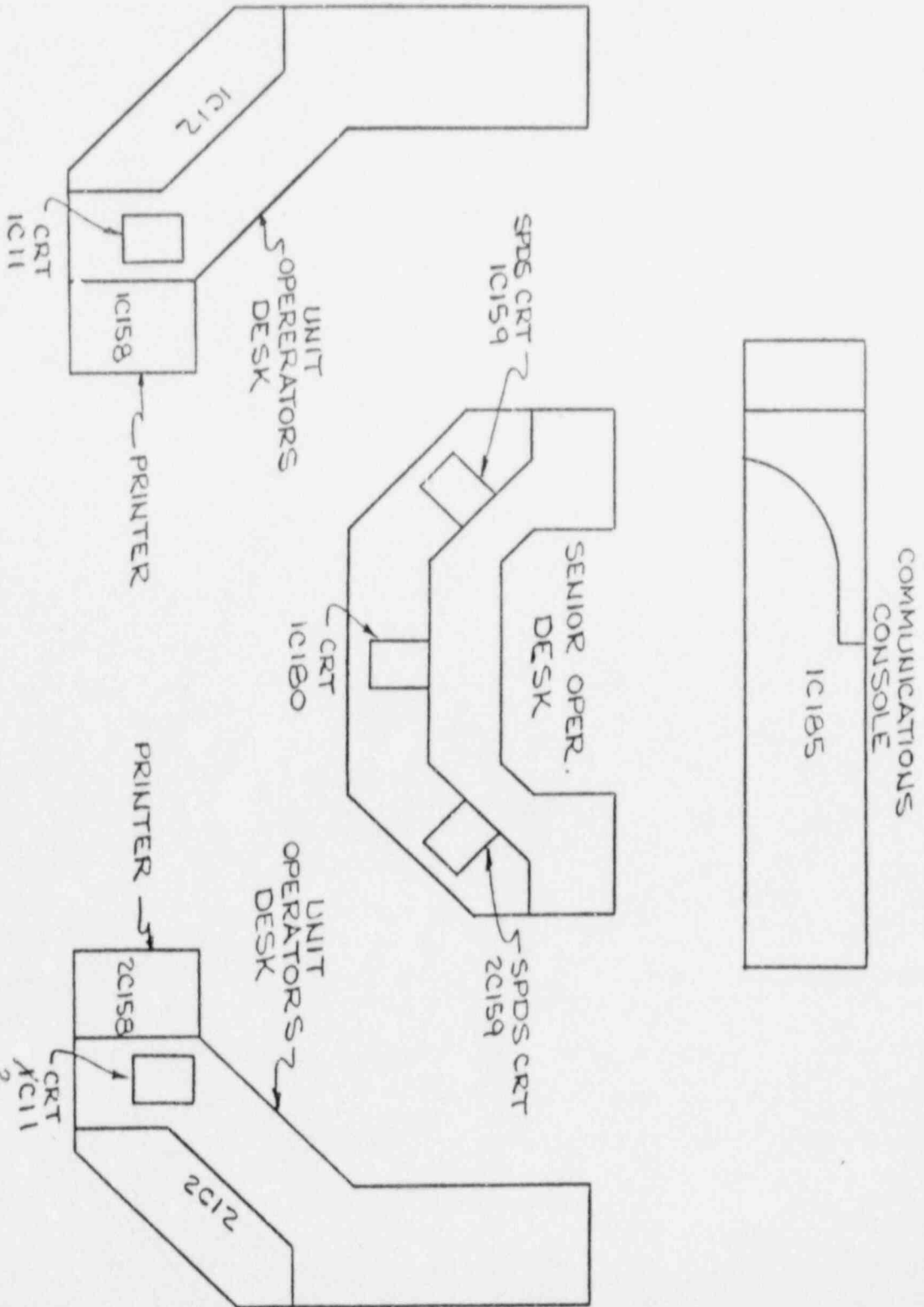
IN ACCORDANCE WITH FCR NO. 83-1029

REASON FOR CHANGE

INSTLN OF PLANT COMPUTER

USE WITH
DWG. NO. 60-277-E
BECHTEL NO. M-100

REV. 17



AFTER

ATTACHMENT # 4

PLANT OPERATING SUMMARY

C.C.N.P.P. UNIT 2

PAGE 2 OF 2 PAGES
REG

REACTIVITY

RCS PRESS & INVENTORY

CORE/RCS HEAT REMOVAL

CONTAINMENT ENVIRONMENT

CONTAINMENT ISOLATION

RADIATION CONTROL

VITAL AUX

INDICATIONS

- 1 LINEAR POWER
- 2 PRESSURIZER PRESSURE
- 3 PRESSURIZER LEVEL
- 4 NET MHE
- 5 LOOP 21 TCOLD
- 6 LOOP 22 TCOLD
- 7 LOOP 21 THOT
- 8 LOOP 22 THOT
- 9 21 50 PRESSURE
- 0 22 50 PRESSURE
- 1 21 50 LEVEL
- 2 22 50 LEVEL

REG

REG

REACTIVITY

C.C.N.P.P. UNIT 2

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REG

REACTIVITY

RCS PRESS & INVENTORY

CORE/RCS HEAT REMOVAL

CONTAINMENT ENVIRONMENT

CONTAINMENT ISOLATION

RADIATION CONTROL

VITAL AUX

LINEAR FWR

SUR

TCOLD

BORON CONC

BAST LEVEL

CHG PUMP FLOW

HRSI FLOW

200
100
0

7

24 22

2000

180
150

150
100
50
0

1500

10
0

4

900

1000

100

750

375

10
0

0

547

400

128

98

0

100 1.08E+04 DPM

F/H 547 547

400 IN 128

98

0

IDENT

STATUS

CHG PR SOURCE

CVOT 1

CV 818

COBENT

CV 818

COBENT

ALARM/INDICATION

PAG FWD

PAG BCK

PAG BCK

REACTIVITY

C.C.N.P.P. UNIT 2

PAGE 2 OF 3 PAGES
REG

REACTIVITY

RCS
PRESS &
INVENTORY

CORE/RCS
HEAT
REMOVAL

CONTAINMENT
ENVIRONMENT

CONTAINMENT
ISOLATION

RADIATION
CONTROL

VITAL
AUX



REACTIVITY

C.C.N.P.P. UNIT 2

REACTIVITY

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ENVIRONMENT

CONTAINMENT
ISOLATION

RADIATION
CONTROL

VITAL
AUX

RED ALARMS

- * 1 TWO OR MORE RODS STUCK
- * 2 POWER HIGH AFTER TRIP
- * 3 ATWS
- * 4 TWO OR MORE DROPPED RODS

INDICATIONS

- 8 LINEAR POWER
- 9 LOG POWER
- 10 START UP RATE
- 11 LOOP 21 TCOLD
- 12 LOOP 22 TCOLD
- 13 BORON CONC
- 14 21 BAST LEVEL
- 15 22 BAST LEVEL
- 16 CHG PUMP FLOW
- 17 HPSI FLOW
- 18 CHARGING SOURCE
- 19 CEH MIMIC
- 20 STATUS BLOCK

YELLOW ALARMS

- * 5 ONE DROPPED ROD
- * 6 ONE STUCK ROD
- * 7 REACTIVITY ADDITION

* VALIDATION CRITERIA NOT APPLIED

: PAGE END

: PAGE BACK

S.C.N.P.P. UNIT 2

RCS PRESS & INVENTORY

REACTIVITY

RADIATION CONTROL

RCS PRESS & INVENTORY

CONTAINMENT ENVIRONMENT

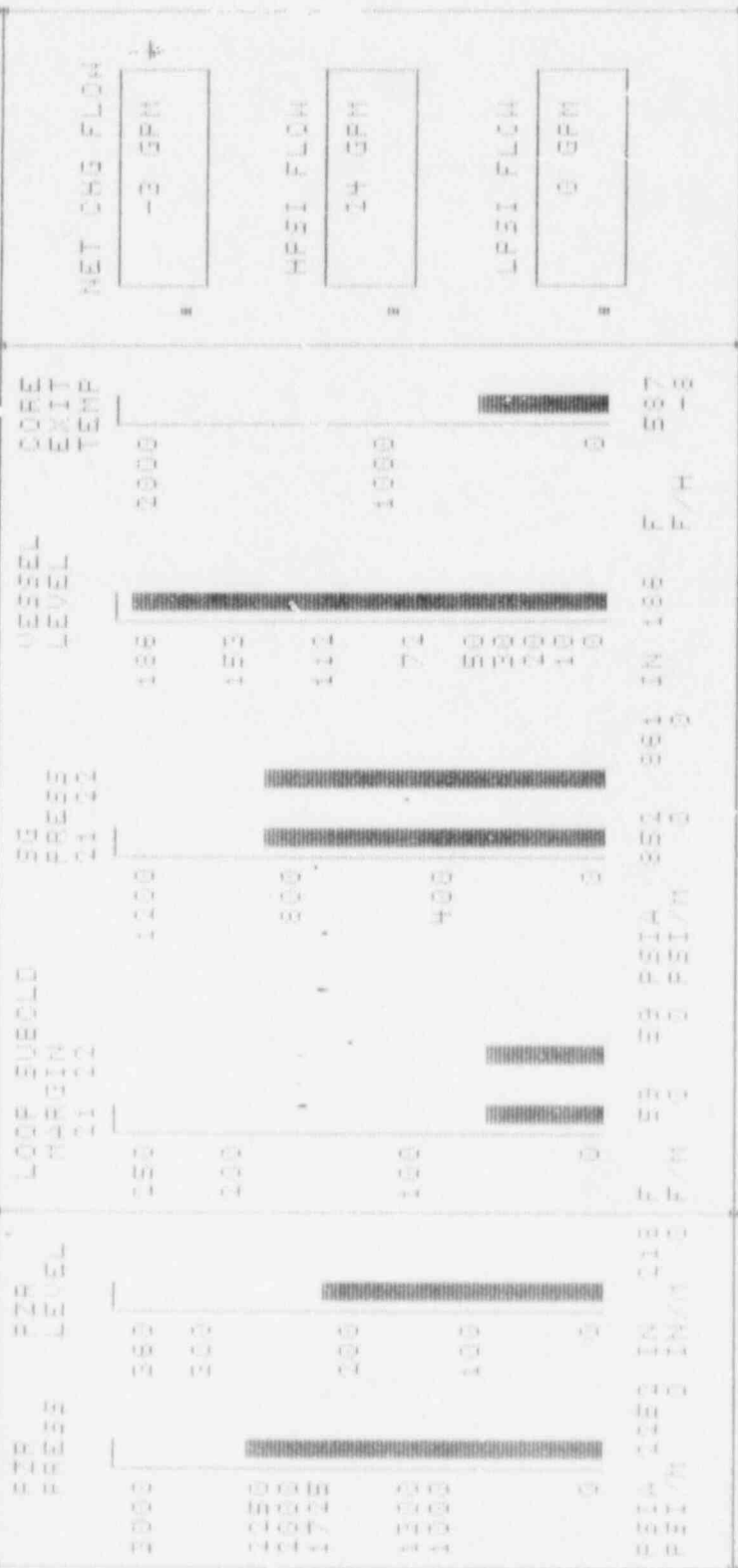
CONTAINMENT ISOLATION

REACTIVITY

RADIATION CONTROL

CONTAINMENT ENVIRONMENT

CONTAINMENT ISOLATION



EVENT	STATUS	IDENT	STATUS	IDENT	STATUS	ALARM/INDICATION	PAGE END
RCS PRESS & INVENTORY	OK	RCS PRESS & INVENTORY	OK	RCS PRESS & INVENTORY	OK	ALARM/INDICATION	PAGE END
REACTIVITY	OK	REACTIVITY	OK	REACTIVITY	OK		
RADIATION CONTROL	OK	RADIATION CONTROL	OK	RADIATION CONTROL	OK		
CONTAINMENT ENVIRONMENT	OK	CONTAINMENT ENVIRONMENT	OK	CONTAINMENT ENVIRONMENT	OK		
CONTAINMENT ISOLATION	OK	CONTAINMENT ISOLATION	OK	CONTAINMENT ISOLATION	OK		

REACTIVITY

RCS PRESS & INVENTORY

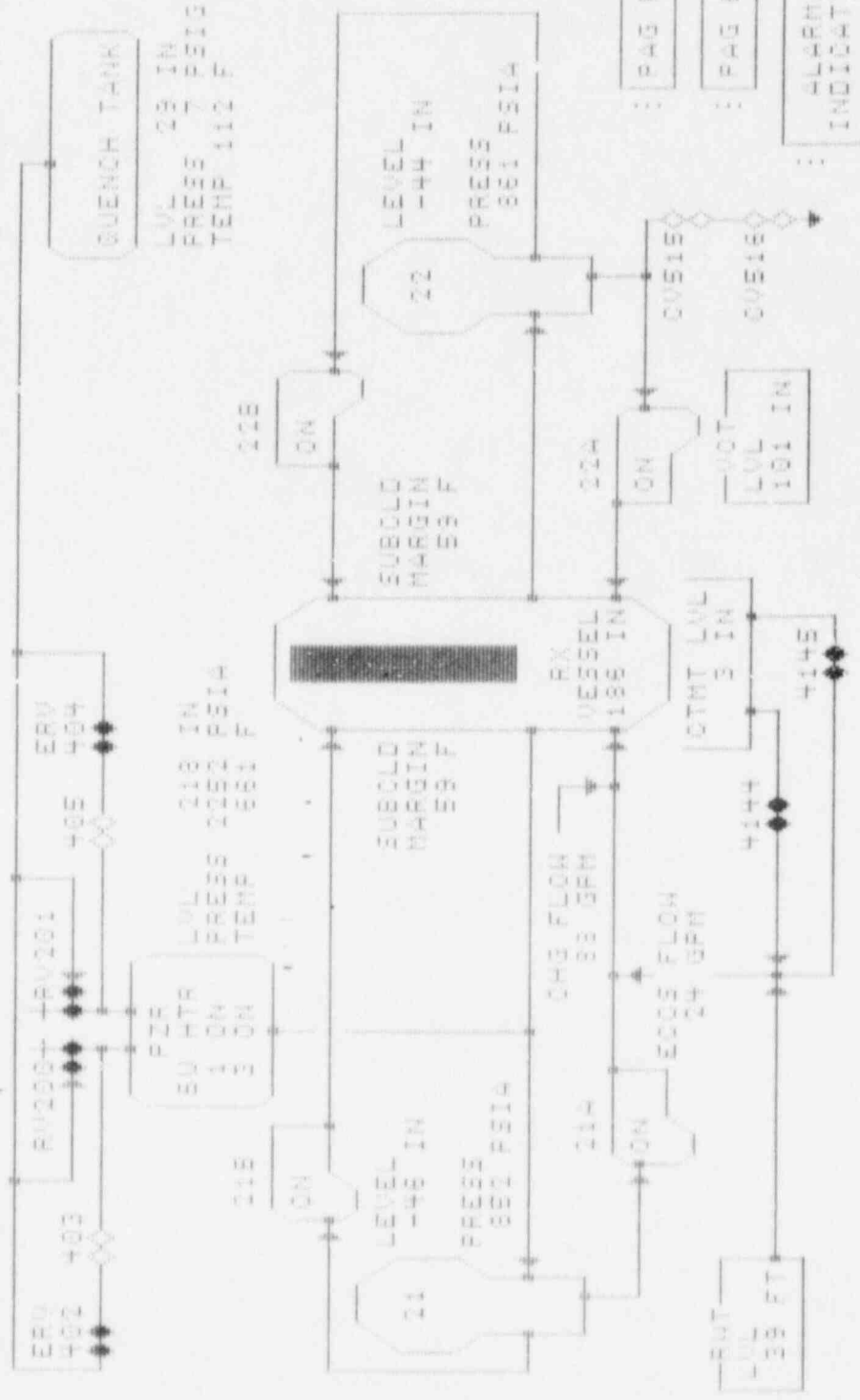
CORE/RCS HEAT REMOVAL

CONTAINMENT ENVIRONMENT

CONTAINMENT ISOLATION

RADIATION CONTROL

VITAL AUX



RCS PRESSURE & INVENTORY

C.C.M.P.P. UNIT 2

REACTIVITY

RCS PRESS & INVENTORY

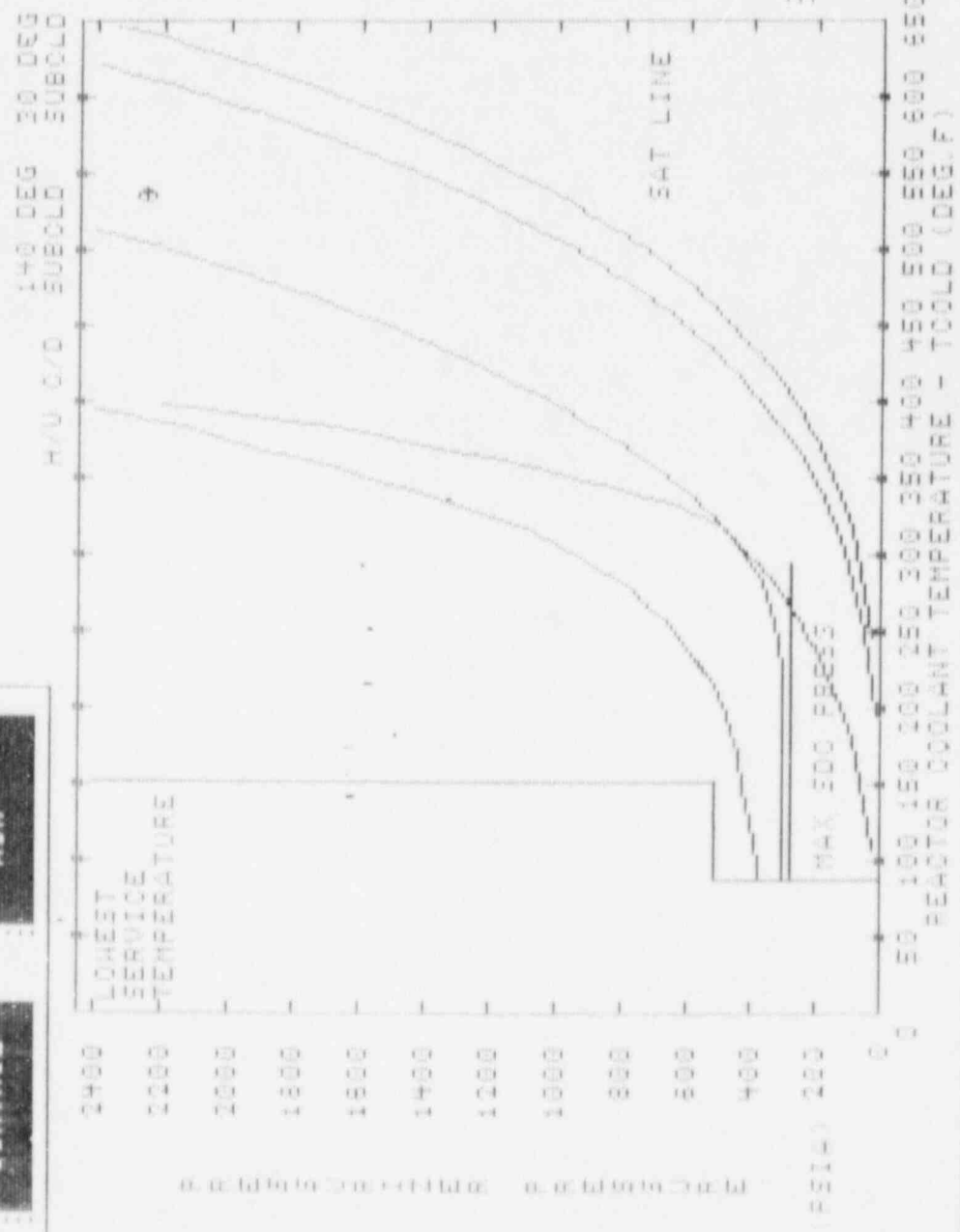
CORE/RCS HEAT REMOVAL

CONTAINMENT ENVIRONMENT

CONTAINMENT ISOLATION

RADIATION CONTROL

VITAL AUX



<p>RCS PRESSURE & INVENTORY</p> <p>REACTIVITY</p> <p>RADIATION CONTROL</p>	<p>RCS PRESS & INVENTORY</p> <p>VITAL AUX</p>	<p>C.C.N.P.P. UNIT 2</p> <p>CORE/RCS HEAT REMOVAL</p> <p>CONTAINMENT ENVIRONMENT</p>	<p>PAGE 4 OF 4 PAGES</p> <p>REG</p> <p>CONTAINMENT ISOLATION</p>
<p>RED ALARMS</p> <ul style="list-style-type: none"> * 1 SUBCOOLED MARGIN HIGH * 2 EOS FAILURE * 3 RAS FAILURE * 4 REACTOR VESSEL LEVEL LOW * 5 RCS PRESSURE HIGH <p>YELLOW ALARMS</p> <ul style="list-style-type: none"> * 6 RELIEF VALVE OPEN * 7 PRESSURIZER LEVEL ABNORMAL 	<p>INDICATIONS</p> <ul style="list-style-type: none"> 9 PRESSURIZER PRESSURE 9 PRESSURIZER LEVEL 10 LOOP 21 SUBCOOLED MARGIN 10 LOOP 22 SUBCOOLED MARGIN 11 21 99 PRESSURE 11 22 99 PRESSURE 12 REACTOR VESSEL LEVEL 13 CORE EXIT TEMP 14 NET CHG FLOW 15 HEAT FLOW 16 STATUS BLOCK 17 PRIMARY MIMIC 18 PRESS/TEMP PLOT 	<p>VALIDATION CRITERIA NOT APPLIED</p>	<p>REG END</p> <p>REG BCK</p>

000001

CORE / RCS HEAT REMOVAL

C.C.N.P.P. UNIT 2

REACTIVITY

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CORE/RCS HEAT REMOVAL

CONTAINMENT ENVIRONMENT

CONTAINMENT ISOLATION

RADIATION CONTROL

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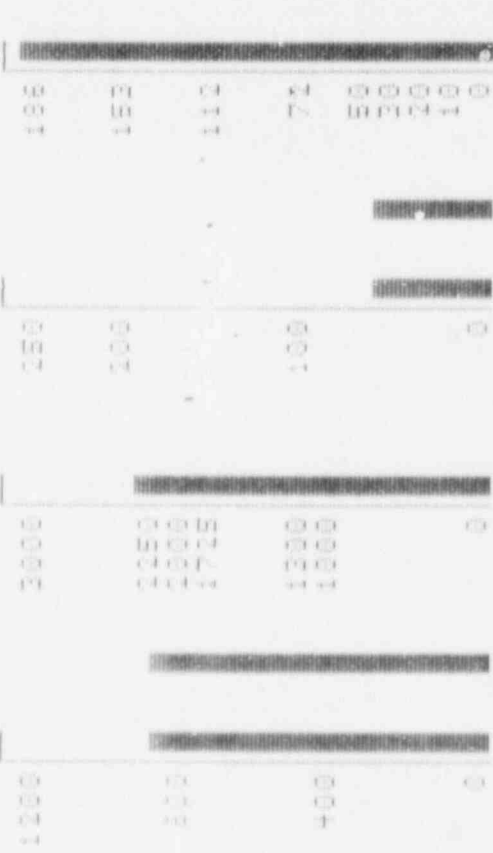
SG PRESS 21 22

RZR PRESS

LOOP SUBCOOL MARGIN 21 22

VESSEL LEVEL

CORE EXIT THERMOCOUPLES PTID DEG.F PTID DEG.F



PTID	DEG.F	PTID	DEG.F
T25	589	T11	587
T27	587	T29	587
T29	589	T12	589
T08	582	T09	589
T00	589	T15	589
T04	589	T22	589
T27	587	T28	589
T17	586	T16	589

CORE SUBCOOLED MARGIN

RSTN 58 59 60 61 62 63 64 65 66 67 68 69 70
 RST/M 58 59 60 61 62 63 64 65 66 67 68 69 70

F/M 58 60

AGENT STATUS
 RCS C ONI

ALARM/INDICATION

PAG FWD

PAG BCK

C.C.N.P.P. UNIT 2

CORE / RCS HEAT REMOVAL

REACTIVITY

RADIATION CONTROL

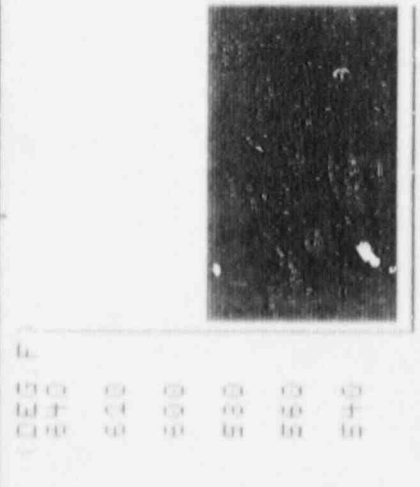
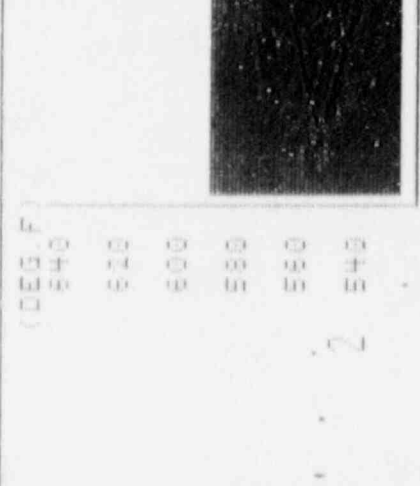
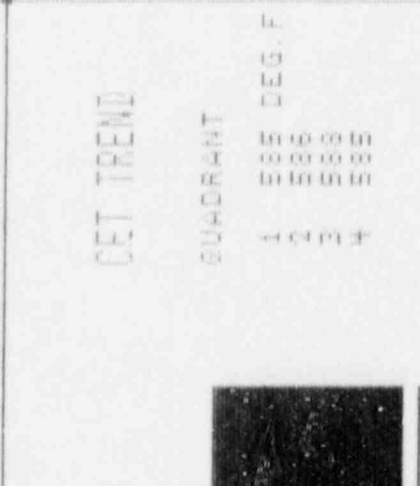
RCS PRESS & INVENTORY

VITAL AUX

CORE/RCS HEAT REMOVAL

CONTAINMENT ENVIRONMENT

CONTAINMENT ISOLATION



CET TREND

QUADRANT

1 55 DEG F

2 55 55

3 55 55

4 55 55

ALARM/INDICATION

PAGE FND

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REACTIVITY
RCS PRESS. & INVENTORY

CONTAINMENT ENVIRONMENT

CONTAINMENT ISOLATION

RADIATION CONTROL
VITAL AUX

CORE/RCS HEAT REMOVAL

(DEG. F)
500
555
600
655
700
755

(DEG. F)
500
555
600
655
700
755



1

2

CET TREND

QUADRANT

4 555 DEG. F
3 555
2 555
1 555

(DEG. F)
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655
700
755

(DEG. F)
500
555
600
655
700
755



3

4

ALARM/INDICATION

PAG FWD

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CORE / RCS HEAT REMOVAL

C. C. N. P. P. UNIT 2

- REACTIVITY
- RCS PRESS & INVENTORY
- VITAL AUX
- RADIATION CONTROL

- CORE/RCS HEAT REMOVAL

- CONTAINMENT ENVIRONMENT
- CONTAINMENT ISOLATION

- RED ALARMS
- 1 TOOLD HIGH
- 2 DELTA HIGH
- 3 LOSS OF FRI/SEC HEAT XFER
- 4 LOSS OF SWICHER FAILURE
- 5 LOSS OF BLOCK FAILURE
- 6 LOSS OF PRESS HIGH
- YELLOW ALARMS
- 8 SUBCOOL COOLDOWN RATE
- 9 SUBCOOLED MARGIN LOW
- 10 PRESS/LEVELS BLOCK
- 11 PRESS/LEVELS HIGH

- 12 LOSS OF PRESSURE
- 13 LOSS OF PRESSURE
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- 97 LOSS OF PRESSURE
- 98 LOSS OF PRESSURE
- 99 LOSS OF PRESSURE
- 100 LOSS OF PRESSURE

INDICATIONS

* VALIDATION CRITERIA NOT APPLIED

REG END

REG BOX

CONTAINMENT ENVIRONMENT

C.C.N.P.P. UNIT 2

REACTIVITY

RCS PRESS & INVENTORY

CORE/RCS HEAT REMOVAL

CONTAINMENT ENVIRONMENT

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RADIATION CONTROL

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RED ALARMS

- 1 CNTMT COOLING INADEQUATE
- 2 CEAS FAILURE
- 3 MFW TRIP FAILURE
- 4 CNTMT HYDROGEN HIGH HIGH

YELLOW ALARMS

- 5 CNTMT RAD HIGH
- 6 CNTMT TEMP HIGH
- 7 CNTMT HYDROGEN HIGH
- 8 CNTMT PRESSURE HIGH
- 9 CNTMT WATER LEVEL HIGH

INDICATIONS

- 10 CNTMT PRESSURE
- 11 CNTMT TEMPERATURE
- 12 CNTMT LEVEL
- 13 CNTMT RAD
- 14 CNTMT SPRAY FLOW
- 15 SA COOLERS
- 16 HYDROGEN (R8819X)
- 17 HYDROGEN (R8817X)

• VALIDATION CRITERIA NOT APPLIED

• PAG F4D

• PAG B0K

CONTAINMENT ISOLATION

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CNTMT RAC
10 7
10 6
10 5
10 4
10 3
10 2
10 1

HR
EPP
MCN

CNTMT NORMAL SUHP
MOV 5462 SHUT
MOV 5463 SHUT

CNTMT PURGE
CV 1410 SHUT
CV 1411 SHUT
CV 1412 SHUT
CV 1413 SHUT

CNTMT HYDROGEN PURGE
MOV 6900 SHUT
MOV 6901 SHUT

1 8+32+00 1 03+32+00
E/P

CNTMT SAMPLE
CV 5291 OPEN
CV 5292 OPEN

AGENT STATUS

0158 0000

0149 0000

0149 0000

ALARM/
INDICATION :
PAG END :
PAG BCK :

CONTAINMENT ISOLATION

C.C.N.P.P. UNIT 2

REACTIVITY

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VITAL AUX

RED ALARMS

- 1 OIS FAILURE
- * 2 CNTMT ISO VALVE FAILURE
- * 3 PEN RM VENT FAILURE
- * 4 RAS AND HRS1 REQIRD TO RMT

INDICATIONS

- 6 CNTMT RAD
- * 7 HR EFF MON
- * 8 VALVE STATUS
- 9 STATUS BLOCK

YELLOW ALARMS

- * 5 REDUNDANT ISOLATION VALVE OPEN

* VALIDATION CRITERIA NOT APPLIED

REC

REC

RAD CONTROL

C.C.N.P.P. UNIT 2

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RBC

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VITAL AUX

RED ALARMS

- * CONDENSER OFFGAS RAO HIGH HIGH
- * WASTE GAS DISCHARGE RAO HIGH HIGH
- * LIQUID WASTE DISCHARGE RAO HIGH HIGH
- * MAIN STM EFFLUENT RAO HIGH HIGH
- * HR EFF MON HIGH HIGH

YELLOW ALARMS

- * MAIN STM EFFLUENT RAO HIGH
- * SERVICE WATER DISCHARGE RAO HIGH
- * LIQUID WASTE DISCHARGE RAO HIGH
- * LEAKDOWN RAO HIGH
- * WASTE GAS MON HIGH
- * CONDENSER COOLING RAO HIGH
- * CONDENSER OFFGAS RAO HIGH
- * BLOWDOWN TANK RAO HIGH
- * HR EFF MON HIGH
- * BLOWDOWN TANK DISCH RAO HIGH

INDICATIONS

- * 16 HR EFF MON
- * 17 COND OFF GAS RAO
- * 18 21 MAIN STM EFF TO
- * 22 MAIN STM EFF RAO
- * 19 WASTE GAS RAO
- * 20 LIQUID WASTE RAO
- * 21 CNTHT RAO
- * 22 STATUS BLOCK

* VALIDATION CRITERIA NOT APPLIED

|| RAO FWD

|| RAO BCK

VITAL AUX

C.C.N.P.P. UNIT 2

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RBC

REACTIVITY

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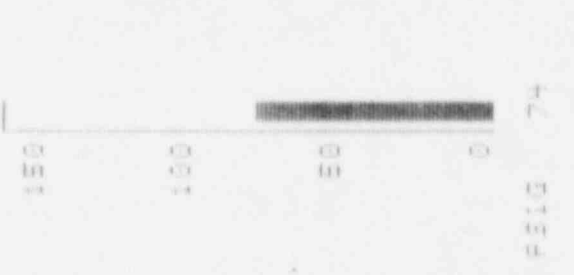
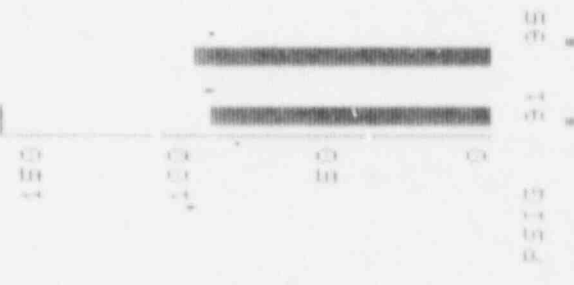
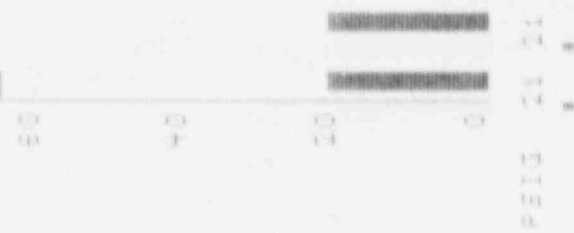
VITAL AUX

SALT WATER 24 24

SERVICE WATER 24 22

COMP COOLING

INSTR AIR



AGENT

6008 60 84R
6009 84R 84
6000 84R 84

STATUS

CLOSED
CLOSED
CLOSED

ALARM/INDICATION

RAS END

RAS BCK

C.C.N.P.P. UNIT 2

VITAL AUX

REACTIVITY
CONTAINMENT ISOLATION

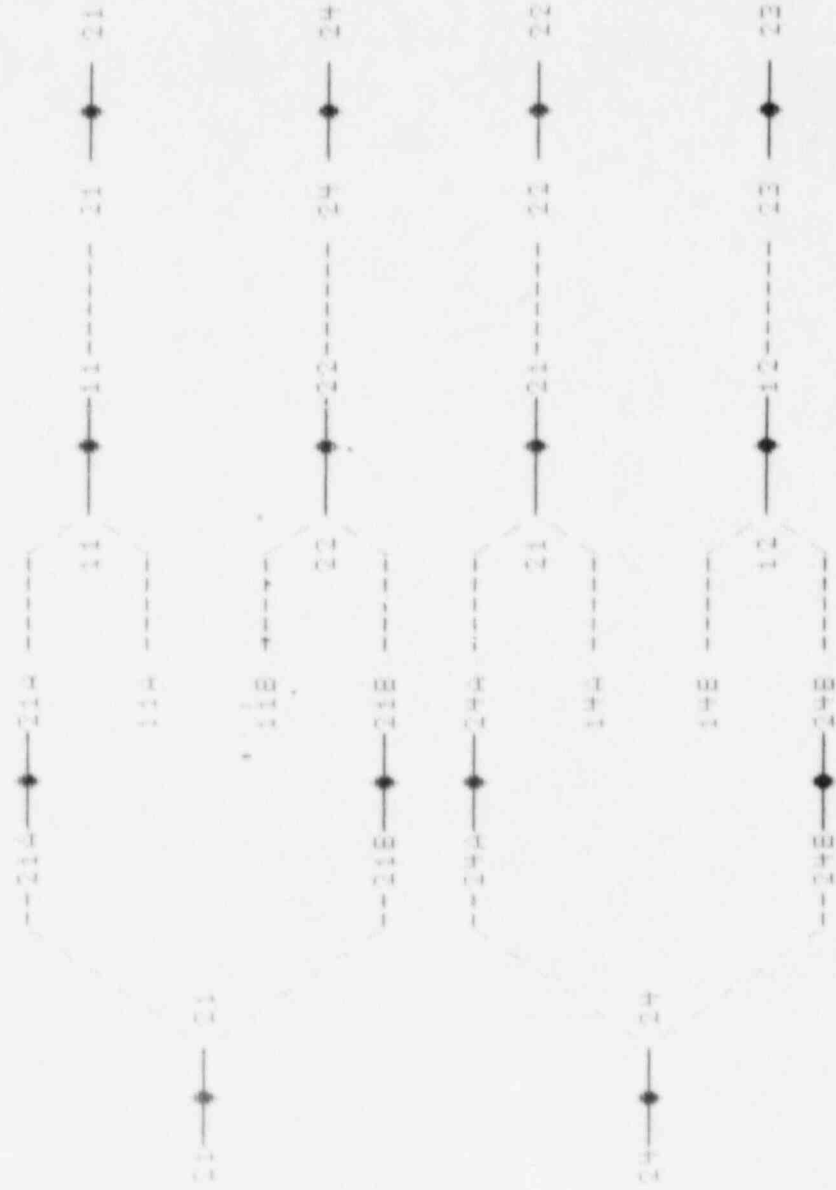
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CONTAINMENT ENVIRONMENT

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RADIATION CONTROL

ELECTRIC BUS MIMIC

480V 480V 125VDC 120VAC



LEGEND

ENERGIZED BUS

DEENERGIZED BUS

ALARM/INDICATION

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PAG BCK

