North Carolina State University

Nuclear Reactor Program
Department of Nuclear Engineering

Box 7909
Raleigh, NC 27695-7909
(919) 515-2321
FAX (919) 515-5115

11 December 1996

U.S. Nuclear Regulatory Commission
Attn: Region II Administrator
101 Marietta Street, N.W.
Atlanta, GA 30323

Subject: **Notification of a Reportable Event in Accordance with the NCSU PULSTAR Reactor's Technical Specifications Reporting Requirements**

Docket No. : 50-297
License No. : R-120

Dear Sir:

Summary

The PULSTAR reactor staff initiated a self assessment of the facility's design bases described in the Updated Final Safety Analysis Report (UFSAR). The Director of the facility contributed to this effort by heading an academic exercise in the form of a student design project for the PULSTAR Scram Logic Unit. The Director discovered through his review of the Scram Logic Unit a discrepancy between the UFSAR description of the unit's operation and the actual operation of the unit. However, the discrepancy is not safety related since the Scram Logic Unit has always provided fail-safe protection with redundancy provided in the form of redundant measuring channels. The discovered discrepancy does not invalidate any assumptions in the UFSAR accident analyses.

The UFSAR Section 7.3.2 describes the Scram Logic Unit as providing three different means which are implemented in two independent circuits to interrupt magnet current and cause a reactor scram. The PULSTAR surveillance program includes pre-start-up "end-to-end" checks of the Scram Logic Unit. These pre-start-up checks can not individually test the two independent circuits.

A special procedure was written for testing the Scram Logic Unit independent circuits and the results were that one of the independent scram paths was not functioning as described in the UFSAR. The functioning circuit is a fail-safe design consisting of contacts from relays associated with each scram input that are connected in series with the magnet power bus. This requires the six inputs to be in logic state 1 (+12 volts) to have magnet power available to the control rods.

Our evaluation also concluded the PULSTAR surveillance program was deficient in the pre-start-up check since it did not verify the full operation of the Scram Logic Unit as described in the UFSAR.

The Scram Logic Unit condition was found to deviate from the intended function described in the UFSAR. This meets the definition of a Reportable Event as defined in the facility's Technical Specifications Section 1.17(c):

> Incidents or conditions which prevented or could have prevented the intended safety function of an engineered safety feature or the reactor safety system.

In accordance with the reporting requirements specified in TS 6.7.1, the facility contacted Region II by telephone on Friday 6 December 1996 and this report is prepared in accordance with TS 6.7.2.

This report discusses the root cause for the discrepancy, corrective actions which have been completed, and descriptions of the sequence of events (Attachment 1) and Scram Logic Unit (Attachment 2).

Root Cause Determination

The root cause determination concludes two contributing factors. A mechanical failure of a cold soldered connection in the Scram Logic Unit was the cause of having one scram circuit contrary to the UFSAR description of two independent circuits. The second factor involves a deficiency in the surveillance procedures which did not test both circuits.

Corrective Actions

The Scram Logic Unit connection has been re-soldered and all connections have been verified to be mechanically sound. The unit has been successfully tested multiple times and has been declared operable. A full description of the corrective steps is provided in Attachment A.

A new surveillance procedure has been written for testing the Scram Logic Unit which demonstrates compliance with the intended function described in the UFSAR. The frequency for this test will be quarterly and supplements the pre-start-up Scram Logic Unit checks.

Conclusions

The PULSTAR reactor staff evaluated the design bases for the Scram Logic Unit and determined the Unit did not meet the UFSAR description. The discrepancy was not safety related since a fail-safe circuit integral to the Scram Logic Unit was available with redundant inputs from protective measuring channels. The facility staff has corrected the discrepancy and implemented a new surveillance procedure to ensure the Scram Logic Unit is tested in the future to demonstrate compliance with the design basis described in UFSAR.

Please feel free to contact us at (919)515-4598 if you or your staff have any questions or comments concerning this report.

Sincerely yours,

Pedro B. Perez
Associate Director, NRP

Charles W. Mayo, Ph.D.
Director, NRP

cc: U.S. Nuclear Regulatory Commission Document Control Desk
Mr. Alexander Adams, Jr., U.S.N.R.C.
Mr. Bruce Mallett, U.S.N.R.C. Region-II
Mr. Craig Bassett, U.S.N.R.C. Region-II
Dr. David Demaster, Chairman, NCSU Radiation Protection Committee

Attachments: Attachment 1 Summary of Events
Attachment 2 Scram Logic Unit Description

North Carolina State University
PULSTAR Reactor Facility

Docket No. : 50-297
License No. : R-120

Attachment A

Summary of Events

Background

The PULSTAR reactor staff initiated a self assessment of the Design Bases described in the UFSAR. Our effort consists of a chapter by chapter review of UFSAR descriptions and commitments and facility operating configuration and practices. The PULSTAR reactor facility is headed by a Director who is a faculty member in the Department of Nuclear Engineering. The academic environment provides unique opportunities for faculty support in PULSTAR reactor licensing matters and educational opportunities for students.

The Director teaches a senior level class titled "Nuclear Power Plant Instrumentation". This course includes the subjects of protection system logic and reliability analysis. Each class is assigned design projects that are performed by teams of 2 - 4 students. One project for the fall 1996 class was to develop a design for a replacement scram logic unit for the PULSTAR reactor. Initial guidance was that it should be more modular and perhaps use a more standard voting logic without decreasing the degree of protection provided by the present unit.

This project was led by a senior in Electrical and Computer Engineering who also had navy nuclear experience. This student would visit the Nuclear Engineering Department and talk with the NRP Reactor Operations Manager (ROM) or the NRP Director to obtain information and guidance about his work. On some occasions when he approached the NRP Director, the Director would go with him to obtain information from the ROM. In a few instances, the Director observed him talking to the ROM and joined the discussion.

Events Leading to Discovery of Scram Logic Unit Problem

Early in the project work, around late October or early November, the student approached the Director about making internal measurements in the scram logic unit. The interest was to obtain voltages at various points in the circuits and to measure power supply ripple. The Director talked with the ROM and was told that policy had been to not go into the scram logic unit and that its functions were tested from the outside only. The Director told the student that it was not sure that measurements of interest to him could be made, and left him to discuss his ideas with the ROM as part of learning how to work with operations personnel under the control of procedures.

On the afternoon of December 3, the student visited the Director and the conversation included the Directors advice about addressing testability in the design project. After their

general discussion, they walked down to the ROM's office where testing again came up and the ROM stated that the scram logic unit was tested at each start-up on an end-to-end basis by testing each scram input and verifying that a scram output was produced.

On the morning of December 4, the Director reviewed the scram logic unit schematic drawing and concluded that the three different means by which magnet current was interrupted could not be individually tested from outside of the chassis. He informed the Associate Director of this on his way to class at about 12:20 pm. The Associate Director advised the Director to check the functional description of the scram logic unit in the UFSAR. Later that afternoon, the Director reviewed Section 7.3.2 of the UFSAR and advised the Associate Director that the functioning of the different scram logic unit internal paths designed to interrupt the magnet current were specifically described in the UFSAR. There was a brief discussion about the need to review the surveillance procedure to assure that features described in the UFSAR were being individually tested and the Director and Associate Director returned to work on other activities.

The conversation between the Director and Associate Director was continued by telephone that evening. It was decided that the reactor would not be operated until this issue has been reviewed with the staff and the functioning of each element of the scram logic unit had been individually verified.

On the morning of Dec. 5, discussions with the ROM verified the conclusion that the different internal scram functions in the scram logic unit as described in the UFSAR had not been individually verified throughout the operating history of the facility. In reviewing the drawings, it was observed that external test points were available that could be used for this purpose. The ROM recalled that these had been made as a modification to the unit after it was received but they had not been used for surveillance. The review of pre-start-up testing records indicated that these modifications had probably been made between April 1972 and July 1972, but there was no record of the modifications other than their presence on a drawing, or of their testing or use.

Since the test points appeared on an approved drawing, it was decided to proceed with using them to test the individual scram logic functions, recognizing that this constituted the beginning of a maintenance activity on the scram logic unit and that the facility would not be operated until testing was complete and a revised surveillance procedure had been prepared and approved. Test instructions were prepared and the scram logic unit scram functions were tested individually between 5:15 and 5:45 pm that evening. All AND relay scrams functioned properly. The alternative scram paths of the K16 relay and the solid state switches, all driven through a common NAND bus, did not operate.

Bench Testing

On December 6, the scram logic unit was removed from the console and tested on the bench. The power supply voltages were normal and the NAND bus voltage was found to be correct. Resistance measurements indicated that the K16 relay contacts had opened in the scram condition as it was supposed to. However, when the AND relay scram contacts were bypassed to test the K16 interruption of the 40 volt magnet power, 40 volts was found to be on both sides of the K16 scram contact. The K16 relay contact resistance measurement and voltage interruption tests were performed several times with the same results. The wiring from the output of the AND relay scram contacts at pin 1 on card NCS 9&10 was traced and verified through card T2, MPR, SCR (the K16 relay card) through to RST (the lockout relay card), and to the test points.

It was then decided to test the unit with one card at a time removed to determine if there was an on-board problem which allowed 40 volts to get to the magnet side of the K16 scram contact when the AND relay scram contacts were bypassed. The RST card was removed, the unit energized, and a scram was not received. The RST card was reinstalled, the unit energized without bypass of the AND relay contacts. Scram was indicated and the NAND bus voltage was determined to be high and the K16 scram contact was open. The RST card test was then repeated by removing the RST card, bypassing the AND relay scram contacts and energizing the unit. This time there was a scram indication and it was known to be due to the K16 relay operation as this was the only relay that could turn the scram indication lamp on with the RST card removed.

Subsequent bench testing demonstrated the that individual scram functions of the AND relays, K16 relay, and the solid state switches were all functioning normally. However, when unit was installed in the console and tested again, the K16 relay scram did not function.

Over the weekend (Dec. 7 - 8) the test results were reviewed and it was concluded that the most likely problem was either degraded 6 volt supply to the NAND circuits or a problem with the NAND bus before it was distributed to the K16 relay and solid state switches. On Monday, Dec, 9, the unit was removed from the console and the 6 volt power distribution and the NAND bus were traced. Each connection was examined with a magnifying glass and each wire was tugged slightly with needle nose pliers to verify the mechanical integrity of the connection.

No suspect connections were found in the 6 volt power distribution. In tracing the NAND bus, a cold solder joint was found where the bus connects to pin 9 of the SCR card socket. This is the point where the NAND bus is distributed to the K16 relay and solid state switches. This was an obvious problem upon inspection. While there was solder on pin 9 and solder on the bus lead, there was no mechanical attachment and the wire moved freely within the eyelet of pin 9.

The incoming NAND bus connection was soldered to pin 9 of the SCR card socket and the unit was tested successfully on the bench and in the console.

Summary of Trouble-shooting Activities

- The wiring associated with the test points is correct as shown on the drawing
- All other wiring examined as part of the troubleshooting is correct as shown on the drawing
- There was a problem inhibiting the NAND bus scram functions when the unit was first tested in the console.
- This problem cleared during the removal and insertion of the RST card.
- The NAND bus was found to be inserted in but not soldered to pin 9 of the SCR card. This is the connection where the bus is distributed to the K16 relay and the solid state switches.
- The RST card is adjacent to the SCR card. Removing and inserting the RST card would slightly flex the bus connections on the backplane. This is consistent with the intermittent operation of the NAND scram functions when testing was being performed with the RST card alternately removed and inserted.
- The unit functioned properly after the NAND bus was soldered to pin 9 of the SCR card.

Attachment 2

Description of
N.C. State University PULSTAR Reactor
Scram Logic Unit

CONTROL RODS

The N.C. State University PULSTAR Reactor has four silver-indium-cadmium control blades that are typically referred to as "rods". Two rods are designated as Safety #1 and Safety #2. A third rod is designated as the Regulating rod. The fourth rod was used for pulsing and is now held out of the core.

The two safety rods and the regulating rod are held to the drive mechanism by electromagnets. When a scram set-point is reached, the scram logic unit interrupts the magnet current and these rods fall into the core.

SCRAM LOGIC UNIT

Control Rod Power

The scram logic unit provides 40 volt DC power to the rod holding magnets. Each magnet draws about 0.040 amperes. When a scram set-point is reached, the scram logic unit is designed to interrupt the magnet current through two different paths.

AND Relays

To obtain scram inputs, the scram logic unit sends 12 volt DC power to normally closed contacts in external components which generate scram inputs. This 12 volt power is returned to the scram logic unit through a separate circuit for each scram input. Within the scram logic unit, each 12 volt input holds a physically different relay (called an AND relay) in the energized position. The magnet power passes through a closed-when-energized contact in each relay. Loss of power to the scram logic unit, a failure of the 12 volt DC power supply, an open circuit between the scram logic unit and the remote contact, the opening of scram channel test switches mounted on the front of the scram logic unit, or the opening of remote scram demand contacts will interrupt the 12 volt return to the associated AND relays. The AND relays which loose 12 volt power go to the de-energized state and open a contact which interrupts the current to all rod magnets.

NAND Bus

The 12 volt returns that hold the AND relays energized is also used as the input to discrete transistor circuits, one for each AND relay, that use a 6 volt power supply to invert the 12 volt input logic and combine the inverted logic in a common NAND bus. The NAND bus is therefore normally "low", but will change to the "high" state (slightly less than 6 volts) when any one or more scram inputs are received. The NAND bus is used as a control input to the K16 relay and the solid state switches that also act to interrupt the magnet current.

Since the NAND bus goes high on receiving a scram demand, a ground on the NAND bus, or an open circuit between the NAND bus inputs and the K16 relay or the solid state switches will inhibit NAND scram functions. The NAND bus 6 volt power supply has a power monitor relay that will interrupt the current to all magnets if the 6 volt power fails.

K16 Relay

A second means by which magnet current is interrupted is the normally de-energized K16 relay. When the NAND bus goes high, the K16 switching transistor is turned on to energize the relay and open a contact that interrupts the 40 volt DC supply to all magnets. This path provides some diversity in interrupting the current to all magnets in the sense that the relay acts on being energized to open as opposed to being de-energized to open.

Solid State Switches

The return current from each magnet passes through a transistor, one transistor per magnet, to reach the 40 volt power supply ground. These transistors are normally turned on so that magnet current can flow through them. The NAND bus is connected to a driver transistor for each current switching transistor. If the NAND bus goes to the "high" state, the magnet current switching transistors turn off and interrupt the magnet current. This path provides diversity in interrupting the current to individual magnets in the sense that the solid state switches also provide backup to the AND relays.