REMOTE I/O EQUIPMENT HARDWARE ACCEPTANCE TEST PROCEDURE for NUS CORP. / BALTIMORE GAS and ELECTRIC CALVERT CLIFFS DATA ACQUISITION SYSTEM

AT ~~C.P.I.~~ (FORT LAUDERDALE)
2 February 1984

VENDOR'S DRAWING REVIEW

1 ☐ Proceed, may proceed.
2 ☒ Revise ... may proceed.
3 ☐ Amend ... may proceed
4 ☐ ... for
5 ☐
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8
By L.W. Stalty 2/21/84
BALTIMORE ... CO.
ELECTRONICS DIVISION

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☐ ISSUED FOR INFORMATION
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COMPUTER PRODUCTS, INCORPORATED

MEASUREMENT & CONTROL SYSTEMS DIVISION

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UNIT # _____

SYSTEM CABINET ID: _____

TEST CONDUCTOR : _____

NUS REPRESENTATIVE : _____

BGE REPRESENTATIVE : _____

Procedure copy complete : Initials : _____/_____/_____

DATE TEST STARTED : _____

LOG BOOK PAGES: _____ _____ _____ _____ _____ _____

_____ _____ _____ _____ _____ _____

_____ _____ _____ _____ _____ _____

TEST COMPLETED BY: _____ DATE _____

(C.P.I.) TITLE: _____

TEST WITNESSED BY: _____ DATE _____

(N.U.S.) TITLE: _____

TEST WITNESSED BY: _____ DATE _____

(B.G.E.) TITLE: _____

1. GENERAL DESCRIPTION

The purpose of this document is to provide a procedure for the performance of a customer acceptance test of the remote input/output equipment hardware purchased by NUS Corporation by purchase order number DA 8827-1 and sold by Computer Products Incorporated, Measurement and Control Systems Division by sales order numbers 28334 (Unit I) and 28335 (Unit II) at the Fort Lauderdale plant of CPI . This equipment is destined to be installed in the Baltimore Gas and Electric Calvert Cliffs power generation plant.

The equipment is broken into two 'units', 'Unit 1' and 'Unit 2'. Each unit is divided into two 'channels', 'Channel A' and 'Channel B'. The channels are composed of the following 'subsystems': 'Safety Related A', 'Safety Related B', 'Non-Safety Related A', 'Non-Safety Related B', 'Shared A-B', 'Data Concentrator / Maintenance Panel A', and 'Data Concentrator/ Maintenance Panel B'. Each subsystem may be composed of one or more cabinets containing the I/O equipment.

The testing of the remote I/O equipment at this level does not include the Data Concentrator equipment nor the Data Concentrator remote links, the Intelligent Remote Control Units.

Testing will be performed on a per cabinet basis with one copy of this procedure assigned to each cabinet. Each type of product in a cabinet will be tested as a group before proceeding to the next type of equipment.

Cabinets in the Non-Safety Related and the Shared subsystems have wiring that source or terminate in another cabinet within its subsystem and due to this inter-cabinet and inter-chassis wiring, some connections and measurements will be made at cabinets or controllers other than the one under test.

2. TABLE OF CONTENTS / SCOPE OF TESTS

SECTION 3. - Dispositioning and Test Data Recording

The dispositioning of the tested product and the recording of test results is described in this section.

SECTION 4. - Test Equipment Requirements

The equipment required to perform this acceptance test is listed in this section.

SECTION 5. - Reference Documents

Documents referenced by the procedure and the documents associated with the equipment under test and the test equipment are listed.

SECTION 6. - Configuration of Equipment for Testing

This section describes the special configurations of the test equipment and the equipment to be tested for the performance of the tests.

SECTION 7. - Equipment Under Test Configuration Verification

The correspondance of the configuration of the equipment in the cabinet to the equipment configuration drawings will be verified.

SECTION 8. - AC Power Distribution/Indicator Panel and Power Supply Validation

The AC Power Distribution and Indicator Panel and the power supplies will be validated as operational and the corresponding power wiring will be validated to be accurate.

SECTION 9. - Optically Isolated Digital Input Module Validation

Each Optically Isolated Digital Input Module and the corresponding signal conditioning module will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 10. - O.I.D.I. Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected Optically Isolated Digital Inputs in the cabinet under test will be validated as operational in compliance with IEEE standard # 472.

SECTION 11. - Change of State Digital Input Module Validation

Each Change of State Digital Input Module and the corresponding signal conditioning module will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 12. - C.O.S.D.I. Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected Change of State Digital Inputs in the cabinet under test will be validated as operational in compliance with IEEE standard # 472.

SECTION 13. - Quad Pulse Counter Module Validation

Each Quad Pulse Counter Module and the corresponding signal conditioning module will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 14. - Quad Pulse Counter Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected Quad Pulse Counters in the cabinet under test will be validated as operational in compliance with IEEE standard # 472.

SECTION 15. - Up/Down Pulse Counter Module Validation

Each Up/Down Pulse Counter Module and the corresponding signal conditioning module will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 16. - Up/Down Pulse Counter Module Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected Up/Down Pulse Counters in the cabinet under test will be validated as operational in compliance with IEEE standard # 472.

SECTION 17. - Digital and Analog Loopback and Calibration Module and Analog to Digital Converter Module Validation

Each Digital and Analog Loopback and Calibration Module and Analog to Digital Converter Module will be validated as operational and accurate; the temperature sensing transducers will be validated as operational and accurate; and the associated cabling will be associated to be accurate.

SECTION 18. - Power Supply Monitoring Analog Inputs Validation

Each analog input gate module monitoring the cabinet power supplies, the RTD SCM power supplies, and the contact sense power supplies will be validated as operational, and the associated cabling will be validated to be accurate.

SECTION 19. - Voltage Sensing Analog Input Gate Module Validation

Each voltage sensing analog input gate module and the corresponding signal conditioning module will be validated as operational, and the associated cabiling will be validated to be accurate.

SECTION 20. - Voltage Sensing Analog Input Gate Module Accuracy, Common Mode Voltage Rejection, and Surge Withstand Capability Validation

The common mode voltage rejection and the accuracy of a sample of up to five percent (or at least one) of the voltage sensing analog input gate modules in the cabinet will be validated. Then a surge will be applied to the sample in compliance with IEEE standard # 472. The common mode voltage rejection and accuracy of the sample will then be revalidated to validate the operation of the surge protection circuitry.

SECTION 21. - Resistive Sensing Analog Input Gate Module Validation

Each resistive sensing analog input gate module and the corresponding signal conditioning module(s) will be validated as operational, and the associated cabling will be validated as accurate.

SECTION 22. - Resistive Sensing Analog Input Gate Module Surge Withstand Capability Validation

The surge withstand capability of a sample of up to five percent (or at least one) of the surge protected resistive sensing analog inputs in the cabinet under test will be validated as operational in compliance with IEEE standard # 472.

SECTION 23. - Voltage Sensing Analog Input Gate Module Stability Validation

The voltage sensing analog input gate modules selected for validation of common mode voltage rejection, accuracy, and surge withstand capability will be validated to be stable.

APPENDIX A. - Test and Repair Log Book Format

The format of the log book used to document records of the testing and any anomalies or non-conformances found is illustrated in this appendix.

APPENDIX B. - CPI RTP Control Panel Description and Operating Instructions

This appendix contains a description and instructions on the operation of the CPI RTP Control Panel, one of the primary pieces of test equipment used to perform the test.

APPENDIX C. - Slot/Address Cross Reference Table for UI/0C and RAUI/0C

This is a table cross referencing the physical slot number of the option card slots of the Universal I/0 Controllers with their programming addresses.

APPENDIX D. - Operating Instructions and Test Configuration for Velonex Transient Surge Transient Generator

The operation and configuration of the Velonex Surge Transient Generator, used to test the surge withstand capabilities of the equipment in compliance with IEEE standard # 472 is described in this appendix.

ATTACHMENT 1. - Test Configuration Drawings

This attachment contains drawings depicting the configurations of test equipment used for the various tests.

ATTACHMENT 2. - Equipment Configuration Drawings

This attachment contains the drawings of the configuration of the equipment in the cabinet as the equipment will be tested.

3. DISPOSITIONING AND TEST DATA RECORDING

The acceptance test will be performed using a copy of this procedure stamped 'Controlled Document' with the required signatures on the approval signature page (page 2).

At the beginning of the test :

1) The test conductor and the representatives from NUS and BGE will print their names on the test performance signature page (page 3) of the copy of the test procedure; (All entries made on all documents will be made in black ink.)

2) The copy will be verified to assure that there is one and only one copy of each page of the procedure included; The test performance signature page will then be initialed;

3) An entry will be made to the 'Test and Repair Log' using the format illustrated in Appendix A, to mark the commencement of the test on a cabinet;

4) The unique identification of the cabinet under test will be entered on the test performance signature page;

5) The page number of any and all pages of the log book associated with the cabinet under test will also be recorded on the test performance signature page; and

6) The CPI identification numbers, where applicable, of the test equipment used to perform this acceptance test will be noted in the required test equipment section (Section 4.) of the copy of the procedure.

A module identifier block appears in each verification/ validation section of this proedure. Successful completion of applicable steps of the procedure on an individual product or product set shall be indicated by entering the location identifier of the module in the controller and the controller's identifier and initialed by the test conductor and a witness.

A signature block appears at the end of each verification/ validation section of this procedure. Successful completion of an applicable section on all products specified by the procedure shall be indicated by the signatures of the appropriate representatives of CPI, NUS, and BGE (where applicable).

When a section of the procedure is NOT applicable to a cabinet, 'N/A' will be entered on the signature lines and will be initialed by the appropriate representatives.

Anomalies or non-conformances encountered during the performance of the test shall be handled as follows:

1) An entry is made in the Test and Repair Log describing the non-conformance;

2) The non-conformance will be documented on a Non-Conforming Material Report (NCMR) form (reference: AQ 5.01);

3) The non-conformance is corrected;

4) The corrective action is documented in the Test and Repair Log;

5) The corrective action is documented on the NCMR form;

6) The applicable validation steps are repeated and successful completion is indicated by the signatures of the representatives on the signature block.

Note that if a non-conformance is encountered during the performance of one of the validations of a five percent sample, the steps above will be performed and in addition another sample is selected and tested.

4. TEST EQUIPMENT REQUIRED

The equipment required to perform this acceptance test is as listed below:

(All electronic test equipment shall be in compliance with C.P.I. Quality Assurance procedure AQ 8.02 - 'Calibration Control System'.)

4.1 Digital multimeter :
Hewlett Packard Co. Model # 3468B . . . . CPI ID # _____

4.2 Programmable DC Voltage Source :
Electronic Development Corp. Model # 501-J CPI ID # _____

4.3 AC/DC V-A Source :
RFL Industries, Inc. Model No. 828 . . . CPI ID # _____.

4.4 Surge Transient Generator :
Velonex Model No. 510 . . . . . CPI ID # _____

4.5 Digital Thermometer :
Omega Engineering Inc. Model No. 2166A . CPI ID # _____

4.6 CPI Analog Input System Test Computer : LSI-11 based

(See the 'Description and Operating Instructions for the CPI Analog Input Test Computer and Analog Input Test Programs')

4.7 CPI RTP Control Panels , 2 ea.
(CPI # 070-0044-001)

4.8 CPI Universal I/O Controller
(CPI # 070-0004-003)

4.9 CPI Special Relay Output Module with contact protection
(CPI # 000-7066-000)

4.10 CPI Special Pulsing Relay Output Module with contact protection
(CPI # 000-7067-000)

4.11 CPI I/O Bus Termination Module
(CPI # 021-0004-000)

4.12 CPI RTP I/O Bus Cables
(CPI # 314-0001-010 1 each and
CPI # 314-0001-020 1 each)

4.13 CPI 12 Volt Power Supply, panel mounted
(CPI # 070-0008-000)

4.14 CPI BTSCA (25 inch, 48 pin) to Test Cable/Connector Adapter
(CPI # 000-7077-000)

4.15 CPI Digital Input Surge Protection Test Connector
(CPI # 000-7078-000)

4.16 CPI Pulse Counter Surge Protection Test Connector
(CPI # 000-7097-000)

4.17 CPI Analog Input Unbalanced (1 Kohm) Test Termination/Connector
(CPI # 000-7079-000)

4.18 CPI Digital Test Cable
(CPI # 000-7080-000)

4.19 CPI Analog Input Test Divider/Connector for BTSCAs
(CPI # 000-7081-000)

4.20 CPI Analog Input Parallel Input Test Connector
(CPI # 000-7082-000)

4.21 CPI Analog Input Test Divider/Connector for UTRPs
(CPI # 000-7085-000)

4.22 CPI RTD Resistor Termination: Platinum 200 ohm, 32 : 350 F
(CPI # 000-7086-000)

4.23 CPI RTD Resistor Termination: Platinum 200 ohm, 32 : 850 F
(CPI # 000-7087-000)

4.24 CPI RTD Resistor Termination: Platinum 200 ohm, 32 : 110 F
(CPI # 000-7088-000)

4.25 CPI RTD Resistor Termination: Copper 10 ohm, -10 : 209 C
(CPI # 000-7089-000)

4.26 CPI Up/Down Pulse Counters Test Headers w/ diodes
(CPI # 000-7098-000, -001, -002, -003)

4.27 AC Power Receptacle Tester :
Ideal Industries, Inc. Model No. 61-035

5. REFERENCE DOCUMENTS

This section lists the documents referenced by the procedure and the documents associated with the equipment under test and the test equipment. Other documents may be referred to by the documents listed in this section.

5.1 CPI Univ. A.D.C. Card and Univ. A.I. Card Set (# 021-0211)

5.1.1 Parts List (CPI # AP 020-0211)
5.1.2 Parts List (CPI # AP 021-0211)
5.1.3 Schematic (CPI # CS 021-0211)
5.1.4 Assembly Dwg. (CPI # CA 021-0211)
5.1.5 Technical Manual (CPI # 980-0021-211)
5.1.6 Engineering Specification (CPI # AE 021-0211)
5.1.7 Test Procedure (CPI # AT 021-0211)

5.2 CPI Digital Input Card (# 021-5227)

5.2.1 Parts List (CPI # AP 020-5227)
5.2.2 Parts List (CPI # AP 021-5227)
5.2.3 Schematic (CPI # CS 021-5227)
5.2.4 Assembly Dwg. (CPI # CA 021-5227)
5.2.5 Technical Manual (CPI # 980-0021-227)
5.2.6 Engineering Specification (CPI # AE 021-5227)
5.2.7 Test Procedure (CPI # AT 021-5227)

5.3 CPI Optically Isolated Digital Input Card (# 021-5230)

5.3.1 Parts List (CPI # AP 020-5230)
5.3.2 Parts List (CPI # AP 021-5230)
5.3.3 Schematic (CPI # CS 021-5230)
5.3.4 Assembly Dwg. (CPI # CA 021-5230)
5.3.5 Technical Manual (CPI # 980-0021-230)
5.3.6 Engineering Specification (CPI # AE 021-5230)
5.3.7 Test Procedure (CPI # AT 021-5230)

5.4 CPI Universal H.S.W.R. Analog Input Gate Card (# 021-5234)

5.4.1 Parts List (CPI # AP 020-5234)
5.4.2 Parts List (CPI # AP 021-5234)
5.4.3 Schematic (CPI # CS 021-5234)
5.4.4 Assembly Dwg. (CPI # CA 021-5234)
5.4.5 Technical Manual (CPI # 980-0021-211)
5.4.6 Engineering Specification (CPI # AE 021-5234)
5.4.7 Engineering Specification (CPI # AE 021-0211)
5.4.8 Test Procedure (CPI # AT 021-5234)
5.4.9 Test Procedure (CPI # AT 021-0211)

5.5 CPI Digital and Analog Loopback and Cal. Card (# 021-5271)

- 5.5.1 Parts List (CPI # AP 021-5271)
- 5.5.2 Schematic (CPI # CS 021-5271)
- 5.5.3 Assembly Dwg. (CPI # CA 021-5271)
- 5.5.4 Engineering Specification (CPI # AE 021-5271)
- 5.5.5 Test Procedure (CPI # AT 021-5271)

5.6 CPI Quad Pulse Counter Card (# 021-5278)

- 5.6.1 Parts List (CPI # AP 021-5278)
- 5.6.2 Schematic (CPI # CS 021-5278)
- 5.6.3 Assembly Dwg. (CPI # CA 021-5278)
- 5.6.4 Engineering Specification (CPI # AE 021-5278)
- 5.6.5 Test Procedure (CPI # AT 021-5278)

5.7 CPI Change of State Digital Input Card (# 038-5064)

- 5.7.1 Parts List (CPI # AP 038-5064)
- 5.7.2 Schematic (CPI # CS 038-5064)
- 5.7.3 Assembly Dwg. (CPI # CA 038-5064)
- 5.7.4 Engineering Specification (CPI # AE 038-5064)
- 5.7.5 Test Procedure (CPI # AT 038-5064)

5.8 CPI Analog Input Signal Conditioning Module (# 038-5097)

- 5.8.1 Parts List (CPI # AP 038-5097)
- 5.8.2 Schematic (CPI # CS 038-5097)
- 5.8.3 Assembly Dwg. (CPI # CA 038-5097)
- 5.8.4 Engineering Specification (CPI # AE 038-5097)
- 5.8.5 Test Procedure (CPI # AT 038-5097)

5.9 CPI Digital Input Signal Conditioning Module (# 038-5098)

- 5.9.1 Parts List (CPI # AP 038-5098)
- 5.9.2 Schematic (CPI # CS 038-5098)
- 5.9.3 Assembly Dwg. (CPI # CA 038-5098)
- 5.9.4 Engineering Specification (CPI # AE 038-5098)
- 5.9.5 Test Procedure (CPI # AT 038-5098)

5.10 CPI C.O.S. D.I. Signal Conditioning Module (# 038-5099)

- 5.10.1 Parts List (CPI # AP 038-5099)
- 5.10.2 Schematic (CPI # CS 038-5099)
- 5.10.3 Assembly Dwg. (CPI # CA 038-5099)
- 5.10.4 Engineering Specification (CPI # AE 038-5099)
- 5.10.5 Test Procedure (CPI # AT 038-5099)

5.11 CPI RTD Signal Cond. Module w/ P.S. Monitor Out (# 038-5108)

- 5.11.1 Parts List (CPI # AP 038-5108-XYZ)
- 5.11.2 Schematic (CPI # CS 038-5108)
- 5.11.3 Assembly Dwg. (CPI # CA 038-5108)
- 5.11.4 Technical Manual (CPI # 980-0040-213)
- 5.11.5 Engineering Specification (CPI # AE 038-5108-XYZ)
- 5.11.6 Test Procedure (CPI # AT 038-5108)
- 5.11.7 Information Drawing (CPI # AH 038-5108-XYZ)

5.12 CPI Up/Down Pulse Counter Card (# 038-5115)

- 5.12.1 Parts List (CPI # AP 038-5115)
- 5.12.2 Schematic (CPI # CS 038-5115)
- 5.12.3 Assembly Dwg. (CPI # CA 038-5115)
- 5.12.4 Engineering Specification (CPI # AE 038-5115)
- 5.12.5 Test Procedure (CPI # AT 038-5115)

5.13 CPI Digital Barrier Terminal Strip Cable Assembly (# 040-5453)

- 5.13.1 Parts List (CPI # AP 040-5453)
- 5.13.2 Assembly Dwg. (CPI # CA 040-5453)
- 5.13.3 Engineering Specification (CPI # AE 040-5453)
- 5.13.4 Wire List (CPI # AW 040-5453)

5.14 CPI Signal Conditioning Module Chassis (# 040-5454)

- 5.14.1 Parts List (CPI # AP 040-5454)
- 5.14.2 Assembly Dwg. (CPI # CA 040-5454)
- 5.14.3 Engineering Specification (CPI # AE 040-5454)

5.15 CPI A.I. Gate Card to Signal Cond. Module Cable (# 040-5455)

- 5.15.1 Parts List (CPI # AP 040-5455)
- 5.15.2 Assembly Dwg. (CPI # CA 040-5455)
- 5.15.3 Engineering Specification (CPI # AE 040-5455)
- 5.15.4 Wire List (CPI # AW 040-5455)

5.16 CPI Digital Card to Signal Cond. Module Cable (# 040-5456)

- 5.16.1 Parts List (CPI # AP 040-5456)
- 5.16.2 Assembly Dwg. (CPI # CA 040-5456)
- 5.16.3 Engineering Specification (CPI # AE 040-5456)
- 5.16.4 Wire List (CPI # AW 040-5456)

5.17 CPI U-16 Universal I/O Controller (# 040-5462)

- 5.17.1 Parts List (CPI # AP 040-5462)
- 5.17.2 Logic Dwg. (CPI # CL 070-5073)
- 5.17.3 Assembly Dwg. (CPI # CA 040-5462)
- 5.17.4 Technical Manual (CPI # 980-0070-004)
- 5.17.5 Engineering Specification (CPI # AE 040-5462)
- 5.17.6 Test Procedure (CPI # AT 070-5073)
- 5.17.7 Wiring Diagram (CPI # CW 318-5010)

5.18 CPI Reversed RTD Signal Conditioning Chassis (# 040-5467)

- 5.18.1 Parts List (CPI # AP 040-5467)
- 5.18.2 Assembly Dwg. (CPI # CA 040-5467)
- 5.18.3 Engineering Specification (CPI # AE 040-5467)
- 5.18.4 Test Procedure (CPI # AT 040-5467)
- 5.18.5 Wiring Diagram (CPI # CW 040-5467)
- 5.18.6 Technical Manual (CPI # 980-0040-213)

5.19 CPI Redundant +/-15 Volt/ 2.25 Amp Power Supply (# 040-5482)

- 5.19.1 Parts List (CPI # AP 040-5482)
- 5.19.2 Assembly Dwg. (CPI # CA 040-5482)
- 5.19.3 Engineering Specification (CPI # AE 040-5482)
- 5.19.4 Test Procedure (CPI # AT 040-5482)
- 5.19.5 Wiring Diagram (CPI # CW 040-5482)

5.20 CPI Redundant 5 Volt/ 30 Amp Power Supply (# 040-5483)

- 5.20.1 Parts List (CPI # AP 040-5483)
- 5.20.2 Assembly Dwg. (CPI # CA 040-5483)
- 5.20.3 Engineering Specification (CPI # AE 040-5483)
- 5.20.4 Test Procedure (CPI # AT 040-5483)
- 5.20.5 Wiring Diagram (CPI # CW 040-5483)

5.21 CPI Redundant +/-15 Volt/ 4.5 Amp Power Supply (# 040-5484)

- 5.21.1 Parts List (CPI # AP 040-5484)
- 5.21.2 Assembly Dwg. (CPI # CA 040-5484)
- 5.21.3 Engineering Specification (CPI # AE 040-5484)
- 5.21.4 Test Procedure (CPI # AT 040-5484)
- 5.21.5 Wiring Diagram (CPI # CW 040-5484)

5.22 CPI Redundant 5 Volt/ 60 Amp Power Supply (# 040-5485)

- 5.22.1 Parts List (CPI # AP 040-5485)
- 5.22.2 Assembly Dwg. (CPI # CA 040-5485)
- 5.22.3 Engineering Specification (CPI # AE 040-5485)
- 5.22.4 Test Procedure (CPI # AT 040-5485)
- 5.22.5 Wiring Diagram (CPI # CW 040-5485)

5.23 CPI Redundant +/-15 Volt/ 9.0 Amp Power Supply (# 040-5486)

- 5.23.1 Parts List (CPI # AP 040-5486)
- 5.23.2 Assembly Dwg. (CPI # CA 040-5486)
- 5.23.3 Engineering Specification (CPI # AE 040-5486)
- 5.23.4 Test Procedure (CPI # AT 040-5486)
- 5.23.5 Wiring Diagram (CPI # CW 040-5486)

5.24 CPI Redundant 5 Volt/ 120 Amp Power Supply (# 040-5487)

- 5.24.1 Parts List (CPI # AP 040-5487)
- 5.24.2 Assembly Dwg. (CPI # CA 040-5487)
- 5.24.3 Engineering Specification (CPI # AE 040-5487)
- 5.24.4 Test Procedure (CPI # AT 040-5487)
- 5.24.5 Wiring Diagram (CPI # CW 040-5487)

5.25 CPI A.I. Gate Card to RTD Sig. Cond. Mod. Cable (# 040-5505)

- 5.25.1 Parts List (CPI # AP 040-5505)
- 5.25.2 Assembly Dwg. (CPI # CA 040-5505)
- 5.25.3 Engineering Specification (CPI # AE 040-5505)
- 5.25.4 Wire List (CPI # AW 040-5505)

5.26 CPI Redundant 125 Volt/ 1.0 Amp Power Supply (# 040-5509)

- 5.26.1 Parts List (CPI # AP 040-5509)
- 5.26.2 Assembly Dwg. (CPI # CA 040-5509)
- 5.26.3 Engineering Specification (CPI # AE 040-5509)
- 5.26.4 Test Procedure (CPI # AT 040-5509)
- 5.26.5 Wiring Diagram (CPI # CW 040-5509)

5.27 CPI AC Power Distribution / Indicator Panel (# 040-5511)

- 5.27.1 Parts List (CPI # AP 040-5511)
- 5.27.2 Assembly Dwg. (CPI # CA 040-5511)
- 5.27.3 Engineering Specification (CPI # AE 040-5511)
- 5.27.4 Test Procedure (CPI # AT 040-5511)
- 5.27.5 Wiring Diagram (CPI # CW 040-5511)

5.28 CPI Pulse Counter Card to S.C.M. Cable (# 040-5517)

- 5.28.1 Parts List (CPI # AP 040-5517)
- 5.28.2 Assembly Dwg. (CPI # CA 040-5517)
- 5.28.3 Engineering Specification (CPI # AE 040-5517)
- 5.28.4 Wire List (CPI # AW 040-5517)

5.29 CPI Up/Down Pulse Counter Card to S.C.M. Cable (# 040-5518)

- 5.29.1 Parts List (CPI # AP 040-5518)
- 5.29.2 Assembly Dwg. (CPI # CA 040-5518)
- 5.29.3 Engineering Specification (CPI # AE 040-5518)
- 5.29.4 Wire List (CPI # AW 040-5518)

5.30 CPI Digital Barrier Terminal Strip Cable Assembly (# 040-5519)

- 5.30.1 Parts List (CPI # AP 040-5519)
- 5.30.2 Assembly Dwg. (CPI # CA 040-5519)
- 5.30.3 Engineering Specification (CPI # AE 040-5519)
- 5.30.4 Wire List (CPI # AW 040-5519-0)
- 5.30.5 Wire List (CPI # AW 040-5519-1)

5.31 CPI Analog Barrier Terminal Strip Cable Assembly (# 040-5520)

- 5.31.1 Parts List (CPI # AP 040-5520)
- 5.31.2 Assembly Dwg. (CPI # CA 040-5520)
- 5.31.3 Engineering Specification (CPI # AE 040-5520)
- 5.31.4 Wire List (CPI # AW 040-5520)

5.32 CPI RTD S.C.M. Barrier Terminal Strip Cable Ass'y (# 040-5521)

- 5.32.1 Parts List (CPI # AP 040-5521)
- 5.32.2 Assembly Dwg. (CPI # CA 040-5521)
- 5.32.3 Engineering Specification (CPI # AE 040-5521)
- 5.32.4 Wire List (CPI # AW 040-5521)

5.33 CPI Uniform Temperature Reference Plate (# 040-5522)

- 5.33.1 Parts List (CPI # AP 040-5522)
- 5.33.2 Assembly Dwg. (CPI # CA 040-5522)
- 5.33.3 Engineering Specification (CPI # AE 040-5522)
- 5.33.4 Wire List (CPI # AW 040-5522)
- 5.33.5 Technical Manual (CPI # 980-0070-052)

5.34 CPI Redundant Access Universal I/O Controller (# 070-5083)

5.34.1 Parts List (CPI # AP 070-5083)
5.34.2 Parts List (CPI # AP 069-5083)
5.34.3 Logic Dwg. (CPI # CL 070-5076)
5.34.4 Assembly Dwg. (CPI # CA 070-5083)
5.34.5 Assembly Dwg. (CPI # CA 069-5083)
5.34.6 Technical Manual (CPI # 980-0070-004)
5.34.7 Engineering Specification (CPI # AE NEQ070-5083)
5.34.8 Engineering Specification (CPI # AE 070-5076)
5.34.9 Test Procedure (CPI # AT 070-5076)

5.35 CPI Analog Barrier Terminal Strip Cable Assembly (# 075-0053)

5.35.1 Parts List (CPI # AP 075-0053)
5.35.2 Assembly Dwg. (CPI # CA 075-0053)
5.35.3 Engineering Specification (CPI # AE 075-0053)
5.35.4 Wire List (CPI # AW 075-0053)

5.36 CPI Digital Barrier Terminal Strip Cable Assembly (# 075-5227)

5.36.1 Parts List (CPI # AP 075-5227)
5.36.2 Assembly Dwg. (CPI # CA 075-5227)
5.36.3 Engineering Specification (CPI # AE 075-5227)
5.36.4 Wire List (CPI # AW 075-5227)
5.36.5 Technical Manual (CPI #980-0075-227)

5.37 CPI DALCAL Card Barrier Terminal Strip Cable Ass'y (# 075-5271)

5.37.1 Parts List (CPI # AP 075-5271)
5.37.2 Assembly Dwg. (CPI # CA 075-5271)
5.37.3 Engineering Specification (CPI # AE 075-5271)
5.37.4 Wire List (CPI # AW 075-5271)

5.38 CPI I/O Bus Cable (# 314-5043)

5.38.1 Parts List (CPI # AP 314-5043)
5.38.2 Assembly Dwg. (CPI # CA 314-5043)
5.38.3 Engineering Specification (CPI # AE 314-5043)

5.39 CPI Current Source Temperature Transducer (# 559-5002)

5.39.1 Parts List (CPI # AP 559-5002)
5.39.2 Assembly Dwg. (CPI # AA 559-5002)

5.40 CPI Universal I/O Controller (# 070-0004)

- 5.40.1 Parts List (CPI # AP 070-0004)
- 5.40.2 Parts List (CPI # AP 069-0004)
- 5.40.3 Logic Dwg. (CPI # CL 070-0004)
- 5.40.4 Assembly Dwg. (CPI # CA 070-0004)
- 5.40.5 Assembly Dwg. (CPI # CA 069-0004)
- 5.40.6 Technical Manual (CPI # 980-0070-004)
- 5.40.7 Engineering Specification (CPI # AE 070-0004)
- 5.40.8 Test Procedure (CPI # AT 070-0004)

5.41 CPI RTP Control Panel (# 070-0044)

- 5.41.1 Parts List (CPI # AP 070-0044)
- 5.41.2 Logic Dwg. (CPI # CL 070-0044)
- 5.41.3 Assembly Dwg. (CPI # CA 070-0044)
- 5.41.4 Technical Manual (CPI # 980-0070-044)
- 5.41.5 Engineering Specification (CPI # AE 070-0044)
- 5.41.6 Test Procedure (CPI # AT 070-0044)

5.42 CPI 12 V Power Supply, panel mounted (# 070-0008)

- 5.42.1 Parts List (CPI # AP 070-0008)
- 5.42.2 Assembly Dwg. (CPI # CA 070-0008)
- 5.42.3 Technical Manual (CPI # 980-0070-008)
- 5.42.4 Engineering Specification (CPI # AE 070-0008)
- 5.42.5 Test Procedure (CPI # AT 070-0008)

5.43 CPI Special Relay Out. Card w/ Contact Prot. (# 000-7066)

- 5.43.1 Parts List (CPI # AP 000-7066/7067)
- 5.43.2 Schematic (CPI # CS 000-7066/7067)
- 5.43.3 Assembly Dwg. (CPI # CA 000-7066/7067)
- 5.43.4 Technical Manual (CPI # 980-0021-232)
- 5.43.5 Engineering Specification (CPI # AE 021-5232)
- 5.43.6 Test Procedure (CPI # AT 021-5232)

5.44 CPI Spec. Pulsing Relay Out. Card w/ Contact Prot. (# 000-7067)

- 5.44.1 Parts List (CPI # AP 000-7066/7067)
- 5.44.2 Schematic (CPI # CS 000-7066/7067)
- 5.44.3 Assembly Dwg. (CPI # CA 000-7066/7067)
- 5.44.4 Technical Manual (CPI # 980-0021-232)
- 5.44.5 Engineering Specification (CPI # AE 021-5232)
- 5.44.6 Test Procedure (CPI # AT 021-5232)

5.45 CPI BTSCA (25 inch, 48 pin) to Test Cable/Connector Adapter (CPI # 000-7077)

5.45.1 Assembly Dwg. (CPI # AA 000-7077)
5.45.2 Wire List (CPI # AW 000-7077)

5.46 CPI Digital Input Surge Protection Test Connector (CPI # 000-7078)

5.46.1 Schematic (CPI # AS 000-7078)

5.47 CPI Pulse Counter Surge Protection Test Connector (CPI # 000-7097)

5.47.1 Schematic (CPI # AS 000-7097)

5.48 CPI Analog Input Unbalanced (1 Kohm) Test Termination/Connector (CPI # 000-7079)

5.48.1 Schematic (CPI # AS 000-7079)

5.49 CPI Digital Test Cable (CPI # 000-7080)

5.49.1 Schematic (CPI # AS 000-7080)

5.50 CPI Analog Input Test Divider/Connector for BTSCAs (CPI # 000-7081)

5.50.1 Schematic (CPI # AS 000-7081)

5.51 CPI Analog Input Parallel Input Test Connector (CPI # 000-7082)

5.51.1 Schematic (CPI # AS 000-7082)

5.52 CPI Analog Input Test Divider/Connector for UTRPs (CPI # 000-7085)

5.52.1 Schematic (CPI # AS 000-7085)

5.53 CPI RTD Resistor Terminations

5.53.1 Platinum 200 ohm, 32 : 350 F (CPI # 000-7086)

5.53.1.1 Information Dwg. (CPI # AH 000-7086)

5.53.2 Platinum 200 ohm, 32 : 850 F (CPI # 000-7087)

5.53.2.1 Information Dwg. (CPI # AH 000-7087)

5.53.3 Platinum 200 ohm, 32 : 110 F (CPI # 000-7088)

5.53.3.1 Information Dwg. (CPI # AH 000-7088)

5.53.4 Copper 10 ohm, -10 : 209 C (CPI # 000-7089)

5.53.4.1 Information Dwg. (CPI # AH 000-7089)

5.54 CPI Quality Assurance Procedure (CPI # AQ 8.02) - 'Calibration Control System'

5.55 CPI Quality Assurance Procedure (CPI # AQ 5.01) - 'Non-Conforming Material Control System'

5.56 CPI 'Description and Operating Instructions for the CPI Analog Input Test Computer and Analog Input Test Programs'

5.57 IEEE Standard # 472-1974 - 'Guide for Surge Withstand Capability (SWC) Testing'

5.58 Hewlett Packard Co. 'Operator's Manual for 3468A/B Multimeter'

5.59 Velonex 'Instruction Manual for Model 510 Surge Transient Generator'

5.60 Electronic Development Corp. 'Operator's Manual for Model 501 Programmable DC Voltage Standard'

5.61 Omega Engineering, Inc. 'Instruction Manual for Model 2166A Multipoint Digital Thermometer'

5.62 RFL Industries, Inc. 'Instruction Manual for Model 828 AC/DC V-A Source'

6. CONFIGURATION OF EQUIPMENT FOR TESTING

Specific or special configurations of the test equipment shall be as follows:

6.1 One RTP Control Panel (070-0044-001), with Device Address Select switches set for '111111', shall be labelled '#1'.

6.2 The test Universal I/O Controller (070-0004-003), with First Device Code set for '111111', shall contain :

6.2.1 a I/O Bus Termination module (021-0004) in slot 2;

6.2.2 a Special Relay Output Module (000-7066) with contact protection in slot 6; and

6.2.3 a Special Pulsing Relay Output Module (000-7067) with contact protection in slot 6.

6.3 One RTP I/O Bus Cable (314-0001-020) shall connect the Control Panel #1 (slot 5) to the test Universal I/O Controller (slot 1).

6.4 The output of the panel mounted 12 volt power supply shall be wired terminal block TB 1 of the test universal I/O controller to supply the 12 volts necessary to drive the relay output modules.

6.5 The other RTP Control Panel (070-0044-001) shall be labelled '#2';

6.6 One RTP I/O Bus Cable (314-0001-001) shall be connected to Control Panel #2 (slot 5) with the other end to be connected to the equipment in the cabinet under test.

6.7 The AC/DC V-A Source shall be configured to output 600 Volts AC RMS, 60 Hertz.

6.8 The Surge Transient Generator shall be configured as described in Appendix D.

6.9 Connect the I/O Bus Cable (314-0001-010) from Control Panel #2 to the 'first' I/O controller (slot 1 of standard Universal I/O Controllers (040-5462) or slot 4 of Redundant Access Universal I/O Controllers (070-5083)) in I/O daisy-chain of the cabinet set under test.

6.10 Set the first device code of the 'first' I/O controller in the cabinet set daisy-chain to '110000' (binary) (48 (decimal)) and the second device code of the first controller to '110001' (binary) (49 (decimal)). Set the devices codes of the successive controllers in the daisy-chain as follows:

DEVICE CODE

	FIRST		SECOND	
	(binary)	(decimal)	(binary)	(decimal)
second controller	'110010'	50	'110011'	51
third controller	'110100'	52	'110101'	53
fourth controller	'110110'	54	'110111'	55
fifth controller	'111000'	56	'111001'	57
sixth controller	'111010'	58	'111011'	59
seventh controller	'111100'	60	'111101'	61
eighth controller	'111110'	62	'111111'	63

6.11 Set the 'One Device Code/Two Device Code' switch on all I/O controllers to 'Two Device Codes'.

6.12 Install the Up/Down Pulse Counters Test Headers (000-7098) on any Up/Down Pulse Counters (038-5115) in the cabinet under test (-000 for counter #0 (DS2), -001 for counter #1 (DS1), -002 for counter #2 (DS3), and -003 for counter #3 (DS4)).

7. EQUIPMENT UNDER TEST CONFIGURATION VERIFICATION

Verify that the configuration of the equipment in the cabinet corresponds to the equipment cabinet configuration drawings of Attachment 2.

If a non-conformance is noted during the configuration verification, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the verification of the configuration will continue with the item found to be non-conforming.

EQUIPMENT UNDER TEST CONFIGURATION VERIFICATION

PERFORMED BY: _____ C.P.I.

APPROVED BY: _____ N.U.S.

APPROVED BY: _____ B.G.E.

8. AC POWER DISTRIBUTION/ INDICATOR PANEL AND POWER SUPPLY VALIDATION

The purpose of this test is to validate the operation of the the power supplies (040-5482, 040-5483, 040-5485, 040-5486, 040-5487, 040-5509); to validate the accuracy of the power supply to chassis cabling; to validate the functionality of the AC Power Distribution/ Indicator Panel (040-5511).

The validation of the AC Distribution/ Indicator Panel is accomplished by validating the presence of contact closures at the circuit breaker indictaor points with a multimeter, then applying AC power and validating the presence of AC voltage at the AC power distribution receptacles with a AC power receptacle tester and the closure of the relay contacts indicating the presence of the AC power with a multimeter. Then one of the circuit breakers is turned off and the presence or absence of AC voltage at the appropriate distribution receptacles will be validated. This is then repeated for the other circuit.

The validation of the power supplies is accomplished by measuring the voltages at the voltage inputs to the I/O controllers in the cabinet subsystem under test with a digital multimeter and validating that the measured voltage is within the specifications of the power supply plus a tolerance for voltage loss in the length of the power supply to chassis cabling.

(Note that in this section and other sections of the procedure, the individual power supplies of the redundant power supply assemblies are differentiated with the designations 'A' and 'B' which are not to be confused with unit subdivisions 'Channel A' and 'Channel B'.)

AC PWER DISTRIBUTION/ INDICATOR PANEL VALIDATION

8.1 Remove all AC power plugs from the distribution receptacles of the AC Power Distribution/ Indicator Panel.

8.2 Turn both circuit breakers (S1 and S2) ON.

8.3 Using the digital multimeter, validate the presence of contact closures (less than one ohm resistance) between the following points:

TB3-3 to TB3-4 (Circuit Breaker A)
TB3-8 to TB3-9 (Circuit Breaker B)

8.4 Using the digital multimeter, validate the absence of contact closures (more than one megaohm resistance) between the following points:

TB3-1 to TB3-2 (AC Monitor Relay A)
TB3-6 to TB3-7 (AC Monitor Relay B)

8.5 Plug power cord 'A' (connected to the AC Distribution/ Indicator Panel) into a source of AC power.

8.6 Using the digital multimeter, validate the presence of contact closures (less than one ohm resistance) between the following points:

TB3-1 to TB3-2 (AC Monitor Relay A)
TB3-3 to TB3-4 (Circuit Breaker A)
TB3-8 to TB3-9 (Circuit Breaker B)

8.7 Using the digital multimeter, validate the absence of contact closures (more than one megaohm resistance) between the following points:

TB3-6 to TB3-7 (AC Monitor Relay B)

8.8 Plug power cord 'B' (connected to the AC Distribution/ Indicator Panel) into a source of AC power.

8.9 Using the digital multimeter, validate the presence of contact closures (less than one ohm resistance) between the following points:

TB3-1 to TB3-2 (AC Monitor Relay A)
TB3-3 to TB3-4 (Circuit Breaker A)
TB3-6 to TB3-7 (AC Monitor Relay B)
TB3-8 to TB3-9 (Circuit Breaker B)

8.10 Plug power cord 'C' (connected to the AC Distribution/ Indicator Panel) into a source of AC power.

8.11 Using the AC power receptacle tester, validate that the AC power at all receptacles (J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, and J12) is ON (indicates 'CORRECT WIRING').

8.12 Turn the 'A' circuit breaker (S1) OFF. Validate that the AC power is ON or OFF (no lamps lighted on tester) at the receptacles per the following table:

J1	OFF	J2	OFF	J3	OFF	J4	OFF
J5	ON	J6	ON	J7	ON	J8	ON
J9	ON	J10	ON	J11	ON	J12	ON

8.13 Turn the 'A' circuit breaker (S1) ON and the 'B' circuit breaker (S2) OFF. Validate that the AC power is ON or OFF at the receptacles per the following table:

J1	ON	J2	ON	J3	ON	J4	ON
J5	ON	J6	ON	J7	ON	J8	ON
J9	OFF	J10	OFF	J11	OFF	J12	OFF

8.14 Turn both circuit breakers OFF. Validate that the AC power is ON or OFF at the receptacles per the following table:

J1	OFF	J2	OFF	J3	OFF	J4	OFF
J5	ON	J6	OFF	J7	OFF	J8	OFF
J9	OFF	J10	OFF	J11	OFF	J12	OFF

8.15 Install the AC power plugs into the AC Distribution/ Indicator Panel per Attachment 2.

8.16 Validate that the cabinet blower is operational.

8.17 Turn both circuit breakers ON.

AC DISTRIBUTION/ INDICATOR PANEL VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the validation of the AC Distribution/ Indicator Panel, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the AC Distribution/ Indicator Panel will be repeated (steps 8.2 to 8.17).

5 VOLT POWER SUPPLY VALIDATION

8.18 Using the digital multimeter, validate that the +5VDC at each of the I/O controllers (terminal block points 4 (ground) and 3 (+5 volts)) wired for 5 volts per Attachment 2 measures +(4.9 : 5.1) volts. Record the chassis ID number and voltage below:

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

5 VOLT POWER SUPPLY VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the validation of the 5 Volt Power Supply, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the 5 Volt Power Supply will be repeated (step 8.18).

+15 VOLT POWER SUPPLY VALIDATION

8.19 Using the digital multimeter, validate that the +15VDC at each of the I/O controllers (terminal block points 6 (ground) and 7 (+15 volts)) wired for +15 volts per Attachment 2 measures +(14.7 : 15.3) volts. Record the chassis ID number and voltage below:

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

+15 VOLT POWER SUPPLY VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the validation of the +15 Volt Power Supply, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the +15 Volt Power Supply will be repeated (step 8.19).

-15 VOLT POWER SUPPLY VALIDATION

8.20 Using the digital multimeter, validate that the -15VDC at each of the I/O controllers (terminal block points 8 (ground) and 9 (-15 volts)) wired for -15 volts per Attachment 2 measures -(14.7 : 15.3) volts. Record chassis ID number and voltage below:

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

CHASSIS ID NO.: _____ VOLTAGE: _____ INITIALS: ____/____

-15 VOLT POWER SUPPLY VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the validation of the -15 Volt Power Supply, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the -15 Volt Power Supply will be repeated (step 8.20).

125 VOLT POWER SUPPLY VALIDATION

8.21 Using the digital multimeter, validate that the 125VDC at the power supply assembly (040-5509) (terminal blocks TB 4 (+125 volts) points 1-8 and TB 5 (ground) points 1-8) measure +(112.5 : 137.5) volts. Record the voltage below:

TB4-1/TB5-1: VOLTAGE: _____ INITIALS: _____/_____

TB4-2/TB5-2: VOLTAGE: _____ INITIALS: _____/_____

TB4-3/TB5-3: VOLTAGE: _____ INITIALS: _____/_____

TB4-4/TB5-4: VOLTAGE: _____ INITIALS: _____/_____

TB4-5/TB5-5: VOLTAGE: _____ INITIALS: _____/_____

TB4-6/TB5-6: VOLTAGE: _____ INITIALS: _____/_____

TB4-7/TB5-7: VOLTAGE: _____ INITIALS: _____/_____

TB4-8/TB5-8: VOLTAGE: _____ INITIALS: _____/_____

125 VOLT POWER SUPPLY VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the validation of the 125 Volt Power Supply, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the 125 Volt Power Supply will be repeated (step 8.21).

9. OPTICALLY ISOLATED DIGITAL INPUT MODULE VALIDATION

The purpose of this test is to validate the operation of the Optically Isolated Digital Input modules (021-5230) and their associated signal conditioning circuits (038-5098) and to validate the accuracy of the input module to signal conditioning module cabling (040-5456) and the signal conditioning module to terminal strip cabling (040-5519).

This validation is accomplished by using a control panel to control a relay output module in a test I/O controller to simulate 'contacts' on the terminal strip which sources the input module. The simulated data is monitored by a second control panel connected to the I/O controllers in the cabinet under test. (Reference Figure 1 of Attachment 1)

9.1 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

9.2 Connect the 'Digital Test Cable' (000-7080) between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/Connector Adapter'.

9.3 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, and WAIT TEST UP

COMMAND WORD : to select random mode, disable interrupts, and to address the 'Special Relay Output Module' (address '0')

INSTRUCTION RATE : 50K range - vernier midrange

9.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Optically Isolated Digital Input Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, WAIT TEST and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50K range - vernier midrange

9.5 RESET both control panels.

9.6 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #1, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #1. Validate the operation of each bit.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

9.7 Repeat steps 9.1 to 9.6 for all Optically Isolated Digital Input Modules in the cabinet under test.

OPTICALLY ISOLATED DIGITAL INPUT VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the Optically Isolated Digital Input Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the O.I.D.I. will be repeated on the module/ cable set where the non-conformance was noted.

10. OPTICALLY ISOLATED DIGITAL INPUT MODULE SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate a sample of the surge withstand capability provided by the signal conditioning modules (038-5098) by simulating contacts on the input terminals to the digital input module under test, then applying a surge to the inputs while monitoring the data input from the module under test with a control panel to validate that no data changes during the application of the surge. Each bit of the module tested will then be revalidated for functionality as per Section 9. (Reference Figure 2 of Attachment 1)

10.1 Select a sample of up to five percent or at least one of the surge protected Optically Isolated Digital Input Modules (021-5230 / 038-5098) in the cabinet under test to have the surge withstand capability tested.

10.2 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

10.3 Connect the 'Digital Input Surge Test Connector' (000-7078) to the 'BTSCA to Test Cable/Connector Adapter'. Connect the red lead of the surge transient generator cable to the test connector. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.

10.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Optically Isolated Digital Input Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, WAIT TEST and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50K range - vernier midrange

10.5 RESET Control Panel #2.

10.6 Ready the surge transient generator to output a surge per Appendix D.

10.7 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

10.8 Repeat steps 10.2 to 10.7 on all of the Optically Isolated Digital Input modules in the selected sample.

10.9 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

10.10 Connect the 'Digital Test Cable' (000-7080) between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/Connector Adapter'.

10.11 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Optically Isolated Digital Input Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, WAIT TEST and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50K range - vernier midrange

10.12 RESET both control panels.

10.13 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #1, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #1. Validate the operation of each bit.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

10.14 Repeat steps 10.9 to 10.13 for each of the Optically Isolated Digital Input Modules selected for surge withstand capability testing.

OPTICALLY ISOLATED DIGITAL INPUT SURGE WITHSTAND CAPABILITY VALIDATION

PERFORMED BY: _____ C.P.I.

APPROVED BY: _____ N.U.S.

APPROVED BY: _____ B.G.E.

If a non-conformance is noted during the Optically Isolated Digital Input Surge Withstand Capability Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Optically Isolated Digital Input Surge Withstand Capability will be repeated on the module/ cabling set where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one, of the Optically Isolated Digital Inputs with surge protection will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

11. CHANGE OF STATE DIGITAL INPUT VALIDATION

The purpose of this test is to validate the operation of the Change of State Digital Input modules (038-5064) and their associated signal conditioning circuits (038-5099) and to validate the accuracy of the input module to signal conditioning module cabling (040-5456) and the signal conditioning module to terminal strip cabling (040-5519).

This validation is accomplished by using a control panel to control a relay output module in a test I/O controller to simulate 'contacts' on the terminal strip which sources the input module. The simulated data is monitored by a second control panel connected to the I/O controllers in the cabinet under test. (Reference Figure 3 of Attachment 1)

11.1 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

11.2 Connect the 'Digital Test Cable' (000-7080) between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/Connector Adapter'.

11.3 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, and WAIT TEST UP

COMMAND WORD : to select random mode, disable interrupts, and to address the 'Special Relay Output Module' (address '0')

INSTRUCTION RATE : 50K range - vernier midrange

11.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Change of State Digital Input Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, INT QRY, and IN UP, WAIT INT DOWN

COMMAND WORD : to select random mode, enable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50 range - vernier midrange

11.5 RESET both control panels.

11.6 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #1, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #1. Validate that the interrupt request display of Control Panel #2 flashes ON then OFF when a bit is toggled. Validate that the interrupt vector displayed corresponds to the controller first device address and the module slot address. Validate the operation of each bit.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

11.7 Repeat steps 11.1 to 11.6 for all Change of State Digital Input modules in the cabinet under test.

CHANGE OF STATE DIGITAL INPUT VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the Change of State Digital Input Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the C.O.S.D.I. will be repeated on the module/ cabling set where the non-conformance was noted.

12. CHANGE OF STATE DIGITAL INPUT MODULE SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate a sample of the surge withstand capability provided by the signal conditioning modules (038-5099) by simulating contacts on input terminals to the digital input module under test, then applying a surge to the inputs while monitoring the data input from the module under test with a control panel to validate that no data shall change during the application of the surge. Each bit of the module tested will then be revalidated for functionality as per Section 11. (Reference Figure 4 of Attachment 1)

12.1 Select a sample of up to five percent or at least one of the surge protected Change of State Digital Input modules (038-5064 / 038-5099) in the cabinet under test to have the surge withstand capability tested.

12.2 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

12.3 Connect the 'Digital Input Surge Test Connector' (000-7078) to the 'BTSCA to Test Cable/Connector Adapter'. Connect the red lead of the surge transient generator cable to the test connector. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.

12.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Change of State Digital Input Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, INT QRY, and IN UP, WAIT INT DOWN

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50K range - vernier midrange

12.5 RESET Control Panel #2.

12.6 Ready the surge transient generator to output a surge per Appendix D.

12.7 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

12.8 Repeat steps 12.2 to 12.7 on all of the Change Of State Digital Input modules in the selected sample.

12.9 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

12.10 Connect the 'Digital Test Cable' (000-7080) between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/Connector Adapter'.

12.11 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Change of State Digital Input Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, INT QRY, and IN UP, WAIT INT DOWN

COMMAND WORD : to select random mode, enable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50 range - vernier midrange

12.12 RESET both control panels.

12.13 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #1, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #1. Validate that the interrupt request display of Control Panel #2 flashes on then off when a bit is toggled. Validate that the interrupt vector displayed corresponds to the controller first device address and the module slot address. Validate the operation of each bit.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

12.14 Repeat steps 12.9 to 12.13 on the Change of State Digital Input modules selected for surge withstand capability testing.

CHANGE OF STATE DIGITAL INPUT SURGE WITHSTAND CAPABILITY VALIDATION

PERFORMED BY: _____ C.P.I.

APPROVED BY: _____ N.U.S.

APPROVED BY: _____ B.G.E.

If a non-conformance is noted during the Change of State Digital Input Surge Withstand Capability Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Change of State Digital Input Surge Withstand Capability will be repeated on the module/ cabling set where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one, of the Change of State Digital Input with surge protection will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

13. QUAD PULSE COUNTER MODULE VALIDATION

The purpose of this test is to validate that the Quad Pulse Counter modules (021-5278) and their associated signal conditioning circuits (038-5099) are operational and to validate the accuracy of the counter module to signal conditioning module cabling (040-5517) and the signal conditioning module to terminal strip cabling (040-5519).

This is accomplished by using a control panel to control a relay output module in a test I/O controller to simulate 'contacts' pulses on the terminal strip which sources the input module. The simulated data is monitored by a second control panel connected to the I/O controllers in the cabinet under test. (Reference Figure 5 of Attachment 1)

13.1 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

13.2 Connect the 'Digital Test Cable' (000-7080) between the 'Special Pulsing Relay Output Module' (000-7067) in the test I/O controller (slot 7) and the 'BTSCA to Test Cable/ Connector Adapter'.

13.3 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the 'Special Pulsing Relay Output Module' (address '1')

INSTRUCTION RATE : 50 range - vernier midrange

OUTPUT WORD : '0000 0000 0000 0000'

13.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Quad Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

13.5 RESET both control panels.

13.6 Initialize the four counters of the module under test to zero counts from the Output Word of Control Panel #2. Set the Output Word to all zeros.

13.7 Validate that counter #0 (Data Word Display of Control Panel #2) indicates a count of zero (all LEDs OFF).

13.8 Select counter #1 from Control Panel #2 Output Word and validate that counter #1 indicates a count of zero.

13.9 Select counter #2 and validate that counter #2 indicates a count of zero.

13.10 Select counter #3 and validate that counter #3 indicates a count of zero.

13.11 Select counter #0 from Control Panel #2 Output Word.

13.12 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #0 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.

13.13 Validate that the Data Word Display of Control Panel #2 increments. Using the Output Word of Control Panel #2, select counters #1,#2, and #3 and validate that these counters are not incrementing.

13.14 Reset the bit set in the Output Word of Control Panel #1.

13.15 Select counter #1.

13.16 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #1 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.

13.17 Validate that counter #1 increments. Validate that counters #0, #2, and #3 do not increment.

13.18 Reset the bit set in the Output Word of Control Panel #1.

13.19 Select counter #2.

13.20 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #2 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.

13.21 Validate that counter #2 increments. Validate that counters #0, #1, and #3 do not increment.

13.22 Reset the bit set in the Output Word of Control Panel #1.

13.23 Select counter #3.

13.24 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #3 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.

13.25 Validate that counter #3 increments. Validate that counters #0, #1, and #2 do not increment.

13.26 Reset the bit set in the Output Word of Control Panel #1.

HOOD of 040-5517 PI/SCM CABLE on MODULE UNDER TEST	COUNTER NUMBER #0	#1	#2	#3
HOOD P1	0	1	2	3
HOOD P2	4	5	6	7
HOOD P3	8	9	10	11
HOOD P4	12	13	14	15

Output Word bit set on Control Panel #1 to control pulsing relay

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

13.27 Repeat steps 13.1 to 13.26 for all Quad Pulse Counter modules in the cabinet under test.

QUAD PULSE COUNTER MODULE VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the Quad Pulse Counter Module Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Quad Pulse Counters will be repeated on the module/ cabling set where the non-conformance was noted.

14. QUAD PULSE COUNTER MODULE SURGE WITHSTAND CAPABILITY VAL

The purpose of this test is to validate a sample of the surge withs capability provided by the signal conditioning modules (038-5099) by applying a surge to the terminals that source the input module while monitoring the data input from the module under test with a control panel to validate that the data shall not change during the application of the surge. The module tested will then be revalidated for functionality as per Section 13. (Reference Figure 6 of Attachment 1)

14.1 Select a sample of up to five percent or at least one of the surge protected Quad Pulse Counter Modules (021-5278 / 038-5099) in the cabinet to have the surge withstand capability tested.

14.2 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

14.3 Connect the 'Pulse Counter Surge Test Connector' (000-7097) to the 'BTSCA to Test Cable/Connector Adapter'. Connect the red lead of the surge transient generator cable to the point on the test connector marked with the number on the hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) installed on the module to be tested. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.

14.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Quad Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

14.5 RESET Control Panel #2.

14.6 Initialize the four counters of the module under test to zero counts from the Output Word of Control Panel #2. Validate that counters #0, #1, #2, and #3 all indicate counts of zero.

14.7 Ready the surge transient generator to output a surge per Appendix D.

14.8 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.

14.9 Validate that counters #0, #1, #2, and #3 all indicate counts of zero.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

14.10 Repeat steps 14.2 to 14.9 on all of the Quad Pulse Counter modules in the selected sample.

14.11 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

14.12 Connect the 'Digital Test Cable' (000-7080) between the 'Special Pulsing Relay Output Module' (000-7067) in the test I/O controller (slot 7) and the 'BTSCA to Test Cable/Connector Adapter'.

14.13 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Quad Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

14.14 RESET both control panels.

14.15 Select counter #0 from Control Panel #2 Output Word.

14.16 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #0 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.

14.17 Validate that the Data Word Display of Control Panel #2 increments.

14.18 Reset the bit set in the Output Word of Control Panel #1.

14.19 Select counter #1.

14.20 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #1 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.

14.21 Validate that counter #1 increments.

14.22 Reset the bit set in the Output Word of Control Panel #1.

14.23 Select counter #2.

14.24 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #2 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.

14.25 Validate that counter #2 increments.

14.26 Reset the bit set in the Output Word of Control Panel #1.

14.27 Select counter #3.

14.28 Set the appropriate bit (in the Output Word of Control Panel #1) from the table below corresponding to counter #3 and which hood of the Quad Pulse Counter to S.C.M. Cable (040-5517) is connected to the module under test.

14.29 Validate that counter #3 increments.

14.30 Reset the bit set in the Output Word of Control Panel #1.

HOOD of 040-5517 PI/SCM CABLE on MODULE UNDER TEST	COUNTER NUMBER #0	#1	#2	#3
HOOD P1	0	1	2	3
HOOD P2	4	5	6	7
HOOD P3	8	9	10	11
HOOD P4	12	13	14	15

Output Word bit set on Control Panel #1 to control pulsing relay

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

14.31 Repeat steps 14.11 to 14.30 on the Quad Pulse Counter modules selected for surge withstand capability testing.

QUAD PULSE COUNTER SURGE WITHSTAND CAPABILITY VALIDATION

PERFORMED BY: _____ C.P.I.

APPROVED BY: _____ N.U.S.

APPROVED BY: _____ B.G.E.

If a non-conformance is noted during the Quad Pulse Counter Surge Withstand Capability Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Quad Pulse Counter Surge Withstand Capability will be repeated on the module/ cabling set where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one, of the Quad Pulse Counters with surge protection will be selected and tested. This will be repeated if an another non-conformance is identified in the second sample.

15. UP/DOWN PULSE COUNTER MODULE VALIDATION

The purpose of this test is to validate that the Up/Down Pulse Counter Modules (038-5115) and their associated signal conditioning circuits (038-5099) are operational and to validate the accuracy of the counter module to signal conditioning module cabling (040-5456 or 040-5518) and the signal conditioning module to terminal strip cabling (040-5519).

This is accomplished by using a control panel to control a relay output module in a test I/O controller to simulate 'contact' pulses on the terminal strip which sources the counter module. The simulated data is monitored by a second control panel connected to the I/O controllers in the cabinet under test. (Reference Figure 7 of Attachment 1)

Note that the 'Channel A' Up/Down Pulse Counters are configured differnetly than the 'Channel B' Up/Down Pulse Counters. The 'Channel B' counters have their 16 inputs conditioned/ sourced by one signal conditioning module/ terminal strip. The 'Channel A' counters have their 16 inputs conditioned/ sourced by two signal conditioning modules/ terminal strips (the UP, DOWN, and SET inputs by one SCM/TS, and the RESET inputs by another SCM/TS).

Also note that the counters can be set to a count determined by a customer selected configuration of diodes on the module. The modules are normally factory configured for a count of zero. This creates a problem in testing in that the SET input yields the same count as the RESET input. For the purpose of this acceptance test, the modules are configured to give counts of 119 (decimal) ('01110111' binary), 187 (decimal) ('10111011' binary), 221 (decimal) ('11011101' binary), and 238 (decimal) ('11101110' binary) for counters #0, #1, #2, and #3 respectively on a SET input. Prior to shipment, the normal factory configured diodes will be installed on the modules.

15.1 Install the 'BTSCA to Test Cable/ Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2 for 'Channel B' counters or on each of the selected BTSCAs for the 'Channel A' counters.

15.2 Connect the 'Digital Test Cable' (000-7080) between the 'Special Pulsing Relay Output Module' (000-7067) in the test I/O controller (slot 7) and the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA for 'Channsl B' counters or on the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the UP, DOWN, and SET inputs to the 'Channel A' counters. For 'Channel A' counters, connect a second 'Digital Test Cable' between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the RESET inputs to the 'Channel A' counters.

15.3 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the 'Special Pulsing Relay Output Module' (address '1')

INSTRUCTION RATE : 50 range - vernier midrange

OUTPUT WORD : '0000 0000 0000 0000'

15.4 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Up/Down Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

15.5 RESET both control panels.

15.6 Set the counter #0 of the module under test to a count of '10000000' (binary) from the Output Word of Control Panel #2.

15.7 Validate that counter #0 indicates a count of '10000000' in the Data Word Display of Control Panel #2.

15.8 Set counter #1 to a count of '10000000' .

15.9 Validate that counter #1 indicates a count of '10000000' .

15.10 Set counter #2 to a count of '10000000' .

15.11 Validate that counter #2 indicates a count of '10000000' .

15.12 Set counter #3 to a count of '10000000' .

15.13 Validate that counter #3 indicates a count of '10000000' .

For 'Channel A' Up/Down Pulse Counters, proceed with steps 15.14 to 15.31, then continue with step 15.48 .

For 'Channel B' Up/Down Pulse Counters, proceed with steps 15.32 to 15.47, then continue with step 15.48 .

'CHANNEL A' COUNTERS ONLY (15.14 to 15.31)

15.14 Set the COMMAND WORD of Control Panel #1 to address the 'Special Relay Output Module' (address '0').

15.15 Select counter #0 from Control Panel #2 Output Word.

15.16 Set bit 0, 4, 8, or 12, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #0.

15.17 Reset the bit set in the Output Word of Control Panel #1.

15.18 Validate that counter #0 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

15.19 Select counter #1 from Control Panel #2 Output Word.

15.20 Set bit 1, 5, 9, or 13, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #1.

15.21 Reset the bit set in the Output Word of Control Panel #1.

15.22 Validate that counter #1 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

15.23 Select counter #2 from Control Panel #2 Output Word.

15.24 Set bit 2, 6, 10, or 14, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #2.

15.25 Reset the bit set in the Output Word of Control Panel #1.

15.26 Validate that counter #2 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

15.27 Select counter #3 from Control Panel #2 Output Word.

15.28 Set bit 3, 7, 11, or 15, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #3.

15.29 Reset the bit set in the Output Word of Control Panel #1.

15.30 Validate that counter #3 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

15.31 Set the COMMAND WORD of Control Panel #1 to address the 'Special Pulsing Relay Output Module' (address '1').

POSITION OF MODULE ON 040-5518 CABLE	COUNTER # 0	1	2	3
FIRST CARD	0	1	2	3
SECOND CARD	4	5	6	7
THIRD CARD	8	9	10	11
FOURTH CARD	12	13	14	15

Output Word bit set on Control Panel #1 to control pulsing relay on RESET inputs of Channel A counters

'CHANNEL B' COUNTERS ONLY (15.32 to 15.47)

15.32 Select counter #0 from Control Panel #2 Output Word.

15.33 Set bit 2 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #0.

15.34 Reset the bit set in the Output Word of Control Panel #1.

15.35 Validate that counter #0 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

15.36 Select counter #1 from Control Panel #2 Output Word.

15.37 Set bit 6 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #1.

15.38 Reset the bit set in the Output Word of Control Panel #1.

15.39 Validate that counter #1 indicates a count of '00000000' .

15.40 Select counter #2 from Control Panel #2 Output Word.

15.41 Set bit 10 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #2.

15.42 Reset the bit set in the Output Word of Control Panel #1.

15.43 Validate that counter #2 indicates a count of '00000000' .

15.44 Select counter #3 from Control Panel #2 Output Word.

15.45 Set bit 14 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #3.

15.46 Reset the bit set in the Output Word of Control Panel #1.

15.47 Validate that counter #3 indicates a count of '00000000' .

'CHANNEL A' and 'CHANNEL B' COUNTERS

15.48 Select counter #0 from Control Panel #2 Output Word.

15.49 Set bit 3 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #0.

15.50 Reset the bit set in the Output Word of Control Panel #1.

15.51 Validate that counter #0 indicates a count of '01110111' in the Data Word Display of Control Panel #2.

15.52 Select counter #1 from Control Panel #2 Output Word.

15.53 Set bit 7 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #1.

15.54 Reset the bit set in the Output Word of Control Panel #1.

15.55 Validate that counter #1 indicates a count of '10111011' .

15.56 Select counter #2 from Control Panel #2 Output Word.

15.57 Set bit 11 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #2.

15.58 Reset the bit set in the Output Word of Control Panel #1.

15.59 Validate that counter #2 indicates a count of '11011101' .

15.60 Select counter #3 from Control Panel #2 Output Word.

15.61 Set bit 15 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #3.

15.62 Reset the bit set in the Output Word of Control Panel #1.

15.63 Validate that counter #3 indicates a count of '11101110' .

15.64 Select counter #0 from Control Panel #2 Output Word.

15.65 Set bit 0 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #0.

15.66 Validate that counter #0 (the Data Word Display of Control Panel #2) increments.

15.67 Reset the bit set in the Output Word of Control Panel #1.

15.68 Set bit 1 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #0.

15.69 Validate that counter #0 (the Data Word Display of Control Panel #2) decrements.

15.70 Reset the bit set in the Output Word of Control Panel #1.

15.71 Select counter #1 from Control Panel #2 Output Word.

15.72 Set bit 4 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #1.

15.73 Validate that counter #1 (the Data Word Display of Control Panel #2) increments.

15.74 Reset the bit set in the Output Word of Control Panel #1.

15.75 Set bit 5 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #1.

15.76 Validate that counter #1 (the Data Word Display of Control Panel #2) decrements.

15.77 Reset the bit set in the Output Word of Control Panel #1.

15.78 Select counter #2 from Control Panel #2 Output Word.

15.79 Set bit 8 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #2.

15.80 Validate that counter #2 (the Data Word Display of Control Panel #2) increments.

15.81 Reset the bit set in the Output Word of Control Panel #1.

15.82 Set bit 9 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #2.

15.83 Validate that counter #2 (the Data Word Display of Control Panel #2) decrements.

15.84 Reset the bit set in the Output Word of Control Panel #1.

15.85 Select counter #3 from Control Panel #2 Output Word.

15.86 Set bit 12 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #3.

15.87 Validate that counter #3 (the Data Word Display of Control Panel #2) increments.

15.88 Reset the bit set in the Output Word of Control Panel #1.

15.89 Set bit 13 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #3.

15.90 Validate that counter #3 (the Data Word Display of Control Panel #2) decrements.

15.91 Reset the bit set in the Output Word of Control Panel #1.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/

15.92 Repeat steps 15.1 to 15.91 for all Up/Down Counter modules in the cabinet.

UP/DOWN PULSE COUNTER MODULE VALIDATION

PERFORMED BY: ______________________________ C.P.I.

WITNESSED BY: ______________________________ N.U.S.

If a non-conformance is noted during the Up/Down Pulse Counter Module Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Up/Down Pulse Counters will be repeated on the module/ cabling set where the non-conformance was noted.

16. UP/DOWN PULSE COUNTER MODULE SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate a sample of the surge withstand capability provided by the signal conditioning modules (038-5099) by applying a surge to the Up/Down Pulse Counter terminals that source the input modules while monitoring the data input from the module under test with a control panel to validate that the data shall not change during the application of the surge. The module tested will then be revalidated for functionality as per Section 15. (Reference Figure 8 of Attachment 1)

16.1 Select a sample of up to five percent or at least one of the surge protected Up/Down Counter modules (038-5115 / 038-5099) in the cabinet to have the surge withstand capability tested.

16.2 Install the 'BTSCA to Test Cable/Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2 for 'Channel B' counters or on each of the selected BTSCAs for the 'Channel A' counters.

16.3 Connect the 'Digital Input Surge Test Connector' (000-7078) to the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA for 'Channel B' counters or on the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the UP, DOWN, and SET inputs to the 'Channel A' counters. For 'Channel A' counters, connect the 'Pulse Counter Surge Test Connector' (000-7097) to the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the RESET inputs to the 'Channel A' counters.

16.4 Connect the red lead of the surge transient generator cable to the 'Digital Input Surge Test Connector' on the BTSCA for 'Channel B' counters or on the BTSCA which sources the UP, DOWN, and SET inputs to the 'Channel A' counters. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.

16.5 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Up/Down Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

16.6 RESET Control Panel #2.

16.7 Set counter #0 of the module under test to a count of '10000000' (binary) from the Output Word of Control Panel #2.

16.8 Validate that counter #0 indicates a count of '10000000' in the Data Word Display of Control Panel #2.

16.9 Set counter #1 to a count of '10000000' .

16.10 Validate that counter #1 indicates a count of '10000000' .

16.11 Set counter #2 to a count of '10000000' .

16.12 Validate that counter #2 indicates a count of '10000000' .

16.13 Set counter #3 to a count of '10000000' .

16.14 Validate that counter #3 indicates a count of '10000000' .

16.15 Select counter #0.

16.16 Ready the surge transient generator to output a surge per Appendix D.

16.17 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.

16.18 Validate that counter #0 indicates a count of '10000000' in the Data Word Display of Control Panel #2.

16.19 Validate that counter #1 indicates a count of '10000000' .

16.20 Validate that counter #2 indicates a count of '10000000' .

16.21 Validate that counter #3 indicates a count of '10000000' .

PERFORM STEPS 16.22 TO 16.28 for 'CHANNEL A' COUNTERS ONLY

16.22 Connect the red lead of the surge transient generator cable to the 'Pulse Counter Surge Test Connector' on the BTSCA which sources the RESET inputs to the 'Channel A' counters. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.

16.23 Ready the surge transient generator to output a surge per Appendix D.

16.24 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds and validate that no bit in the Data Word Display of Control Panel #2 changes state during or after the application of the surge voltage.

16.25 Validate that counter #0 indicates a count of '10000000' in the Data Word Display of Control Panel #2.

16.26 Validate that counter #1 indicates a count of '10000000' .

16.27 Validate that counter #2 indicates a count of '10000000' .

16.28 Validate that counter #3 indicates a count of '10000000' .

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

16.29 Repeat steps 16.2 to 16.28 (as applicable) on all of the Up/Down Pulse Counter modules in the sample selected.

16.30 Install the 'BTSCA to Test Cable/ Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2 for 'Channel B' counters or on each of the selected BTSCAs for the 'Channel A' counters.

16.31 Connect the 'Digital Test Cable' (000-7080) between the 'Special Pulsing Relay Output Module' (000-7067) in the test I/O controller (slot 7) and the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA for 'Channel B' counters or on the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the UP, DOWN, and SET inputs to the 'Channel A' counters. For 'Channel A' counters, connect a second 'Digital Test Cable' between the 'Special Relay Output Module' (000-7066) in the test I/O controller (slot 6) and the 'BTSCA to Test Cable/ Connector Adapter' on the selected BTSCA which sources the RESET inputs to the 'Channel A' counters.

16.32 Configure Control Panel #1 as follows:

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts. and to address the 'Special Pulsing Relay Output Module' (address '1')

INSTRUCTION RATE : 50 range - vernier midrange

OUTPUT WORD : '0000 0000 0000 0000'

16.33 Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O Controller containing the Up/Down Pulse Counter Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

16.34 RESET both control panels.

16.35 Set the counter #0 or the module under test to a count of '10000000' (binary) from the Output Word of Control Panel #2.

16.36 Validate that counter #0 indicates a count of '10000000' in the Data Word Display of Control Panel #2.

16.37 Set counter #1 to a count of '10000000' .

16.38 Validate that counter #1 (Data Word Display of Control Panel #2) indicates a count of '10000000' .

16.39 Set counter #2 to a count of '10000000' .

16.40 Validate that counter #2 (Data Word Display of Control Panel #2) indicates a count of '10000000' .

16.41 Set counter #3 to a count of '10000000' .

16.42 Validate that counter #3 (Data Word Display of Control Panel #2) indicates a count of '10000000' .

For 'Channel A' Up/Down Pulse Counters, proceed with steps 16.43 to 16.60, then continue with step 16.77 .

For 'Channel B' Up/Down Pulse Counters, proceed with steps 16.61 to 16.76, then continue with step 16.77 .

'CHANNEL A' COUNTERS ONLY (16.43 to 16.60)

16.43 Set the COMMAND WORD of Control Panel #1 to address the 'Special Relay Output Module' (address '0').

16.44 Select counter #0 from Control Panel #2 Output Word.

16.45 Set bit 0, 4, 8, or 12, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #0.

16.46 Reset the bit set in the Output Word of Control Panel #1.

16.47 Validate that counter #0 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

16.48 Select counter #1 from Control Panel #2 Output Word.

16.49 Set bit 1, 5, 9, or 13, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #1.

16.50 Reset the bit set in the Output Word of Control Panel #1.

16.51 Validate that counter #1 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

16.52 Select counter #2 from Control Panel #2 Output Word.

16.53 Set bit 2, 6, 10, or 14, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #2.

16.54 Reset the bit set in the Output Word of Control Panel #1.

16.55 Validate that counter #2 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

16.56 Select counter #3 from Control Panel #2 Output Word.

16.57 Set bit 3, 7, 11, or 15, per the table below depending on the position of the card under test on the counter to SCM cable (040-5518), in the Output Word of Control Panel #1 to cause a relay on the Special Relay Output Card to 'make contact' on the RESET input to counter #3.

16.58 Reset the bit set in the Output Word of Control Panel #1.

16.59 Validate that counter #3 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

16.60 Set the COMMAND WORD of Control Panel #1 to address the 'Special Pulsing Relay Output Module' (address '1').

POSITION OF MODULE ON 040-5518 CABLE	COUNTER # 0	1	2	3
FIRST CARD	0	1	2	3
SECOND CARD	4	5	6	7
THIRD CARD	8	9	10	11
FOURTH CARD	12	13	14	15

Output Word bit set on Control Panel #1 to control pulsing relay on RESET inputs of Channel A counters

'CHANNEL B' COUNTERS ONLY (16.61 to 16.76)

16.61 Select counter #0 from Control Panel #2 Output Word.

16.62 Set bit 2 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #0.

16.63 Reset the bit set in the Output Word of Control Panel #1.

16.64 Validate that counter #0 indicates a count of '00000000' in the Data Word Display of Control Panel #2.

16.65 Select counter #1 from Control Panel #2 Output Word.

16.66 Set bit 6 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #1.

16.67 Reset the bit set in the Output Word of Control Panel #1.

16.68 Validate that counter #1 (Data Word Display of Control Panel #2) indicates a count of '00000000' .

16.69 Select counter #2 from Control Panel #2 Output Word.

16.70 Set bit 10 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #2.

16.71 Reset the bit set in the Output Word of Control Panel #1.

16.72 Validate that counter #2 (Data Word Display of Control Panel #2) indicates a count of '00000000' .

16.73 Select counter #3 from Control Panel #2 Output Word.

16.74 Set bit 14 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the RESET input to counter #3.

16.75 Reset the bit set in the Output Word of Control Panel #1.

16.76 Validate that counter #3 (Data Word Display of Control Panel #2) indicates a count of '00000000' .

'CHANNEL A' and 'CHANNEL B' COUNTERS

16.77 Select counter #C from Control Panel #2 Output Word.

16.78 Set bit 3 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #0.

16.79 Reset the bit set in the Output Word of Control Panel #1.

16.80 Validate that counter #0 indicates a count of '01110111' in the Data Word Display of Control Panel #2.

16.81 Select counter #1 from Control Panel #2 Output Word.

16.82 Set bit 7 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #1.

16.83 Reset the bit set in the Output Word of Control Panel #1.

16.84 Validate that counter #1 (Data Word Display of Control Panel #2) indicates a count of '10111011' .

16.85 Select counter #2 from Control Panel #2 Output Word.

16.86 Set bit 11 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #2.

16.87 Reset the bit set in the Output Word of Control Panel #1.

16.88 Validate that counter #2 (Data Word Display of Control Panel #2) indicates a count of '11011101' .

16.89 Select counter #3 from Control Panel #2 Output Word.

16.90 Set bit 15 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the SET input to counter #3.

16.91 Reset tne bit set in the Output Word of Control Panel #1.

16.92 Validate that counter #3 (Data Word Display of Control Panel #2) indicates a count of '11101110' .

16.93 Select counter #0 from Control Panel #2 Output Word.

16.94 Set bit 0 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #0.

16.95 Validate that counter #0 (Data Word Display of Control Panel #2) increments.

16.96 Reset the bit set in the Output Word of Control Panel #1.

16.97 Set bit 1 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #0.

16.98 Validate that counter #0 (Data Word Display of Control Panel #2) decrements.

16.99 Reset the bit set in the Output Word of Control Panel #1.

16.100 Select counter #1 from Control Panel #2 Output Word.

16.101 Set bit 4 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #1.

16.102 Validate that counter #1 (Data Word Display of Control Panel #2) increments.

16.103 Reset the bit set in the Output Word of Control Panel #1.

16.104 Set bit 5 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #1.

16.105 Validate that counter #1 (Data Word Display of Control Panel #2) decrements.

16.106 Reset the bit set in the Output Word of Control Panel #1.

16.107 Select counter #2 from Control Panel #2 Output Word.

16.108 Set bit 8 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #2.

16.109 Validate that counter #2 (Data Word Display of Control Panel #2) increments.

16.110 Reset the bit set in the Output Word of Control Panel #1.

16.111 Set bit 9 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #2.

16.112 Validate that counter #2 (Data Word Display of Control Panel #2) decrements.

16.113 Reset the bit set in the Output Word of Control Panel #1.

16.114 Select counter #3 from Control Panel #2 Output Word.

16.115 Set bit 12 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the UP input to counter #3.

16.116 Validate that counter #3 (Data Word Display of Control Panel #2) increments.

16.117 Reset the bit set in the Output Word of Control Panel #1.

16.118 Set bit 13 in the Output Word of Control Panel #1 to cause a relay on the Special Pulsing Relay Output Card to start 'pulsing' on the DOWN input to counter #3.

16.119 Validate that counter #3 (Data Word Display of Control Panel #2) decrements.

16.120 Reset the bit set in the Output Word of Control Panel #1.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

16.121 Repeat steps 16.30 to 16.120 on the remaining Up/Down Pulse Counters selected for surge withstand capability testing.

UP/DOWN PULSE COUNTER MODULE SURGE WITHSTAND CAPABILITY VALIDATION

PERFORMED BY: _____ C.P.I.

APPROVED BY: _____ N.U.S.

APPROVED BY: _____ B.G.E.

If a non-conformance is noted during the Up/Down Pulse Counter Surge Withstand Capability Validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the Up/Down Pulse Counter Surge Withstand Capability will be repeated on the module/ cabling set where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one, of the Up/Down Pulse Counters with surge protection will be selected and tested. This will be repeated if an another non-conformance is identified in the second sample.

17. DIGITAL and ANALOG LOOPBACK and CALIBRATION MODULE VALIDATION

The purpose of this test is to validate the operation of the different functional blocks of the Digital and Analog Loopback and Calibration modules (021-5271) where applicable; to validate the accuracy of the DALCAL module to terminal strip cabling (075-5271) where applicable; and to validate the functionality of the temperature transducer (559-5002) within the cabinet where applicable.

The Universal Analog to Digital Converter module (021-0211) is also validated when configured in a controller containing a DALCAL module.

The digital loopback functional block validation is accomplished by using a control panel to output data to the module under test and validating that the data input from the module echos the data output.

The analog loopback/ calibration functional block validation is accomplished by using a test computer system (see the CPI Description and Operating Instructions for the CPI Analog Input Test Computer and Programs) to run a test program to acquire analog data from the DALCAL / Universal A/D Converter module pair under test and validate the data acquired per data derived from the specifications of the Universal A/D Converter module (AE 021-0211) and the DALCAL module (AE 021-5271).

The temperature transducer monitoring functional block is validation is accomplished by using the test computer system to run the test program to acquire analog data from the DALCAL / Universal A/D Converter module pair sensing the output of the temperature transducer. The test program displays the raw analog data and also converts the data to the corresponding temperature. The temperature measured is compared to the temperature measured by a digital thermometer and the data is validated per data derived from the specifications of the Universal A/D Converter module, the DALCAL module, the temperature transducer, and the test digital thermometer.

DALCAL MODULE DIGITAL LOOPBACK VALIDATION

17.1 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O controller containing the DALCAL Module under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, OUT, WAIT TEST, and IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 5K range - vernier midrange

17.2 Starting with an Output Word of '0000 0000 0000 0000' from Control Panel #2, validate that the Data Word Display of Control Panel #2 matches the Output Word Select switches of Control Panel #2. Validate the operation of each bit.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

17.3 Repeat steps 17.1 to 17.2 for all DALCAL modules in the cabinet under test.

DALCAL MODULE DIGITAL LOOPBACK VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the DALCAL module digital loopback validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the DALCAL module digital loopback will be repeated on the module where the non-conformance was noted.

DALCAL MODULE ANALOG LOOPBACK VALIDATION

17.4 Load the DALCAL module test program into the Analog Input Test Computer per the CPI Description and Operating Instructions for the Analog Input Test Computer.

17.5 Use information from the operating instructions, Attachment 2, Appendix C, Section 6, and the following steps to answer the program prompts to run the DALCAL test program on the DALCAL module / Analog to Digital Converter Module pair under test.

17.6 Run an offset test at gain code 0 for 100 scans and validate an offset within (-0.050 : +0.050)V.

17.7 Run an offset test at gain code 1 for 100 scans and validate an offset within (-0.025 : +0.025)V.

17.8 Run an offset test at gain code 2 for 100 scans and validate an offset within (-0.0125 : +0.0125)V.

17.9 Run an offset test at gain code 3 for 100 scans and validate an offset within (-0.00625 : +0.00625)V.

17.10 Run a positive full scale test at gain code 0 for 100 scans and validate a voltage within (+9.950 : +10.050)V.

17.11 Run a positive full scale test at gain code 1 for 100 scans and validate a voltage within (+4.975 : +5.025)V.

17.12 Run a positive full scale test at gain code 2 for 100 scans and validate a voltage within (+2.4875 : +2.5125)V.

17.13 Run a positive full scale test at gain code 3 for 100 scans and validate a voltage within (+1.24375 : +1.25625)V.

17.14 Run a negative full scale test at gain code 0 for 100 scans and validate a voltage within (-9.950 : -10.050)V.

17.15 Run a negative full scale test at gain code 1 for 100 scans and validate a voltage within (-4.975 : -5.025)V.

17.16 Run a negative full scale test at gain code 2 for 100 scans and validate a voltage within (-2.4875 : -2.5125)V.

17.17 Run a negative full scale test at gain code 3 for 100 scans and validate a voltage within (-1.24375 : -1.25625)V.

MODULE PAIRS TESTED:

CHASSIS #	DALCAL / A.D.C SLOT #		INITIALS
_____	_____	_____	_____/_____
_____	_____	_____	_____/_____
_____	_____	_____	_____/_____
_____	_____	_____	_____/_____

17.18 Repeat steps 17.5 to 17.17 on all DALCAL modules configured with Analog to Digital Converter cards in the cabinet under test.

DALCAL MODULE ANALOG LOOPBACK/ CALIBRATION VALIDATION

PERFORMED BY: _____ C.P.I.

APPROVED BY: _____ N.U.S.

APPROVED BY: _____ B.G.E.

If a non-conformance is noted during the DALCAL module analog loopback validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the DALCAL module analog loopback will be repeated on the module where the non-conformance was noted.

DALCAL MODULE TEMPERATURE MONITORING VALIDATION

17.19 Using the Digital Thermometer, measure the temperature (in Celsius) at the temperature transducer (559-5002) monitored by the DALCAL module in the cabinet under test. Record the temperature measured below.

17.20 Use information from the operating instructions, Attachment 2, Appendix C, Section 7, and the following steps to answer the program prompts to run the DALCAL test program on the DALCAL modules configured to measure the cabinet temperature.

17.21 Run the system monitor test for 100 scans and validate that the DALCAL modules configured to measure cabinet temperature indicate a temperature within 3 degrees Celsius of that temperature measured with the digital thermometer.

MODULES TESTED:

CHASSIS # SLOT # INITIALS

_____ _____ _____/_____

CABINET TEMPERATURE USING DIGITAL THERMOMETER : _____

CABINET TEMPERATURE USING DALCAL : _____

CHASSIS # SLOT # INITIALS

_____ _____ _____/_____

CABINET TEMPERATURE USING DIGITAL THERMOMETER : _____

CABINET TEMPERATURE USING DALCAL : _____

17.22 Repeat steps 17.19 to 17.21 on all DALCAL modules configured to measure cabinet temperature.

DALCAL MODULE TEMPERATURE MONITORING VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the DALCAL module temperature monitoring validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the DALCAL module temperature monitoring will be repeated on the module where the non-conformance was noted.

18. POWER SUPPLY MONITORING VALIDATION

The purpose of this test is to validate the gross operation of the analog input modules (021-5234) monitoring cabinet power supplies and the RTD signal conditioning module power supplies; to validate the accuracy of the input module to terminal strip cabling (075-0053) and the terminal strip to power supply dividers or terminal strip to RTD SCM power supply cabling; and to validate the operation of the digital input module (021-5227) monitoring the contact sense (125 Volt) power supply and the accuracy of the input module to terminal strip cabling (075-5227) and any other associated cabling.

The validation of the analog inputs monitoring the power supplies is accomplished by using the test computer system to run a test program to acquire analog data from the analog input gate module under test and validating that the data acquired represents voltages representative of the outputs from the power supply dividers. Then Each power supply will be powered down and the corresponding data must indicate a loss of power supply.

The validation of the digital inputs monitoring the contact sense (125 Volt) power supply is accomplished by using a control panel to monitor the digital input module under test, removing the source of 125 Volts to the module under test and validating that the appropriate digital bit changes state.

CABINET POWER SUPPLY MONITOR VALIDATION

18.1 Use information from the analog input test computer operating instructions, Attachment 2, Appendix C, Section 6, and the following steps to answer the program prompts to run the analog input test program on the analog input gate module that is wired to monitor cabinet power supplies.

18.2 Validate that the channels monitoring the +5 volt power supplies, where applicable, measure (4.0 : 6.0) volts.

18.3 Validate that the channels monitoring the +15 volt power supplies, where applicable, measure (4.0 : 6.0) volts.

18.4 Validate that the channels monitoring the -15 volt power supplies, where applicable, measure (-4.0 : -6.0) volts.

18.5 Validate that the channels monitoring the +125 volt power supplies, where applicable, measure (4.0 : 6.0) volts.

18.6 Unplug the 'A' power cord of the 5 volt power supply monitored by the analog input module under test, where applicable, from its AC panel.

18.7 Rerun the analog input test program and validate that the channel monitoring the 'A' 5 volt power supply indicates a voltage less than 1.0 volt.

18.8 Reinstall the 'A' power cord in the AC panel and unplug the 'B' power cord.

18.9 Rerun the analog input test program and validate that the channel monitoring the 'B' 5 volt power supply indicates a voltage less than 1.0 volt.

18.10 Reinstall the 'B' power cord in the AC panel.

18.11 Unplug the 'A' power cord of the +15 volt power supply monitored by the analog input module under test, where applicable, from its AC panel.

18.12 Rerun the analog input test program and validate that the channel monitoring the 'A' +15 volt power supply indicates a voltage less than 1.0 volt.

18.13 Reinstall the 'A' power cord in the AC panel and unplug the 'B' power cord.

18.14 Rerun the analog input test program and validate that the channel monitoring the 'B' +15 volt power supply indicates a voltage less than 1.0 volt.

18.15 Reinstall the 'B' power cord in the AC panel.

18.16 Unplug the 'A' power cord of the -15 volt power supply monitored by the analog input module under test, where applicable, from its AC panel.

18.17 Rerun the analog input test program and validate that the channel monitoring the 'A' -15 volt power supply indicates a voltage of between (0.0 : -1.0) volts.

18.18 Reinstall the 'A' power cord in the AC panel and unplug the 'B' power cord.

18.19 Rerun the analog input test program and validate that the channel monitoring the 'B' -15 volt power supply indicates a voltage of between (0.0 : -1.0) volts.

18.20 Reinstall the 'B' power cord in the AC panel.

18.21 Unplug the 'A' power cord of the 125 volt power supply monitored by the analog input module under test, where applicable, from its AC panel.

18.22 Rerun the analog input test program and validate that the channel monitoring the 'A' 125 volt power supply indicates a voltage less than 1.0 volt.

18.23 Reinstall the 'A' power cord in the AC panel and unplug the 'B' power cord.

18.24 Rerun the analog input test program and validate that the channel monitoring the 'B' 125 volt power supply indicates a voltage less than 1.0 volt.

18.25 Reinstall the 'B' power cord in the AC panel.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

18.26 Repeat steps 18.1 to 18.25 for all analog inputs in the cabinet wired to monitor cabinet power supplies.

CABINET POWER SUPPLY MONITORING VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the cabinet power supply monitoring validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the cabinet power supply monitoring will be repeated on the module where the non-conformance was noted.

RTD SCM POWER SUPPLY MONITORING VALIDATION

18.27 Use information from the analog input test computer operating instructions, Attachment 2, Appendix C, Section 6, and the following steps to answer the program prompts to run the analog input test program on the analog input gate module that is wired to monitor RTD Signal Conditioning Module power supplies.

18.28 Validate that the channels monitoring RTD SCM power supplies, where applicable, measure (+9.9 : +10.1) volts.

18.29 Remove the first RTD signal conditioning module from its backplane connector with its hood still attached.

18.30 Allow thirty seconds or more to allow the filter capacitors of the analog input module monitoring the RTD SCM power supply to settle.

18.31 Rerun the analog input test program and verify that the channel monitoring the power supply of the RTD SCM removed from the backplane indicates a voltage of less than 1.0 volts.

18.32 Repeat steps 18.29 to 18.31 on each of the RTD SCMs monitored by the analog input module under test.

18.33 Unplug the power cord of the RTD signalling conditioning chassis from the AC panel and reinstall the RTD SCMs removed from the backplane then reinstall the power cord.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	____/____	_____	_____	____/____
_____	_____	____/____	_____	_____	____/____

18.34 Repeat steps 18.27 to 18.33 for all analog inputs in the cabinet under test wired to monitor RTD SCM power supplies.

RTD SCM POWER SUPPLY MONITORING VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the RTD SCM power supply monitoring validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the RTD SCM power supply monitoring will be repeated on the module where the non-conformance was noted.

CONTACT SENSE VOLTAGE MONITORING VALIDATION

18.35 Configure Control Panel #2 as follows:

DEVICE ADDRESS SELECT : to address the first device code of the I/O controller containing the digital input module monitoring the 125 volts under test per Attachment 2, Section 6, and Appendix B.

INSTRUCTION SELECT : COM, WAIT TEST, AND IN UP

COMMAND WORD : to select random mode, disable interrupts, and to address the module under test using Attachment 2, Appendix B, and Appendix C.

INSTRUCTION RATE : 50K range - vernier midrange

18.36 RESET the control panel.

18.37 Validate that the bits, in the control panel Data Word Display, associated with the contact sense voltage are ON.

18.38 For input modules monitoring the contact sense voltage of 'Channel B' Up/ Down Pulse Counters, unplug both power cords of the 125 volt power supply supplying the contact sense voltage being monitored by the input module under test and validate that the bits, in the control panel data word display, associated these pulse counter modules are OFF.

18.39 For input modules monitoring the contact sense voltage of modules other than the 'Channel B' Up/ Down Pulse Counters, remove the hood from the 300/400 side of the signal conditioning module and validate that the bit associated with the module whose hood was disconnected is OFF. Repeat this for all modules monitored by the module under test.

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	____/____	_____	_____	____/____
_____	_____	____/____	_____	_____	____/____

18.40 Repeat steps 18.35 to 18.39 for all digital inputs in the cabinet under test wired to monitor contact sense voltage.

CONTACT SENSE MONITORING DIGITAL INPUT VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the contact sense voltage monitoring validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the contact sense voltage monitoring will be repeated on the module where the non-conformance was noted.

19. VOLTAGE SENSING ANALOG INPUT GATE MODULE VALIDATION

The purpose of this test is to validate the gross operation of the Universal High Speed Wide Range Analog Input modules (021-5234) and their associated signal conditioning circuits (038-5097) and to validate the accuracy of the input module to signal conditioning module (040-5455) and the signal conditioning module to terminal strip (040-5520) or Uniform Temperature Reference Plate cabling (040-5522). It is not intended to validate the accuracy of the analog input cards.

This validation is accomplished by connecting a voltage divider network to the terminals sourcing the analog input module, and applying a voltage to the divider. Then data is read from the analog input module using the Analog Input Test Computer and test programs. This data is validated against a table of voltages derived from the divider network and the voltage applied. (Reference Figure 9 of Attachment 1)

19.1 Set the programmable DC voltage standard to zero volts.

19.2 Install the 'BTSCA to Test Cable/ Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test for those analog inputs terminated with BTSCAs.

19.3 Connect the Analog Input Test Divider/ Connector for BTSCAs (000-7081) to the BTSCA to Test Cable/ Connector Adapter for BTSCA terminated analog inputs. Connect the Analog Input Test Divider/ Connector for UTRPs (000-7085) to the UTRP terminals for UTRP terminated analog inputs.

19.4 Connect the output of the programmable DC voltage standard to the test divider inputs corresponding to the module under test.

19.5 Set the programmable DC voltage standard to +4.070 volts (voltage standard switch setting : 65C00 hexidecimal).

19.6 Use information from the analog input test computer operating instructions, Attachment 2, Appendix C, Section 6, and the following steps to answer the program prompts to run the analog input test program on the analog input gate module under test.

19.7 Run the Analog Input Test Program on the selected module for 100 scans at Gain Code 8. Validate that the mean voltages of each channel scanned are within the following voltages :

CH 0 = +(38 : 42) mV	CH 4 = +(18 : 22) mV
CH 1 = +(33 : 37) mV	CH 5 = +(13 : 17) mV
CH 2 = +(28 : 32) mV	CH 6 = +(8 : 12) mV
CH 3 = +(23 : 27) mV	CH 7 = +(3 : 7) mV

MODULES TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/
		/			/

19.8 Repeat steps 19.1 to 19.7 for all analog input modules with voltage sense inputs in the cabinet under test.

ANALOG INPUT (with voltage sense inputs) VALIDATION

PERFORMED BY: ______________________________ C.P.I.

WITNESSED BY: ______________________________ N.U.S.

If a non-conformance is noted during the voltage sensing analog input module validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the voltage sense analog input monitoring will be repeated on the module where the non-conformance was noted.

20. VOLTAGE SENSING ANALOG INPUT GATE MODULE ACCURACY, COMMON MODE REJECTION, and SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate that the accuracy and common mode rejection of a sample of the analog to digital converter module/ analog input gate module (021-0211 / 021-5234) pairs and associated signal conditioning circuitry (038-5097) and cabling are within the published CPI specifications for the products being tested. Also validated is the surge withstand capability of this sample of the signal conditioning modules (038-5097). The drift/stability of this sample will also be validated in section 23.

The validation of the accuracy and common mode rejection are accomplished by using the analog input test computer to run the analog input test program to acquire data from the analog input module sets. First the module set will be run with zero common mode voltage to record the baseline noise on the inputs, then a common mode voltage source will be connected to the inputs to the gate module and the test program will be rerun to record the input noise with common mode voltage applied. The two runs will be compared and the difference between the baseline noise and the noise with common mode voltage applied must be less than specifiations derived from the specifications of the module set. Then a precision voltage standard will be used to excite the inputs of the gate module in parallel and the test program will be run to record baseline offset in the channels then the precision voltage will be applied and the program will be rerun. The difference between the offset run and the voltage applied must be within specifications derived from the specifiations of the module set. (Reference Figures 10 and 11 of Attachment 1)

The validation of the surge withstand capability is accomplished by simulating transducers with one kiloohm resistors between the HIGH and LOW input terminals to the module. Then a surge is applied to one side of the resistors. Data is not acquired from the analog input module during the surge application. After the surge has been applied, the accuracy and common mode rejection of the module set will be retested to validate that the surge did not affect the performance of the module set. (Reference Figure 12 of Attachment 1)

20.1 Select up to five percent or at least one of the surge protected analog inputs modules with voltage sense BTSCA terminations in the cabinet to have common mode rejection, accuracy, surge withstand capability and drift/stability (in section 23.) validation performed on them.

20.2 Install the 'BTSCA to Test Cable/ Connector Adapter' (000-7077) on the selected BTSCA in the cabinet under test per Attachment 2.

20.3 Install the 'Analog Input Unbalanced Test Termination/ Connector' (000-7079) on the 'BTSCA to Test Cable/ Connector Adapter'.

20.4 Connect the output of the AC/DC V-A Source between the bussed inputs (red/high lead) corresponding to the module under test on the unbalanced test termination/ connector and the surge ground bus bar (black/low lead) in the cabinet under test.

20.5 With the AC/DC V-A source at zero volts, run the Analog Input Test Program on the selected module for 100 scans at Gain Code 8. This is to record the baseline noise on the channels of the module under test.

20.6 Set the AC/DC V-A source to 600 volts RMS (1697 V P-P), 60 HZ.

20.7 Run the Analog Input Test Program on the selected module for 100 scans at Gain Code 8. This is to record the increase in noise due to the common mode voltage not rejected.

20.8 Set the common mode voltage source to zero.

20.9 Validate that the peak to peak noise with the common mode voltage applied does not increase more than 2.7 millivolts for 021-5234-002 analog input gate modules, or more than 540 microvolts for 021-5234-003 analog input gate modules.

20.10 Set the programmable DC voltage standard to output zero volts.

20.11 Replace the 'Analog Input Unbalanced Test Terminator/ Connector' with the 'Analog Input Parallel Input Test Connector' (000-7082) on the 'BTSCA to Test Cable/ Connector Adapter'.

20.12 Connect the output of the programmable DC voltage standard to the input on the 'Analog Input Parallel Input Test Connector' corresponding to the module under test.

20.13 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

20.14 With the programmable DC voltage standard at zero volts, run the Analog Input Test Program on the selected module for 100 scans at Gain Code 8. This is to record the baseline offset on the channels of the module under test.

20.15 Set the programmable DC voltage standard for +0.070 volts (programmable DC voltage standard setting : 01C00 hexa-decimal).

20.16 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

20.17 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 8.

20.18 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.14 is within +(69.96 : 70.04) millivolts.

20.19 Set the programmable DC voltage standard for -0.070 volts.

20.20 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

20.21 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 8.

20.22 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.14 is within -(69.96 : 70.04) millivolts.

20.23 Set the programmable DC voltage standard to output zero volts.

20.24 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

20.25 Run the Analog Input Test Program on the selected module for 100 scans at Gain Code 4. This is to record the baseline offset on the channels of the module under test.

20.26 Set the programmable DC voltage standard for +0.560 volts (programmable DC voltage standard setting : 0E000 hexa-decimal).

20.27 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

20.28 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 4.

20.29 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.25 is within +(559.68 : 560.32) millivolts.

20.30 Set the programmable DC voltage standard for -0.560 volts.

20.31 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

20.32 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 4.

20.33 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.25 is within -(559.68 : 560.32) millivolts.

20.34 Set the programmable DC voltage standard to output zero volts.

20.35 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

20.36 Run the Analog Input Test Program on the selected module for 100 scans at Gain Code 0. This is to record the baseline offset on the channels of the module under test.

20.37 Set the programmable DC voltage standard for +8.960 volts (programmable DC voltage standard setting : E0000 hexadecimal).

20.38 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

20.39 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 0.

20.40 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.36 is within +(8.955 : 8.965) volts.

20.41 Set the programmable DC voltage standard for -8.960 volts.

20.42 For 021-5234-003 analog input gate modules, allow a minimum of thirty seconds before continuing to allow the filter capacitors to settle.

20.43 Rerun the Analog Input Test Program on the selected module for 100 scans at Gain Code 0.

20.44 Validate that the mean of each channel scanned with voltage applied less the mean of the same channel with zero volts applied in step 20.36 is within -(8.955 : 8.965) volts.

20.45 Set the programmable DC voltage standard to output zero volts.

20.46 Replace the 'Analog Input Parallel Input Test Connector' with the 'Analog Input Unbalanced Test Terminator/ Connector' on the 'BTSCA to Test Cable/ Connector Adapter'.

20.47 Connect the red lead of the surge transient generator cable to the the bussed inputs on the test connector corresponding to the module under test. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.

20.48 Ready the surge transient generator to output a surge per Appendix D.

20.49 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds.

20.50 Repeat steps 20.3 to 20.49 to validate that the module set under test continues to meet specifications.

MODULE(S) SELECTED and TESTED:

CHASSIS #	SLOT #	INITIALS	CHASSIS #	SLOT #	INITIALS
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____
_____	_____	_____/_____	_____	_____	_____/_____

20.51 Repeat steps 20.2 to 20.50 on all of the modules in the selected sample.

VOLTAGE SENSING ANALOG INPUT COMMON MODE REJECTION, ACCURACY, and SURGE WITHSTAND VALIDATION

PERFORMED BY: _____ C.P.I.

APPROVED BY: _____ N.U.S.

APPROVED BY: _____ B.G.E.

If a non-conformance is noted during the voltage sensing analog input common mode rejection, accuracy, and surge withstand capability validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the voltage sensing analog input common mode rejection, accuracy, and surge withstand capability will be repeated on the module where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one of the voltage sensing analog input modules (with BTSCA terminations) will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

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1. RESISTIVE SENSING ANALOG INPUT GATE MODULE VALIDATION

The purpose of this test is to validate the gross operation of the analog input modules (021-5234) whose inputs are conditioned wth resistive thermal device bridge completion circuits (038-5108); to validate the accuracy of the analog input gate module to RTD signal conditioning module cabling (040-5505) and the RTD signal conditioning module to terminal strip cabling (040-5521); and to validate the gross operation of the resistive thermal device in the uniform temperature reference plate (040-5522) and the accuracy of the associated cabling.

The validation of the analog inputs is accomplished by simulating resistive thermal devices with resistors on the terminal strip sourcing the input circuitry, then monitoring the data read from the analog input modules with the test computer and validating that the data read corresponds to the expected voltage from the RTD SCM per a table of voltage output versus resistance applied. (Reference Figure 13 of Attachment 1)

The validation of the resistive thermal device is accomplished by monitoring the data read from the analog input modules with the test computer and validating that the data read corresponds to a voltage corresponding to room temperature (assuming a room temperature range of 70F to 85F).

21.1 Connect the appropriate RTD Resistor Terminations (000-7086 for 038-5108-100, 200 ohm Pl, 32-350F; 000-7087 for 038-5108-101, 200 ohm Pl, 32-850F; 000-7088 for 038-5108-102, 200 ohm Pl, 32-110F; 000-7089 for 038-5108-103, 10 ohm Cu, -10-209C) to the appropriate points on the selected RTD BTSCA in the cabinet under test per Attachment 2 except on the channels wired to monitor the UTR RTD.

21.2 Run the Analog Input Test Program on the selected module set for 100 scans at gain code 4. Validate that the analog inputs indicate voltages within the voltage range in the following table: (all values in millivolts)

(Each RTD bridge completion module has circuits for the conditioning of four analog channels. Thus the eight channel gate modules require two RTD bridge completion modules, one for the first four channels, and another for the second four channels. This necessitates that the test program be run twice and the data from the SCM not being tested be ignored.)

(Note that some analog input gate modules are conditioned with only four channels of RTD conditioning, thus the other four channels are unterminated and their data must be ignored).

(The channels (of the 038-5108-100) wired to monitor the UTR RTD must indicate a voltage corresponding to the temperature of the uniform temperature reference plate which is assumed to be at room temperature of between 70F (19 millivolts) and 85F (27 millivolts).)

RTD TYPE =	200 Ohm Pl	200 Ohm Pl	200 Ohm Pl	10 Ohm Cu
TEMP =	32 : 350 F	32 : 850 F	32 : 110 F	-10 : 209 C
P/N :	038-5108-100	038-5108-101	038-5108-102	038-5108-103
CH 0 =	+32 : +48	+64 : +96	+6 : +14	+2.0 : +3.0
CH 1 =	+72 : +88	+144 : +176	+16 : +24	+4.5 : +5.5
CH 2 =	+112 : +128	+224 : +256	+26 : +34	+7.0 : +8.0
CH 3 =	+152 : +168	+304 : +336	+36 : +44	+9.5 : +10.5

VOLTAGES (millivolts) OUTPUT FROM RTD BRIDGE COMPLETION CIRCUITS

MODULES TESTED:

GATE MODULE CHASSIS #	SLOT #	CH 0-3 RTD SCM CHASSIS #	SLOT #	CH 4-7 RTD SCM CHASSIS #	SLOT #	INITIALS
_____	_____	_____	_____	_____	_____	_____/_____
_____	_____	_____	_____	_____	_____	_____/_____
_____	_____	_____	_____	_____	_____	_____/_____
_____	_____	_____	_____	_____	_____	_____/_____
_____	_____	_____	_____	_____	_____	_____/_____
_____	_____	_____	_____	_____	_____	_____/_____
_____	_____	_____	_____	_____	_____	_____/_____
_____	_____	_____	_____	_____	_____	_____/_____

21.3 Repeat steps 21.1 to 21.2 for all analog input gate modules with resistive thermal device signal conditioning in the cabinet under test.

ANALOG INPUT (with resistive sense inputs) VALIDATION

PERFORMED BY: _____ C.P.I.

WITNESSED BY: _____ N.U.S.

If a non-conformance is noted during the resistive sensing analog input validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the resistive sensing analog input modules will be repeated on the module where the non-conformance was noted.

22. RESISTIVE SENSING ANALOG INPUT GATE MODULE SURGE WITHSTAND CAPABILITY VALIDATION

The purpose of this test is to validate the surge withstand capability of a sample of the RTD signal conditioning modules (038-5108). This is accomplished by simulating RTD inputs on the input terminals to the module set, and first acquiring baseline/ reference data from the analog input module. A surge is then applied to the inputs. Data is not acquired during the surge application. Data is again acquired from the analog input module after the surge application and the data is validated as not changing by more than a predefined limit. (Reference Figure 14 of Attachment 1)

22.1 Select up to five percent or at least one of the surge protected Analog Inputs with RTD signal conditioning (021-5234 / 038-5108) to have the surge withstand capability tested. Since two RTD SCMs are required to condition one analog input gate module, two RTD SCMs will be surge tested for every analog input gate selected.

22.2 Connect the appropriate RTD Resistor Terminations (000-7086 for 038-5108-100, 200 ohm Pl, 32-350F; 000-7087 for 038-5108-101, 200 ohm Pl, 32-850F; 000-7088 for 038-5108-102, 200 ohm Pl, 32-110F; 000-7089 for 038-5108-103, 10 ohm Cu, -10-209C) to the appropriate points on the selected RTD BTSCA in the cabinet under test per Attachment 2 except on the channels wired to monitor the UTR RTD.

22.3 Run the Analog Input Test Program on the selected module set for 100 scans at gain code 4. Validate that the analog inputs indicate voltages within the voltage range in the following table: (all values in millivolts)

(Each RTD bridge completion module has circuits for the conditioning of four analog channels. Thus the eight channel gate modules require two RTD bridge completion modules, one for the first four channels, and another for the second four channels. This necessitates that the test program be run twice and the data from the SCM not being tested be ignored.)

(Note that some analog input gate modules are conditioned with only four channels of RTD conditioning, thus the other four channels are unterminated and their data must be ignored).

(The channels (of the 038-5108-100) wired to monitor the UTR RTD must indicate a voltage corresponding to the temperature of the uniform temperature reference plate which is assumed to be at room temperature of between 70F (19 millivolts) and 85F (27 millivolts).)

RTD TYPE =	200 Ohm Pl	200 Ohm Pl	200 Ohm Pl	10 Ohm Cu
TEMP =	32 : 350 F	32 : 850 F	32 : 110 F	-10 : 209 C
P/N :	038-5108-100	038-5108-101	038-5108-102	038-5108-103
CH 0 =	+32 : +48	+64 : +96	+6 : +14	+2.0 : +3.0
CH 1 =	+72 : +88	+144 : +176	+16 : +24	+4.5 : +5.5
CH 2 =	+112 : +128	+224 : +256	+26 : +34	+7.0 : +8.0
CH 3 =	+152 : +168	+304 : +336	+36 : +44	+9.5 : +10.5

VOLTAGES (millivolts) OUTPUT FROM RTD BRIDGE COMPLETION CIRCUITS

22.4 Connect the red lead of the surge transient generator cable to the RTD test termination on the selected BTSCA. Connect the black lead of the surge transient generator cable to the surge ground bus bar in the cabinet under test.

22.5 Ready the surge transient generator to output a surge per Appendix D.

22.6 Depress the surge transient generator Start pushbutton to apply the surge voltage for two seconds.

22.7 Rerun the Analog Input Test Program on the selected module set for 100 scans at gain code 4. Validate that the analog inputs indicate voltages within the voltage range in the table above (all values in millivolts).

22.8 Validate that the means of the channels on the analog input module conditioned with the selected RTD SCM do not change by more than 1 bit between the pre-surge sample and the post-surge sample.

22.9 Validate that the peak to peak noise of the channels on the selected module does not increase by more than 2 bits peak to peak between the pre-surge sample and the post-surge sample.

MODULES SELECTED and TESTED:

GATE MODULE CHASSIS #	GATE MODULE SLOT #	CH 0-3 RTD SCM CHASSIS #	CH 0-3 RTD SCM SLOT #	CH 4-7 RTD SCM CHASSIS #	CH 4-7 RTD SCM SLOT #	INITIALS
_____	_____	_____	_____	_____	_____	____/____
_____	_____	_____	_____	_____	_____	____/____
_____	_____	_____	_____	_____	_____	____/____
_____	_____	_____	_____	_____	_____	____/____
_____	_____	_____	_____	_____	_____	____/____

22.10 Repeat steps 22.2 to 22.9 on all of the analog input/ RTD signal conditioning modules in the selected sample.

RESISTIVE SENSING ANALOG INPUT SURGE WITHSTAND CAPABILITY VALIDATION

PERFORMED BY: _____ C.P.I.

APPROVED BY: _____ N.U.S.

APPROVED BY: _____ B.G.E.

Note that, due to design constraints, the inputs to the resistive thermal device bridge completion circuits are not surge protected, but the output of the circuits is surge protected and will protect the analog input gate module.

If a non-conformance is noted during the resistive sensing analog input surge withstand capability validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the resistive sensing analog input surge withstand capability will be repeated on the module where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one of the resistive sensing analog input modules will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

23. ANALOG INPUT DRIFT/STABILITY TEST

The purpose of this test is to validate that the sample of voltage sense analog input modules selected for common mode rejection, accuracy, and surge withstand capability validation are within the CPI published specifications for drift/stability.

23.1 Using bus wire, short the input terminals of the voltage sense analog input modules selected for common mode rejection, accuracy, and surge withstand capability testing . Connect the shorted channels to the surge ground bus bar in the cabinet under test.

23.2 Allow the cabinet (cabinet subsystem) to stabilize for a minimum of 2 hours.

23.3 Run the Analog Input Test Program on the selected modules for 100 scans at Gain Code 11.

23.4 Using the digital thermometer, record the temperature at the temperature transducer inside the cabinet under test.

23.5 Repeat steps 23.3 to 23.4 at two hour intervals four times.

INITIAL SCAN TIME: __________ TEMP: __________

(Enter mean voltage from scan below)

MODULE TESTED: CHASSIS # ________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # ________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # ________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # ________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # ________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # ________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

SECOND SCAN: TIME: ____________ TEMP: ____________

(Enter mean voltage from scan below and deviation from initial scan under mean)

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

THIRD SCAN: TIME: ____________ TEMP: ____________

(Enter mean voltage from scan below and deviation from initial scan under mean)

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

FOURTH SCAN: TIME: ___________ TEMP: ___________

(Enter mean voltage from scan below and deviation from initial scan under mean)

MODULE TESTED: CHASSIS # _________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # _____ INITIALS: _____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

FIFTH SCAN: TIME: ____________ TEMP: ____________

(Enter mean voltage from scan below and deviation from initial scan under mean)

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

MODULE TESTED: CHASSIS # _________ SLOT # ______ INITIALS:_____/_____

CHAN 0	CHAN 1	CHAN 2	CHAN 3	CHAN 4	CHAN 5	CHAN 6	CHAN 7

23.6 Determine the channel with the most deviation from the initial scan for for each successive scan.

SECOND SCAN : CHASSIS # _____ SLOT # _____

CHAN # _____ MAX. DEVIATION _____

THIRD SCAN : CHASSIS # _____ SLOT # _____

CHAN # _____ MAX. DEVIATION _____

FOURTH SCAN : CHASSIS # _____ SLOT # _____

CHAN # _____ MAX. DEVIATION _____

FIFTH SCAN : CHASSIS # _____ SLOT # _____

CHAN # _____ MAX. DEVIATION _____

23.7 Validate that the maximum deviation for each sampling is within +/- 10 microvolts plus +/- 0.5 microvolts per degree C change in ambient temperature of the initial reading.

Second reading : temp change _____ C

maximum allowable deviation =

(temp change _____ C X 0.5 uV/C) + 10 uV = _____ uV

maximum measured deviation : _____

Third reading : temp change _____ C

maximum allowable deviation =

(temp change _____ C X 0.5 uV/C) + 10 uV = _____ uV

maximum measured deviation : _____

Fourth reading : temp change _____ C

maximum allowable deviation =

(temp change _____ C X 0.5 uV/C) + 10 uV = _____ uV

maximum measured deviation : _____

Fifth reading : temp change _____ C

maximum allowable deviation =

(temp change _____ C X 0.5 uV/C) + 10 uV = _____ uV

maximum measured deviation : _____

ANALOG INPUT DRIFT/ STABILITY TEST

PERFORMED BY: _____ C.P.I.

APPROVED BY: _____ N.U.S.

APPROVED BY: _____ B.G.E.

If a non-conformance is noted during the voltage sensing analog input drift/ stability validation, the non-conformance will be dispositioned per Section 3., the non-conformance will be corrected, and the validation of the voltage sensing analog input drift/ stability will be repeated on the module where the non-conformance was noted. After the test is complete, an additional sample of five percent, or at least one of the voltage sensing analog input modules (with BTSCA terminations) will be selected and tested. This will be repeated if another non-conformance is identified in the second sample.

APPENDIX A

TEST AND REPAIR LOG BOOK FORMAT

The Test and Repair Log is used to record any and all acceptance testing of the data acquisition system supplied by Computer Products, Inc. to NUS Corp. and Baltimore Gas and Electric for the Calvert Cliffs power generation plant. It is also used to record any and all anomalies noted during this testing and the corrective action taken to correct the anomalies.

Entries (in black ink) are to be made in the log as follows:

Identification of Cabinet under test :
Unit # (I or II), CPI cabinet # (1 - 11);

Title of test procedure used for testing
(or 'Continuation of Anomalies of Unit X Cabinet X' if an additional page is required to list the anomalies);
Date test started;
Date test completed;
Name of test conductor printed and signed;
Name of the witness printed and signed;
If no anomalies are noted during the test, then NONE is checked in the anomalies noted section;
If anomalies are noted, then a description of the anomaly is entered and the action taken to correct the anomaly is described. The last anomaly is followed by 'End of Anomalies'.

The following are sample pages of the log with typical responses.

********** THE FOLLOWING IS A SAMPLE ONLY. **********

TEST and REPAIR LOG for
NUS / BALTIMORE GAS and ELECTRIC CALVERT CLIFFS
DATA ACQUISITION SYSTEM supplied by COMPUTER PRODUCTS, INC.

UNIT # I CPI CABINET # 3

TESTED PER

REMOTE I/O HARDWARE ACCEPTANCE TEST PROCEDURE dated 1/29/84
(procedure used for testing)

DATE STARTED: 1 MARCH 1984 DATE COMPLETED: 3 MARCH 1984

PERFORMED BY: (conductor's name) (conductor's sign.)
(printed) (signed)

WITNESSED BY: (auditor's name) (auditor's sign.)
(printed) (signed)

==========

ANOMALIES NOTED and CORRECTIVE ACTION TAKEN: (NONE:(X))

_____

_____

_____

_____

_____

_____

********** THE PRECEDING IS A SAMPLE ONLY. **********

********** THE FOLLOWING IS A SAMPLE ONLY. **********

TEST and REPAIR LOG for
NUS / BALTIMORE GAS and ELECTRIC CALVERT CLIFFS
DATA ACQUISITION SYSTEM supplied by COMPUTER PRODUCTS, INC

UNIT # II CPI CABINET # 9

TESTED PER

(CONTINUATION OF ANOMALIES NOTED)
(procedure used for testing)

DATE STARTED: _____ DATE COMPLETED: _____

PERFORMED BY: _____ _____
(printed) (signed)

WITNESSED BY: _____ _____
(printed) (signed)

==========

ANOMALIES NOTED and CORRECTIVE ACTION TAKEN: (NONE:( ))

5) Section 17. : Analog to Digital Converter (9F3-11) (P/N 021-0211-008 S/N C0099) out of calibration. Recalibrated ADC per AT 021-0211 and test rerun.

(END OF ANOMALIES)

********** THE PRECEDING IS A SAMPLE ONLY. **********

APPENDIX B

CPI RTP CONTROL PANEL DESCRIPTION AND OPERATING INSTRUCTION SUMMARY

The following is a condensed description and summary of operation of the CPI RTP7505/05 Control Panel (P/N 070-0044) required for the performance of this acceptance test. For more information refer to CPI Technical Manual # 980-0070-044.

The RTP7505/05 Control Panel is used to provide an easy to use method of exercising the various inputs and outputs of equipment connected via the RTP bus. Connection to the bus is through a ribbon cable connected from slot #5 of the control panel to the 'I/O Bus In' slot of the first chassis in the I/O string. A computer may be connected to slot #1 of the control panel allowing either the computer or the control panel to access the peripheral equipment attached to the RTP I/O bus.

The following controls and indicators are used on the Control Panel:

1. MAN/COMP (Manual/Computer) switch
2. DATA WORD DISPLAY
3. INTERRUPT VECTOR DISPLAY
4. OUTPUT WORD SELECT switches
5. COMMAND WORD SELECT switches
6. CONTROL DISPLAY
7. INSTRUCTION RATE controls
8. DEVICE ADDRESS SELECT switches
9. INSTRUCTION SELECT switches
10. RESET switch

APPENDIX B cont'd

The MAN/COMP (MANual/COMPuter) switch is a two position switch which is used to select the operating mode of the RTP Control Panel. When the switch is placed in the MANual position, the control panel is set to the manual mode of operation and the computer is disconnected from the RTP peripheral devices connected to the control panel. When the switch is placed in the COMPuter position, the computer is connected thru the control panel to the peripheral devices on the RTP I/O bus.

The DATA WORD DISPLAY provides a visual display of the data loaded into the input buffer. Sixteen light emitting diodes (LED's), represent the 16 data bits. Each data bit will light in the presence of a '1', and be dark in the presence of a '0'. The MAN/COMP switch selects the source of the data to be loaded and displayed. In the MANual mode, the data displayed is the result of a transfer from the selected peripheral device by an input transfer function from the control panel. In the COMputer mode, the data displayed is from the computer.

The INTERRUPT VECTOR DISPLAY provides a visual display of the data bits representing the address of the current interrupt vector from the selected peripheral. Ten light emitting diodes (LED's), represent the 10 data bits. Each data bit will light in the presence of a '1', and be dark in the presence of a '0'. The data displayed is the result of a transfer from the selected peripheral device by an Interrupt Query (INT QRY) instruction from the control panel.

The OUTPUT WORD SELECT consists of 16 two position toggle switches, representing the 16 data bits, which are used to format an output data word. In the MANual mode, the data word is transfered to the selected peripheral. In the COMPuter mode, the data word is transferred to the computer during a DATA INPUT instruction addressed to the first device address of the control panel. The UP position of each switch represents a '1', and the DOWN position represents a '0'.

The COMMAND WORD SELECT consists of 16 two position toggle switches, representing the 16 data bits, which are used to format a command data word. In the MANual mode, the data word is transferred to the selected peripheral. In the COMPuter mode, the switches perform no function. The UP position of each switch represents a '1', and the DOWN position represents a '0'.

APPENDIX B cont'd

The CONTROL WORD DISPLAY provides a visual display of the status of various functions using 6 light emitting diodes (LED's), to represent the 6 functions as follows:

DEV SEL - The DEVice SELect display, when lighted, indicates that the device address switches in one of the RTP peripheral devices connected to the control panel is set to the address corresponding to the setting of the DEVICE ADDRESS SELECT switches. This display is only active in the MANual mode.

INT - The INTerrupt request display, when lighted, indicates that one or more RTP peripheral devices connected to the control panel are requesting interrupt service. The priority of the interrupts is determined by the electrical proximity of the devices to the control panel. Interrupt requests are always reset by an INTERRRUPT QUERY instruction, and depending on the type of device, by either an INPUT, OUTPUT, or COMMAND instruction or Master Reset. This display is only active in the MANual mode.

DATA RDY - The DATA ReaDY display, when lighted, indicates that the peripheral device being addressed is in a ready state. Note: the DATA RDY indicator actually monitors the RTP TEST RETURN line. This display is only active in the MANual mode.

RUN - The RUN display, when lighted, indicates that an instruction is in the instruction register and is being executed.

MAN - The MANual display, when lighted, indicates that the control panel is in the manual mode.

COMP - The COMPuter display, when lighted, indicates that the control panel is in the computer mode.

The INSTRUCTION RATE controls consist of a six position rotary switch designated RANGE and a potentiometer designated VERNIER. The overall instruction rate can be varied, using the two controls, over the total range of about 0.5 to 500,000 instructions per second.

RANGE - The RANGE selector switch is designated 5, 50, 500, 5K (5000), 50K (50,000), and 500K (500,000) which define the nominal instruction rate per second for each range.

VERNIER - The VERNIER potentiometer varies the instruction rate within each range from the maximum rate down to the minimum rate for that range.

APPENDIX B cont'd

The DEVICE ADDRESS SELECT consists of 6 two position toggle switches representing the 6 data bits, which are used to format the DEVICE ADDRESS lines on the RTP I/O bus. These switches are only active in the MANual mode and are designated 32, 16, 8, 4, 2, and 1. The UP position of each switch represents a '1', and the DOWN position represents a '0'.

The INSTRUCTION SELECT consists of 5 three position toggle switches with an LED indicator associated with each switch. The five switches are used to select MANual mode instructions to be executed and have no function in the COMPuter mode.

Four switches, COMmand, OUTput, INTerrupt QueRY, and INput each have three positions : UP - (locked) allows continuous execution; CENTER - skip execution (or no execution); and DOWN - (momentary contact with spring return) single cycle execution.

The WAIT TEST/WAIT INT switch is also a three position switch. The UP position (WAIT TEST) causes a wait in the execution sequence until the test return line tests 'ready'. The CENTER position causes a skip or no execution, and the DOWN position causes a wait in the execution sequence until an interrupt request is initiated from one of the RTP peripheral devices.

Any of the four instructions COMMAND, OUTPUT, INTERRUPT QUERY, or INPUT, can be single cycle executed in any order manually. When any of the instruction select switches are set to the up position (continuous execution), the instructions are executed in the following order: COMMAND, OUTPUT, WAIT TEST / WAIT INTERRUPT, INTERRUPT QUERY, INPUT. When the last selected instruction is executed, the sequence starts over and continues until it is stopped or the switches are changed.

Each switch has a LED associated with it which lights during execution of that particular instruction.

The RESET switch is a momentary contact with spring return switch, which when depressed, resets the logic circuitry in the RTP Control Panel and also causes an I/O Reset to all peripheral devices on the RTP I/O bus. This switch is only active in the MANual mode.

APPENDIX C

PHYSICAL SLOT NUMBER to SLOT ADDRESS CROSS REFERENCE TABLE

UNIVERSAL I/O CONTROLLERS
(070-0004 & 040-5462)

SLOT	ADDRESS (binary)	ADDRESS (decimal)
6	0000	00
7	0001	01
8	0010	02
9	0011	03
10	0100	04
11	0101	05
12	0110	06
13	0111	07
14	1000	08
15	1001	09
16	1010	10
17	1011	11
18	1100	12
19	1101	13
20	1110	14
21	1111	15

REDUNDANT ACCESS
UNIVERSAL I/O CONTROLLERS
(070-5083)

SLOT	ADDRESS (binary)	ADDRESS (decimal)
10	0000	00
11	0001	01
12	0010	02
13	0011	03
14	0100	04
15	0101	05
16	0110	06
17	0111	07

These addresses (binary) represent data bits 12 - 15 of the Command Word when used to address an option card.

APPENDIX D

OPERATING INSTRUCTIONS AND CONFIGURATION FOR TEST of the VELONEX SURGE TRANSIENT GENERATOR

****

THIS GENERATOR IS CAPABLE OF OUTPUTTING VOLTAGES THAT ARE LETHAL.

USE EXTREME CAUTION AT ALL TIMES WHEN USING THIS GENERATOR.

****

This piece of test equipment is used to generate surge transients. The surge transient required for this test is defined by IEEE Standard # 472 ('Surge Withstand Capability Testing'). Configure the generator as follows to generate the required surge transient.

Set the BURST MODE selector switch to '2X LINE FREQUENCY'; set the OUTPUT TIMER MODE selector switch to 'TIMED OUTPUT'; set the OUTPUT TIMER DURATION control to '2 seconds'; and set the SOURCE IMPEDANCE selector switch to '150 OHMS'. The settings of the BURST FREQUENCY and BURST PHASE controls are ignored in this operating mode.

Install a connector on the LOW OUTPUT terminal to connect the LOW OUTPUT to the chassis ground (connected internally to the connector).

Install a 'HV connector to alligator clip cable' to the HIGH OUTPUT terminal.

Depress the white POWER ON pushbutton to put the generator in standby mode.

To ready the generator for generating a surge transient, connect the output cable to the item to be tested (black to the surge ground reference and red to the point(s) to be tested); depress the two red HV ON pushbuttons simultaneously; adjust the OUTPUT AMPLITUDE control to the full clockwise position.

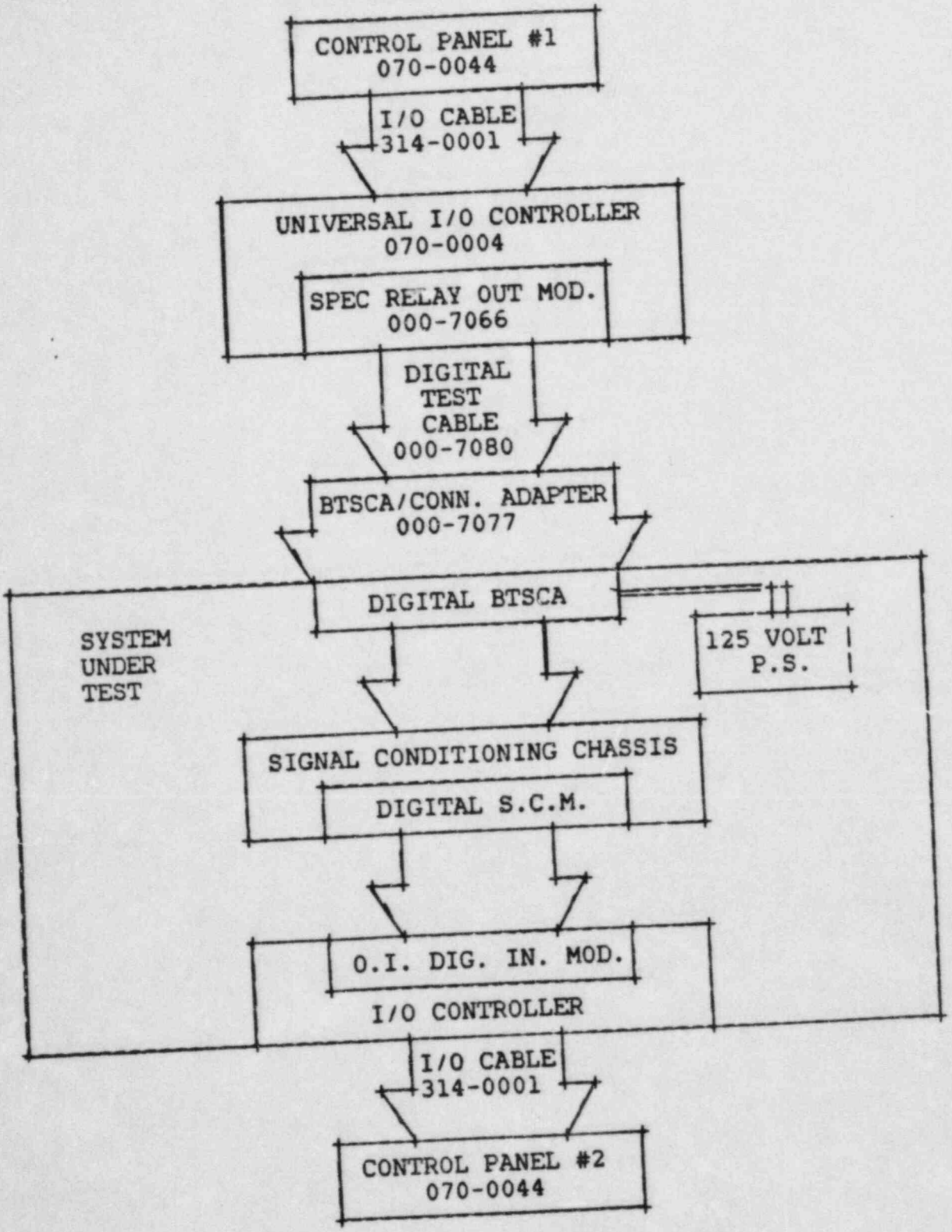
To apply the surge transient, depress the START pushbutton. This will cause a dangerous high voltage to be present at the output of the generator for two seconds, USE CAUTION.

To put the generator back into standby mode, push one of the red HV ON pushbuttons.

ATTACHMENT 1

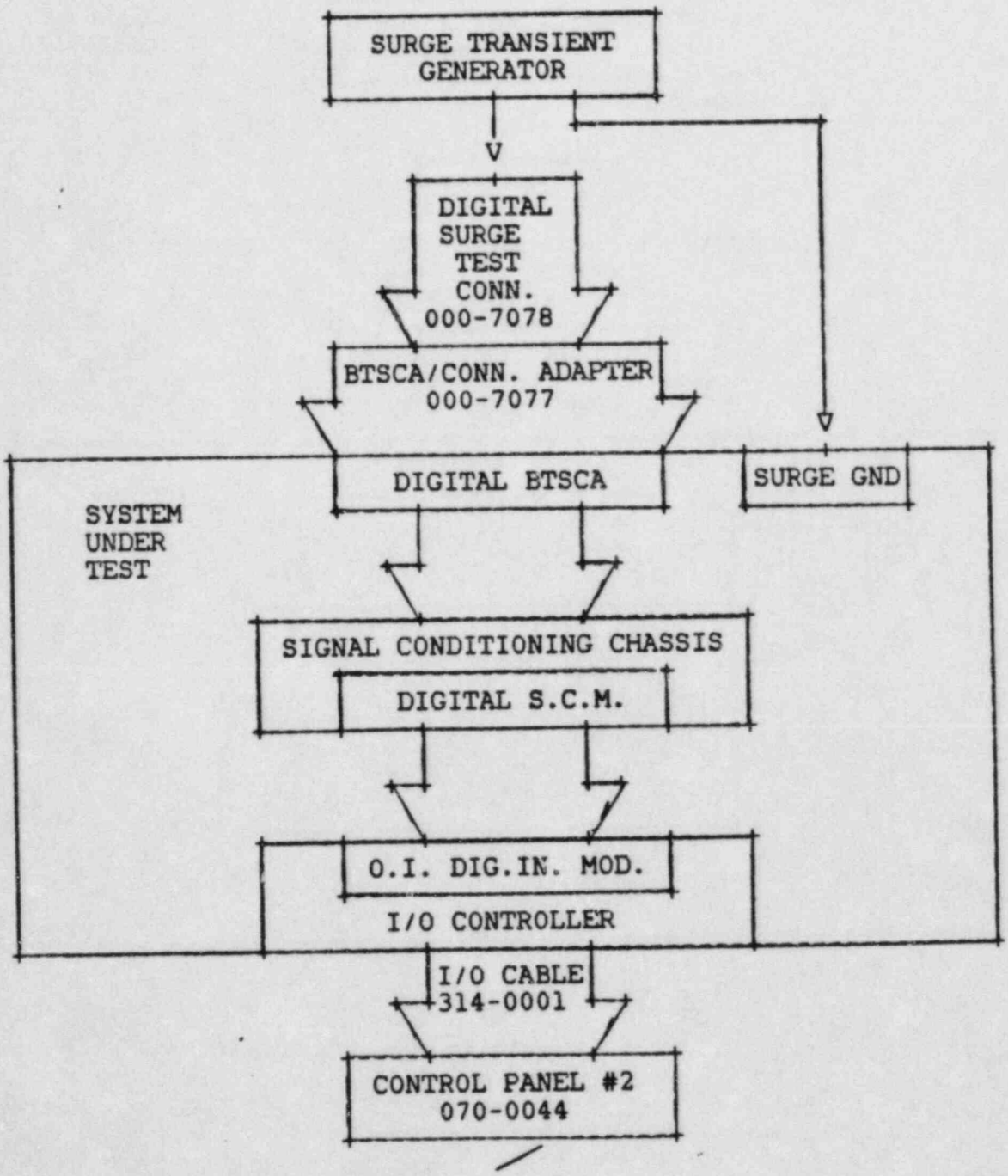
TEST CONFIGURATION DRAWINGS

The following figures are drawings depicting the configuration of test equipment used to perform the different sections of the procedure.



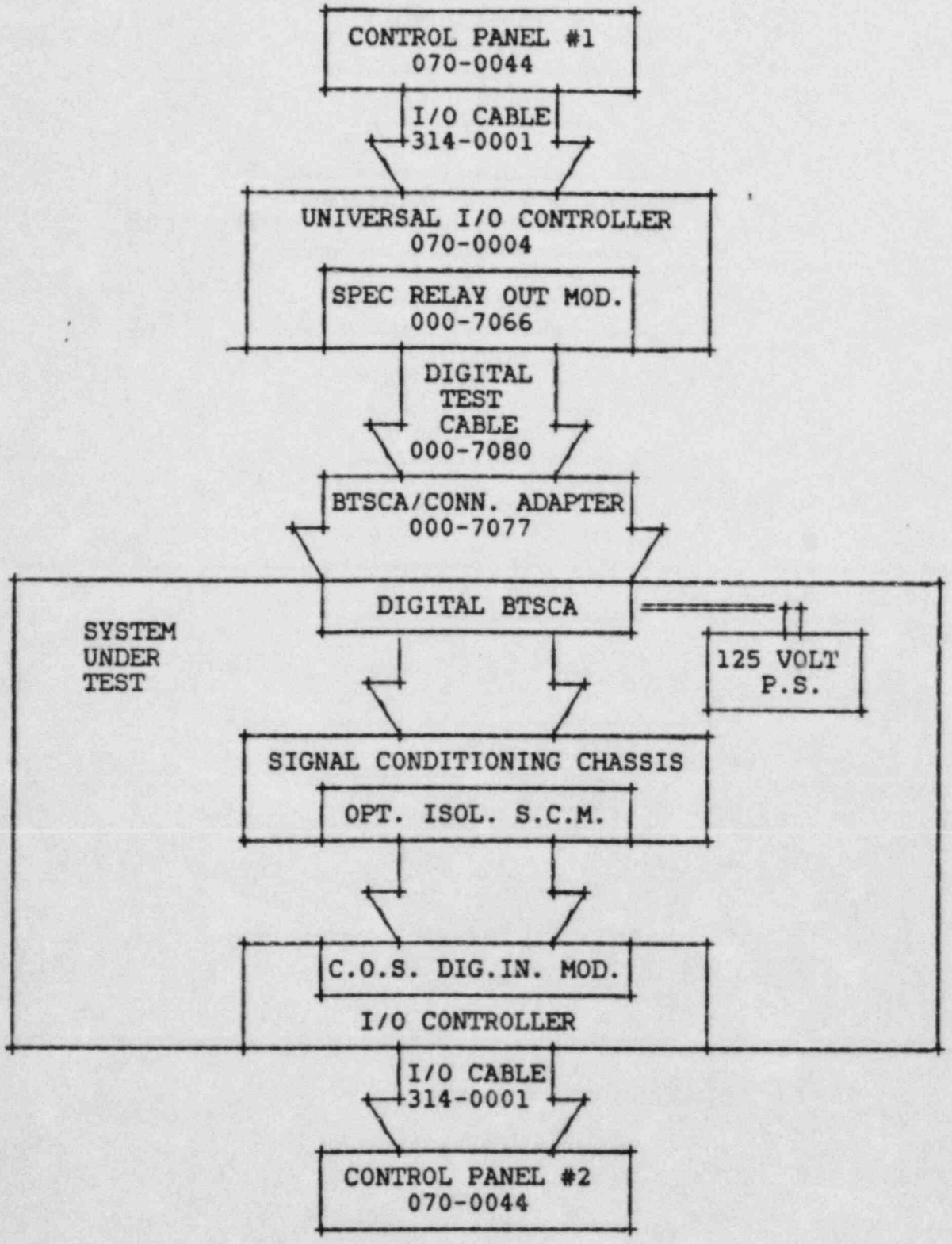
OPTICALLY ISOLATED DIGITAL INPUT VALIDATION

FIGURE 1



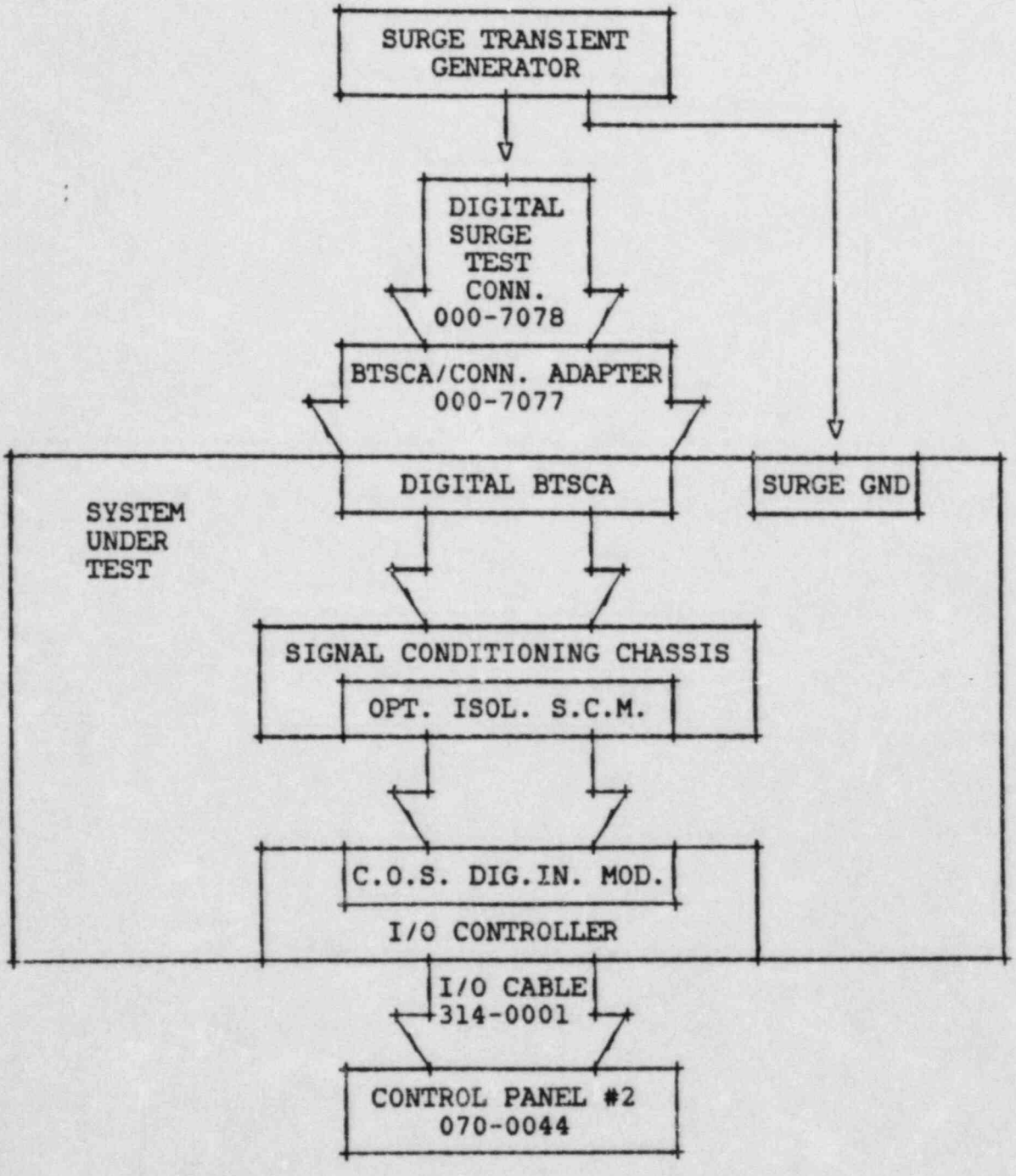
OPTICALLY ISOLATED DIGITAL INPUT
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 2



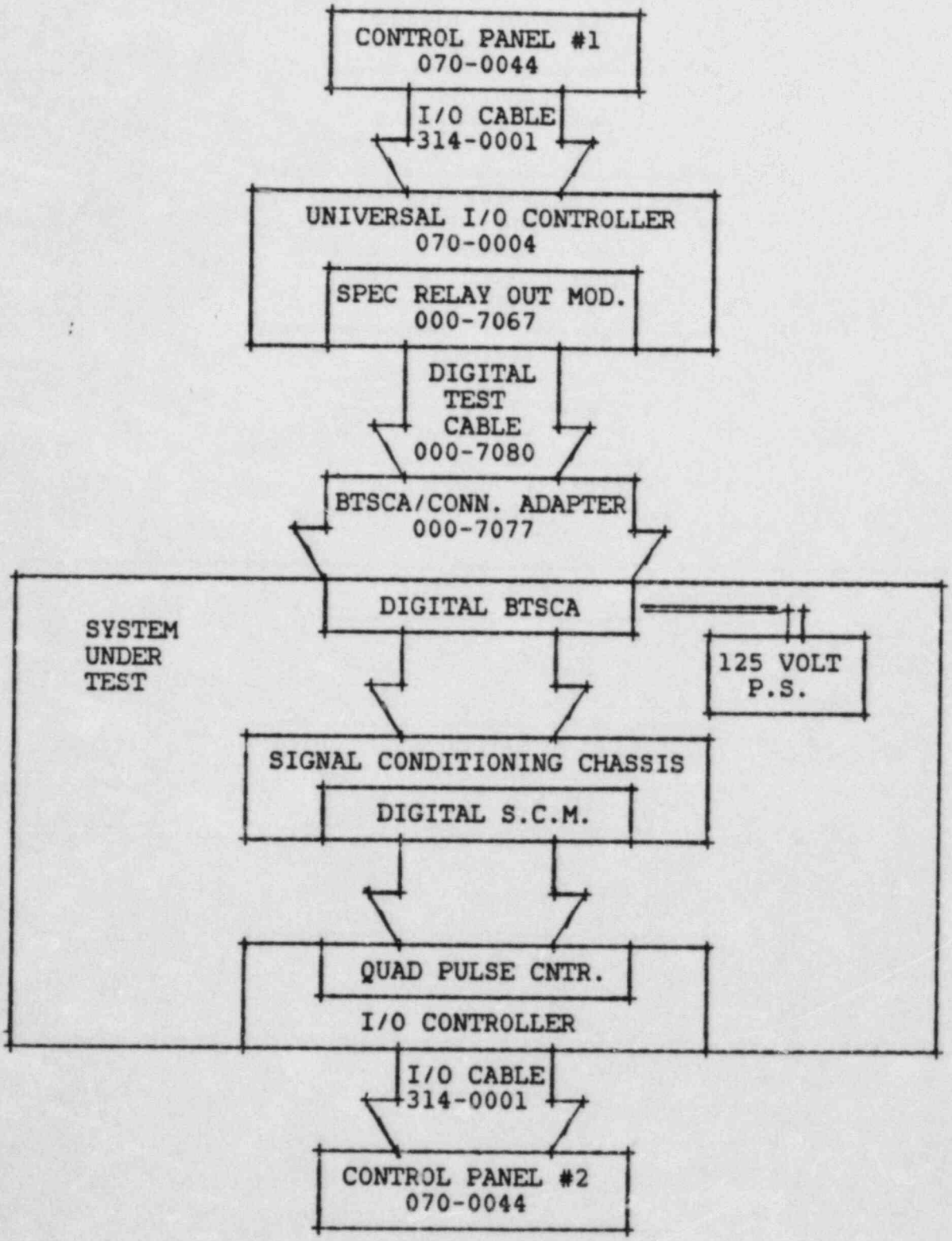
CHANGE OF STATE DIGITAL INPUT VALIDATION

FIGURE 3



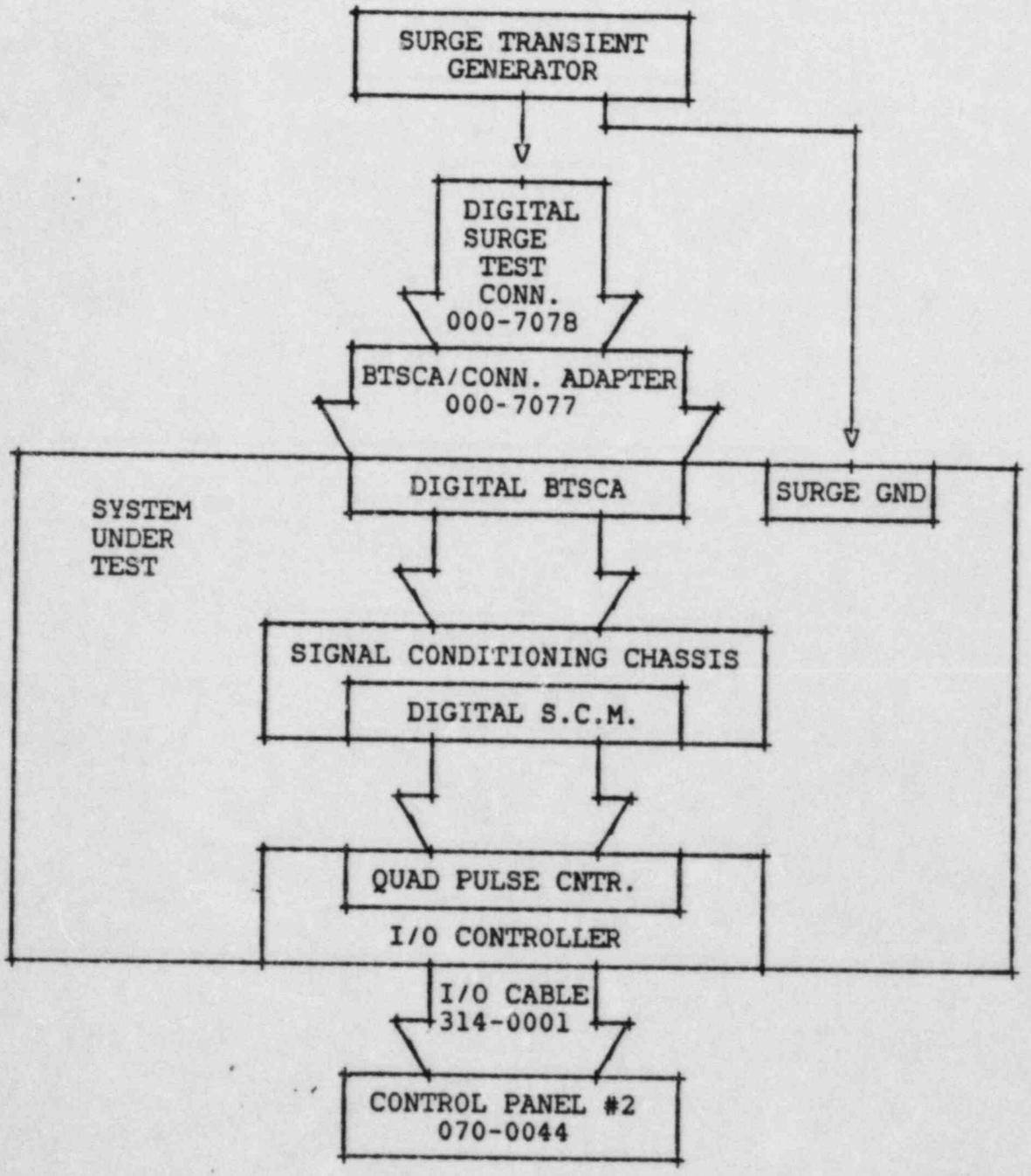
CHANGE OF STATE DIGITAL INPUT
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 4



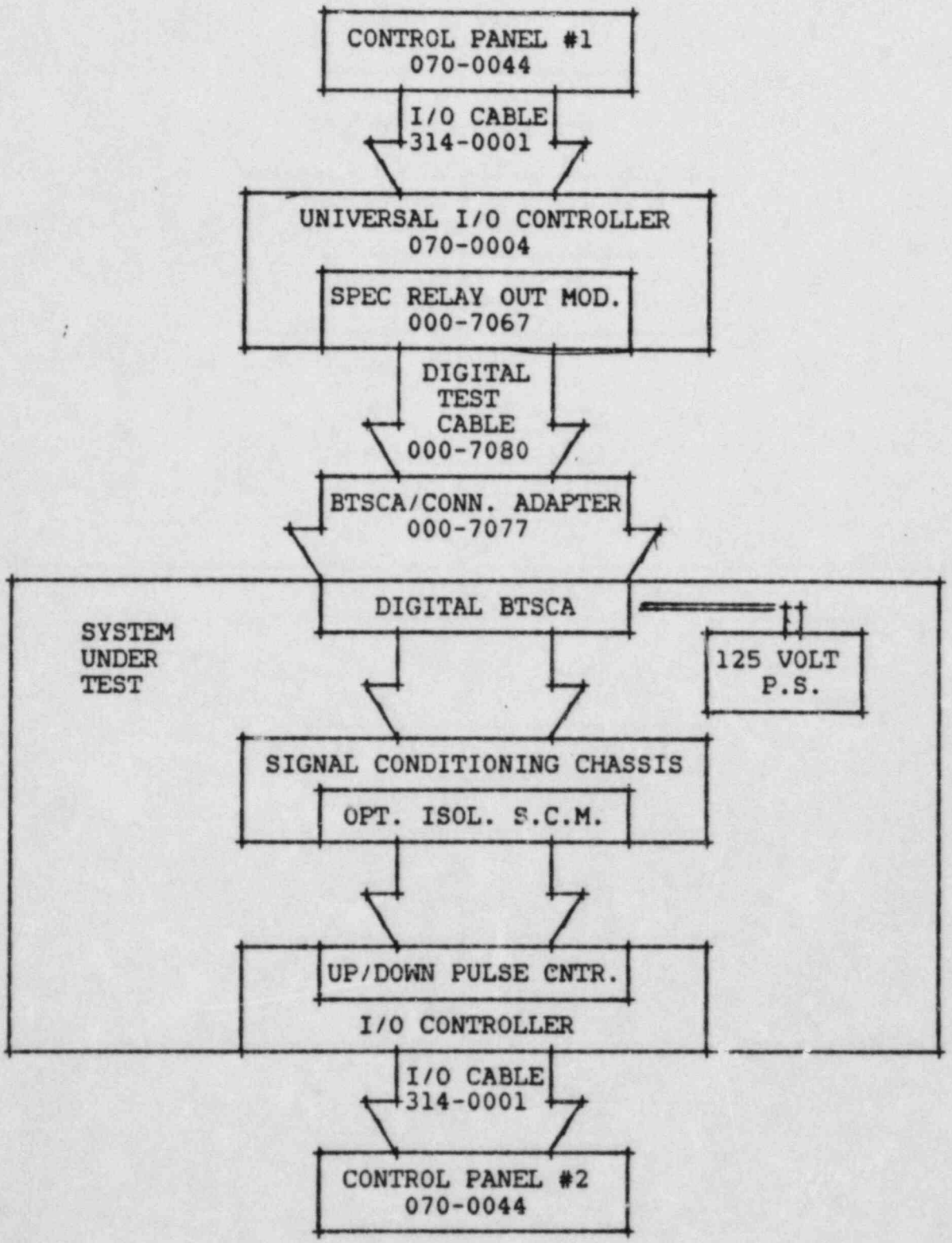
QUAD PULSE COUNTER VALIDATION

FIGURE 5



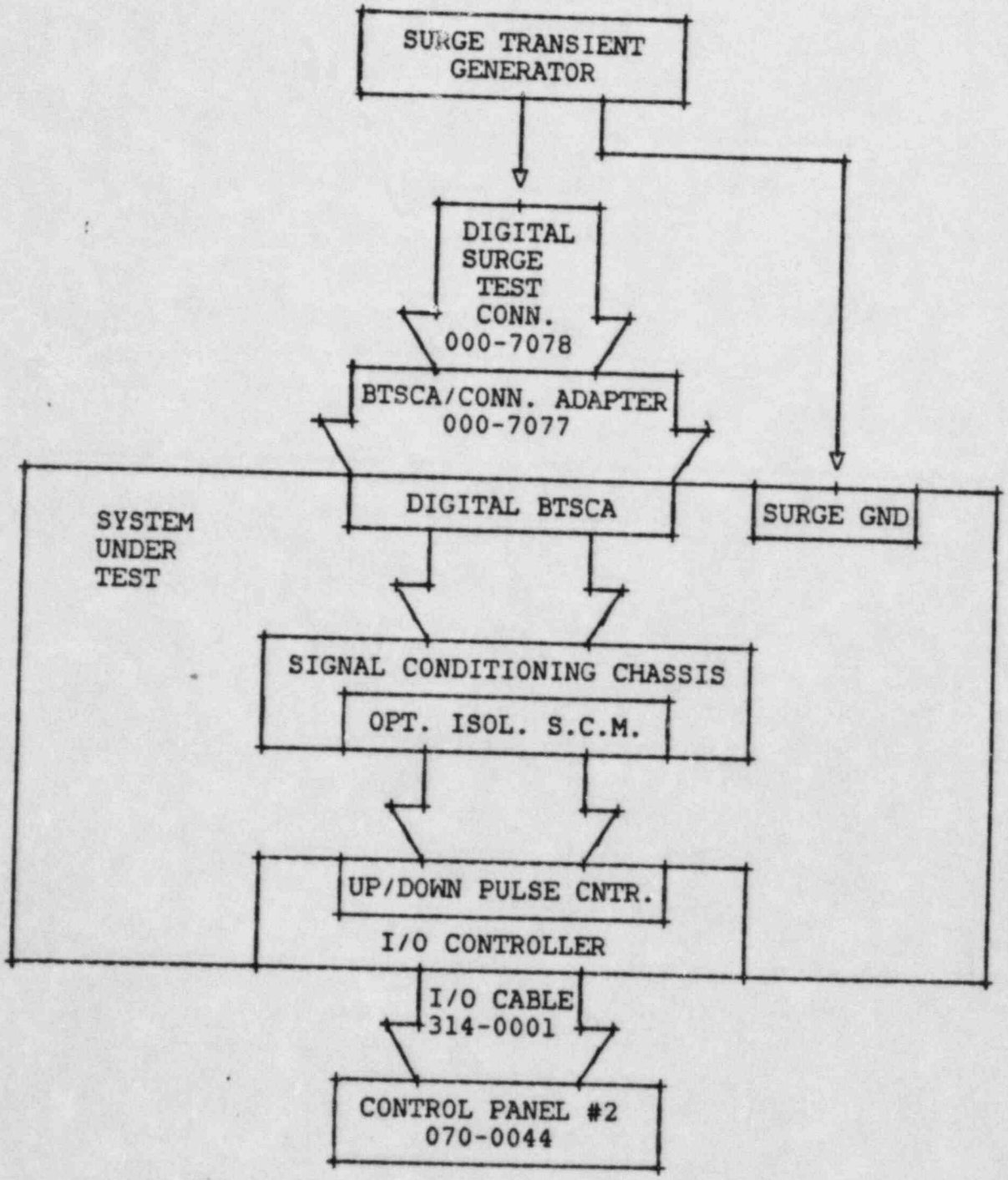
QUAD PULSE COUNTER
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 6



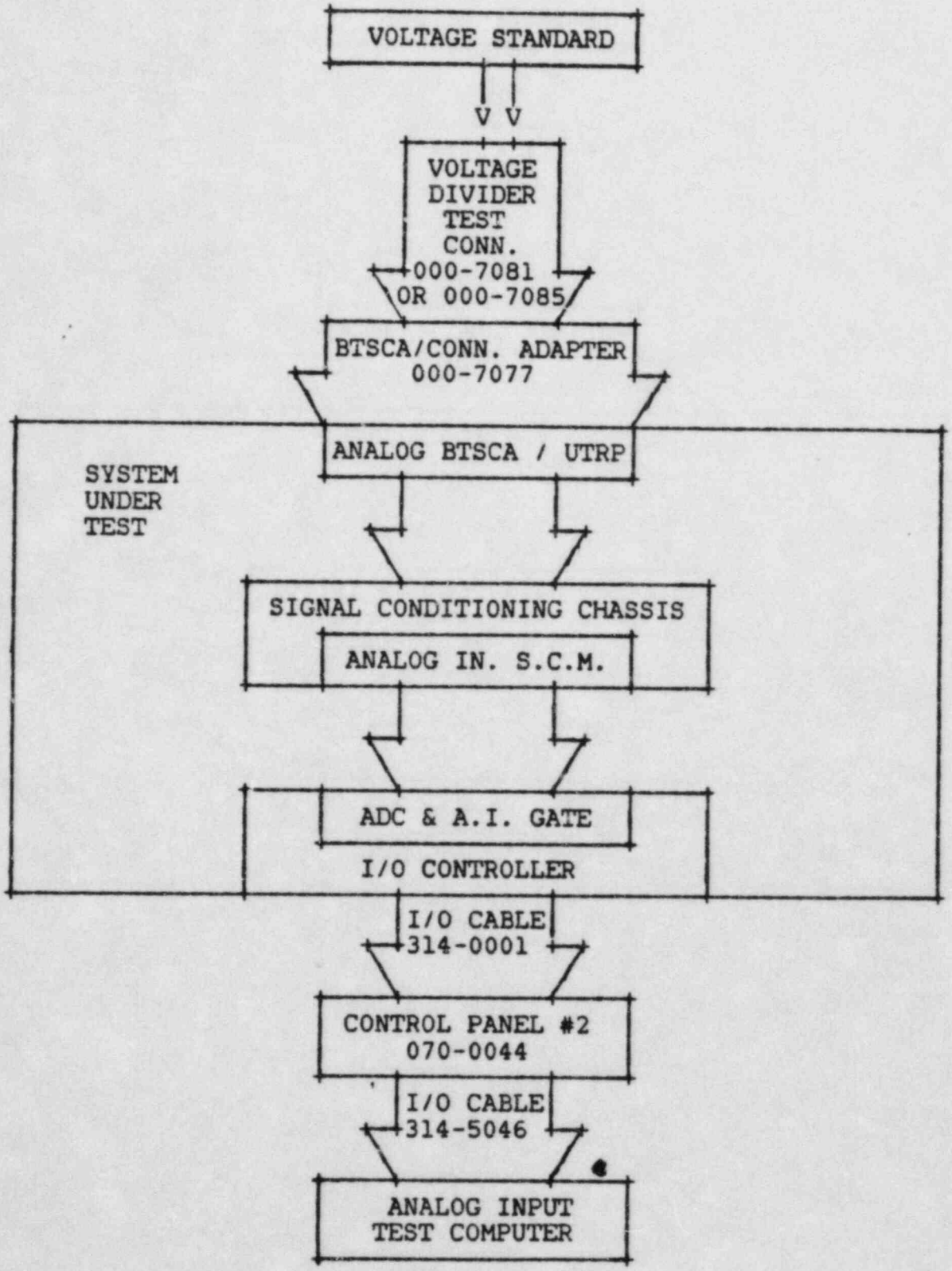
UP/DOWN PULSE COUNTER VALIDATION

FIGURE 7



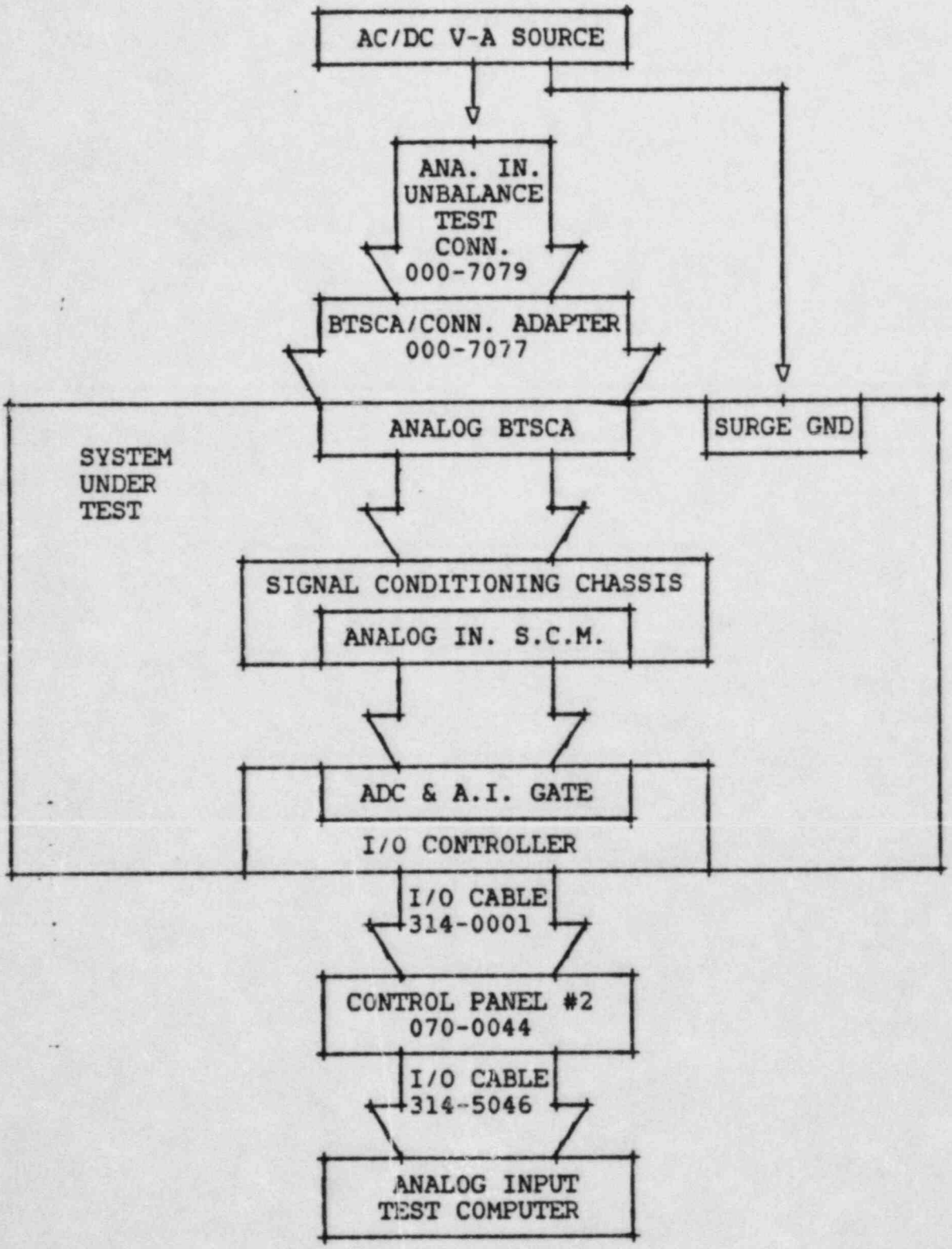
UP/DOWN PULSE COUNTER
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 8



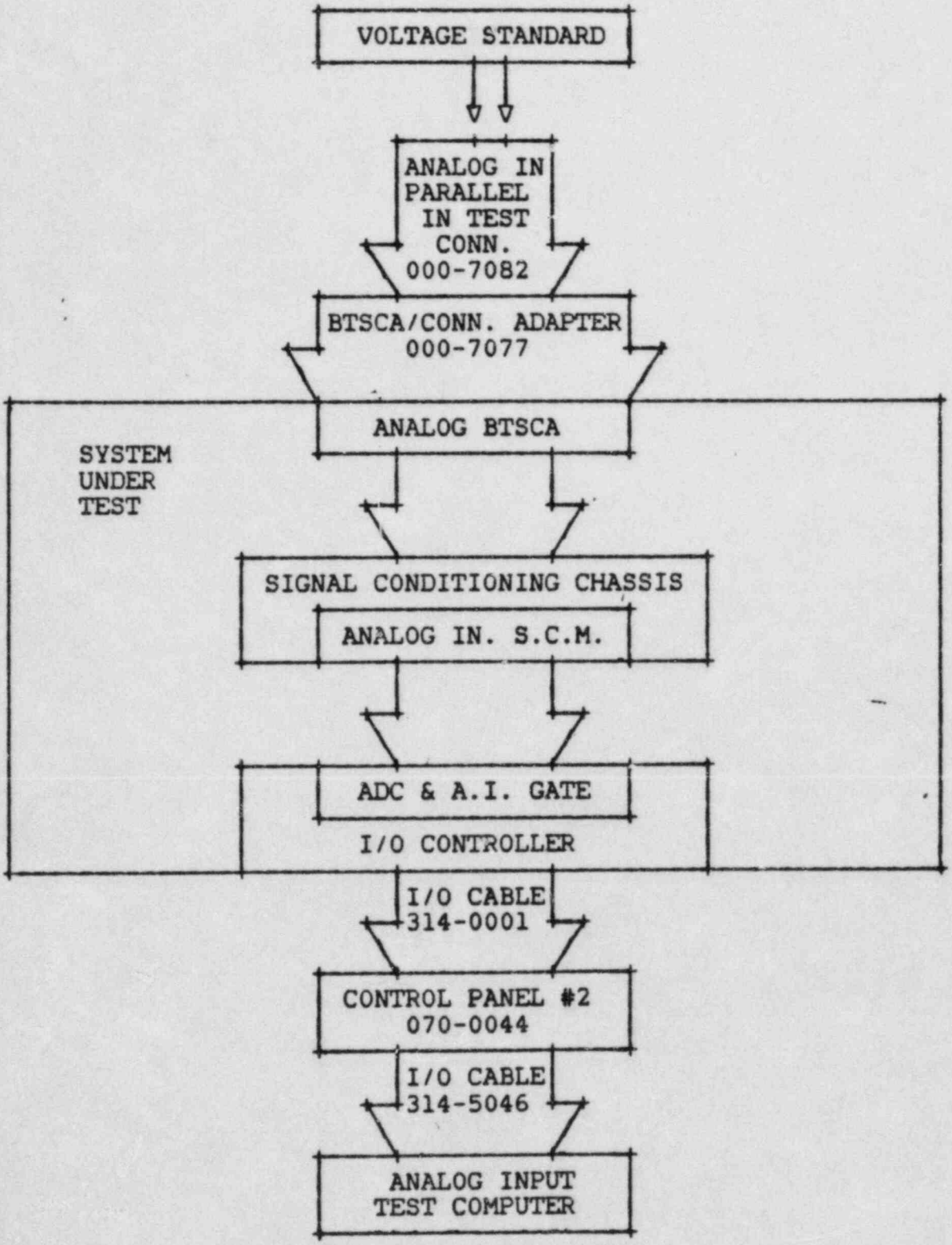
VOLTAGE SENSING ANALOG INPUT GATE VALIDATION

FIGURE 9



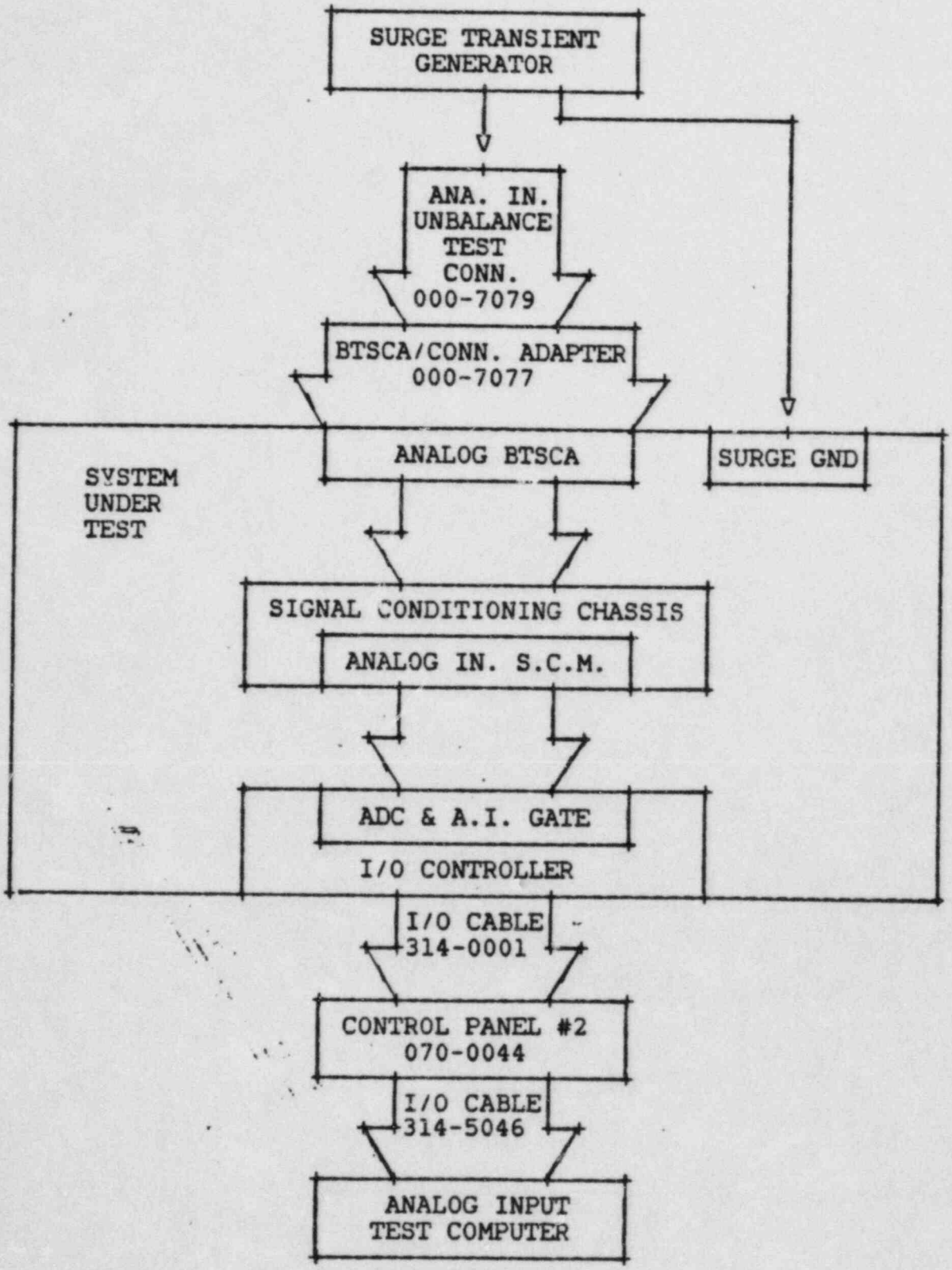
VOLTAGE SENSING ANALOG INPUT
COMMON MODE REJECTION VALIDATION

FIGURE 10



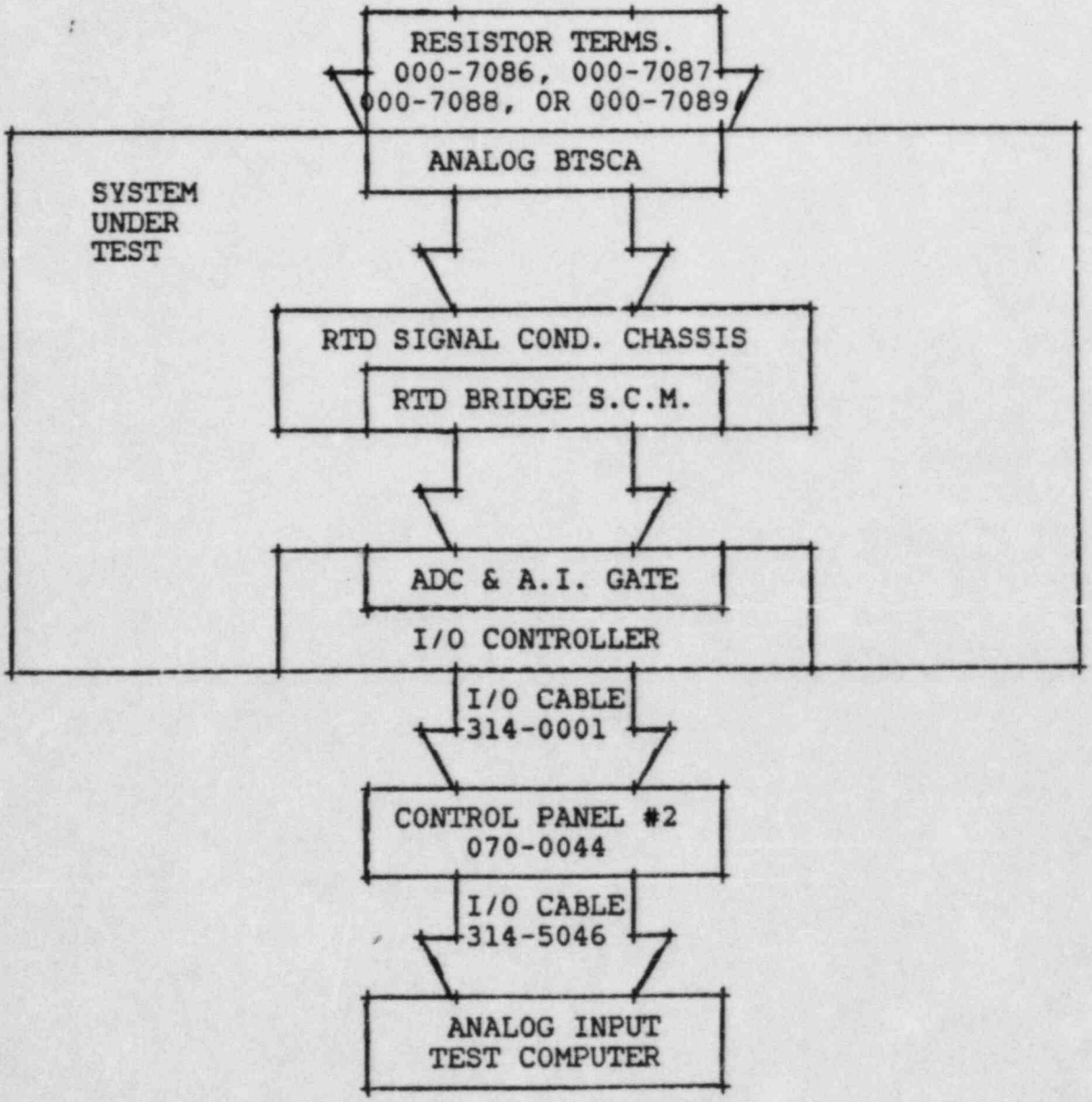
VOLTAGE SENSING ANALOG INPUT
ACCURACY VALIDATION

FIGURE 11



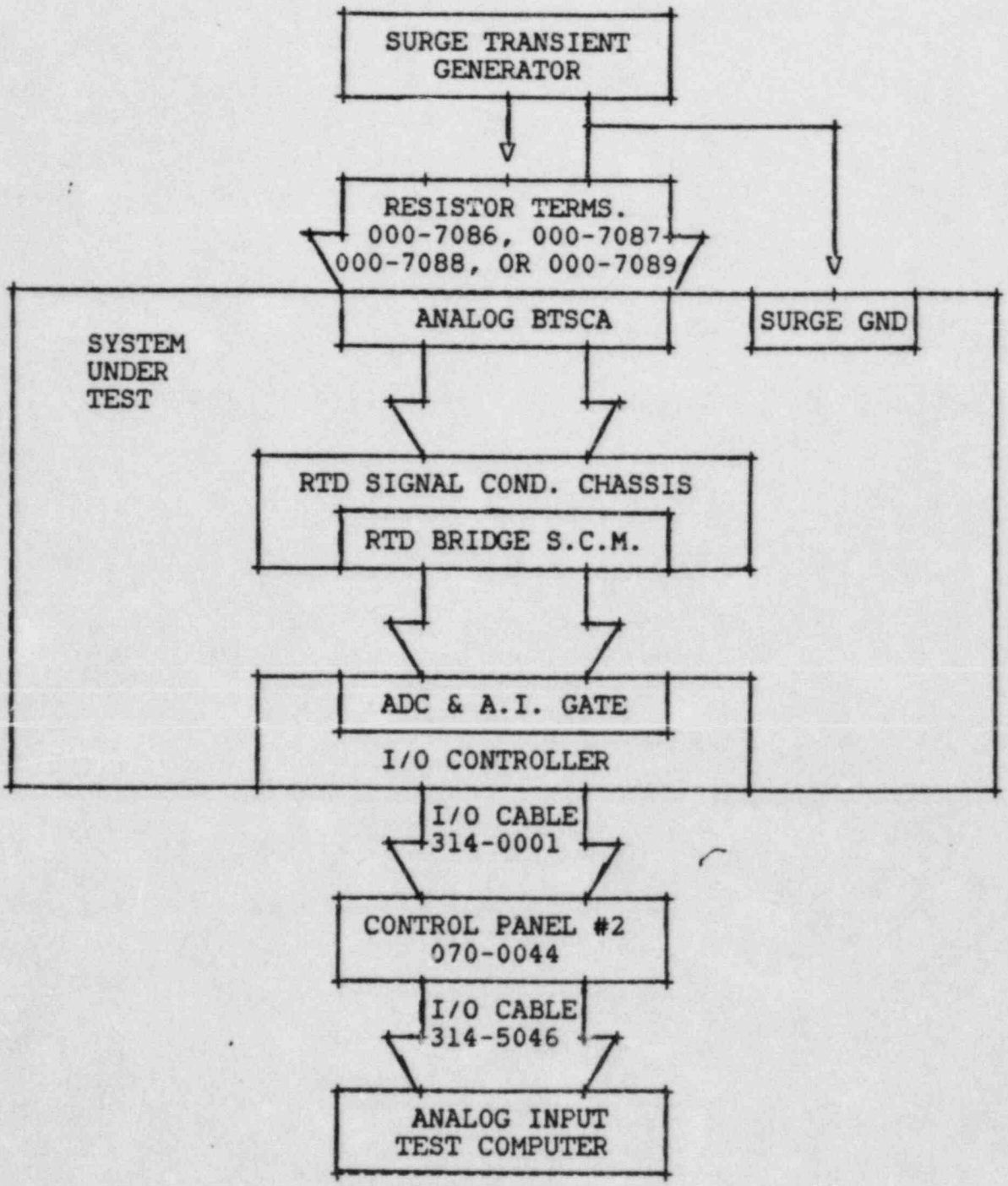
VOLTAGE SENSING ANALOG INPUT
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 12



RESISTIVE SENSING ANALOG INPUT VALIDATION

FIGURE 13



RESISTIVE SENSING ANALOG INPUT
SURGE WITHSTAND CAPABILITY VALIDATION

FIGURE 14

ATTACHMENT 2

CABINET CONFIGURATION DRAWINGS

(TO BE SUPPLIED PRIOR TO TESTING)

DRAWING CHANGE NOTICE

BALTIMORE GAS & ELECTRIC CO.

PLANT *Calvert Cliffs Unit 1 & 2*

DCN NO. 60277-2 SH 2 OF 3

DRAWN / DATE / DESIGNED / CHECKED / DATE
MTN/10-19-84/MTN/PNE/10-31-84

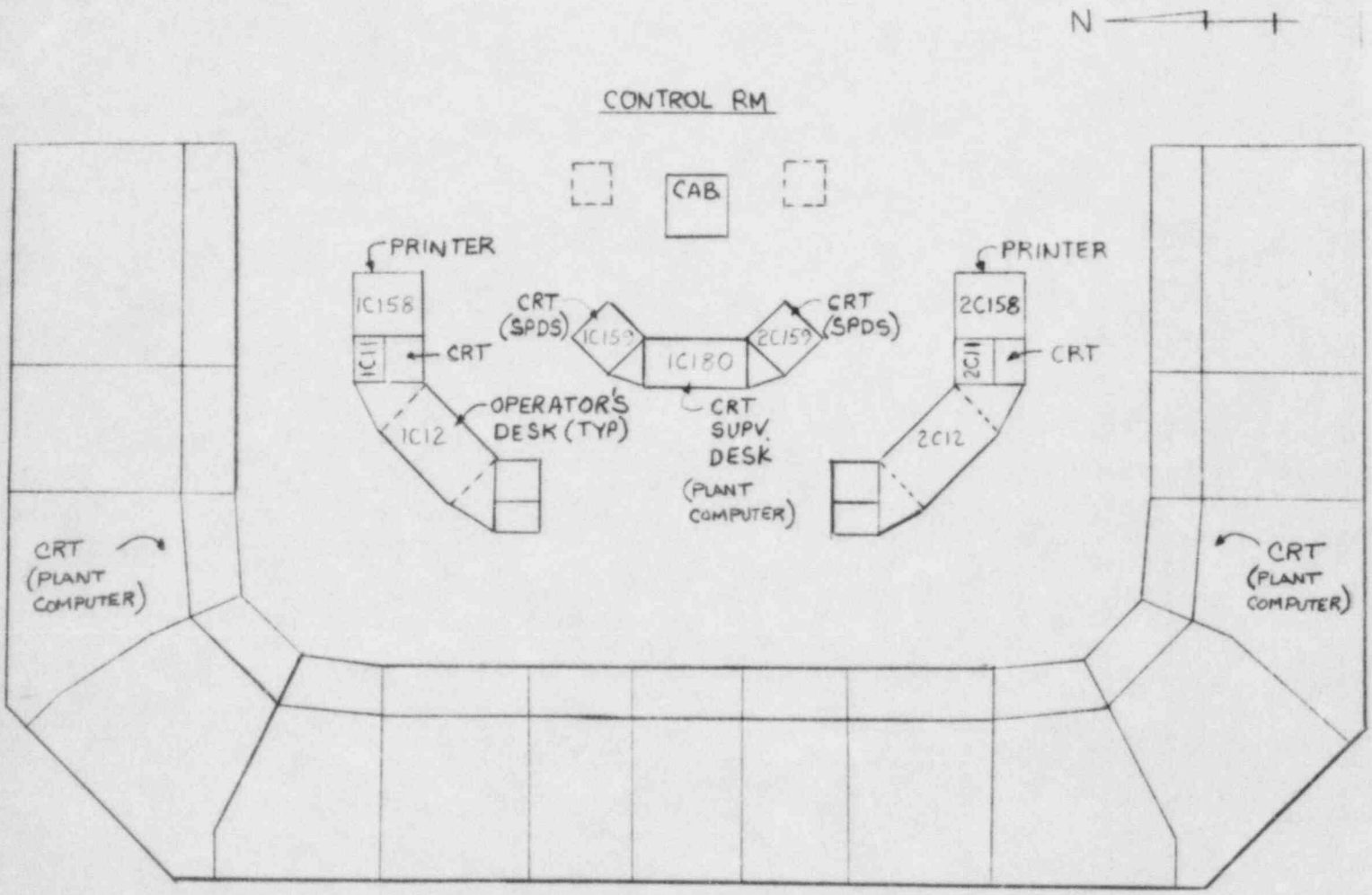
APPROVED
D & D THFRAN2 RE MTN PE/CE WP

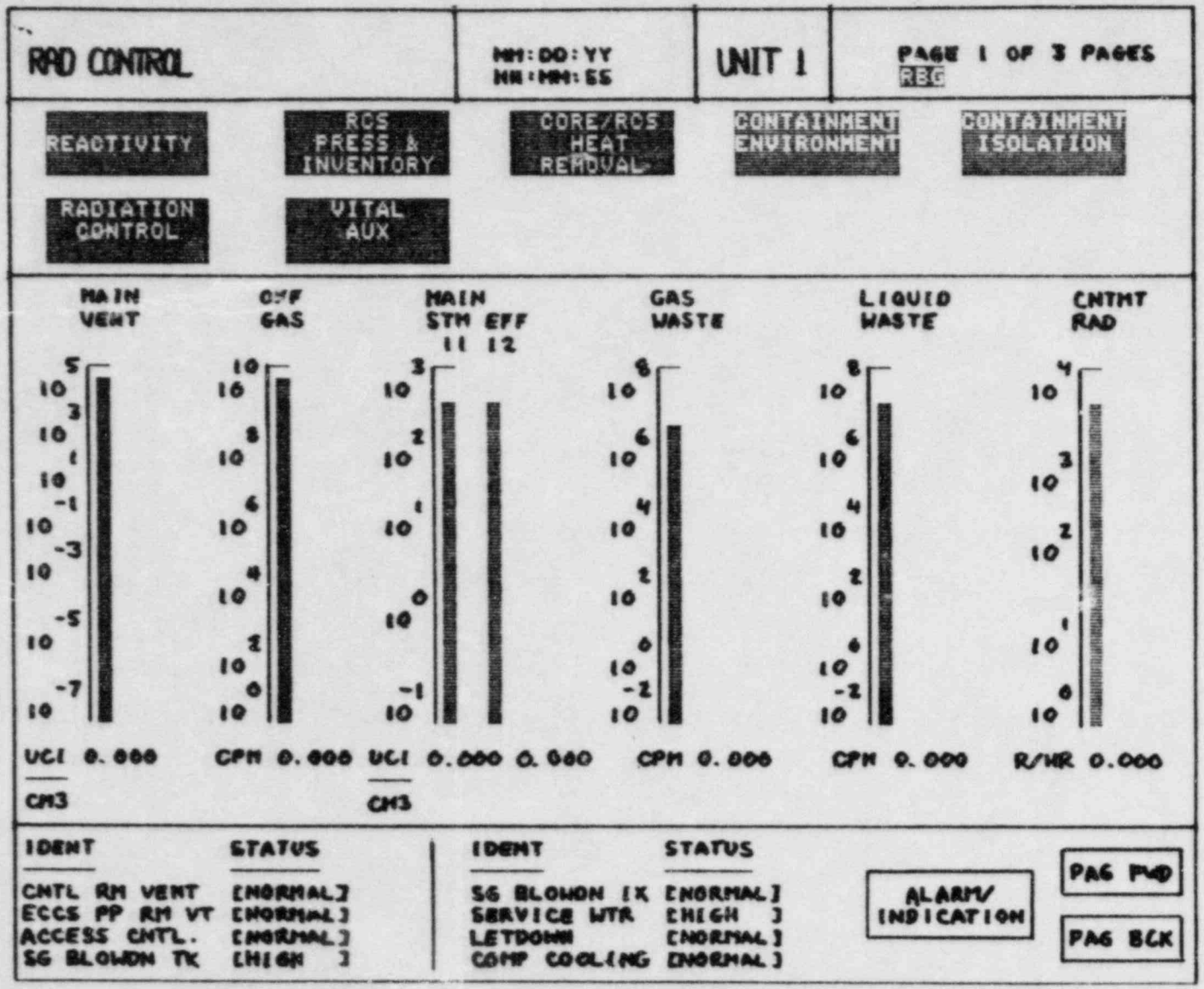
REASON FOR CHANGE

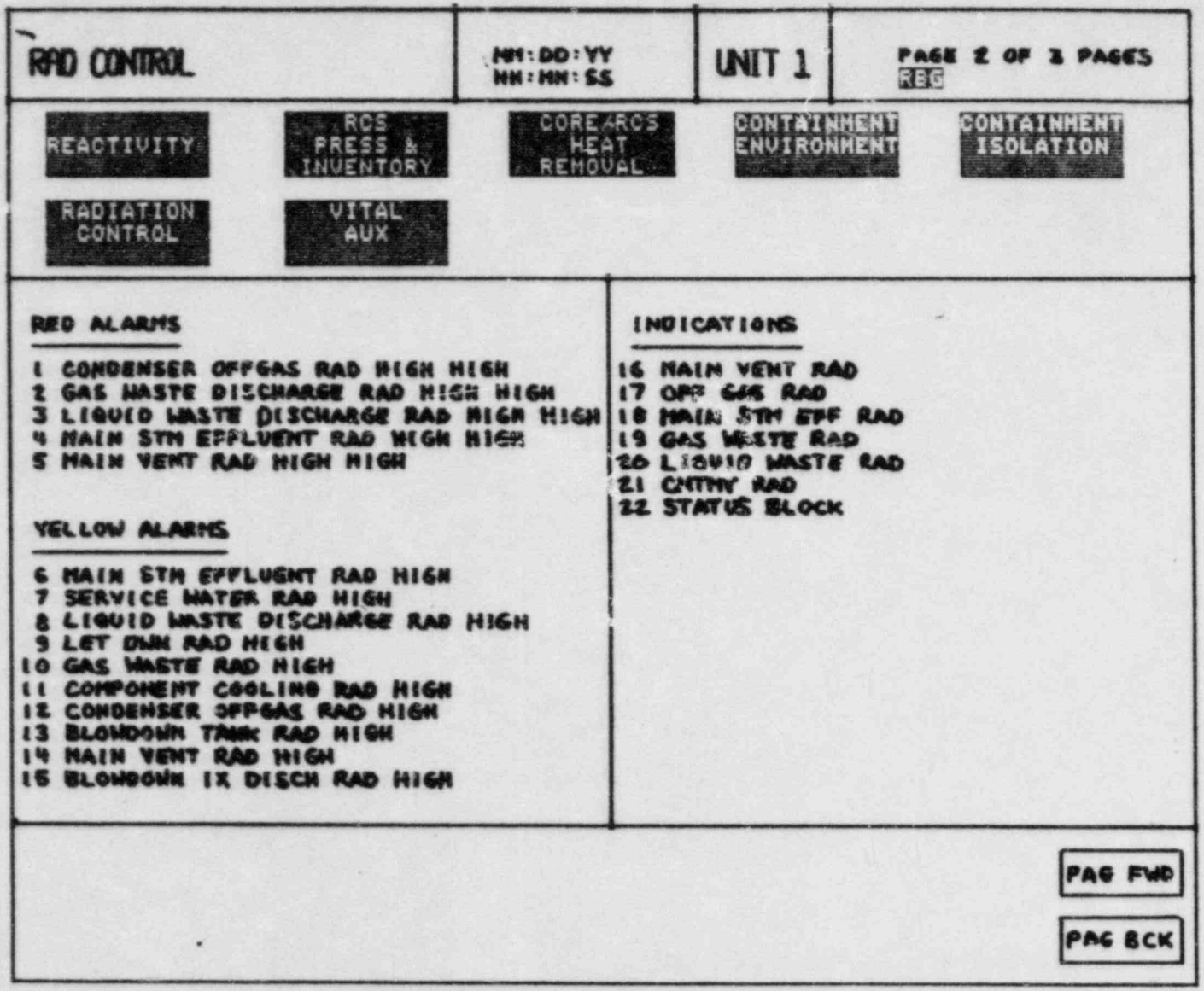
INSTLN OF PLANT COMPUTER

IN ACCORDANCE WITH FCR NO. 83-1029

USE WITH DWG. 60-277-E REV. 12




RAD CONTROL
MM:DD:YY
HH:MM:SS
UNIT 1
PAGE 1 OF 3 PAGES
REG
REACTIVITY
RCS PRESS & INVENTORY
CORE/RCS HEAT REMOVAL
CONTAINMENT ENVIRONMENT
CONTAINMENT ISOLATION
RADIATION CONTROL
VITAL AUX
MAIN VENT
OFF GAS
MAIN STM EFF
11 12
GAS WASTE
LIQUID WASTE
CNTMT RAD
UCI 0.000
CPM 0.000
UCI 0.000 0.000
CPM 0.000
CPM 0.000
R/HR 0.000
CM3
CM3
IDENT
STATUS
CNTL RM VENT [NORMAL]
ECCS PP RM VT [NORMAL]
ACCESS CNTL. [NORMAL]
SG BLOWDN TK [HIGH]
IDENT
STATUS
SG BLOWDN TK [NORMAL]
SERVICE WTR [HIGH]
LETDOWN [NORMAL]
COMP COOLING [NORMAL]
ALARM/ INDICATION
PAG FWD
PAG BCK


RAD CONTROL
MM:DD:YY
HH:MM:SS
UNIT 1
PAGE 2 OF 3 PAGES
REG
REACTIVITY
RCS PRESS & INVENTORY
CORE/RCS HEAT REMOVAL
CONTAINMENT ENVIRONMENT
CONTAINMENT ISOLATION
RADIATION CONTROL
VITAL AUX
RED ALARMS
1 CONDENSER OFFGAS RAD HIGH HIGH
2 GAS WASTE DISCHARGE RAD HIGH HIGH
3 LIQUID WASTE DISCHARGE RAD HIGH HIGH
4 MAIN STM EFFLUENT RAD HIGH HIGH
5 MAIN VENT RAD HIGH HIGH
YELLOW ALARMS
6 MAIN STM EFFLUENT RAD HIGH
7 SERVICE WATER RAD HIGH
8 LIQUID WASTE DISCHARGE RAD HIGH
9 LET DWN RAD HIGH
10 GAS WASTE RAD HIGH
11 COMPONENT COOLING RAD HIGH
12 CONDENSER OFFGAS RAD HIGH
13 BLOWDOWN TANK RAD HIGH
14 MAIN VENT RAD HIGH
15 BLOWDOWN IX DISCH RAD HIGH
INDICATIONS
16 MAIN VENT RAD
17 OFF GAS RAD
18 MAIN STM EFF RAD
19 GAS WASTE RAD
20 LIQUID WASTE RAD
21 CNTMT RAD
22 STATUS BLOCK
PAG FWD
PAG BCK

SAFETY FUNCTION STATUS CHECK BASES
REACTOR TRIP
Figure 4-9a

The safety functions listed below and their respective criteria are those used to confirm the adequacy of the RT Guideline in mitigating the event.

SAFETY FUNCTION	ACCEPTANCE CRITERIA	INDICATION	RANGE	BASES
Reactivity Control	Reactor Power Decreasing and [Negative Startup Rate] and Not more than 1 CEA Bottom Light Not Lit or Borated per Tech Specs	Power Range Power Rate CEA Status Display	[0-125%] [-1 → 7 dpm] On/Off Light for each CEA	For all emergency events, the reactor must be shutdown. The criteria that no more than one CEA be stuck out or the RCS be borated observes typical Technical Specification requirements.
Maintenance of Vital Auxiliaries (AC & DC Power)	[<----------Plant Specific---------->			
RCS Inventory Control	[35"] ≤ Pressurizer Level ≤ [245"] and Charging and Letdown are being operated manually or automatically to maintain or restore pressurizer level and RCS ≥ [20°F] Subcooled and [No reactor vessel voiding as indicated by the RVLMS]	Pressurizer Level [RVLMS]	[0"-350"] [0-100%]	A value of [245"] ([70%] of range) was chosen as an upper limit for pressurizer level to account for instrument inaccuracies and other uncertainties. A value of [35"] ([10%] of range) was chosen as a lower limit to account for instrument inaccuracy. A [20°F] subcooling margin coexisting with a pressurizer level in the range [35" to 245"] indicates adequate RCS inventory control via a saturated bubble in the pressurizer.

SAFETY FUNCTION STATUS CHECK BASES
REACTOR TRIP
Figure 4-9b

The safety functions listed below and their respective criteria are those used to confirm the adequacy of the RT Guideline in mitigating the event.

SAFETY FUNCTION	ACCEPTANCE CRITERIA	INDICATION	RANGE	BASES
RCS Inventory Control (Cont'd)				An uncomplicated reactor trip should not result in reactor vessel voiding.
RCS Pressure Control	[1700 psia] < Pressurizer Pressure < [2350 psia] and Pressurizer heaters and spray are being operated manually or automatically to maintain or restore pressurizer pressure to within the limits of the P/T curves, Figure 4-1.	Pressurizer Pressure	[1500-2500 psia]/ [0-1600 psia]	[1700 psia] corresponds to the SIAS alarm setpoint. [2350 psia] is the high pressure alarm setpoint. Best estimate analysis shows that the selected events will fall within the above range.
Core Heat Removal	$T_H - T_C$ < [10°F] and RCS ≥ [20°F] subcooled	T_H T_C [Subcooled Margin Monitor]	[520°-610°F] [0°-600°F] [0°-100°F]	Best estimate analysis demonstrates that S/G ΔT will be less than [10°F] in the steaming loop with RCPs running and at least one S/G steaming. [20°F] subcooled margin is based on engineering judgement to assure adequate core cooling accounting for temperature variations in the RCS. Best Estimate analysis shows that the noted events will fall in the selected ranges.

SAFETY FUNCTION STATUS CHECK BASES
REACTOR TRIP
Figure 4-9c

The safety functions listed below and their respective criteria are those used to confirm the adequacy of the RT Guideline in mitigating the event.

SAFETY FUNCTION	ACCEPTANCE CRITERIA	INDICATION	RANGE	BASES
RCS Heat Removal	a) At least one S/G has level: i) within the normal level band with feedwater available to maintain the level or ii) being restored by a feedwater flow > [150 gpm] and b) RCS T_{ave} is < [545°F]	Steam Generator Level	[+63.5" - (-)116.5"]	Decay heat levels may not be high enough to require a feedwater flow of [150 gpm]. If this is the case, once steam generator level is returned to the zero power level band and feedwater remains available to maintain that level, then RCS heat removal is being satisfied. [545°F] is based on control program for atmospheric dump valves and turbine bypass valves, and best estimate analysis.
Containment Isolation	Containment Pressure < [1.5 psig]	Containment Pressure	[0-60 psig] [0-15 psig]	[1.5 psig] is based on the containment pressure alarm. It is not expected, for the selected events, that containment pressure will increase to the alarm setpoint.
	and			
	No Containment Area Radiation Monitors Alarming	Containment Area Radiation Monitors	Alarming - Not Alarming	During an uncomplicated reactor trip there should be no radiation in containment. The indicators should not be alarming.
	and			
	No Steam Plant Activity Monitors Alarming	Steam Plant Radiation Monitors	Alarming - Not Alarming	Steam plant activity is an indication of an SGTR and is not anticipated for a RT.

SAFETY FUNCTION STATUS CHECK BASES
REACTOR TRIP
Figure 4-9d

The safety functions listed below and their respective criteria are those used to confirm the adequacy of the RT Guideline in mitigating the event.

SAFETY FUNCTION	ACCEPTANCE CRITERIA	INDICATION	RANGE	BASES
Containment Temperature and Pressure Control	Containment Pressure < [1.5 psig]	Containment Pressure	[0-60 psig] [0-15 psig]	[1.5 psig] is based on the containment pressure alarm. It is not expected, for the selected events, that containment pressure will increase to the alarm setpoint.
	and			
	Containment Temperature < [120°F]	Containment Temperature	[50°-300°F]	Maximum normal expected average containment air temperature.
Containment Combustible Gas Control	H_2 < [2%]	[<----------Plant Specific----------]		