SOUTHERN CALIFORNIA EDISON, SAN ONOFRE
NUCLEAR GENERATING STATION 2 (SONGS 2)

DOCKET 50-361

CEN-269(S)-NP
REVISION 02-NP

CPC/CEAC SYSTEM
PHASE II SOFTWARE VERIFICATION
TEST REPORT

NOVEMBER 1984

COMBUSTION ENGINEERING, INC.
Nuclear Power Systems
Power Systems Group
Windsor, Connecticut

LEGAL NOTICE

THIS RESPONSE WAS PREPARED AS AN ACCOUNT OF WORK SPONSORED BY COMBUSTION ENGINEERING, INC. NEITHER COMBUSTION ENGINEERING NOR ANY PERSON ACTING ON ITS BEHALF:

a. MAKES ANY WARRANTY OR REPRESENTATION, EXPRESS OR IMPLIED INCLUDING THE WARRANTIES OF FITNESS FOR A PARTICULAR PURPOSE OR MERCHANTABILITY, WITH RESPECT TO THE ACCURACY, COMPLETENESS, OR USEFULNESS OF THE INFORMATION CONTAINED IN THIS RESPONSE, OR THAT THE USE OF THE INFORMATION CONTAINED IN THIS RESPONSE, OR THAT THE USE OF ANY INFORMATION, APPARATUS, METHOD, OR PROCESS DISCLOSED IN THIS RESPONSE, OR THAT THE USE OF ANY INFORMATION, APPARATUS, METHOD, OR PROCESS DISCLOSED IN THIS RESPONSE MAY NOT INFRINGE PRIVATELY OWNED RIGHTS; OR

b. ASSUMES ANY LIABILITIES WITH RESPECT TO THE USE OF, OR FOR DAMAGES RESULTING FROM THE USE OF, ANY INFORMATION, APPARATUS, METHOD OR PROCESS DISCLOSED IN THIS RESPONSE.

ABSTRACT

Phase II Testing is performed on the CPC/CEAC System to (1) verify that the CPC and CEAC software modifications have been properly integrated with the CPC and CEAC software and system hardware and (2) provide confirmation that the static and dynamic operation of the integrated system as modified is consistent with that predicted by design analyses, which provide design inputs to CPC/CEAC Functional Design Specifications.

This report presents the Phase II test results for the San Onofre Nuclear Generating Station Unit 2 Plant CPC/CEAC Revision 03 software. This revision is applicable to SONGS-2 Cycle 2.

The Phase II Software Verification Tests have been performed as required in Reference 1. In all cases, the test results fell within the acceptance criteria, or are explained. The test results are that both the CPC and CEAC software have no indication of software error and that the operation of the integrated system is consistent with the performance predicted by design analyses.

TABLE OF CONTENTS

1.0 INTRODUCTION

The verification of software modifications of the CPC/CEAC System consists of several steps which address two major areas of the modification process:

(1) Definition of software modifications
(2) Implementation of software modifications

The definition of software modifications is documented in the Software Change Procedure (Reference 1), CPC and CEAC Functional Design Specifications (References 2 & 3), and the Data Base Listing, (Reference 4), and is verified by design analyses contained in recorded calculations. The implementation of software modifications is documented in Software Design Specifications and program listings.

The verification process for the modified software implementation is two-phase: Phase I testing (Reference 5), must be performed before Phase II. Successful Completion of Phase I Testing verifies the correct implementation of the modified software. Phase II testing completes the software modification process by validating that the integrated CPC System responds as expected.

This document contains the test results and conclusions for the Phase II software verification test.

1.1 Objectives

The primary objective of Phase II Testing is to validate that the CPC and CEAC software modifications have been properly integrated with the CPC and CEAC software and system hardware. In addition, Phase II testing provides confirmation that the static and dynamic operation of the integrated system as modified is consistent with that predicted by design analyses. These objectives are achieved by

comparing the response of the integrated system to the response predicted by the CPC/CEAC FORTRAN Simulation Code. This comparison is performed for a selected set of simulated static and dynamic input conditions.

1.2 Description of Phase II Testing

Phase II testing consists of the following tests:

(1) Input Sweep Tests for the CPC and the CEAC,
(2) Dynamic Software Verification Test, and
(3) Live Input Single Parameter Test.

These tests are performed on a Single Channel Test Facility (SCTF) of the CPC/CEAC System with integrated software that has undergone successful Phase I testing. (Reference 5)

1.3 Applicability

This report applies to the Phase II Testing performed on the Southern California Edison (SCE), San Onofre Nuclear Generating Station 2 (SONGS-2) CPC/CEAC System Software. The software revisions documented in this report are designated as Revision 03 to the SONGS-2 CPC/CEAC System Software. This revision is applicable to SONGS-2 Cycle 2.

2.0 CPC/CEAC INPUT SWEEP TESTS

The Input Sweep Test is a real-time exercise of the CEAC and CPC application software and executive software with steady-state CPC and CEAC input values read from a storage device. These tests have the following objectives:

(1) To determine the processing uncertainties that are inherent in the CPC and CEAC designs;

(2) To verify the ability of the CPC and CEAC algorithms used in the system hardware to initialize to a steady state after an auto-restart for each of a large number of input combinations within the CPC/CEAC operating space; and

(3) To complement Phase I module testing by identifying any abnormalities in the CPC and CEAC algorithms used in the system hardware which were not previously uncovered.

2.1 CPC Input Sweep

2.1.1 CPC Input Sweep Test Case Selection

[ ] test cases, each involving different combinations of process inputs and addressable constants, were used for CPC design qualification testing of the Revision 03 software.

2.1.2 CPC Processor Uncertainty Results

For each test case, differences in the results of the FORTRAN Simulation Code and Single Channel Test Facility (SCTF) were calculated. A statistical analysis of these differences produced the processing uncertainties.

The DNBR statistics did not include those cases for which the DNBR as calculated on either system was at the limits [ ]. This is because a difference of zero (or close to zero) would be computed and would incorrectly weight the distribution of differences. A total of [ ] cases remained after these cases were eliminated. The LPD statistics did not include those cases for which the LPDDC as calculated on either system was equal to or greater than the upper limit of [ ] core average kW/ft (= [ ] kW/ft). A total of [ ] cases remained after these cases were eliminated.

Although [ ] cases were not included in the computation of DNBR and LPD statistics, respectively, they were still included as Input Sweep Test cases for the purpose of identifying potential software errors.

The processor uncertainties for DNBR and LPD are defined as the one-sided tolerance limits which encompass 95% of the distribution of DNBR and LPD differences for all test cases with a 95% confidence level. The processor uncertainties thus determined from Input Sweep for DNBR and LPD, respectively, are [ ] DNBR units, and [ ] core average kW/ft. However, since the distribution of differences is so restrictive, the maximum error may be used (that is, the limits which encompass 100% of the difference). This is more conservative and yet still results in small processor uncertainties. Thus, defined the DNBR and LPD processing uncertainties for Revision 03 of the CPC are [ ] DNBR units and [ ] core average kW/ft, respectively.

2.1.3 Analysis of CPC Input Sweep Test Results

[ ]

[ ]

The results of the test cases exceeding the 95/95 tolerance limit were analyzed for evidences of software errors. For DNBR there were [ ] cases below the lower tolerance limit of [ ] (DNBR units) and [ ] test cases above the upper tolerance limit of [ ] (DNBR units). For these [ ] test cases the difference between the SCTF and the CPC Fortran Simulation Code is within the accuracy of the two systems. The largest percent error among the [ ] cases was [ ]. These differences do not show a significant commonality since the differences are absolute (not relative) and it should be expected that the largest differences should occur at high DNBR's. It is therefore concluded that no errors are indicated in the CPC Single Channel DNBR program.

For LPD the cases examined there were [ ] cases with differences below the lower 95/95 tolerance limit of [ ] (% of core average kW/ft) and [ ] cases with differences greater than the upper tolerance limit of [ ]

The largest percent error among the [ ] cases was [ ] The common input to these test cases was found in other test cases with less maximum difference and less percent error. Examination of the inputs to all [ ] LPD cases outside the tolerance limits showed that the inputs covered a wide spectrum. No common area was found.

Therefore it is concluded that the Input Sweep test results do not indicate software errors either in the DNBR or in the LPD calculations.

2.2 CEAC Input Sweep Test

2.2.1 CEAC Input Sweep Test Case Selection

[ ] test cases, each involving different combinations of CEAC process inputs were used for CEAC design qualification testing of the Revision 03 software. These test cases covered all CEAC operating space.

2.2.2 CEAC Input Sweep Test Results

For each test case, differences between the CEAC FORTRAN Simulation Code and CEAC single channel system results were calculated. The processor uncertainties for DNBR and LPD are defined as the one sided tolerance limits which encompass 95% of the distribution of DNBR and LPD penalty factor differences for all test cases with a 95% confidence level.

The processor uncertainties for the DNBR and the LPD penalty factor differences are less than [ ] and less than [ ] respectively.

2.2.3 Analysis of CEAC Input Sweep Test Results

[

]

The SONGS-2 cycle 2 CEAC Input Sweep Test results were reviewed for evidence of computational differences between the CPC/CEAC FORTRAN Simulation Code and the SCTF. In all cases the deviation was less than [ ]. This is acceptable as an indication of the absence of software errors.

[ ]

It is therefore concluded that the CEAC Input Sweep Test results do not indicate software errors either in the DNBR or in the LPD penalty factor calculations.

3.0 DYNAMIC SOFTWARE VERIFICATION TEST

The Dynamic Software Verification Test (DSVT) is a real time exercise of the CPC application software and executive software with transient CPC input values read from a storage device. This test has two objectives:

(1) To verify that the dynamic response of the integrated CPC software is consistent with that predicted by design analyses, and

(2) To supplement design documentation quality assurance, Phase I module tests, and Input Sweep Tests in assuring correct implementation of software modifications.

Further information concerning DSVT may be found in Reference 1.

3.1 DSVT Case Selection

Test cases for DSVT are selected to exercise dynamic portions of the CPC software with emphasis on those portions of the software that have been modified.

DSVT requires that, as a minimum, cases [ ] be selected for testing Reference 1. These cases are from the Phase II test series (identified in Reference 1) and consist of a [ ]

[ ]

However, because of extensive software modifications the entire series of applicable DSVT Test cases was executed using the CPC/CEAC FORTRAN Simulation Code and the Single Channel Test Facility (SCTF) with the Rev. 03 CPC Software.

[ ]

[redacted]

3.2 Generation of DSVT Acceptance Criteria

Acceptance criteria for DSVT are defined in Reference 1 as the trip times and initial values of DNBR and LPD for each test case. These Acceptance Criteria are generated using the certified CPC/CEAC FORTRAN Simulation Code and the Data Base Listing for SONGS-2. Processing uncertainties obtained during Input Sweep testing are factored into the acceptance criteria for initial values of DNBR and LPD where necessary. Trip times are affected by program execution lengths as well as by the processing uncertainties. The minimum, average, and maximum execution lengths (in milliseconds) calculated for the Revision 03 software are listed below.

CPC Application Program Execution Lengths

Program	Minimum (msec)	Average (msec)	Maximum (msec)
FLOW	[redacted]		
UPDATE			
POWER			
STATIC			

Each DSVT case is initially executed on the CPC/CEAC FORTRAN Simulation Code once with the nominal program execution lengths (values between the minimum and maximum) and the data base values of

trip setpoints. During this phase, it is verified that the test data executed for each test case produces the intended initialization and transient output. Once the test cases have been adjusted appropriately for the given plant and CPC/CEAC configuration, they are executed on the Single Channel Test Facility (SCTF). [ ] [ ]. The test case is executed with the CPC/CEAC FORTRAN Simulation Code once with minimum execution lengths and the most conservative trip setpoints and once with maximum execution lengths and/or least conservative trip setpoints. This process produces a band of trip times for the test cases which contains the effects of processing uncertainties. The largest band of acceptable trip times will be obtained if the modified execution lengths and adjusted trip setpoints are used simultaneously.

The software DSVT program includes a [ ]-millisecond interrupt cycle, to check for DNBR and LPD trip signals. This results in a [ ]-millisecond-interval limit on trip time resolution which is factored into the acceptance criteria. The following tables contain the final DSVT acceptance criteria for initial values and trip times for DNBR and LPD.

Acceptance Criteria for

DNBR and LPD Initial Values (DNBR Units and kW/ft., respectively)

Test Case	DNBR (Min.)	DNBR (Max.)	LPD (Min.)	LPD (Max.)
[redacted]				

Acceptance Criteria for

DNBR and LPD Initial Values (DNBR Units and kW/ft., respectively)

(Continued)

Test Case	DNBR (Min.)	DNBR (Max.)	LPD (Min.)	LPD (Max.)
[				]

Acceptance Criteria for
DNBR and LPD Trip Times (seconds)

Test Case	DNBR (Min.)	DNBR (Max.)	LPD (Min.)	LPD (Max.)

Acceptance Criteria for
DNBR and LPD Trip Times (seconds)
(Continued)

Test Case	DNBR (Min.)	DNBR (Max.)	LPD (Min.)	LPD (Max.)
[redacted]				

3.3 Analysis of DSVT Results

Results of DSVT are listed in the table on the following pages.

Therefore, it is concluded that the DSVT does not indicate any errors in the CPC software.

DSVT Results

Test Case	Initial DNBR (DNBR Units)	Initial LPD (kW/ft.)	DNBR Trip (sec.)	LPD Trip (sec.)
[redacted]				

DSVT RESULTS (Cont.)

Test Case	Initial DNBR (DNBR Units)	Initial LPD (kW/ft.)	DNBR Trip (sec.)	LPD Trip (sec.)
[				]

4.0 LIVE INPUT SINGLE PARAMETER TEST

The Live Input Single Parameter test is a real-time exercise of the CPC/CEAC application and executive software, with transient CPC/CEAC input values generated from an external source and read through the CPC/CEAC input hardware. The objectives of this test are:

(1) To verify that the dynamic response of the integrated CPC/CEAC software and hardware is consistent with that predicted by design analyses.

(2) To supplement design documentation quality assurance, Phase I module tests, Input Sweep Tests, and DSVT in assuring correct implementation of software modifications.

(3) To evaluate the integrated hardware/software system during operational modes approximating plant conditions.

4.1 LISP Test Case Selection

Reference 1 identifies the test cases to be used for LISP. These cases are the single variable dynamic transient test cases from the Phase II test series.

These test cases, which are applicable to SONGS-2, consist of a

[ ]

4.2 Generation of LISP Acceptance Criteria

The acceptance criteria for LISP are based on trip times for the dynamic test cases. For the non-target CEA drop test case, there should be no trip.

These cases are simulated within the FORTRAN Simulation Code and contain the following adjustment components.

[

]

Application program execution lengths used for LISP testing were the same as those for DSVT, with the addition of CEAC minimum and maximum execution lengths of [ ] msec, respectively.

The final acceptance criteria (generated by the FORTRAN Simulation Code and adjusted for the above components) for LISP are contained in the following table.

Test Case	Minimum Trip Time (seconds)	Maximum Trip Time (seconds)
[		]

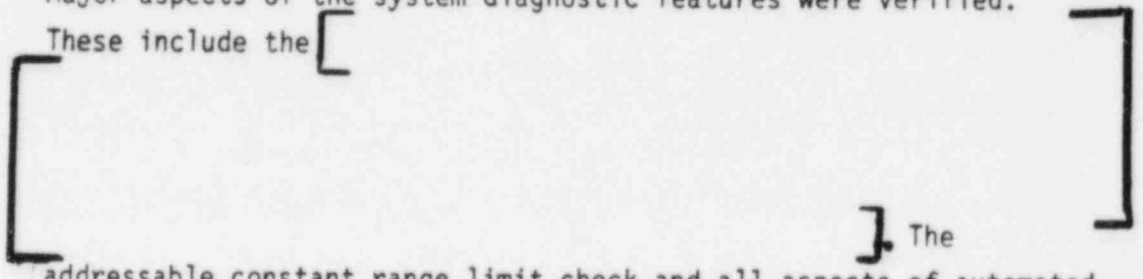
4.3 LISP Test Results

The [ ] dynamic transients were executed on the Single Channel Test Facility (SCTF). The recorded trip times (in seconds) for each case are listed in the following table:

Run

All recorded trip times met the final acceptance criteria for LISP.

Major aspects of the system diagnostic features were verified. These include the



The addressable constant range limit check and all aspects of automated reentry of Addressable constants were also tested. Therefore, all testing was determined to be acceptable and the system diagnostic features were correctly implemented.

5.0 PHASE II TEST RESULTS SUMMARY

The Phase II software verification tests have been performed as required in Reference 1. The test results are that both the CPC and CEAC software have no indication of errors and that the operation of the integrated system is consistent with the performance predicted by design analyses, which provide design inputs to CPC/CEAC Functional Design Specifications.

6.0 REFERENCES

1. CPC Protection Algorithm Software Change Procedure, CEN-39(A)-NP, Revision 02, December 1978

2. Functional Design Specification for a Core Protection Calculator, CEN-147(S)-NP, February 1981

3. Functional Design Specification for a Control Element Assembly Calculator, CEN-148(S)-NP, January 1981

4. CPC and CEAC Data Base Listing, CEN-266(S)-NP, Revision 01, November 1984.

5. CPC/CEAC System Phase I Software Verification Test Report, CEN-176(S)-NP, Revision 03, November 1984

COMBUSTION ENGINEERING, INC.