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CPC/CEAC SYSTEM
PHASE II SOFTWARE VERIFICATION
TEST REPORT

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ABSTRACT

Phase II Testing is performed on the CPC/CEAC System to (1) verify that the CPC and CEAC software modifications have been properly integrated with the CPC and CEAC software and system hardware and (2) provide confirmation that the static and dynamic operation of the integrated system as modified is consistent with that predicted by design analyses, which provide design inputs to CPC/CEAC Functional Design Specifications.

This report presents the Phase II test results for the San Onofre Nuclear Generating Station Unit 2 Plant CPC/CEAC Revision 02 software.

The Phase II Software Verification Tests have been performed as required (Reference 1). In all cases, the test results fell within the acceptance criteria, or are explained. The test results are that both the CPC and CEAC software have no indication of software error and that the operation of the integrated system is consistent with the performance predicted by design analyses.

TABLE OF CONTENTS

1.0 INTRODUCTION

The verification of software modifications of the CPC/CEAC System consists of several steps which address two major areas of the modification process:

(1) Specification of software modifications
(2) Implementation of software modifications

The specification of software modifications is documented in the Software Change Procedure (Reference 1), CPC and CEAC Functional Design Specifications (References 2 & 3), and the Data Base Listing, and is verified by design analyses contained in recorded calculations. The implementation of software modifications is documented in Software Design Specifications and assembly listings (Reference 4).

The verification process for the modified software implementation is two-phase: Phase I testing (Reference 5), must be performed before Phase II. Phase I testing, which was successful, verified the correct implementation of the modified software. Phase II testing completes the software modification process by verifying that the integrated CPC System responds as expected.

This document contains the test results and conclusions for the Phase II software verification test.

1.1 Objectives

The primary objective of Phase II testing is to verify that the CPC and CEAC software modifications have been properly integrated with the CPC and CEAC software and system hardware. In addition, Phase II testing provides confirmation that the static and dynamic operation of the integrated system as modified is consistent with that predicted by design analyses. These objectives are achieved by

comparing the response of the integrated system to the response predicted by the CPC/CEAC FORTRAN Simulation Code. This comparison is performed for a selected range of simulated static and dynamic input conditions.

1.2 Description of Phase II Testing

Phase II testing consists of the following tests:

(1) Input Sweep Tests for the CPC and the CEAC,
(2) Dynamic Software Verification Test, and
(3) Live Input Single Parameter Test.

These tests are performed on a single channel CPC/CEAC System with integrated software that has undergone successful Phase I testing.

1.3 Applicability

This report applies to the Phase II Testing performed on the San Onofre Nuclear Generating Station Unit 2 CPC/CEAC system software Revision 02.

2.0 CPC/CEAC INPUT SWEEP TESTS

The Input Sweep Test is a real-time exercise of the CEAC and CPC application and executive software with steady-state CPC and CEAC input values read from a storage device. These tests have the following objectives:

(1) To determine the processing uncertainties that are inherent in the CPC and CEAC designs.

(2) To verify the ability of the CPC and CEAC algorithms used in the system hardware to initialize to a steady state after an auto-restart for each of a large number of input combinations within the CPC/CEAC operating space.

(3) To complement Phase I module testing by identifying previously unnoticed abnormalities in the CPC and CEAC algorithms used in the system hardware.

2.1 CPC Input Sweep Test Case Selection

[ ] cases, each involving different combinations of process inputs and addressable constants, were used for CPC design qualification testing of the Revision 02 software.

2.1.1 CPC Processor Uncertainty Results

For each test case, differences in the results of the FORTRAN simulation code and CPC system were calculated. A statistical analysis of these differences produced the processing uncertainties.

The DNBR statistics did not include those cases for which the DNBR as calculated on either system was at the limits [ ]. This is because a difference of zero (or close to zero) would be computed and would incorrectly weight the distribution of differences. A

total of [ ] cases remained after these cases were eliminated. The LPD statistics did not include those cases for which the LPD as calculated on either system was equal to or greater than the upper limit of [ ] core average kW/ft (= [ ] kW/ft). A total of [ ] cases remained after these cases were eliminated.

Although [ ] cases were not included in the computation of DNBR and LPD statistics, respectively, they were still included as Input Sweep Test cases for the purpose of identifying potential software errors.

The processor uncertainties for DNBR and LPD are defined as the one-sided tolerance limits which encompass 95% of the distribution of DNBR and LPD differences for all test cases with a 95% confidence level. The processor uncertainties determined from Input Sweep for DNBR and LPD, respectively, are [ ] DNBR units, and [ ] core average kW/ft. However, since the distribution of differences is so restrictive, the maximum error may be used (that is, the limits which encompass 100% of the difference). This is more conservative and yet still results in small processor uncertainties. Thus defined, the processor uncertainties (for Revision 01 of the CPC Input Sweep tests) on DNBR and LPD are [ ] DNBR units and [ ] core average kW/ft, respectively.

2.1.2 Analysis of CPC Input Sweep Test Results

The results of the test cases exceeding the 95/95 tolerance limit were analyzed for evidences of software errors. The review results of the DNBR and LPD test cases outside the 95/95 tolerance limit will now be discussed. For DNBR there were [ ] cases below the lower tolerance limit of [ ] (DNBR units) and [ ] test cases above the upper tolerance limit of [ ] (DNBR units). For these [ ] test cases the difference between the single channel and the CPC Fortran is within the accuracy of the two systems. The largest percent error among the [ ] cases was [ ].

These differences do not show a significant commonality since the differences are absolute (not relative) and it should be expected that the largest differences should occur at high DNBRs. It is therefore concluded that no errors are indicated in the CPC Single Channel DNBR program.

For LPD the cases examined were: [ ] cases with differences below the lower 95/95 tolerance limit of [ ](% of core average kW/ft), [ ]cases with differences greater than the upper tolerance limit of [ ].

The largest percent error among the [ ]cases was [ ] . The common input to these test cases was found in other test cases with less maximum difference and less percent error. Examination of the inputs to all [ ]LPD cases outside the tolerance limits showed that the inputs covered a wide spectrum. No common area was found. It is therefore concluded that there is no indication from the Input Sweep test results of software errors in the Single Channel calculation of LPD.

2.2 CEAC Input Sweep Test Case Selection

[ ] test cases, each involving different combinations of CEAC process inputs were used for CEAC design qualification testing of the Revision 02 software. These test cases covered all CEAC operating space.

2.2.1 CEAC Processor Uncertainty Results

For each test case, differences between the CEAC FORTRAN simulation code and CEAC single channel system results were calculated. The processor uncertainties for DNBR and LPD are defined as the one-sided tolerance limits which encompass 95% of the distribution of DNBR and LPD penalty factor differences for all test cases with a 95% confidence level.

The processor uncertainties for the DNBR and the LPD penalty factor differences are [ ] DNBR units and [ ] core average kW/ft, respectively.

2.2.2 Analysis of CEAC Input Sweep Test Results

The results were reviewed for representativeness and for any evidence of computational differences between the CPC FORTRAN simulation and the Single Channel Facility (SCF). The test data produced penalty factors which swept the respective DNBR and LPD penalty factor ranges with emphasis on the midrange values. The differences between the penalty factors from the SCF and the FORTRAN simulation were within a range which is justified by the differences in word length.

[ ]

In conclusion, the CEAC Input Sweep Test result did not indicate the existence of a software error.

3.0 DYNAMIC SOFTWARE VERIFICATION TEST

The Dynamic Software Verification Test (DSVT) is a real time exercise of the CPC application software and executive software with transient CPC input values read from a storage device. This test has two objectives:

(1) To verify that the dynamic response of the integrated CPC software is consistent with that predicted by design analyses, and

(2) To supplement design documentation quality assurance, Phase I module tests, and Input Sweep Tests in assuring correct implementation of software modifications.

Further information concerning DSVT may be found in Reference 1.

3.1 DSVT Case Selection

Test cases for DSVT are selected to exercise dynamic portions of the CPC software with emphasis on those portions of the software that have been modified.

DSVT requires that, as a minimum, cases [ ] be selected for testing. These cases are from the Phase II test series and consist of a [ ] respectively. Because the changes made for this software revision were limited to the CEAC portion of the data base, it was only necessary to perform a subset of the entire battery of DSVT cases listed below. Therefore, in addition to the minimum group of cases required, those others containing CEA deviations were also conducted [ ]. Also, one test case [ ], which was

designed to test a feature of the Reactor Power Cutback System installed in some other C-E plants, was included because it demonstrates the proper [ ] [ ]

3.2 Generation of DSVT Acceptance Criteria

Acceptance criteria for DSVT are defined (in Reference 1) as the trip times and initial values of DNBR and LPD for each test case. These trip times and initial values are generated using the certified CPC/CEAC FORTRAN simulation code. Processing uncertainties obtained during Input Sweep testing are factored into the acceptance criteria for initial values of DNBR and LPD where necessary. Trip times are affected by program execution lengths as well as by the Input Sweep uncertainties. The minimum, average, and maximum execution lengths (in milliseconds) calculated for the Revision 02 software are listed below.

CPC Application Program Execution Lengths

Program	Minimum (msec)	Average (msec)	Maximum (msec)
FLOW	[		]
UPDATE			
POWER			
STATIC			

Each DSVT case is initially executed once with nominal program execution lengths (values between the minimum and maximum) and data base values of trip setpoints using the CPC/CEAC FORTRAN simulation code. Following execution of the same cases using the single channel facility, those cases which do not yield trip times equivalent to those calculated by the CPC FORTRAN code are re-executed: once with minimum execution lengths and/or the most conservative trip setpoints and once with maximum execution lengths

and/or least conservative trip setpoints. This process produces a band of trip times for the test cases which contains the effects of processing uncertainties. The largest band of acceptable trip times will be obtained if the modified execution lengths and adjusted trip setpoints are used simultaneously.

The software DSVT program includes a[ ]-millisecond interrupt cycle, to check for DNBR and LPD trip signals. This results in a [ ]-millisecond-interval limit on trip time resolution which is factored into the acceptance criteria. The following tables contain the final DSVT acceptance criteria for initial values and trip times for DNBR and LPD.

Acceptance Criteria for

DNBR and LPD Initial Values (DNBR Units and kW/ft., respectively)

Test Case	DNBR (Min.)	DNBR (Max.)	LPD (Min.)	LPD (Max.)
[redacted]				

Acceptance Criteria for
DNBR and LPD Initial Values (DNBR Units and kW/ft., respectively)
(Continued)

Test Case	DNBR (Min.)	DNBR (Max.)	LPD (Min.)	LPD (Max.)
[				]

Acceptance Criteria for
DNBR and LPD Trip Times (seconds)

Test Case	DNBR Trip (Min.)	DNBR Trip (Max.)	LPD Trip (Min.)	LPD Trip (Max.)
[				]

Acceptance Criteria for
DNBR and LPD Trip Times (seconds)
(Continued)

Test Case	DNBR Trip (Min.)	DNBR Trip (Max.)	LPD Trip (Min.)	LPD Trip (Max.)
[redacted]				

3.3 Analysis of DSVT Results

Results of DSVT are listed in the following table.

The trip times for all of the test cases executed on the Single Channel Facility met the acceptance criteria determined by the CPC/CEAC FORTRAN simulation code. Because the trip times on the Single Channel Facility were identical to those on the FORTRAN simulation, generation of trip time acceptance bands was not necessary.

For all test cases with the exception of Case , the initial values of DNBR and LPD were within the acceptance criteria.

[ ]

no software error is indicated.

DSVT Results

Test Case	Initial DNBR (DNBR Units)	Initial LPD (kW/ft.)	DNBR Trip (sec.)	LPD Trip (sec.)
[				]

DSVT RESULTS (Cont.)

Test Case	Initial DNBR (DNBR Units)	Initial LPD (kW/ft.)	DNBR Trip (sec.)	LPD Trip (sec.)
[				]

4.0 LIVE INPUT SINGLE PARAMETER TEST

The Live Input Single Parameter test is a real-time exercise of the CPC/CEAC application and executive software, with transient CPC/CEAC input values generated from an external source and read through the CPC/CEAC input hardware. The objectives of this test are:

(1) To verify that the dynamic response of the integrated CPC/CEAC software and hardware is consistent with that predicted by design analyses.

(2) To supplement design documentation quality assurance, Phase I module tests, Input Sweep Tests, and DSVT in assuring correct implementation of software modifications.

(3) To evaluate the integrated hardware/software system during operational modes approximating plant conditions.

4.1 LISP Test Case Selection

Reference 1 identifies the test cases to be used for LISP. These cases are the single variable dynamic transient test cases from the Phase II test series.

These test cases, which are applicable to SONGS-2, consist of a [ ].

4.2 Generation of LISP Acceptance Criteria

The acceptance criteria for LISP are based on trip times for the dynamic test cases. For the non-target CEA drop test case, there should be no trip.

These cases are simulated within the CPC FORTRAN Simulation Code and contain the following adjustment components.

[

]

Application program execution lengths used for LISP testing were the same as those for DSVT, with the addition of CEAC minimum and maximum execution lengths of [ ]msec, respectively.

The final acceptance criteria (generated by the CPC FORTRAN simulation code and adjusted for the above components) for LISP are contained in the following table.

Test Case	Minimum Trip Time (seconds)	Maximum Trip Time (seconds)
[		]

4.3 LISP Test Results

The [ ] dynamic transients were executed on the CPC Single Channel facility. The recorded trip times (in seconds) for each case are listed in the following table:

All recorded trip times met the final acceptance criteria for LISP.

Major aspects of the system diagnostic features were verified. These include the [

] All aspects of automated reentry of Addressable Constants were also tested.

5.0 PHASE II TEST RESULTS SUMMARY

The Phase II software verification tests have been performed as required in Reference 1. The test results are that both the CPC and CEAC Revision 02 software have no indication of errors and that the operation of the integrated system is consistent with the performance predicted by design analyses, which provide design inputs to CPC/CEAC Functional Design Specifications.

6.0 REFERENCES

1. CPC Protection Algorithm Software Change Procedure, CEN-39(A)-NP, Revision 02, December 1978.

2. Functional Design Specification for a Core Protection Calculator, CEN-147(S)-NP, February 1981.

3. Functional Design Specification for a Control Element Assembly Calculator, CEN-148(S)-NP, January 1981.

4. CPC and CEAC Data Base Listing, CEN-266(S)-NP, Revision 00, January 1984.

5. CPC/CEAC System Phase I Software Verification Test Report, CEN-176(S)-NP, Revision 02, February 1984.

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