ATTACHMENT B

EAGLE-21 VERIFICATION AND VALIDATION

TEST REPORT

WCAP-12889

ZION UNIT 1

EAGLE 21

PROCESS PROTECTION SYSTEM

REPLACEMENT EARDWARE

VERIFICATION AND VALIDATION

REPORT

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ABSTRACT

This report documents the implementation of the Eagle 21, Replacement Hardware Design, Verification and Validation Plan (DS 408A47, R3), as applied to Commonwealth Edison Company's Ziol Station

The report summarizes the Verification and Validation program results which demonstrate that the Zion Eagle 21 process protection system functional upgrade has been satisfactorily completed in accordance with all of its functional and design requirements.

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Commonwealth Edison Company has purchased and will install a microprocessor based system to replace 16 racks of the analog process protection system at Zion Unit 1.

The Microprocessor based equipment is the Eagle 21 Process Protection System Replacement Hardware. This equipment performs the following major functions:

- 1. Reactor Trip Protection (Channel Trip to Voting Logic)
- 2. Engineered Safeguard Features (ESF) Actuations.
- 3. Isolated Outputs to Control Systems, Control Panels, and Plant Computers
- 4. Isolated Outputs to information displays for Post Accident Monitoring (PAM) indication
- 5. Automatic Surveillance Testing to verify channel performance.

A brief description of the Eagle 21 System hardware architecture and related functions is given in Section 2.0.

A comprehensive Verification and Validation (V&V) program was conducted in accordance with Regulatory Guide 1.152 and ANSI/IEEE/ANS 7-4.3.2 to ensure the functionality of the system to a level commensurate with that described in the system requirements. The Eagle 21 Replacement Hardware Design, Verification and Validation Plan is documented by Design Specification 408A47, Revision 3, dated May 12, 1989. A brief discussion of the V&V program is provided in section 3.0 of this report.

This report presents the results of the V&V program conducted on the Zion Unit 1 Eagle 21 System.

The software verification for the Zion Unit 1 Eagle 21 System vas completed in February 1991 with the total number of software units involved being 1169. For these units, a total of 408 verification problem reports were generated. All verification problem reports generated have been resolved. All changes to the software documentation have been reviewed and/or tested to demonstrate successful resolution of the problems found.

It should be noted that the software verification effort was performed on generic type Eagle-21 software. This software includes all possible Eagle-21 process algorithms, whether they are used in a particular installation or not. Therefore not all of the 1169 software units are actually ever executed in the Zion Unit 1 system, nor are all the 408 verification problem reports directly applicable. However, as the totality of the software package includes this code, this report covers all findings in the software.

The system validation program for the Eagle 21 System was also completed in February 1991, including 11 comprehensive tests and 93 hardware/software/FAT reviews. The hardware/software/FAT reviews and validation tests are completed. All validation problem reports which were generated are resolved. These reviews and tests are, unlike the verification findings, all directly applicable to the Zion Unit 1 upgrade. The 11 validation tests were not the extent of testing for evaluation of validation concerns; reviews were made of applicable prior testing such as applicable tests from previous Eagle-21 systems and Zion FAT's (Factory Acceptance Tests).

It should be noted that none of the anomalies identified in the validation problem reports are errors that would be expected to be identified during the verification process. All problem reports generated during the validation process are in areas specific to validation.

The Eagle 21 upgrade implemented for Zion Unit 1 has been demonstrated to meet its functional and design requirements.

2.0 EAGLE 21 SYSTEM FUNCTION OVERVIEW

The Westinghouse Eagle 21 microprocessor based process protection upgrade system is applicable for those instrument systems which are "safety-related" as defined by IEEE Std. 279-1971, "Criteria for Protection Systems for Nuclear Power Generating Stations". The Eagle 21 portion of process instrumentation includes all necessary devices with the exception of transmitters, indicators, and recorders.

The Westinghouse Eagle 21 microprocessor-based process protection system is a functional replacement for existing analog process protection equipment used to monitor process parameters at nuclear generating stations and initiate actuation of the reactor trip and engineering safeguards systems. Features of the Eagle 21 equipment include the following:

- A. Automatic surveillance testing to significantly reduce the time required to perform surveillance tests.
- B. Self calibration to eliminate rack drift and time consuming calibration procedures.
- C. Self diagnostics to reduce the time required for troubleshooting.
- D. Significant expansion capability to easily accommodate functional upgrades and plant improvements.
- E. Modular design to allow for a phased installation into existing process racks and use of existing field terminations.

The Eagle 21 System Hardware consists of three basic subsystems per rack: Loop Processor Subsystem, Tester Subsystem and Input/Output Subsystem.

1. Loop Processor Subsystem

The Loop Processor Subsystem receives a subset of the process signals, performs one or more protection algorithms, and drives the required isolated outputs.

2. Tester Subsystem

The Tester Subsystem serves as the focal point of the human interaction with the protection rack. When used in conjunction with the Man-Machine-Interface (MMI) test cart, the Tester Subsystem provides a user-friendly interface that permits test personnel to configure (adjust setpoints and tuning constants), test, and maintain the system.

3. Input/Output (I/O) Subsystem

The microprocessor based system interfaces with the field signals through various input/output (I/O) modules. These modules accommodate the plant signals and test inputs from the Tester Subsystem, which regularly monitors the integrity of the Loop Processor Subsystem.

In an Eagle 21 Process Protection Instrument Channel, field sensors are connected to cabinet mounted terminal blocks. The process electronics power the sensors and perform signal conditioning, calculation, and isolation operations on the input signals. However, each element of the process is not an individual electronic module or printed circuit board assembly. A multiple channel Analog Input module is used to power the field sensor(s) and perform signal conditioning. All calculations for the process channel functions are performed by a centralized Loop Calculation Processor (LCP). Typical functions performed by the Loop Calculation Processor are as follows: summation, lead/lag, Jultiplication, comparator, averaging, and square root conversion. Trip logic is provided through multiple channel Partial Trip Output modules. Multiple channel isolated analog outputs are provided by Analog Output modules. In addition, all Eagle 21 process protection channels are configured to perform automatic surveillance testing via a centralized Test Sequence Processor (TSP).

Protection and Monitoring channels processed with the Eagle 21 process protection system are as follows:

- A. Average Temperature and Delta Temperature
- B. Pressurizer Pressure and Water Level
- C. Reactor Coolant System Flow
- D. Containment Pressure
- E. Steam Generator Water Level
- F. Steamline Pressure and Differential Pressure
- G. Loop Stop Valve Interlocks
- H. Reactor Coolant Wide Range Temperatures
- I. RCS Wide Range Pressure
- J. Turbine Impulse Chamber Pressure
- K. Steam Flow
- L. Feedwater Flow

The Eagle 21 equipment has been designed to fit into existing process tacks and to interface with other plant systems in a manner identical the existing analog equipment. This design maintains the existing rield terminals to avoid new cable pulls or splices within the rack. The components for each rack are built into subassemblies which are easily installed into the existing racks. All internal rack cabling is prefabricated. The subassemblies are tested in a factory mock-up to verify proper fit and operation. Detailed installation procedures and drawings are provided with each system.

3.0 VERIFICATION AND VALIDATION PROCESS PHILOSOPHY

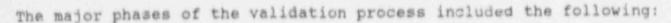
3.1 Verification Philosophy

With the application of programmable digital computer systems in safety systems of nuclear power generating stations, in order to ensure the functionality of software to a level commensurate with that described in the system requirements, designers are obligated to conduct independent reviews of the software associated with the computer system.

Figure 3-1 illustrates the integration of the system verification and validation with the system design process. The verification process was divided into two distinct phases: verification of design documentation and verification of software. Figure 3-1 illustrates where an independent review of design documentation was performed. After completed software was turned over to the verifier by the design team, an independent review and/or test of each software unit was performed to verify the software unit met the applicable Software Design Specification. As part of the software unit review, the unit was linked with other interfacing software units where appropriate. Structura) testing was performed on the software units. This Structural testing exercised the software program code and its component logic structures. This process required the verifier to inspect the code against its associated documentation and understand how it functions before selecting the test inputs and predicting the test outputs consistent with code documentation. The test inputs were chosen to exercise all executable lines of code within the software entity.

3.2 Validation Philosophy

Whereas the system verification process was performed to verify the software entities, the system validation process was performed to demonstrate the system functionality. The system validation testing results demonstrated that the system design completely satisfied the system functional requirements. Hence, any inconsistencies that may have occurred during the system development in this area that were not discovered during the software verification activities were identified through the validation process. Validation compliments the verification process by ensuring that the system meets its functional requirements by conducting testing from a total systems perspective.



- A. Functional Requirements/Abnormal-Mode Testing Phase
- B. Prudency Review and/or Testing of the Design and Implementation Phase.

The functional requirements/abnormal-mode testing process treated the system as a black box, while prudency review and/or testing required that the internal structure of the integrated software/hardware system be understood and analyzed in detail. This dual approach to the validation process provided a level of thoroughness and testing accuracy which ensured the functionality of the system commensurate with that described in the system requirements.

The Validation Plan defines the methodology utilized to perform a series of reviews and tests which compliment the verification process. Four independent types of reviews and/or tests were conducted to ensure overall system integrity:

- 1. Functional requirements testing -- ensured that the final system satisfied the functional requirements. A functional decomposition was prepared from the system functional requirements and used as a basis for the validation test procedures. The functional requirements documents reviewed were
 - a) CWE-300/3, Revision 2, "Functional Requirements for Thermal Overpower and Overtemperature Protection".
 - b) CWE-300/4, Revision 1, "Functional Requirements for Reactor Coolant System Pressure and Water Level Protection".
 - c) CWE-300/5, Revision 1, "Functional Requirements for Reactor Coolant System Low Flow Protection".
 - d) CWE-300/6, Revision 0, "Functional Requirements for Safety Systems Actuated by Containment Pressure Signals".
 - e) CWE-300/7, Revision 1, "Functional Requirements for Steam Generator Protection System".
 - f) CWE-300/8, Revision 1, "Functional Requirements for Secondary High Energy Line Break Protection Systems".
 - g) CWE-300/9, Revision 2, "Functional Requirements for Miscellaneous Protection System".
 - g) CWE-300/18, Revision 1, "Functional Requirements for Reactor Coolant System Loop Stop Valve Core Protection System".
 - c) Zion Supplemental Functional Requirements, Revision 0.

- Abnormal-mode testing -- ensured that the design operated properly under abnormal-mode conditions.
- 3. System Prudency Review/Testing -- ensured that good design practice was utilized in the design and implementation of critical design areas of the system. These tests required that the internals of the system design and implementation be analyzed in detail.

DESIGN, VERIFICATION, AND VALIDATION PROCESS

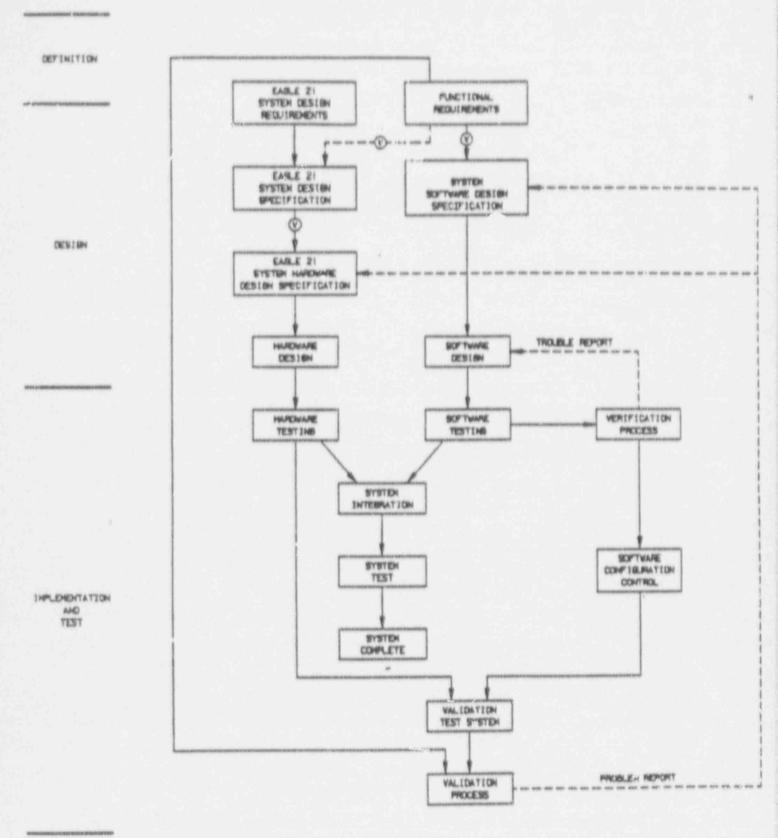


Figure 3-1

O DENOTES INSPENDENT VERIFICATION REVIEW

4.0 SUMMARY OF VERIFICATION ACTIVITIES

The verification process was performed in accordance with the Eagle 21 Replacement Hardware Design, Verification and Validation Plan. All Eagle 21 system software was verified using Level 1 (safety related) type of testing and review. The overall scope of the verification effort on the Ezgle 21 System consisted of 1169 units of software whose configuration is documented on Figure 4-2.

Related software units were grouped together into software modules. Each software module consisted of a single source code file. When any anomaly was discovered during the source code review or during testing, a verification problem report was issued from the verification team to the design team for resolution. These problem reports consisted of three types, depending upon the scope of the discovered anomaly; 1) unit level problem reports, 2) module level problem reports, and 3) generic problem reports. The unit level problem reports addressed anomalies specific to a single unit of code. The module level problem reports addressed anomalies covering entire modules (typically due to formatting standards concerns). Generic problem reports covered issues which spanned multiple modules (again typically due to formatting standards concerns). A total of 408 problem reports were generated consisting of 179 unit level problem reports, 164 module level problem reports, and 65 generic problem reports. All verification problem reports were satisfactorily resolved.

The verification problem reports were assigned error codes as the reports were generated. Working from a list of 11 possible error codes, error types were assigned to problem reports. A problem report may contain more than one error type.

A significant portion of the total unit problem reports, 91.6%, was made up of 6 error types:

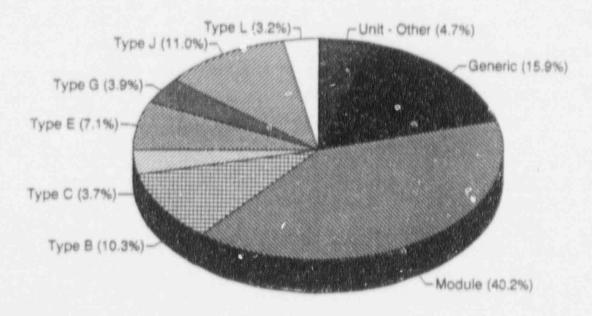
Α.	Design Requirements Implemented Incorrectly (Type B)	23.5%
ki -	Implementation includes Items not in Design Requirements (Type C).	8.4%
c.	Logic Anomaly (Type E)	20.1%
D.	Data Handling Anomaly (Type G)	10.6%
Ε.	Header/Comment Anomaly (Type J)	29.6%

Note that a single unit problem report may be counted several times in the above percentages as it may have multiple categories.

F. Coding Standards Anomaly (Type L)

A categorized breakdown of all software verification problem reports is provided in Figure 4-1.

ZION Eagle-21 Software Verification Total of 408 Problem Reports



Note: Problem Reports with multiple Types are Listed under the first letter designation

Figure 4-1

SOFTWARE CONFIGURATION (Continued on Next Page)

Firmware Drawing	Rev	Description	Software Vers Rev
8250C58G01	4	Zion Unit 1 Rack 1 LCP Firmware Configuration	V01 - 02
8250C58G02	4	Zion Unit 1 Rack 2 LCP Firmware Configuration	V01 02
8250C58G03	4	Zion Unit 1 Rack 3 LCP Firmware Configuration	V01 - 02
8251 J58G04	4	Zion Unit 1 Rack 8 LCP Firmware Configuration	V01 - 03
8250C58G05	4	Zion Unit 1 Rack 9 LCP Firmware Configuration	V01 - 02
8250C58G06	4	Zion Unit 1 Rack 10 LCP Firmware Configuration	V01 - 02
8250C58G07	4	Zion Unit 1 Rack 11 LCP Firmware Configuration	V01 ·· 02
9250C58G08	4	Zion Unit 1 Rack 12 LCP Firmware Configuration	V01 - 02
8250C58G09	4	Zion Unit 1 Rack 15 LCP Firmware Configuration	V01 - 02
8250C58G10	4	Zion Unit 1 Rack 16 LCP Firmware Configuration	V01 - 02
8250C08G02	8	E21 STD TSP Firmware Configuration	V02 - 13

Figure 4-2

SOFTWARE CONFIGURATION (Continued from previous Page)

8250C07G01	2	E21 STD DFP Firmware Configuration	V01 - 01
8250C06G01	2	E21 STD DLH Firmware Configuration	V01 - 00
8250C05G02	5	E21 STD MMI Firmware Configuration	V02 - 08
8250C20	3	E21 STD Microcontroller Firmware Config.	V01-03 (G01) V01-02 (G02)

Figure 4-2

5.0 SUMMARY OF VALIDATION ACTIVITIES

The validation process was performed in accordance with the Eagle 21 Replacement Hardware Design, Verification and Validation Plan, by a team of individuals independent from the design team. The overall scope of the validation effort on the Eagle 21 System consisted of performing 18 comprehensive tests and 130 hardware/software/FAT reviews.

When any validation test result failed the applicable acceptance criteria, a problem report was issued from the validation team to the design group for resolution. A total of 8 validation problem reports were generated. All validation problem reports were satisfactorily resolved. It should be noted that all problem reports were in areas specific to validation. None of the errors precipitating a validation problem report were of a type that should have been found during the verification process. The number of problem reports generated by the validation phase were:

Functional Requirements/Abnormal

5

Prudency Phase

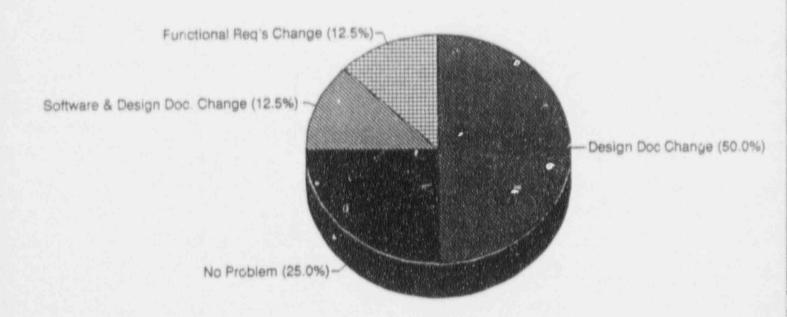
3

The specific problem reports are:

TRI.001-VAL	TRI.002-VAL
TRI.003-VAL	TRI.004-VAL
TRI.006-VAL	TRI.008-VAL
TRI.009-VAL	TRI.010-VAL

The validation and design teams identified four avenues for resolving the problem reports: Software changes, Functional Requirements changes, requirements documentation revision and validation test procedure changes. The number of validation problem reports resolved by each avenue are shown in Figure 5-1.

Zion Eagle-21 Validation Total of 9 Problem Reports



Analyzed By Resolution

Figure 5-1

ATTACHMENT C

EAGLE-21

NOISE, FAULT, SURGE, AND RADIO INTERFERENCE

TEST REPORTS

WCAP-11733

AND

WCAP-11896



Westinghoung facing Systems



4005110030

NOISE, FAULT, SURGE, AND RADIO FREQUENCY INTERFERENCE TEST REPORT

FOR

Westinghouse Eagle-21™ Process Protection Upgrade System

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ABSTRACT

The following test report documents the Eagle 21% protection system adverse electrical noise test program. The primary objective of this test program was to demonstrate that the Eagle 21% system remained operational before, during, and after the applied noise conditions. Other objectives were to demonstrate the physical independence of class non-1E and class-1E circuitry within the Eagle 21% system.

The Eagle 21° system met all performance requirements specified by the acceptance criteria. The adverse noise conditions applied to the Eagle 21° system are designed to exceed worst-case noise environment conditions.

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SECTION 1

This report documents the "adverse noise" test results of the Eagle 21° Process Protection System.

The Eagle 21^∞ is a microprocessor-based functional replacement for the analog process protection equipment originally installed in a nuclear power generating plant.

The testing of the Eagle 21* equipment was performed to demonstrate system operability before, during, and after the "adverse noise" conditions were applied. These adverse noise conditions are separated into four catagories:

- o Noise Interference
- o Fault Isolation
- c Surge Withstand Capability (SWC)
- o Radio Frequency Interference (RFI)

A description of the tests, acceptance criteria, and test results of the Eagle 21^∞ in these adverse noise environments are contained in this report.

The Radio Frequency Interference tests were performed in an anechoic chamber $\begin{bmatrix} & & & & \\ & & & \\ & & & \end{bmatrix}_{\mathbb{C}}, \text{ with the balance of the tests} \\ \text{performed at the Westinghouse Instrumentation Technology Training Center} \\ \text{(ITTC) located in Monroeville, Pennsylvania. These tests were performed during a three-month period from December 1987 through February 1988.} \\ \end{bmatrix}$

SECTION 2 EAGLE 21° SYSTEM DESCRIPTION

2.1 INTRODUCTION

The Westinghouse Eagle 21^M Process Protection Upgrade System is a qualified, microprocessor-based functional replacement for the analog process protection equipment originally installed in a nuclear power generating plant. the modular design of the Eagle 21^M hardware permits installation in existing process protection system cabinets after the analog electronics and internal cabinet wiring are removed. There is minimum disruption of external wiring because cabinet field terminal blocks and field cables are mostly undisturbed. All system inputs and outputs are preserved, and all existing field interfaces are maintained. Figure 2-1 depicts one Eagle 21^M cabinet.

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Figure 2-1 Eagle 21 Process Protection Upgrade System Com net

Figure 2-2 Eagle 21™ Cabinet Installation

2.1.2 Plant Applications

The Eagle 21m Process Protection Upgrade System is utilized in nuclear power generating stations to monitor Nuclear Steam Supply System (NSSS) parameters and to display indications of these parameters to the operating personnel. These indications meet the post-accident monitoring (PAM) requirements of Regulatory Guide 1.97, "Instrumentation for Light-Water-Cooled Nuclear Power Plants to Assess Plant and Environs Conditions During and Follog an Accident." Figure 2-3 depicts the typical interconnections between the process protection equipment and other plant systems. [



Figure 2-3 Typical 1&C System Configuration

The NSSS parameters monitored by the Eagle 21" Process Protection Upgrade System consist of temperatures, pressures, liquid levels, and flows. Resistance temperature detectors (RTDs) are used for temperature measurements. Electronic transmitters having either a 4- to 20-mA or 10- to 50-mA range are used to monitor pressure, level, and flow parameters. The system can also accept analog voltage or current inputs from other nuclear process systems such as the Nuclear Instrumentation System (NIS).

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All inputs are converted to digital signals by the microproceasor-based Eagle 21m electronics. After the desired signal conditioning is accomplished (including dynamic compensation of time-dependent signals, summation, and scaling), the system produces the following types of outputs:

- o Analog output: -- 10- to 50-mA or 4- to 20-mA (or 1- to 5-vdc) signals supplied to control boord indicators or the process control systems
- Contact outputs -- On/off signals used to actuate control board annunciators
- o Channel trip outputs -- On/off signals us. 2 to control 120-vac input relays of the Solid State Protection System (SSPS), or a relay-based protection system, for reactor trip and safeguards actuation signals

2.1.3 Design Features

Major derign features of the Eagle 21' Process Protection Upgrade System are described in the following paragraphs.

2.1.3.1 Single Failure Criterion

2.1.3.2 Instrument Power Source

2. 3.3 Channel Integrity

The Eagle 21^{∞} Process Protection Upgrade System has been designed to perform its protective functions under extreme operating conditions relating to its environment, its energy supply, any malfunctions, and any accidents.

2.1.3.4 Channel Independence

2.1.3.5 Control and Protection System Interaction

The Eagle 21th Process Protection Upgrade System functions with complete independence from the plant's control systems. (Control systems include remote indicators, computer data points, and annunciators as well as circuits that automatically control plant parameters.) Protective functions are electrically isolated from any fault or malfunction that occurs in the control systems.

2.2 FUNCTIONAL DESCRIPTION

The following paragraphs provide a brief functional description of the Eagle 21^{∞} Process Protection Upgrade System, based on the simplified functional block diagram shown in figure 2-4.

2.2.1 Block Diagram

a,c

Figure 2-4. Eagle 21th Simplified System Block Diagram

a,c

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2.3 CABINET DESCRIPTION

The Eagle 21 $^{\rm w}$ Process Protection Upgrade System is housed in existing process instrumentation cabinets to which structural bracing and mounting rails have been installed. Cabinet front and rear views are shown in figures 2-6 and 2-7. [

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å,¢

Figure 2-5 Man-Machine Interface (MMI) Cart

a,c

Figure 2-6 Cabinet Front View



Figure 2-7 Cabinet Rear View

SECTION 3 EAGLE 21 SYSTEM CONFIGURATION

3.1 DESCRIPTION

The Eagle 21th system tested (Qualification Unit 2) is an exact replica of Watts Bar Nuclear Power Station protection rack 13. This rack contains the following instrument loops (subsystems):

- p Delta T/Tavg, Protection
- Steam Generator Wide Range Level, Post Accident Monitoring (PAM) (2 Channels)
- o Pressurizer Vapor Temperature, (PAM)
- o Residual Heat Removal Pump Discharge Temperature, (PAM)
- o Reactor Coolant System Wide Range Pressure, (PAM)

3.2 CONFIGURATION/DESIGN LEVEL DRAWINGS

The following drawings/revision levels are attached to document the system configuration tested:

Drawing Description	Drawing Number/Revision
Terminal Block Wiring Diagram, Protection Set 4	1-47043, PW-13, Revision 3E
Process Control Block Diagram, Delta T/Tavg System	108D408, sheet 10, Revision 11
Process Control Block Diagram, WR SG Level	108D408, sheet 34, Revision 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temperature	108D408, sheet 38, Revision 4

Drawing Description

Drawing Number/Revision

Process Control Block Diagram, RHR Pump Discharge Temperature 108D408, sheet 39, Revision 5

Process Control Block Diagram, RCS Wide Range Pressure

1080408, sheet 43, Revision 1

Eagle 21™ Schematic Diagrams, Rack 13 Protection Set 4

1856E69, sheet 2 Revision 2

The following drawings/revision levels are referenced to document the system hardware tested:

90		70		26.					à			4		
T) w	F-25 To 1	U. H 18	100		15.	201	m.	SK.	- 49	904	*	*	ph,	m.
DY	- Q Y	4.1.5	1.64	160	₩.	ъ.	₩.	т		34	1		w	

Drawing Number/Revision

Cabinet General Assembl	y
-------------------------	---

1870E97G01, Revision 3

Analog Input Board, 10-50, 4-20 mA 5367C57, Revision 4 (EAI-G01)

WR RTD Input Board (ERI-GO1)

5368029, Revision 2

NR RTD Input Board (ERI-GO2)

5368C29, Revision 2

Partial Trip Output Board (EPT-GO1)

2033786, Revision 2

Digital Contact Output Board (ECO-GO1) 5367C61, Revision 3

Analog Output Board 10-50 mA (EAO-GO2)

53670° . Revision 3

Power Distribution Box (GO1)

1871E34, Revision 3

Termination Module Assembly 0-10 Volt (G01)

2033779, Revision 1

Drawing Description

Drawing Number/Revision

Termination Module Assembly 4-20 mA (GO1)

2D27362, Revision 1

Termination Module Assembly 10-50 mA (GO6)

2027362, Revision 1

Baseline Design Document

956093, Revision 0

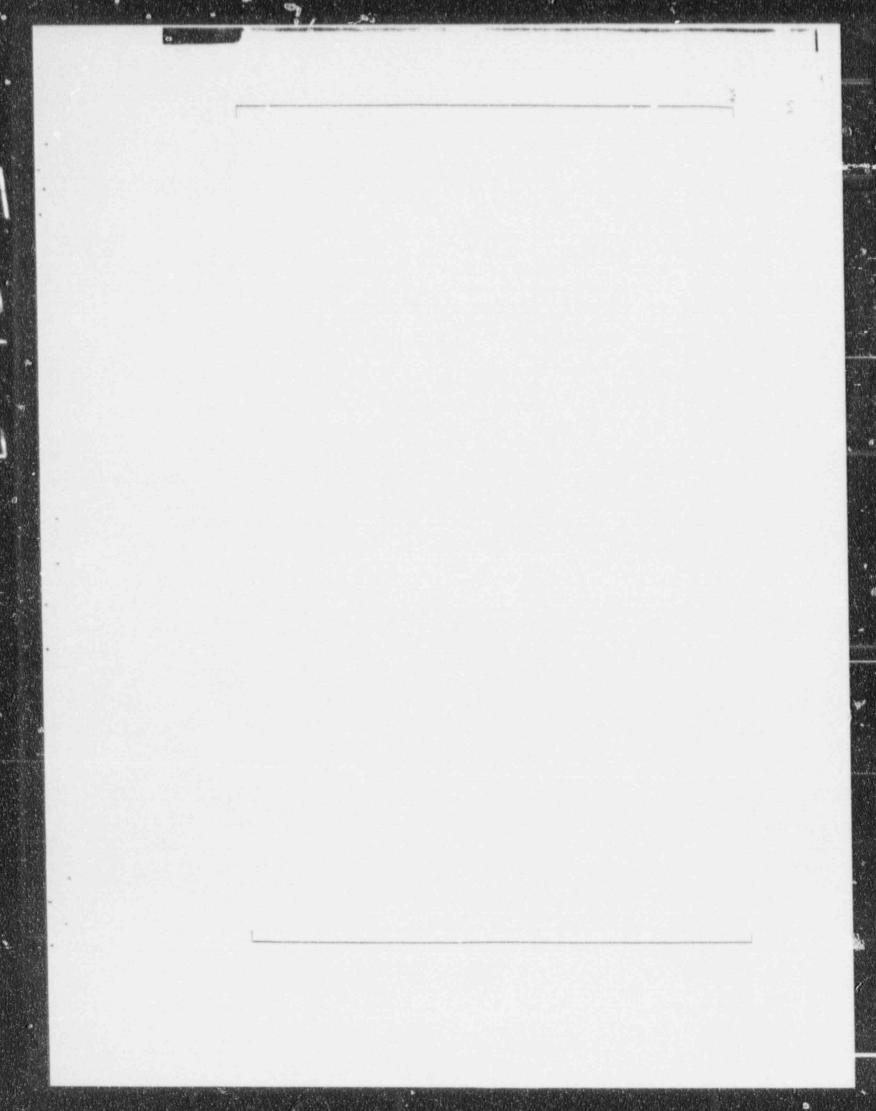
*Digital Contact Output Board (ECO-GO1) 5367C61, Revision 4

*Partial Trip Output Board (EPT-GO1) 2033786, Revision 3

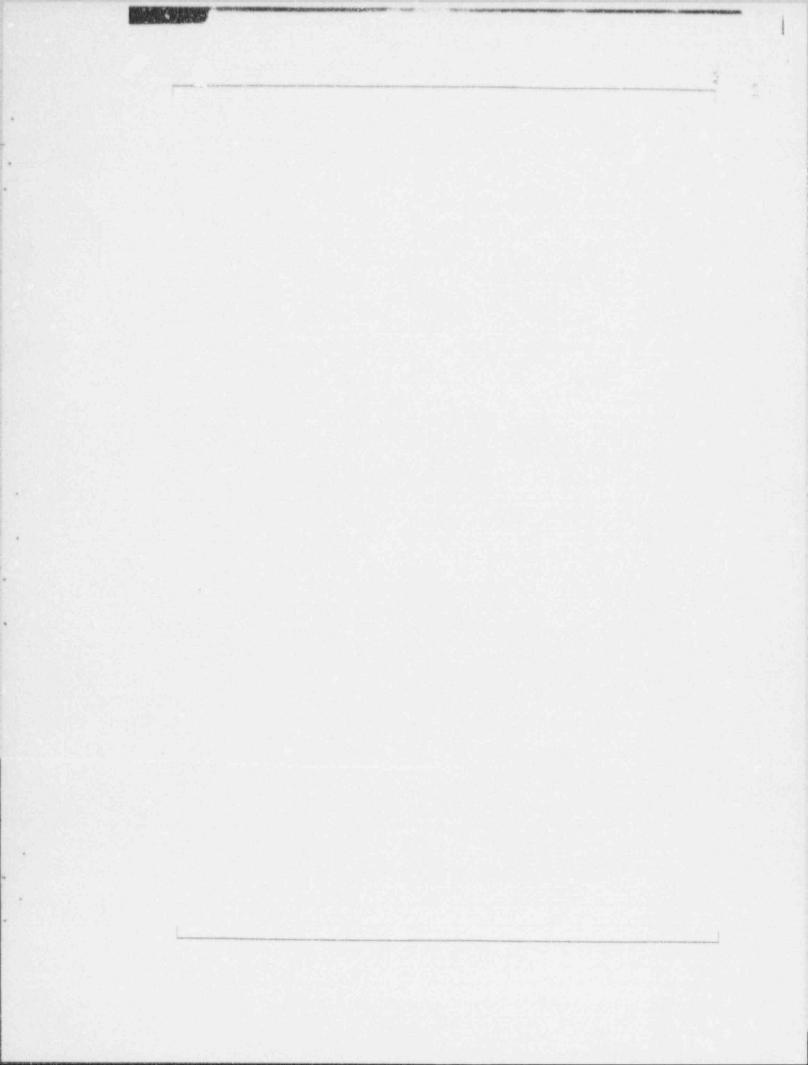
1/O and microprocessor boards were configured per design specification 956073. Revision D.

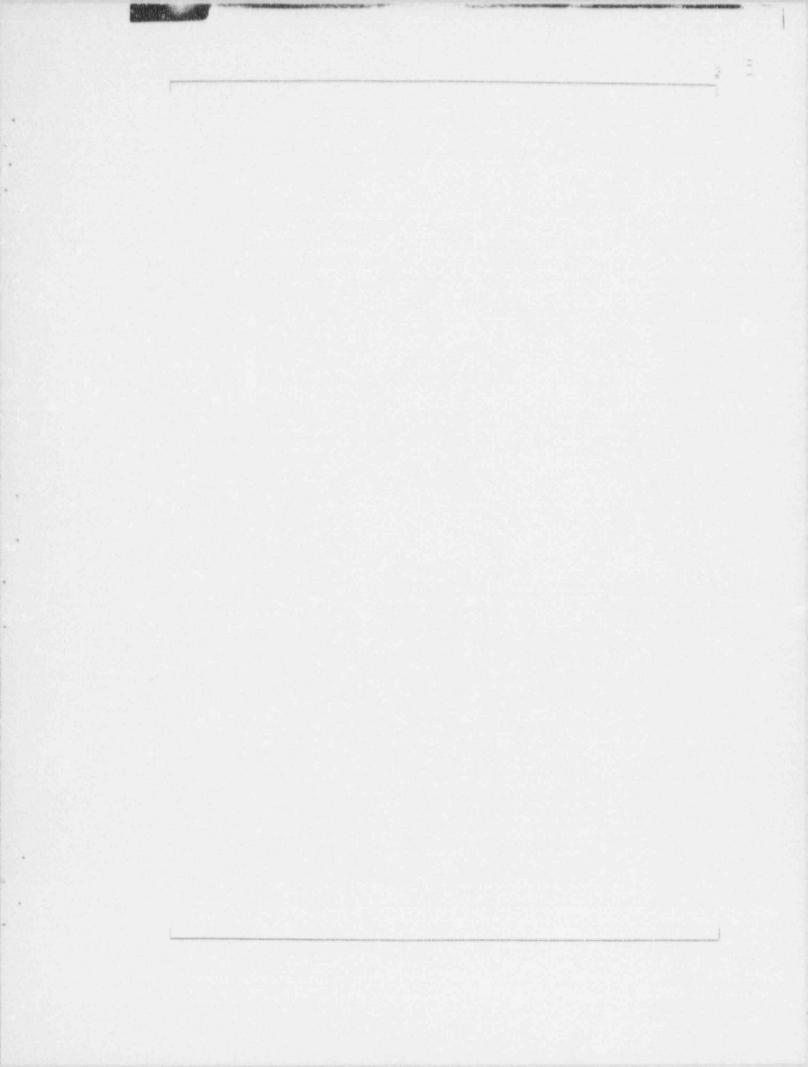
System software used has been retained on permanent file.

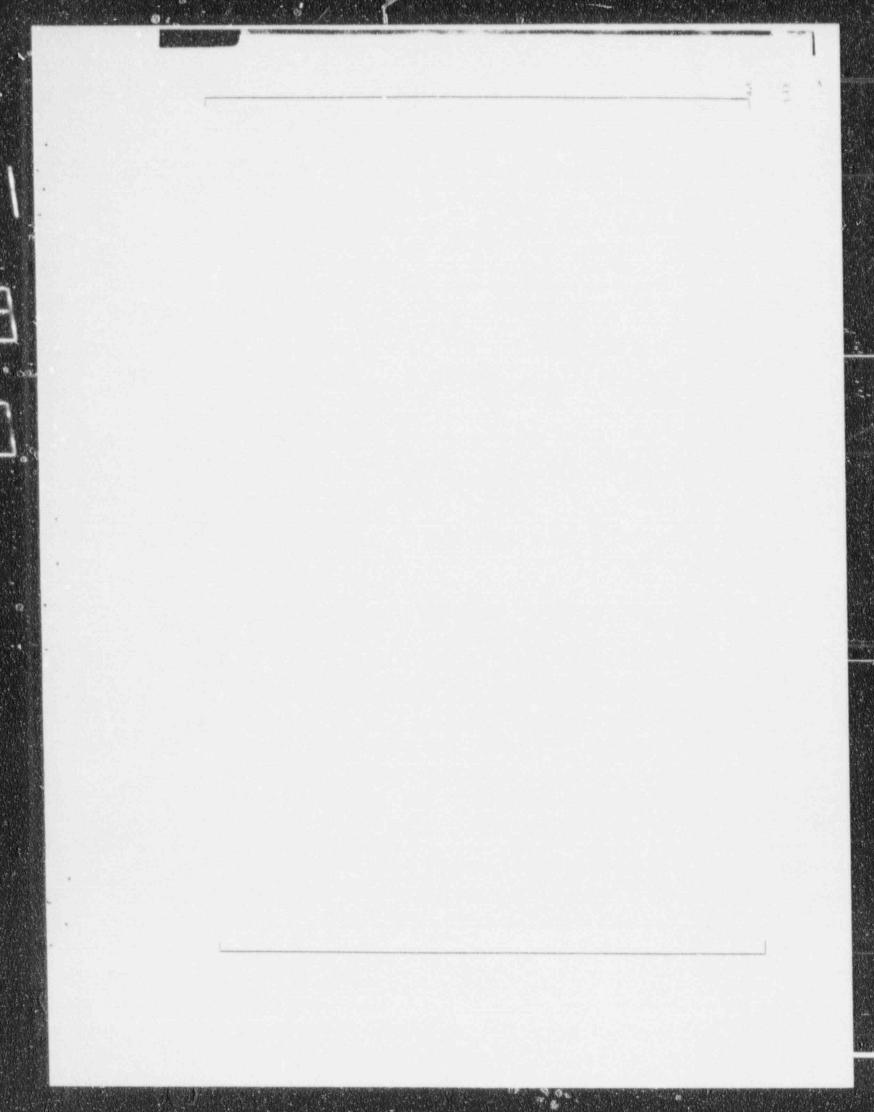
^{*}Boards modified to successfully complete fault testing. Modifications made and required retests are described in sections 8.2, 8.3 and Appendix A.

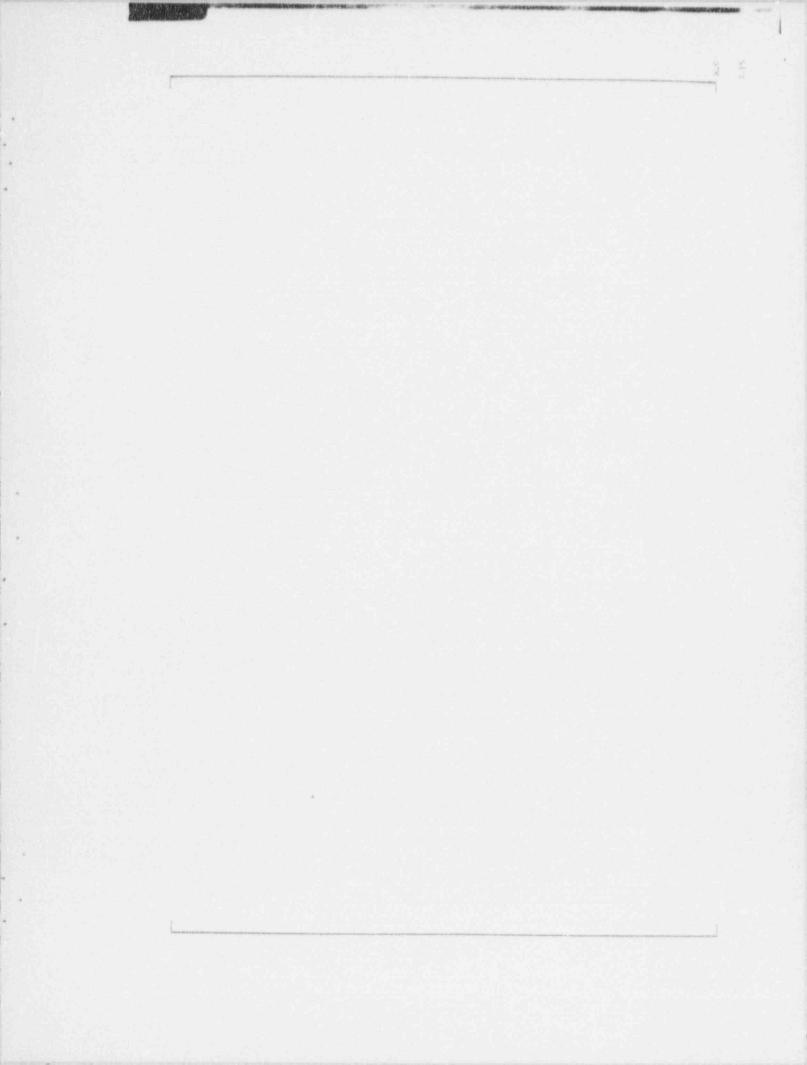


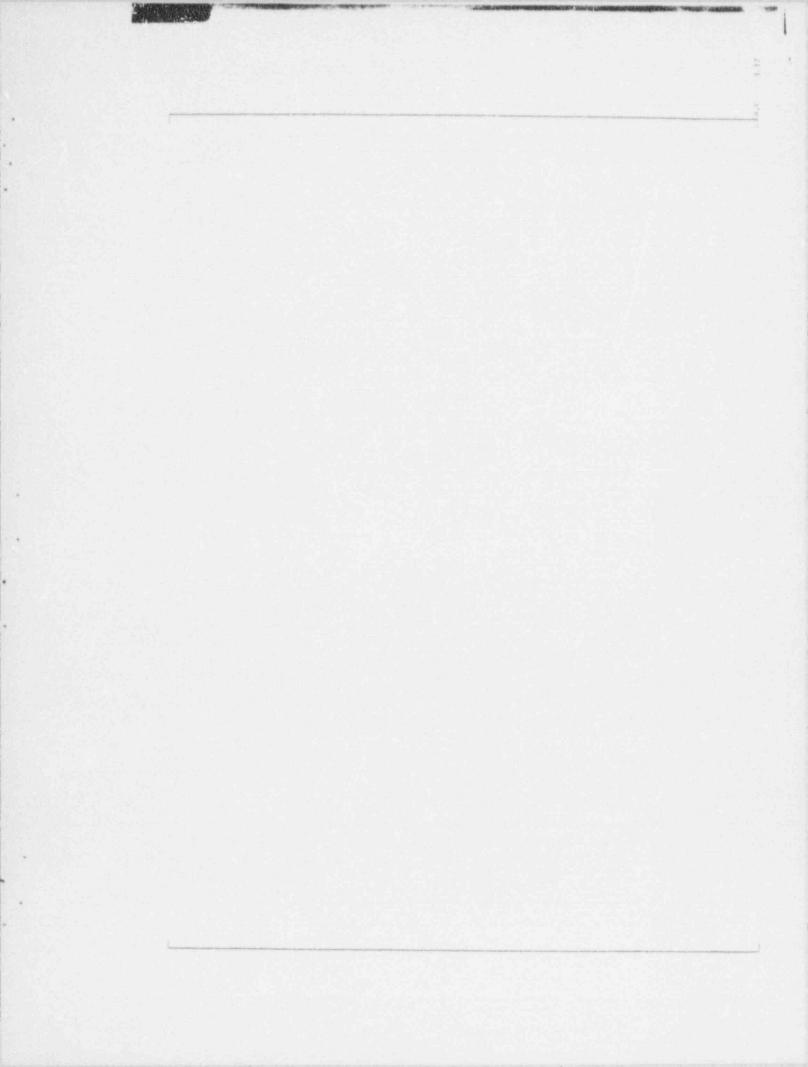












SECTION 4 ISOLATION DEVICES PHILOSOPHY

4.1 DESCRIPTION

The Eagle 21^{∞} System uses the output signal conditioning boards as an isolation barrier between field level signals and the microprocessor subsystem. The Eagle 21^{∞} uses the following types of isolation devices for interfacing Class 1E signals with non-1E equipment.

isolator Board Type	Isolation De	avice
Analog Output Board (current loop), EAO		
Digital Contact Output Board, ECO		
Partial Trip Output Board, EPT	Table 1	

In addition, high voltage transient protection is provided for each cabinet input/output, including the ac power feed, by transient suppression circuitry. Fault currents are limited by preferred failure mode components.

SECTION 5 TEST DESCRIPTION

5.1 NOISE TESTS

The Eagle 21^M system is a microprocessor upgrade to existing analog plant instrumentation and control (I & C) equipment. The Eagle 21^M is installed in the existing plant I & C process racks. The field termination wiring in these racks does not meet the spatial separation requirements between Class 1E and non-1E wiring as specified by IEEE-384-1977 and Nuclear Regulatory Guide 1.75 Rev. 2. The purpose of the noise tests in to demonstrate that the protective actions of the Eagle 21^M system are not affected by noise injected into or adjacent to class non-1E wiring. Protective action is defined as the ability to generate a partial trip output signal upc. input signal demand. NUREG 1.75 Appendix 1 section 4.5 allows the use of tests to demonstrate that class 1E circuits are not degraded when minimum separation distance is not maintained. The noise sources were chosen to emulate worst-case noise conditions which may be present on non-1E wiring in the Eagle 21^M process rack.

5.1.1 Test Outline

The Eagle 21™ equipment was subjected to the following noise sources:

- o Random Noise Test (Antenna Coupled)
- o Crosstalk Noise Chattering Relay Test (Antenna and Direct Coupled)
- o Military Specification MIL-N-19900B Noise Test (Antenna Coupled)
- o High Voltage Transient Noise Test (Antenna Coupled)
- o Static Noise Test (Antenna and Direct Coupled)

For the random, high-voltage transient and military specification noise tests, the noise source was antenna coupled to the class non-1E field wiring under test. The noise source was applied to a 40-foot antenna wire adjacent to a 40-foot length of unshielded class non-1E field wiring. The antenna was brought directly into the cabinet and bundled with Class 1E input/output cables upon entering the process rack (see figure 5-1).

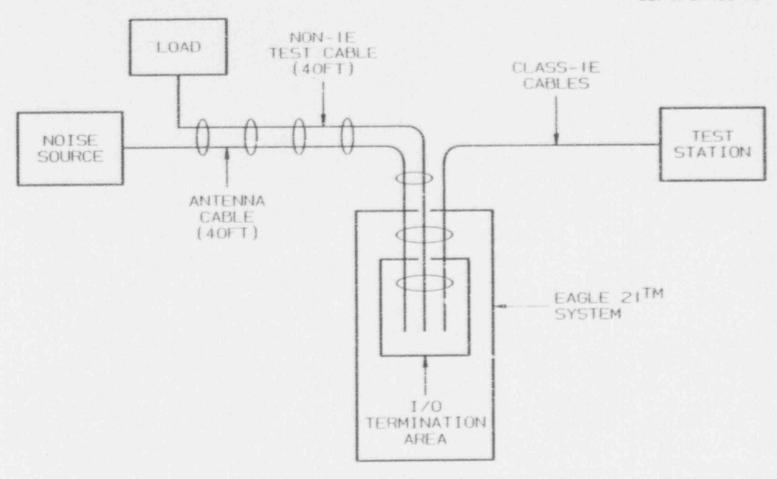


Figure 5-1. Noise Test Setup (Antenna Coupled) Used for Random, HV Transient, Mil-N and Crosstalk Tests

The non-1E test cable was terminated with a nominal load value. Load values for each board type tested are given below:

Isolatur Board Type

Load

10-50 mA current loop output, EAO Digital Contact Output, ECO Partial Trip Output, EPT

*Open circuit and short circuit
**40 watt incandescent light bulb

The crosstalk and static noise tests were conducted similarly, except that an additional test was performed where the noise source was applied directly to the non-'E wiring. To prevent damage, the isolator was disconnected at the Eagle 21% termination frame and the disconnected non-1E wires shorted to complete the crosstalk noise circuit loop. The disconnected non-1E wires were open-circuited for the static noise test (See figures 5-2, 5-4, and 5-7).

Each noise test run consisted of 2 minutes of pretest data, 2 minutes of test data (noise source supplied), and 2 minutes of post-test data.

For a detailed description of the noise test setup, see section 6.2.1.

For a detailed test sequence, channel monitoring, and system external connection information, see the noise test procedure in appendix C.

5.1.2 Random Noise Test

This noise source was generated by a random noise generator [].c Its output was fed through a power amplifier [1.c

^{*} Since the contact output board nominal load is unknown, both open and short circuit tests were performed.

^{**} This load is considered conservative since the resultant loop impedence to transient signals is low compared to the inductive load this board would normally service.

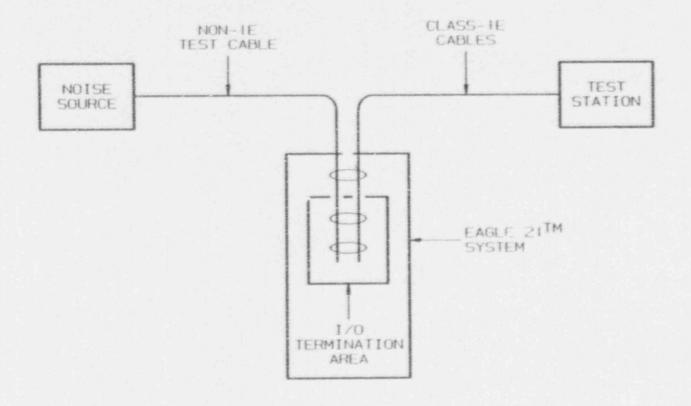


Figure 5-2. Noise Test Setup (Direct Coupled) Used for Crosstalk and Static Noise Tests

The radiated random noise characteristics are as follows:

Peak value: 21

Frequency: 20 kHz - 10 MHz

Figure 5-3 shows the random noise source test setup.

5.1.3 Crosstalk Noise - Chattering Relay Test

A dc and an ac relay were used to generate a radiated cross-alk noise. The relays were set in a "chattering" or "buzzer" mode by wiring the normally closed relay contacts in series with the relay coil. The following types of relays were used during the crosstelk noise-chattering relay test:

- o Relay with a 118 Vac coil, 0.3 amp nominal
- o Relay with a maximum rating of 600 Vdc, 125 Vdc coil, 0.22 amp rominal

Figure 5-4a shows the dc crosstalk noise source -- chattering relay test setup. Figure 5-4b shows the ac crosstalk noise source -- chattering relay test setup.

5.1.4 Military Specification Noise Test

Military specification noise testing was performed using switched cycling noise sources with the characteristics of Noise Sources No. 1 and No. 2 in Military Specification MIL-N-19900B.

The characteristics for Noise Source No. 1 were:

Voltage: 115 Vdc Inductance: 3 H

Resistance: 500 ohm

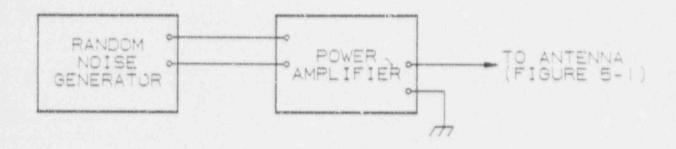


Figure 5-3. Random Noise Source Test Setup

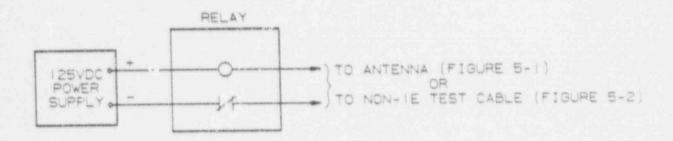


Figure 5-4a. Crosstalk Noise -- Chattering dc Relay Test Setup

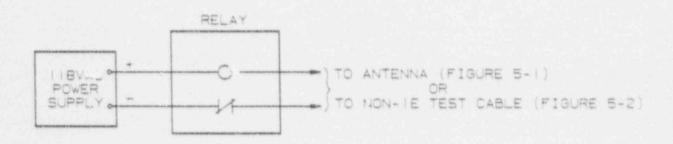


Figure 5-4b. Crosstalk Noise -- Chattering ac Relay Test Setup

The characteristics for Noise Source No. 2 were:

Voltage: 115 Vac Inductance: 10 mH Resistance: 2 oim

Repetition rate for both noise so; roes was 10 on-off cycles per minute.

Figure 5-5 shows the military specification noise source test betup.

5.1.5 High Voltage Transient Noise Test

This noise source was generated from a surge transient generator () coupled to an isolation network box [).c The high voltage transient noise characteristics are in accordance with IEEE-472-1974 as follows:

ECREST: 3.3 kV Surgs Frequency 1.25 MHz Time to 1/2 ECREST * 6.4 us Repetition rate: 120 Hz

Figure 5-6 shows the high voltage transient oice source test setup.

5.1.6 Static Noise Test

This noise source was generated using a step-up transformer [$\rm J_{-c}$ A value of 580 Vrms at 60 Hz was injected into the non-1E test cable and into the antenna assembly.

Figure 5-7 shows the static noise test setup.

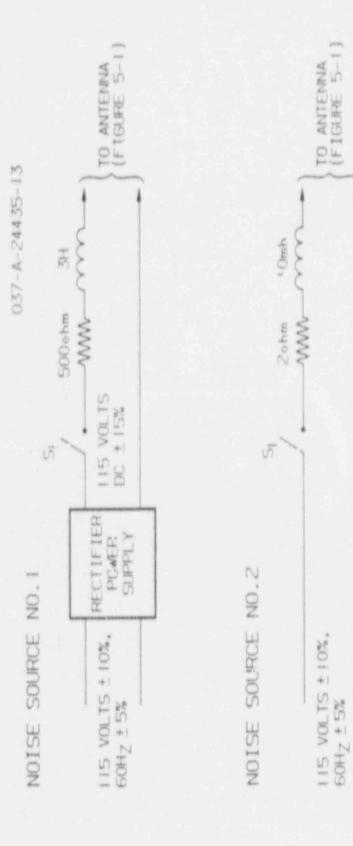


Figure 5-5. Military Specification Noise

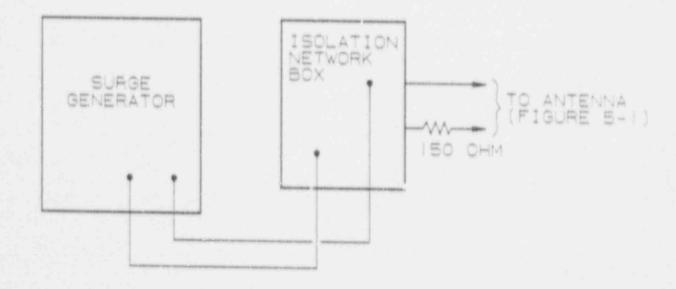


Figure 5-6. High Voltage Transient Noise Source Test Setup

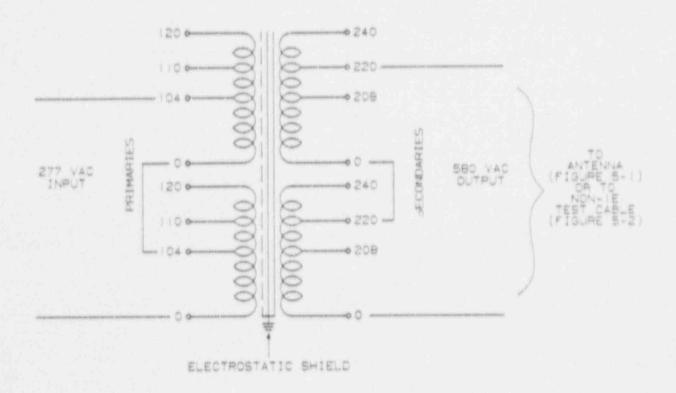


Figure 5-7. Static Noise Source Test Setup

5.2 FAULT TESTS

The purpose of the fault tests is to demonstrate that credible faults injected into the non-1E system do not propagate across the class non-1E to class 1E isolation barrier or from channel to channel within the Eagle 21th process rack. These tests are designed to verify that the Eagle 21th system isolation devices are in compliance with IEEE-279-1971, IEEE-384-1981, IEEE-603-1980, and Nuclear Regulatory Guide 1.75 Rev. 2 concerning the physical independence of class 1E circuits and class 1E/non-1E interaction.

5.2.1 Test Outline

Maximum predible fault voltages were determined to be 580 Vac and 250 Vdc per previous protection system tests (7300 system, QDPS, etc.). In addition, 125 Vac and 125 Vdc tests were performed where applicable. A fault was considered applicable only if the fault challenged the nominal voltage or current ratings of the channel under test. For cases where 125 Vac and 125 Vdc tests were considered not applicable, 580 Vac and 250 Vdc tests were performed thus enveloping the lower voltage tests.

Fault voltages were applied line to ground and line to line (ungrounded) into the isolator terminals. Tables 5-la and 5-lb list tests performed by board type. Figures 5-8a and 5-8b show the ac and dc fault connections. Positive and negative dc voltage line-to-ground faults were applied.

5.2.2 Test Implementation

Ac fault voltages were generated using a 7.5 KVA isolation transformer []. $_{\rm C}$ Figures 5-9 and 5-10 show the transformer connections used.

Do fault voltages were generated using a 250 V, 20 A do power supply [... Two external 3300 μf capacitors were added to increase the potential energy available for fault application (See figure 5-11).

TABLE 5-1a LINE TO GROUND FAULT TESTS PERFORMED

Isolator Board Type

Faults Applied

Partial	Trip Output, Energized	125 Vdc, 125 Vac, 250 Vdc, 580 Vac
Partial	Trip Output, Deenergized	250 Vdc, 580 Vac
Digital	Contact Output, NO, Energized	250 Vdc, 580 Vac
Digital	Comment to "put, N", Energized	250 Vdc, 580 Vac
Current	Loup Ostrui. Malu mA	125 Vac. 125 Vdc. 250 Vdc. 580 Vac

TABLE 5-16 LINE TO LINE FAULT TESTS PERFORMED

Isolator Board Type

Faults Applied

Partial	Trip Output, Energized	125 Vac, 125 Vdc, 250 Vdc, 580 Vac
Partial	Trip Output, Deenergized	250 Vdc, 580 Vac
figital	Contact Output, NO, Energized	125 Vac. 125 Vdc, 250 Vdc, 580 Vac
Digital	Contact Output, NC, Energized	250 Vdc, 580 Vac
Digital	Contact Output, NO, Deenergized	250 Vdc, 580 Vac
Digital	Contact Dutput, NC, Deenergized	125 Vac. 125 Vdc. 250 Vdc. 560 Vac
Current	Loop Output 10-50 mA	125 Vac, 125 Vdc, 250 Vdc, 580 Vac



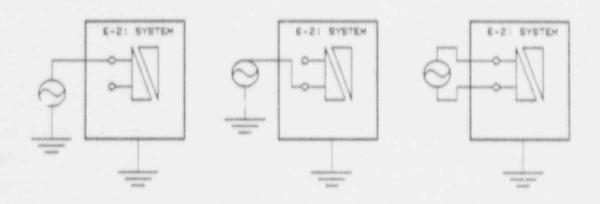


Figure 5-8a. Ac Fault Connections

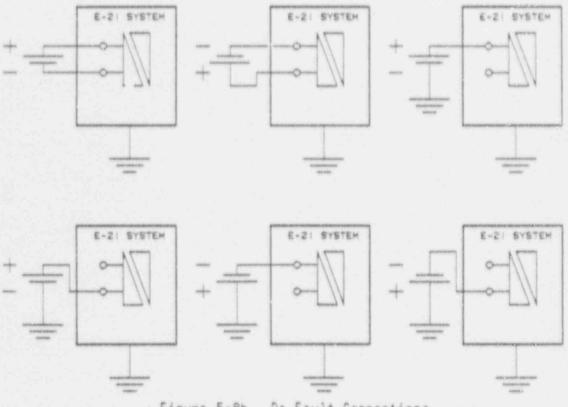


Figure 5-8b. Dc Fault Connections

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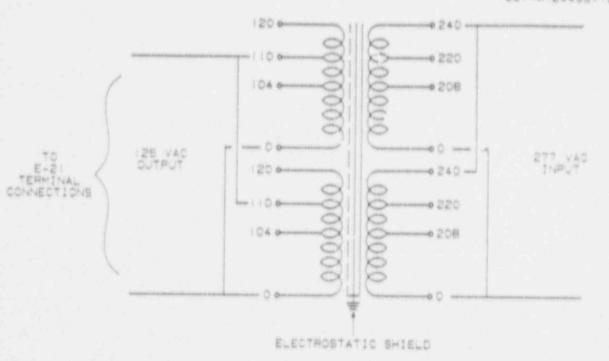


Figure 5-9. Transformer Connection for the 125 Vac Fault Source

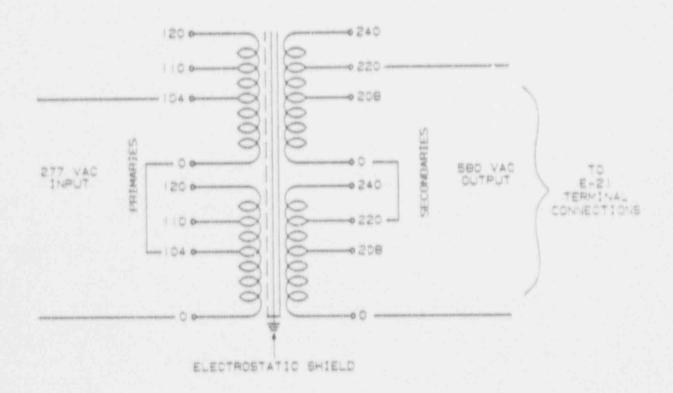


Figure 5-10. Transformer Connection for the 580 Vac Fault Source

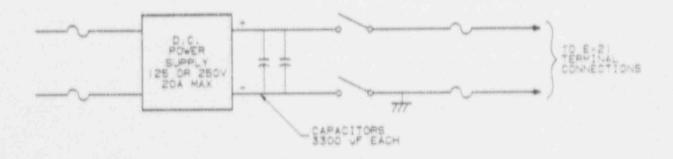


Figure 5-11. Do Power Supply Fault Connections

Each fault test consisted of a 1-minute pretest run, a 1-minute application of fault and a 1-minute post-test run. Repairs required following each fault test were recorded noting all failed components.

For a detailed description of the fault test setup, see section 6.2.2.

For detailed test sequence, channel monitoring, and system external connection information, see the fault test procedure in Appendix C.

5.3 SURGE WITHSTAND CAPABILITY (SWC) TEST

The SWC tests were conducted under normal operating conditions of the system in accordance with IEEE 472-1974. The purpose of this test was to determine: (1) the protective actions of the Eagle 21% system are not affected by application of the surge withstand test wave to the designated class non-IE to class IE isolators. (2) that no component failures occurred, and (3) that no change in channel calibrations occurred due to the application of the surge withstand test wave.

5.3.1 Test Outline

All system inputs/outputs were surge tested in the common and transverse modes including the system power supply input circuitry.

Each of the following system interfaces were tested:

- Digital Contact Output (NO and NC configurations), class non-1E/1E isolator
- o Partial Trip Output (energized and deenergized conditions), class non-1E/1E isolator
- o Current Loop Output 10-50 mA, class non-1E/1E isolator
- o Current Loop Input (4-20 mA, 10-50 mA, with and without loop power supply)
- o WR RTD Input

- o WR RTD Input (0-10 volt application)
- o NR RTD Input
- o Cabinet AC power feed

5.3.1.1 Common Mode Test

For this test, one terminal of the test generator was connected to each system input or output connection group. The other terminal of the test generator was connected to the ground of the surge generator (See figure 5-12a).

5.3.1.2 Transverse Mode Test

For this test, the terminals of the test generator were connected to the high and low of each system input or output signal pair (See figure 5-12b).

5.3.2 Test Implementation

The surge withstand capability test was carried out by using a surge generator [] and an isolation network []. $_{\rm C}$

The SWC test wave generated was in accordance with IEEE-472-1974 and had the following characteristics:

FCREST * 2.5kV Surge Frequency * 1.25 MHz Time to 1/2 E_{CREST} * 6.4 us Repetition Frequency = 120 Hz

Each SWC test run consisted of a 2-minute pretest run, 2-second application of the SWC test wave, and a 2-minute post-test run.

Figure 5-12c shows a schematic diagram of the equipment connections which were implemented during the SWC test.

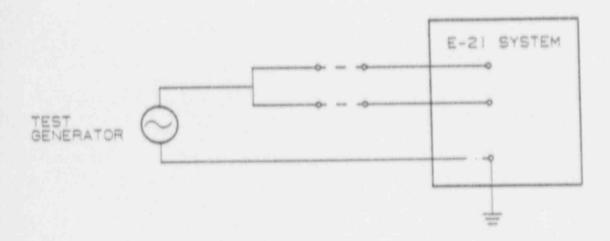


Figure 5-12a. Common Mode Surge Withstand Capability Test Connection

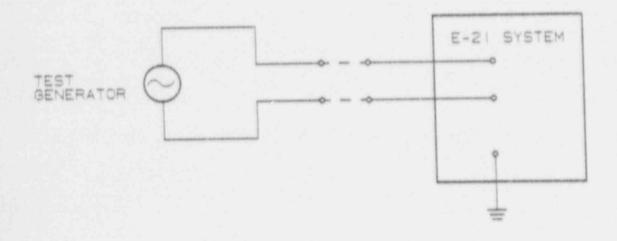


Figure 5-12b. Transverse Mode Surge Withstand Capability
Test Connection

A detailed description of the SWC test implementation is given in the SWC Test Setup Description, section 6.2.3.

For detailed test sequence, channel monitoring, and system external connection information, see the SWC tast procedure in appendix C.

5.4 RADIO FREQUENCY INTERFERENCE (RF1) SUSCEPTIBILITY TEST

The purpose of this is susceptibility test was to evaluate the performance of the system when subjected to electromagnetic fields such as those generated from portable radio transceivers or any other devices that generate continuous-wave radiated electromagnetic energy.

5.4.1 Test Methodology

The RF1 suscept bility tests were conducted in accordance with SAMA Standard PMC 33.1-1978. The classes of field strengths the system was subjected to were 3 V/m and 10 V/m over the entire frequency range of 20 MHz to 1 GHz.

Two types of tests were performed. In the first, referred to as a "modulation" test, a computer-controlled sweep of the signal generator was utilized. [

].b.c In the second test, referred to as a "keying" test, the signal generator output was turned on and off at 1-second intervals and with very short rise and fall times to simulate the keying of a transceiver.

5.4.2 Test Location

The tests were carried out in a shielded enclosure (anechoic chamber) [

5.4.3 Test Equipment

Two types of antennae were used during the testing. A biconical antenna covered frequencies ranging from 20 MHz to 160 MHz, and a log periodic antenna covered frequencies ranging from 160 MHz to 1 GHz.

Two power amplifiers were used to cover the whole frequency range. The first amplifier covered 20 MHz to 500 MHz; the second amplifier covered 500 MHz to 1 GHz.

5.4.4 Test Procedure

Calibration testing was conducted to generate a calibration data file for the control computer for the signal generator. Once calibration testing was completed, modulation and keying tests were performed on the system.

A detailed description of the radio frequency interference test implementation is given in the Radio Frequency Interference Test Setup Description (section 6.2.4).

For detailed test sequence, channel monitoring, and system external connection information, see the Radio Frequency Interference test procedure in appendix C.

5.4.5 Calibration Test

The calibration data files were generated for 3 V/m and 10 V/m over the entire frequency band (20 MHz to 1 GHz), for both vertical and horizontal polarizations, for use in implementing the modulation and keying tests. Figure 5-14 is a photo of the anechoic chamber showing the log periodic antenna in the horizontal polarization calibration [

1.0

0719c.1b-042888

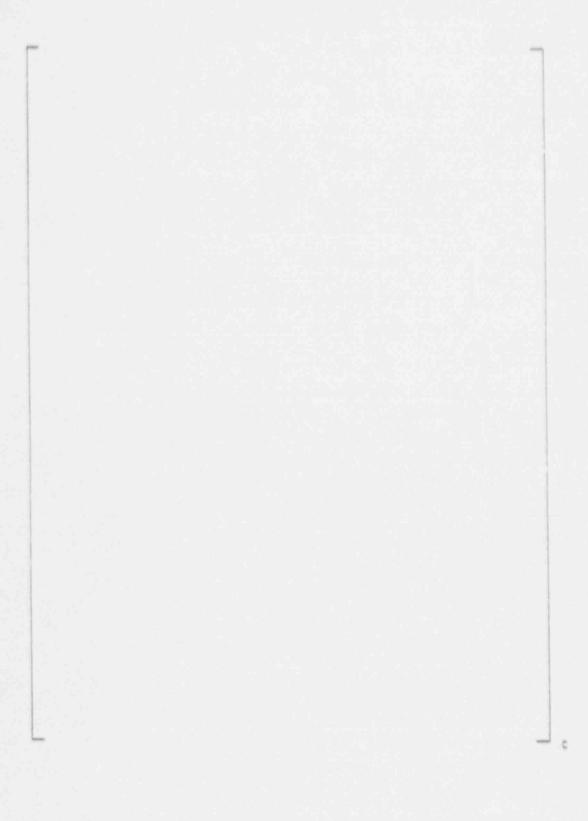


Figure 5-13. Radio Frequency Interference Equipment Test Setup

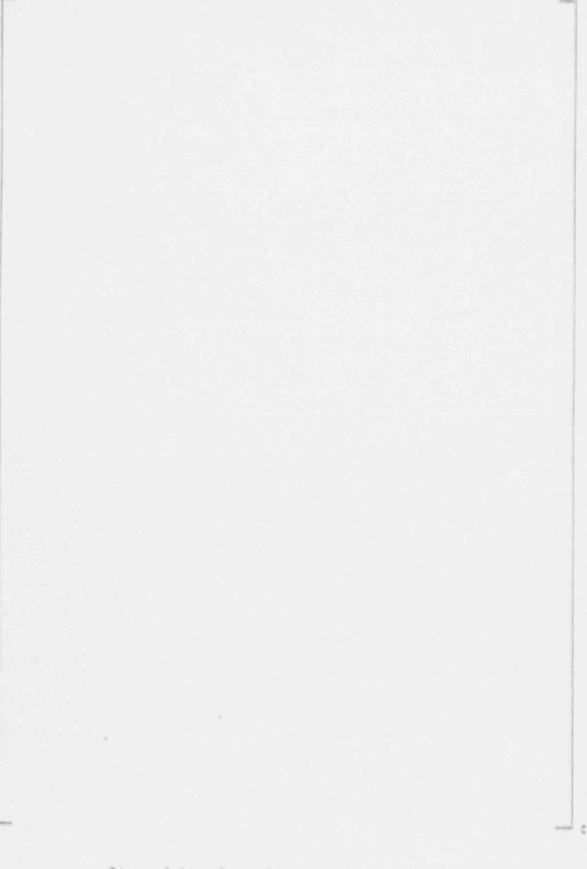


Figure 5-14. Radio Frequency Field Calibration

_ b,c 5.4.6 Modulation Test

0719c.1b-042888

Figure 5-15. Bloc: Diagram of Radio Frequency Interference Calibration Tests

Figure 5-16. Cabinet Subject to Radio Frequency Field

ь,с

Figure 5-17. Block Diagram of Radio Frequency Interference Modulation Tests

b.c

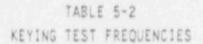
A detailed description of the RFI test implementation is given in the RFI Test Setup Description, Section 6.2.4.

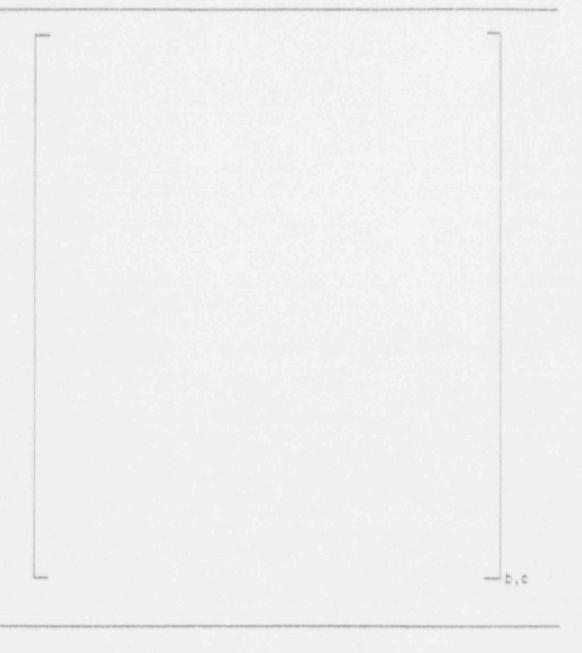
For detailed test sequence, channel monitoring, and system external connection information, see the RFI test procedure in Appendix C.

5.4.7 Keying Test

The keying test frequency selection was performed manually. The most susceptible points, as determined by the modulation tests, were subjected to the keying test. At least three data points per octave were tested. Table 5-2 shows the keying test frequencies.

b . r





During the keying test, only the front of the cabinet was targeted, because this was considered to be the "most susceptible side" to the RF field. Vertical and horizontal polarizations were implemented.

b,c

07190:16-042888

Figure 5-18. Block Diagram of Radio Frequency Interference Keying Tests

SECTION 6 TEST SETUP AND MONITORING

5.1 TEST SETUP

The test setup consisted of an input/output simulator and recording test station. Test equipment included a data logger, tape recorder strip chart recorder, voltmeter, and an oscilloscope. Figure 6-1 shows the cabinet and field cable setup. Figure 6-2 shows the test equipment setup. Figure 6-3 is a test configuration block diagram.

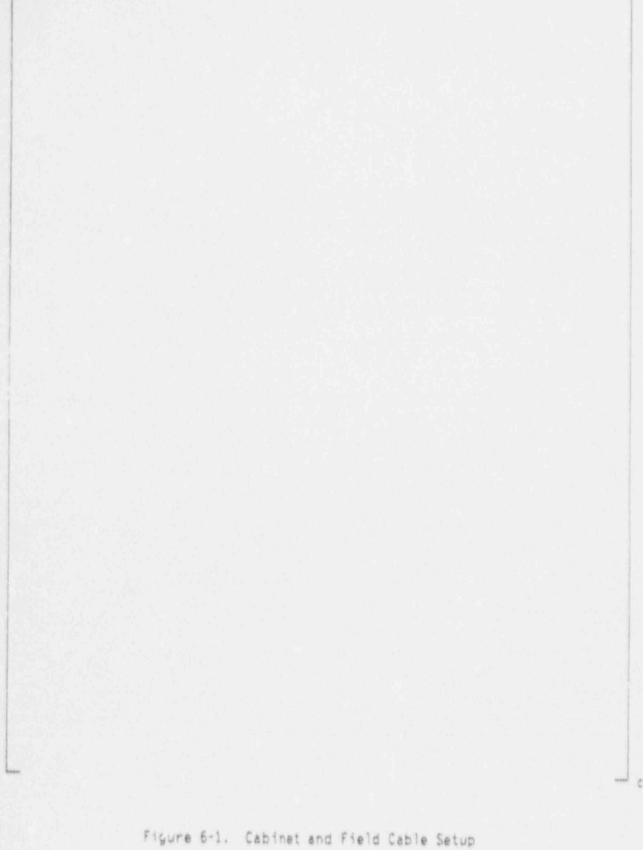
6.1.1 System Connections

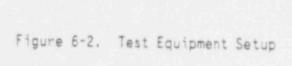
Forty-foot field cables were routed from the test station through the cabinet top entry and were terminated at the field terminal blocks. Cable shields were terminated at the field terminal blocks and left open at the test station per standard wiring practice. All cables were bundled together (IE and non-1E) upon entry into the cabinet. System external connection diagrams are provided in section 3.

6.1.2 Simulated Input Signals

Input signals were simulated in a manner which replicates, as close as possible, actual plant sensors. The listing below gives signal type, simulation method, and circuit figure reference:

Input Signal Type	Simulation Method	Figure
0 - 100	Voltage source	N/A
4-20 mA/10-50 mA	Transmitter	6-4
Wide Range RTD	Potentiometer	6-5
Narrow Range RTD	Precision resistor	6-6
	network	





1

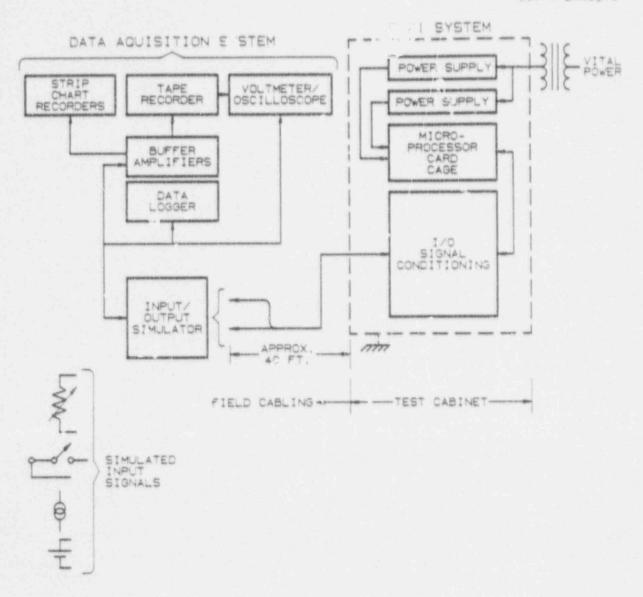
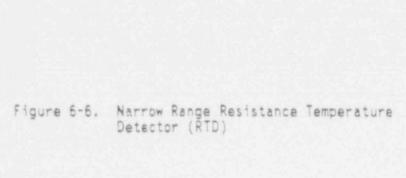


Figure 6-3. Test Configuration Block Diagram





Actual simulated input values for each test are specified in the test procedures, appendix C.

6.1.3 Data Acquisition System

The data acquisition system provided a record of cabinet performance during each test. The data acquisition system consisted of a tape recorder, strip chart recorder and a data logger.

The listing below gives output signal type, monitoring method, and circuit figure reference:

Output	Monitoring	
Signal Type	Method	Figure
10 - 50 mA	resistor	6-7
Trip Output	120 Vac detector, status light	6-3
Contact Output	voltage/resistor	6-9

Actual output points monitored for each test are specified in the test procedures, appendix C.

6 J.3.1 Tape Recorder

A 14-channel FM tape recorder was used to provide a permanent record of system performance before, during and after each abnormal event (noise, surge, RFI, etc.). [

b,c

Tape recorder monitored signals were processed through buffer amplifiers.

6.1.3.2 Data Logger

The digital data logger was used for pre-test and post-test verification of system status. Prior to each test, it was used to generate a printout for all



Figure 6-9. Contact Output Monitoring

monitored channels to verify that system performance was normal. After each test, another printout of the data for all monitored channels was generated to verify that system performance had not degraded during testing. These printouts were then attached to the backs of the data sheets. To prevent noise spikes caused by periodic data sampling, the data logger was not connected during testing.

6.1.3.3 Strip Chart Recorder

Two 8-channel strip chart recorders were used as a continuous monitor of system performance before, during, and after each abnormal event. An event marker was used to mark the beginning and end of each abnormal event. The monitored signals were processed through buffer amplifiers. [

b,c

6.2 TEST MONITORING

The tests were monitored in accordance with the acceptance criteria cutlined in section 7. Selected system input/output points were monitored to measure system performance during the noise, fault, surge, and radio frequency interference testing. The man-machine interface (MMI) terminal was disconnected during the test runs. The MMI connection can be construed as an additional antenna. During actual plant operation, the MMI is only connected during cabinet testing and only one protection set is allowed in test at a time. Thus, the MMI connection is not considered common mode [

].b,c The MMI was connected periodically to trouble-shoot and interrogate input signal processing performance.

Specific data points monitored were determined by the particular test being performed. In general, points monitored were chosen to best monitor overall Eagle 21^{∞} system performance.

Data sheets, strip chart recorder printouts, data logger printouts, and tape recorder log sheets were utilized to record data. Data sheets are attached at the end of this section for information.

6.2.1 Noise Test Setup Description

Eagle 21^∞ system input/output performance, while subjected to the noise tests described in section 5.1, was monitored in the following manner:

- o putputs -- four analog output channels were monitored

 v du. 7 the noise tests. The channels monitored

 finals processed by current loop, wide range RTD, and

 put signal conditioning boards. Thus, system

 processing performance was measured.
- Digital outputs ... single variable NR RTD (Thot3) was chosen to toggle all six Delta T/Tavg System trip outputs. All six trip output channels were toggled utilizing the variable RTD circuit shown in Figure 6-6. The control relay was cycled continuously during pre-test, test and post-test runs [

I.b.c. The Delta T/Tavg system inputs were set just below and above the trip output toggle point (.2% or less). The Delta T/Tavg system utilizes current loop, NR RTD and O-10 volt analog input signals to generate partial trip output signals (see section 3 for system block diagrams). Thus, any significant degradation in system input signal processing would result in a trip output status failure. A normally open contact output channel was also monitored. The contact output was normally energized throughout the test.

Trip output status was monitored continuously during the noise tests using a strip chart recorder.

Analog/digital channels adjacent to the non-1E channel under test were chosen for monitoring to emulate worst case system configuration. See figure 6-10 for the noise test data sheet.

EAGLE 21 M NOISE TEST REPORT

TEST TYPE/PROCE	DURE NUMBER (REV)			
DATE	SPECIAL SECURITY CONTRACTOR CONTRACTOR CONTRACTOR			
NOISE INJECTION	CHANNEL NUMBER/TAG NO			
DATA LOGGER PRI	NTOUT:			
(PRETEST/POST-T	EST).			
BISTABLE PERFOR	MANCE (PASS/FAIL):			
REMARKS/OBSERVA	TIONS:			
ANALOG OUTPUT	PRETEST	NOISE AF	PLIED	DC
NAME/TAG NO.	DC VALUE P-P NOIS	DC VALUE	P-P NOISE	MOEV
PZR VAP/T454A				
NR TEMP/T441L				
NR TEMP/T441K				
WR PRE/P408B				
TAPE SET:				
'NPE FOOTAGE: (PRE-TEST/TE	EST/POST-TEST)			
REMARKS/OBSERVA	ATIONS:			
PERFORMED BY/DA	ATE:			

Figure 6-10. Noise Test Data Sheet

6.2.2 Fault Test Setup Description

Eagle 21™ system performance, while subjected to the fault tests described in section 5.2, was monitored in the following manner:

- o Channels adjacent (left, right, top, bottom) to the channel under test were chosen for monitoring.
- Minimum physical separation between the channel under test and adjacent channels was provided. Cabinet configuration was altered to provide minimum physical separation for the digital contact output board tests.
- o The channel under test was continuously moditored immediately prior to the fault application, disconnected from the data acquisition system (DAS) during fault application, and reconnected to the DAS upon removal of the fault.

Following the test, all necessary repairs were recorded noting all component failures and channel operability was verified.

Figure 5-11 is the fault test data sheet.

6.2.3 Surge Withstand Capability (SWC) Test Setup Description

Eagle 21" system input/output performance, while subjected to the SWC tests described in section 5.3, was monitored in the following manner:

Analog outputs -- Four analog output channels were monitored continuously during the surge tests. The channels monitored replicated signals processed by current loop, wide range RTD, and narrow range RTD input signal conditioning boards. Thus, system analog input/output processing performance was measured.

I/O Module			Procedure Rev. Date Test #
TYPE			Management Annual Community of the Commu
SHORT CIRCUIT	, AC _	,	DC
COMMON MODE GRO	DUND CONNECTED	TO VOLTS PLUS	MINUS GROUND
LINE TO LINE	VOLTS (+)	TO (+)	_ (+) TO (-)
TEST INJECTION POINT		TEST CONDITION	***************************************
I/O CARD TYPE		POINT #	
PRE-TEST			
DATA LOGGER VERIFICATION*		PRINT OUTPUT #	
SYSTEM STATUS			
REMARKS AND TEST OBSERVAT	ON		
DISCONNECT DATA LOGGER			
TEST			
TAPE RECORDER FOOTAGE BEG SPE	N	END TIME: (STAF	SET # (STOP):
SYSTEM STATUS:			
REMARKS AND TEST OBSERVAT	ION		
POST-TEST			
DATA LOGGER DATA VERIFICA	TION* PRINT OU	TPUT #	
SYSTEM STATUS:			
REMARKS AND TEST OBSERVAT			
PERF	ORMED	REVIEWED	

Figure 6-11. Fault Test Data Sheet

o Digital outputs -- A single variable NR RTD (Thot3) was chosen to toggle all six Delta T/Tavg system trip outputs. All six trip output channels were toggled utilizing the variable RTD circuit shown in Figure 6-6. The control relay was cycled continuously during pre-test, test, and post-test runs [

T/Tavg system inputs were set just below and above the trip output toggle point (.2% or less). The Delta T/Tavg system utilizes current loop, NR RTD and O-10 volt analog input signals to generate partial trip output signals (see section 3 for system block diagrams). Thus, any significant degradation in system input signal processing would result in a trip output status failure. The control relay was not cycled during the partial trip module tests to ensure that the channel in test remained in one state (energized/deenergized) during the application of the surge.

Trip output status was monitored continuously during the noise tests using a strip chart recorder.

The following test methods were utilized to best measure system performance:

- o Input/output channels adjacent to the output channel under test were monitored.
- During application of the surge test wave, the strip chart recorder chart speed was increased to improve resolution.
- Analog putput channels replicating input channels under test were monitored.

Figure 6-12 is the Surge Test Data Sheet.

SURGE TEST DATA SHEET

		Procedure Rev.
YPE		TEST #
RANSVERSE MODE	on, invariance	
COMMON MODE		
TEST INJECTION POINT	I/O CARD TYPE	POINT #
PRE-TEST		
DATA LOGGER VERIFICATION	PRINT OUTPUT #	
SYSTEM STATUS:		
REMARKS AND TEST OBSERVATION		
DISCONNECT DATA LOGGER		
TEST		
TAPE RECORDER FOOTAGE BEGIN	END	SET #
SYSTEM STATUS:		
REMARKS AND TEST OBSERVATION	(\$:	
POST-TEST		
DATA LOGGER DATA VERIFICATION	ON* PRINT OUTPUT #	
SYSTEM STATUS:		AND RESIDENCE OF THE PROPERTY

Figure 6-12. Surge Test Data Sheet

6.2.4 Radio Frequency Interference Test Setup Description

Eagle 21™ system input/output performance, while subjected to RFI, was monitored in the following manner:

- o Analog outputs -- four analog output channels were monitored continuously during the RFI test. The channels monitored replicated signals processed by current loop, wide-range RTD, and narrow-range RTD input signal conditioning boards. Thus, system analog input/output processing performance was measured.
- o Digital outputs -- A single variable NR RTD (Thot3) was chosen to toggle all six Delta T/Tavg System trip outputs. All six trip output channels were toggled utilizing the variable RTD circuit shown in figure 6-6. The control relay was cycled at the start of each frequency run, measuring trip output performance during the RFI event. The Delta T/Tavg system inputs were set just below and above the trip output toggle point (.2% or less). The Delta T/Tavg system utilizes current loop, NR RTD and 0-10 volt analog inputs to generate partial trip output signals (see section 3 for system block diagrams). Thus, any significant degradation in system input signal processing would result in a trip output status failure. A normally open contact output channel was also monitored. The contact output was normally energized throughout the test.

In addition to continuous monitoring via the strip chart recorder, trip output status was also sampled by the control computer before, during, and after energization of the control relay. Any discrepancies between actual and expected trip output status were flagged by an error message. See figures 6-13 and 6-14 for RFI modulation and keying test data sheets. Figure 6-15 is the Tape Recorder Log Sheet.

RADIO FREQUENCY INTERFERENCE TEST DATA

TARGET: (CABINET POSITION) CALIBRATION FILE: FIELD STRENGTH LEVEL: (V/m)
TYPE OF ANTENNA: (LOG PERIODIC OR BICONICAL) ANTENNA POLARIZATION: (HORIZONTAL OR VERTICAL) DATE: TEST PERFORMED BY: REVIEWED BY: TAPE NAME: TAPE SET: TAPE RECORDER START AT: (FOOT) FREQUENCY: (MHZ) (DATE) (TIME) EVENT DIG/INPUT 00 0011 (EXPECTED TRIP OUTPUT PATTERN) 11 1100 00 0011 REMARKS: FREQUENCY: (MHZ) (DATE) (TIME) EVENT DIG/INPUT 00 0011 11 1100 00 0011 REMARKS: FREQUENCY: (MHZ) (DATE) (TIME) ERROR I'I THE CHANGING CONDITION OF BISTABLE STATUS (TRIP OUTPUT ERROR MESSAGE) EVENT DIG/INPUT 00 0011 11 1101 00 0011 REMARKS: ENDING TAPE RECORDER FOOTAGE FOR THIS SET OF DATA: (FOOT)

0720c:16-042888

Figure 6-13. RFI Modulation Test Data Sheet

RADIO FREQUENCY INTERFERENCE TEST DATA

TARGET: (CABINET POSITION) FIELD STRENGTH LEVEL: (V/M)
TYPE OF ANTENNA: (LOG PERIODIC OR BICONICAL)
ANTENNA POLARIZATION: (HORIZONTAL OR VERTICAL) DATE: TEST PERFORMED BY: REVIEWED BY: TAPE NAME: TAPE SET: TAPE RECORDER START AT: (FOOT) FREQUENCY: (MHZ) (DATE) (TIME) (FIRST KEY CYCLE)
DIG (K-OFF) INPUT
00 0011
11 1100 (SECOND KEY CYCLE) DIG [K-ON] INPUT 00 0011 11 1100 EVENT (EXPECTED TRIP OUTPUT PATTERN) REMARKS: FREQUENCY: (MHZ) (DATE) (TIME) DIG [K-OFF] INPUT 00 0011 11 1100 DIG [K-ON] INPUT 00 0011 11 1100 EVENT REMARKS: FREQUENCY: (MHZ) (DATE) (TIME) DIG [K-OFF] INPUT 00 0011 11 1100 DIG [K-ON] INPUT 00 0011 11 1100 EVENT .EMARKS:

Figure 6-14. RFI Keying Test Data Sheet

ENDING TAPE RECORDER FOOTAGE FOR THIS SET OF DATA: (FOOT)

006-A-19566-29 TAPE RECORDER:

TAPE RECORDER LOG SHEET

	RENARKS								
68 CORD [145]	START STOP 1775 MIN GROUP 112 3 4 5 6 7 8 9 00 10 21314								
	TAPE STA								
LUAN CURTITIONS	F1MP'S TEMP, PRESS TAPE IN PRESS TAPE					1010 1010 1010 1010 1010 1010 1010 101			
erak.	¥			П					
	SET DATE TIME								
and the same	<u> </u>							-	

SECTION 7 ACCEPTANCE CRITERIA

7.1 DESCRIPTION

The general acceptance criterion for the 1E safety-related system is that the system shall remain operational before, during, and after any one of the abnormal events described in Section 5 and listed below. Specific acceptance criteria for the noise, fault, surge withstand capability, and radio frequency interference tests are defined in the following paragraphs.

7.1.1 Noise Test Acceptance Criteria

The Eagle 21^{∞} system shall remain operational and maintain protective action before, during, and after any credible noise event described in section 5.1.

7.1.2 Fault Test Acceptance Criteria

The Eagle 21^{∞} system shall remain operational and maintain protective action before, during, and after the application of any credible faults as described in section 5.2. Faults shall not propagate across the class non-1E to class 1E isolation barrier or from channel to channel.

7.1.3 Surge Withstand Capability Test Acceptance Criteria

The Eagle 21° system shall remain operational and maintain protective action before, during, and after application of the surge withstand test wave to the designated class non-1E to class 1-E isolators as described in section 5.3. In addition, no component damage or shift in calibration exceeding the specified accuracy of the board under test shall occur due to the application of the surge withstand test wave to any cabinet input/output excluding the test panel and MMI communications connections.

7.1.4 Radio Frequency Interference Test Acceptance Criteria

The Eagle 21^m system shall remain operational (i.e., continuous microprocessor operation) while exposed to the radio frequency interference tests described in section 5.4.

SECTION 8 TEST RESULTS

The results of the system noise, fault, surge, and RFI tests are based on the acceptance criteria defined in Section 7. System performance during these abnormal events is described in the ensuing sections. The results are reported in tabular format at the end of this section.

8.1 NOISE TEST RESULTS

Tables 8-la through 8-lg report the results of the noise tests. Analog output noise in all cases was coupled wire-to-wire from the non-1E cabling to the 1E cabling or directly into the analog output channel. The noise did not affect analog input or digital output signal processing. Thus, protective action was maintained before, during, and after all credible noise events. In all cases the analog output signals returned to normal upon removal of the noise signal.

The test effects column of tables 8-1a through 8-1g reports the worst-case analog output signal shift for each test run.

A system performance summary is given below for each type of noise test:

	Worst Case Shift in	
Noise Test	Analog Output Signals	Results in Table
Random		7
Ac Chattering Relay		
Do Chattering Relay		
Mil-Spec Noise #1		
Mil-Spec Noise #2		
High Voltage Transien	t	
Static	Manager 1	b,c

The ac noise sources (ac chattering relay and Mil-spec noise #2) produced spiking on the analog output signal and an increase in the background noise level. There was no recorded shift in the nominal dc value. The random high-voltage transient and dc chattering relay noise sources produced a shift in nominal dc value and an increase in background noise level.

8.2 FAULT TEST RESULTS

Tables 8-2a and 8-2b report the results of the line-to-ground and the line-to-line fault tests. Class-1E isolation was maintained in all cases. Damage was limited to components located on the non-1E side of the isolator or the non-1E side of the isolator or the non-1E side of the isolation device. Analog output noise recorded was coupled wire-to-wire and was limited to a spike upon fault application in isolated instances. No effects were observed on the system input processing or trip/contact output processing subsystems. Thus, protective action was maintained before, during, and after fault application. Sections 8.2.1 and 8.2.2 summarize the test results of the final board designs (see section 3 for drawing references). Section 8.2.3 describes the board modifications required and tables 8-2a and 8-2b report the test results of the original board designs.

8.2.1 Line-to-Ground Fault

System Performance Summary:

Board Type	Fault Voltage	Effects on Adjacent Channels	Damage
Current Loop Output	125 Vac		
10-50 mA	125 Vdc		
	250 Vdc		
	580 Vac		
Digital Contact Output	125 Vac		
	125 Vdc		
	250 Vdc		
	580 Vac		_ b,c

Board Type	Fault Voltage	Effects on Adjacent Channels	Damage
Partial Trip Output	125 Vac	_	
	125 Vdc		
	250 Vdc		
	580 Vac		_ b.c

8.2.2 Line-to-Line pult

System Performance Summary:

Board Type	Fault Voltage	Effects on Adjacent Channels	Damage
Current Loop Output 10-50 mA	125 Vac	F	
	125 Vdc		
	250 Vdc		
	580 Vac		
Digital Contact Output	125 Vac		
	125 Vdc		
	250 Vdc		
	580 Vac		
			b,c

Soard Type	Fault Voltage	Effects on Adjacent Channels	Damage	
Partial Trip Output	125 Vac	Γ		
	125 Vdc			
	250 Vdc			
	580 Vac			
		_		b,c

MOV = Metal Oxide Varistor

SSR = Solid State Relay

8.2.3 Board Modifications Required

During fault testing of the original contact output and partial trip output board designs, failures in transient suppression devices (metal oxide varistors, MOV) caused component rupture and damage to adjacent channel circuitry. Since the fault test acceptance criteria (section 7) state that adjacent channels shall not be affected by faults applied to a non-1E channel, modifications were required. Applicable fault retests were performed following the board modifications. The modifications by board type are summarized below.

8.2.3.1 Partial Trip Output (EPT) Board

Design changes implemented to prevent MOV rupture are as follows. [

)b,c

For more information concerning the EFT modifications see Appendix A.

8.2.3.2 Digital Contact Output (ECO) Board

The original ECO board design utilized line-to-line MOVs [], b,c These MOVs failed and ruptured upon application of a 580 Vac line-to-line fault. Although there was no recorded degradation in adjacent channel performance, MOV material was sprayed on adjacent channel circuitry. Since the EPT board experienced adjacent channel failure due to MOV rupture, a design change was implemented to prevent MOV rupture. [

b,c

8.3 SURGE WITHSTAND CAPABILITY (SWC) TEST RESULTS

Table 8-3 reports the results of the SWC tests. No component failures occurred and there was no recorded changes in channel calibrations due to application of the SWC test wave. Protective action was maintained before, during, and after application of the SWC test wave to the designated class non-1E to class IE isolators. Analog output noise recorded was coupled through the associated input signal conditioning channel while the surge was applied. Noise was radiatively, and conductively, coupled into the input

channel. This conclusion is substantiated by the fact that noise was recorded on the channel under test as well as on adjacent channels. Trip output status failures were caused by noise coupled through the NR RTD input channels. Since the trip outputs are a function of the NR RTD inputs, erroneous trip outputs did occur. In no case was a false triggering of a partial trip occurred output hardware module recorded. In all cases these modules provided the appropriate outputs per loop calculation processor request. Thus, adverse system performance was limited to the analog I/O processing subsystem. In all cases, the analog I/O processing subsystem returned to normal operation upon removal of the SWC test wave. The loop processor subsystem maintained continuous operation before, during, and after all SWC test cases.

The test effect column of Table 8-3 reports the maximum recorded shift from nominal of an analog output signal for a specified test.

8.3.1 Common Mode Tests

System Performance Summary:

Type of 1/0 Board	Worst-Case Shift in Analog Output Signals	Component Damage, Calibration Shift
Wide-Range RTD Input		
Narrow-Range RTD Input		
WR RTD 0-10V Input		
Current Loop Input		
10-50 mA, Active		
Current Loop Input		
10-50 mA, Passive		
Current Loop Input		
4-20 mA, Active		
Current Loop Output		
10-50 mA		
	Secondo	→ b,c
1		1
		, b, c

Type of I/O Board (cont)	Worst Case Shift in Analog Output Signals	Component Damage, Calibration Shift
AC Input, Cabinet Power		
Partial Trip Output Digital Contact Output		Jb,c
A 3 2 Transporter Made To		

8.3.2 Transv_rse Mode Tests

System Parformance Summary:

Type of 1/0 Board	Worst Case Shift in Analog Output Signals	Component Damage, Calibration Shift
kide-Range RTD Inpu	t [7
Nrow-Range RTD in		
wn RTD 0-10V Input		
Current Loop Input		
10-50 mA, Active		
Current Loop Input		
10-50 mA, Passiv	e	
Current Loop Input		
4-20 mA, Active		
Current Loop Output		
10-50 mA		
Ac Input, Cabinet P	ower	
Partial Trip Output		
Digital Contact Out	put	J b, r
		- 511

8.3.3 Board Modifications/Retests

The digital contact output and partial trip output boards experienced failures during the fault tests. See section 8.2 for a report on the required board modifications. These modifications were made to the transient voltage suppression circuitry on these boards.

The contact output board was retested to verify compliance with IEEE-472-1974. Only transverse mode transient suppression across open contacts was affected by the the modifications. Retests S57 and S58 were performed following the modifications to verify board performance.

The partial trip output board common and transverse mode transient suppression circuitry was modified. An analysis was performed (appendix A) in lieu of retesting and supports the original SWC tests, S13-S16.

8.4 RADIO FREQUENCY (RF) INTERFERENCE TEST RESULTS

Tables 8-4a and 8-4b report the results of the RF modulation and keying tests. In general, unalog output noise recorded was coupled through the associated input signal conditioning channel. At isolated low frequencies (100 MHz or lass) some noise was coupled directly into the analog output channel. Trip utput status failures were caused by noise coupled through the NR RTD input channels. Since the trip outputs are a function of the NR RTD inputs, erroneous trip outputs did occur. In no case was a false triggering of a partial trip or contact output hardware module recorded. In all cases, these modules provided the appropriate outputs per loop calculation processor request. Thus, adverse system performance was limited to the analog I/O processing subsystem. In all cases the analog I/O processing subsystem returned to normal operation upon removal of the RF field. The loop processor subsystem maintained continuous operation before, during, and after all modulation and keying test cases.

The two noise coupling paths (input and output) produced different recorded noise characteristics. The noise coupled through the inputs was most severe at the start and end of each frequency test run. The noise consisted of a spike upon application of the RF field, followed by a period of reduced noise, and ending with a spike upon removal of the RF field. The keying test results summary reports the worst-case transient analog output signal shifts. Noise coupled directly into the analog output channel produced a shift in the nominal 60 value and an increase in the background noise level throughout the affected frequency test run.

An additional test was performed to confirm that the noise coupled through the input channel was radiatively coupled and not conductively coupled. The RF signal generator was used to inject an ac coupled RF signal directly into the NR RTD input board with a nominal dc voltage applied to the input. The man-machine interface terminal was monitored during the noise injection and no effect on the input signal was observed. [

10,0

The test effect column of Tables 8-4a and 8-45 reports the maximum recorded shift from nominal of an analog output signal over the frequency range specified and reports the frequencies at which trip output status failures occurred.

8.4.1 Modulation Tests

System Performance Summary:

Frequency Band	Worst-Case Shift in Analog Output Signals	
20 - 160 MHz 160 - 500 MHz 500 - 1000 MHz		J b.c

8.4.2 Keying Tests

System Performance Summary:

Frequency Band	Worst-Case Shift in Analog Output Signals	
	_	7
20 - 160 MHz 160 - 500 MHz		
500 - 1000 MHz		_ b.c
Ţ		l _{b,c}

8.4.3 Cabinet Modifications Required

Modifications were made to the Eagle $21^{\rm m}$ cabinet to improve system immunity to RF1. [

 $\rm J_{b,\,c}$ There modifications were made prior to the recording of final data shown in tables 8-4a and 8-4b.

TABLE 8-1a RANDOM NOISE TESTS (ANTENNA COUPLED)

Test	Tyr	pe of	Test	
Number		Board	Effect	
N1	Partial Trip (Output	Γ	1
N2	10-50 mA Curre	ent Loop Output		
N3	Digital Contac	ct Output		
	NO, OC			
N4	Digital Contac	t Output		
	NO, SE			
N5	Digital Contac	t Output		
	NC, OC			
N6	Digital Contac	t Output		
	NC, SC		L	J b,
AOS = Analog Ou	tpur Signal Shifts	OC = Open Circuit	NO = Normally Og	nen.
TOF = Trip Outp		SC = Short Circuit		

Test Number	Type of 1/0 Board	Test Effect
N7	Partial Trip Output, Ant Co.	ГТ
N8	Partial Trip Output, Dir Co.	
N9	10-50 mA Current Loop Output, Ant Co.	
N10	10-50 mA Current Loop Output, Dir Co.	
N11	Digital Contact Output, NO, OC, Ant Co.	
N12	Digital Contact Output, NO, SC, Ant Co.	
N13	Digital Contact Output, NO, Dir Co.	
N14	Digital Contact Output, NC, OC, Ant Co.	
N15	tal Contact Output, NC, SC, Ant Co.	
		b,c

TABLE 8-1c DC CROSSTALK NOISE TESTS - CHATTERING RELAYS

lest umber	Type of 1/0 Board	Test Effect
N16	Partial Trip Output, Ant Co.	[]
N17	Partial Trip Output, Dir Co.	
N18	10-50 mA Current Loop Output, Ant Co	
N19	10-50 mA Current Loop Output, Dir Co.	
N20	Digital Contact Output, NO, OC, Ant Co.	
N21	Digital Contact Output, NO, SC, Ant Co.	
N22	Digital Contact Output, NJ, Bir Co.	
N23	Digital Contact Outrut, NC, OC, Ant Co.	
N24	Digital Contact Output, NC, SC, Ant Co.	
		L

TABLE 8-1d MILITARY SPECIFICATION NOISE SOURCE #1 TESTS (ANTENNA COUPLED)

c Outs	out Signal Shifts OC = Open Circuit SC = Short Circuit	NO = Normally Open NC = Normally Closed
N30	Digital Contact Output, NC, SC	L J _{b,c}
N29	Digital Contact Output, NC, OC	
N28	Digital Contact Output, NO, SC	
N27	Digital Contact Output, NO, OC	
N26	10-50 mA Current Loop Output	
N25	Partial Trip Output	
Test umber	Type of 1/0 Board	Test Effect

	۹				,
	1				
			۰		
	3	۰		ø	,
	٠				ъ
	8		d		r

Test Yumber	Type of 1/0 Board	Test Effect
N37	Partial Trip Output	
N38	10-50 mA Current Loop Output	
N39	Digital Contact Output, NO, OC	
N40	Digital Contact Output, NO, SC	
N41	Digital Contact Output, NC, CC	
N42	Digital Contact Oulput, NC, SC	b,c
OS = Analog Out OF = Trip Outpu	tput Signal Shifts OC = Open Circuit SC = Short Circuit	NO = Normally Open NC = Normally Closed

TABLE 8-1g STATIC NOISE TESTS

Test Number	Type of 1/0 Board	Test Effect
N43	Partial Trip Output, Ant Co.	Γ 7
N44	Partiai Trip Output, Dir Co.	
N45	10-50 mA Current Loop Output, Ant Co.	
N46	10-50 mA Current Loop Output, Dir Co.	
K47	Digital Contact Output, NO, OC, Ant Co.	
N48	Digital Contact Output, NO, SC, Ant Co.	
N49	Digital Contact Output, NO, Dir Co.	
N50	Digital Contact Output, NC, OC, Ant Co.	
N51	Digital Contact Output, NC, SC, Ant Co.	b,c
OC = Open Circuit SC = Short Circuit	NO = Normally Open NC = Normally Closed	Ant Co. = Antenna Coupled Dir Co. = Direct Coupled

lest lo.	Voltage Level	Type of I/O Board	Test Connect Ions	Effects on Adjacent Channels	Damage
		Connect Love Output 10.50 -t	H to *	Γ	
F1	125 VAC	Current Loop Output, 10-50 mA	H to		
F2	125 VAC	Current Loop Output, 10 50 mA		1	
F3	125 VDC	Current Loop Output, 10-50 mA	* to *	1	
F-4	125 VDC	Current trop Output, 10-50 mA	* to -		
F5	125 V9C	Current Loop Output, 10-50 mA	- to *		
F6	125 VDC	Current Loop Output, 10-50 mA	* 10 *		
F7	250 VDC	Current Loop Output, 10-50 mA	+ 10	1	
FB	250 VDC	Current Loop Output, 10-50 mA	to *		
F9	250 VOC	Current Loop Output, 10-50 mA			
F10	250 VOC	Current Loop Output, 10-50 mA	10	1	
F11	580 VAC	Current Loop Output, 10-50 mA	H to *	1	
F 12	580 YAC	Current Loop Output, 10-50 mA	H to		
F 13	250 VDC	Digital Contact Dutput, EN	* to NO		
F 14	250 VDC	Digital Contact Output, EN	* to NC		
F 15	250 VƏC	Digital Contact Dutput, EN	to NO		
F 16	250 VDC	Digital Contact Output, EN	- to NC		
F17	580 VAC	Digital Contact Output, EN	H to NG		
F 18	580 VAC	Digital Contact Output, EN	H to NC		
F 19	125 VAC	Partial Trip Output, EN	H to to		
F20	125 VAC	Partial Trip Output, EN	H to HI		
F21	125 VDC	Partial Trip Output, EN	* to 10		
F22	125 VDC	Partial Trip Output, EN	- to 10		
F23	125 VDC	Partial Trip Cutput, EN	* to HI		
F24	125 VDC	Partial Trip Output, EN	to HI		
F25	250 VDC	Partial Trip Output, EN	- to HI		
F 26	250 VDC	Partial Trip Output, EN	* to HI		

TABLE 8-2a (Continued) LINE-GROUND FAULT TESTS

Test No.	Voltage Level	Type of 1/0 Board	Test Connect Ions	Effects on Adjacent Channels	Damage
*F 27	250 ° DC	Factial Trip Output, EN	* to 10		
*F28	250 VDC	Partial Trip Output, EN	- to £0		
F29	250 VDC	Partial frip Output, DEN	+ to HI		
F30	250 VDC	Partial Irip Output, EN	+ to HI		
F31	250 VDC	Partial Trip Output, EN	to HI		
F32	250 V0C	Partial Tri, Output, DEN	to HI		
F33	250 VDC	Partial Trip Output, EN	- to t0		
F34	250 VDC	Partial Trip Output, PEN	- to t0	The second secon	
F35	250 VDC	Partial Trip Output, EN	* to t0		
F36 F37	250 VDC 580 VAC	Partial Trip Output, DEN Partial Trip Output, EN	* to L0		
F38	580 VAC	Partial Trip Output, DEN	# to 10		
F 39	580 VAC	Partial Trip Output, EN	H to HI	The state of the s	
F40	580 VAC	Partial Trip Output, DEN	H to HI		
-	200			L_	

D.C

* - Tests of original partial trip output board design

EN * energized

NO - Mormally Open

DEN = Deenergized

NO - Normally Open NC - Normally Closed

TABLE 8-2b (continued)

Test No.	Voltage Level	Type of 1/0 Board	Test Connect tons	Effects on Adjacent Channels	Damage
F66	580 VAC	Digital Contact Output, EN	H to NC, N to C		
		Fartial Trip Output, EN	H to HI, N to LO		
F67	\$25 VAC	Partial Trip Output, EN	+ to ML, - to LD		
F68	125 VBC	Partial Trip Output, EN	* to LO to HI		
F69	125 VDC	Partial trip Output, A.	* to LO to HI		
F70	250 VBC	Partial Trip Output, DEN			
		The state of the s	* to HI to 10		
F71	250 VDC	Partial Irip Output, DEN	+ to 10, - to HI		
F72	250 VDC	Partial Trip Output, IN			
F73	250 VDC	Partial Trip Output, IN	* to HI, - to LO		
F74.	580 VAC	Partial Trip Output, DEN	H to H1, S to L0		
		Partial Trip Output, EN	H to HI, N to 10		
F75	580 VAC	ration to be company			
trculted					

_l b.c

** - Tests of original digital contact output Board Design

EN: energized DEN: Deenergized

* 1000

N() = Nr Agily Open NC = Nr Agily Closed

SURGE WITHSTANG CAPABILLITY (SWC) TESTS

S	Test	Test	Type of	Test	Test
TRANS	No.	Mode	:/O Board	Connect tons	Effect
S 2	5 1	CUM	Digital Contact Output, EN	NO/C	
\$ 3 COM		TRANS	Digital Contact Output, EN	NO/€	
TRANS		COM	Digital Contact Output, DEN	NO/C	1
S			Distral Contact Detput, DEN	NB/€	
S 6				NC/C	
S		FRANS	Digital Contact Output, FN	NC/C	1
S B		COM	Digital Contact Dutput, DEN		
COM		TRANS	Digital Contact Output, DEN		
Side		COM	Digital Contact Output, EN	NO/NC/C	
TRANS		COM	Digital Contact Output, DEN	NO/NC/C	
S12				NG/NC	
S13			Olgital Contact Output, DEN		
TRANS		COM	Partial Trip Output, EN		
S15		TRANS	Partial Trip Output, EN	H/N	
S16		COM	Partial Trip Outout, DEN	H/N	
S17 COM		TRANS	Partial 1: 1p Output, DEN	H/N	
STANS		COM	Current Loop Output, 10-50 mA	*/-	
COM			Current Loop Output, 10-50 mA	+2-	1
S20			Current Loop Output, 10-50 mA		
COM		TRANS	Current Loop Output, 10-50 mA		
S22 TRANS Wide Range RID Input 1*. 1-		COM			
S23		TRANS	Wide Range RIB Input	V*, V-	
S25 TRANS Wide Range RID Input V*. I*		TRANS	Wide Range RID Input		
S26		TRANS	Wide Range RID Input	V*. I-	
S27 TRANS Wide Range RID Input V 1*	525	TRANS	Wide Range RTD Input	V*. I*	
S27 TRANS Wide Range RID Input V I*	526	TRANS	Wide Range RTD Input		
S29		TRANS	Wide Range RID Input	V-, 1*	
S30	528	COM	Wide Range RID Input	V*, V-, I*, I~	
S30	529	TRANS	Wide Range RID Input		
\$31 COM Narrow Range RID Input		TRANS	Wide Range RID Input		1
532 TRANS Narrow Range RID Input I*, I- *534 COM Narrow Range RID Input V*, V-, I*, I-		C(IM	Narrow Range RID Input	V*. V I*. I-	
S34 COM Narrow Range RID Input V+, V-, I+, I-	532	TRANS	Narrow Range RIO Input	V, V-	
7334 108	533	TRANS	Narrow Range RTD Input	1+, 1-	
	*534	COM	Narrow Range RTD Input	V+, V-, I+, I-	

TABLE 8-3 (continued) SURGE WITHSTAND CAPABILITY (SWC) TESTS

Test No.	Test Mode	Type of 1/0 Board	Fest Connect tons	Test Effect
535	TRANS	Warrow Range RTD Input	V, V-	Γ -
*536	TRANS	Narrow Range RTD Input	14, 1-	
537	COM	Nacrow Range RTD Input	V*. V I+. I-	
538	TRANS	Narrow Range RID Input	V+, V-	1
539	TRANS	Narrow Range RTO Input	14, 1-	
540	COM	Narrow Range RTD Input	V, V-, 3*, 1-	
541	TRANS	Narrow Range RID Input	V, V-	
*542	TRANS	Narrow Range RIF Input	14, 1-	
**543	COM	Narrow Range K7D Input	V*, V-, 1*, 1-	
544	COM	WR RTD 0-10V Input	+/-	
545	TRANS	WR RID 0-10V Input	*/-	
546	COM	Current Loop Input, 10-50 mt, act	15*/11*	
547	COM	Current Loop Input, 10-50 mA, act	15*, 11*, 15, 11-	
548	TRANS	Current Loop Input, 10-50 mA, act	LS*, LS-	
549	TRANS	Current Loop Input, 10-50 mA, act	1.1+, 1.1-	
550	TRANS	Corrent Loop Input, 10-50 mA, act	15+, 11+	
551	COM	Current Loop Input, 10-50 mA, pass	(1*, 1.1-	
552	TRANS	Current Loop Input. 10-50 ma, pass	1.1*, 1.1-	
553	COM	Current Loop Input, 4-20 mA, act	11*, 11-	
554	TRANS	Current Loop Input, 4-20 mA, act	1.1+, 1.1-	
\$55	COM	AC Input, Cabinet Power	H/N	
556	TRANS	AC Input, Cabinet Power	H/N	
\$57	TRANS	Digital Contact Output, EN	NC/C	
·558	TRANS.	Digital Contact Output, DEN	NO/C	

^{* *} Tests performed at 60 HZ repetition rate

AOS: Analog Output Signal Shifts NG = Normally Open EN = Energized

TOF: Trip Output Failures

NC = Normally Closed DEN = Deenergized ES = Loop Supply act = Active L1 = Loop Input pass = Passive

^{** -} Test performed at 50 HZ repetition rate

^{+ -} Retests required due to addiffications made during fault testing

TABLE 8-4a
RADIO FREQUENCY MODULATION TEST RESULTS
(ALL RESULTS WITH CABINET BOORS CLOSES)

Test No.	Fleld Strength	Frequency Band(MHZ)	Antenna Type	Polar tzat ion	(Cabinet Side) Target	Test Effect
RF 1	3 V/m	20 - 160	BICONICAL	VERT	FRONT	
RF 2	3 V/m	20 - 160	BICUNICAL	HORZ	FRONT	
RF 3	3 V/m	160 - 500	LOG PERIGOIC	HORZ	FRONT	
RF 4	3 V/m 3 V/m	500 - 1000 160 - 500	LOG PERIODIC LOG PERIODIC	MEST VEST	FRENT FRONT	
RF 6 RF 7	3 V/m 3 V/m	500 - 1000 20 - 160	LOG PERIODIC BICONICAL	VERT HERZ	FRONT RIGHT	
RF 8	3 V/m	160 - 500	LOG PERIODIC	VERT	RIGHT	

AOS - Analog Output Signal Shifts FOF - Trip Output Failures

RADIO FREQUENCY MODULATION 165T RESULTS (ALL RESULTS WITH CABINET DOORS CLOSED)

	_												
Test Effect													
(Cabinet 5100) Target	RIGHT	1667	LEFT	1133	PEAR	RE AR	SEAR	RE AR	PEAR	REAR	FRENT	FRONT	FROME
Polar tzat lon	VERI	WERT	18882	14/38/2	23694	VERT	YERT	HORZ	VERT	2.00,000	Z8(34)	2804	14JR.Z
Antenna Type	LOG PERIODIC	BICONICAL	LOG PERTODIC	LOG PERIODIC	LOG PERIODIC	1.0G PERIODIC	LOG PER1001C	LOG PERIODIC	BICONICAL	BICONICAL	BICONICAL	LOG PERIODIC	LOG PERHODIC
Frequency Band(MHZ)	500 - 1000	20 - 160	500 - 1000	160 - 500	500 - 1000	160 - 500	1.	160 - 500	20 - 160	20 - 160	20 - 160	200 - 1000	160 ~ 500
Strength	3 V/m	(7)	M	(%)	3 V/m	3 V/m		3 V/m		3 V/m	10 V/m	10 V/m	10 V/m
No.	RF 9				RF 13	RF 14		RF 16		RF 16	RF 19	RF 20	RF 21

Tust Effect						
(Cabinet Side) Target	FROME	FRONT	7 RONT	RIGHT	RIGHT	
Potar traffon	VERT	VERI	VERT	14.19.2	VERT	
Antenna Type	1.06 PERIODIC	LOG PURIODIC	BICGNICAL	BECONICAL	106 PERIODIC	
rest Field Frequency Band(MHZ) Antenna Type	0001 - 305	160 - 500	20 - 160	20 - 160	160 - 500	
Field	RF 22 10 V/m	RF 23 10 V/m	10 V/m	RF 25 10 V/m	10 V/m	
rest	RF 22	BF 23	RF 24	RF 25	RF 26	

J 0,c

TABLE 8-4a (Continued)
RADIO FREQUENCY MODULATION TEST RESULTS
(ALL RESULTS WITH CABINET DOORS CLOSED)

Test No.	Fleld Strength	Frequency Band(MHZ)	Antenna Type	Polarization	(Cabinet Side) Target	lest Effect
RF 27	10 V/m	500 - 1000	LOG PERIODIC	VERT	RIGHT	
RF 28	10 V/m	20 - 160	BICONICAL	VERT	LEFT	
RF 29	10 V/m	160 - 500	LOG PERIODIC	HORZ	LEFT	
RF 30	10 V/m	500 - 1000	LOG PERIODIC	HORZ	LEFT	
RF 31	10 V/m	20 - 160	BICONICAL	HORZ	REAR	
RF 32	10 V/m	20 - 160	BICONICAL	VERT	REAR	

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(finned)	ON TEST	I DOMBRS
(Cons	ATI	HIN
-43	MEDIDIGI	H CAR
8 311	NC.V	1417
TAB	REVER	SBC #5
	H 63	RE
	RABE	ALL

Test Effect				
(Cabinet Side) Target	7 N 10	RE AR	RE AR	
(Cabinet 5 Antenna Type Potarization Target	140812	VERT	140812	
Antenna Type	1.06 PER1001C	LOG PERTOBIC LOG PERTODIC	106 PER1001C	
Test Field Frequency Band(#4Z)	RF 33 10 V/m 500 - 1000	500 - 1000	160 - 500	
Field Strength	10 V/m	RF 34 10 V/m RF 35 10 V/m	RF 36 10 V/m	
Test No.	RF 33	RF 34	RF 36	

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RADIO FREQUENCY MEVING TEST RESULTS (ALL RESULTS WITH CABINET DOORS CLOSED)

Test Effect								
(Cabinet Side) Target	FROME	FROMI	FROM	FRONT	FRONT FRONT FRONT	FRONT	FRUNT	FRONT
Polar tzat ton	1408.2	HORZ	HORZ	280H	HORZ VERT VERT	VERT	VERT	VERT
Antenna Type	BICONICAL	LOG PERIODIC	UNG PERIODIC	BICONICAL	LOG PERIODIC BICONICAL LOG PERIODIC	LOG PERIODIC	BICONICAL	1.06 PERTODIC
Frequency Band(MCZ)	20 - 160	160 - 500	160 - 500	20 - 160	500 - 1000 20 - 160 160 - 500	160 - 500	20 - 160	200 - 1000
Strength	3 V/m	3 V/m	10 V/m	10 V/m	3 V/m 3 V/m 3 V/m	10 V/m	10 V/m	10 V/m
Test No.	RF 37	RF 38	RF 39	RF 40	RF 41 RF 42 RF 43	RF 44	RF #S	RF 46

AOS - Analog Butput Signal Shifts TOF - Irip Output Fallure

D, C

SECTION 9

The Eagle 21TM system performance satisfied the acceptance criteria stated in section 7. The microprocessor subsystem maintained continuous operation while subjected to the abnormal events described in section 5.

Analog output signal noise coupled wire-to-wire or through the analog output channel has no effect on the protective action of the plant protection system since the Eagle 21* does not use analog output signals for protection signal transmission. Analog output signals are used as interfaces to the plant control and monitoring equipment (e.g., computer, post-accident monitoring system (PAMS)).

9.1 NOISE TESTS

The protective action of the Eagle 21° system was not affected by noise injected into or adjacent to class non-1E wiring. Analog output signal noise recorded was coupled wire-to-wire or through the analog output channel. Possible analog output noise effects on plant class non-1E systems and PAMS are summarized as follows:

- o The AC noise sources (AC chattering relay, Mil-Spec noise source #1) generated noise spikes on the analog output signal. No change in the nominal DC value of the analog output signal was recorded. These noise spikes will not affect slow responding monitoring equipment.
- The DC and high voltage transient noise sources produced a shift in the nominal DC value of the analog output signal of 0.5% or less. Since the accuracy requirements of the plant monitoring systems are large compared to the observed effects, these effects are considered minimal.

9.2 FAULT TESTS

The protective action of the Eagle 21* system was not affected by the injection of credible faults into the designated class non-1E to class 1E isolators. Analog output signal noise recorded was coupled wire to wire and consisted of a noise spike of 0.88% or less upon fault application. No change in the nominal DC value of the analog output signal was recorded. These noise spikes will not affect monitoring equipment.

9.3 SURGE WITHSTAND CAPABILITY (SWC) TESTS

The protective action of the Eagle 21° system was not affected by the application of the surge withstand test wave to the designated class non-18 to class-18 isolators. In addition, no component damage occurred and no changes in channel calibrations were recorded due to the application of the surge withstand test wave to any cabinet input/output under test.

9.4 RADIO FREQUENCY INTERFERENCE TESTS

The Eagle 21^∞ system remained operational while exposed to radio frequency interference (RFI). Analog input/output processing and protective action functions were affected but delistrated full recovery upon removal of the RFI. To avoid protection system perturbations, Westinghouse recommends that the Eagle 21^∞ system equipment room(s) be "zoned" to prohibit the use of transceivers in the 20-700 MHz band.

APPENDIX A PARTIAL TRIP OUTPUT BOARD SURGE WITHSTAND CAPABILITY ANALYSIS

Performed by: R. Nero, Westinghouse

During the fault testing portion of the qualification test for EAGLE-21%, it was necessary to modify the output circuitry of the EPT 1/0 board. Since the modification did not affect the portion of circuitry that was designed to handle high frequency oscillatory surges. The SWC tests (IEEE-472-1974) were not rerun on the EPT 1/0 board.

The modification involved suppresser devices on the output. [______]

To substantiate the decision not to rerun the SWC tests (IEEE-472-1974) on the EPT 1/O board, analysis was performed with a circuit analysis program [$$\rm J_{\rm b,c}$$. The analysis confirms that the passive surge network attenuates the surge well below the requirements. The analysis was run worst case for both the common mode and differential mode surge conditions. Worst case for both modes is that no MOVs are installed, all outputs are deenergized, and the outputs are not loaded.

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Figure A-1. EPT Common Mode Equivalent Circuit

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Figure A-3. FPI Differential Mode Equivalent Circuit

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- B.1 Signal Conditioning Boards
- B.1.1 Eagle Analog Input (EAI) Signal Conditioning Board
- B.1.1.1 Functional Description

The EAI board is classified as 1E protection-grade equipment, but since it receives inputs from protection-grade transmitters and supplies outputs to the protection-grade loop processor subsystem, it is not a class 1E isolation barrier.

- B.1.1.2 Performance Specifications
- B.1.1.2.1 Analog Input Characteristics --

b,c

B.1.1.2.2 Loop Supply Characteristics --

b. (

B.1.1.2.3 Power Supply Requirements --

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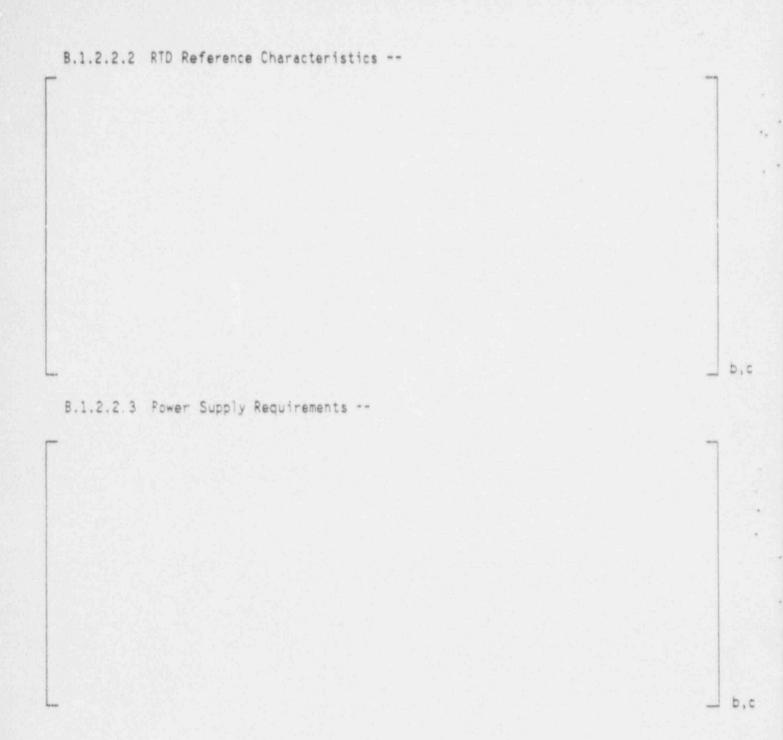
B.1.2 Eagle RTD Input (ERI) Signal Conditioning Board

R.1.2.1 Functional Description

The ERI boards are classified as 1E protection-grade equipment, but since they receive inputs from protection-grade RTDs and supply outputs to the protection-grade loop processor subsystem, they are not class 1E isolation barriers.

- B.1.2.2 Performance Specifications
- B.1.2.2.1 Analog Input Characteristics --

D, C



B.1.3 Eagle Partial Trip (EPT) Signal Conditioning Board

B.1.3.1 Functional Description

[The four EPT channels are fail-safe in that the failure of the loop processor subsystem causes the channels to trip after a brief time-out period.] In most applications, the EPT receives input signals from the class 1E LPS and sends output signals to the class 1E voting logic systems (SSPS or relay logic). In these applications it is not a class 1E isolation barrier. However the EPT has been classified as a class 1E isolation barrier for possible future applications.

B.1.3.2 Performance Specifications B.1.3.2.1 Digital Output Characteristics --_ b,c B.1.3.2.2 Power Supply Requirements --

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B.1.4 Eagle Contact Output (ECO) Signal Conditioning Board

B.1.4.1 Functional Description

2. Provides class 1E isolation between the protection cabinet and the control systems that receive the contact signals

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B.1.4.2 Performance Specifications

B.1.4.2.1 Contact Output Characteristics --

B.1.4.2.2 Power Supply Requirements --

_ b,c

B.1.5 Eag1	e Analog	Output (8	(AO) Signal	Conditioning	Board
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B.1.5.1 Functional Description

2. Provides class IE isolation for current loop signals sent to field receivers such as control board indicators and process control loops

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B.1.5.2 Performance Specifications

B.1.5.2.1 Analog Output Characteristics --

B.1.5.2.2 Power Supply Requirements --

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_ b,c

- B.2 Microprocessor Boards
- B.2.1 Digital Filter Processor (DFP) Board
- B.2.1.1 Functional Description

b.0

B.2.1.2 Performance Specifications

B.2.1.2.1 Power Supply Requirements --

b.c

B.2.2 Analog to Digital Converter (ADC) Board

B.2.2. T Functional Description

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B.2.2.2 Performance Specifications

B.2.2.2.1 Compatibility --

B.2.2.2. Power Supply Requirement --

_b,c

- B.2.3 Loop Calculation Processor (LCP) Board
- B.2.3.1 Functional Description

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- B.2.3.2 Performance Specifications
- B.2.3.2.1 Power Supply Requirements --

_ b,c

- B.2.4 Loop Processor Subsystem Digital Input/Output (LPSDIO) Board
- B.2.4.1 Functional Description

0720c 1b-061688

B.2.4.2 Performance Specifications B.2.4.2.1 Power Supply Requirements --B.2.5 Digital-to-Analog Converter (DAC) Board B.2.5.1 Functional Description

0720c 15-061688

B.2.5.2 Performance Specifications

B.2.5.2.1 Electrical Specifications --

__b,c

b,c

B.2.5.2.2 Power Supply Requirements

__b,c

- B.2.6 Loop Processor Subsystem Data Link Handler (DLH) Board
- B.2.6.1 Functional Description

07200 16-061660

B.2.6.2 Performance Specification

B.2.6.2.1 Power Supply Requirement (as shipped) --

_b,c

- B.2.7 Tester Subsystem Data Link Handler (DLH) Board
- B.2.7.1 Functional Description

9220: 10-061666

B.2.7.2 Performance Specification

B.2.7.2.1 Power Supply Requirement (as shipped) --

J b.c

B.2.8 Test Sequence Processor (TSP) Board

B.2.8.1 Functional Description

0720c:16-061668

B.2.8.2 Performance Specifications

B.2.8.2.1 Power Supply Requirements --

.... b,c

0720s:16-061668

B.2.9 High Precision Digital-to-Analog Converter (HPDAC) Board

B.2.9.1 Functional Description

8.2.9.2 Performance Specifications

B.2.9.2.1 Electrical Specifications --

07204 16-061888

__ b,c

_ b,c

8.2.9.2.2 Power Supply Requirements

_ b,c

B.2.10 Test Subsystem Digital Input/Output (TSDIO) Board

B.2.10.1 Functional Description

C

B.2.10.2 Performance Specifications

B.2.10.2.1 Power Supply Requirements --

_ b,c

APPENDIX C TEST PROCEDURES

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- o Adjust the high adjust potentiometer so that channel TE-441A3 reads 618.261+/-.375 Deg f on the MMI.
- Verify that the TAVG MM1 reading equals 589.740 + .2 Deg f.
 Verify the following actual bistable output status:

TS/441C - Not Tripped

TS/4416 - Not Tripped

TS/441D - Not Tripped

TS/441H - Not Tripped

TS/442D - Tripped

TS/442G * Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Close the manual switch input to the variable RTD board.
- o Adjust the low adjust potentiometer so that channel TE-441A3 reads 615.501+/-.375 Deg f on the MMI.
- o Verify that the Delta T MMI reading equals 104.237-.3PU.
 Verify the following actual bistable output status:

TS/1441C - Tripped

TS/14416 - Tripped

TS/1441D - Tripped

TS/1441H = Tripped

TS/1442D - Not Tripped

TS/1442G - Not Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Open the manual switch input to the variable RTD board and record the results. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.
- 2.2.3 Set the function generator output to the variable RTD board (see figure B-3) in the positive square wave pulse mode with a 0-5 volt amplitude at .O5HZ and a duty cycle of approximately 10%.
- 2.2.4 Close the recorder start switch and verify that the trip output signals switch upon receipt of the function generator switch signal (positive square wave pulse).

3.0 NOISE TEST PROCEDURE SEQUENCE

The noise test sequence described below will be followed for each noise test type specified in fections 4.0 through 8.0.

3.1 Pretest

Obtain a data logger printout of "normal" analog input/output and digital output values.

- 3.2 Disconnect data log and verify "antenna" connections and configuration for each injection point per Attachment A.
- 3.3 Connect the noise source and verify the readiness of the data acquisition system. Enter identifying records in tape recorder log and noise test data sheet (figure 1-6). Follow the test specific instructions given in Sections 4 through 8.
- 3.4 Disconnect the data logger, close the recorder start switch, start the tape recorder and record 2 minutes of pretest data. Simultaneously energize the noise sources and close the event marker switch. Record 2 minutes of data with the noise source applied. Observe the strip chart recorder and record and analog output signal deviations

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1.0 INTRODUCTION

This procedure details the electrical interference "noise" tests to be applied to the Engle-21 protection system.

These tests will consist of applying the following noise sources to the antenna/non-class 1E wiring and measuring the effects on system input/output processing.

- o Randum Noise
- o Crosstalk Noise
- o Mil N19900 Noise
- o High Voltage Transient Noise
- o Static Noise

The test configuration is documented in Attachment B.

2.0 PREPARATION FOR TEST

- 2.1 Connect the field cabling to sensor simulation, load simulation, and contact output loads per Attachments B, C and table 1-1.
- 2.2 Obtain system baseline data:
 - 2.2.1 System baseline data will be taken to verify system operation. Input voltage and current and resistance values corresponding to 0 100% of scale in 25% increments and record. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.
 - 2.2.2 Set signal inputs per table 1-1. Adjust analog input signals, using the MMI to obtain the expected engineering unit values specified in table 1-1. Using figure 8-6 as a reference, adjust the variable RTD channel per the following procedure:
 - Open the manual switch input to the variable RTD board.

- o Adjust the high adjust potentiometer so that channel TE-441A3 reads 618.261+/-.375 Deg f on the MMI.
- Varify that the TAVG MMI reading equals 589.740 + .2 Deg f.
 Verify the following actual bistable output status:

TS/441C - Not Tripped

TS/441G = Not Tripped

TS/441D - Not Tripped

TS/441H - Not Tripped

TS/442D - Tripped

TS/442G + Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Close the manual switch input to the variable RTD board.
- o Adjust the low adjust potentiometer so that channel TE-441A3 reads 615.501+/-.375 Deg f on the MMI.
- Verify that the Delta T MMI reading equals 104.237-.3PU.
 Verify the following actual bistable output status:

TS/1441C - Tripped

TS/14416 - Tripped

TS/1441D = Tripped

TS/1441H - Tripped

TS/1442D - Not Tripped

TS/1442G = Not Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Open the manual switch input to the variable RTD board and record the results. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.
- 2.2.3 Set the function generator output to the variable RTD board (see figure B-3) in the positive square wave pulse mode with a 0-5 volt amplitude at .OSHZ and a duty cycle of approximately 10%.
- 2.2.4 Close the recorder start switch and verify that the trip output signals switch upon receipt of the function generator switch signal (positive square wave pulse).

3.0 NOISE TEST PROCEDURE SEQUENCE

The noise test sequence described below will be followed for each noise test type specified in Sections 4.0 through 8.0.

3.1 Pretest

Obtain a data logger printout of "normal" analog input/output and digital output values.

- 3.2 Disconnect data logger and verify "antenna" connections and configuration for each injection point per Attachment A.
- 3.3 Connect the noise source and verify the readiness of the data acquisition system. Enter identifying records in tape recording and noise test data sheet (figure 1-6). Follow the test specific instructions given in Sections 4 through 8.
- 3.4 Disconnect the data logger, close the recorder start switch, start the tape recorder and record 2 minutes of pretest data. Simultaneously energize the noise sources and close the event marker switch. Record 2 minutes of data with the noise source applied. Observe the strip chart recorder and record and analog output signal deviations

and/or trip output status failures. A trip output status failure is defined as a failure of a trip output signal to switch upon receipt of the switch signal from the test station. Remove the noise source und open the event marker switch. Record 2 minutes of post test data and open the recorder start switch and stop the tape recorder.

- 3.1 Obtain a data logger printout and confirm system recovery by comparing to pretest data. Record any discrepancies.
- 3.6 With the system confirmed to be in the pretest condition, proceed to the next test.

4.0 RANDOM NUISE TEST

- 4.1 Connect the []_{b,c} random noise generator to the ENI 240L power amplifier as shown in figure 1-1. Connect the center conductor of the power amplifier to one conductor of the antenna. Terminate the cubinet end of the antenna to an unused internal block connection.
- 4.2 Follow the instructions given for antenna coupled tests given in Table A-2u. Follow the test sequence described in Section 3 for each channel designated in Table A-2a.

5.0 CROSSTALK NOISE TEST

- 5.1 Connect the 125 wolt DC chattering relay to the antenna assembly as shown in figure A-2a. Short the cabinet end of the antenna across an unused terminal block connection. Terminate and load the non-1E test cable as specified in Table A-2a.
- 5.2 Follow the test sequence described in Section 3 for each channel designated in Table A-2a.
- 5.3 Repeat 5.1 and 5.2 above using a 118V AC chattering relay. (figure 1-2b)

- 5.4 Disconnect the cabinet end of the antenna and terminate across the first set of terminals shown in Table A-2b. Disconnect the isolator wiring and short the wires specified in Table A-2b.
- 5.5 Follow the test asquence described in Section 3 for each channel designated in table A-2b.
- 5.6 Repeat 5.4 and 5.5 above using a 125 volt DC chattering relay. (figure 1-2b)

6.0 MIL N19900 NO/SE TEST

- 6.1 Connect "noise source 1" to the antenna assembly as shown in figure 1-3. Short the cabinet end of the antenna across an unused terminal block connection. Terminate and load the non-1E test cable as specified in Table A-2a.
- 6.2 Follo ne test sequence described in Section 3 for each channel designed in Table A-2a.
- 6.3 Repeat 6.1 and 6.2 above using "noise source 2." (see figure 1-3)

7.0 SURGE TRANSIENT GENERATOR

- 7.1 Connect the [1 b,c surge generator and [] b,c isolation network as shown in figure 1-4. Terminate the cabinet end of the antenna across 150 ohms. Terminate and load the non-1E test cable as specified in Table A-2a.
- 7.2 Follow the test sequence described in Section 3 for each channel designated in Table A-2a.

8.0 STATIC NOISE TEST

- 8.1 Connect the 580 VAC static noise sour eleo the antenna assembly as shown in figure 1-5. Terminate the cubinet end of the antenna across two separate (open circuit) unused terminal block connections. Terminate and load the non-1E test cable as specified in Table A-2a.
- 8.2 Follow the test sequence described in Section for each channel designated in Table A-2a.
- 8.3 Disconnect the cabinet end of the antenn and terminate across the first set of terminals shown in table A-2b. Disconnect the isolator wiring at the termination frame and per circuit the wires as specified in table Λ -2b.
- 8.4 Follow the test sequence described i Section 3 for each channel designated in table A-2b.

(See figure 5-3 of WCAP test report)

Figure 1-1 Random Noise Test Connections

(See figure 5-4a of WCAP test report)

Figure 1-2a Crosstalk Noise - Chattering dc Relay Test Connections

(See figure 5-4b of WCAP test report)

Figure 1-2b Crosstalk Noise - Chattering ac Relay Test Connections

(See figure 5-5 of WCAP test report)

Figure 1-3 Military Specification Noise Sources

(See figure 5-6 of WCAP test report)

Figure 1-4 High Voltage Transient Noise Test Connections

(See figure 5-7 of WCAP test report)

Figure 1-5 Transformer Connection for the 580 Vac Static Noise Source

9.0 ACCEPTANCE CRITERIA

9.1 Description

The acceptance criteria for the Eagle 21 (IE Safety Related System) is that the system shall maintain protective actions before, during and after the injection of credible noise into or adjacent to the class non-IE wiring.

TABLE 1-1 SIMPLATED INTUT SIGNAL

	Osemei Jene	Tag of	Yerzinsi Eleck	z	Terminel Commention Lo	8	1/0 Board Location	ä	1/0 Meand Commention Lo		Simistor Signal	Expected Signal in E.S.
**	Soutree Flam Lower fon	FT-441A	13-0		en		137.4				3.00	18.00 ± .003
**	Seutres Flux Syper Ion	第至-44-2第	13-0	**			111-4	**			4.84 well.	28.82 ± .08.82
'n	Pressurisor Pressure	FE/4380	#-CI				137-8	11	11	*	38,73 Ht	2235 ± 1.96
·	Celd Lag Tomperature	11 -44 IB	13-8	3,2	2	**	131-4	6,3	7,8	**	425.856 obse	362.70 ± .375
ń	Cold Lag Tomperebers	TE-4408	13-8	17.8	10.0	12.2	137-6	8.11	6,12	n	425.886 obse	542.70 ± .375
	Sot Leg Temperature	TE-441A1	13-4	1,2	6,3	m	137-3	0,3	2,4	*	447.392 obse	816.041 ± .375
	Ant Leg Tomperstars	TE-441A2	10-4	3.8	10,0	12	137-3	8,12	8,12	*	447.352 obms	816.041 + .375
	Not Lag Tampereture	17-44143	13-0		11,10	12	137-5	20,17	21,18	113	27 oless	H +1
	Steem Consentor Level Loop 2	11-361	2-61	**	M		131-2		п	#	雑れ	25 ± .1361
9	Steem Generator Level Long 3	11-303	3-61	*	n		131-2	20	13	g	2 2	75 ± .1281
mi.	MCS Mide Eamge Freesure	FT-408	*-01	18	н		131-6	320	*	12	11 Rs	1300 ± 3.78
12	Pricection Toper Temp	18-434	0-11	#4	67	**	137-4	20,17	21,18	13	400 OBS	488.288 ± 3.05
13	Secidest Sest Sement. Pump Stocharge Temp.	78-613	9-0		11,10	12	137-4	22, 25	23,26	n	300 086	280.406 ± 1.05

XX - Tarisble MID impot, set needsally at 447 175 obse (813 902 Deg I) for the low realstance reading and 448 184 obser (818 20) Deg I) for the bigh resistance reading. See step 2.3.2 for details.

EAGLE-21 NOISE TEST REPORT

TEST TYPE/PROCES		EV)			_
NOISE INJECTION		ER/TAG NO			
DATA LOGGER PRIM					
(PRETEST/POST-TE		ORNO SERVICE			
BISTABLE PERFORM	NANCE (PASS/F	AIL):	-		
REMARKS/OBSERVAT	IONS:				
ANALOG OUTPUT					
NAME/TAG NO.	DC VALUE	P-P NOISE	DC VALUE	P-P NOISE	%DEV
PZR VAP/T454A					
NR TEMP/T441L					
NR TEMP/T441K					
MR PRE/P408B					
TAPE SET:					
TAPE FOOTAGE:					
(PRETEST/TEST/PO	ST-TEST)				
REMARKS/OBSERVAT	IONS:				
PERFORMED BY/DAT	E:				

Figure 1-6. Noise Test Data Sheet

ATTACHMENT A NOISE INJECTION "ANTENNA" CONNECTIONS

NOTE: The antenna for noise injection is to be a 40 foot length of unshielded, non-twisted two conductor cable bundled to the non-class 1E test cable. The class non-1E test cable shall consist of a non-shielded twisted pair cable. The antenna and class non-1E cabling is separated from the class-1E cabling outside the protection cabinet. The antenna, class-1E and class non-1E cabling are all bundled together inside the protection cabinet. See figures 8-1 and 8-2 for antenna placement.

This attachment contains the following tables:

- Table A-la Noise Injection Field Connections (Antenna Coupled)
- Table A-1b Noise Injection Field Connections (Direct Coupled)

C+20

TABLE A-1a

MOISE INJECTION FIELD CONNECTION (Antenna Coupled)

			CONNECT NO	N-1E 1	TEST C	ABLE T	0			COMMECT
Channel	I/O Description	Channel Tag #	Terminal Block		rminal nnecti Lo		Isolator Type		I/O Board Location/ Channel #	CONNECT LOAD TO NON-IE TEST CABLE
1.	Bistable Partial Trip	1TS/442G	13-M	1	2		Class non Is lation Barrier	1E/1E	13T-10/1	40 Watt Light Bulb
2.	Analog Output	IPY/408A	13-N	4	5	6	Class son Isolation Barrier	1E/1E	13T-16/2	600 OHMS
3.	Contact Output (No)	ITY/441A	13-M	7	8		Class non Isolation Barrier	1E/1E	13T-12/2	Open Circuit
4.	Contact Output (NC)	ITY/441A	13-M*	7	8		Class non Isolation Barrier	1E/1E	13T-12/2	Open Circuit
5.	Contact Output (Mo)	TY/441A	13-M	7	8		Class non Isolation Barrier	1E/1E	13T-12/2	Short Circuit
6.	Contact Output (Nc)	TY/441A	13-M*	7	8		Class non Isolation Barrier	1E/1E	13T-12/2	Short

^{*}Move wire terminated on 13T-12-6 to 13T-12-7 to test NC configuration.

C

TABLE A-1b
NOISE INJECTION FIELD CONNECTION (Direct Coupled)

Channel	I/O Description	Channel Tag #	Terminal Block	Connect Artenna to HI Lo	Isolator Type	1/0 Board Location/ Channel #	DISCONNECT WIRES AT TERMINATION FRAME
1.	Bistable Partial Trip	ITS/442G	13-M	1 2	Class non IE/IE Isolation Barrier	13T-10/1	2, 3
2.	Analog Output	IPY/408A	13-N	4 5	Class non 1E/1E Isolation Barrier	137-16/2	5, 7
3.	Contact Output	ITY/441A	13-M	7 8	Class non 1E/1E Isolation Barrier	13T-12/2	5, 6

ATTACHMENT B FIELD CONNETTIONS AND SIMULATION

This attachment contains the following figures:

0	Figure	B-1	Noine Test Setup (Antenna Coupled)
0	Figure	B-2	Noise Test Setup (Direct Coupled)
0	Figure	B-3	Strip Chart Recorder/Function Generator Connections
٥	Figure	B-4	4-50 mA Transmitter
0	Figure	B-5	Wide Range Resistance Temperature Detector
0	Figure	B-6	Marrow Range Resistance Temperature Detector
0	Figure	P-7	10-50 mA Current Loop Output Monitoring
¢	Figure	B-8	Contact Output Monitoring Connection
0	Figure	B-9	Partial Trip Output Monitoring

Cabinet Configuration Information:

The cabinet under test, Qualification Unit 2, is an exact replica of Watts Bar Nuclear Power Station Protection Rack 13. The following drawings document the cabinet configuration. Copies of these drawings will be included as part of the final test report.

Drawing Description	Drawing Number/Rev.
Terminal Block Wiring Diagram, Protection Set 4	1-47043 PW-13, rev. 3E
Process Control Block Diagram, Delta T/T _{AVG} System	1080408 sh. 10, rev. 11
Process Control Block Diagram, W.R. S.G. Level	108D408 sh. 34, rev. 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temp.	108D408 sh. 38, rev. 4

Process Control Block Diagram, 108D408 sh. 39, rev. 5 RHR Pump Discharge Temp

Process Control Block Diagram, 108D408 sh. 43, rev. 1 RCS Wide Range Pressure

Eagle-21 Schematic Diagrams, Rack 13 Protection Set 4

1856E69 sh. 2, rev. 2

(See figure 5-1 of WCAP test report)

Figure B-1 Noise Te - Setup (Antenna Coupled)

(See figure 5-2 of WCAP test report)

Figure B-2 Noise Test Setup (Direct Coupled)

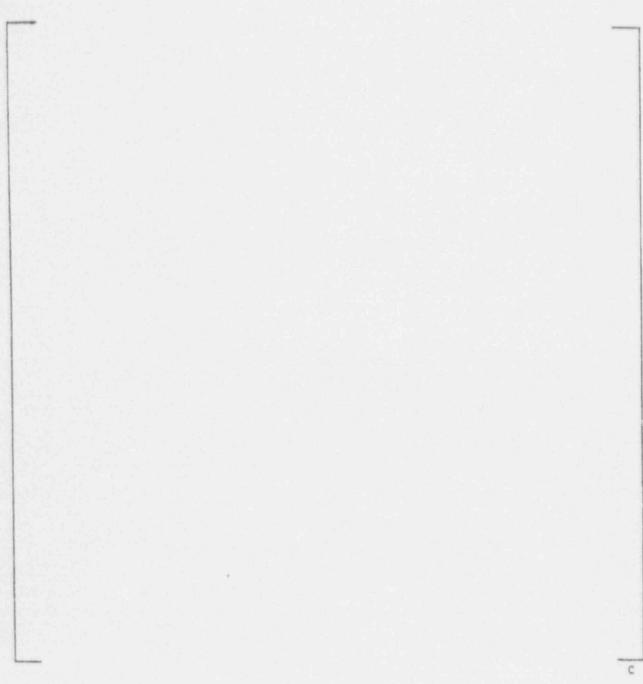


Figure B-3 Strip Chart Recorder/Function Generator Connections

(See figure 6-4 of WCAP test report)

Figure B-4 4-50 mA Transmitter

(See figure 6-5 of WCAP test report)

Figure B-5 Wide Range Resistance Temperature Detector (RTD)

(See figure 6-6 of WCAP test report)

Figure B-6 Narrow Range Resistance Temperature Detector

(See figure 6-7 of WCAP test report)

Figure B-7 10-50 mA Current Loop Output Monitoring

(See figure 6-9 of WCAP test report)

Figure B-8 Contact Output Monitoring

(See figure 6-8 of WCAP test report)

Figure 8-9 Partial Trip Output Monitoring

ATTACHMENT C TRANSIENT DATA RECORDING SYSTEM CONNECTIONS

This attachment contains the following:

- o Table C-1 Tape Recorded Data
- o Table C-2 Data Logger Recorded Data
- o Table C-3 Strip Chart Recorded Data

TABLE C-1 TAPE RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block		ermina onnect Lo		Buffer Amplifier Gain
1.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
2.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
3.	Bistable Partial 'rip	ITS/441C	13-L	1	2		.05
4.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
5.	Bistable Partial Trip	1TS/441H	13-L	7	8		.05
6.	Jistable Partial Trip	ITS/441G	13-L	5	6		.05
7.	Contact Output	ITY/441	13-M	5	5		.02
8.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
9.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
10.	Analog Input I/E	IPY/4580	*				10
11.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
12.	Analog Input I/E	IPY/408	*				20
13.	Analog Output E/1	IPY/408B	13-N	7	8	9	10
14.	Function Generator Sig.	N/A	**				. 05

^{*}Measure current across 20 ohm transmitter test resistor. See figure B-4.

^{**}Monitor function generator output signal. See figure B-3.

TABLE C-2 DATA LOGGER RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block		minal necti Lo	
	Analog Input E/E	TNV/AA1D	13-C	1	2	3
6. 7.	Analog Input E/E Analog Input E/E	INY/441B INY/441A	13-C	4	5	6
9.	Contact Output	ITY/441	13-M	5	6	
10.	Contact Output	ITY/441A	13-M	7	8	
22.	Analog Output E/I	ITY/641L	13-2	10	11	12
23.	Analog Output E/I	ITY/454A	13-G	4	5	6
24.	Analog Output E/I	ITY/441K	13-P	7	8	9
25.	Analog Output E/I	ILY/502B	13-K	1	4	5
26.	Analog Output E/I	IPY/408B	13-N	7	8	11
27.	Analog Output E/I	ILY/503B	13-K	7	10	11
35	Analog Input I/E	IPY/458Q				
36	Anal o Input I/E	ILY/502				
37	Analog Input I/E	ILY/503	*			
38	Analog Input I/E	IPY/408	*			

^{*}Measure current across 20 ohm transmitter test resistor. See figure 8-4.

TABLE C-3 STRIP CHART RECORDED

Channel #	Recorded Signal	Tag #	Terminal Block		ermina onnect Lo		Buffer*** Amplifier Gain
1.	Function Generator Sig.	N/A	**				.05
2.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
3.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
4.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
5.	Bistable Partial Trip	ITS/441D	13-L	3	4		. 05
6.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
7.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
9.	Contact Output	ITY/441	13-M	5	6		.02
10.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
11.	Analog Cutput E/I	ITY/441L	13-K	7	10	11	10
12.	Analog Input I/E	IPY/4580					10
13.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
14.	Analog Input I/E	IPY/408	*				20
15.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
16.	Anaiog Input E/E	INY/441A	13-C	4	5	6	2.0

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

^{**} Monitor function generator output signal. See figure B-3.

^{***} Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

FOR

EAGLE-21 PROTECTION

SYSTEM

1.0 INTRODUCTION

Yris projection system.

These tests will consist of applying fault voltages to the Eagle-21 system isolation devices. Tests are summarized by isolator board type below:

LINE TO GROUND FAULT TEST PERFORMED

isulator Board	Faults Applied
Partial Trip Output, Energized	125 Vdc, 125 Vac, 250 Vdc, 580 Vac
Partial Trip Output, Deenergized	250 Vdc, 580 Vac
Digital Contact Cutput, NO, Energized	250 Vdc, 580 Vac
Digital Contact Output, NC, Energized	250 Vdc, 580 Vac
Current Loop Output	125 Vac, 125 Vdc, 250 Vdc, 580 Vac

LINE TO LINE FAULT TESTS PERFORMED

Isolator Board	Faults Applied
Partial Trip Output, Energized	125 VAC, 125 Vdc, 250 Vdc, 580 Vac
Partial Trip Output, Deenergized	250 Vdc, 580 Vac
Digital Contact Output, NO, Engargized	125 Vac, 125 Vdc, 250 Vdc, 580 Vac
Digital Contact Output, NC, Engergized	250 Vdc, 580 Vac
Digital Contact Output, NO, Deenergized	250 Vdc, 580 Vac
Digital Contact Output, NC, Deenergized	125 Vac, 125 Vdc, 250 Vdc, 580 Vac
Current Loop Output 10-50 mA	125 VAC, 125 Vdc, 250 Vdc, 580 Vac

The test configuration is documented in Attachment B.

2.0 PREPARATION FOR TEST

- 2.1 Connect the field cabling to sensor simulation, load simulation, and contact output loads per Attachment B and table 1-1.
- 2.2 Obtain system baseline data:
 - 2.2.1 System baseline data will be taken to verify system operation. Input voltage and current and resistance values corresponding to 0 100% of scale in 25% increments and record. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.
 - 2.2.2 Set signal inputs per table 1-1. Adjust analog input signals, using the MMI to obtain the expected engineering unit values specified in table 1-1. Using figure B-6 as a reference, adjust the variable RTD channel per the following procedure:
 - o Open the manual switch input to the variable RTD board.
 - o Adjust the high adjust potentiometer so that channel TE-441A3 reads 618.261+/-.375 Deg f on the MMI.
 - o Verify that the TAVG MMI reading equals 589.740 + .2 Deg f. Verify the following actual bistable output status:

TS/441C - Not Tripped

TS/441G = Not Tripped

TS/441D - Not Tripped

TS/441H = Not Tripped

TS/442D = Tripped

TS/442G = Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Close the manual switch input to the variable RTD board.
- o Adjust the low adjust potentiometer so that channel TE-441A3 reads 615.501+/-.375 Deg f on the MMI.
- Verify that the Delta T MMI reading equals 104.237-.3PU.
 Verify the following actual bistable output status:

TS/1441C - Tripped

TS/1441G = Tripped

TS/1441D = Tripped

TS/1441H = Tripped

TS/1442D = Not Tripped

75/1442G - Not Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Open the manual switch input to the variable RTD board and record the results. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.
- 2.2.3 Set the function generator output to the variable RTD board (see figure 8-3) in the positive square wave pulse mode with a 0-5 volt amplitude at .OSHZ and a duty cycle of approximately 10%.
- 2.2.4 Close the recorder start switch and verify that the trip output signals switch upon receipt of the function generator switch signal (positive square wave pulse).

3.0 FAULT TEST PROCEDURE SEQUENCE

The fault test sequence described below will be followed for each isolator board type specified in Sections 4.0 through 6.0.

3.1 Pretest

Obtain a data logger printout of "normal" analog input/output and digital output values.

- 3.2 Disconnect data logger and verify "antenna" connections and configuration for each injection point per Attachment A.
- 3.3 Connect the fault voltage source and verify the readiness of the data acquisition system. Enter identifying records in tape recorder log and noise test data sheet (figure 1-6). Follow the test specific instructions given in Sections 4 through 6.
- 3.4 Disconnect the data logger, close the recorder start switch, start the tape recorder and record 1 minute of pretest data. Disconnect the test station from the channel under test. Simultaneously energize the fault voltage source and close the event marker switch. Record 1 minute of data with the fault voltage source applied. Observe the strip chart recorder and record any analog output signal deviations and/or trip output status failures. A trip output status failure is defined as a failure of a trip output signal to switch upon receipt of the switch signal from the test station. Remove the fault voltage source and open the event marker switch. Reconnect the test station to the channe! under test. Record 1 minute of post test data and open the recorder start switch and stop the tape recorder.
- 3.5 Obtain a data logger printout and confirm system recovery by comparing to pretest data. Record any discrepancies. If channel under test or adjacent channels are inoperable and damaged following fault application, channel(s) must be repaired. Record all

- romponent and/or board (i.e.,blown/damaged PC track) repairs required to return channel under test or adjacent channel to operation. If board is damaged see note in Appendix A for guidance.
- 3.6 If the fault voltage source breaker is tripped the fault test is invalid. Increase the fault voltage source breaker current rating and repeat the test.
- 3.7 With the system confirmed to be in the pretest condition, proceed to the next test.

4.0 CURRENT LOOP OUTPUT BOARD TEST

- 4.1 Configure the []b,c transformer as a 125 VAC fault voltage source (figure 1-1). Monitor the channels designated per tables C-la, C-2a and C-2b.
- 4.2 Connect the transformer secondary hot lead to the terminal connection of the EAO channel under test as specified in table A-la. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth ground (third prong of the AC power feed).
- 4.3 Follow the test sequence in section 3 for each test specified in table A-la for the EAO channel under test.
- 4.4 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 4.5 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-1b.
- 4.6 Follow the test sequence in section 3 for each test specified in table A-1b for the EAO channel under test.

- 4.7 Connect the []b,c DC power supply as a 125 VDC fault voltage source (figure 1-2).
- 4.8 Connect the DC power supply positive and negative leads to the terminal connection of the EAO channel under test as specified in table A-2a.
- 4.9 Follow the test sequence described in section 3 for each test specified in table A-2a for the EAO channel under test.
- 4.10 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-2b.
- 4.11 Follow the test sequence in section 3 for each test specified in table A-2b for the EAO channel votest.
- 4.12 Connect the [$_{\rm b,c}$ DC power supply as a 250 VDC fault voltage source (figure 1-2).
- 4.13 Connect the DC power supply positive and negative leads the terminal connection of the EAO channel under test as specified in table A-3a.
- 4.14 Follow the test sequence described in section 3 for each test specified in table A-3a for the EAO channel under test.
- 4.15 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-3b.
- 4.16 Follow the test sequence in section 3 for each test specified in table A-3b for the EAO channel under test.
- 4.17 Configure the []_{b,c} transformer as a 580 VAC fault voltage source (figure 1-3).

- 4.18 Connect the transformer secondary hot lead to the terminal connection of the EAO channel under test as specified in table A-4a. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth ground (third prong of the AC power feed).
- 4.19 Follow the test sequence described in section 3 for each test specified in table A-4a for the EAO channel under test.
- 4.20 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 4.21 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-4b.
- 4.22 Follow the test sequence in section 3 for each test specified in table A-4b for the EAO channel under test.

5.0 DIGITAL CONTACT OUTPUT BOARD TEST

- 5:1 Configure the []_{b,c} transformer as a 125 VAC fault voltage source (figure 1-1). Monitor the channels designated per table C-1b, C-2b, C-3b.
- 5.2 Connect the transformer secondary hot and neutral leads to the terminal connection of the ECO channel under test as specified in table A-1b.
- 5.3 Follow the test sequence in section 3 for each test specified in table A-1b for the ECO channel under test.
- 5.4 Connect the [$j_{b,c}$ DC power supply as a 125 VDC fault voltage source (figure 1-2).

- 5.5 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-2b.
- 5.6 Follow the test sequence in section 3 for each test specified in table A-2b for the ECO channel under test.
- 5.7 Connect the [$j_{b,c}$ DC power supply as a 250 VDC fault voltage source (figure 1-2).
- 5.8 Connect the DC power supply positive and negative leads to the terminal connection of the ECO channel under test as specified in table A-3a.
- 5.9 Follow the test sequence described in section 3 for each test specified in table A-3a for the ECO channel under test.
- 5.10 Connect the DC power supply positive and negative terminal leads to the terminal connection of the channel under test as specified in table A-3b.
- 5.11 Follow the test sequence in section 3 for each test specified in table A-3b for the ECO channel under test.
- 5.12 Configure the []b,c transformer as a 580 VAC fault voltage source (figure 1-3).
- 5.13 Connect the transformer secondary hot lead to the terminal connection of the ECO channel under test as specified in table A-4a. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth ground (third prong of the AC power feed).
- 5.14 Follow the test sequence described in section 3 for each test specified in table A-4a for the ECO channel under test.

- 5.15 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 5.16 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-4b.
- 5.17 Follow the test sequence in section 3 for each test specified in table A-4b for the ECO channel under test.

6.0 PARTIAL TRIP OUTPUT BOARD TEST

- 6.1 Configure the [$]_{b,c}$ transformer as a 125 VAC fault voltage source (figure 1-1). Monitor the channels designated per tables C-1c, C-2c, C-3c.
- 6.2 Connect the transformer secondary hot lead to the terminal connection of the EPT channel under test as specified in table A-la. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth ground (third prong of the AC power feed).
- 6.3 Follow the test equence in section 3 for each test specified in table A-la for the EPT channel under test.
- 6.4 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 6.5 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-1b.

- 6.6 Follow the test sequence in section 3 for each test specified in table A-la for the EPT channel under test.
- 6.7 Connect the []b,c DC power supply as a 125 VDC fault voltage source (figure 1-2).
- 6.8 Connect the DC power supply positive and negative leads to the terminal connection of the EPT channel under test as specified in table A-2a.
- 6.9 Follow the test sequence described in section 3 for each test specified in table A-2a for the EPT channel under test.
- 5.10 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-2b.
- 6.11 Follow the test sequence in section 3 for each test specified in table A-2b for the EPT channel under test.
- 6.12 Connect the [$j_{b,c}$ DC power supply as a 250 VDC fault voltage source (figure 1-2).
- 6.13 Connect the DC power supply positive and negative lead the terminal connection of the EPT channel under test as specified in table A-3a.
- 6.14 Follow the test sequence described in section 3 for each test specified in table A-3a for the EPT channel under test.
- 6.15 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-3b.
- 6.16 Follow the test sequence in section 3 for each test specified in Table A-3b for the EPT channel under test.

- 6.17 Configure the []b,c transformer as a 580 VAC fault voltage source (figure 1-3).
- 6. 3 Connect the transformer secondary hot lead to the terminal connection of the EPT channel under test as specified in table A-4a. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth gr und (third prong of the AC power ted).
- 6.19 Follow the test sequence described in section 3 for each test specified in table A-4a for the EPT channel under test.
- 6.20 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 6.21 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-4b.
- 6.22 Follow the test sequence in section 3 for each test specified in table A-4b for the EPT channel under test.

(See figure 5-9 of WCAP test report)

Figure 1-1 Transformer Connection for the 125 VAC Fault Source

(See figure 5-11 of WCAP test report)

Figure 1-2 DC Power Supply Connections

(See figure 5-10 of WCAP test report)

Figure 1-3 Transformer Connection for the 580 VAC Fault Source

7.0 ACCEPTANCE CRITERIA

7.1 Description

The acceptance criteria for the Eagle 21 (1E Safety Related System) is that the system shall remain operational and maintain protective actions before, during and after the application of credible fault voltages. Faults shall not propagate across the Class non-1E to Class 1E isolation barrier or from channel to channel.

TABLE 1-1 SUMMATED IMPUT SIGNAL

	Chemina I. France	Chemei Tug #	Firefall	ı ü	Terminel Commection Lo	d e	L/O Boerd Localism	ű	1/0 Board Commention Lo	6	Simeletor Signal	Expected Eigent In E. II.
ú	Neutron Flux Lower Ion	FF-44 LA	2.0		en		*-101		n		3.00	18.00 ± .005
ni	Reutero Flux Upper Inc	87-4418	13-6	wi	24		135-4	н			4.54 welt	29.00 ± .005
	Presentiser Presents	PT/4580	13-8	í	v	,	137-8	2.2	13	1	38.75 88.	2235 ± 1.00
	Cold ing Tampersture	TE-4413	4-11	1,2	6,3		137-6	6,3	7.4	**	423, 956 class	362.76 ± .875
	Cold Lag Temperature	1E-4408	13-1	2,6	10,9	111	137-8	8,11	8,12	*	425.888 obs	562.76 ± 375
	Sot Leg Tempersture	TE-44 [M]	13-8	1,2	4.3	*	1313	6.9	1.4	44	447.382 class	818.041 ± .875
	Sot Lag Tampersture	TE-441342	13-8	7.6	10,0	113	137-3	9,11		1.6	447.392 obses	818.041 ± .373
	Sot Lay Temporature	TR-441A3	13-C	0.00	11,10	12	1377-3	20,17	23,18	113	ands at	***
	Stomm Generator Level Long 2	17-502	13-41	**	74	m	1317-2	٠	п	£	2 22	25 ± .1268
10.	Steem Generator Level Loop 3	LT-303	3-61	*	*		137-2	20	a	13	8 1	75 ± .1268
ii.	MCS Wide Zenge Pressure	FT-406	10-8	44	н		13T-8	2		n	12 Ns.	1306 ± 8.78
13.	Presentiser Vapor Temp	725-434	13-0	1.2	¥.3	*1	137-4	20,17	21,10	n	9400 00+	490,268 ± 1.05
13.	Residuel Bost Removel Pump Discharge Temp	18-612	13-0	8,8	11,10	ņ	*10	27.72	23,25	n	300 0846	260.406 ± 1.05

XX - Teriable RTD input, set nominally at 467.175 obms (815.302 Deg f) for the low resistance reading and 448.284 obms (818.261 Deg f) for the high resistance reading. See step 2.3.2 for details.

I/O Module			Procedure Rev	
TYPE				
SHORT CIRCUIT	, AC	Burkey Kare	, DC	
			MINUS GR	
LINE TO LINE	VOLTS (+) 7	(+) OT	_ (+) TO (-)	
TEST INJECTION POINT		TEST CONDITI	ON	
I/O CARD TYPE		POINT #		
PRE-TEST				
DATA LOGGER VERIFICA	TION*	PRINT OUTPUT #		
SYSTEM STATUS			THE RESIDENCE OF THE PERSON OF	
REMARKS AND TEST OBS	ERVATION			
DISCONNECT DATA LOGG	ER			
TEST				
TAPE RECORDER FOOTAG	E BEGIN	END	SET # (STOP):	
SYSTEM STATUS:				
POST-TEST				
DATA LOGGER DATA VE				
REMARKS AND TEST OB				
	A P P P P P P P P P P P P P P P P P P P	DENTERED		

Figure 1-4. Fault Test Data Sheet

ATTACHMENT A FAULT VOLTAGE SOURCE CONNECTIONS

NOTE: If the isolator board is damaged (i.e., blown/damaged PC track) during fault testing an alternath channel must be chosen for testing. The Data Recording System Connections, Appendix C must be modified to ensure that Channels adjacent (left, right, top, bottom) to the channel under test are monitored. Record in a permanent record book any changes made to the test connections specified in this Appendix and the recording connections specified in Appendix C.

This attachment contains the following tables:

- o Table A-la 125 VAC Line-to-Ground Fault Connections
- o Table A-15 125 VAC Line-to-Line Fault Connections
- o Table A-2a 125 VDC Line-to-Ground Fault Connections
- o Table A-2b 125 VDC Line-to-Line Fault Connections
- o Table A-3a 250 VDC Line-to-Ground Fault Connections
- o Table A-3b 250 VDC Line-to-Line Fault Connections
- o Table A-4a 580 VAC Line-to-Ground Fault Connections
- o Table A-4b 580 VAC Line-to-Line Fault Connections

TABLE A-la

125 VAC LINE-TG-GROUND FAULT CONNECTIONS

				HOL L	ead To		I/O Board
Ch #	annel	1/0 Description	Channel Tag #	Terminal Block	Connection	Isolator Type	Location/ Channel #
*	8.	Bistable Partial Trip (EPT), Energized	ITS/44iC	13-L	1	Class non 1E/1E Isolation Barrier	13T-9/1
*	2.	Bistable Partial Trip (EPT), Energized	1TS/441C	13-L	2	Class non IE/IE Isolation Barrier	13T-9/1
	3.	Current Loop Output (EAO)	ITY/441N	13-R	5	Class non 1E/1E Isolation Barrier	131-14/4
	4.	Current Loop Output (EAO)	ITY/441N	13-R	4	Class non 1E/1E Isolation Barrier	13T-14/4

^{*} Disconnect Function Generator input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

TABLE A-15
125 VAC LINE-TO-LINE FAULT CONNECTIONS

Channel	I/O Description	Channel Tag #	Terminal Block	Connect Tran	THE RESERVE OF THE PARTY OF THE	Isolator Type	I/O Board Location/ Channel #
* 1.	Bistable Partial Trip (EPT) Energized	ITS/441C	13-L	1	2	Class non IE/IE Isolation Barrier	13T-9/1
2.	Current Loop Output (EAO)	ITY/441N	13-R	4	5	Class non 1E/1E Isolation Barrier	13T-14/4
3.	Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
	Digital Contact Output (ECO), Deenergized, NC	ITY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	13T-12/2

^{*} Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

^{**} Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

TABLE A-2a

125 VDC LINE-TO-GROUND FAULT CONNECTIONS

Ch	ennel	1/0 Description	Channel Tag #	Terminal Block	Positive	Negative	Isolator Type	1/0 Board Location/ Channel #
*	1.	Bistable Partial Trip (EPT), Energized	1TS/441C	13-L	1	G	Class non IE/IE Isolation Barrier	13T-9/1
*	2.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	2	G	Class non 1E/1E Isolation Barrier	13T-9/1
*	3.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	G	1	Class non 1E/1E Isolation Barrier	13T-9/1
*	4.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	G	2	Class non 1E/1E Isolation Barrier	13T-9/1
	5.	Current Loop Output (EAO)	ITY/441N	13-R	4	G	Class non 1E/1E Isolation Barrier	13T-14/4

G - Earth ground (third prong of AC power feed)

^{*} Disconnect function generator input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

TABLE A-2a (Continued) 125 VDC LINE-YO-GROUND FAULT CONNECTIONS

hanne]	i/O Description	Channel Tag #	Terminal Block		Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
6.	Current Loop Output (EAO)	ITY/441N	13-R	5		Class non 1E/1E Isolation Barrier	13T-14/4
7.	Current Loop Output (EAG)	1TY/441N	13-R	G	4	Class non 1E/1E Isolation Barrier	13T-14/4
8.	Current Loop Output (EAO)	ITY/144N	13-R	G	5	Class non 1E/1F Isolation Barrier	13T-14/4

G - Earth ground (third prong of AC power feed)

TAB'E A-2b

125 VDC LINE-TO-LINE FAULT CONNECTIONS

Cha	annel	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
*	1.	Bistable Partial Trip (EPT) Energized	1TS/441C	13-L	1	2	Class don 1E/1E Isolation Barrier	13T-9/1
*	2.	Bistable Partial Trip (EPT) Energized	1TS/441C	13-L	2	1	Class non 1E/1F Isolation Barrier	13T-9/1
	3.	Current Loop Output (EAO)	ITY/44IN	13-1	4	5	Class non 1E/1E Isolation Barrier	13T-14/4
	4.	Current Loop Output (EAO)	11Y/441N	13-K	5	4	Class non 1E/1E Isolation Barrier	131-14/4
	5.	Digita: Contact Output (ECO), Energized, NO	1TY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	131-12/2

^{*} Di connect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

^{**} Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

TABLE A-2b (Continued) 125 VDC LINE-TO-LINE FAULT CONNECTIONS

Channel #	1/0 Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
6.	Digital Contact Output (ECO), Deenergized, NC	1TY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	137-12/2
7.	Digital Contact Output (ECO) Energized, NO	ITY/441A	13-M	8	7	Class non 1E/1E Isolation Barrier	131-12/2
8.	Digital Contact Output (ECO) Deenergized, DC	ITY/441A	13-M**	8	7	Class non 1E/1E Isolation Barrier	13T-12/2

^{**} Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

TABLE A-3a
250 VDC LINE-TO-GROUND FAULT CONNECTIONS

I/O Description	Channel Tay #	Te.minal Block			Isolator Type	I/O Board Location/ Channel 4
Bistable Partial Trip (EPT) Energized	ITS/441C	13-L	1	G	Class non 1E/1E Isolation Barrier	13T-9/1
Bistable Partial Trip (EPT) Energized	ITS/144C	13-L	2	G	Class non 1E/1E Isolation Barrier	13T-9/1
Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	G	1	Class non 1E/1E Isolation Barrier	13T-9/1
Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	G	2	Class non 1E/1E Isolation Barrier	13T-9/1
Bistable Partial Trip (EPT), Deenergized	1TS/441C	13-L	1	G	Class non 1E/1E Isolation Barrier	137-9/1
Bistable Partial 7rip (EPT), Deenergized	ITS/441C	13-L	2	G	Class non 1E/1E Isolation Barrier	137-9/1
	Description Bistable Partial Trip (EPT) Energized Bistable Partial Trip (EPT) Energized Bistable Partial Trip (EPT), Energized Bistable Partial Trip (EPT), Energized Bistable Partial Trip (EPT), Deenergized Bistable Partial Trip (EPT), Deenergized	Bistable Partial Trip ITS/441C Bistable Partial Trip ITS/144C Bistable Partial Trip ITS/144C Bistable Partial Trip ITS/441C Bistable Partial Trip ITS/441C	Description Tag # Block Bistable Partial Trip ITS/441C 13-L Bistable Partial Trip ITS/144C 13-L (EPT) Energized Bistable Partial Trip ITS/441C 13-L (EPT), Energized Bistable Partial Trip ITS/441C 13-L (EPT), Energized Bistable Partial Trip ITS/441C 13-L (EPT), Deenergized Bistable Partial Trip ITS/441C 13-L Bistable Partial Trip ITS/441C 13-L Bistable Partial Trip ITS/441C 13-L Bistable Partial Trip ITS/441C 13-L	Description Tag # Block Positive Bistable Partial Trip ITS/441C 13-L 1 Bistable Partial Trip ITS/144C 13-L 2 (EPT) Energized ITS/441C 13-L G Bistable Partial Trip ITS/441C 13-L G (EPT), Energized ITS/441C 13-L G (EPT), Energized ITS/441C 13-L G Bistable Partial Trip ITS/441C 13-L 1 (EPT), Deenergized ITS/441C 13-L 1 Bistable Partial Trip ITS/441C 13-L 1 Bistable Partial Trip ITS/441C 13-L 2	Description Tag # Block Positive Negative Bistable Partial Trip ITS/441C 13-L 1 G Bistable Partial Trip ITS/144C 13-L 2 G Bistable Partial Trip ITS/441C 13-L G 1 Bistable Partial Trip ITS/441C 13-L G 2 Bistable Partial Trip ITS/441C 13-L G 2 Bistable Partial Trip ITS/441C 13-L G 6 Bistable Partial Trip ITS/441C 13-L 1 G Bistable Partial Trip ITS/441C 13-L 2 G	Description Tay # Block Positive Negative Type Bistable Partial Trip ITS/441C 13-L 1 G Class non 1E/1E Isolation Barrier Bistable Partial Trip ITS/144C 13-L 2 G Class non 1E/1E Isolation Barrier Bistable Partial Trip ITS/441C 13-L G 1 Class non 1E/1E Isolation Barrier Bistable Partial Trip ITS/441C 13-L G 2 Class non 1E/1E Isolation Barrier Bistable Partial Trip ITS/441C 13-L G 2 Class non 1E/1E Isolation Barrier Bistable Partial Trip ITS/441C 13-L G Class non 1E/1E Isolation Barrier Bistable Partial Trip ITS/441C 13-L 1 G Class non 1E/1E Isolation Barrier Bistable Partial Trip ITS/441C 13-L 2 G Class non 1E/1E Isolation Barrier Bistable Partial Trip ITS/441C 13-L 2 G Class non 1E/1E Isolation Barrier

G - Earth Ground (third prong of AC power feed)

^{*} Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

TABLE A-3a (Continued) 250 VDC LINE-TO-GROUND FAULT CONNECTIONS

Channel	I/G Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	I/O Board Location, Channel #
7.	Bistable Partial Trip (EPT) Deenergized	ITS/441C	10 L	G	1	Class non 1E/1E Isolation Barrier	137-9/1
8.	Bistable Partial Trip (EPT) Deenergized	ITS/4410	13-L	G	2	Class non 1E/IE Isolation Barrier	13T-9/1
9.	Current Loop Output (EAO)	ITY/44IN	13-R	•	G	Class non 1E/1E Isolation Barrier	13T-14/4
10.	Current Loop Out, ut (EAO)	1TY/441N	13-R	5	ů	Class non 1E/1E Isolation Barrier	13T-14/4
11.	Current Loop Output (EAO)	ITY/441N	13-R	G		Class non 1E/1E Isolation Barrier	13T-14/4
12.	Current Loop Output (EAO)	ITY/441N	13-R	G		Class non 1E/1E Isolation Barrier	13T-14/4

G = Earth Ground (third prong of AC power feed)

^{*} Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to contro' partial trip output condition during fault application.

Channel	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
13.	Digital Contact Output (ECO), Energized, NO	1TY/441A	13-M	7	G	Class non 1E/1E Isolation Barrier	13T-12/2
14.	Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	G	7	Class non IE/IE Isolation Barrier	13T-12/2
15.	Digital Contact Output (ECO), Energized, NC	ITY/441A	13-M**	7	G	Class non 1E/1E Isolation Barrier	131-12/2
16.	Digital Contact Output (ECO), Energized, NC	ITY/441A	13-M**	6	7	Class non 1E/1E Isolation Barrier	13T-12/2

G = Earth Ground (third prong of AC power feed)

^{**} Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

TABLE A-3b
250 VDC LINE-TO-LINE FAULT CONNECTIONS

Channel	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	1/G Board Location/ Channel
* 1.	Bistable Partial Trip	1TS/441C	13-L	1	2	Class non 1E/1E Isolation Barrier	131-9/1
* 2.	Bistable Partial Trip (EPT) Energized	1TS/154C	13-L	2	1	Class non 1E/1E Isolation Barrier	13T-9/1
* 3.	Bistable Partial Trip (EPT), Deenergized	1TS/441C	13-L	1	2	Class non IE/IE Isolation Barrier	13T-9/1
* 4.	Bistable Partial Trip (EPT), Deenergized	1TS/441C	13-L	2	1	Class non IE/IE Isolation Barrier	13T-9/1
5.	Current Loop Output (EAO)	1TY/441N	13-R	4	5	Class non 1E/1E Isolation Barrier	13T-14/4
6.	Current Loop Output (EAO)	ITY/441N	13-R	5	4	Class non 1E/1E Isolation Barrier	13T-14/4

^{*} Disconnect function generation frout to variable RTD channel (figure 8-1) and use manual switch to control partial trip output condition during fault application.

TABLE A-3b (Continued)
250 VCC LINE-TO-LINE FAULT CONNECTIONS

1/0 Description	Channel Tag #	Terminal Block			Isolator Type	I/O Board Location/ Civannel #
Digital Contact Output (ECO) Energized, NO	ITY/441A	13-M	7	8	Class non it/lE Isolation Barrier	13T-12/2
Digital Contact Output (ECO) Deenergized, NC	ITY/144A	12-M**	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	8	7	Class non 1E/1E Isolation Barrier	13T-12/2
Digital Contact Output (ECO) Deenergized, NC	ITY/441A	13-M*	8	7	Class non 1E/1E Isolation Barrier	13T-12/2
Digital Contact Output (ECO), Deenergized, NO	1TY/441A	13-H	7	8	Class non 1E/1E Isolation Barrier	131-12/2
	Description Digital Contact Output (ECO) Energized, NO Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO), Energized, NO Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO) Deenergized, NC	Description Tag # Digital Contact Output (ECO) Energized, NO Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO), Energized, NO Digital Contact Output (ECO), Energized, NO Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO) Deenergized, NC	Description Tag # Block Digital Contact Output (ECO) Energized, NO Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO), Energized, NO Digital Contact Output (ECO), Energized, NO Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO) Deenergized, NC	Description Tag # Block Positive Digital Contact Output ITY/441A 13-M 7 Digital Contact Output ITY/144A 13-M** 7 Digital Contact Output ITY/441A 13-M** 8 Digital Contact Output ITY/441A 13-M* 8 Digital Contact Output ITY/441A 13-M* 8 Digital Contact Output ITY/441A 13-M* 7	Digital Contact Output (ECO) Deenergized, NO Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO), Energized, NO Digital Contact Output (ECO), Energized, NO Digital Contact Output (ECO), Energized, NC Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO) Deenergized, NC Digital Contact Output (ECO) Deenergized, NC	Digital Contact Output ITY/441A 13-M 7 8 Class non 1E/1E Isolation Barrier Digital Contact Output ITY/441A 13-M 7 8 Class non 1E/1E Isolation Barrier Digital Contact Output ITY/441A 13-M 8 7 Class non 1E/1E Isolation Barrier Digital Contact Output ITY/441A 13-M 8 7 Class non 1E/1E Isolation Barrier Digital Contact Output ITY/441A 13-M 8 7 Class non 1E/1E Isolation Barrier Digital Contact Output ITY/441A 13-M 8 7 Class non 1E/1E Isolation Barrier Digital Contact Output ITY/441A 13-M 8 7 Class non 1E/1E Isolation Barrier Digital Contact Output ITY/441A 13-M 7 8 Class non 1E/1E Isolation Barrier

^{*} Disconnect function generation input to variable RTD channel (figure B-I) and use manual switch to control partial trip output condition during fault application.

^{**} Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

TABLE A-3b (Continued)
250 VDC LINE-TO-LINE FAULT CONNECTIONS

Channel	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Hegative	Isolator Type	I/O Board Location/ Channel #
12.	Digital Contact Output (ECO) Energized, NC	ITY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
13.	Digital Contact Output (ECO) Deenergized, NO	TTY/144A	13-M	8	7	Class non 1E/1E Isolation Barrier	13T-12/2
14.	Digital Contact Output (ECO), Energized, NC	1TY/441A	13-H**	8	7	Class non 1E/1E Isolation Barrier	13T-12/2

^{**} Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

TABLE A-4a
580 VAC LINE-TO-GROUND FAULT CONNECTIONS

Channe #	l I/O Description	Channel Tag #	Terminal Block	Connect Transformer Secondary Hot Lead to Connection	Isolator Type	I/O Board Location/ Channel #
* L.	Bistable Partial Trip (EPT) Energized	1TS/441C	13-L	1	Class non 1E/1E Isolation Barrier	13T-9/1
* 2.	Bistable Partial Trip (EPT) Energized	ITS/144C	13-L	2	Class non 1E/1E Isolation Barrier	131-9/1
* 3.	Bistable Partial Trip (EPT), Deenergized	1TS/441C	13-L	1	Class non 1E/1E Isolation Barrier	131-9/1
4.	Bistable Partial Trip (EPT), Deenergized	TTS/441C	13-L	2	Class non 1E/1E Isolation Barrier	13T-9/1
5.	Current Loop Output (EAO)	ITY/441H	13-R	4	Class non 1E/IE Isolation Barrier	131-14/4
6.	Current Loop Output (EAO)	ITY/441N	13-R	5	Class non 1E/1E isolation Ba:rier	13T-14/4

^{*} Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

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TABLE A-4a (Continued)

580 VAC LINE-TO-6 " FAULT CONNECTIONS

Channel	I/O Description	Channel Tag #	Terminal Block	Connect Transformer Secondary Hot Lead to Connection	Isolator T _{3-P} e	I/O Board Location/ Channel #
7.	Digital Contact Output (ECO) Energized, NO	ITY/441A	13-M	7	Class non 1E/1E Isolation Barrier	137-12/2
8.	Digital Contact Output (ECO) Energized, NC	ITY/144A	13-M**	7	Class non 1E/1E Isolation Barrier	13T-12/2

^{**} Move wire terminated on 13T-12-6 to 12-T-12-7 to test NC configuration.

TABLE A-45
580 VAC LINE-TO-LINE FAULT CONNECTIONS

Ch:	annel	I/O Description	Channel Tag #	Terminal Block	Connect Tra		Isolator Type	I/O Board Location/ Channel #
	1.	Bistable Partial Trip (EPT) Energized	1TS/441C	13-L	1	2	Class non 1E/1E Isolation Barrier	13T-9/1
	2.	Bistable Partial Trip (EPI) Deenergized	ITS/144C	13-L	1	2	Class non 1E/1E Isolation Barrier	131-9/1
	3.	Current Loop Output (EAO)	1TY/441N	13-R	4	5	Class non IE/IE Isolation Barrier	13T-14/4
	4.	Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	13T-14/4
	5.	Digital Contact Output (ECO), Deenergized, NC	ITY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	137-12/2
	6.	Digital Contact Output (ECO), Deenergized, NO	ITY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
	7.	Digital Contact Output (ECO) Energized, NC	ITY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	13T-12/2

^{*} Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition G ing fault application.

^{**} Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

ATTACHMENT B FIELD CONNECTIONS AND SIMULATION

See test procedure JPD-111687-O figures B-3 through B-9 for input simulation and input/output monitoring connections.

Cobinet Configuration Information:

The cabinet under test, Qualification Unit 2, is an exact replica of Watts Bar Nuclear Power Station Protection Rack 13. The following drawings document the cabinet configuration. Copies of these drawings will be included as part of the final test report.

Drawing Description	Drawing Number/Rev.
Terminal Block Wiring Diagram, Protection Set 4	1-47043 PW-13, rev. 3E
Process Control Block Diagram, Delta T/T _{AVG} System	108D408 sh. 10, rev. 11
Process Control Block Diagram, W.R. S.G. Level	108D408 sh. 34, rev. 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temp.	1080408 sh. 38, rev. 4
Process Control Block Diagram, RHR Pump Discharge Temp	108D408 sh. 39, rev. 5
Process Control Block Diagram, RCS Wide Range Pressure	108D408 sh. 43, rev. 1
Eagle-21 Schematic Diagrams, Rack 13 Protection Set 4	1856E69 sh. 2, rev. 2

. ATTACHMENT C TRANSIENT DATA RECORDING SYSTEM CONNECTIONS

This attachment contains the following:

- o Table C-la Tape Recorded Data, Current Loop Output Test
- o Table C-1b Tape Recorder Data, Digital Contact Output Test
- o Table C-1c Tape Recorder Data, Partial Trip Output Test
- o Table C-2a Data Logger Recorded Data, Current Loop Output Test
- o Table C-2b Data Logger Recorder Data, Digital Contact Output Test
- o Table C-2c Data Logger Recorder Data, Partial Trip Output Test
- o Table C-3a Strip Chart Recorded Data, Current Loop Output Test
- o Table C-3b Strip Chart Recorder Data, Digital Contact Output Test
- o Table C-3d Strip Chart Recorder Data, Partial Trip Output Test

TABLE C-1a
TAPE RECORDED DATA, CURRENT LOOP OUTPUT TEST

,	Record Signal	port of		Tag #	Terminal Block	Co	rmina nnect		Buffer Amplifie Gain
						711		211	0.0.111
1.	Analog	Output	E/1	ITY/441L	13-P	10	11	12	10
2.	Analog	Output	E/I	ITY/503A	13-J	10	11	12	10
3.	Analog	Output	E/I	ITY/502A	13-J	7	8	9	10
4.	Analog	Output	E/I	ITY/441Q	13-5	1	2	3	10
5.	Analog	Output	E/1	17Y/441G	13-H	1	4	5	10
6.	PolsnA	Output	E/I	ITY/441F	13-J	1	4	5	10
7.	Analog	Jutput	E/I	1TY/502B	13-K	1	4	5	10
8.	Arralog	Output	E/I	ITY/442C	13-F	9	11	12	10
9.	Analog	Output	E/1	ITY/441M	13-R	1	2	3	10
10.	Inalog	Output	E/I	ITY/441P	13-R	7	8	9	10
11.	inalog	Output	F/1	ITY/442G	13-G	1	2	3	10
12.	Analog	Output	E/I	ILY/503B	13-K	7	10	11	10
13.	Analog	Output	E/I	ITY/441E	13-H	7	10	11	10
14.	Analog	Output	E/1	ITY/454B	13-F	1	2	3	10

^{*} Measure current across 20 ohm transmitter test resistor. See figure 8-4.

^{**} Monitor function generator output signal. See figure B-3.

TABLE C-16
TAPE RECORDED DATA, DIGITAL CONTACT OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block		rmina nnect Lo		Buffer Amplifier Gain
1.	Bistable Partial Trip	ITS/442D	13-M	3	4		.05
2.	Bistable Partial Trip	1TS/442G	13-M	1	2		.05
3.	Contact Output	ITY/441C	13-M	11	12		.02
4.	Contact Output	ITY/441D	13-M	9	10		.02
5.	Analog Output E/I	1TY/441G	13-H	1	4	5	10
6.	Analog Output E/I	ITY/441F	13-J	1	4	5	10
7.	Contact Output	ITY/441	13-M	5	6		.02
8.	Analog Output E/I	ITY/442C	13-G	- 1	2	3	10
9.	Analog Output E/I	1TY/441E	13-H	7	10	11	10
10.	Analog Output E/I	ITY/441H	13-P	1	2	3	10
11.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
12.	Analog Output E/1	ITY/441J	13-P	4	5	6	10
13.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
14.	Function Generator Sig	. N/A	**				.05

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

Note: For ECO test move EPT board and termination frame wiring from T-10 to T-11.

^{**} Monitor function generator output signal. See figure B-3.

TABLE C-1c

TAPE RECORDED DATA, PARTIAL TRIP OUTPUT TEST

Channel	Recorded Signal	Tag #	Terminal Block	Co	rmina nnect Lo		Buffer Amplifier Gain
1.	Bistable Partial Trip	ITS/441G	13-L	5	6	P STATE OF THE STA	.05
2.	Bistable Partial Trip	ITS/442D	13-M	3	4		.05
3.	Bistable Partial Trip	ITS/4426	13-M	1	2		.05
4.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
5.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
6.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
7.	Analog Input I/E	IPY/408					20
8.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
9.	Analog Input I/E	1PY/458Q					10
10.	Analog Output E/I	ITY/441G	13-H	1	4	5	10
11.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
12.	Analog Output E/I	1LY/503B	13-K	7	10	11	10
13.	Analog Output E/1	ITY/441E	13-H	7	10	11	10
14.	Function Generator Sig.	N/A	**				.05

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

^{**} Monitor function generator output signal. See figure B-3.

TABLE C-2a

DATA LOGGER RECORDED DATA, CURRENT LOOP CUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection Hi Lo Sh			
6.	Analog Input E/E	INY/441B	13-C	1	2	3	
7.	Analog Input E/E	INY/441A	13-C	4	. 5	6	
21.	Analog Output E/I	ITY/441L	13-P	10	11	12	
22.	Analog Output E/I	ITY/441M	13-R	1	2	3	
23.	Analog Output E/I	ITY/442C	13-F	9	11	12	
24.	Analog Output E/I	ITY/442G	13-G	1	2	3	
25.	Analog Output E/I	ITY/441G	13-H	1	4	5	
26.	Analog Output E/I	1TY/441E	13-H	. 7	10	11 -	
27.	Analog Output E/I	ITY/441F	13-J	1	4	5	
28.	Analog Output E/I	ITY/441P	13-R	. 7	8	9	
29.	Analog Output E/I	ITY/441Q	13-S	1	2	3	
30.	Analog Output E/I	ITY/502B	13-K	1	4	5	
31.	Analog Output E/I	ITY/503A	13-J	10	11	12	
32.	Analog Output E/I	ITY/502A	13-J	7	8	9	
33.	Analog Output E/I	ITY/503B	13-K	7	10	11	
34.	Analog Output E/I	ITY/454B	13-F	1	2	3	
35	Analog Input I/E	IPY/458Q	*				
36	Analog Input I/E	ILY/502	*				
37	Analog Input I/E	ILY/503	*				
38	Analog Input I/E	IPY/408	*				

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

DATA LOGGER RECORDED DATA, DIGITAL CONTACT OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			
				Hi	Lo	Sh	
6.	Analog Input E/E	INY/441B	13-C	1	2	3	
7.	Analog Input E/E	INY/441A	13-C	4	5	6	
9.	Contact Output	ITY/441	13-M	5	6		
10.	Contact Output	ITY/441A	13-M	7	8		
11.	Contact Ou.put	ITY/441C	13-M	11	12		
12.	Contact Output	ITY/441B	13-M	9	10		
22.	Analog Output E/1	ITY/441E	13-F	5	6	7	
23.	Analog Output E/I	1TY/442C	13-F	. 9	11	12	
24.	Analog Sutput E/I	ITY/442G	13-G	1	2	3	
25.	Analog Output E/I	ITY/441G	13-H	1	4	5	
26.	An og Output E/I	ITY/441E	13-H	7	10	11	
27.	And og Output E/I	ITY/441F	13-J	1	4	5	
28.	Analog Output E/I	ITY/441H	13-P	1	2	3	
29.	Analog Output E/I	ITY/441J	13-P	4	5	6	
35.	Analog Input I/E	IPY/458Q					
36.	Analog Input 1/E	1LY/502	*				
37.	Analog Input I/E	ILY/503	*				
38.	Analog Input I/E	IPY/408	*				

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE C-2c
DATA LOGGER RECORDED DATA, P ARTIAL TRIP OUTPUT TEST

Channel	Recorded Signal	Tag	Terminal Block		minal	
	Signer		BIOCK	Hi		Sh
	Analog Input E/E	INY/441B	13-C	1	2	3
7.	Analog Input E/E	INY/441A	13-C	4	5	6
21.	Analog Output E/I	ITY/441L	13-P	10	11	12
22.	Analog Output E/I	ITY/441M	13-R	1	2	3
L.	Analog Output E/I	IPY/408B	13-N	7	8	9
24.	Analog Output E/I	ITY/442G	13-G	1	2	3
25.	Analog Output E/I	ITY/441G	13-H	1	4	5
26.	Analog Output E/I	ITY/441E	13-H	7	10	11
27.	Analog Output E/I	ITY/441F	13-J	4	4	5
28.	. log Output E/I	ITY/441P	13-R	7	8	9
29.	Analog Putput E/I	ITY/441Q	13-S	1	2	3
30.	Analog Output E/I	ITY/502B	13-K	- 1	4	5
31.	Analog Output E/I	ITY/503A	11.0	10	11	12
32.	Analog Output E/I	ITY/502A	13-3	7	8	9
33.	Analog Output E/1	17Y/.03B	13-K	7	10	11
34.	Analog Out, E/I	ITY/454B	13-F	1	2	3
35	Analog Input I/E	IPY/458Q	*			
36	Analog Input 1/E	ILY/502	*			
37	Analog I	1LY/503	*			
38	Analog Input I/E	IPY/408	*			

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE C-3a
STRIP CHART RECORDED, CURRENT LOOP OUTPUT TEST

Channel #	Recorded Signal		Tag #	Terminal Block		ermina onnect Lo		Buffer ** Amplifier Gain
1.	Analog Out	put E/I	ITY/454B	13-F	1	2	2	10
2.	Analog Out	put E/I	ITY/441L	13-P	10	11	12	10
3.	Analog Out	put E/I	ILY/503A	13-J	10	11	12	10
4.	Analog Out	put E/I	ILY/502A	13-J	7	8	9	10
5.	Analog Out	put E/I	ITY/441Q	13-5	1	2	3	10
6.	Analog Out	put E/I	ITY/441G	13-H	1	4	5	10
7.	Analog Out	put E/I	ITS/441F	13-J	1	4	5	10
8.	Analog Inp	ut E/E	INY/441B	13-C	1	2	3	2.0
9.	Analog Out	put E/I	1LY/502B	13-K	1	4	5	10
10.	Analog Out	put E/I	ITY/442C	13-F	9	11	12	10
11.	Analog Out	put E/I	ITY/441M	13-R	1	2	3	10
12.	Analog Out	put E/I	ITY/441P	13-R	7	8	9	10
13.	Analog Out	put E/I	ITY/442G	13-G	1	2	3	10
14.	Analog Out	put E/I	ILY/503B	13-K	7	10	11	10
15.	Analog Out	put E/I	ITY/441E	13-H	7	10	11	10
16.	Analog Inp	ut E/E	INY/441A	13-C	4	5	6	2.0

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

^{**} Monitor function generator output signal. See figure B-3.

^{***} Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

TABLE C-3b

STRIP CHART RECORDED, DIGITAL CONTACT OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Co	ermina onnect Lo		Buffer*** Amplifier Gain
1.	Function Generator Sig.	N/A	**				.05
2.	Bistable Partial Trip	ITS/-42D	13-M	3	- 4		.05
3.	Bistable Partial Trip	1TS/442G	13-M	-1	2		.05
4.	Contact Output	ITY/441C	13-M	11	12		.02
5.	Contact Output	ITY/441B	13-M	9	10		.02
6.	Analog Output E/I	ITY/441G	13-H	1	4	5	10
7.	Analog Output E/I	ITY/441F	13-J	1	4	5	10
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
9.	Contact Output	ITY/441	13-M	5	. 6		.02
10.	Analog Output E/I	ITY/442C	13-G	1	2	3	10
11.	Analog Output E/I	ITY/441E	13-H	1	2	3	10
12.	Analog Output E/I	ITY/441H	13-P	1	2	3	10
13.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
14.	Analog Cutput E/I	ITY/441J	13-P	4	5	6	10
15.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

^{**} Monitor function generator output signal. See togure 8-3.

^{***} Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

TABLE C-3c STRIP CHART RECORDED, PARTIAL TRIP OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Co	rmina nnect Lo		Buffer*** Amplifier Gain
1.	Function Generator Sig.	N/A	**				.05
2.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
3.	Bistable Partial Trip	ITS/442D	13-M	3	4		.05
4.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
5.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
6.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
7.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
9.	Analog Input I/E	IPY/408	*				20
10.	Analog Output E/I	IPY/408B	13-M	7	8	9	10
11.	Analog Input I/E	IPY/458Q	*				10
12.	Analog Output E/I	ITY/441G	13-H	1	4	5	10
13.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
14.	Analog Output E/I	ILY/503B	13-K	7	10	11	10
15.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

^{**} Monitor function generator output signal. See figure B-3.

^{***} Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

JPD 111687-2

DATE 11/16/87 REVISION NO.

SURGE WITHSTAND CAPABILITY TEST PROCEDURE

FOR

EAGLE-21 PROTECTION

SYSTEM

1.0 INTRODUCTION

This procedure details the Surge Withstand Capability (SWC) tests to be performed on the Eagle-21 protection system.

These tests will consist of applying the surge withstand test wave to the following system interfaces and measuring the effects on system input/output processing.

- Digital Contact Output (NO and NC configurations), class non-lE/lE isolator
- Partial Trip Output (energized and deenergized conditions), class non-1E/1E isolator
- o Current Loop Output 10-50 mA, class non-1E/1E isolator
- Current Loop Input (4-20 mA, 10-50 mA, with and without loop power supply)
- o WR RTD Input
- o WR RTD Input (0-10 volt application)
- o NR RTD Input
- o Cabinet AC power feed

The test configuration is documented in Attachments B and C.

2.0 PREPARATION FOR TEST

- 2.1 Connect the field cabling to sensor simulation, load simulation, and contact output loads per Attachments B, C and table 1-1.
- 2.2 Obtain system baseline data:
 - 2.2.1 System baseline data will be taken to verify system operation. Input voltage and current and resistance values corresponding to 0 100% of scale in 25% increments and record. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.

- 2.2.2 Set signal inputs per table 1-1. Adjust analog input signals, using the MMI to obtain the expected engineering unit values specified in table 1-1. Using figure B-6 in Noise Test Procedure JPD-111687-0 as a reference, adjust the variable RTD channel per the following procedure:
 - o Open the manual switch input to the variable RTD board.
 - o Adjust the high adjust potentiometer so that channel TE-441A3 reads 618.261+/-.375 Deg f on the MMI.
 - Verify that the TAVG MMI reading equals 589.740 + .2 Deg f.
 Verify the following actual bistable output status:

TS/441C = No: Tripled

TS/441G = Not Tripped

TS/441D = Not Tripped

TS/441H = Not Tripped

TS/442D = Tripped

TS/442G = Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Close the manual switch input to the variable RTD board.
- o Adjust the low adjust potentiometer so that channel TE-441A3 reads 615.501+/-.375 Deg f on the MMI.
- Verify that the Delta T MMI reading equals 104.237-.3PU.
 Verify the following actual bistable output status:

is/1441C = Tripped

TS/1441G = Tripped

TS/1441D = Tripped

TS/1441H = Tripped

TS/1442D = Not Tripped TS/1442G = Not Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Open the manual switch input to the .ariable RTD board and record the results. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.
- 2.2.3 Set the function generator output to the variable RTD board (see figure B-3 in Noise Test Procedure JPD-111687-0) in the positive square wave pulse mode with a 0-5 volt amplitude at .05HZ and a duty cycle of approximately 10%.
- 2.2.4 Close the recorder start switch and verify that the trip output signals switch upon receipt of the function generator switch signal (positive square wave pulse).

3.0 SWC TEST PROCEDURE SEQUENCE

The SWC test sequence described below will be followed for each noise test type specified in Sections 4.0 and 5.0.

3.1 Pretest

Obtain a data logger printout of "normal" analog input/output and digital output values.

3.2 Disconnect data logger. Configure the [

 $J_{b,c}$ and [$J_{b,c}$ isolation network as shown in figure 1-3. Set the surge generator at 120 HZ repetition rate, 3.3 KV crest voltage and timed output with a 3 second duration.

- 3.3 Connect the isolation network line out connection to the channel under test and verify the readiness of the data acquisition system. Enter identifying records in tape recorder lrg and surge test data sheet (figure 1-4). Follow the test specific instructions given in sections 4 and 5.
- 3.4 Disconnect the data logger, close the recorder start switch, start the tape recorder and record 2 minutes of pretest data. Increase strip chart speed to 25 mm/sec. Simultaneously energize the surge generator and close the event marker switch. Monitor the surge waveform on the oscilloscope and deenergize the event marker upon removal of the surge. Decrease chart speed to 100 mm/min Observe the strip chart recorder and record and analog output signal deviations and/or trip output status failures. A trip output status failure is defined as a failure of a trip output signal to switch upon receipt of the switch signal from the test station. Record 2 minutes of post test data. Open the recorder start switch and stop the tape recorder.
- 3.5 Obtain a data logger printout and confirm system recovery by comparing to pretest data. Record and discrepancies. Record any component damage incurred.
- 3.6 With the system confirmed to be in the pretest condition, proceed to the next test.

4.0 COMMON MODE SWC TEST

- 4.1 Connect the [$]_{b,c}$ isolation network line out terminals to the designated terminal block connections as specified in Table A-la. Use hook-up wire to make connections and minimize lead length.
- 4.2 Connect the surge generator "High" output to surge transient input 1 of the isolation network. Connect the surge generator "Low" output to the ground connector of the isolation network.

- 4.3 Connect the surge generator chassis ground to the isolation network ground.
- 4.4 Set the isolation network mode switch to the "Common Mode" position.
- 4.5 Follow the test sequence described in section 3 for each channel designated in Table A-la.

5.0 TRANSVERSE MODE SWC

- 5.1 Connect the [] b,c isolation network line and terminal to the designated terminal block connections as specified in Table A-lb. Use hook-up wire to make connections and minimize lead length.
- 5.2 Connect the surge generator "High" output to surge transient input 1 of the isolation network. Connect the surge generator "Low" output to surge generator transient input 2 of the isolation network.
- 5.3 Connect the surge generator chassis ground to the isolation network ground.
- 5.4 Set the isolation network mode switch to the "Transverse Mode" position.
- 5.5 Follow the test sequence described in Section 3 for each channel designated in table A-lb.

6.0 ACCEPTANCE CRITERIA

6.1 Description

The acceptance criteria for the Eagle 21 (1E Safety Related System) is that the system shall remain operational and maintain protective actions before, during and after application of the surge withstand test wave to designated class non-1E to class 1-E isolators. In addition, no component damage or change in channel calibration shall occur due to the application of the SWC test wave to any cabinet input/output excluding the test panel and MMI communication connection.

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(See figure 5-12a of WCAP test report)

Figure 1-1 Common Mode SWC Test Connections

(See figure 5-12b of WCAP test report)

Figure 1-2 Transverse Mode SWC Test Connections

(See figure 5-12c of WCAP test report)

Figure 1-3 Block Diagram of SWC Test

SURGE TEST DATA SHEET

	Procedure Rev. DATE TEST #
TYPE	
TRANSVERSE MODE	
COMMON MODE	
TEST INJECTION POINT I/O CARD TYPE	POINT #
PRE-TEST	
DATA LOGGER VERIFICATION PRINT OUTPUT #	
SYSTEM STATUS:	
REMARKS AND TEST OBSERVATION	
DISCONNECT DATA LOGGER	
IEST	
TAPE RECORDER FOOTAGE BEGIN END	SET #
SYSTEM STATUS:	
REMARKS AND TEST OBSERVATION	
POST-TEST	
DATA LOGGER DATA VERIFICATION* PRINT OUTPUT #	
SYSTEM STATUS:	
REMARKS AND TEST OBSERVATION	
PERFORMED REVIEW	VED.

Figure 1-4 Surge Test Data Sheet

TABLE 1-1 SIMMATED INPUT SIGNAL

	Charson's 1.	Chercrell Teg #	Terminal Block	ä	Terminal Connection Lo	lon Sh	1/G Board Location	II	I/O Board Commettion Lo	é	Signal	Expect in E.U
									4			18.00
ei.	Meutron Flux Lower Ion	ET-441A	13-C		en.	0	13T-4		2			
73	Meutron Flux Upper Ion	7Y-441B	13-C	**	77	n	131-4	N	*		4.84 volt	28.00
ei	Pressurizer Pressure	PY/458Q	13-8		,	1	131-6	11	13	14	36, 75 MA	2235 +
	Cold Les Temperature	TE-441B	13-8	1,2	4,3	8	131-6	6.3	7.4	and .	425.865 olves	362.70
wi.	Cold Leg Temperature	TE-440B	13-B	7,8	10,9	11	131-6	6,11	9,12	3.6	425.0°6 ohns	362.79
	Bot Leg Temperature	TZ-441A1	13-A	1,2	4,3	3	13T-5	6,3	7,4	1	447,392 ohms	816.04
*	But Les Temperature	TE-441A2	13-и	7,8	10,9	111	137-5	8,11	9,12	14	447,392 ohme	619.04
	Not Leg Yampersture	TE-441A3	13-C	60	11,10	12	131-5	20,17	21,18	13	xx olms	# 1
0	Steam Generator Level Loop 2	LT-502	13-E	**	2		131-2		11	3.	20 MA	23 +
10.	Steem Generator Level Loop 3	LT-503	13-E	•	5 0	0	131-2	20	17	13	40 88	13 +
11	RCS Wide Range Freshure	904-14	33-W		7	n	137-8	20	19	13	32 MA	1300
12.	Pressuriter Vapor Temp	TE-454	7 91	1,2	£.4	8	137-4	20,17		22	400 OBPS	499.26
13.	Residual Best Removal Fump Discharge 1emp	TE-612	13-0	œ å	11,10	12	137-4	22,25	23,26	28	300 0848	007
1	move xx - Variable STD input, set nominally	set nominally										

at -7.175 obes (615.502 Deg E) for the low resistance r'ading and 448.284 o.c. (618.261 Deg E) for the high resistance reading. See step 2.3.2 for details.

ATTACHMENT A SWC TEST CONNECTIONS

NOTE: Use two isolation networks for Bistable Partial Trip and Cabinet AC power input common and transverse mode tests. Install isolation network No. 1 to protect the test lah AC power source. Install isolation network No. 2 to protect the test station trip output conitoring device. Disconnect isolation network "line in' connection during surge application for all transverse mode tests excluding the cabinet AC power input test.

This attachment contains the following tables:

- o Table A-la Common Mode SWC Test Connections
- o Table A-1b Tranverse Mode SWC Test Connections

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			CONNECT LIN				
Channel #	I/O Description	Channel Tag #	Terminal Block		nal ection Lo	Isolator Type	I/O Board Location/ Channel #
*1.	Bistable Partial Trip, Energized	ITS/442G	13-M	1	2	Class non 1E/1E Isolation Barrier	13T-10/1
*2.	Bistable Partial Trip, Deenergized	ITS/442G	13-M	1	2	Class non 1E/1E Isolation Barrier	13T-10/1
3.	Analog Output	1PY/408A	13-N	4	5	Class non 1E/1E Isolation Barrier	13T-16/2
4.	Contact Output (No), Energized	ITY/441A	13-M	7	8	Class non 1E/1E Isclation Barrier	13T-12/2
5.	Contact Output (NC), Energized	1TY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
6.	Contact Output (No), Deenergized	TY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	13T-12/2

^{*} Disconnect function generator input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during surge application.
**Move wire terminated on 13T-12-6 to 13T-12-7 to test NC configuration.

4284N:4

TABLE A-la (Continued)

COMMON MODE SUS TEST CONNECTIONS

			CONNECT LIN	E-OUT TO			
Channel	1/0 Description	Channel Tag #	Terminal Block	Termin Connec Hi		Isolator Type	1/0 Board Location/ Channel #
7.	Contact Output (NC), Deenergized	TY/441A	13-#**	7	8	Class now 1E/1E Isolation Barrier	131-12/2
8.	WR RTD Input	ITY/612	13-D	8,9	11,10	N/A	13T-4/4
9.	NR RTD Input	ITY/441Y	13-A	7,8	10,9	N/A	13T-5/2
10.	Current Loop Input, Active***	TPY/4580	137-8	8,9	11,12	N/A	13T-8/2
1.	Current Loop Input Passive***	IPY/4580	131-8	11	12	N/A	13T-8/2
2.	Current Loop Input Active	IPY/408	13-N	1	2	N/A	13T-8/3
13.	WR RTD Input, 0-10 volt application	IMY/441A	13-C	4	5	N/A	13T-4/2
4.	Cabinet AC Power Input	N/A	13-W	11	12	N/A	N/A
5.	Contact Output (NO/NC/C), Energized	1TY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	131-12/2

^{**}Move wire terminated on 13T-12-6 to 13T-12-7 to test NC configuration.
***Active operation utilizes on-board DC power supply. Passive operation utilizes external power supply.

TABLE A-1a (Continued)
COMMON MODE SWC TEST CONNECTIONS

			CONNECT LIN	E-OUT TO			
Channel	1/0 Description	Channel Tag #	Terminal Block	Termi Conne Hi		Isolator Type	I/O Board Location/ Channel #
16.	Contact Output (NO/NC/C), Deenergized	1TY/441A	13-M	7	8	Class non IE/1 Isolation Barrier	13T-12/2
17.	WR RTD Input	TTY/454	13-0	1,2	4,3	N/A	13T-4/3
18.	NR RTD Input	ITY/441X	13-A	1,2	4,3	N/A	137-5/1
19.	Current Loop Input Active	IPY/458Q	13T-8	8	the state of	N/A	137-8/2

TABLE A-1b
TRANVERSE MODE SWC TEST CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Conn Line Hi	The state of the s	Isolator Type	I/O Board Location/ Channel #
1.	Bistable Partial Trip, Energized	TTS/442G	13-M	1	2	Class non 1E/1E Isolation Barrier	13T-10/1
*2.	Bistable Partial Trip, Deenergized	1TS/442G	13-M	1	2	Class non 1E/1E Isolation Barrier	13T-10/1
3.	Analog Output	IPY/408A	13-N	4	5	Class non 1E/1E Isolation Barrier	13T-16/2
4.	Contact Output (NO), Energized	1TY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	131-12/2
5.	Contact Output (NC), Energized	1TY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
6.	Contact Output (NG), Deenergized	ITY/441A	13-M	7	8	Class non 1E/1E	13T-12/2
7.	Contact Output (NC), Deenergized	ITY/441A	13-M**	7	8	Class non 1E/1E Isolation Earrier	13T-12/2

TABLE A-1b (Continued)
TRANVERSE MODE SWC TEST CONNECTIONS

Channel	I/O Description	Channel Tag #	Terminal Block		-Out	Isolator Type	I/O Board Location/
				Hi	Lo		Channel #
8. i	VR RTD Input	ITY/612	13-D	8	9	A/A	13T-4/4
9.	R RTD Input	ITY/612	13-D	10	11	N/A	13T-4'4
10. 1	R RTD Input	114/612	13-0	8	10	N/A	13T-4/4
11.	R RTD Input	ITY/612	13-D	8	11	N/A	13T-4/4
12.	RTD Input	ITY/612	13-D	9	10	N/A	13T-4/4
13.	R RTD Input	ITY/612	13-D	9	11	N/A	131-4/4
	Current Loop Input,	IPY/458Q	13T-8	8	11	N/A	13T-8/2
	Current Loop Input,	IPY/458Q	i3T-8	8	9	N/A	13T-8/2
	current Loop Input,	IPY/458Q	13T-8	11	12	N/A	13T-8/2
	urrent Loop Input, assive	IPY/458Q	13T-8	8	9	N/A	13T-8/2
	urrent Loop Input,	1PY/408	13-N	1	2	N/A	13T-8/3

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TABLE A-1b (Continued) TRANVERSE MODE SWC TEST CONNECTIONS

hannel	1/0 Description	Channe? Tag #	Terminal Block	Conn ine Hi	ect -Out Lo	Isolator Type	I/O Board Location/ Channel #
9.	WR RTD Input, 0-16 Volt Application	INY/441A	13-C	4	5	N/A	13T-4/2
0.	Cabinet AC Power Input	N/A	13-9	1	2	N/A	N/A
1.	Contact Output (MO/MC), Energized	ITY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
2.	Contact Output (NO/NC), Deenergized	ITY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
3.	WR RTD Input	ITY/454	13-D	2	3	N/A	13T-4/3
4.	WR RTD Input	ITY/454	13-D	1	4	N/A	13T-4/3
5.	NR RTD Input	ITY/441X	13-A	2	3	H/A	137-5/1
б.	NR RTD Input	1TY/441X	13-A	1	4	N/A	13T-5/1
7.	NR RTD Input	ITY/441Y	13-A	9	10	N/A	13T-5/2
8.	NR RTD Input	ITY/441Y	13-A	8	11	N/A	13T-5/2

ATTACHMENT B FIELD CONNECTIONS AND SIMULATION

See test procedure JPD-111687-0 figures B-3 through B-9 for input simulation and input/output monitoring connections.

Cabinet Configuration Information:

The cabinet under test, Qualification Unit 2, is an exact replica of Watts Bar Nuclear Power Station Protection Rack 13. The following drawings document the cabinet configuration. Copies of these drawings will be included as part of the final test report.

Drawing Description	Drawing Number/Rev.
Terminal Block Wiring Diagram, Protection Set 4	1-47043 PW-13, rev. 3E
Process Control Clock Diagram, Delta T/TAVG System	1080408 sh. 10, rev. 11
Process Control Block Diagram, W.R. S.G. Level	108D408 sh. 34, rev. 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temp.	108D408 sh. 38, rev. 4
Process Control Block Diagram, RHR Pump Discharge Temp	108D408 sh. 39, rev. 5
Process Control Block Diagram, RCS Wide Kange Pressure	108D408 sh. 43, rev. 1
Eagle-21 Schematic Diagrams, Rack 13 Protection Set 4	1856E69 sh. 2, rev. 2

ATTACHMENT C TRANSIENT DATA RECORDING SYSTEM CONNECTIONS

This attachment contains the following:

- o Table C-1 Tape Recorded Data
- o Table C-2 Data Logger Recorded Data
- o Table C-3 Strip Chart Recorded Data

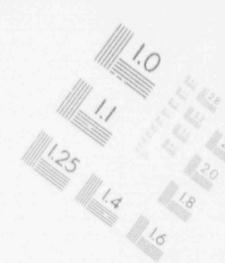
TABLE C-1 TAPE RECORDED DATA

Channel	Recorded Signal	Tag #	Terminal Block		ermina onnect Lo		Buffer Amplifier Gain
1.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
2.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
3.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
4.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
5.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
6.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
7.	Contact Output	ITY/441	13-M	5	6		.02
Α.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
9.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
10.	Analog Input I/E	IPY/458Q	*				10
11.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
12.	Analog Input I/E	IPY/408	*				20
13.	Analog Output E/I	1PY/408B	13-N	7	8	9	10
14.	Function Generator Sig	. N/A	**				.05

^{*}Measure current across 20 ohm transmitter test resistor. See figure B-4.

^{**}Monitor function generator output signal. See figure B-3.

IMAGE EVALUATION TEST TARGET (MT-3)





150mm

91 STATE OF

IMAGE EVALUATION TEST TARGET (MT-3)



150mm



91 STILL STI

IMAGE EVALUATION TEST TARGET (MT-3)





150mm •

91 81 SZIIII

	TAB	TE C-5	
DATA	LOGGER	RECORDED	DATA

Channel	Recorded Signal	Tag	Terminal Block	Cor	minal	on
				Hi	Lo	Sh
6.	Analog Input E/E	INY/4418	13-C	1	2	3
7.	Analog Input E/E	INY/441A	13-C	4	5	6
9.	Contact Output	ITY/441	13-M	5	6	
10.	Contact Output	ITY/441A	13-M	7	8	
22.	Analog Output E/I	1TY/441L	13-P	10	11	12
23.	Analog Output E/I	ITY/454A	13-G	4	5	6
24.	Analog Output E/I	ITY/441K	13-P	7	8	9
25.	Analog Output E/I	ILY/5028	13-K	1	4	5
26.	Analog Output E/I	IPY/408B	13-K	7	8	11
27.	Analog Output E/I	ILY/5038	13-K	7	10	11
35	Analog Input I/E	IPY/458Q	*			
36	Analog Input I/E	ILY/502	*			
37	Analog Input I/E	1L*/503	*			
38	Analog Input I/E	IPY/408	*			

^{*}Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE C-3 STRIP CHART RECORDED

Channel	Recorded Signal	Tag	Terminal Block		ermina onnect Lo		Buffer*** Amplifier Gain
1.	Function Generator Sig.	N/A	**	-		*****	Λ.Γ
2.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
3.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
4.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
5.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
6.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
7.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
9.	Contact Output	ITY/441	13-M	5	6		.02
10.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
11.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
12.	Analog Input I/E	IPY/458Q	*		10	11	
13.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
14.	Analog Input I/E	IPY/408	*			3	10
15.	Analog Output E/I	IPY/408B	13-N	7	8	9	20
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

^{**} Monitor function generator output signal. See figure B-3.

^{***} Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

JPD 111587-3

DATE 11/16/87 REVISION NO.

RADIO FREQUENCY INTERFERENCE TEST PROCEDURE

FOR

EAGLE-21 PROTECTION

SYSTEM

1.0 INTRODUCTION

This procedure details the Radio Frequency Interference (RFI) tests performed on the Eagle-21 protection system.

These tests will consist of exposing the Eagle-21 protection system to a known electromagnetic field and measuring the affects on system input/output processing. Tests are to be conducted per the intent of SAMA standard PMC 33.1-1978, Class 1 and 2, bands a,b and c.

The test configuration is documented in Attachments A and B.

2.0 PREPARATION FOR TEST

2.1 Locate the Eagle-21 cabinet in the anechoic chamber. Position the cabinet such that the cabinet is 1 meter from the transmitting antenna and the center of the microprocessor card cage is 59-1/2 inches from the anechoic chamber floor.

Connect the cabinet bus bar to the test facility ground plane via a short bonding cable.

- 2.2 Connect the field cabling to sensor simulation, load simulation, and contact output loads per Attachments B and Table 1-1. Input/output signal cabling shall be run in exposed vashielded cable trays.
- 2.3 Obtain system baseline data:
 - 2.3.1 System baseline data will be taken to verify system operation. Input voltage and current and resistance values corresponding to 0 100% of scale in 25% increments and record. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.

2.3.2 Set signal inputs per table 1-1. Adjust analog input signals, using the MMI to obtain the expected engineering unit values specified in table 1-1. Using figure B-6 in Noise Test Procedure JPD-111687-0 as a reference, adjust the variable RTD channel per the following procedure: Open the manual switch input to the variable RTO board. Adjust the high adjust potentiometer so that channel 0 TE-441A3 reads 618.261+/-.375 Deg f on the MMI. Verify that the TAVG MMI reading equals 589.740 + .2 Deg f. Verify the following actual bistable output status: is/4410 = Not Tripped TS/441G = Not Tripped (S/441D = Not Tripped TS/441H = Not Tripped TS/442D = Tripped TS/442G = Tripped Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens. Close the manual switch input to the variable RTD board. o Adjust the low adjust potentiometer so that channel TE-441A3 reads 615.501+/-.375 Deg f on the MMI. Verify that the Delta T MMI reading equals 104.237-.3PU. Verify the following actual bistable output status: TS/1441C = Tripped TS/1441G = Tripped TS/1441D = Tripped 0-113 4274N:4

TS/1442D - Not Tripped TS/1442G - Not Tripped Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens. Open the manual switch input to the variable RTD board and record the results. Obtain MMI printout of analog input information ar record analog input/outgut readings via data logger printout. 2.3.3 Using the []b.c Control Computer request a baseline test run of at least 5 data points. Verify that the trip output signals switch upon receipt of the control relay switch signal. 3.0 RFI MODULATION TEST PROCEDURE SEQUENCE The RFI test sequence described below will be followed for each frequency test run specified in Sections 4.0 through 6.0. See figure 1-1 for a modulation test block diagram. 3.1 Pretest Obtain a data logger printout of "normal" analog input/output and digital output values. 3.2 Disconnect data logger and verify "antenna" connections and configuration for each frequency run as specified in sections 4.0 through 6.0. 3.3 Initiate a modulation test run via the $[]_{b,c}$ control computer. Enter configuration data as prompted by the control computer. Configuration data is specified in sections 4.0 through 6.0 for each C-114 4274N:4

TS/1441H - Tripped

test run. Ready the [] $_{b,c}$ Control Computer by entering the calibration file name for the appropriate frequency test run as specification in sections 4.0 through 6.0. Enter the identifying records in the tape recorder log. Simultaneously enter the test run start command via the [] $_{b,c}$ control computer and start the tape recorder. The frequency test run will automatically execute until completion without operator intervention. Upon completion of the frequency test run stop the tape recorder and record the ending tape footage.

- 3.4 Review the strip chart recorder printouts and the control computer data sheets and record any analog output signal deviation and/or trip output status failures. Using the MMI investigate any input/output signal processing anamolies to determine cause.
- 3.5 If significant abnormal system performance is measured, calibration file information for the affected frequency should be examined. If the drive signal for the RF signal generator at the affected frequencies is significantly higher than the adjacent frequency signal levels, repeat the affected frequency test at a signal level consistent with adjacent frequencies.
- 3.6 Obtain a data logger printout and confirm system recovery by comparing to pretest data. Record any discrepancies.
- 3.7 With the system confirmed to be in the pretest condition, proceed to the next test.

4.0 20-160 MHZ FREQUENCY RUN

4.1 Mount the beconical antenna to the antenna tripod/coupler assembly. Ensure that the antenna center-line is 59-1/2 inches from the anechoic chamber floor and 1 meter from the Eagle-21 cabinet.

Connect the [] b,c power amplifier to the antenna coupler assembly input.

4.2 Follow the test sequence described in Section 3 for each frequency run specified below:

	Antenna	Calibration
Field Strength	Polarization	File
2/=	Vont	104A
3 V/M	Morz	101A
3 v/m	Vert	104A
3 v/m	Horz	101A
3 V/m	Vert	104A
3 v/m	Horz	101A
10 v/m	Horz	102A
10 v/m	Vert	105A
10 v/m	Horz	102A
10 v/m	Vert	105A
10 v/m	Vert	105A
10 v/m	Horz	102A
	3 v/m 3 v/m 3 v/m 3 v/m 3 v/m 3 v/m 10 v/m 10 v/m 10 v/m 10 v/m 10 v/m	Field Strength Polarization 3 v/m Vert 3 v/m Horz 3 v/m Horz 3 v/m Vert 3 v/m Horz 10 v/m Horz 10 v/m Vert 10 v/m Vert

5.0 160-500 MHZ FREQUENCY RUN

- 5.1 Mount the log periodic antenna to the antenna tripod/coupler assembly. Ensure that the antenna center-line is 59-1/2 inches from the anechoic chamber floor and 1 meter from the Eagle-21 cabinet. Connect the [$]_{b,c}$ power amplifier to the antenna coupler assembly input.
- 5.2 Follow the test sequence described in Section 3 for each frequency run specified below:

Cabinet Position	Fiela Strength	Antenna Polarization	Calibration File
Front	3 v/m	Vert	204A
Front	3 v/m	Horz	201A
Rear	3 v/m	Vert	204A
Rear	3 v/m	Horz	201A

Left side	3 v/m	Horz	201A
Right side	3 v/m	Vert	204A
Front	10 v/m	Horz	202A
Front	10 v/m	Vert	205A
Rear	10 v/m	Horz	202A
Rear	10 v/m	Vert	205A
Left side	10 v/m	Horz	202A
Right side	10 v/m	Vert	205A

6.0 160-500 MHZ FREQUENCY RUN

- 6.1 Mount the log periodic antenna to the antenna tripod/coupler assembly. Ensure that the antenna center-line is 59-1/2 inches from the anechoic chamber floor and I meter from the Eagle-21 cabinet. Connect the [$_{\rm b,c}$ power amplifier to the antenna coupler assmebly input.
- 6.2 Follow the test sequence discribed in Section 3 for each frequency run specified below:

			Antenna	Calibration
Cabinet Position	Field	Strength	Polarization	<u>File</u>
Front	3	V/m	Vert	304A
Front		v/m	Horz	301A
Rear	3	v/m	Vert	304A
Rear	3	v/m	lorz	301A
Left side	3	v/m	Horz	301A
Right side	3	v/m	Vert	304A
Front	10	v/m	Horz	302A
Fron*	10	v/m	Vert	305A
Rear	10	v/m	Horz	302A
Rear	10	v/m	Vert	305A
Left side	10	v/m	Horz	302A
Right side	10	v/m	Vert	305A

7.0 KEYING TESTS

The keying tests will be performed exposing the most susceptable side of the equipment as determined from the modulation tests. At least three frequency data points per octave must be chosen.

Frequencies which generated input/output processing anamolies during the modulation test should be chosen. If no anamolies occurred over a given octave frequency data points should be evenly spaced. Follow the test sequence below for each keying frequency data point. See figure 1-2 for a keying test block diagram.

- 7.1 Obtain a data logger printout of "normal" analog input/output and digital output valves.
- 7.2 Disconnect the data logger and verify proper "antenna" connections for the data point chosen.
- 7.3 Initiate a keying test run via the [] $_{b,c}$ Control Computer. Enter configuration data as prompted by the control computer. Manually enter the frequency and amplitude into the RF signal generator using appropriate calibration file information. Manually start the strip chart recorders, the tape recorder and trigger the IBM control computer. The [] $_{b,c}$ Control Computer will then automatically execute the keying test. Repeat the above sequence for each selected keying test data point.

Note: Follow the guidelines as stated for the modulation test in step 3.5.

(See figure 5-17 of WCAP test report)

Figure 1-1 Block Diagram of Radio Frequency
Interference Modulation Tests

(See figure 5-18 of WCAP test report)

Figure 1-2 Block Diagram of Radio Frequency Interference Keying Tests

8.0 ACCEPTANCE CRITERIA

8.1 Description

The acceptance criteria for the Eagle 21 (IE Safety Related System) is that the system shall remain operational while exposed to radio frequency interference and demonstrate recovery upon removal of radio frequency interference.

TABLE 1-1 SIMPLATED IMPUT SIGNAL

President Fluid Private Privat		Charmel	Charmel 7ag #	Termine! Block	ä	Terminal Connection Lo	fs.	I/O Board Location	i	I/O Board Commetion Lo	£.	Simulator Signel	Expected Signs in E.U.
Newton Flux No. 4418 13-5 15 15 15 15 15 15 15													4 00 4
Section Float Fig. 4818 13-C	**	Heutron Flux	ET-441A	L) M	*		w.	137-4	0	13		00.6	
Presentiant Freshure Friedholm 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 13-16 1	es	Meutice Finx	HY-441B	13-C	**		n	137-4	N	10		4.64 volt	28.02 + .083
Cold Leg Temperature TE-441B 13-9 1,2 4,3 5 13T-7 6,3 7,4 1 422 860 others Cold Leg Temperature TE-441B 13-8 1,2 4,3 5 13T-5 6,11 8,12 14 4,2 860 others Cold Leg Temperature TE-441B 13-8 1,2 4,3 5 13T-5 6,11 8,12 14 4,2 860 others Stock Leg Temperature TE-441B 13-6 13-6 1,0 1,1 1,1 1,1 1,1 1,1 1,1 1,1 1,1 1,1		Prassiries Prassirs	. PY/458Q	13-H	1			137-8	11	12	2.6	36.75 MA	2235 ± 1.00
Cold Leg Temperature TE-44161 13-8 1,8 10,9 11 13T-6 6,11 9,12 14 422,866 ohems		Cold Lag Jamperature	TE-441B	13-9	1,2		*	131-4	6,3	7.4	M	425,866 obms	562.70 ± .37
Stot Leg Temperature		Cold Leg Temperature	TE-440B	13-8	7,8		20.00	137-6	8,11	9,12	1.4	425.866 ohms	362.70 ± .37
Steel Leag Temperature	8	Sot Leg Temperature	TE-44161	13-A	1,2		*1	137-5	6,3	7,4	gel	447.392 obms	016.041 2.3
State Constitute TE-441A3 13-C 8.8 11,10 12 137-5 20,17 21,18 15 22 DMA		Sot Leg Temperature	TE-441A2	13-A	7,8		11	137-5	8,11	9,12	2.6	447,392 obms	616.041 + 3
Steen Generator LT-502 13-E 2 3 13T-2 6 11 13 40 MM	10	Not Les Temperature	TE-441A3	13-C	0,0		12	137-5	20,17	21,18	13	zz ohms	24 4 1265
Steem Generator LT-503 13-E		Steam Ganerator Lavel Loop 2	1.1-502	13-E	**			137-2	0	11			
pot TE-456 13-W 1 2 3 13T-6 20 18 35 MATMA 13-0	10.	Steem Generator Level Loop 3	1.1-503	13-2	*		10	131-2	20	n	12	40 PM	87 5 4 0001
Presentiser Vapot Tenap Temp Temp Residual Best Removel TE-612 13-D 8.9 11,10 12 13T-4 20,27 23,28 23 309 OMPR Residual Best Removel TE-612 13-D 8.9 11,10 12 13T-4 22,25 23,28 28 309 OMPR - x x - Variable RTD input, set nominally at 445.284 obes low resistance res	*1	RCS Wide Renga Pressure	PT-408	13-8	**		n	131-6	20		n :	ACO COMPC	ASS 266 + 1
Residual Best Removel 1E-612 13-D 8.9 11,10 12 13T** 22,25 23,26 28 300 OMPES Pump Discharge Temp - XX - Variable RID input, set nominally at 447 175 ohms (613.502 Deg f) for the lost the lost temistance resistance resi	64	Pressurizer Vapor Temp	IE-454	13-0	1,2	4,3	en.	137-4	20,17		9		1 400
	rs.	Residual Beat Removel. Pump Discharge Temp	18-612	13-D	8.0		12	137-4	22,25	23,26	28	300 0848	100
	OTE		ut, set nominally 502 Deg f) for the g and 448.284 obes to high resistance 3.2 for details.										

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RADIO FREQUENCY INTERFERENCE TEST DATA

TARGET: (CABINET POSITION) CALIBRATION FILE: FIELD STRENGTH LEVEL: (V/m) TYPE OF ANTENNA: (LOG PERIODIC OR BICONICAL) ANTENNA POLARIZATION: (HORIZONTAL OR VERTICAL) DATE: TEST PERFORMED BY: __ REVIEWED BY: TAPE NAME: TAPE SET: TAPE RECORDER START AT: (FOOT) FREQUENCY: (MHZ) (DATE) (TIME) EVENT DIG/INPUT 00 0011 (EXPECTED TRIP OUTPUT PATTERN) 11 1100 3 00 0011 REMARKS: FREQUENCY: (MHZ) (DATE) (TIME) DIG/INPUT EVENT 00 0011 11 1100 3 00 0011 REMARKS: FREQUENCY: (MHZ) (DATE) (TIME) ERROR IN THE CHANGING CONDITION OF BISTABLE STATUS (TRIP OUTPUT ERROR MESSAGE) EVENT DIG/INPUT 00 0011 11 1101 00 0011 REMARKS:

ENDING TAPE RECORDER FOOTAGE FOR THIS SET OF DATA: (FOOT)

Figure 1-3. RFI Modulation Test Data Sheet

RADIO FREQUENCY INTERFERENCE TEST DATA

TARGET: (CABINET POSITION) FIELD STRENGTH LEVEL: (V/M) TYPE OF ANTENNA: (LOG PERIODIC OR BICONICAL) ANTENNA POLARIZATION: (HORIZONTAL OR VERTICAL) DATE: TEST PERFORMED BY: _ REVIEWED BY: TAPE NAME: TAPE SET: TAPE RECORDER START AT: (FOOT) FREQUENCY: (MHZ) (DATE) (TIME) (FIRST KEY CYCLE) (SECOND KEY CYCLE)
DIG [K-OFF] INPUT DIG [K-ON] INPUT EVENT DIG [K-ON] INPUT (EXPECTED TRIP 00 0011 00 0011 OUTPUT PATTERNS) 2 11 1100 11 1100 REMARKS: FREQUENCY: (MHZ) (DATE) (TIME) EVENT DIG [K-OFF] INPUT DIG [K-ON] INPUT 00 0011 00 0011 11 1100 2 11 1100 REMARKS: FREQUENCY: (MHZ) (DATE) (TIME) DIG [K-OFF] INPUT 00 00]1 EVENT DIG [K-ON] INPUT 00 0011 2 11 1100 11 1100 REMARKS: ENDING TAPE RECORDER FOOTAGE FOR THIS SET OF DATA: (FOOT) Figure 1-4. RFI Keying Test Data Sheet

ATTACHMENT A FIELD CONNECTIONS AND SIMULATION

This attachment contains the following figures:

o Figure A-1 Control Computer(s)/Test Station Connections

See test procedure JPD-111687-0 figures B-4 through B-9 for input simulation and input/output monitoring connections.

Cabinet Configuration Information:

The cabinet under test, Mullification Unit 2, is an exact replica of Watts Bar Nuclear Power Station Protection Rack 13. The following drawings document the cabinet configuration. Copies of these drawings will be included as part of the final test report.

Drawing Description	Drawing	Number/Rev.
Terminal Block Wiring Diagram, Protection Set 4	1-47043	PW-13, rev. 3E
Process Control Block Diagram, Delta T/T _{AVG} System	1080408	sh. 10, rev. 11
Process Control Block Diagram, W.R. S.G. Level	1080408	sh. 34, rev. 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temp.	1080408	sh. 38, rev. 4
Process Control Block Diagram, RHR Pump Discharge Temp	108D408	sh. 39, rev. 5

Process Control Block Diagram, 108D408 sh. 43, rev. 1 RCS Wide Range Pressure

Eagle-21 Schematic Diagrams, 1856E69 sh. 2, rev. 2 Rack 13 Protection Set 4

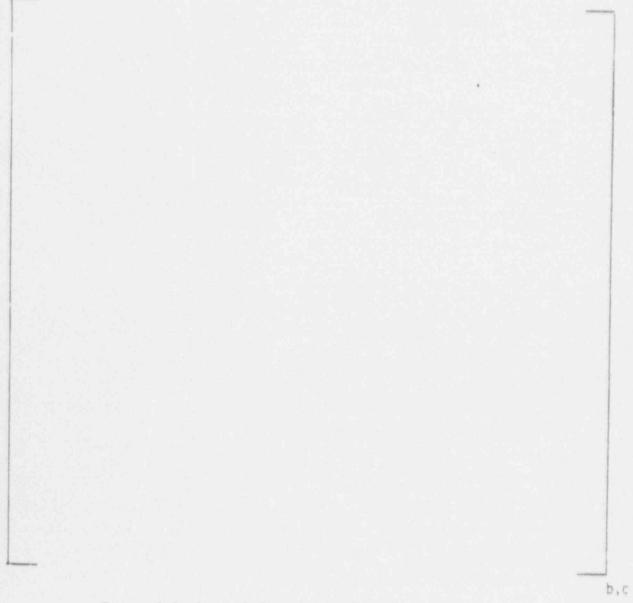


Figure A-1 Control Computer(s)/Test Station Connections

ATTACHMENT B TRANSIENT DATA RECORDING SYSTEM CONNECTIONS

This attachment contains the following:

- o Table B-1 Tape Recorded Data
- o Table B-2 Data Logger Recorded Data
- o Table 6-3 Strip Chart Recorded Data

TABLE B-1 TAPE RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block		ermina onnect Lo		Buffer Amplifier Gain
1.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
2.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
3.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
4.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
5.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
6.	Bistable Partial Trip	1TS/441G	13-L	5	6		.05
7.	Contact Output	ITY/441	13-M	5	6		.02
8.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
9.	Analog Output E/I	1TY/441L	13-K	7	10	11	10
10.	Analog Input I/E	IPY/458Q	*				10
11.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
12.	Analog Input I/E	IPY/408	*				20
13.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
14.	Function Generator Sig.	N/A	**				.05

^{*}Measure current across 20 ohm transmitter test resistor. See figure 8-4.

^{**}Monitor function generator output signal. See figure B-3.

TABLE B-2 DATA LOGGER RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block	Cor	minal necti Lo	on
6.	Analog Input E/E	INY/441B	13-C	1	2	3
7.	Analog Input E/E	INY/441A	13-C	4	5	6
9.	Contact Output	ITY/441	13-M	5	6	
10.	Contact Output	ITY/441A	13-M	7	8	
22.	Analog Output 2/1	ITY/441L	13-P	10	11	12
23.	Analog Output E/1	ITY/454A	13-G	4	5	6
24.	Analog Output E/I	ITY/441K	13-P	7	8	9
25.	Analog Output E/I	ILY/502B	13-K	1	4	5
26.	Analog Output E/I	IPY/408B	13-N	7	8	11
27.	Analog Output E/I	ILY/503B	13-K	7	10	11
35	Analog Input I/E	IPY/458Q	*			
36	Analog Input I/E	1LY/502	*			
37	Analog Input I/E	ILY/503	*			
38	Analog Input 1/E	IPY/408	*			

^{*}Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE B-3 STRIP CHART RECORDED

Channel #	Recorded Signal	Tag #	Terminal Block		ermina onnect Lo		Buffer*** Amplifier Gain
1.	Function Generator Sig.	N/A	**				.05
2.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
3.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
4.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
5.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
6.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
7.	Bistable Partial Trip	1TS/441G	13-L	5	6		.05
8.	Analog Input E/E	INY/441B	13-C	4	2	3	2.0
8a.	Keying Signal	N/A	****				.05
9.	Contact Output	ITY/441	13-M	5	6		.02
10.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
11.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
12.	Analog Input I/E	IPY/4580					10
13.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
14.	Analog Input I/E	IPY/408	*				20
15.	Analog Output E/1	IPY/4088	13-N	7	8	9	10
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

^{*} Measure current across 20 ohm transmitter test resistor. See figure B-4.

^{**} Monitor function generator output signal. See figure B-3.

^{***} Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

^{****} Monitor analog input INY/441B for modulation tests. Monitor control signal to keying relay for keying tests.

APPENDIX D TEST EQUIPMENT LIST

Table D-1 describes the test equipment.

TABLE D-1 TEST EQUIPMEN: LIST

D, C

TABLE D-1 TEST EQUIPMENT LIST

b,c

TABLE D-1 TEST EQ! SMENT LIST

__ b,c

TABLE D-1 TEST EQUIPMENT LIST

b,c