UNITED STATES
NUCLEAR REGULATORY COMMISSION
WASHINGTON, D. C. 20555

MAR 9 1983

APPLICANT: Illinois Power Company

FACILITY: Clinton Power Station, Unit 1

SUBJECT: MEETING SUMMARY - CLINTON, UNIT 1 NUCLEAR SYSTEM PROTECTION SYSTEM (NSPS) SELF TEST CAPABILITY (JANUARY 11 and 12, 1983)

On January 11th and 12th, 1983, a meeting was held at the General Electric Co. offices in Bethesda, Md. to provide the staff design details of the automatic testing system used to test protection system circuitry at Clinton, Unit 1. This automatic testing system (called the "Self Test System", STS) continuously monitors the Nuclear System Protection System (NSPS) for faults. The NSPS circuitry receives inputs from sensors monitoring plant parameters and actuates plant safety systems automatically if associated coincidence logic is satisfied. The NSPS consists of four independent and redundant divisions that include protection system circuitry comprised of CMPS (complementary metal oxide semiconductor) and other solid state logic elements arranged on replaceable printed circuit (PC) cards located in the main control room. The safety systems actuated by the NSPS are: Reactor Protection System (RPS), Nuclear Steam Supply Shutoff System (NS^4), Automatic Depressurization System (ADS), High Pressure Core Spray System (HPCS), Low Pressure Core Spray System (LPCS), Residual Heat Removal System (RHR), and the Reactor Core Isolation Cooling System (RCIC).

The meeting started with an overview of the NSPS. This presentation was given previousiy in greater detail on July 21 and 22, 1981 at the G. E. offices in Bethesda during the Clinton OL review. The presentation was repeated here for the benefit of staff GESSAR reviewers and as background for the STS presentation. The GESSAR and Clinton designs both include the NSPS and STS. Copies of the slides used for the NSPS overview are provided in Attachment 1.

MEMO DATED: MAR 9 1983

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Following the NSPS overview, G.E. gave a presentation explaining the operation of the STS. Copies of the slides used for this STS presentation are provided in Attachment 2. During the presentation, G.E. answered numerous questions from the staff. A drawing review of various NSPS circuit cards (RPS logic cards, digital signal conditioners, and high power isolator cards) was performed. STS/NSPS interfaces were identified and STS circuits traced to the staff's satisfaction.

On the second day of the meeting, Illinois Power Company explained how they intend to use the STS to satisfy various Technical Specification surveillance testing requirements on the NSPS circuitry. Each of the tests to be performed by the STS, the extent of these tests, and their limitations were discussed. Copies of the slides used for this presentation are provided in Attachment 3. The plant unique Technical Specification surveillance requirements for the Clinton NSPS were not discussed. It was agreed that this would be the topic of a future meeting.

Following is a list of observations made during this two day meeting:

1) Each NSPS component (analog trip module (ATM), digital signal conditioner (DSC), optical isolator (OI), Load Driver, logic card, etc.) is dedicated to one division only.

2) ATM inputs are 4-20mA signals from transmitters. The ATMs have a "live zero" (i.e., upon loss of power, the ATM will fail offscale; the 4-20mA signal must be present to have a zero indication).

3) The STS must be operable to test the logic portion of the NSPS. There are no provisions in the NSPS design for manual testing of the NSPS logic. Drawings must be checked to determine whether the load drivers can be tested manually (i.e., does manual initiation (e.g., in service inspection or in service testing) exercise the load drivers?). The ATM instrument channels can be tested manually.

4) Plant Personnel can interface with the STS through the plant computer via a diagnostic terminal. This allows technicians to quickly isolate a fault detected by the STS to the PC card level for replacement with a spare card. The STS is designed to be completely functional independent of the plant computer. A faulted PC card, however, cannot be easily identified, independent of the plant computer. The division and system containing the faulted card can be identified from NSPS front panel indications.

5) Each of the four NSPS cabinets (one cabinet associated with each of the four class 1E powered NSPS divisions) contains its own STS. Each STS tests the NSPS circuitry within its cabinet (from ATM input through load driver) and verifies proper inputs from the remaining three NSPS cabinets. Each STS in turn becomes the master test unit with the other three STS units acting as slaves responding to commands from the master unit. It takes a STS (acting as the master unit) roughly 15 minutes to perform its testing function before passing control on to the next STS (to act as the master unit). Thus, all four NSPS divisions are tested roughly in an hours time.

6) Each path between NSPS cabinets used for communication between STSs contains optical isolation devices. These are the same optical isolation devices (one inch quartz rods) located in the 3 isolation bays in each of the 4 NSPS cabinets to isolate protective signals (prior to that signal leaving its divisional NSPS cabinet and then being routed in metal raceways associated with the divisional NSPS cabinet to which it enters) between redundant divisions. These isolation devices are similar to those used at Grand Gulf and approved during that OL review. Some of the devices used at Clinton are higher speed devices which have undergone the same qualification and fault testing. Further documentation regarding the isolation devices is being requested.

7) The STSs were installed in the NSPS cabinets during the seismic and environmental qualification testing of the NSPS cabinets. Following these tests, the STS was verified to be operable (i.e., functioned properly after the tests).

8) The NSPS is comprised of approximately 1700 PC cards (including STS cards).

9) A concern was raised about that portion of NSPS circuitry common to both the automatic and manual scram functions (this circuitry consists of several logic gates used to make up the 1-out-of-2 taken twice logic for the scram solenoids of the four rod groups - it is downstream of the 2-out-of-4 trip logic). It was suggested that another means of accomplishing a manual scram from the control room, which is independent of the automatic scram circuitry, should be provided.

10) There are four annunciator points on the main control board (one associated with each NSPS division) which are activated when their associated STS detects a fault within itself or its associated NSPS circuitry. The annunciator cannot be cleared until the fault has been removed.

11) Illinois Power will request staff approval for use of the STS to perform various surveillance testing. This includes channel checks (this is accomplished by using the STS "monitor compare function" which calls up all four transmitter outputs (ATM inputs) for a selected parameter and displays them side by side for comparison). A channel check can be performed at any of the four NSPS cabinets (each NSPS cabinet has this display). This type of channel check does not verify operability of the vertical indicators on the ECCS benchboard or the nuclenet CRT displays, on the principal plant console, provided from the plant computer.

12) The STS can be used to perform channel calibrations. Each of the four STSs contains circuitry which can determine the exact trip setpoints of its divisionally associated ATMs by ramping a current signal (0 to 50 mA) into the ATM input and displaying the value at which the ATM trips. Sensors must be calibrated separately. This ATM calibration function can be accomplished manually independent of the STS.

13) The STS can be used to perform channel functional tests. These tests (as defined by Illinois Power) verify that each ATM is operable (i.e., will trip on an increasing or decreasing trip signal - whichever applies) but will not test the exact trip setpoint as is done during calibration - explained in Item 12 above. These channel functional tests can also be performed independent of the STS. The STS tests are too fast to activate the associated control room annunciators. The operability of the annunciators (and computer printout) will be verified separately as part of the channel functional test.

14) Logic (divisional trip) channels can only be tested by the STS as discussed in Item 3 above.

15) The STS can be used for response time testing of the NSPS circuitry from the ATMs to the load drivers (i.e., tests everything except the response times of the sensor and the actuated equipment). The STS will not indicate the actual response time of the circuitry, but can be used to show that the response time is less than a defined interval ($\sim$1 msec).

16) The tests performed by the STS (channel functional test, logic test, etc.) are overlapping such that the entire NSPS is tested.

17) Illinois Power indicated that the Clinton STS software was designed to the same engineering operating procedures (EOPs) used to develop the software engineering manual which standardizes G.E.'s approach to software verification. The staff will require that the applicant submit the software "verification and validation" program for staff review.

18) The STS stops its test sequence upon detection of a fault. Once the fault has been cleared, the STS test sequence is manually restarted via the diagnostic terminal through the plant computer. If not manually restarted, the STS test sequence will automatically begin after 30 minutes. The test sequence can be manually started downstream of an existing fault.

19) The STS within a given division (when testing that division) serially loads test data (taken from ROM) into shift registers located on the various PC cards within its division, and signals the other three (slave) STSs to similarly load test data to be used as inputs (from the "slave divisions" to the "master division" during the test). This test data is then strobed in parallel from the shift registers to the NSPS functional circuitry on a 1 msec pulse. A read pulse (a shorter duration 50 μsec pulse applied within the 1 msec test pulse interval) is then used to strobe output data from the NSPS functional circuits in parallel into another set of shift registers. This output data is then serially removed from the shift registers for comparison to data stored in ROM corresponding to the expected output. Any inconsistencies between the data detected by the STS is annunciated as a fault.

20) STS gating circuits allow the 1 msec test pulse to momentarily disable (steal time from) the NSPS functional logic inputs and to strobe test data thru the functional logic in their place. The 1 msec pulse is generated from a STS timer. The gating circuitry (Resistor/Capacitor circuits) automatically reconnects the NSPS functional inputs independent of the test pulse duration. Therefore, a failure within the test pulse timing circuits will not prevent proper functioning of the NSPS.

21) The staff noted that it does not appear that the failure of certain components (e.g., shorted capacitors) within the STS gating circuits can be detected. A concern was raised that if over a long period of time a number of these failures occurred, that the operation of the NSPS circuits could possibly be affected. This item will be pursued with the applicant.

22) The capability exists to detect proper operation of the load drivers within the NSPS via STS current sense circuits used to detect current flow in the output circuits, or the interruption of current flow (depending on whether "energize-to-actuate" or "de-energize-to-actuate" logic is used).

23) All load driver output circuits are provided with overvoltage transient suppression (field effect transistors- FETs, and metal oxide varistors- MOVs) devices for protection.

In conclusion, the staff noted that the STS used to automatically test the Clinton solid state NSPS circuitry offers several advantages over conventional surveillance testing methods. Among these, the circuitry is continually being checked as opposed to once per month or less. The applicant hopes that this will reduce the time to detection of failed components and lead to increased plant availability as well as increased protection system availability. Another significant advantage of the STS is that the test circuitry is hard wired in place such that temporary modifications to the NSPS functional circuitry during testing (e.g., bypassing channels, connecting and disconnecting test leads and other test equipment within protection system cabinets, etc.) is not necessary. This eliminates the potential for not returning functional circuits to their normal operating mode following system testing.

The staff indicated to Illinois Power Company and G. E. that the STS would probably be approved for surveillance testing to fulfill Technical Specification requirements at Clinton. The staff noted that there would be Technical Specification requirements on the STS itself. The staff intends to approve the STS design following the documentation (the applicant indicated that this would be in the form of an FSAR amendment) of several key items brought out during the meeting. A list of these items is provided in Attachment 4. In addition, acceptable responses to several staff concerns not resolved during the meeting must also be provided by the applicant. These concerns are not considered to be major, and we anticipate that the applicant will respond to these acceptably in the near future. These items are also listed in Attachment 4.

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Original signed by:

R. Kendall, Instrumentation &
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Attachments:
As stated

cc: See next page

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ATTACHMENT 1

CLINTON / GESSAR

NUCLEAR SYSTEM PROTECTION SYSTEM

(NSPS)

REVIEW

NSPS PRESENTATION

PURPOSE: TO SUPPLEMENT THE FORMAL LICENSING SUBMITTALS WITH EXPLANATIONS OF THE CLINTON DESIGN

SCOPE: A SYSTEM HARDWARE OVERVIEW OF NSPS WITH LOWER LEVEL DISCUSSION WHERE REQUESTED

FORMAT: A 3 PART PRESENTATION DIVIDED INTO

- o SYSTEM OVERVIEW (FUNCTIONAL)
- o HARDWARE IMPLEMENTATION
- o LICENSING VIEWPOINT OF NSPS

NSPS - HISTORY

- BWR-1, 2, 3, 4, 5, 6

- ANALOG TRIP SYSTEM - SOME BWR-4, 5.
  ALL DOMESTIC BWR-6

- SOLID STATE LOGIC - CLINTON
  - STANDARD GW OFFERING

NSPS - THE BEGINNINGS

- RAPID FAULT DETECTION AND REPAIR TIME TO REDUCE DOWNTIME

- SEMICONDUCTOR DEVICES HAD EMERGED AS RELIABLE AND AVAILABLE. PROVEN BY YEARS OF APPLICATION.

- IMPROVED LOGIC AND ENHANCED TESTABILITY; IMPROVED PROBABILITY TO PERFORM SAFETY FUNCTION WHEN REQUIRED.

- REDUCED POWER CONSUMPTION, SPACE REQUIREMENTS.

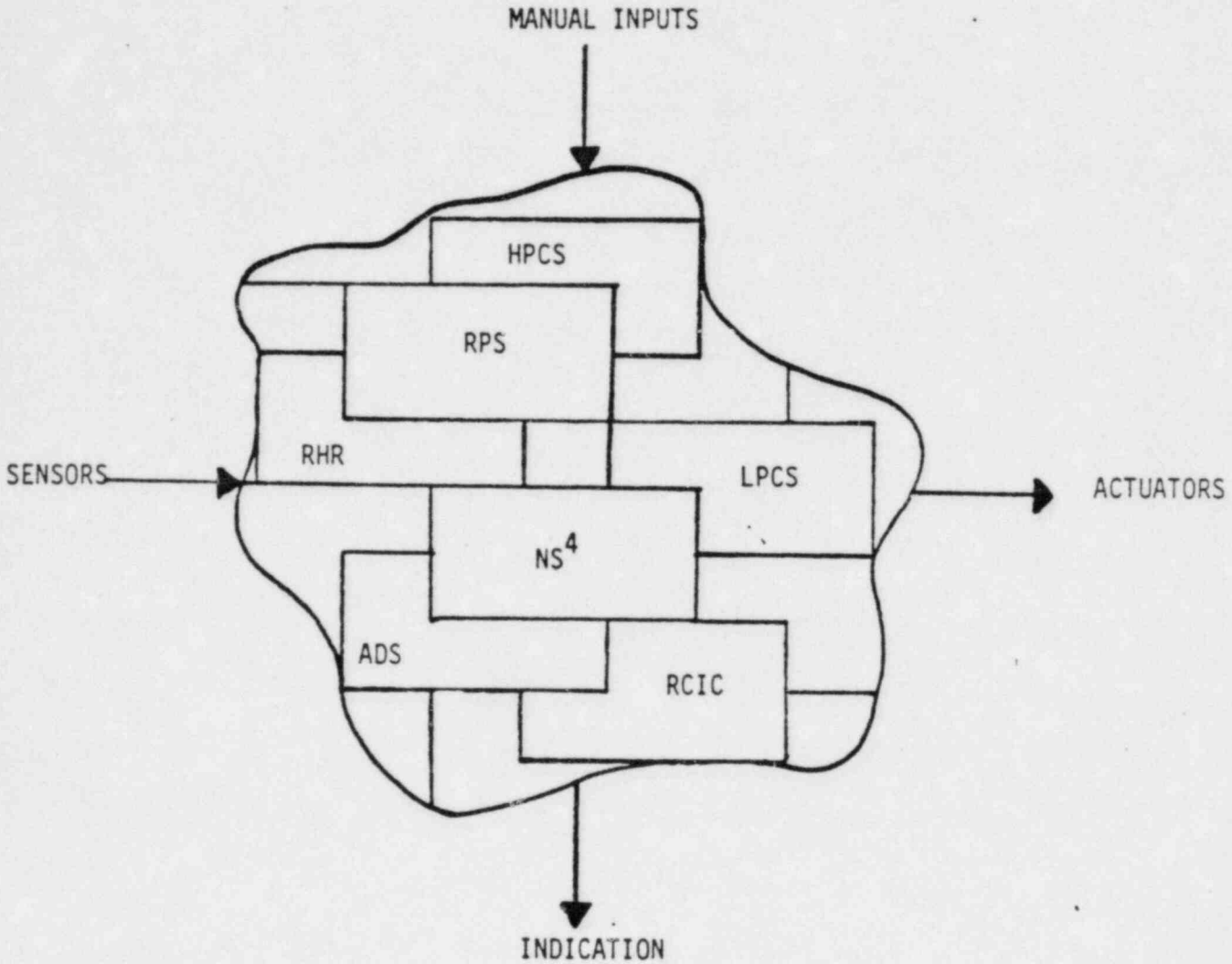


FIGURE 2: PRE-NSPS DESIGN

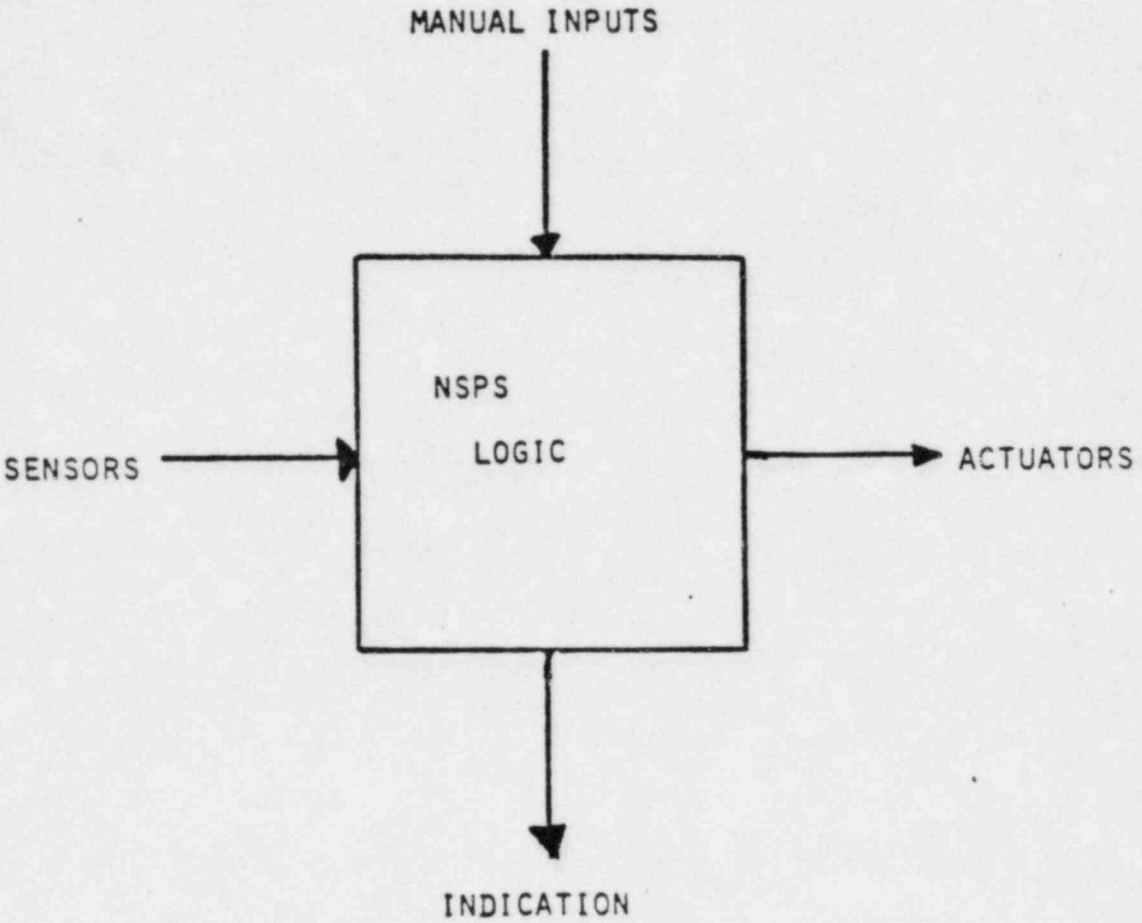


FIGURE 1

NSPS DESIGN

NSPS - DIFFERENCES FROM RELAY DESIGN (LOGIC)

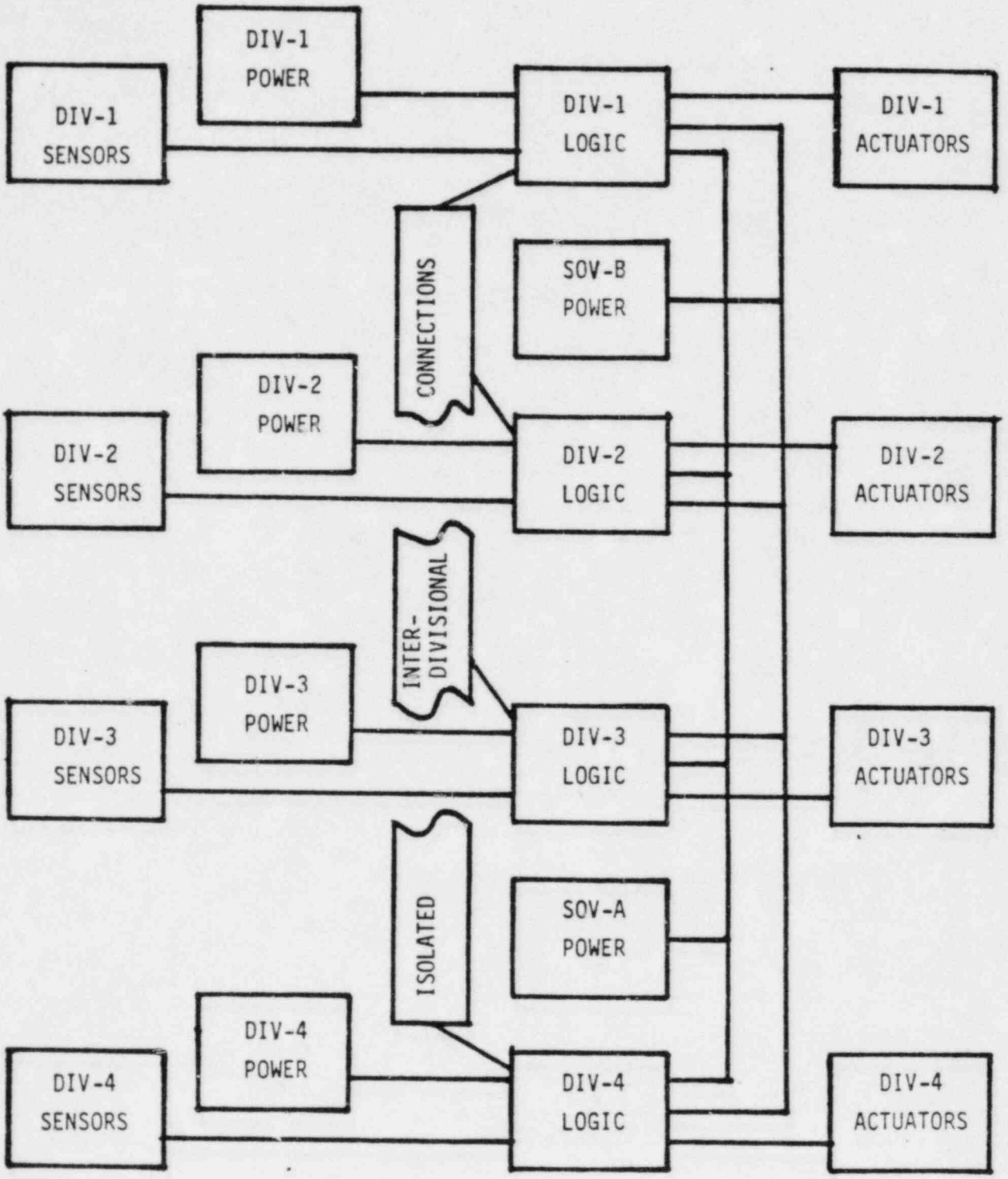
- (2/4) - RPS
  - MSIV ISOLATION

- (TRIP ON LIKE VARIABLES)
  - RPS
  - NS^4

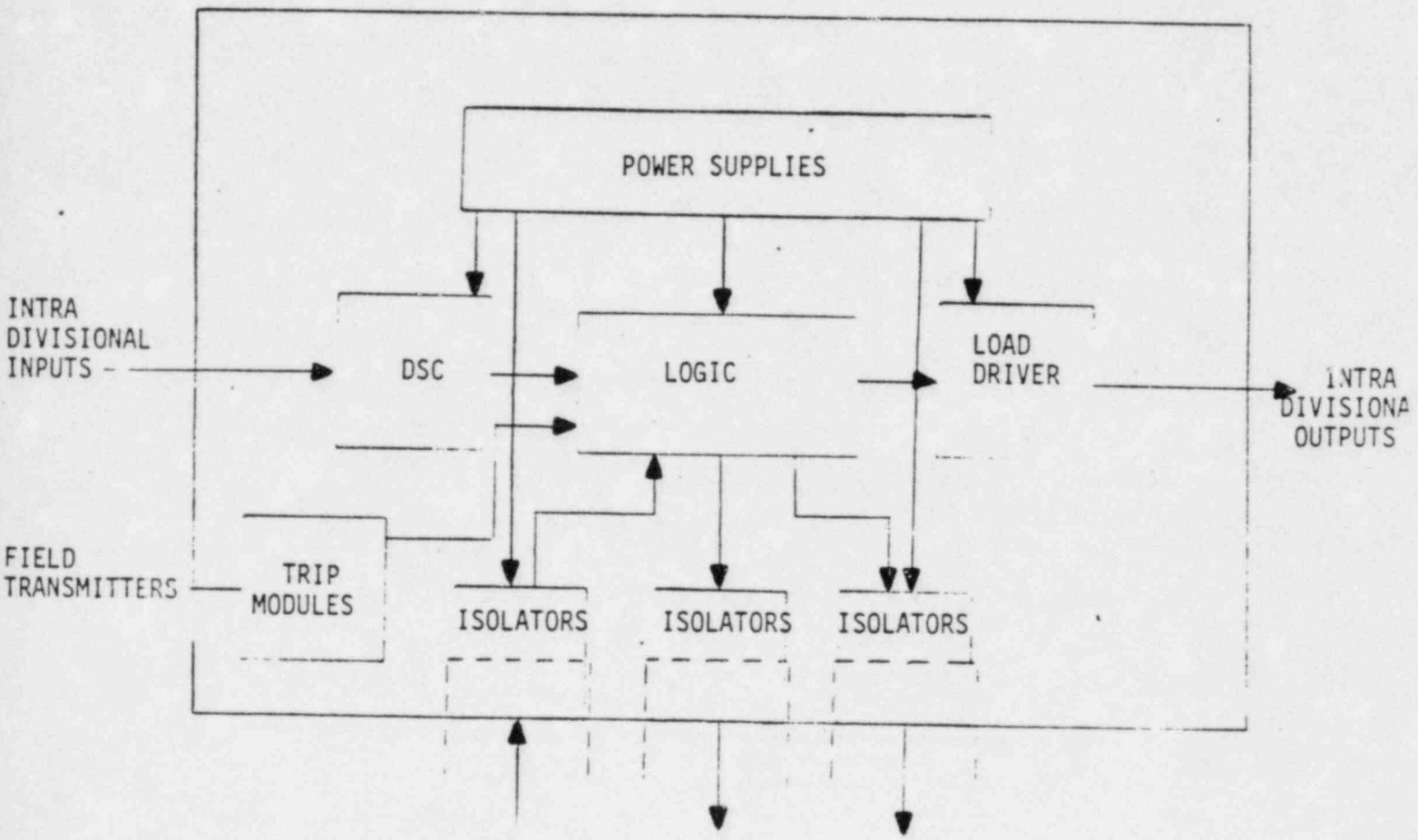
- (DIVISION BYPASS)
  - 2/4 BECOMES 2/3

- SOLID STATE INSTEAD OF RELAY

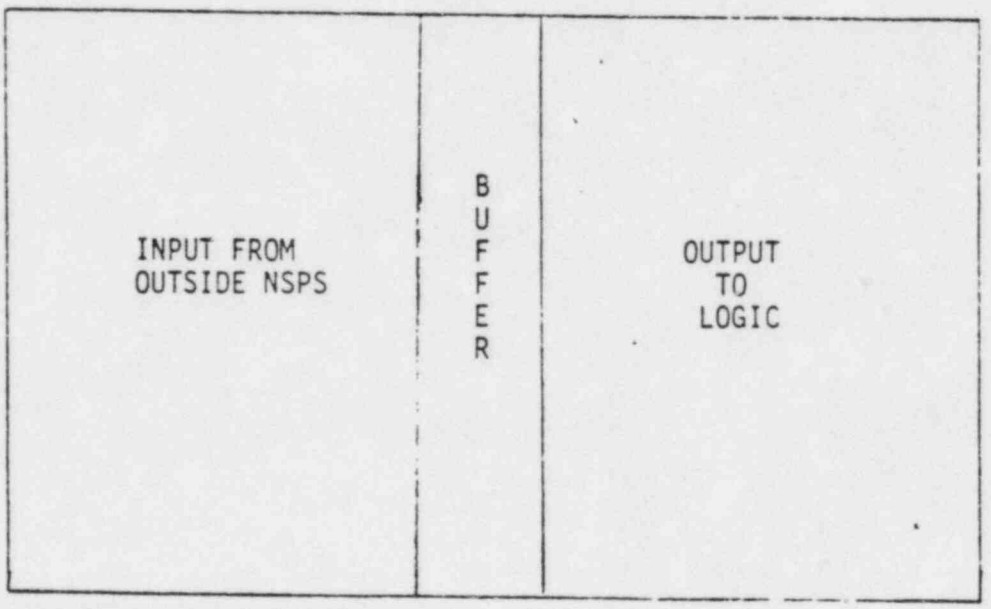
NSPS - SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM OF NSPS DEVICES



DSC CARD



DCS'S: DIGITAL SIGNAL CONDITIONERS

PURPOSE: TO PROVIDE AN INTERFACE TO THE CMOS LOGIC FROM NSPS EXTERNAL, DIVISIONAL SIGNALS

- o FIELD SWITCHES (LIMIT SWITCHES, ETC.)
- o PRESSURE SWITCHES (E.G. TURBINE TRIP)
- o MANUAL SWITCHES (CONTROL PANEL)

FEATURES:
- o ELECTRICAL ISOLATION
- o TESTABLE
- o REPLACEMENT MODULE

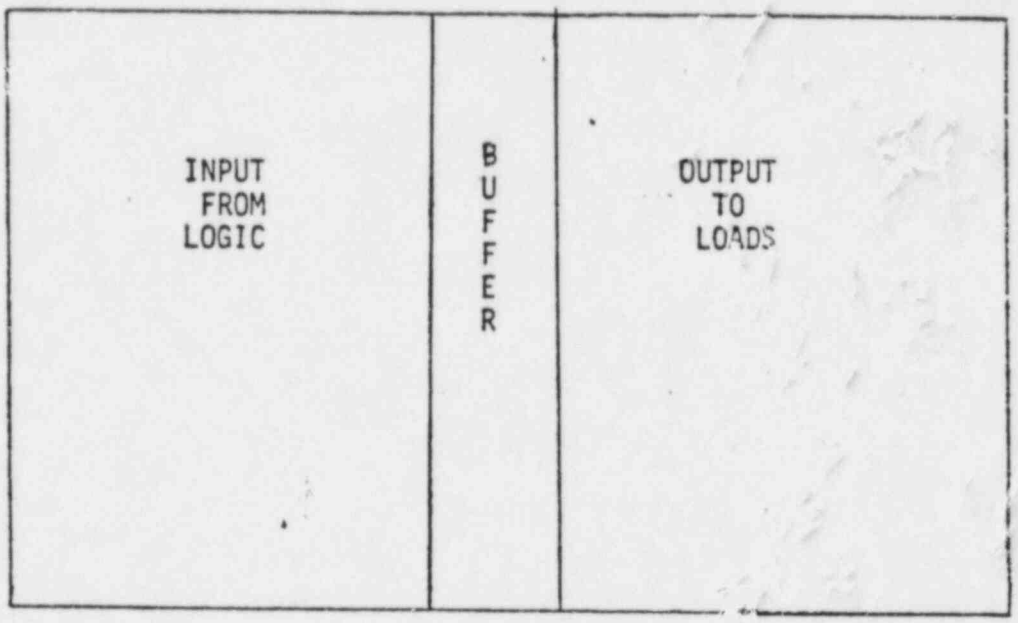
ATM'S: ANALOG TRIP MODULES

PURPOSE: MONITOR PLANT PARAMETERS AND PROVIDE A LOGIC INPUT WHEN THEY HAVE CHANGED IN SUCH A WAY AS TO REQUIRE ACTION FROM NSPS CIRCUITS.

FEATURES:

- ELECTRICAL ISOLATION/BUFFERING
- TESTABLE
- REPLACEABLE MODULE
- DIGITAL READOUT OF PLANT PARAMETER
- COMPARES SENSORS AGAINST OTHER DIVISIONS
- CAN BE CALIBRATED WITHOUT BEING REMOVED
- UPSCALE AND DOWN SCALE TRIPS IN ONE UNIT

LOAD DRIVER



LOAD DRIVERS:

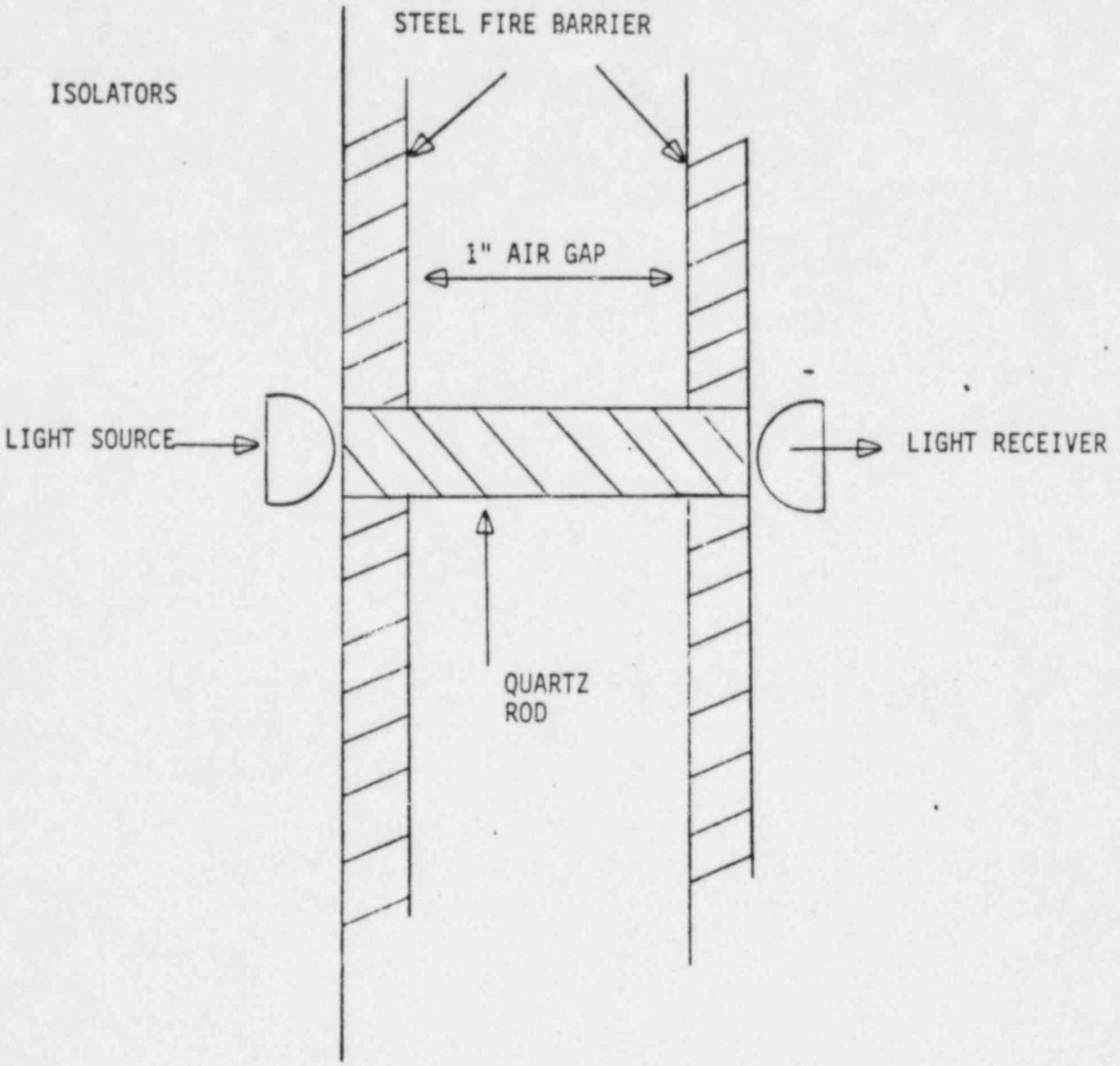
PURPOSE: NSPS INTERFACE TO

- o MOTOR CONTROL CENTERS
- o BOP LOADS
- o OTHER DIVISIONAL LOADS (RPT ETC.)

FEATURES:

- o ELECTRICAL ISOLATION
- o TESTABLE
- o REPLACEABLE MODULE
- o LOW VOLTAGE DROP & POWER DISSIPATION
- o SINGLE TYPE FOR ALL APPLICATIONS

INTERDIVISIONAL ISOLATION



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ISOLATORS

PURPOSE: TO PROVIDE COMMUNICATION BETWEEN DIVISIONS, AND BETWEEN DIVISIONAL AND NON-DIVISIONAL LOCATIONS.

- o 2/4 LOGIC DECISIONS
- o SELF TEST SYSTEM COMMUNICATION
- o ANALOG, OUTPUTS TO RECORDERS, METERS, ETC.

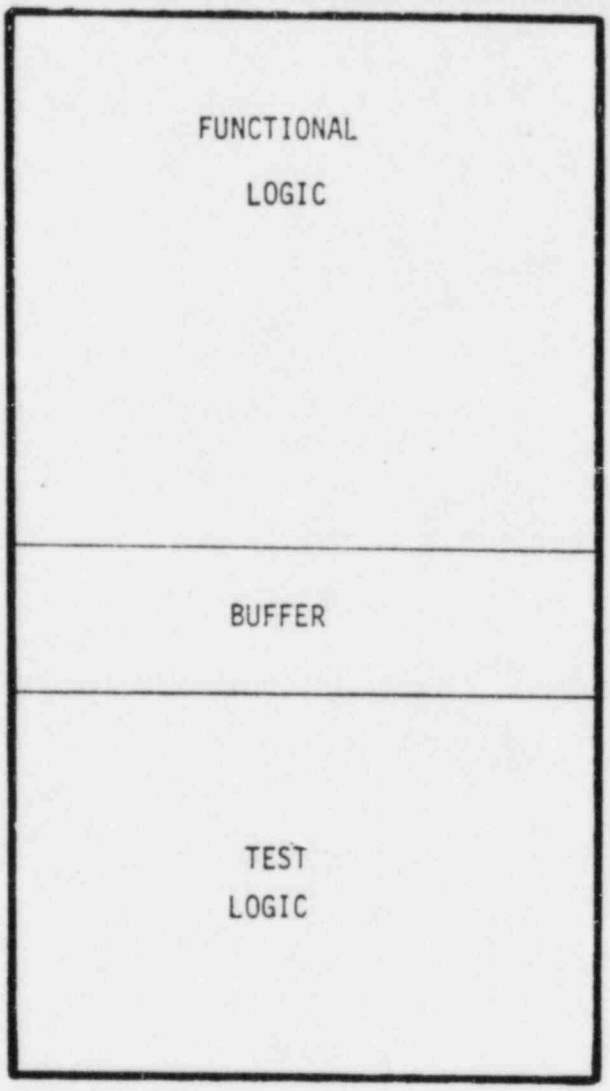
FEATURES:

- o TYPE DEDICATION BY APPLICATION
- o FULL ELECTRICAL & THERMAL SEPARATION (R.G. 1.75) IN CONJUNCTION WITH PANEL DESIGN
- o REPLACEABLE MODULES
- o ANNUNCIATE ON LOSS OF POWER WHERE APPROPRIATE

TYPES:

- o LLOI'S - LOGIC TO LOGIC OPTICAL ISOLATORS
  INTER-DIVISIONAL COMMUNICATION
- o CAOI'S - COMPUTER/ANNUNCIATOR/OPTICAL ISOLATORS
  DIVISIONAL TO NON-DIVISIONAL COMMUNICATION
- o AISO - ANALOG OPTICAL ISOLATORS
  PLANT PARAMETERS TO RECORDING/INDICATING DEVICES

NSPS LOGIC CARD



LOGIC CARDS

PURPOSE:

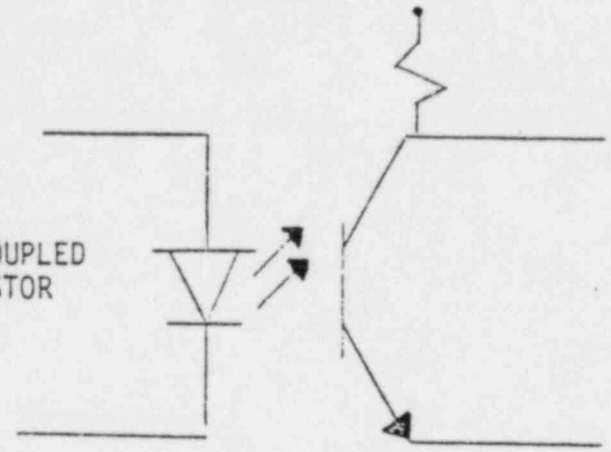
- o TO PERFORM THE SYSTEM LOGIC FUNCTIONS
- o PROCESS INPUTS AND PRODUCE OUTPUTS
- o CAUSE ACTUATION OF PLANT EQUIPMENT TO MAINTAIN OR PRODUCE DESIRED PLANT PARAMETERS

FEATURES:

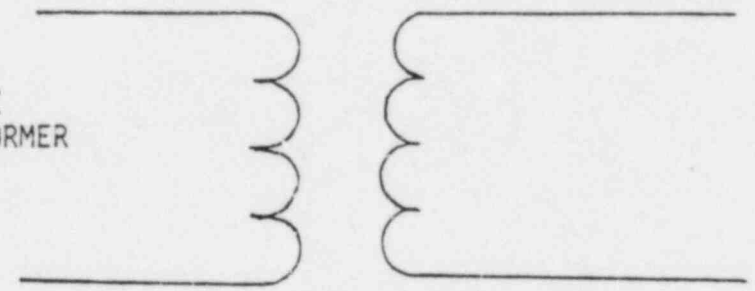
- o A LIMITED NUMBER OF CARD TYPES TO SATISFY ALL CONTROL EQUATIONS
- o REPLACEABLE MODULES
- o TESTABLE
- o CMOS LOGIC ELEMENTS
- o BUFFERING BETWEEN FUNCTIONAL & TEST CIRCUITRY

BUFFERING TECHNIQUES

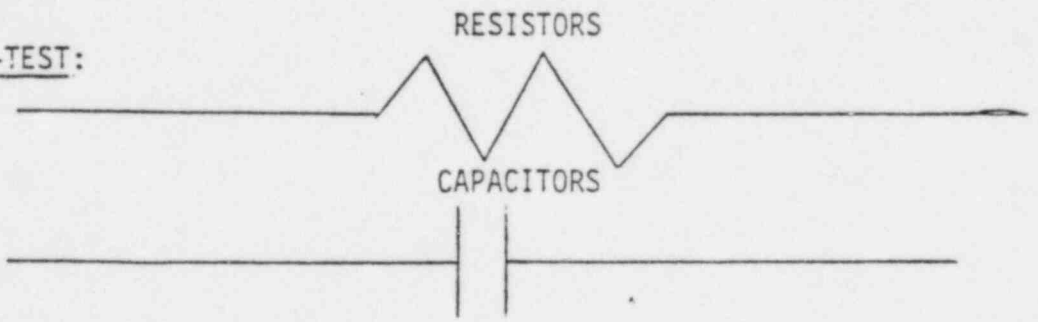
DSC's:

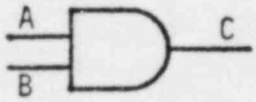


LD's:



SELF-TEST:





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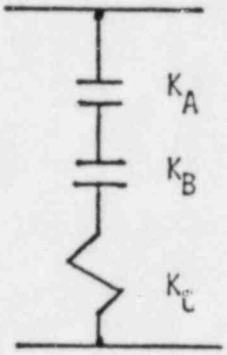

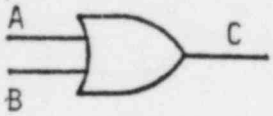

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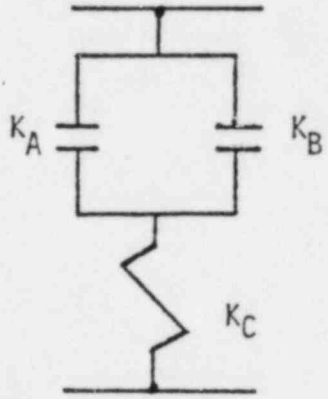
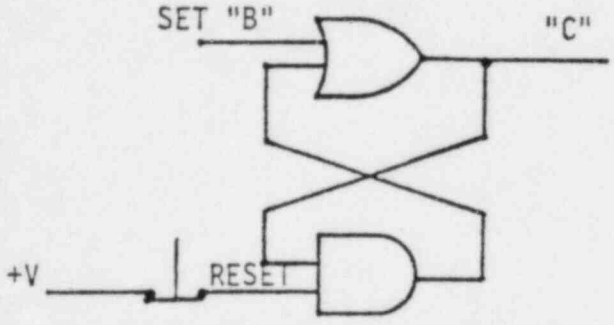
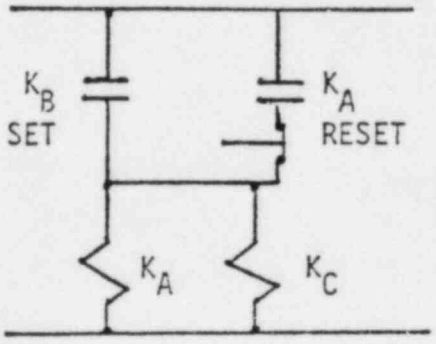
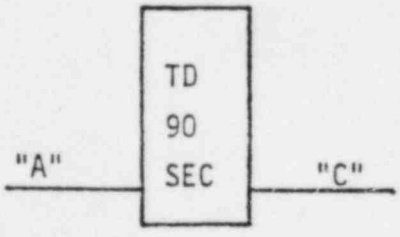


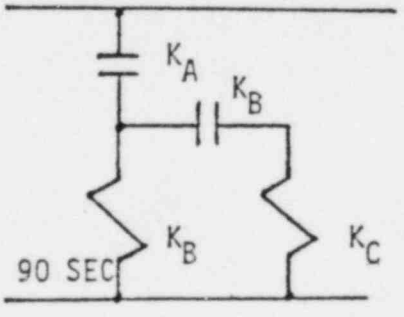
LATCH





TIME
DELAY





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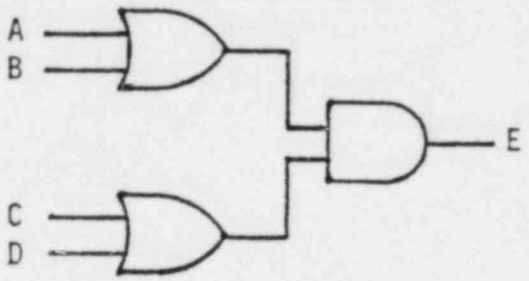

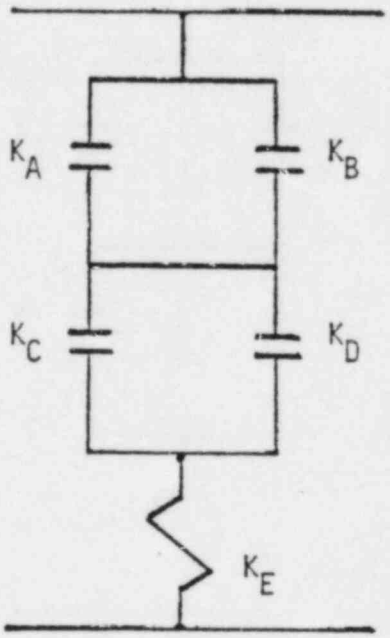

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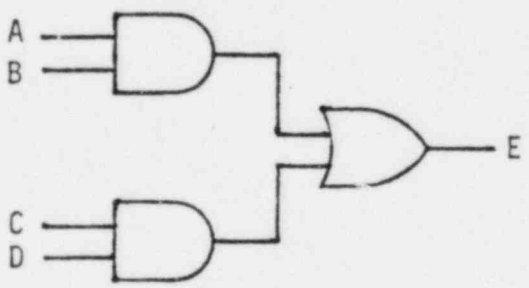
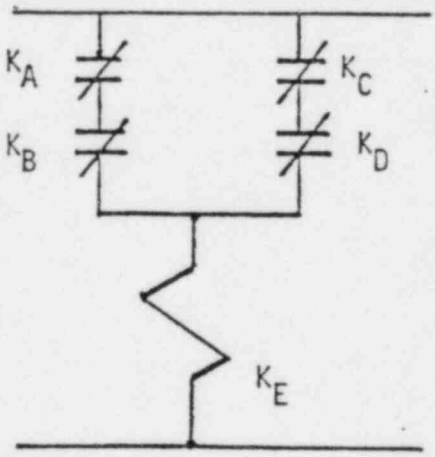
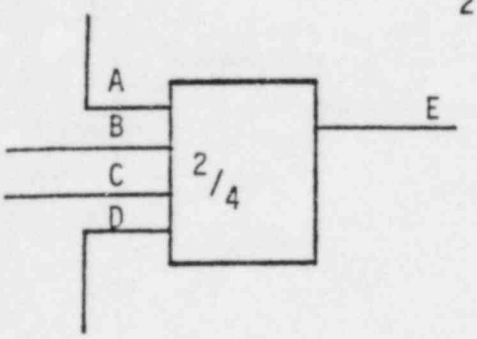
(NEG LOGIC)

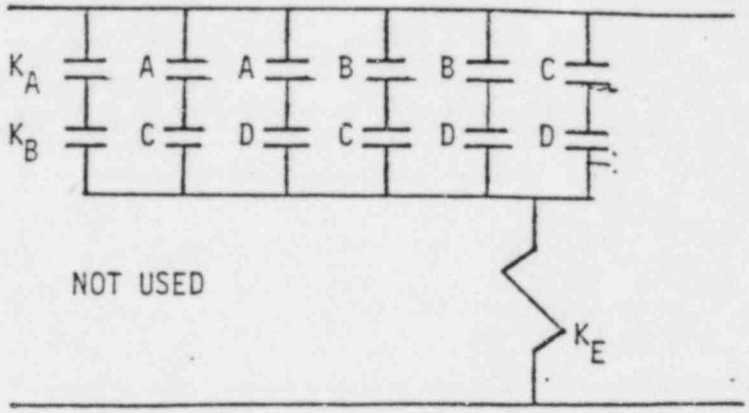




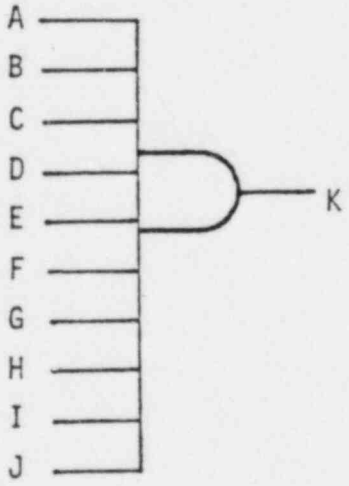
SOLID STATE VERSUS RELAY LOGIC

2 OUT OF 4





SCRAM LOGIC
(NEG LOGIC)



POWER SUPPLIES:

PURPOSE: TO PROVIDE RELIABLE, STABLE, AND EFFICIENT POWER SOURCES FOR THE SOLID STATE DEVICES.

FEATURES:

- o 20 MS HOLDING TIME AFTER INTERRUPTION OF SOURCE POWER
- o BROWN OUT PROTECTION
- o ADJUSTABLE OUTPUT VOLTAGE
- o CURRENT LIMITING
- o OVER VOLTAGE PROTECTION
- o TOLERANT TO LOAD CHANGES
- o TOLERANT TO SOURCE VOLTAGE FREQUENCY

NET EFFECT: ELECTRICAL ISOLATION OF THE DECISION MAKING CIRCUITRY

SELF TEST SYSTEM:

PURPOSE: TO ENHANCE PLANT AVAILABILITY WITHOUT DEGRADING RELIABILITY.

FEATURES:
- o ON LINE TESTING OF NSPS FUNCTIONAL CIRCUITS
- o ISOLATION OF DEFECTIVE COMPONENTS TO A REPLACEABLE MODULE
- o SELF-CHECKING ROUTINE

NSPS CABINETS:

PURPOSE: TO HOUSE NSPS SYSTEMS IN CONFORMANCE TO SEPARATION & OTHER DESIGN REQUIREMENTS.

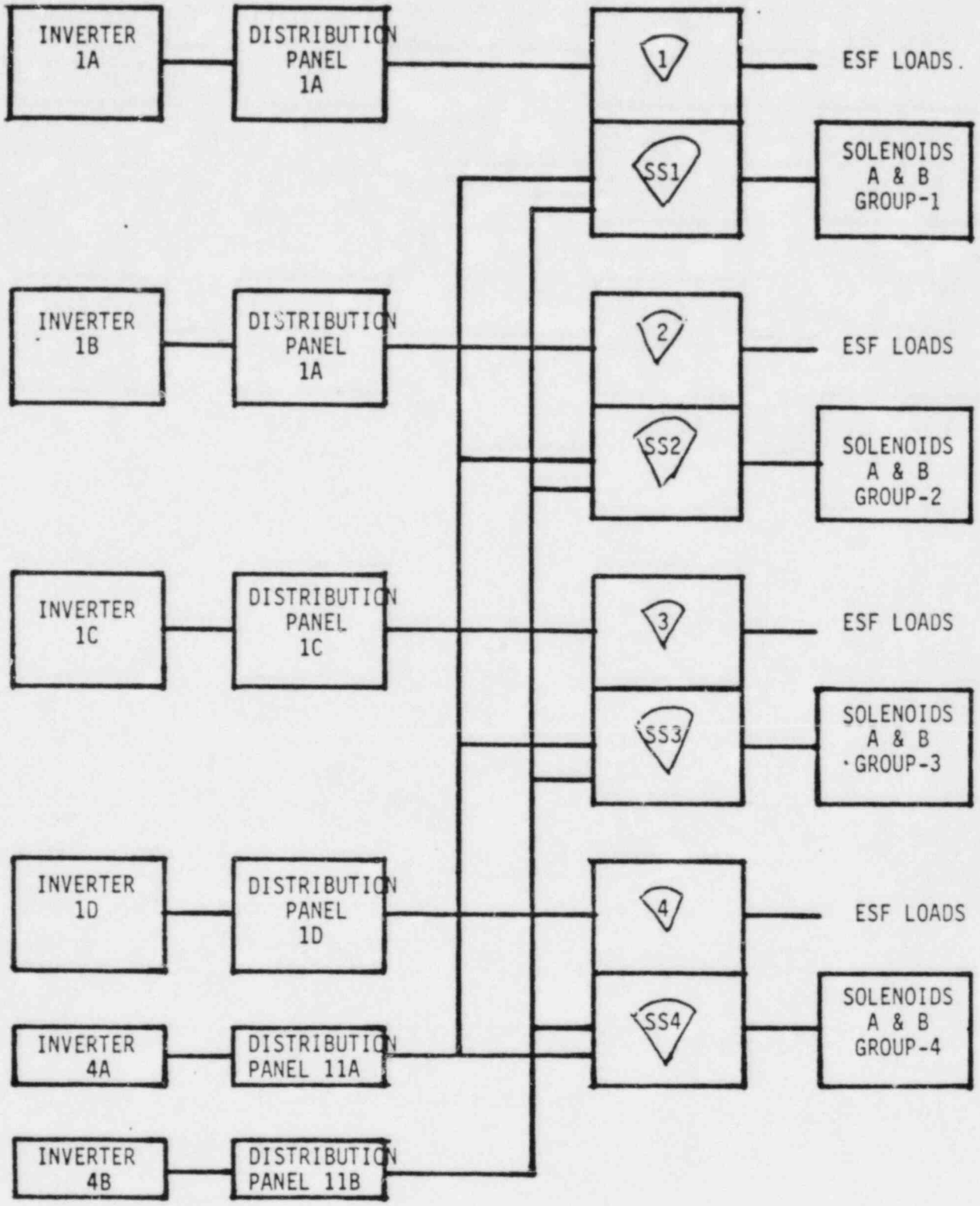
FEATURES:

- o 4 PANELS, ONE FOR EACH DIVISION
- o COMPATIBLE WITH PGCC SEPARATION
- o EACH PANEL HAS SEPARATE BAYS FOR
  - ISOLATORS
  - LOGIC CARDS
  - TRIP MODULES
- o ISOLATOR BAYS PROVIDE INTERDIVISIONAL AND DIVISIONAL TO NON-DIVISIONAL PHYSICAL INTERFACE
- o NSPS SYSTEMS OF EACH DIVISION ARE GROUPED TOGETHER IN ONE CABINET.

NSPS POWER DISTRIBUTION

- CLASS 1E
- FOUR DIVISIONS OF POWER PLUS TWO SPECIAL DIVISIONS
- NORMAL CONNECTION TO OFFSITE POWER
- BATTERY, BATTERY CHARGER, INVERTER, STATIS BYPASS SWITCH
- ALL LOGIC PLUS ESF LOADS POWERED BY DIVISIONAL BUSSES
- RPS, MSIV LOADS POWERED BY SPECIAL BUSSES
- SPECIAL BUSSES SIMILAR TO PRESENT RPS BUSSES

NSPS POWER DISTRIBUTION



PANEL CONFIGURATION

A	B	C	D
ISOLATOR BAY	INSTRUMENT BAY	LOGIC BAY	ISOLATOR BAY
	RPS (ATM)	RPS	
	NS4 (ATM)	RPS	
	HPCS (ATM)	STC	
	SPARE	NS4	
	SPARE	NS4	
		HPCS	
		MISC. SYSTEMS	
		SPARE	
	REDUNDANT POWER SUPPLY MODULE	POWER SUPPLY MODULE	

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PANEL POWER DISTRIBUTION:

- AUCTIONEERED POWER SUPPLIES
- BUSSES FUSED BY SYSTEM
  NS^4, RPS, ETC.
- HARDWARE DETECTION/ANNUNCIATION OF BUS FAULT
- SELF TEST MONITORING OF INDIVIDUAL SUPPLIES
- SELF TEST MONITORING OF AUCTIONEERED BUSSES
- AUXILLIARY +12 VDC AND SELF TEST POWERED FROM DIFFERENT 120 VAC SOURCE THAN PRIMARY SYSTEM POWER

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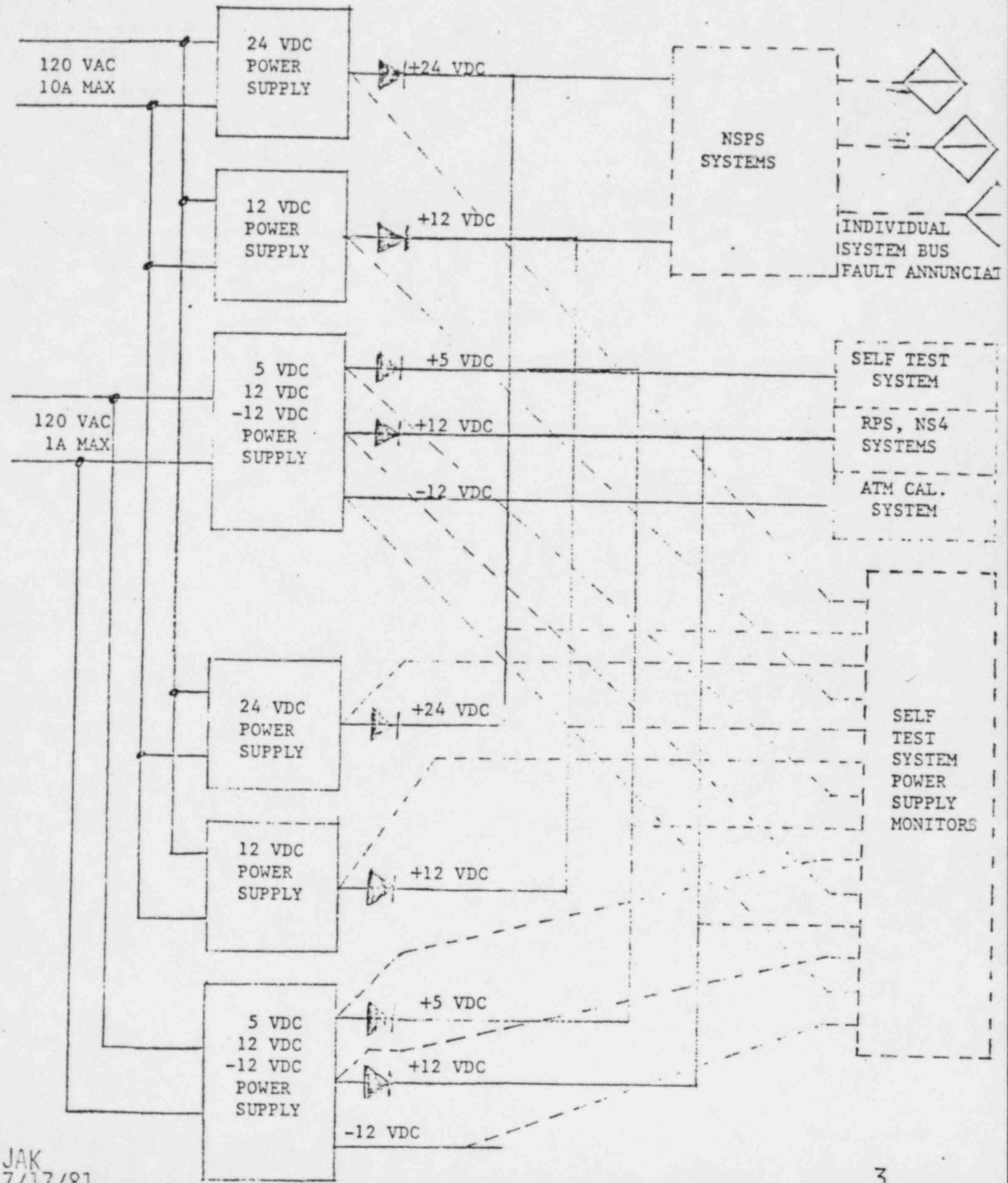
PANEL POWER



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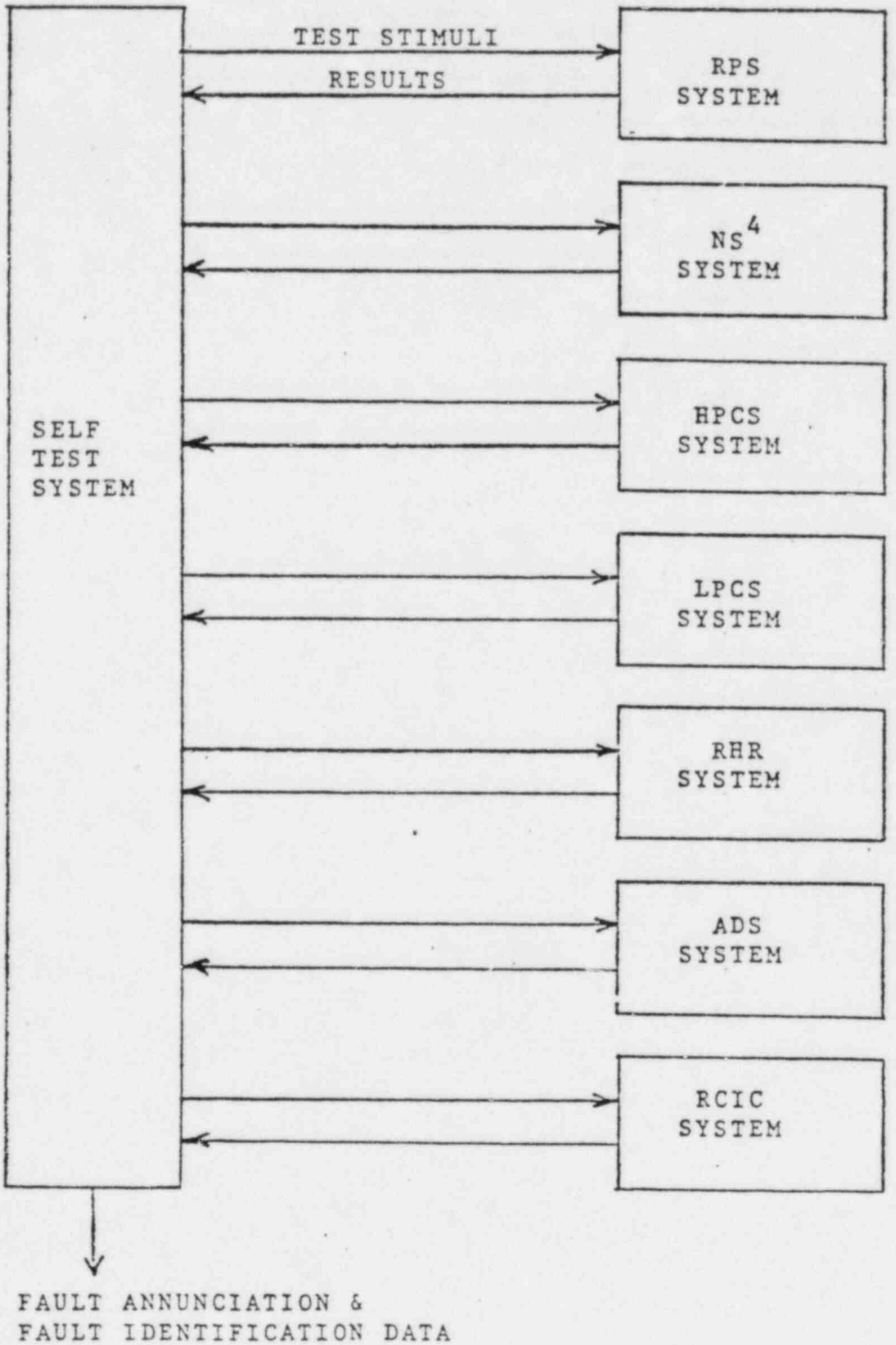
REPRESENTATIVE PANEL



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SELF TEST SYSTEM

- NOT A SUBSTITUTE FOR NORMAL SURVEILLANCE TEST ACTIVITIES.

- ENHANCE THE AVAILABILITY OF THE NSPS BY REDUCING THE MEAN TIME TO DETECT AND REPAIR A FAILURE

  TESTING PERFORMED ON AN AUTOMATIC CYCLE

  CARD FAILURES IDENTIFIED TO PANEL, BAY, CARD FILE, CARD SLOT, CARD TYPE UPON REQUEST

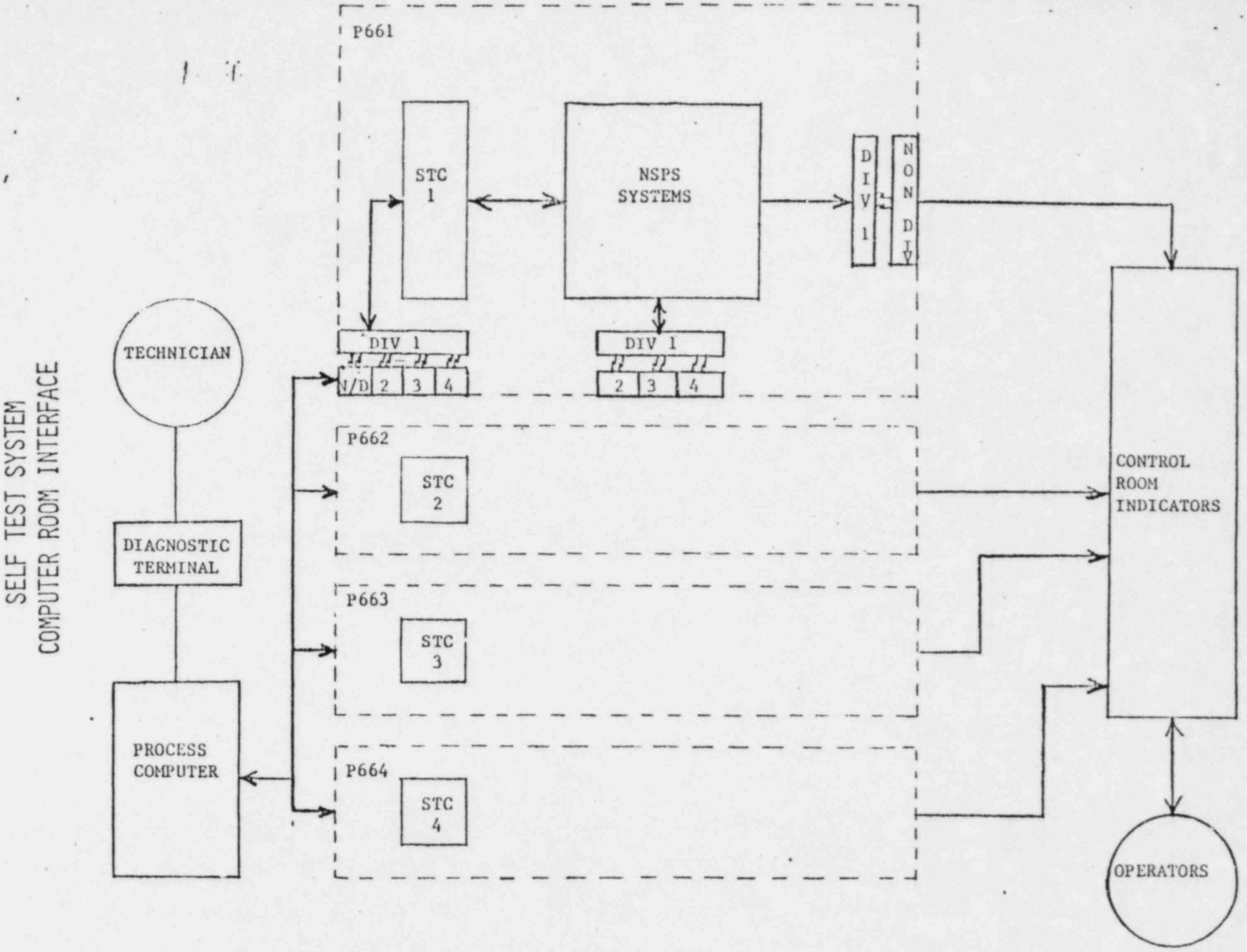
  SUPPORTING FAILURE DATA AVAILABLE UPON REQUEST

  SINGLE CARD TEST UPON REQUEST TO VERIFY FIX

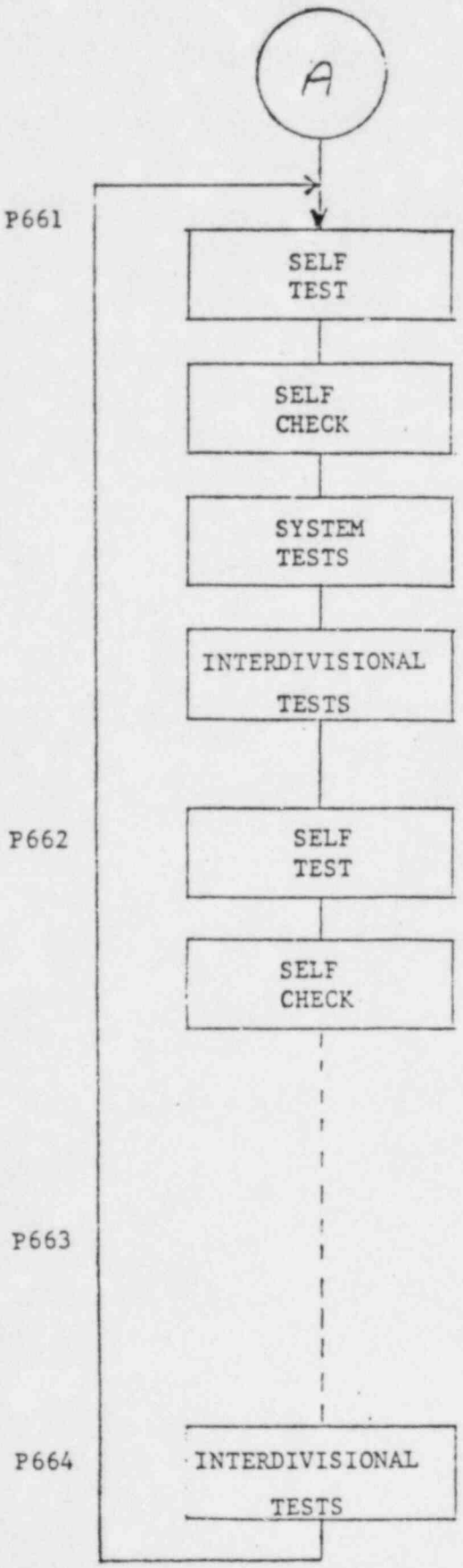
- NO SINGLE FAILURE OF THE SELF TEST SYSTEM WILL PREVENT THE FUNCTIONAL LOGIC FROM PERFORMING ITS REQUIRED OPERATION

  SELF TEST SYSTEM CIRCUITRY DECOUPLED FROM FUNCTIONAL LOGIC BY CURRENT LIMITING RESISTORS

  TEST PULSE A/C COUPLED IN ADDITION TO HARDWARE AND SOFTWARE METERING


SELF TEST SYSTEM
COMPUTER ROOM INTERFACE
P661
STC 1
NSPS SYSTEMS
DIV 1
NON DIV
DIV 1
N/D 2 3 4
DIV 1
2 3 4
TECHNICIAN
DIAGNOSTIC TERMINAL
PROCESS COMPUTER
P662
STC 2
P663
STC 3
P664
STC 4
CONTROL ROOM INDICATORS
OPERATORS

AUTOMATIC TEST SEQUENCE



PERFORMS TEST OF CPU, RAM, ROM

PERFORMS TEST OF UNIVERSAL I/O, SERIAL I/O, HARDWARE TIMERS, CARD SELECTORS, POWER MONITORS, CARD OUT OF FILE INDICATORS

PERFORMS TEST OF ALL SYSTEMS THAT DO NOT HAVE SIGNALS FROM OTHER DIVISIONS

PERFORMS TEST OF ALL SYSTEMS THAT HAVE INPUTS FROM OTHER DIVISIONS

SAME AS ABOVE

SAME AS ABOVE

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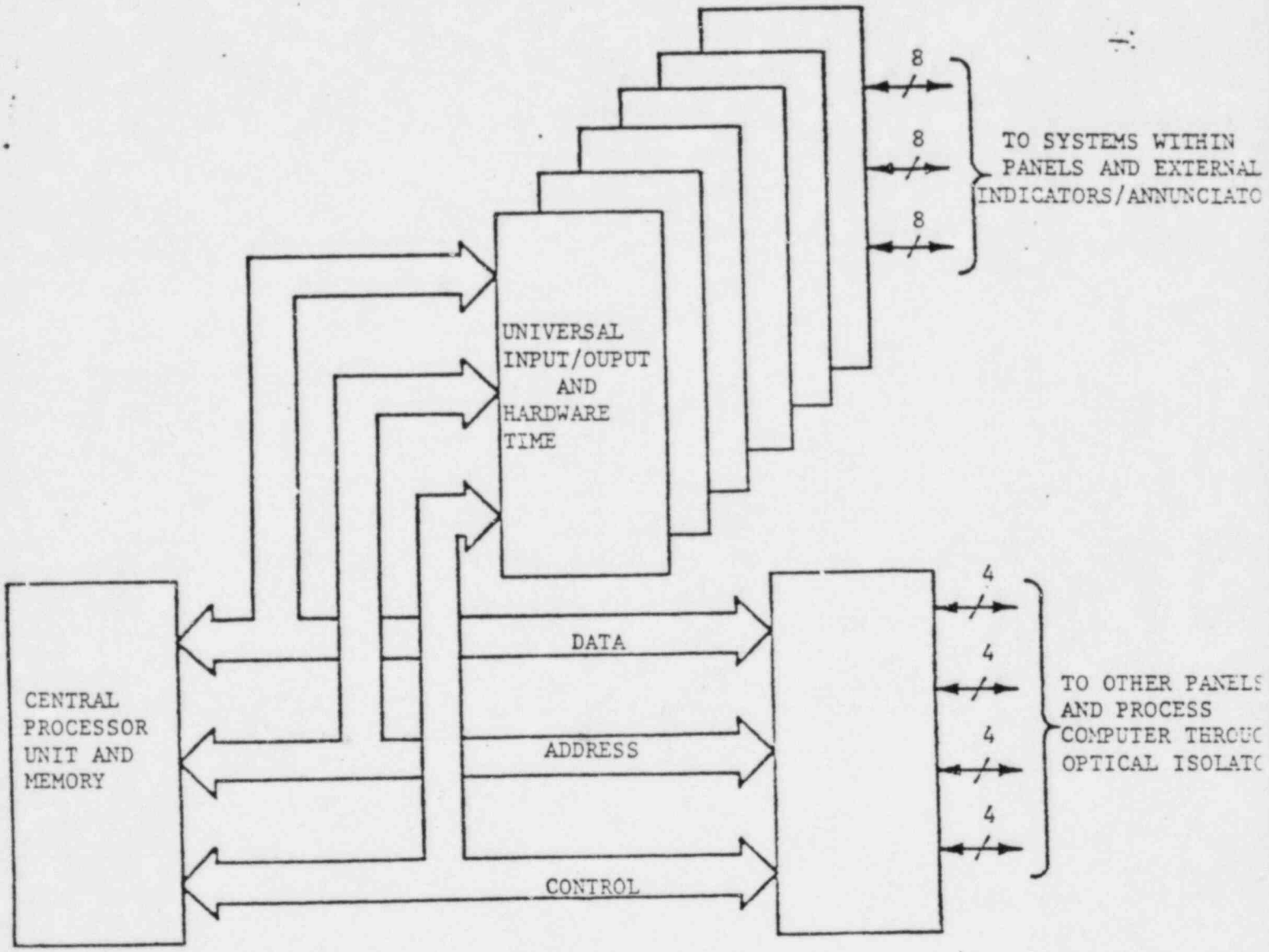
7/17/81

SELF TEST SYSTEM



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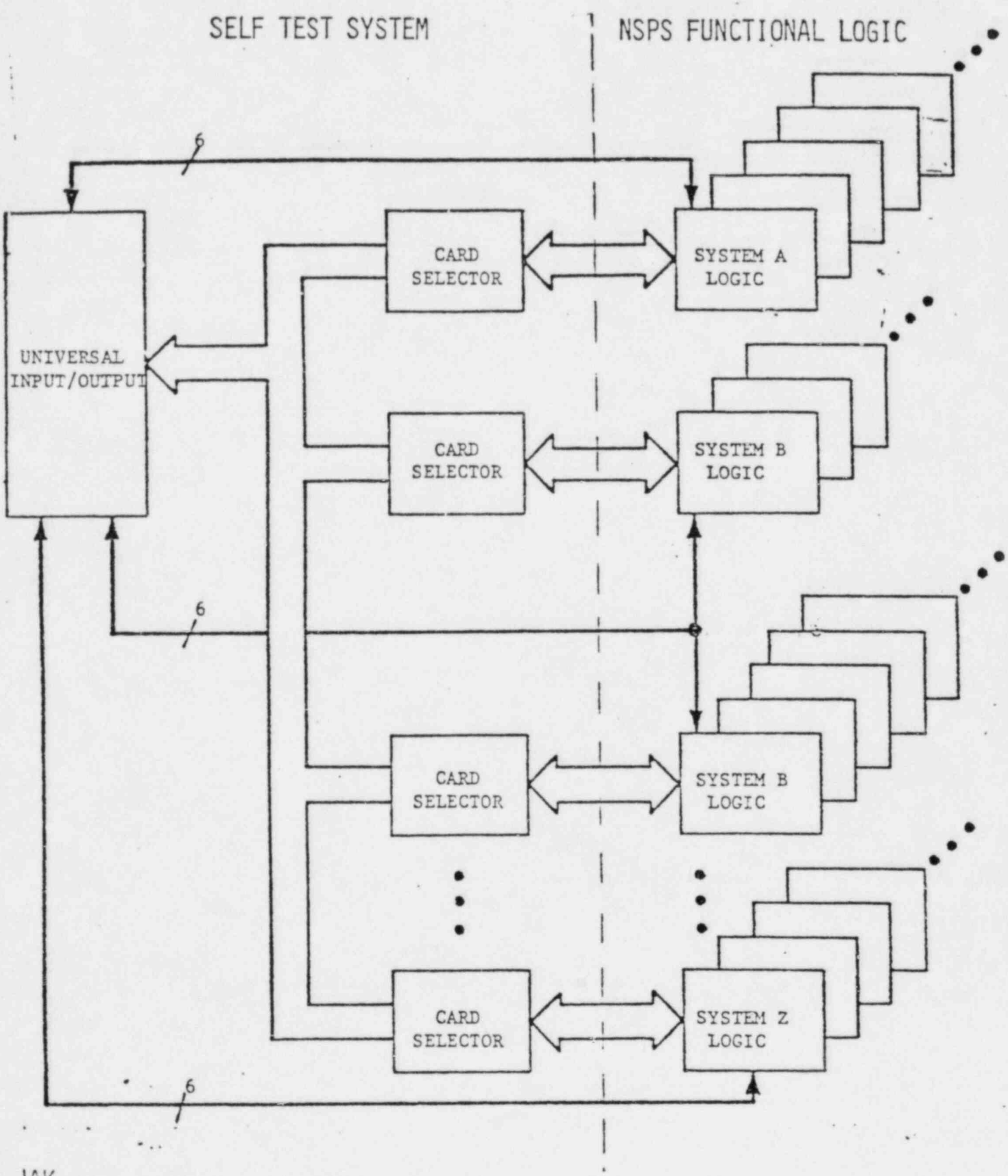
SELF TEST SYSTEM
NSPS FUNCTIONAL LOGIC
6
UNIVERSAL INPUT/OUTPUT
CARD SELECTOR
SYSTEM A LOGIC
CARD SELECTOR
SYSTEM B LOGIC
6
CARD SELECTOR
SYSTEM B LOGIC
CARD SELECTOR
SYSTEM Z LOGIC
6

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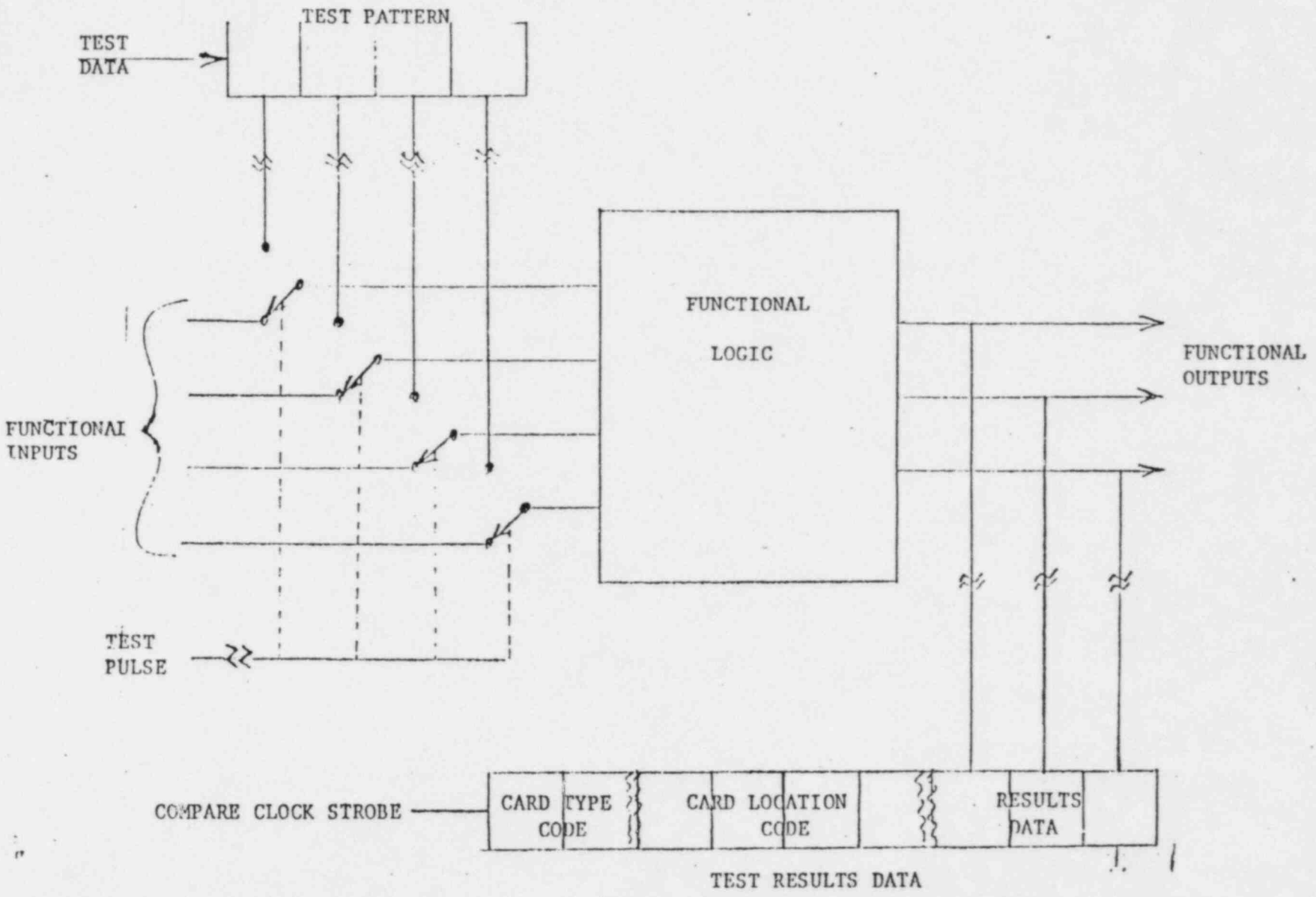
REPRESENTATIVE CARD BLOCK DIAGRAM

SELF TEST INTERFACE



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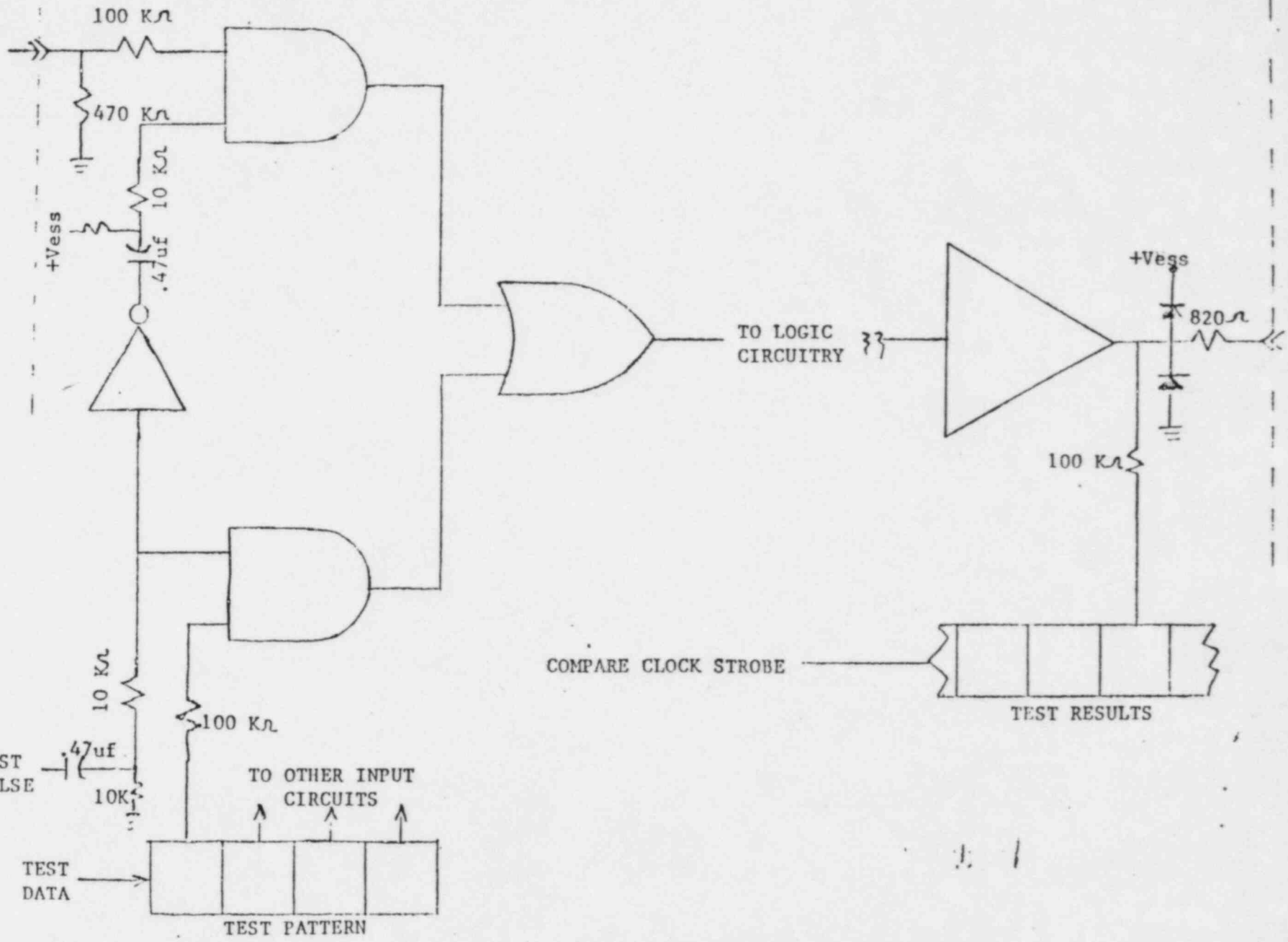
SELF TEST SIGNAL ISOLATION - REPRESENTATIVE CARD



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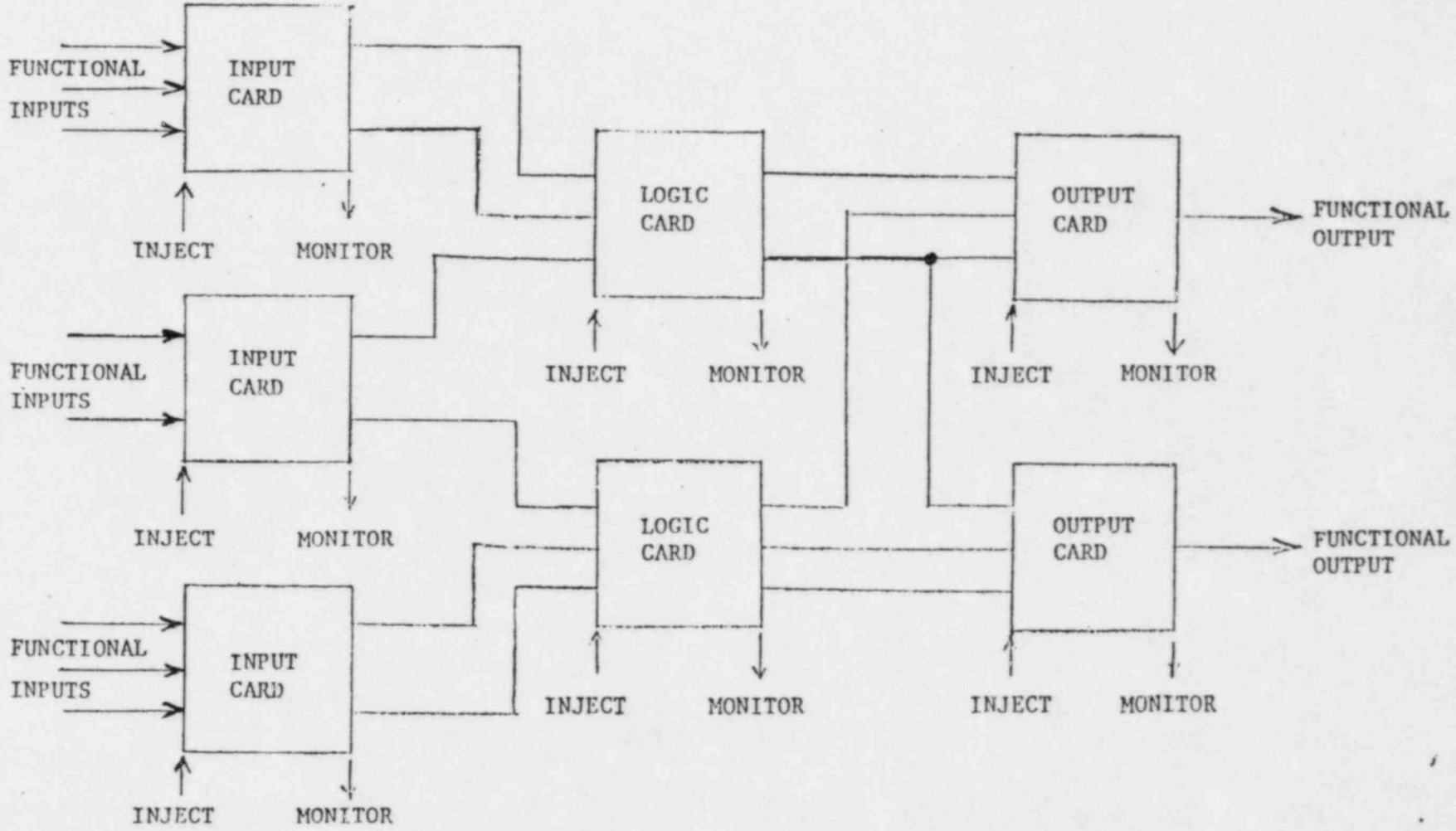
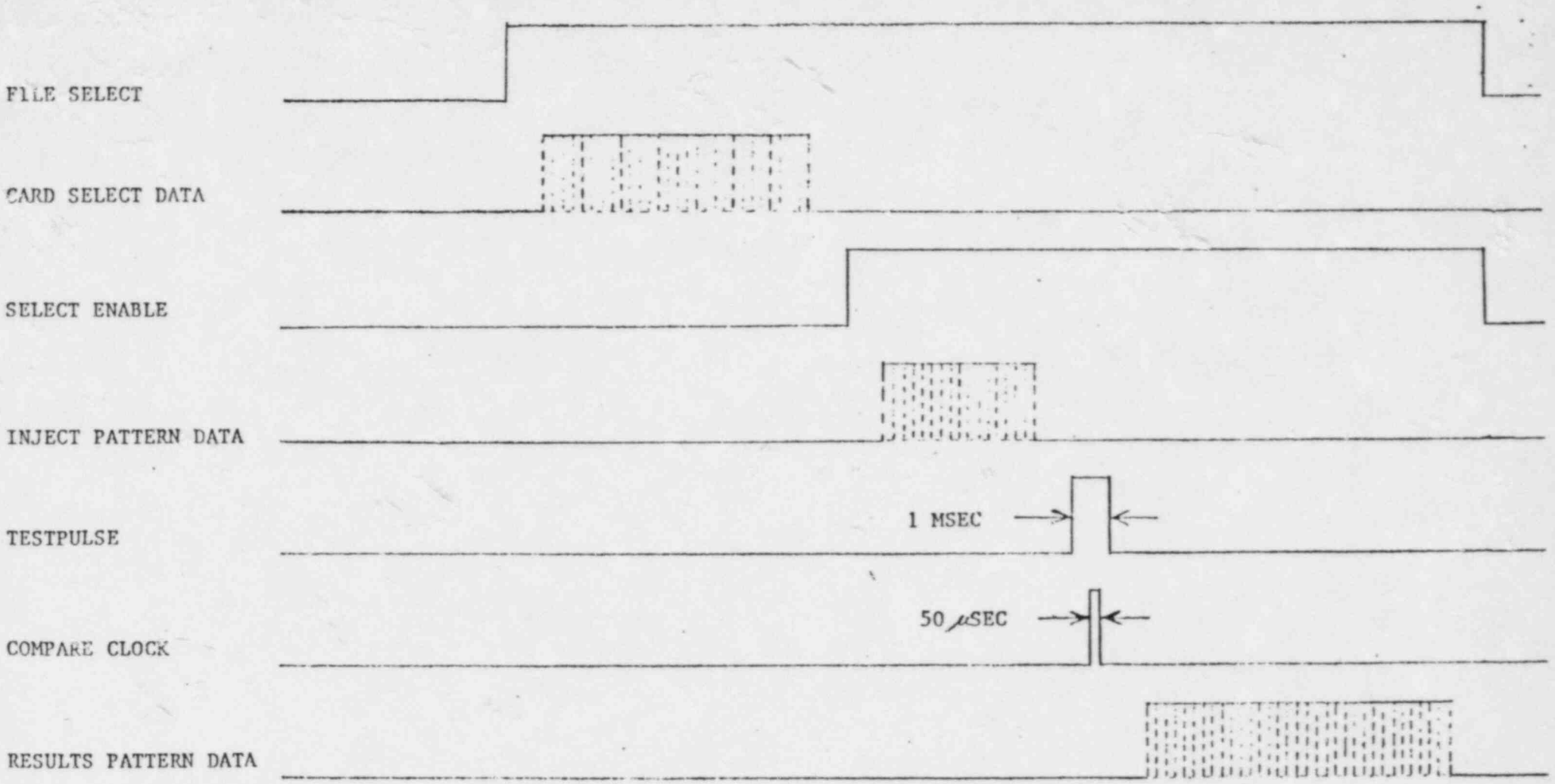
SYSTEM TEST METHODOLOGY - WITHIN DIVISION

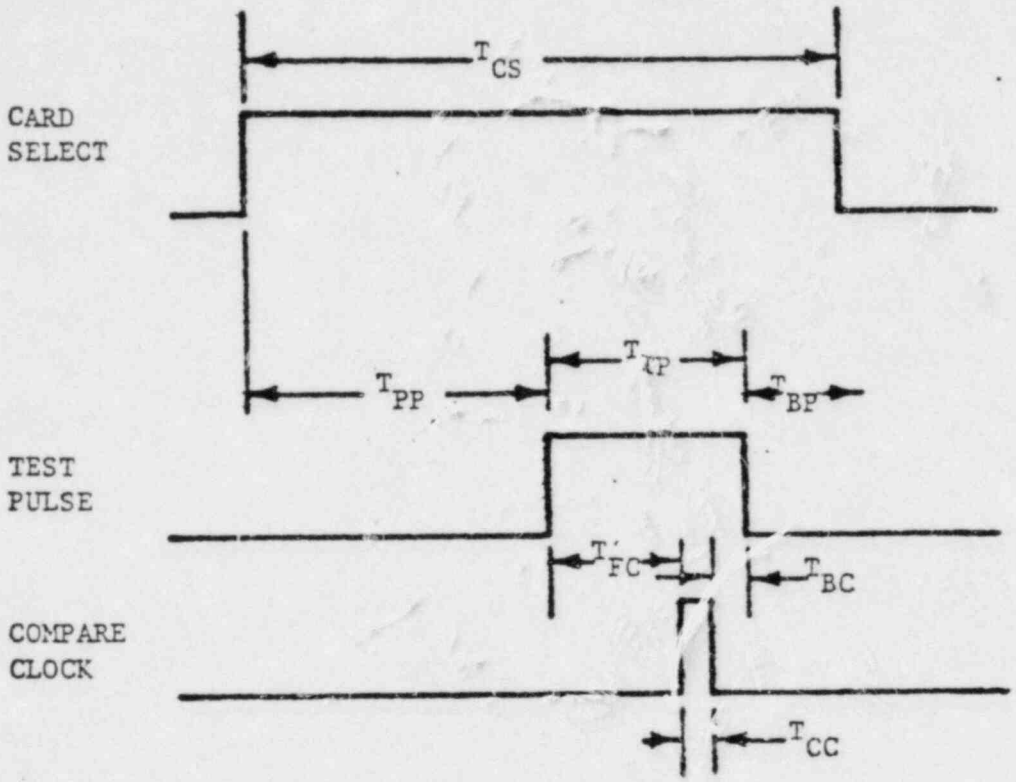


SELF TEST TIMING DIAGRAM



JAK
9/17/81
13

CARD TEST TIMING



T_{CS} (MINIMUM) = T_{TP} + 5 μSECONDS

T_{TP} = 1000 $\pm$ 10 μSECONDS, TEST PULSE DUTY CYCLE = 3% (MAXIMUM)

T_{CC} = 50 $\pm$ 6 μSECONDS

T_{FC} = 800 $\pm$ 124 μSECONDS

T_{BC} (MINIMUM) = 0

T_{FP} (MINIMUM) = 5 μSECONDS

T_{BP} (MINIMUM) = 0

ALL RISE AND FALL TIME 2 μSECONDS

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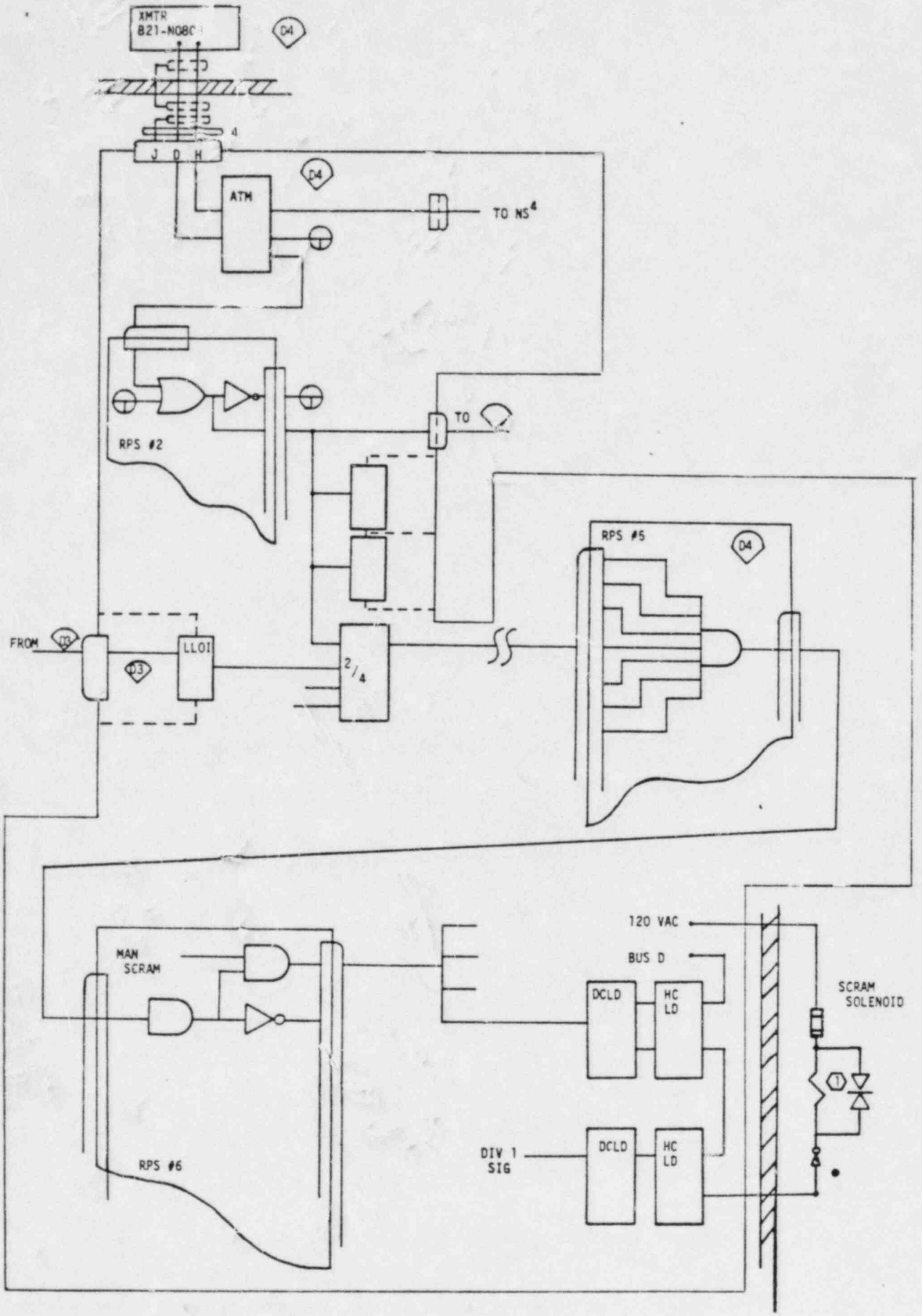
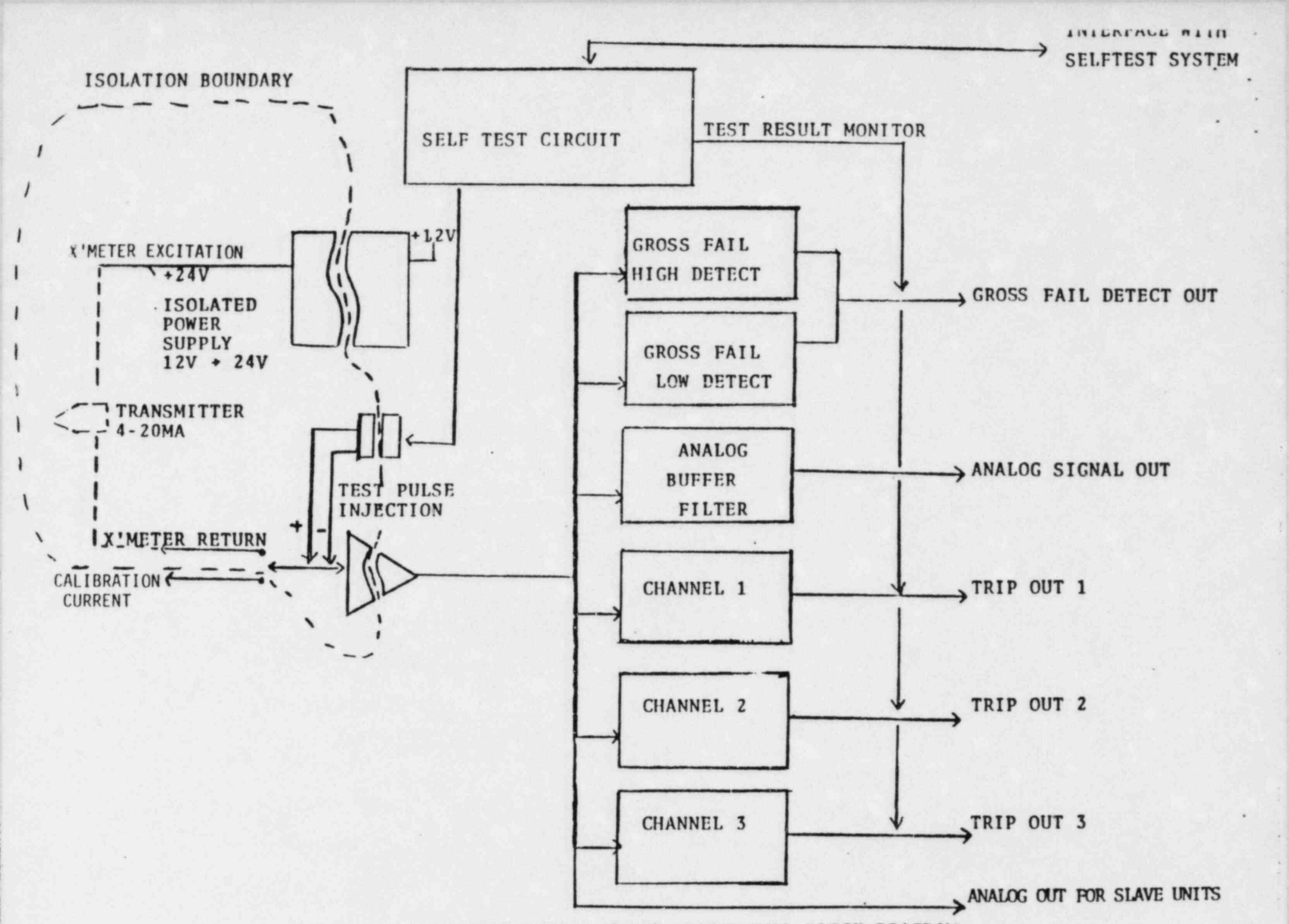
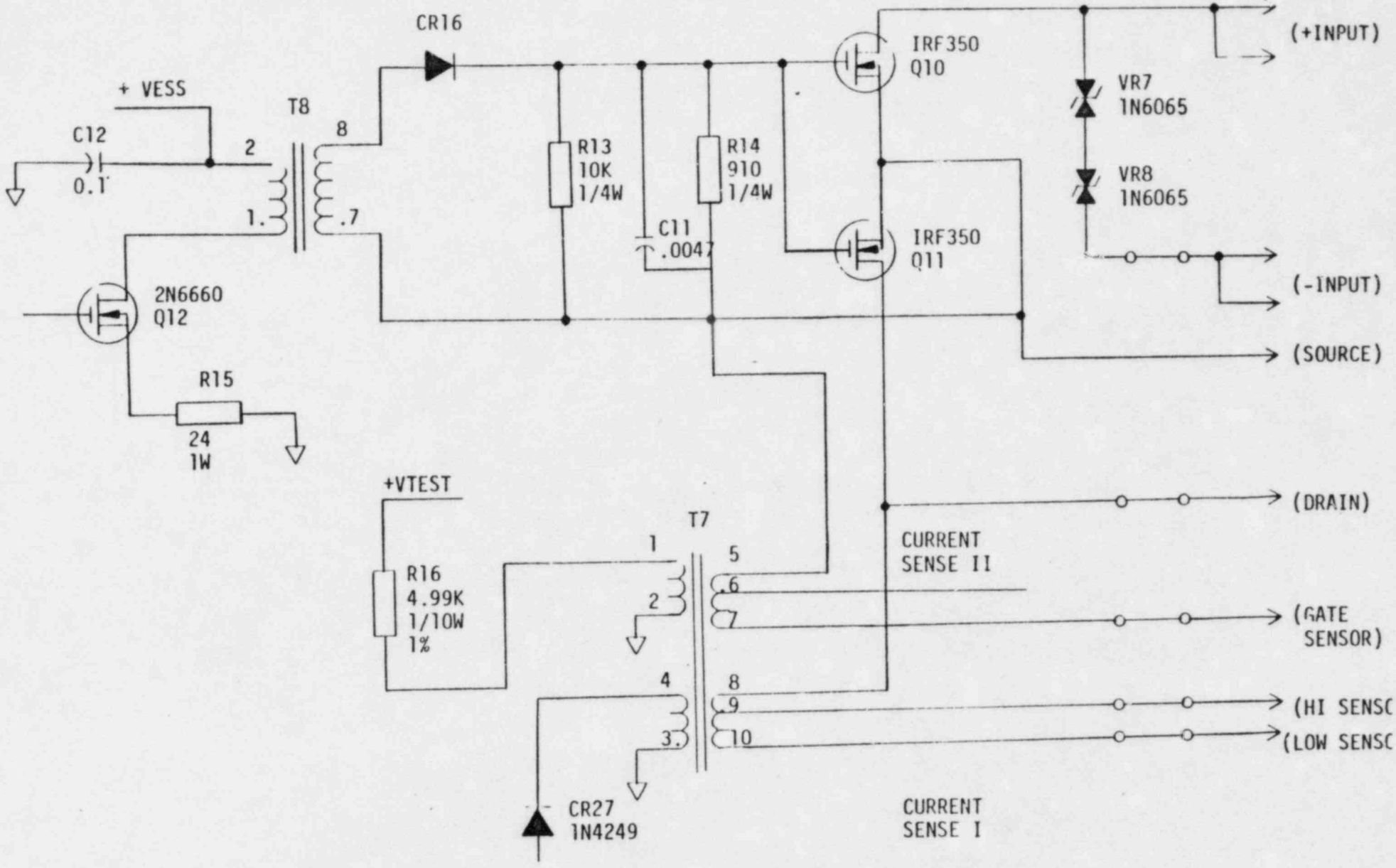
TYPICAL CONTROL PATH





ANALOG TRIP MODULE (ATM) FUNCTIONAL BLOCK DIAGRAM


CR16
+ VESS
T8
C12
0.1
2
8
1.
.7
R13
10K
1/4W
R14
910
1/4W
C11
.0047
IRF350
Q10
IRF350
Q11
VR7
1N6065
VR8
1N6065
(+INPUT)
(-INPUT)
(SOURCE)
2N6660
Q12
R15
24
1W
+VTEST
T7
R16
4.99K
1/10W
1%
1
2
5
6
7
4
8
9
3.
10
CURRENT
SENSE II
(DRAIN)
(GATE
SENSOR)
(HI SENSC
(LOW SENSC
CR27
1N4249
CURRENT
SENSE I

NSPS

RELIABILITY/AVAILABILITY

- o SOLID STATE TECHNOLOGY
- o THOROUGH PRE-OPERATIONAL TESTING
  - FACTORY
  - FIELD
- o REPLACEABLE MODULES
- o INCREASED SURVEILLANCE
  - AUTO TEST
  - AUTO DIAGNOSIS
  - SEMI-AUTOMATIC DIAGNOSTICS
  - BUILT-IN DIAGNOSTIC HARDWARE

ATTACHMENT 2

CLINTON / GESSAR

SELF TEST SYSTEM

(STS)

PRESENTATION

Design Considerations

Self Test System

- **Enhance safety system availability**
  - **Reduce mean time to detection of failure**
  - **Reduce mean time to repair**
  - **Supplement normal surveillance**

ATTACHMENT 2

Design Considerations

Self Test System

- **Enhance failure detection capability**
  - — **Verify correct output for current state**
  - — **Verify correct output for any other state**
    - **All inputs**
    - **All logic and timing**
    - **All outputs**

Design Considerations

Self Test System

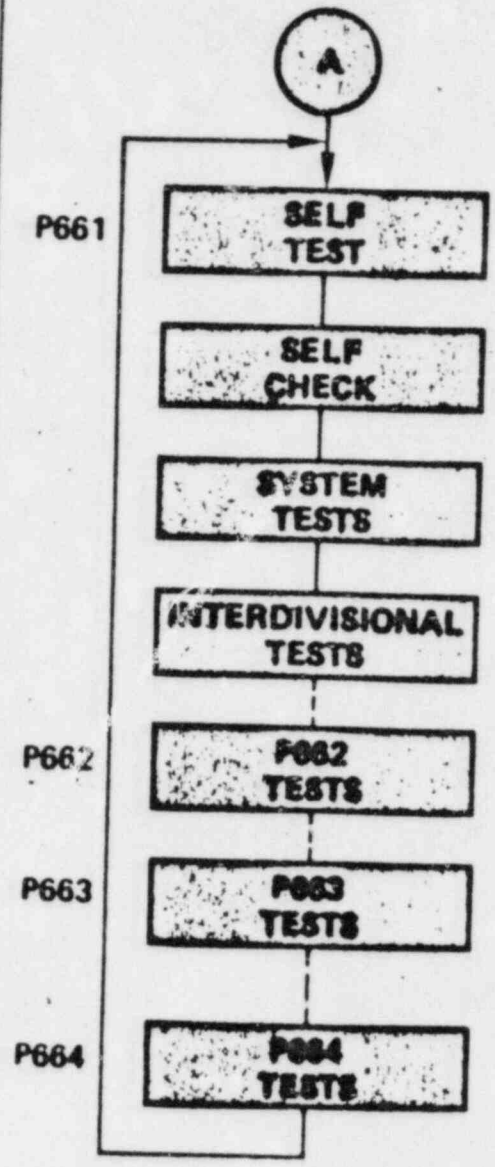
- **Shorten repair time**
  - **Automatic testing**
  - **Testing by request**
  - **Identify failed components**
  - **Provide supporting data**
  - **Verify repair**

Self Test System

- **No single failure of the Self Test System will prevent the functional logic from performing its required operation**
  - **Self Test System Circuitry decoupled from functional logic by current limiting resistors**
  - **Test Pulse A/C coupled in addition to hardware and software metering**

OPTICALLY COUPLED SOLID STATE RELAY

Automatic Test Sequence



PERFORMS TEST OF CPU, RAM, ROM

PERFORMS TEST OF UNIVERSAL I/O, SERIAL I/O, HARDWARE TIMERS, CARD SELECTORS, POWER MONITORS, CARD OUT OF FILE INDICATORS

PERFORMS TEST OF ALL SYSTEMS THAT DO NOT HAVE SIGNALS FROM OTHER DIVISIONS

PERFORMS TEST OF ALL SYSTEMS THAT HAVE INPUTS FROM OTHER DIVISIONS

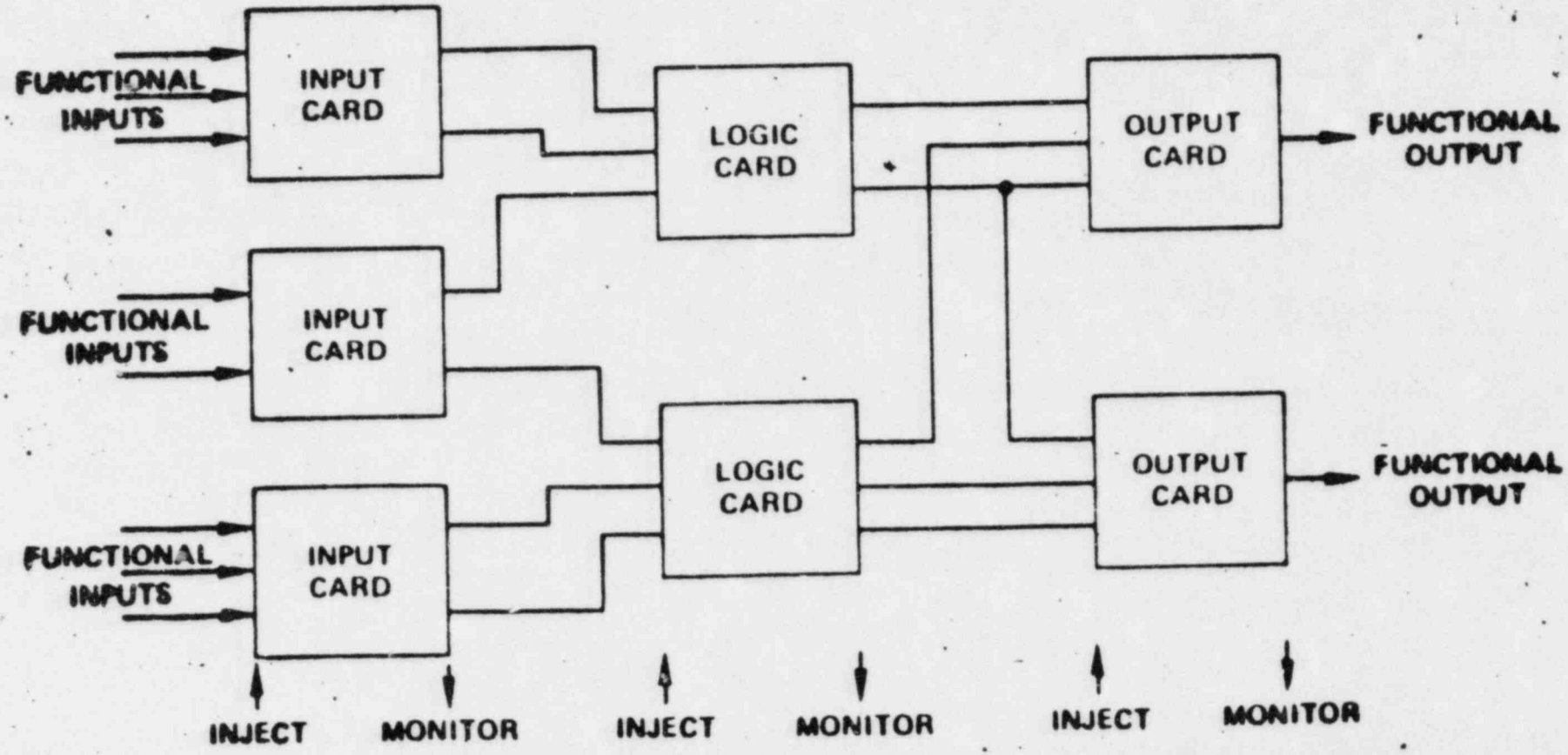
REPEAT ALL ABOVE

REPEAT ALL ABOVE

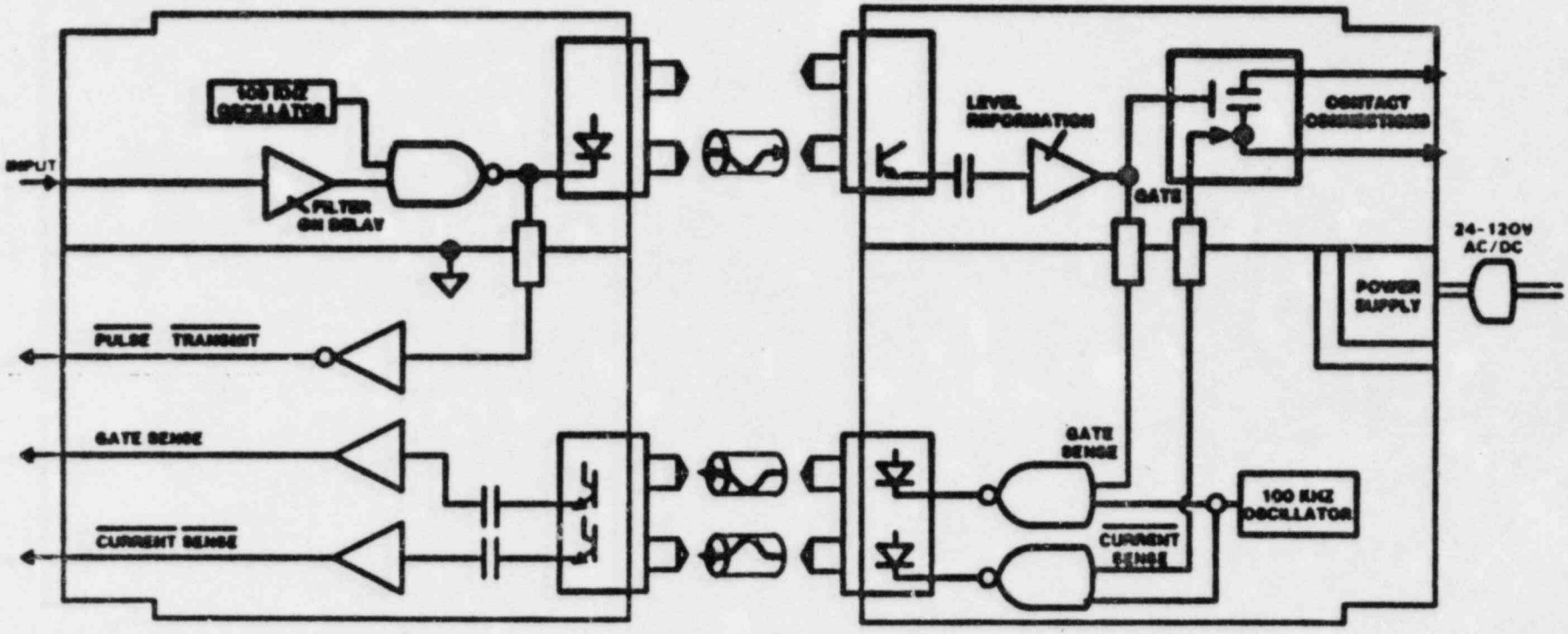
REPEAT ALL ABOVE

System Test Methodology

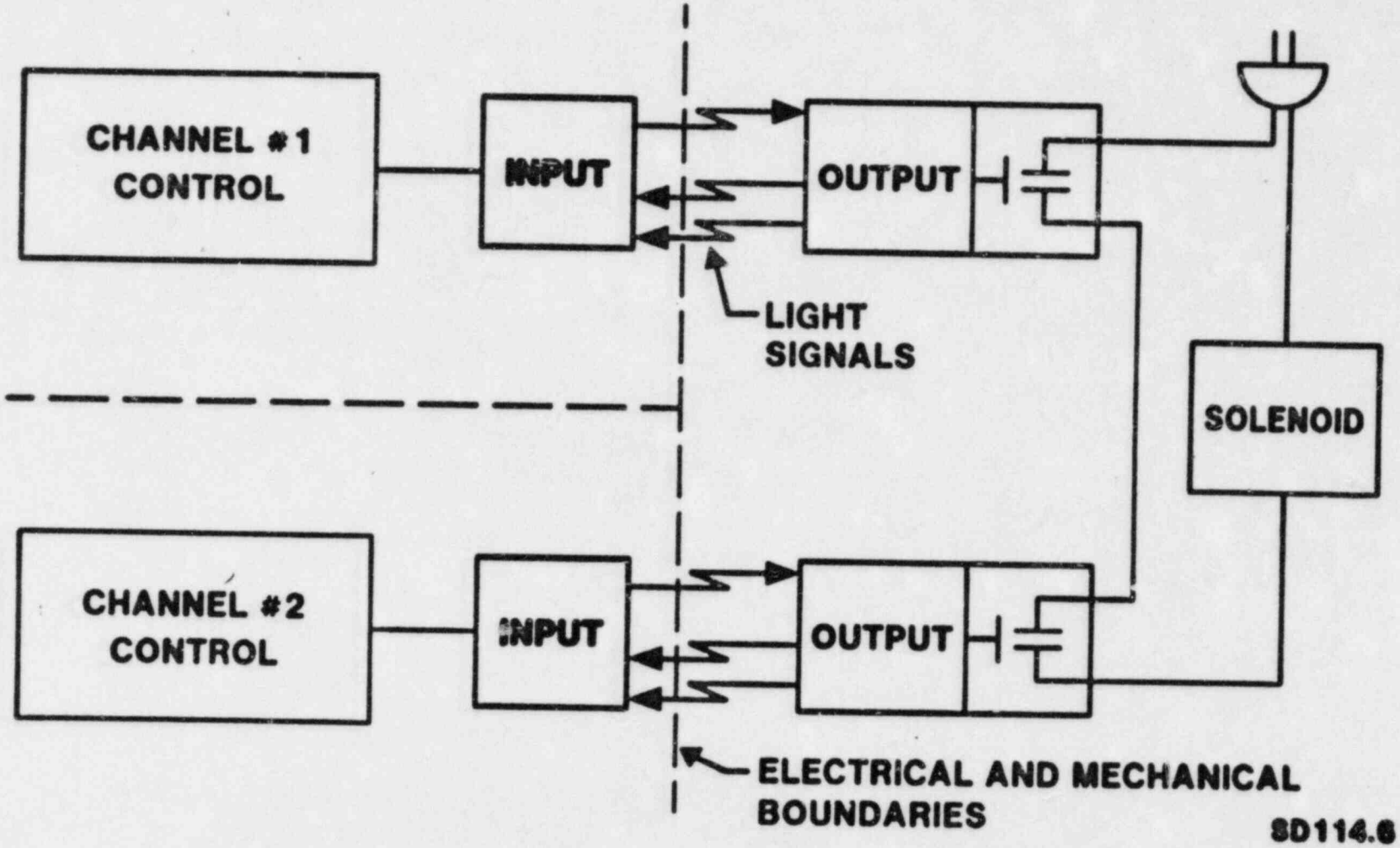
Within Division



BLOCK DIAGRAM



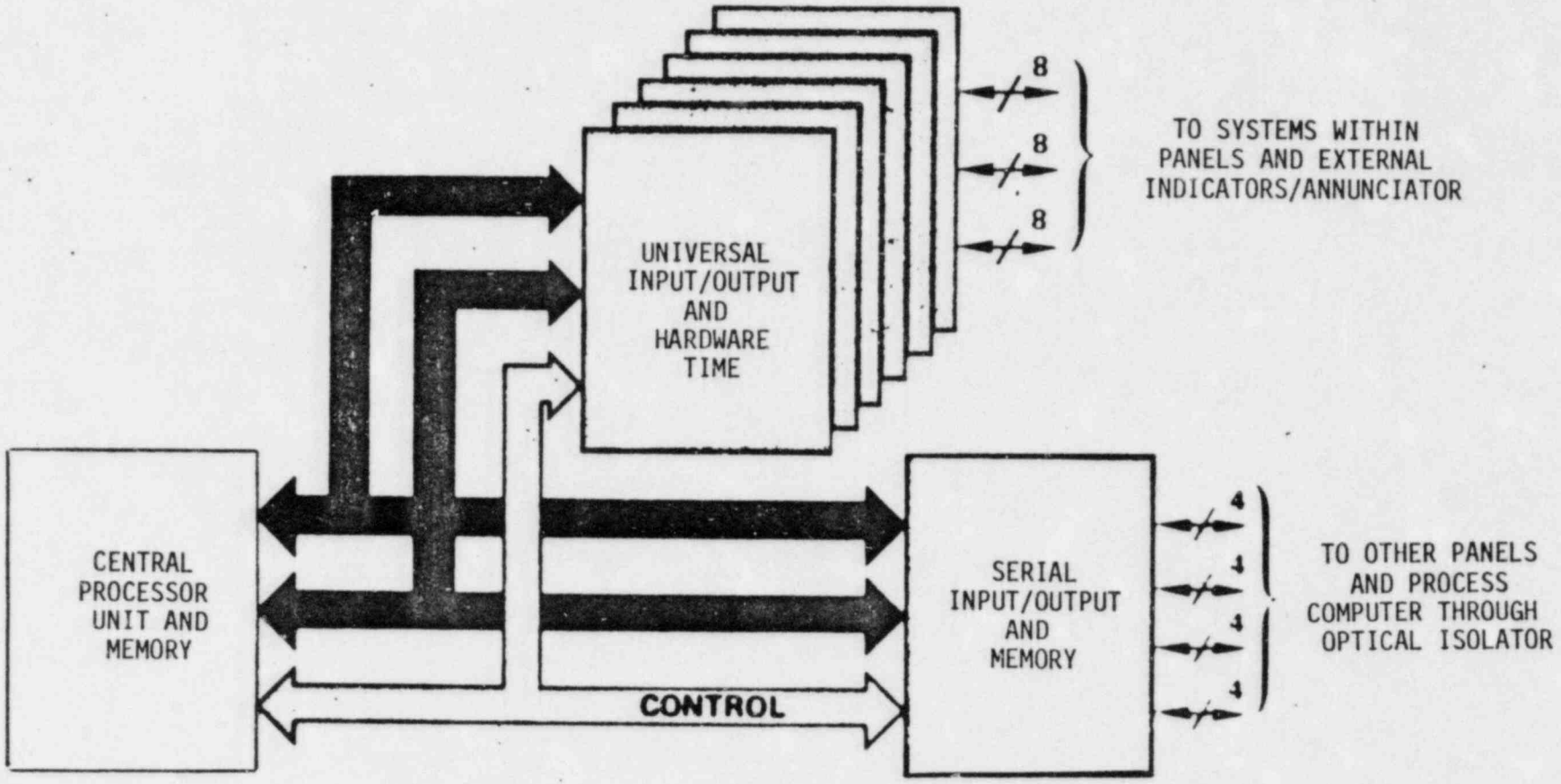
TYPICAL SYSTEM LEVEL USE



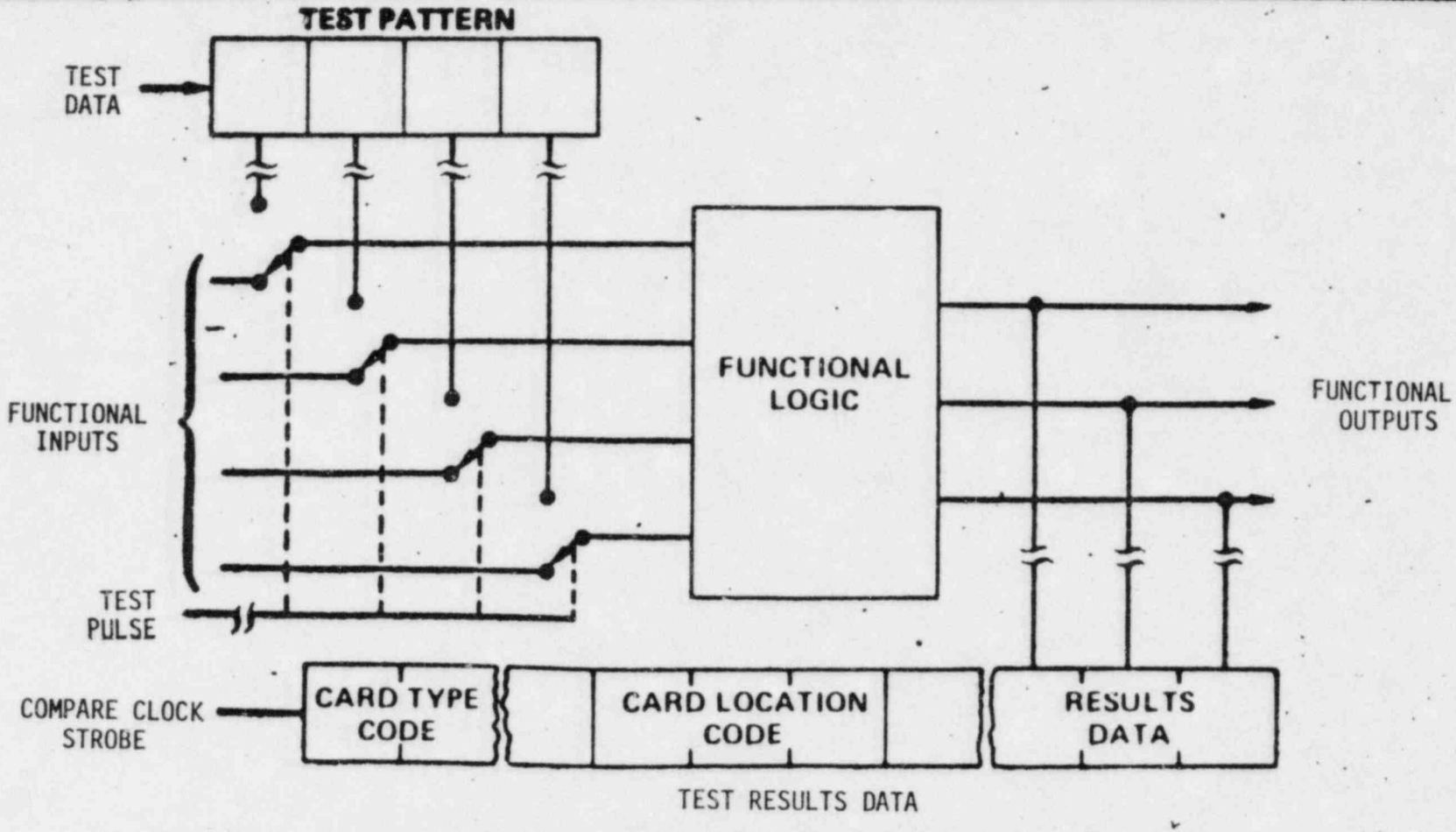
Panel Configuration

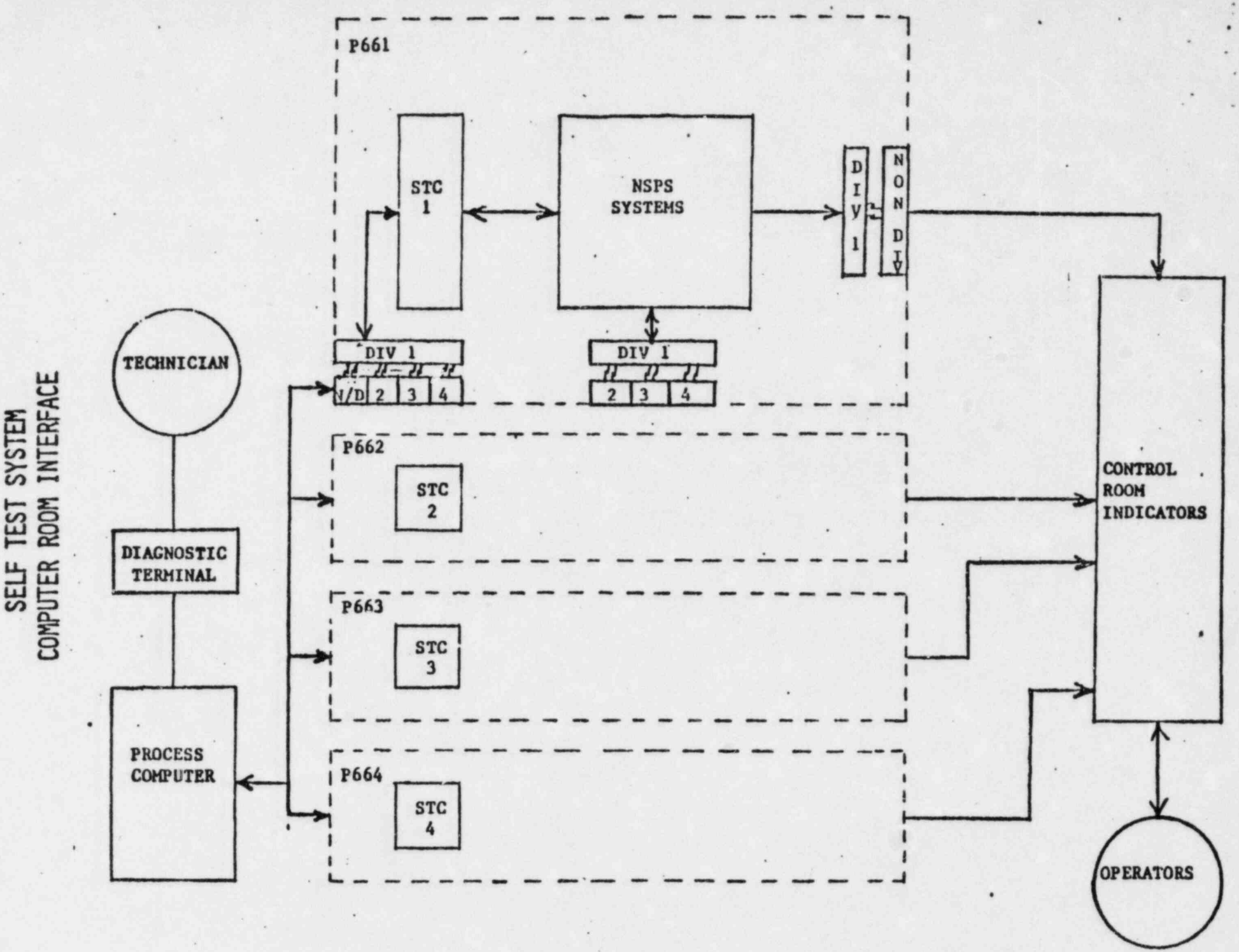
A	B	C	D
ISOLATOR BAY	INSTRUMENT BAY	LOGIC BAY	ISOLATOR BAY
	RPS (ATM)	RPS	
	NS4 (ATM)	RPS	
	HPCS (ATM)	STC	
	SPARE	NS4	
	SPARE	NS4	
		HPCS	
		MISC SYSTEMS	
		SPARE	
	REDUNDANT POWER SUPPLY MODULE	POWER SUPPLY MODULE	

Data Flow
Self Test System



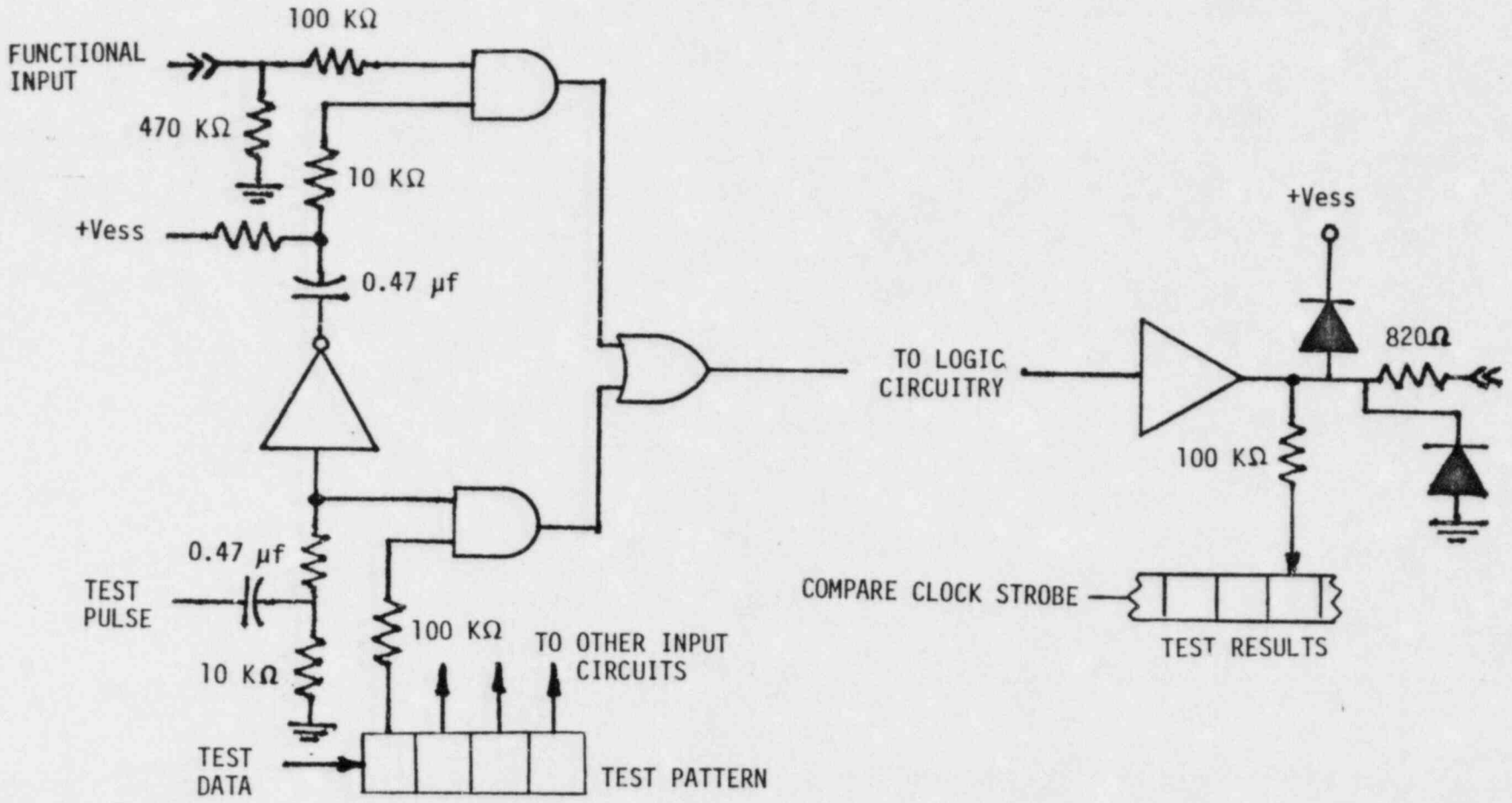
Representative Card Block Diagram
Self Test Interface



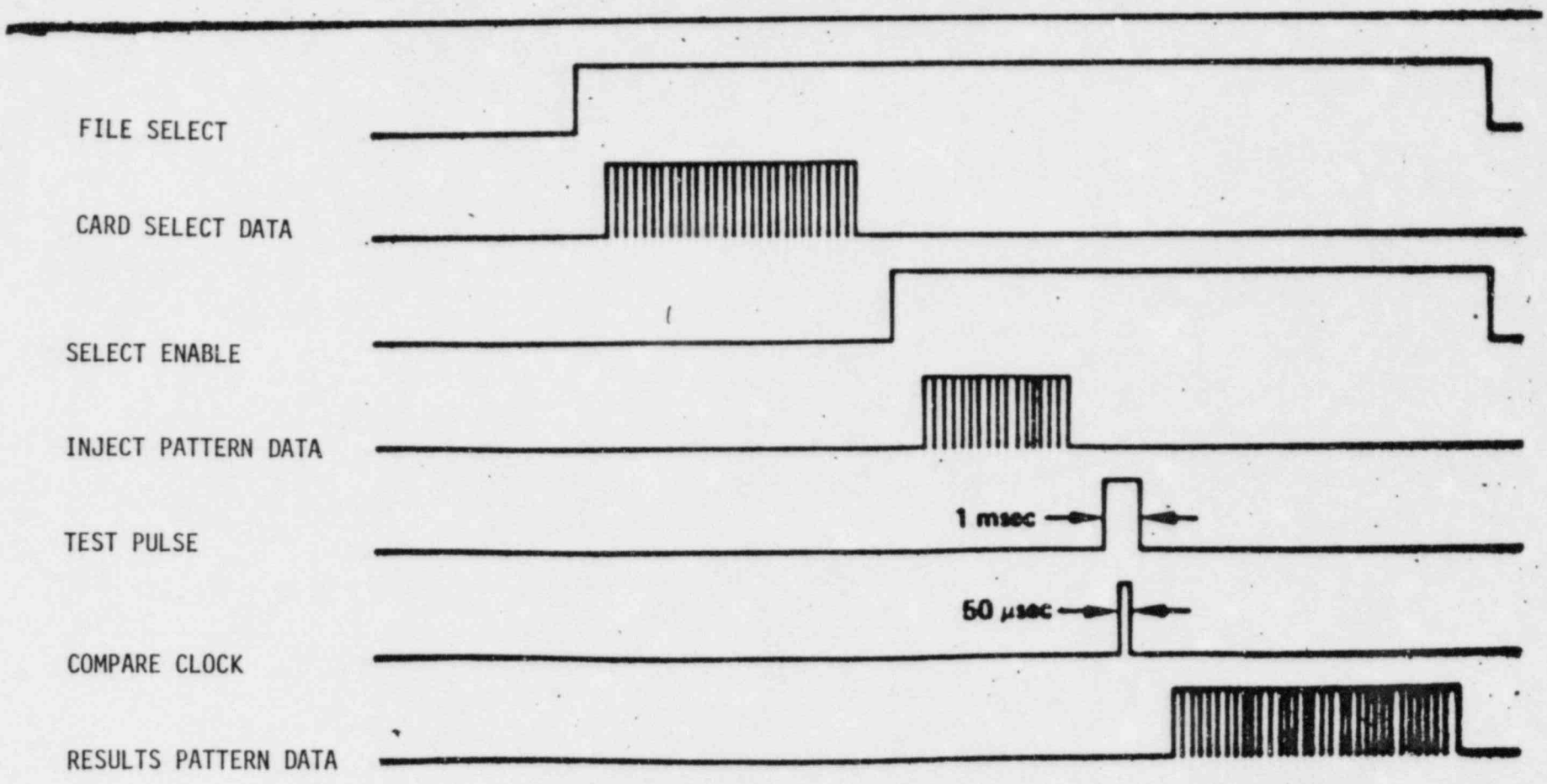

SELF TEST SYSTEM
COMPUTER ROOM INTERFACE
P661
STC 1
NSPS SYSTEMS
DIV 1
NON DIV
DIV 1
I/D 2 3 4
DIV 1
2 3 4
TECHNICIAN
DIAGNOSTIC TERMINAL
PROCESS COMPUTER
P662
STC 2
P663
STC 3
P664
STC 4
CONTROL ROOM INDICATORS
OPERATORS

Representative Card

Self Test Signal Isolation



Self Test Timing Diagram



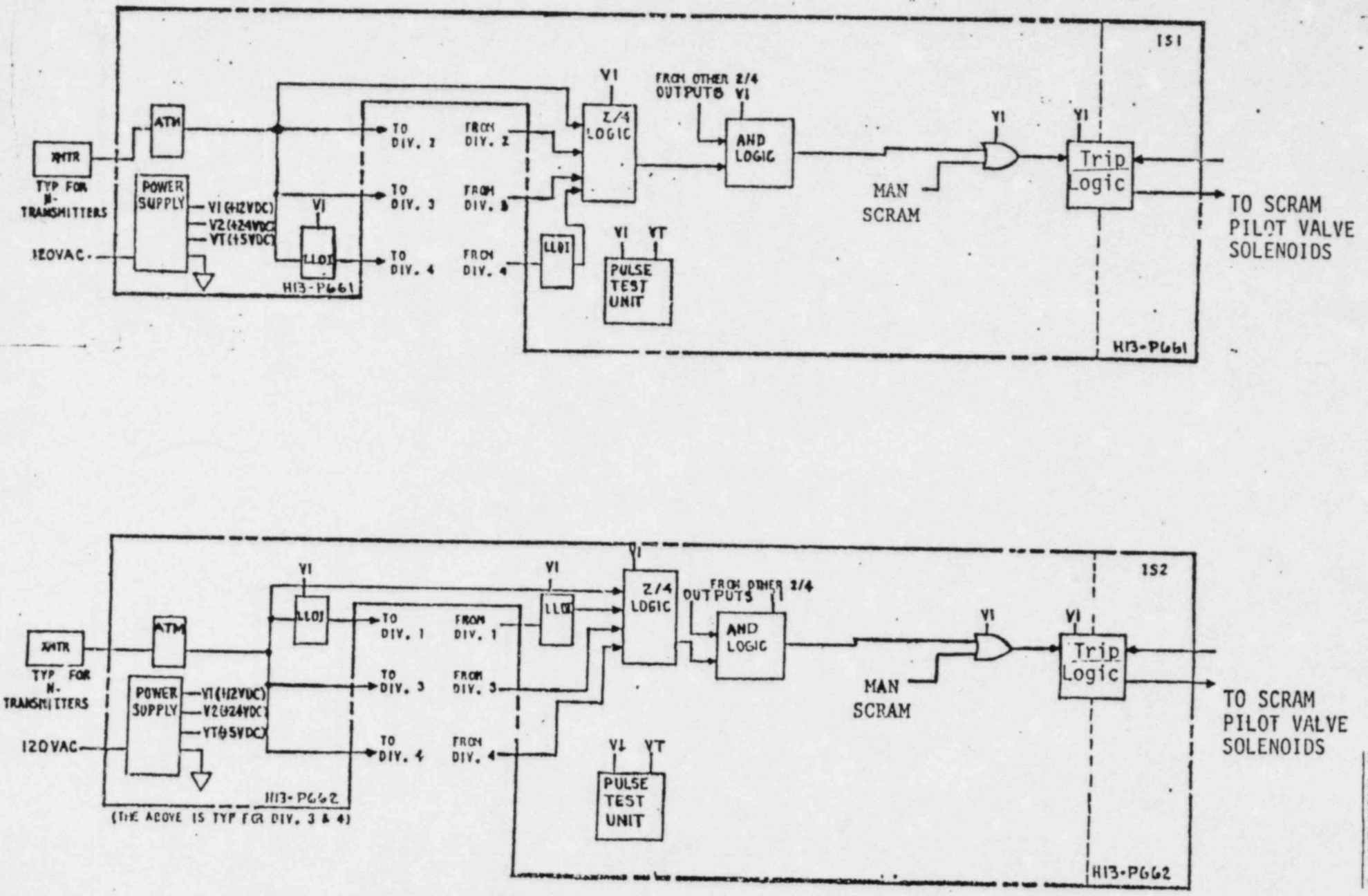
ATTACHMENT 3

USE OF THE STS TO SATISFY

TECHNICAL SPECIFICATION

SURVEILLANCE REQUIREMENTS

AT CLINTON



DIV 1	1A	2B	3B
DIV 2	1A	2A	3B
DIV 3	1B	2A	3A
DIV 4	1B	2B	3A

ATTACHMENT 3

C H A N N E L C H E C K

DEFINITION:

A CHANNEL CHECK shall be the qualitative assessment of channel behavior during operation by observation. This determination shall include, where possible, comparison of the channel indication and/or status with other indications and/or status derived from independent instrument channels measuring the same parameter.

SELF TEST SYSTEM ADVANTAGE:

Improves Qualitative Assessment of Channel Behavior

C H A N N E L C A L I B R A T I O N

DEFINITION:

A CHANNEL CALIBRATION shall be the adjustment, as necessary, of the channel output such that it responds with the necessary range and accuracy to known values of the parameter which the channel monitors. The CHANNEL CALIBRATION shall encompass the entire channel including the sensor and alarm and/or trip functions, and shall include the CHANNEL FUNCTIONAL TEST. The CHANNEL CALIBRATION may be performed by any series of sequential, overlapping or total channel steps such that the entire channel is calibrated.

SELF TEST SYSTEM ADVANTAGE:

Reduces Human Error During Setpoint Verification.

C H A N N E L F U N C T I O N A L T E S T I N G

DEFINITION:

A CHANNEL FUNCTIONAL TEST shall be:

a. Analog channels - the injection of a simulated signal into the channel as close to the sensor as practicable to verify OPERABILITY including alarm and/or trip functions and channel failure trips.

b. Bistable channels - the injection of a simulated signal into the sensor to verify OPERABILITY including alarm and/or trip functions.

The CHANNEL FUNCTIONAL TEST may be performed by any series of sequential, overlapping or total channel steps such that the entire channel is tested.

SELF TEST SYSTEM ADVANTAGE:

Supplements (by overlap) Manual Channel Functional Testing

L O G I C S Y S T E M F U N C T I O N A L T E S T I N G

DEFINITION:

A LOGIC SYSTEM FUNCTIONAL TEST shall be a test of all logic components, i.e., all relays and contacts, all trip units, solid state logic elements, etc., of a logic circuit, from sensor through and including the actuated device, to verify OPERABILITY. The LOGIC SYSTEM FUNCTIONAL TEST may be performed by any series of sequential, overlapping or total system steps such that the entire logic system is tested.

SELF TEST SYSTEM ADVANTAGES:

1. Systematically Tests All Logic Combinations at Reactor Power
2. Significantly Reduces the Potential for Human Error during Logic System Functional Testing
3. Reduces the Number of Operations of Safety Related Equipment

RESPONSE TIME TESTING

DEFINITION (RPS):

REACTOR PROTECTION SYSTEM RESPONSE TIME shall be the time interval from when the monitored parameter exceeds its trip setpoint at the channel sensor until de-energization of the scram pilot valve solenoids. The response time may be measured by any series of sequential, overlapping or total steps such that the entire response time is measured.

SELF TEST SYSTEM ADVANTAGES:

1. Systematically Demonstrates the Response Times of All Logic Combinations
2. Significantly Reduces the Potential for Human Error During the Performance of Logic Response Time Measurements
3. Reduces the Number of Operations of Safety Related Equipment

ATTACHMENT 4

DOCUMENTATION REQUIRED

FROM ILLINOIS POWER (CLINTON)

PRIOR TO STAFF ACCEPTANCE

OF THE NSPS / STS DESIGN

Prior to staff acceptance of the STS for satisfying Technical Specification surveillance requirements regarding the NSPS circuitry at Clinton, the following information should be provided by the applicant:

1) Confirmation that the STS was installed and operational prior to the qualification testing of the NSPS cabinets (including seismic testing) and functioned properly following completion of these tests.

2) Confirmation that interdivisional isolation between the STSs is provided by fully qualified one inch quartz optical isolation devices similar to those used throughout the NSPS.

3) A description of how the functional inputs (from the sensors) to the NSPS are blocked while the tests are being performed by the STS. A detailed discussion (beyond that of p7.2-22 of FSAR Amendment 9) of why the functional inputs cannot be blocked for longer than 1 msec should also be provided.

4) The exact portion of the NSPS circuitry which will be response time tested by the STS should be defined. A statement that the STS does not test the actual response time of the NSPS circuitry, but will demonstrate that the response time is less than a specific value (1 msec) should be provided. Also, the applicant should indicate that the various tests performed by the STS overlap sufficiently such that there remains no untested portion of NSPS circuitry.

5) A list of each control room annunciator point associated with the STS, what actuates each of these, and confirmation that these annunciator points cannot be cleared until the detected fault has been removed.

6) A brief discussion of how the STS performs a test on itself prior to starting the NSPS test sequence.

7) Confirmation that a structured methodology program for development and testing of the STS such as V&V has been followed and that documentation of this program is available for audit by the staff.

8) A discussion of the role of the plant computer in the STS design and confirmation that successful STS operation does not in any way depend on the plant computer.

9) A description of each STS test (including the portion of circuitry being tested) and how it is accomplished (e.g., current ramp versus current step when testing bistable operability/setpoints).

10) A discussion of how latching (seal in) circuits within the NSPS are tested by the STS.

11) STS test signals are capacitively coupled to the NSPS circuitry to block the NSPS functional inputs and to strobe test data through the NSPS circuits. A discussion of the effect on NSPS and STS performance given the failure of either and both of these capacitors and the potential for a large number of undetected capacitor failures over a period of time for adversely affecting the NSPS or STS should be provided. An indication of whether test plans exist or are being developed to test these capacitors should be provided.

ATTACHMENT 5

CLINTON / GESSAR

NUCLEAR SYSTEM PROTECTION SYSTEM / SELF TEST SYSTEM

MEETINGS OF JANUARY 11TH AND 12TH, 1983

LIST OF ATTENDEES

Attendees: January 11 & 12, 1983

General Electric Co.

Paul Scherer
Arnold Koslow
Lyle McCready
Brad Erbes
Fletcher Downey
Dave Hill
Bob Strong
Garrett O'Brien

Illinois Power Co.

John O'Brien
John Cook
Joe Miller
George Wuller
Aaron Valdivia

NRC

Ernie Rossi
Dino Scaletti
Marty Virgilio
Harvey Ableson
John Elsbergas (ANL)
Rick Kendall

The following additional attendees were present on January 12, 1983 only:

General Electric

D. Krueger
Jon Kwong

C.F. Braun

Baneij Basu
Ed Willingham