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POWER AUTHORITY OF THE STATE OF NEW YORK

10 COLUMBUS CIRCLE NEW YORK, N. Y. 10019

(212) 397-6200

November 17, 1978
JNRC-78-59

Director of Nuclear Reactor Regulation
United States Nuclear Regulatory Commission
Washington, D. C. 20555

Attention: Mr. Thomas A. Ippolito
Operating Reactors Branch No. 3
Division of Operating Reactors

Subject: James A. FitzPatrick Nuclear Power Plant
Additional Information For Proposed
Technical Specification Change
Docket No. 50-333

Dear Sir:

Transmitted herewith are our responses to your letter dated September 13, 1978 which requested additional information concerning proposed changes to the Technical Specifications, Reload 2 Licensing Submittal for Cycle 3 operation.

Very truly yours,

Paul J. Early
Assistant Chief Engineer-
Projects

Att.

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ADDITIONAL INFORMATION

CONCERNING PROPOSED CHANGES TO TECHNICAL SPECIFICATIONS FOR THE JAMES A. FITZPATRICK NUCLEAR POWER PLANT

Question 1A: Provide logic and wiring diagrams for the changes to the flow referenced and fixed high neutron flux scram systems.

Response: Logic and wiring diagrams are attached as Attachment A.

Question 1B: Demonstrate qualification of these systems to the IEEE 279 standards.

Response: The neutron monitoring system for the James A. FitzPatrick Nuclear Plant (JAFNPP) has several subsystems of which the Average Power Range Monitoring (APRM) subsystem is one. The APRM subsystem was augmented to include the Simulated Thermal Power Trip (STPT). The APRM subsystem has six (6) APRM channels, each using input signals from a number of LPRM channels. Three APRM channels are associated with each of the trip systems of the Reactor Protection System. The APRM subsystem is designed to meet the requirements of IEEE-279 (from JAFNPP FSAR #7.5.7.3). The STPT augments each of the six (6) APRM channels such that each APRM channel has a 120% neutron flux trip whose setpoint is not recirculation flow biased. The new thermal power upscale trip has a setpoint that is flow biased and is obtained by filtering the APRM signal to obtain a signal which represents the thermal flux of the fuel.

This time delay is accomplished by conditioning the APRM neutron flux through a first order low pass filter that has a six (6) second RC time constant. Since each of the six (6) APRM channels was identically modified to add the STPT and the independence between the six (6) APRM channels was not altered, the redundancy requirements of IEEE 279 are still maintained.

Question 2: Provide analyses which demonstrate the adequacy of the revised scram systems logic at low power conditions for the loss-of-feedwater heating transient and rod drop accident.

Response: The adequacy of the revised scram systems logic at low power conditions for a loss-of-feedwater heating transient and the rod drop accident is shown in the following discussions:

Loss-of-Feedwater Heating Transient

As load is reduced from rated power, the decrease in steam flow and feedwater flow results in a lower temperature rise across any given feedwater heater. Taking this inherent feature into consideration, the loss-of-feedwater heater transient at low power results in smaller core sub-cooling changes associated with the loss-of-feedwater heating than for the same transient at a higher power. Therefore, the change in the critical power ratio (Δ CPR) decreases with decreasing power, thus the difference between the safety limit and the transient MCPR increases with decreasing power irrespective of any scram systems logic. In addition, at any given recirculation loop flow rate, the Simulated Thermal Power Trip (STPT) logic is designed to maintain a relatively constant margin between the reactor power and the STPT setting. This margin or power difference between the reactor power and the thermal power trip setting is specified by the STPT setpoint specification:

$$S \leq \text{minimum of } \begin{cases} 0.66w + 54\% \text{ or} \\ 117\% \end{cases}$$

where "w" is the recirculation loop flow rate in percent of rated. This specification requires that the STPT setpoint be reduced as the recirculation loop flow rate (and hence reactor power) is reduced.

The APRM STPT setpoint specification in the Technical Specifications therefore assures the adequacy of the STPT scram logic at low power conditions for a loss-of-feedwater heating transient.

The characteristic decrease in ΔCPR with decreasing power, and the reduction in APRM STPT setpoint with decreased recirculation loop flow (and hence reactor power), both act to assure that the fuel cladding integrity Safety Limit is not violated during the loss-of-feedwater heating transient at less than rated power.

As an additional point of interest, at less than rated recirculation loop flow ($w < 100\%$), the K_f factor increases the operating limit. This is to assure that the Safety Limit is not violated during events which produce a larger ΔCPR from low power conditions than from rated power. Examples of such events are the inadvertent startup of an idle recirculation pump, recirculation flow controller failure (increasing flow), feedwater controller failure (maximum demand), and rod withdrawal error.

Further, since the ΔCPR during a loss-of-feedwater heating event is less at low power than at rated power, the increased operating limit (due to the K_f factor) at less than rated recirculation loop flow provides even more margin between the Safety Limit and the transient MCPR than exists at rated power. These factors assure that the fuel cladding integrity safety limit is not violated during the loss-of-feedwater heating transient at less than rated power.

Rod Drop Accident

A description of the control rod drop accident is presented in Section 5.5.1 of General Electric Company's BWR Generic Reload Fuel Application Licensing Topical Report, NEDO-24011-P-A, March 1978. The analysis of this event (Page 5-40)

assumes that when the control blade falls from the fully inserted to the fully withdrawn position, the reactor is subjected to a relatively short period and the initial power transient is terminated by the doppler reactivity feedback in $\leq$ 1 second. The transient causes a reactor scram on APRM 120% neutron flux. The APRM STPT trip is not expected to occur because the transient time is less than the time delay associated with the STPT trip point. Therefore, the APRM STPT has no effect on the control rod drop accident from any reactor power level.

Question 3: Provide the effect on Δ CPR of the change in SRV setpoint to the results of the load rejection without bypass.

Response: An analysis was performed for the postulated load rejection incident with failure of the bypass valve using new SRV setpoints. The result shows that the operating limit Minimum Critical Power Ratios for 7x7 and 8x8R fuel types have decreased by 0.01. These changes are given in NEDO-24129-1, Supplement 1, and have been incorporated into the proposed Technical Specifications on Page 30. This page was transmitted to the Commission on October 13, 1978. The result of this analysis demonstrate the ability of the plant to operate safetly within the constraints of the calculated safety limits.

Question 4: Provide criteria similar to that of the Standard Technical Specifications 4.2.1 for time to measure MFLPD in your specification 4.1.B, i.e., change of power, etc.

Response: The Authority would agree to adopt criteria similar to that of the Standard Technical Specifications 4.2.1 for time to measure MFLPD. Therefore, the proposed specification 4.1.B which the Authority transmitted to the Commission on Aug. 18, 1978 would then read:

B. Maximum Fraction of Limiting Power Density (MFLPD)

The MFLPD shall be determined:

a. At least once per 24 hours,

b. Whenever THERMAL POWER has been increased by at least 15% of RATED THERMAL POWER and steady state operating conditions have been established, and

c. Initially and at least once per 12 hours when the reactor is operating with a LIMITING CONTROL ROD PATTERN for MFLPD.

Question 5: Concerning the spectrum of postulated fuel loading errors, either show that any fuel loading error is detectable by the available nuclear instrumentation and hence remediable prior to fuel failures, or show that the consequences of any fuel damage will remain a small fraction of the 10 CFR 100 guidelines.

The staff currently considers it sufficient if the operating reactor adjusts the operating limit MCPR such that the core wide safety limit MCPR will not be violated for the worst case fuel loading error.

In our May 1978 SER on NEDE-20411P, we have approved alternate fuel loading error analyses, subject to the conditions specified therein. Please state whether your fuel loading analysis is the original model, or one of the alternates.

Response: During the last refueling outage in 1977, the Authority lowered the setpoint of the off-gas radiation monitor as a solution with regard to a fuel loading error. The likelihood of fuel loading error is mitigated by the existing fuel loading procedures; that is, two different verifications of correct loading with the proper orientation is performed. In addition, following the completion of fuel loading, the core is verified by a visual inspection and the actual loading is recorded on video tape and compared with the intended loading pattern, and again, checked for proper fuel bundle

orientation. Therefore, the Authority believes that adequate protection against fuel loading errors already exist. In any case, the Authority has requested General Electric Company to perform the Fuel Loading Analysis using one of the alternate analyses approved by the Nuclear Regulatory Commission in May of 1978. The results of this analysis will be available in the near future and will be transmitted to the Commission as soon as we receive it from General Electric.

As indicated in the telephone conversation with Marvin Mendonca of the Commission in September of 1978, this alternate analysis will allow the setpoint for the off-gas radiation monitor to be returned to the value used during Cycle 1 operation of the James A.FitzPatrick Nuclear Power Plant following approval of the analysis by the Commission.

ATTACHMENT A

LOGIC AND WIRING DIAGRAMS
FOR THERMAL POWER MONITORING SYSTEM

OPERATION AND MAINTENANCE INSTRUCTIONS THERMAL TRIP UNIT 195B9074AAG1

GEK-45878A
FEB. 1977

SECTION I

DESCRIPTION AND THEORY OF OPERATION

1-1 DESCRIPTION

1-2 The Thermal Trip Unit (195B9074AAG1) is used in the neutron monitoring system. The thermal trip unit provides latching and non-latching thermal trip outputs plus either a "thermal first" or a "neutron first" latching trip output. After the trip condition is cleared, the latching trip must be reset; the non-latching trip automatically resets.

1-3 The thermal trip unit consists of transistors, integrated circuits, and other circuit components packaged in a plug-in, printed circuit card (module) which is mounted in a vertical position in its file, and is removable by means of a nylon retainer-ejector mounted on the lower exterior corner of the card.

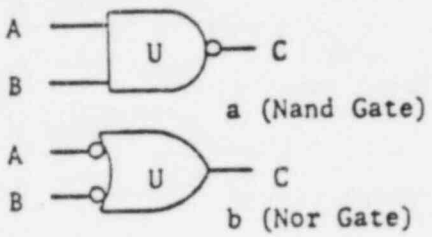
1-4 This manual presents the theory of operation, troubleshooting, and repair information for the thermal trip unit. Assembly drawings, elementary diagram, and parts lists are included in Section III of this manual. For an overall explanation of the thermal trip unit function refer to the theory of operation in the power range neutron monitoring system manual.

1-5 THEORY OF OPERATION

1-6 Logic Circuits. The following paragraphs describe the logic circuits used in this module.

1-7 Nand Gates and Nor Gates. The Nand gates used are quadruple 2-input positive Nand gate integrated circuits. Since there are four Nand gates to an integrated circuit component, the same designation may appear up to four times on the schematic diagram. Refer to Figure 1-1a. Only when input A and input B are both logical one's (ONE's) is the output from U a logical zero (ZERO). Figure 1-1a, a Nand gate, is logically equivalent to Figure 1-1b,

a Nor gate, since $\overline{AB} = \overline{A} + \overline{B}$ but functionally Figure 1-1a implies we are looking for a low output, while Figure 1-1b implies we are looking for a high output. The Truth Table is shown below and can be functionally represented by either of the two symbols.

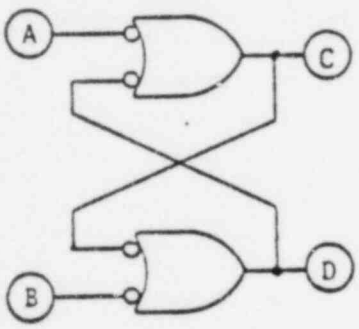


TRUTH TABLE

INPUT A	INPUT B	OUTPUT C
1	1	0
1	0	1
0	1	1
0	0	1

Figure 1-1. Nand Gate, Nor Gate, And Truth Table

1-8 The Reset Set or RS Flip-Flop. Refer to Figure 1-2. Figure 1-2a is the way the RS flip-flop appears on the schematic diagram, and Figure 1-2a is a summary of the input signals and resulting states of the flip-flop (at the C output).



(a)

INPUT SIGNAL A or Set	INPUT SIGNAL B or Reset	STATE OF FLIP-FLOP (C OUTPUT) Initial	Resulting
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	1
0	1	0	1
0	0	1	Both C and D Outputs are ONE's
0	0	0	

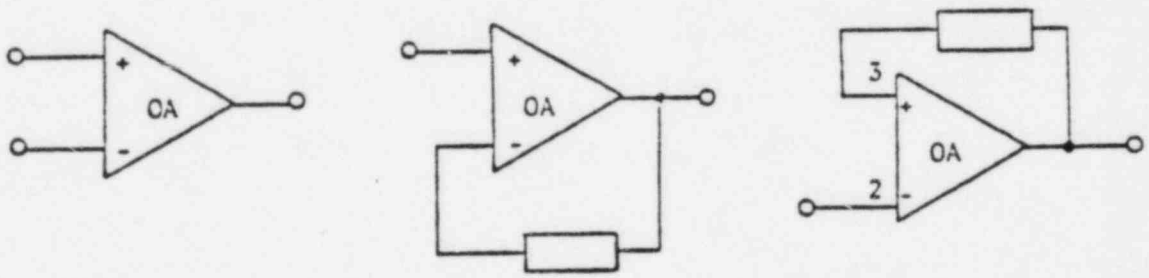
(b)

Figure 1-2. The Reset Set or RS Flip-Flop

1-9 Operational Amplifier Circuit. (See Figure 1-3a.) Operational amplifiers are basically high gain, high input impedance, low output impedance, direct coupled amplifiers which use external feedback for control of response characteristics. If we first consider a typical operational amplifier, OA, without the feedback connection, it has two inputs, one inverting and the other non-inverting. This characteristic means that if a negative signal is applied to only the (+) input, the output will swing negative. Similarly, with a negative signal connected to only the (-) input, the output will swing positive. We can further see that if the same signal voltage is applied at the same time to the (+) and (-) outputs, the output will not change, it will stay zero.

1-10 Consider the operation of OA with its output connected back to the (-) input, as shown in Figure 1-3b. The application of negative feedback around OA causes the difference in voltage between the (+) and (-) inputs to approach zero. With a negative input to the (+) terminal, the output is negative and the feedback voltage to the (-) terminal for all practical purposes equals the (+) terminal input. In this case the operational amplifier operates as a voltage follower. This is the configuration of AR1 on the schematic diagram.

1-11 Next consider the operation of OA with its output connected back to the (+) input, as shown in Figure 1-3c. In this configuration the circuit has infinite gain. The smallest difference in potential between the two inputs is sufficient to drive the output of OA to its maximum (±) potential. If pin 3 is more negative than pin 2, the output from OA is maximum negative. If pin 2 is more negative than pin 3, the output from OA is maximum positive (used as a trip output). In this case described OA is used as a comparator, which is the configuration of AR2 on the schematic diagram.



1-3a 1-3b 1-3c

Figure 1-3. Operational Amplifier Configurations

1-12 Block Diagram Theory of Operation. For convenience we start at Reset. Reset is a ZERO input, which resets all the RS flip-flops to the state where their lower outputs are ONE'S, their upper outputs are ZERO'S. In this condition, assuming no trip inputs, transistor Q1 is conducting, and transistors Q2, Q3, and Q4 are cut off. There are two possible trip inputs to the thermal trip unit, the APRM Input and the Fixed Scram. One trip will occur before the other. If the APRM trip occurs first, the outputs are: a Non-Latching trip output, a Latching trip output, and the external indicator associated with the transistor Q3 circuit lights. This same APRM trip prevents the external indicator associated with transistor Q4 from lighting. On the other hand, if the Fixed Scram trip occurs first, the external indicator associated with transistor Q4 lights and this same trip prevents the external indicator associated with transistor Q3 from lighting. The following paragraphs discuss this logic in greater detail.

1-13 APRM Trip. The APRM Input is a negative voltage in the range of 0 to -10 volts. The reference voltage is also a negative voltage. Operational amplifier AR1 is a voltage follower with unity gain, which has a low pass filter with a 6 second RC time constant at its APRM Input. The output from operational amplifier AR1, a negative voltage, is applied to one input of comparator AR2. If this input is more negative than the reference input to AR2, then the output from AR2 immediately goes to its maximum positive value, placing a ONE on one input to Nand gate U1. The other input to Nand gate U1 (unless an Inhibit signal, ZERO, is present) is always a ONE, so with both inputs ONE, the output from Nand gate U1 is a ZERO.

1-14 This ZERO through two Nand gates cuts off transistor Q1, generating the non-latching trip output. This same ZERO causes RS flip-flop U3 to go to its tripped state; its top output goes to a ONE; its bottom output goes to a ZERO. Its bottom output causes transistor Q2 to conduct, generating the latching output. Its top output is a ONE, and this ONE is applied to Nand gate U1. Assume that the APRM trip occurs first (before the Fixed Scram trip). Since in the reset condition the lower output from all the RS flip-flops is a ONE, we have two ONE inputs to the Nand gate U1 controlling the middle RS flip-flop (U3, U3). Nand gate U1's output goes to a ZERO, and the RS flip-flop goes to its tripped state, so transistor Q3 conducts and the externally located indicator lights. Suppose that after this indicator lights, that RS flip-flop U4 trips, providing a ZERO input to Nand gate U1. This does not cause the middle RS flip-flop (U3, U3) to change state, so the external indicator remains lighted.

1-15 Fixed Scram Input. Suppose that the Fixed Scram input goes to a trip condition first (before the APRM Input). The Fixed Scram trip input, a ONE, causes the top output of RS flip-flop U4 to go to a ONE, and the bottom output to go to a ZERO. The output from RS flip-flow U4 causes transistor Q4 to conduct and this causes the associated indicator to light. The ZERO

output from RS flip-flop U4 is also applied to the Nand gate U1 controlling the middle RS flip-flop (U3, U3), and this flip-flop is now locked in its reset state by this action, so transistor Q3 can't conduct, and the externally associated indicator remains extinguished.

1-16 Inhibit Input. The inhibit signal is a ZERO. ZERO to Nand gate U1 controls U1 so that the inhibit signal holds the Q1 transistor circuit untripped and prevents the Q2 transistor circuit from tripping. If the Q2 transistor circuit is already tripped, the inhibit signal will not affect it; it remains tripped. If the Reset signal (ZERO) is now applied, the Q2 transistor circuit resets and the inhibit signal prevents it from tripping.

1-17 Reset. The Reset signal is a ZERO which resets all trip circuits associated with RS flip-flops.

SECTION II

TROUBLESHOOTING

2-1 GENERAL

2-2 Malfucntions of plug-in modules are normally isolated by module substitution. When a malfunction has been isolated to the thermal trip unit, remove it from its file in the page and perform the troubleshooting procedures listed in Table 2-1. Test equipment used for troubleshooting the thermal trip unit should be equivalent to the following:

Digital Voltmeter, Dana 5000 with options 44 and 54.

2-3 ADJUSTMENTS

2-4 There are no adjustable components in the thermal trip unit.

CAUTION

Do not use acid or any other corrosive material as a cleaning agent or soldering flux when making electrical or electronic solder joints.

Table 2-1. Thermal Trip Unit Troubleshooting Procedures

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL INDICATION	REMEDY
1.	Connect power to the thermal trip unit.	N/A	N/A	N/A
2.	Connect -3 volts to Ref. input and an adjustable negative 0-10 volts to the APRM Input.	N/A	N/A	N/A
3.	Vary the APRM Input. Using a dvm, monitor the output at pin six (6) of AR1.	Same as input. (Wait for about 10 time constants-a minute-after each change.)	Defective AR1.	Replace AR1.
4.	Monitor the voltage at the inputs to AR2 (using dvm). Adjust the APRM Input at this point to a slightly more positive (less negative) value than the Ref input. Be sure to allow for hysteresis. Using a dvm, monitor the output from AR2.	Max negative.	Defective AR2.	Replace AR2.
5.	Momentarily ground Reset input. Using a dvm, measure the outputs at P1-19, P1-20, P1-21, P1-22 (after the ground is removed).	(An open is a ONE) P1-19...ZERO P1-20...ONE P1-21...ONE P1-22...ZERO	Defective Nand gates, defective transistor circuits.	Replace defective component.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL INDICATION	REMEDY
6.	Monitor the voltage at the inputs to AR2 (using dvm). Adjust the APRM Input at this point to a slightly more negative value than the Ref input. Using a dvm, monitor the output from AR2.	Max positive.	Defective AR2.	Replace AR2.
7.	Connect temporary ground clips to Inhibit, Fixed Scram, and Reset inputs. Using dvm, monitor outputs at P1-19, P1-20, P1-21, P1-22.	(An open is a ONE) P1-19...ZERO P1-20...ONE P1-21...ONE P1-22...ONE	Defective Nand gates, defective transistor circuits.	Replace defective component.
8.	Remove temporary ground clip from	P1-19...ONE P1-20...ONE	Defective Nand gates, defective transistor circuits.	Replace defective component.

Table 2-1. Thermal Trip Unit Troubleshooting Pro

Table 2-1. Thermal Trip Unit Troubleshooting Procedures (Continued)

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL INDICATION	REMEDY
10.	Connect temporary ground clip to Inhibit input. Remove temporary ground clip from Fixed Scram input. Momentarily ground Reset input. Using dvm, monitor outputs at P1-19, P1-20, P1-21, P1-22.	P1-19...ZERO P1-20...ONE P1-21...ONE P1-22...ZERO	Defective Nand gates, defective transistor circuits.	Replace defective component.
11.	Remove temporary ground clip from Inhibit input. Using dvm, monitor outputs at P1-19, P1-20, P1-21, P1-22.	P1-19...ONE P1-20...ZERO P1-21...ONE P1-22...ZERO	Defective Nand gates, defective transistor circuits.	Replace defective component.

SECTION III

REFERENCE DATA

3-1 GENERAL

3-2 Table 3-1 lists the parts list, assembly drawing, and elementary diagram for the thermal trip unit 195B9074AAG1 in the order of presentation.

Table 3-1. Reference Drawings

TITLE	DRAWING NUMBER
Thermal Trip Unit Assembly Drawing and Parts List	195B9074AAG1
Elementary Diagram	127D1787AA

3-3 SPARE PARTS PROCUREMENT

3-4 The component descriptive data shown on the elementary diagram reflects the components that were contained in the original design. Component changes may have been made since that time as a result of component standardization programs. When parts are being replaced, refer to the applicable parts list of the correct replacement part. The parts list will identify the parts by either an industry standard number (such as 2N697) or by a U.S. Government Federal Specification number (such as MS3102A-16S-1S) or by General Electric part number (such as 117C2368P2). Parts identified by industry standard or U.S. Government Specification numbers can be locally procured if desired. A cross reference between G.E. part numbers and the applicable vendor and catalog number, industry standard number, or Federal Specification number for standard parts is furnished in GEG-21406. (GEG-21406 also shows the correct G.E. part number for a replacement part in cases where the original G.E. part numbers have been superseded by another part number.) Parts may be procured locally if desired. All replacement parts should be ordered from the General Electric Co. by G.E. part number. Parts ordered should be addressed as follows:

General Electric Co.
Nuclear Energy Division
175 Curtner Avenue
San Jose, California 95125

ATTN: NUCLEAR ENERGY MARKETING DEPARTMENT
SPARE AND RENEWAL PARTS

REVISION STATUS SHEET

GENERAL ELECTRIC

NUCLEAR ENERGY DIVISION

DOCUMENT NO. PL195B9074AA REV. 2

APPLICATION PEM CABINET

FCF 145C3096BB

☐ SPECIFICATION ☒ DRAWING ☐ OTHER _____ TYPE _____

DOCUMENT TITLE THERMAL TRIP UNIT

LEGEND:

REVISIONS			
2	B Fraasch Dec 26-73 G. FRAASCH CONVERTED TO EIS FORMAT E EN718792	RRS	

DESCRIPTION OF GROUPS	PRINTS TO
	A13
	6
	57
	69
	23

MADE BY G.FRAASCH Dec 10,73

ISSUED B.SUGGS B Suggs Dec 26-73

APPROVALS 12-11-74 J. Kwong J. KWONG

BWRS DEPT.

SAN JOSE LOCATION

PL.195B9074AA

CONT. ON SHEET 2 DR. NO. 1

A1

FTC

GENERAL ELECTRIC

BOILING WATER REACTOR SYSTEMS DEPARTMENT, SAN JOSE, CA

TITLE: THERMAL TRIP UNIT

PL 1958907-4AA | SECT A | REV 7

ITEM NO	ALT	DOCUMENT TYPE	DESCRIPTION NAME	DESCRIPTION IDENTIFICATION	DOC STA	E C	C C	GROUP NUMBER AND QUANTITY 0001	U/M	SRC	SPA	ACT.
001		SCHEM DIAG	THERMAL TRIP UNIT	127D1787AA				1			NO	
002			PC BOARD	1958907-3PCP001				1				ENG
003			RETAINER	175A3197P001				1				
004			INTEGRATED CIRCUIT	176A1664P946				4				
005			INT CIRCUIT	225A4820P001				1			B	
006			CAPACITOR (TYPE CSR13)	112C2642P038				3				
007			CAPACITOR	175A7453P002				4				ENG
008			CAPACITOR	175A7453P004				1				
009			CAPACITOR	175A7452P003				1			B	
011			RESISTOR,FIXED COMP	117C1504P049				1				
012			RESISTOR,FIXED COMP	117C1504P059				1				
013			RESISTOR,FIXED COMP	117C1504P065				3				
014			RESISTOR,FIXED COMP	117C1504P108				1			B	
015			RESISTOR,FIXED COMP	117C1504P149				1				
016			RESISTOR,FIXED METAL FILM	145C3399P6812F55				1			B	
017			RESISTOR,FIXED METAL FILM	145C3399P1003F55				1			B	
018			RESISTOR,FIXED METAL FILM	145C3399P1004F65				2			B	
019			RESISTOR,FIXED FILM	176A1989P522				2			B	
020			TRANSISTOR	175A9230P008				4				
021			DIODE,ZENER	209A6112P040				4				
022			OPERATOR AMP	1958917-4P001				1			B	

MADE BY: EDP | DATE: 12 20 73 | LAST ITEM NO USED - 022 | FINAL SECTION | LAST SHEET: FINAL | SH NO 2

PL 1958907-4AA | SECT A | REV 7

GENERAL ELECTRIC

195B9074AA F 1

UNLESS OTHERWISE SPECIFIED USE THE FOLLOWING —

APPLIED PRACTICES	SURFACES
248A9226	✓

195B9074AA F 1

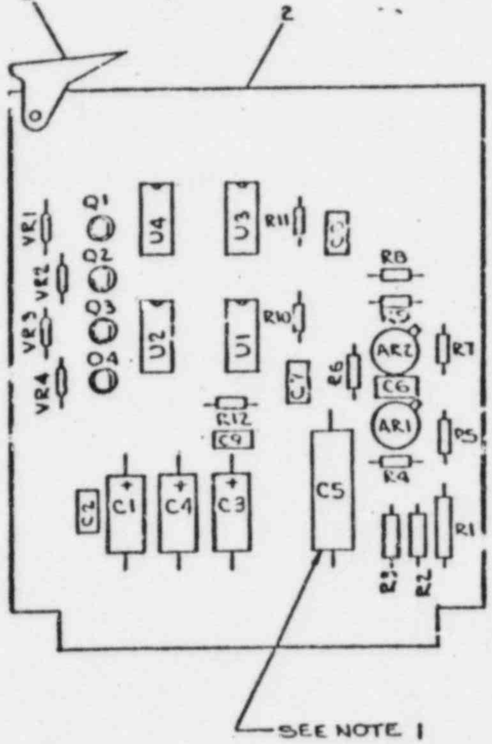
ASSY

THERMAL TRIP UNIT

FIRST MADE FOR PRM CAB

PL ISSUED

FCF: 145C3096DB



ITEM	REF DESIGNATION
5	U1 THRU U4
6	AR2
7	C1, C3, C4
8	C2, C7, C8, C9
9	C6
10	C5
11	R9
12	R8
13	R10, R11, R12
14	R4
15	R7
16	R6
17	R5
18	R1
19	R2, R3
20	Q1 THRU Q4
21	VR1 THRU VR4
22	AR1

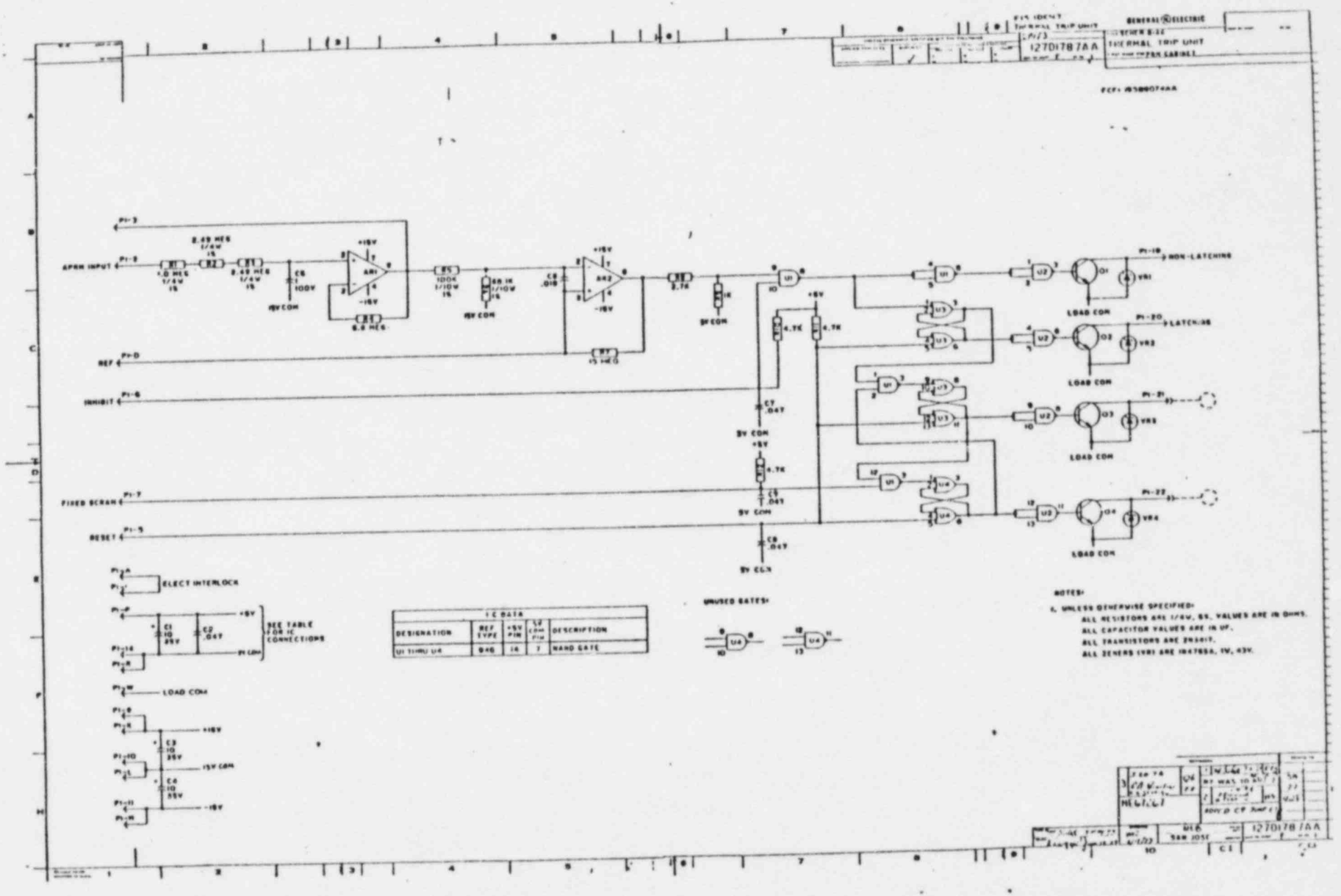
NOTES:
1. MOUNT ITEM 10, WITH MARKING SHOWN ON TOP.

REVISIONS		C	PRINTS TO
3	R. Y... 10-13 R YEE 73	REI RRS	428
			6
	NE C2517 CHKD RRI RRS		57

KA Calberry JUN 8, 73 — R Langford June 15, 73 — WG 6/15/73 — NED SAN JOSE — 195B9074AA F 1

C1

EIS


GENERAL ELECTRIC
1270178AA
APRM INPUT
REF
INHIBIT
FIXED SCRAM
RESET
ELECT INTERLOCK
LOAD COM
+15V
-15V
15V COM
5V COM
+5V
NON-LATCHING
LATCHING
UNUSED GATES:
IC DATA
DESIGNATION
REF TYPE
+5V PIN
DESCRIPTION
U1 THRU U4
9046
14
7
NAND GATE
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 1/4W, 5%. VALUES ARE IN OHMS.
ALL CAPACITOR VALUES ARE IN UF.
ALL TRANSISTORS ARE 2N3417.
ALL ZENERS (VR1 ARE 1N4733A, 1W, 43V.