

WESTINGHOUSE CLASS 3

WCAP-11896

NOISE, FAULT, SURGE, AND
RADIO FREQUENCY INTERFERENCE
TEST REPORT

FOR

Westinghouse Eagle-21™ Process Protection
Upgrade System

Prepared by:

J. P. Doyle 7/24/88
J. P. Doyle, Process Control Application

Reviewed by:

G. H. Madden 8/2/88
G. H. Madden, Process Control Application

Carl A. Vitalbo
C. A. Vitalbo, Process Control Application

L. E. Erin 8-2-88
L. E. Erin, Instrumentation and Control
Systems Licensing

Approved by:

J. B. Waclo 8/2/88
J. B. Waclo, Manager
Process Control
Application

Approved by:

D. P. Adomaitis 8/3/88
D. P. Adomaitis, Manager
Instrumentation and Control
Application Engineering

July 1988

9005110030 900508
PDR ADDCK 05000327
P PIC

WESTINGHOUSE POWER SYSTEMS
Pittsburgh, Pennsylvania 15230

ABSTRACT

The following test report documents the Eagle 21™ protection system adverse electrical noise test program. The primary objective of this test program was to demonstrate that the Eagle 21™ system remained operational before, during, and after the applied noise conditions. Other objectives were to demonstrate the physical independence of class non-1E and class-1E circuitry within the Eagle 21™ system.

The Eagle 21™ system met all performance requirements specified by the acceptance criteria. The adverse noise conditions applied to the Eagle 21™ system are designed to exceed worst-case noise environment conditions.

ACKNOWLEDGEMENTS

The author wishes to express his appreciation to G. Madden, C. Vitalbo, R. Nero, C. Antoniak, R. Mischler, K. Patrick, L. Erin, C. Nasrallah, Dr. V. Liepa, M. Kuttner, T. Leonard, S. Iverson, and R. Domitrovic whose help was instrumental in completing the testing and writing of this report.

TABLE OF CONTENTS

<u>Section</u>	<u>Title</u>	<u>Page</u>
1	INTRODUCTION	1-1
2	EAGLE 21™ SYSTEM DESCRIPTION	2-1
2.1	Introduction	2-1
2.1.1	Replacement of Existing Process Instrumentation	2-1
2.1.2	Plant Applications	2-4
2.1.3	Design Features	2-5
2.1.3.1	Single Failure Criterion	2-5
2.1.3.2	Instrument Power Source	2-6
2.1.3.3	Channel Integrity	2-6
2.1.3.4	Channel Independence	2-6
2.1.3.5	Control and Protection System Interaction	2-7
2.2	Functional Description	2-7
2.2.1	Block Diagram	2-7
2.3	Cabinet Description	2-11
3	EAGLE 21™ SYSTEM CONFIGURATION/OPERATION	3-1
3.1	Description	3-1
3.2	Configuration/Design Level Drawings	3-1
4	ISOLATION DEVICES PHILOSOPHY	4-1
4.1	Description	4-1
5	TEST DESCRIPTION	5-1
5.1	Noise Tests	5-1
5.1.1	Test Outline	5-1

TABLE OF CONTENTS (Cont)

<u>Section</u>	<u>Title</u>	<u>Page</u>
5.1.2	Random Noise Test	5-3
5.1.3	Crosstalk Noise - Chattering Relay Test	5-5
5.1.4	Military Specification Noise Test	5-5
5.1.5	High Voltage Transient Noise Test	5-8
5.1.6	Static Noise Test	5-8
5.2	Fault Tests	5-12
5.2.1	Test Outline	5-12
5.2.2	Test Implementation	5-12
5.3	Surge Withstand Capability (SWC) Test	5-18
5.3.1	Test Outline	5-18
5.3.1.1	Common Mode Test	5-19
5.3.1.2	Transverse Mode Test	5-19
5.3.2	Test Implementation	5-19
5.4	Radio Frequency Interference (RFI) Susceptibility Test	5-22
5.4.1	Test Methodology	5-22
5.4.2	Test Location	5-22
5.4.3	Test Equipment	5-23
5.4.4	Test Procedure	5-23
5.4.5	Calibration Test	5-23
5.4.6	Modulation Test	5-26
5.4.7	Keying Test	5-30
6	TEST SETUP AND MONITORING	6-1
6.1	Test Setup	6-1
6.1.1	System Connections	6-1
6.1.2	Simulated Input Signals	6-1
6.1.3	Data Acquisition System	6-8
6.1.3.1	Tape Recorder	6-9
6.1.3.2	Data Logger	6-8
6.1.3.3	Strip Chart Recorder	6-12

TABLE OF CONTENTS (Cont)

<u>Section</u>	<u>Title</u>	<u>Page</u>
6.2	Test Monitoring	6-12
6.2.1	Noise Test Setup Description	6-13
6.2.2	Fault Test Setup Description	6-15
6.2.3	Surge Withstand Test Setup Description	6-15
6.2.4	Radio Frequency Interference Test Setup Description	6-19
7	ACCEPTANCE CRITERIA	7-1
7.1	Description	7-1
7.1.1	Noise Test Acceptance Criteria	7-1
7.1.2	Fault Test Acceptance Criteria	7-1
7.1.3	Surge Withstand Capability Test Acceptance Criteria	7-1
7.1.4	Radio Frequency Interference Test Acceptance Criteria	7-1
8	TEST RESULTS	8-1
8.1	Noise Test Results	8-1
8.2	Fault Test Results	8-2
8.2.1	Line-to-Ground Fault	8-2
8.2.2	Line-to-Line Fault	8-3
8.2.3	Board Modifications Required	8-4
8.2.3.1	Partial Trip Output Board	8-5
8.2.3.2	Digital Contact Output Board	8-5
8.3	Surge Withstand Capability Test Results	8-5
8.3.1	Common Mode Tests	8-6
8.3.2	Transverse Mode Tests	8-7
8.3.3	Board Modifications/Retests	8-7
8.4	Radio Frequency Interference (RFI) Test Results	8-8
8.4.1	Modulation Tests	8-9
8.4.2	Keying Tests	8-10
8.4.3	Cabinet Modifications Required	8-10

TABLE OF CONTENTS (Cont)

<u>Section</u>	<u>Title</u>	<u>Page</u>
9	CONCLUSION	9-1
9.1	Noise Tests	9-1
9.2	Fault Tests	9-2
9.3	Surge Withstand Capability Tests	9-2
9.4	Radio Frequency Interference Tests	9-2
Appendix A	Partial Trip Output Board Surge Withstand Capability Analysis	A-1
Appendix B	Microprocessors and I/O Boards Description	B-1
Appendix C	Test Procedures	C-1
Appendix D	Test Equipment List	D-1

LIST OF ILLUSTRATIONS

<u>Figure</u>	<u>Title</u>	<u>Page</u>
2-1	Eagle 21™ Process Protection Upgrade System Cabinet	2-2
2-2	Eagle 21™ Cabinet Installation	2-3
2-3	Typical I&C System Configuration	2-4
2-4	Eagle 21™ Simplified System Block Diagram	2-8
2-5	Man-Machine Interface (MMI) Cart	2-12
2-6	Cabinet Front View	2-13
2-7	Cabinet Rear View	2-14
5-1	Noise Test Setup (Antenna Coupled) Used for Random, HV Transient, Mil-N and Crosstalk Tests	5-2
5-2	Noise Test Setup (Direct Coupled) Used for Crosstalk and Static Noise Tests	5-4
5-3	Random Noise Source Test Setup	5-6
5-4a	Crosstalk Noise -- Chattering dc Relay Test Setup	5-7
5-4b	Crosstalk Noise -- Chattering ac Relay Test Setup	5-7
5-5	Military Specification Noise Sources	5-9
5-6	High Voltage Transient Noise Source Test Setup	5-10
5-7	Static Noise Source Test Setup	5-11
5-8a	Ac Fault Connections	5-14
5-8b	Dc Fault Connections	5-14
5-9	Transformer Connection for the 125 Vac Fault Source	5-15
5-10	Transformer Connection for the 580 Vac Fault Source	5-16
5-11	Dc Power Supply Fault Connections	5-17
5-12a	Common Mode Surge Withstand Capability Test Connection	5-20
5-12b	Transverse Mode Surge Withstand Capability Test Connection	5-20
5-12c	Block Diagram of Surge Withstand Capability (SWC) Test	5-21

LIST OF ILLUSTRATIONS (Cont)

<u>Figure</u>	<u>Title</u>	<u>Page</u>
5-13	Radio Frequency Interference Equipment Test Setup	5-24
5-14	Radio Frequency Field Calibration	5-25
5-15	Block Diagram of Radio Frequency Interference Calibration Tests	5-27
5-16	Cabinet Subject to Radio Frequency Field	5-28
5-17	Block Diagram of Radio Frequency Interference Modulation Tests	5-29
5-18	Block Diagram of Radio Frequency Interference Keying Tests	5-33
6-1	Cabinet and Field Cable Setup	6-2
6-2	Test Equipment Setup	6-3
6-3	Test Configuration Block Diagram	6-4
6-4	4-50 mA Transmitter	6-5
6-5	Wide Range Resistance Temperature Detector (RTD)	6-6
6-6	Narrow Range Resistance Temperature Detector (RTD)	6-7
6-7	10-50 mA Current Loop Output Monitoring	6-9
6-8	Trip Output Monitoring	6-10
6-9	Contact Output Monitoring	6-11
6-10	Noise Test Data Sheet	6-14
6-11	Fault Test Data Sheet	6-16
6-12	Surge Test Data Sheet	6-18
6-13	RFI Modulation Test Data Sheet	6-20
6-14	RFI Keying Test Data Sheet	6-21
6-15	Tape Recorder Log Sheet	6-22

LIST OF TABLES

<u>Figure</u>	<u>Title</u>	<u>Page</u>
5-1a	Line to Ground Fault Tests Performed	5-13
5-1b	Line to Line Fault Tests Performed	5-13
5-2	Keying Test Frequencies	5-31
8-1a	Random Noise Tests (Antenna Coupled)	8-11
8-1b	Ac Crosstalk Noise Tests -- Chattering Relays	8-12
8-1c	Dc Crosstalk Noise Tests -- Chattering Relays	8-13
8-1d	Military Specification Noise Source #1 Tests (Antenna Coupled)	8-14
8-1e	Military Specification Noise Source #2 Tests (Antenna Coupled)	8-15
8-1f	High Voltage Transient Noise Tests (Antenna Coupled)	8-16
8-1g	Static Noise Tests	8-17
8-2a	Line-Ground Fault Tests	8-18
8-2b	Line-to-Line Tests	8-20
8-3	Surge Withstand Capability (SWC) Tests	8-22
8-4a	Radio Frequency Modulation Test Results (All Results with Cabinet Doors Closed)	8-24
8-4b	Radio Frequency Keying Test Results (All Results with Cabinet Doors Closed)	8-29

SECTION 1

INTRODUCTION

This report documents the "adverse noise" test results of the Eagle 21™ Process Protection System.

The Eagle 21™ is a microprocessor-based functional replacement for the analog process protection equipment originally installed in a nuclear power generating plant.

The testing of the Eagle 21™ equipment was performed to demonstrate system operability before, during, and after the "adverse noise" conditions were applied. These adverse noise conditions are separated into four categories:

- o Noise Interference
- o Fault Isolation
- o Surge Withstand Capability (SWC)
- o Radio Frequency Interference (RFI)

A description of the tests, acceptance criteria, and test results of the Eagle 21™ in these adverse noise environments are contained in this report.

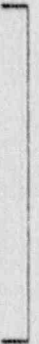
The Radio Frequency Interference tests were performed in an anechoic chamber []_c, with the balance of the tests performed at the Westinghouse Instrumentation Technology Training Center (ITTC) located in Monroeville, Pennsylvania. These tests were performed during a three-month period from December 1987 through February 1988.

SECTION 2

EAGLE 21™ SYSTEM DESCRIPTION

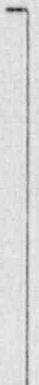
2.1 INTRODUCTION

The Westinghouse Eagle 21™ Process Protection Upgrade System is a qualified, microprocessor-based functional replacement for the analog process protection equipment originally installed in a nuclear power generating plant. The modular design of the Eagle 21™ hardware permits installation in existing process protection system cabinets after the analog electronics and internal cabinet wiring are removed. There is minimum disruption of external wiring because cabinet field terminal blocks and field cables are mostly undisturbed. All system inputs and outputs are preserved, and all existing field interfaces are maintained. Figure 2-1 depicts one Eagle 21™ cabinet.

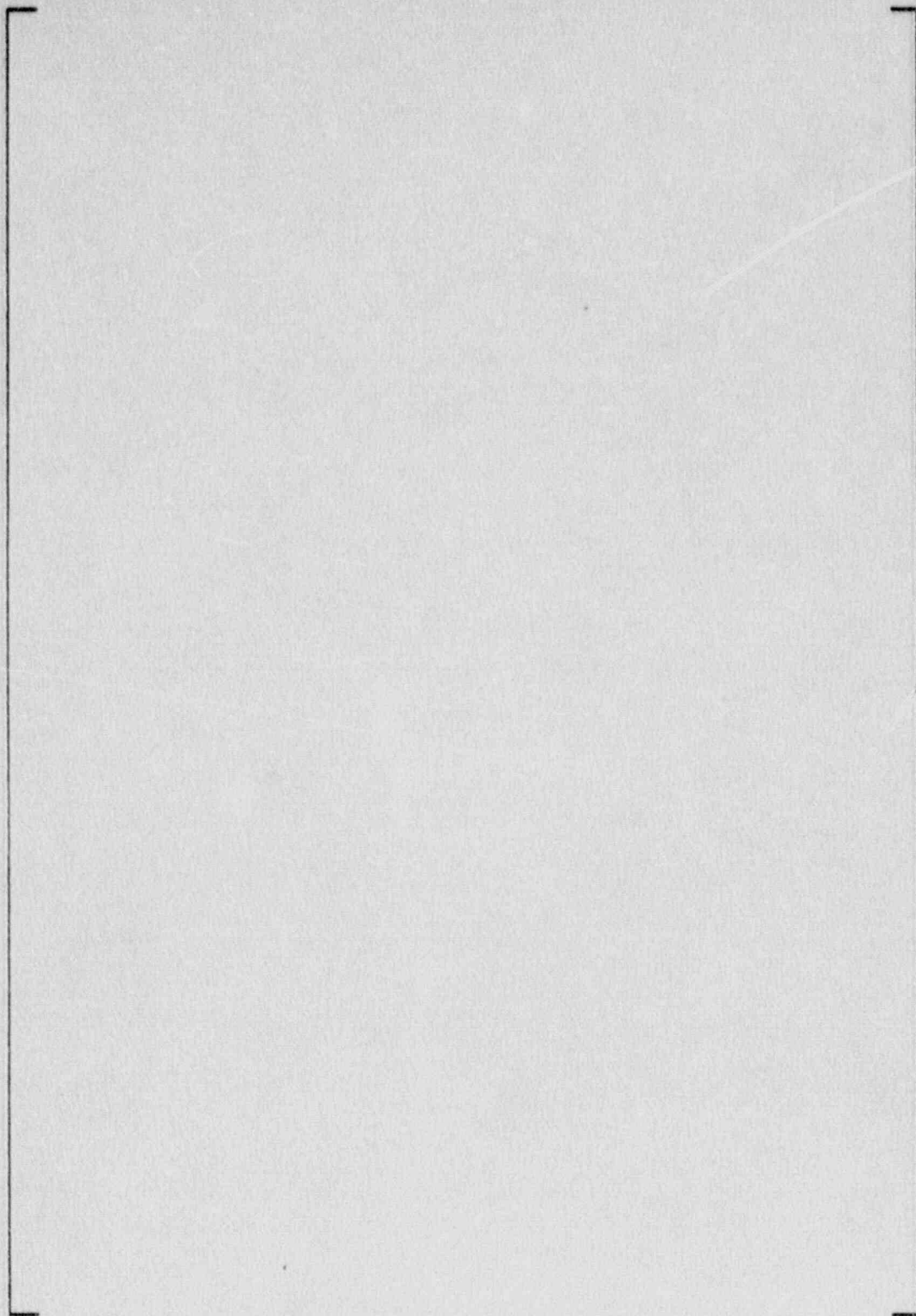


a, c

2.1.1 Replacement of Existing Process Instrumentation

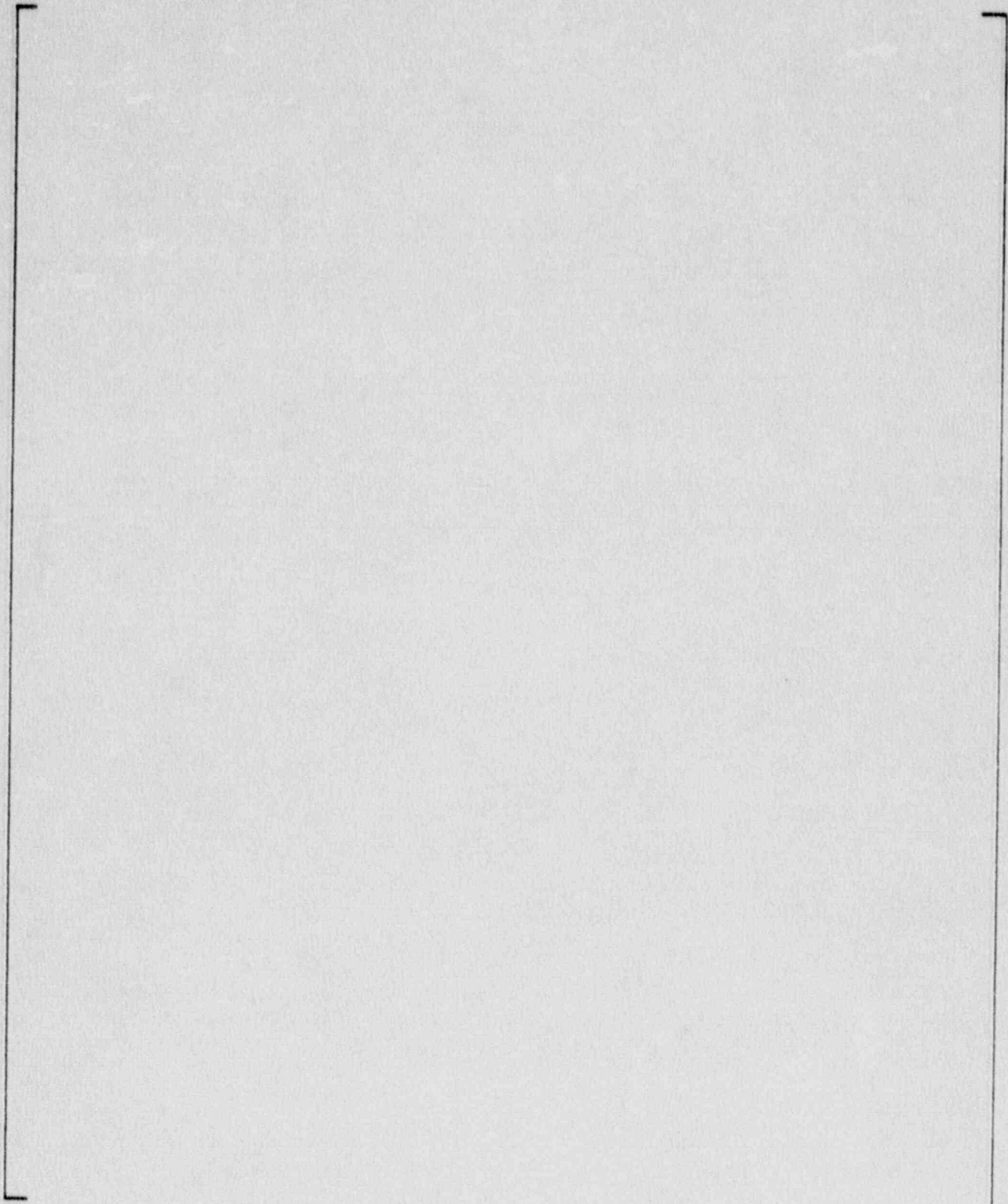


a, c



a, c

Figure 2-1 Eagle 21™ Process Protection Upgrade System Cabinet



a,c

Figure 2-2 Eagle 21™ Cabinet Installation

2.1.2 Plant Applications

The Eagle 21™ Process Protection Upgrade System is utilized in nuclear power generating stations to monitor Nuclear Steam Supply System (NSSS) parameters and to display indications of these parameters to the operating personnel. These indications meet the post-accident monitoring (PAM) requirements of Regulatory Guide 1.97, "Instrumentation for Light-Water-Cooled Nuclear Power Plants to Assess Plant and Environs Conditions During and Following an Accident." Figure 2-3 depicts the typical interconnections between the process protection equipment and other plant systems. [

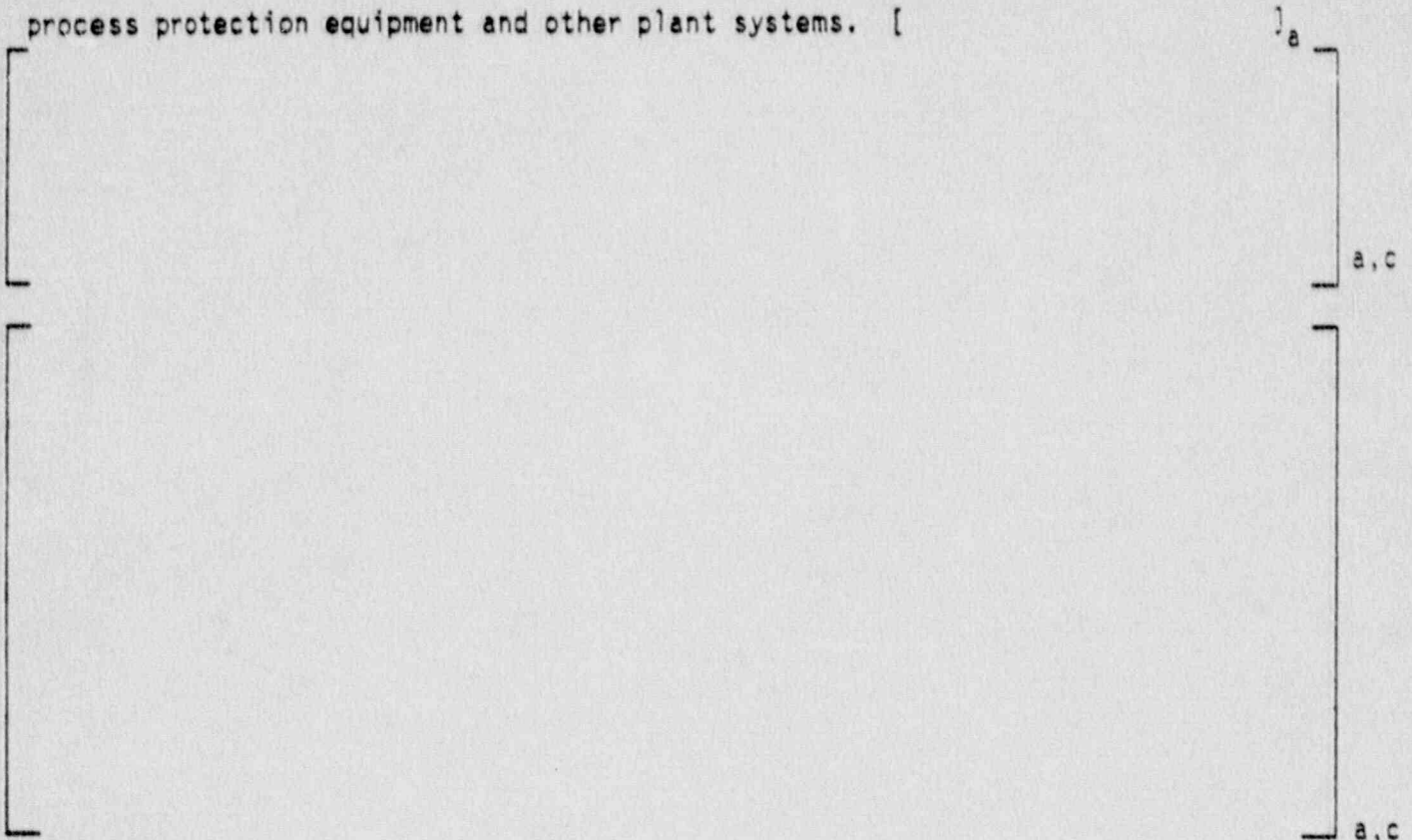


Figure 2-3 Typical I&C System Configuration

The NSSS parameters monitored by the Eagle 21™ Process Protection Upgrade System consist of temperatures, pressures, liquid levels, and flows. Resistance temperature detectors (RTDs) are used for temperature measurements. Electronic transmitters having either a 4- to 20-mA or 10- to 50-mA range are used to monitor pressure, level, and flow parameters. The system can also accept analog voltage or current inputs from other nuclear process systems such as the Nuclear Instrumentation System (NIS).

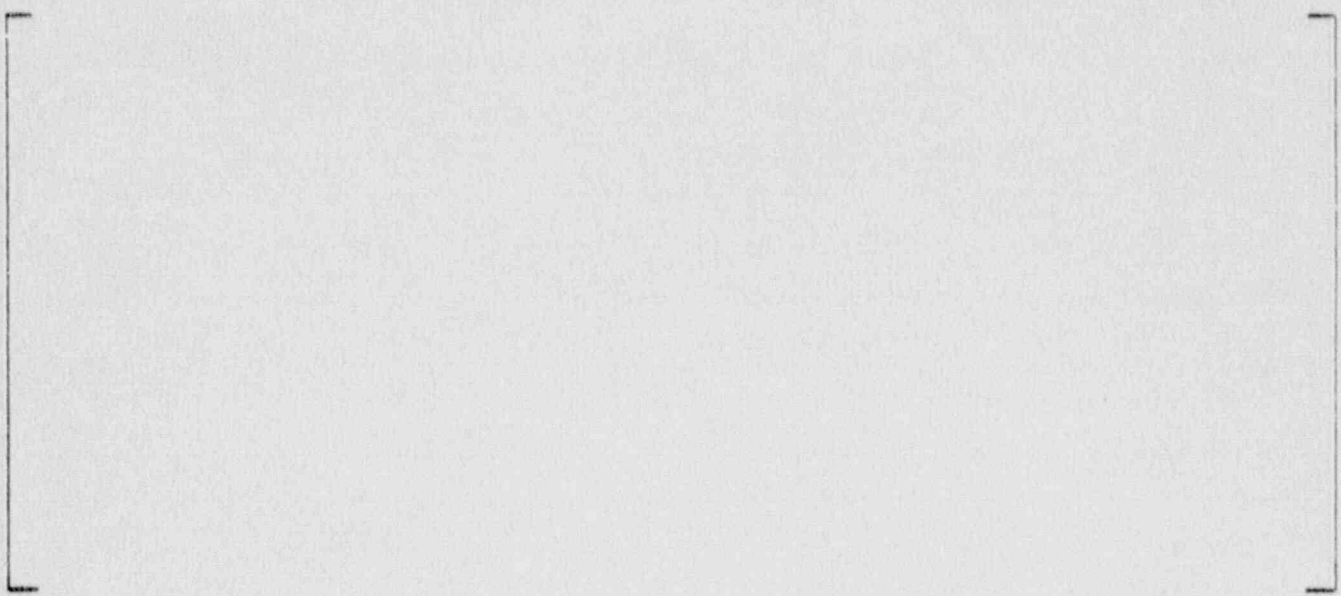
All inputs are converted to digital signals by the microprocessor-based Eagle 21™ electronics. After the desired signal conditioning is accomplished (including dynamic compensation of time-dependent signals, summation, and scaling), the system produces the following types of outputs:

- o Analog outputs -- 10- to 50-mA or 4- to 20-mA (or 1- to 5-vdc) signals supplied to control board indicators or the process control systems
- o Contact outputs -- On/off signals used to actuate control board annunciators
- o Channel trip outputs -- On/off signals used to control 120-vac input relays of the Solid State Protection System (SSPS), or a relay-based protection system, for reactor trip and safeguards actuation signals

2.1.3 Design Features

Major design features of the Eagle 21™ Process Protection Upgrade System are described in the following paragraphs.

2.1.3.1 Single Failure Criterion



2.1.3.2 Instrument Power Source



2.1.3.3 Channel Integrity

The Eagle 21™ Process Protection Upgrade System has been designed to perform its protective functions under extreme operating conditions relating to its environment, its energy supply, any malfunctions, and any accidents.

2.1.3.4 Channel Independence



[] a

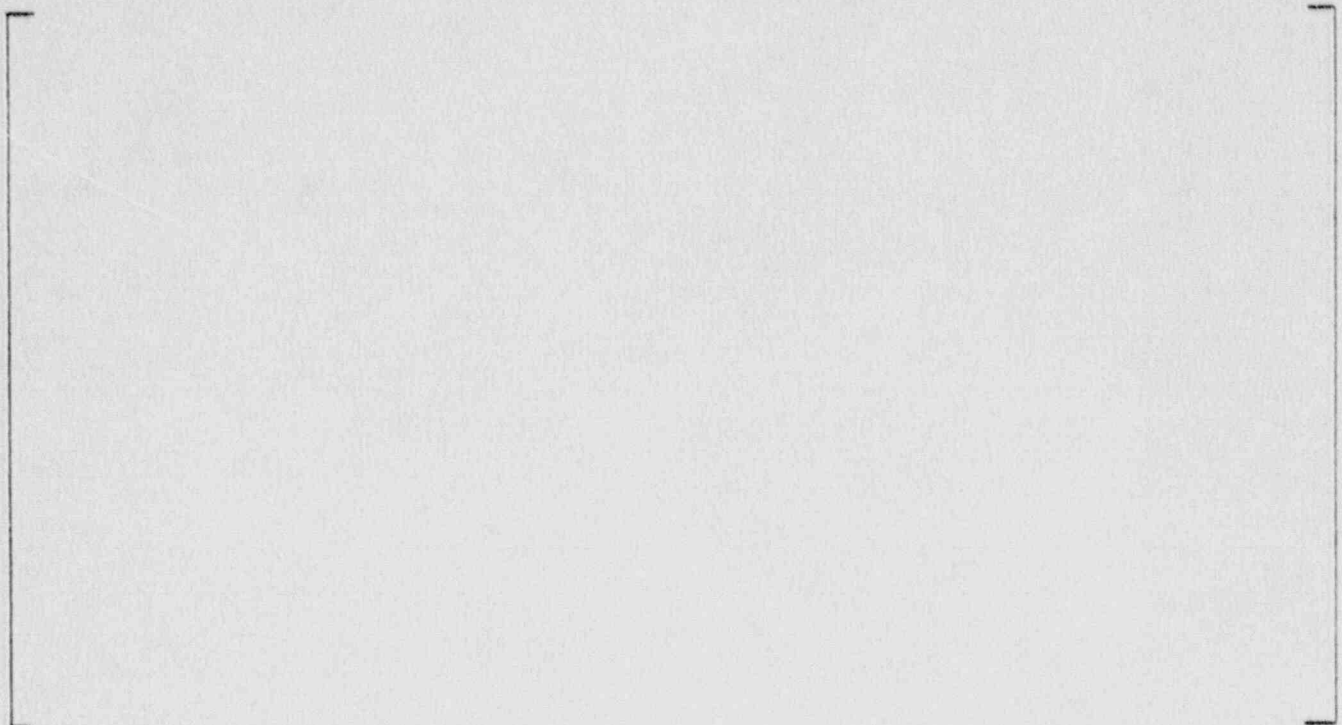
2.1.3.5 Control and Protection System Interaction

The Eagle 21™ Process Protection Upgrade System functions with complete independence from the plant's control systems. (Control systems include remote indicators, computer data points, and annunciators as well as circuits that automatically control plant parameters.) Protective functions are electrically isolated from any fault or malfunction that occurs in the control systems.

2.2 FUNCTIONAL DESCRIPTION

The following paragraphs provide a brief functional description of the Eagle 21™ Process Protection Upgrade System, based on the simplified functional block diagram shown in figure 2-4.


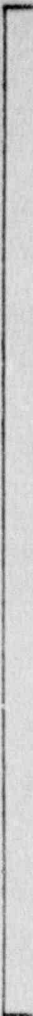
2.2.1 Block Diagram



a, c

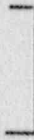
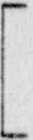
Figure 2-4. Eagle 21st Simplified System Block Diagram

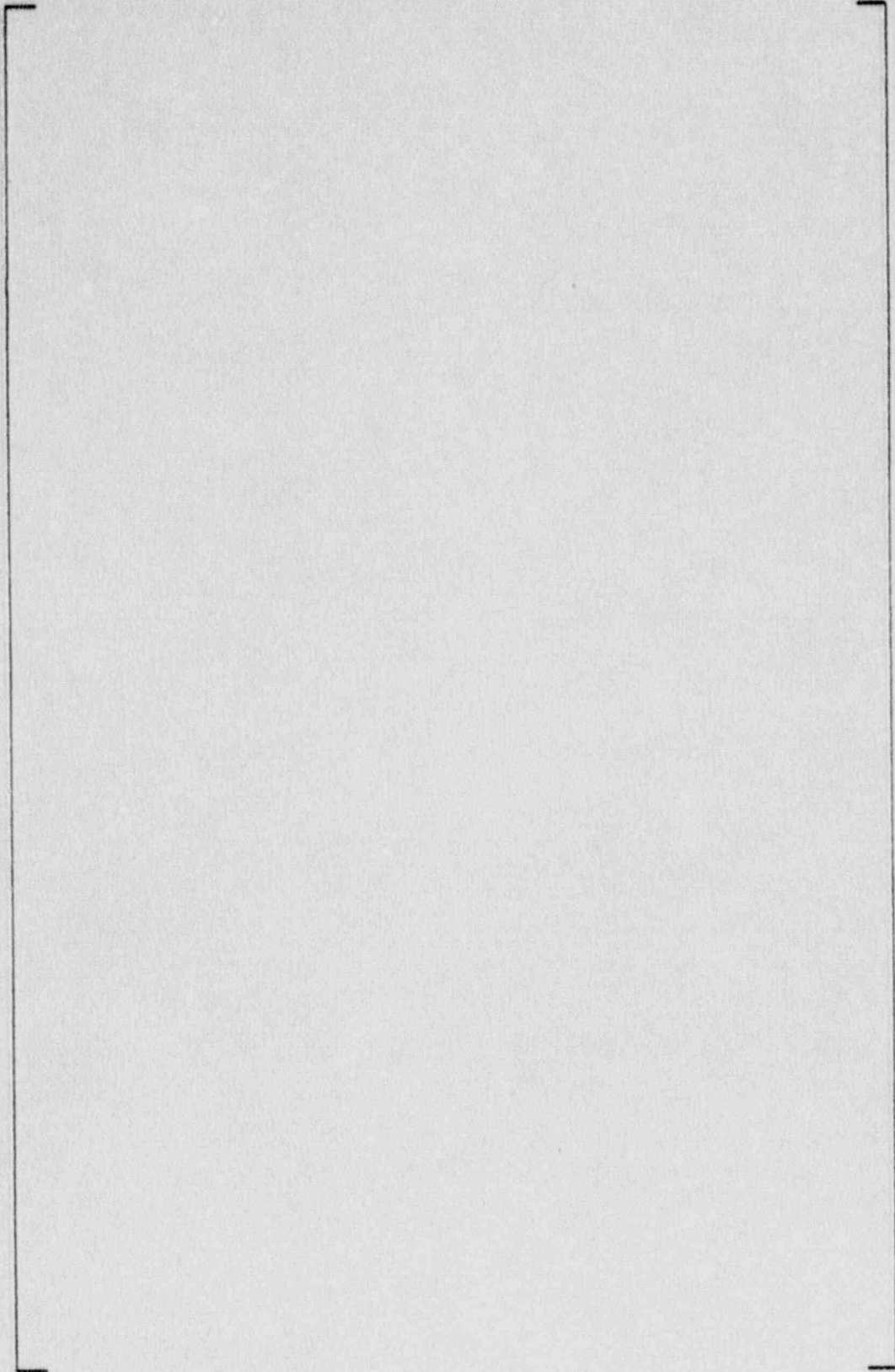
a, c



2.3 CABINET DESCRIPTION

The Eagle 21™ Process Protection Upgrade System is housed in existing process instrumentation cabinets to which structural bracing and mounting rails have been installed. Cabinet front and rear views are shown in figures 2-6 and 2-7. [





a,c

Figure 2-5 Man-Machine Interface (MMI) Cart

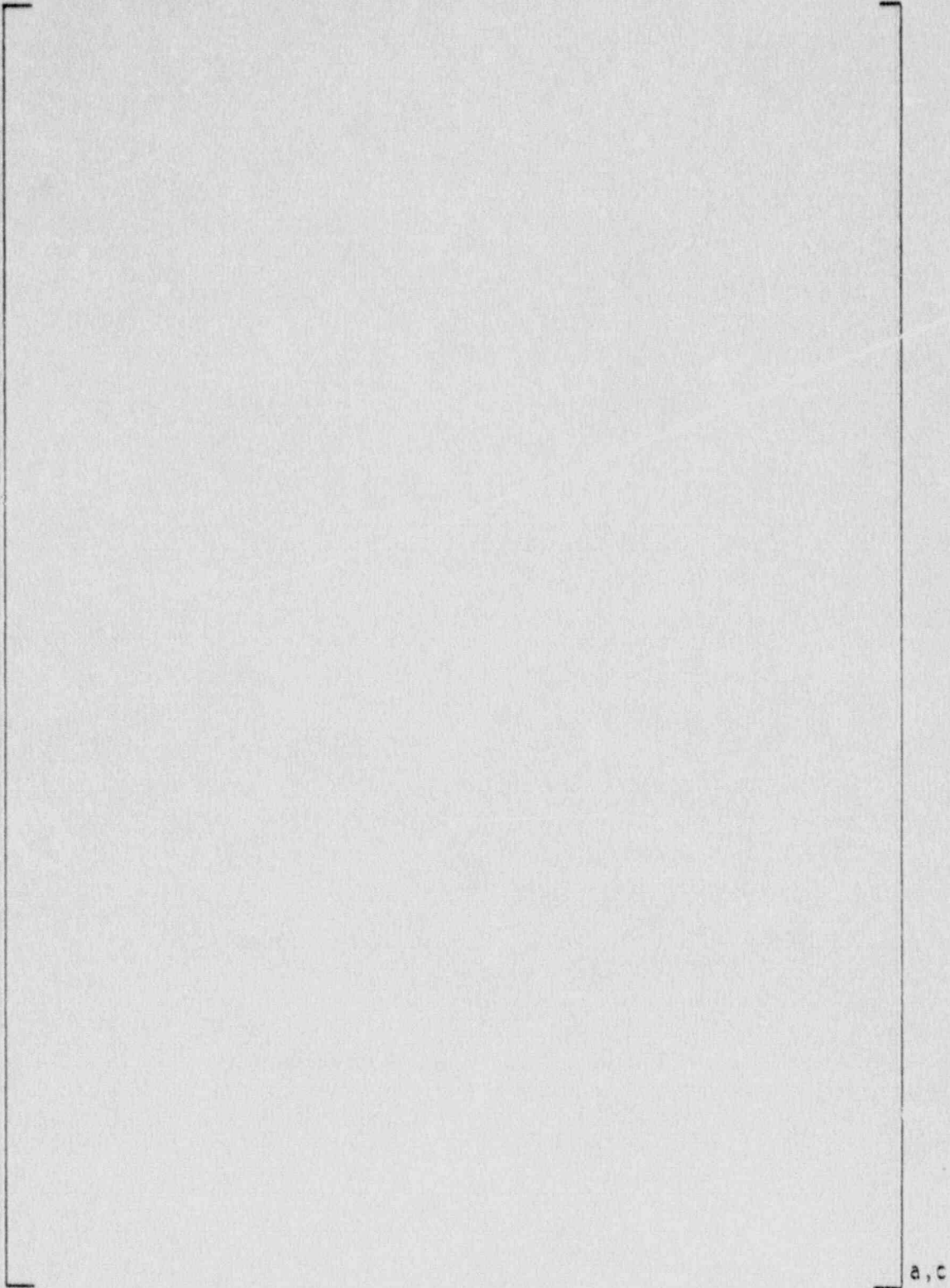


Figure 2-6 Cabinet Front View

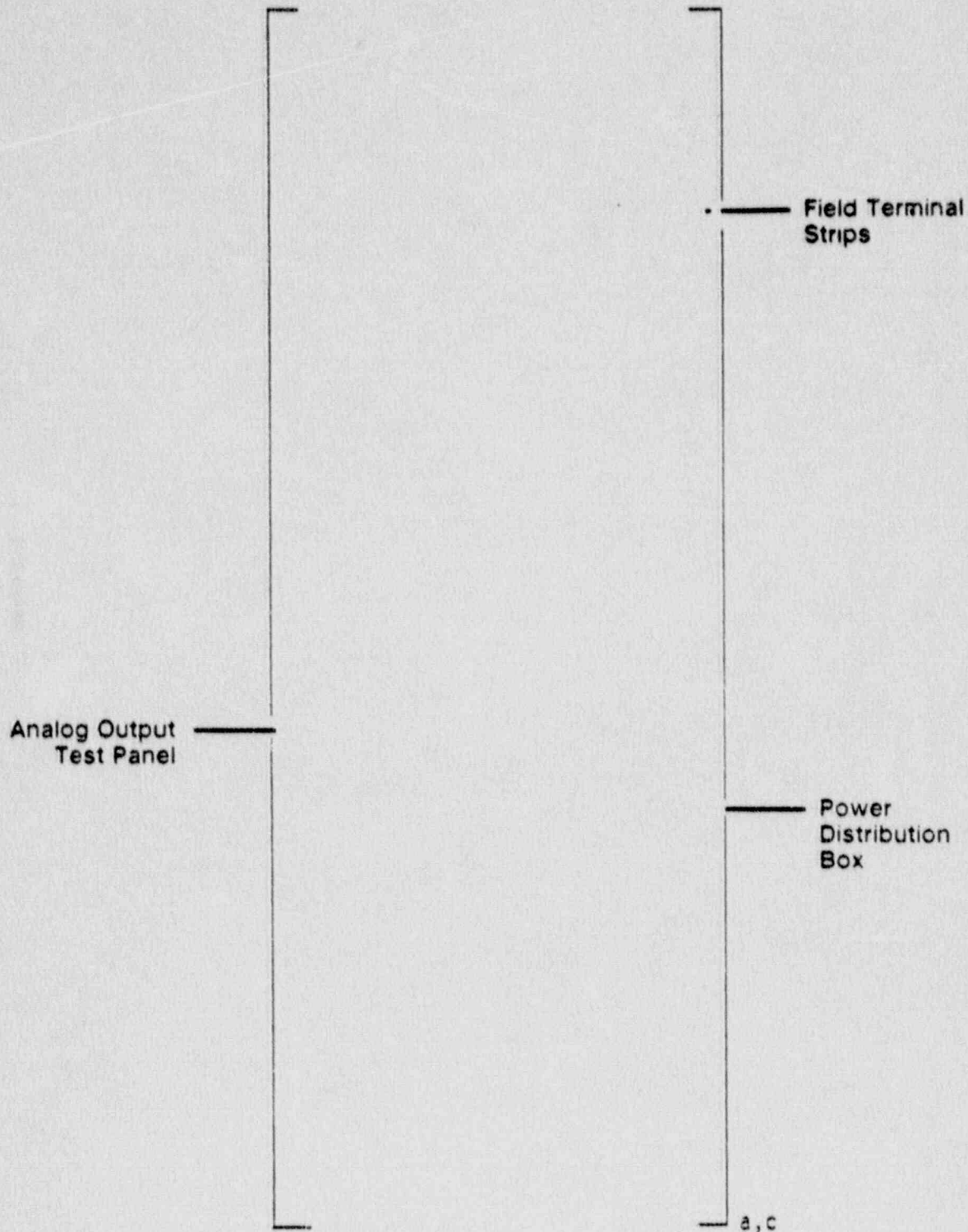


Figure 2-7 Cabinet Rear View

SECTION 3

EAGLE 21™ SYSTEM CONFIGURATION

3.1 DESCRIPTION

The Eagle 21™ system tested (Qualification Unit 2) is an exact replica of Watts Bar Nuclear Power Station protection rack 13. This rack contains the following instrument loops (subsystems):

- o Delta T/T_{avg}, Protection
- o Steam Generator Wide Range Level, Post Accident Monitoring (PAM) (2 Channels)
- o Pressurizer Vapor Temperature, (PAM)
- o Residual Heat Removal Pump Discharge Temperature, (PAM)
- o Reactor Coolant System Wide Range Pressure, (PAM)

3.2 CONFIGURATION/DESIGN LEVEL DRAWINGS

The following drawings/revision levels are attached to document the system configuration tested:

<u>Drawing Description</u>	<u>Drawing Number/Revision</u>
Terminal Block Wiring Diagram, Protection Set 4	1-47043, PW-13, Revision 3E
Process Control Block Diagram, Delta T/T _{avg} System	108D408, sheet 10, Revision 11
Process Control Block Diagram, WR SG Level	108D408, sheet 34, Revision 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temperature	108D408, sheet 38, Revision 4

<u>Drawing Description</u>	<u>Drawing Number/Revision</u>
Process Control Block Diagram, RHR Pump Discharge Temperature	108D408, sheet 39, Revision 5
Process Control Block Diagram, RCS Wide Range Pressure	108D408, sheet 43, Revision 1
Eagle 21™ Schematic Diagrams, Rack 13 Protection Set 4	1856E69, sheet 2, Revision 2

The following drawings/revision levels are referenced to document the system hardware tested:

<u>Drawing Description</u>	<u>Drawing Number/Revision</u>
Cabinet General Assembly	1870E97G01, Revision 3
Analog Input Board, 10-50, 4-20 mA (EAI-G01)	5367C57, Revision 4
WR RTD Input Board (ERI-G01)	5368C29, Revision 2
NR RTD Input Board (ERI-G02)	5368C29, Revision 2
Partial Trip Output Board (EPT-G01)	2033786, Revision 2
Digital Contact Output Board (ECO-G01)	5367C61, Revision 3
Analog Output Board 10-50 mA (EAO-G02)	5367C60, Revision 3
Power Distribution Box (G01)	1871E34, Revision 3
Termination Module Assembly 0-10 Volt (G01)	2033779, Revision 1

Drawing Description

Drawing Number/Revision

Termination Module Assembly 4-20 mA (G01)	2D27362, Revision 1
Termination Module Assembly 10-50 mA (G06)	2D27362, Revision 1
Baseline Design Document	956093, Revision 0
*Digital Contact Output Board (ECO-G01)	5367061, Revision 4
*Partial Trip Output Board (EPT-G01)	2D33786, Revision 3

*Boards modified to successfully complete fault testing. Modifications made and required retests are described in sections 8.2, 8.3 and Appendix A.

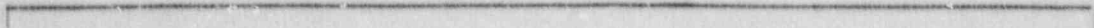
I/O and microprocessor boards were configured per design specification 956073, Revision D.

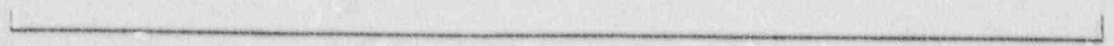
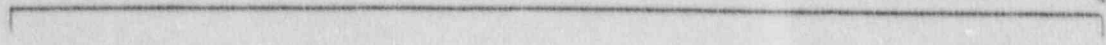
System software used has been retained on permanent file.



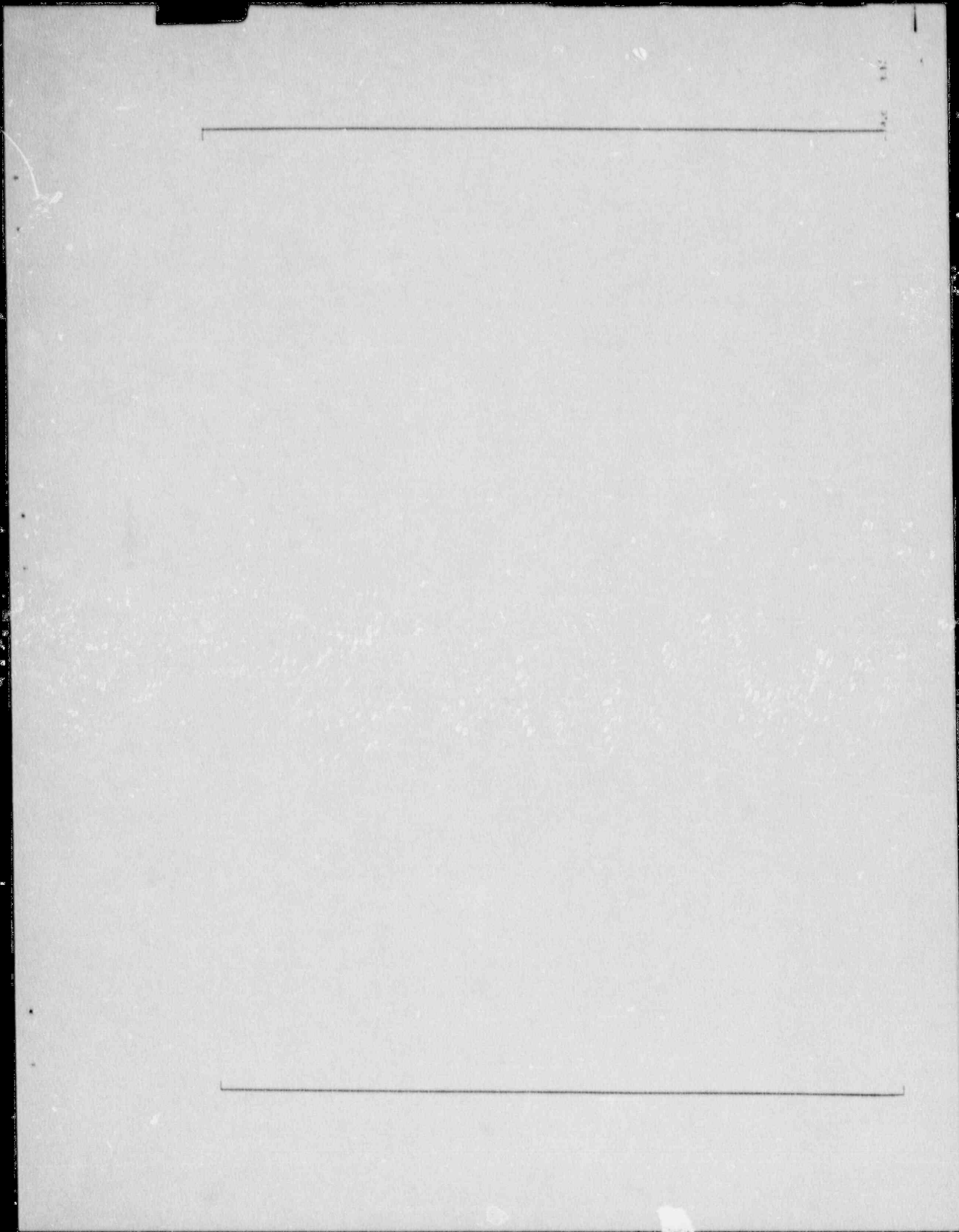
3.1.0

3.7





111



SECTION 4 ISOLATION DEVICES PHILOSOPHY

4.1 DESCRIPTION

The Eagle 21™ System uses the output signal conditioning boards as an isolation barrier between field level signals and the microprocessor subsystem. The Eagle 21™ uses the following types of isolation devices for interfacing Class 1E signals with non-1E equipment.

<u>Isolator Board Type</u>	<u>Isolation Device</u>
Analog Output Board (current loop), EAO Digital Contact Output Board, ECO Partial Trip Output Board, EPT	[] c

In addition, high voltage transient protection is provided for each cabinet input/output, including the ac power feed, by transient suppression circuitry. Fault currents are limited by preferred failure mode components.

SECTION 5

TEST DESCRIPTION

5.1 NOISE TESTS

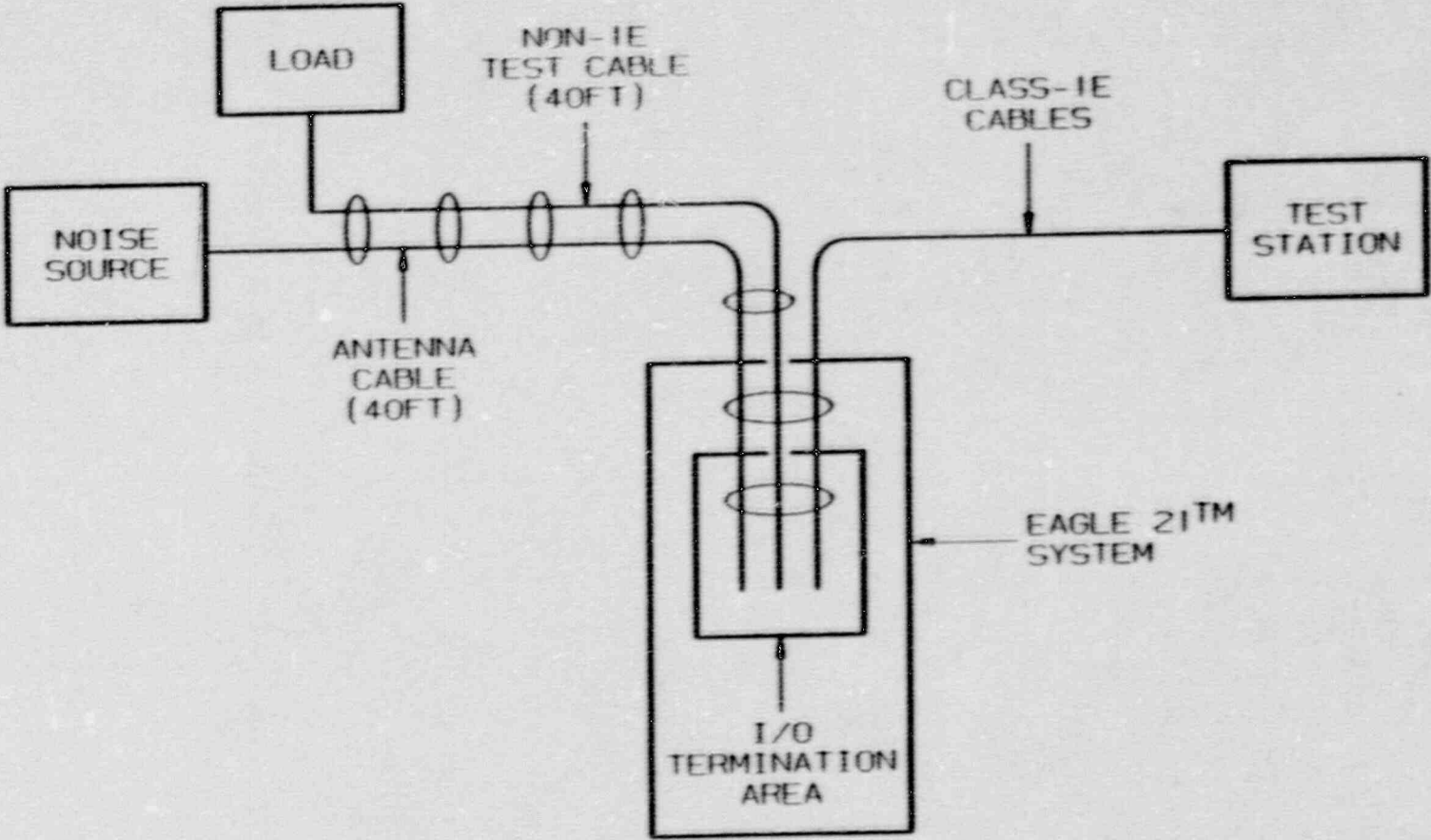
The Eagle 21™ system is a microprocessor upgrade to existing analog plant instrumentation and control (I & C) equipment. The Eagle 21™ is installed in the existing plant I & C process racks. The field termination wiring in these racks does not meet the spatial separation requirements between Class 1E and non-1E wiring as specified by IEEE-384-1977 and Nuclear Regulatory Guide 1.75 Rev. 2. The purpose of the noise tests is to demonstrate that the protective actions of the Eagle 21™ system are not affected by noise injected into or adjacent to class non-1E wiring. Protective action is defined as the ability to generate a partial trip output signal upon input signal demand. NUREG 1.75 Appendix 1 section 4.5 allows the use of tests to demonstrate that class 1E circuits are not degraded when minimum separation distance is not maintained. The noise sources were chosen to emulate worst-case noise conditions which may be present on non-1E wiring in the Eagle 21™ process rack.

5.1.1 Test Outline

The Eagle 21™ equipment was subjected to the following noise sources:

- o Random Noise Test (Antenna Coupled)
- o Crosstalk Noise - Chattering Relay Test (Antenna and Direct Coupled)
- o Military Specification MIL-N-19900B Noise Test (Antenna Coupled)
- o High Voltage Transient Noise Test (Antenna Coupled)
- o Static Noise Test (Antenna and Direct Coupled)

For the random, high-voltage transient and military specification noise tests, the noise source was antenna coupled to the class non-1E field wiring under test. The noise source was applied to a 40-foot antenna wire adjacent to a 40-foot length of unshielded class non-1E field wiring. The antenna was brought directly into the cabinet and bundled with Class 1E input/output cables upon entering the process rack (see figure 5-1).



5-2

Figure 5-1. Noise Test Setup (Antenna Coupled) Used for Random, HV Transient, Mil-N and Crosstalk Tests

The non-1E test cable was terminated with a nominal load value. Load values for each board type tested are given below:

<u>Isolator Board Type</u>	<u>Load</u>
10-50 mA current loop output, EAO	600 ohms
Digital Contact Output, ECO	*Open circuit and short circuit
Partial Trip Output, EPT	**40 watt incandescent light bulb

-
- * Since the contact output board nominal load is unknown, both open and short circuit tests were performed.
 - ** This load is considered conservative since the resultant loop impedance to transient signals is low compared to the inductive load this board would normally service.

The crosstalk and static noise tests were conducted similarly, except that an additional test was performed where the noise source was applied directly to the non-1E wiring. To prevent damage, the isolator was disconnected at the Eagle 21" termination frame and the disconnected non-1E wires shorted to complete the crosstalk noise circuit loop. The disconnected non-1E wires were open-circuited for the static noise test (See figures 5-2, 5-4, and 5-7).

Each noise test run consisted of 2 minutes of pretest data, 2 minutes of test data (noise source supplied), and 2 minutes of post-test data.

For a detailed description of the noise test setup, see section 6.2.1.

For a detailed test sequence, channel monitoring, and system external connection information, see the noise test procedure in appendix C.

5.1.2 Random Noise Test

This noise source was generated by a random noise generator []_c. Its output was fed through a power amplifier []_c.

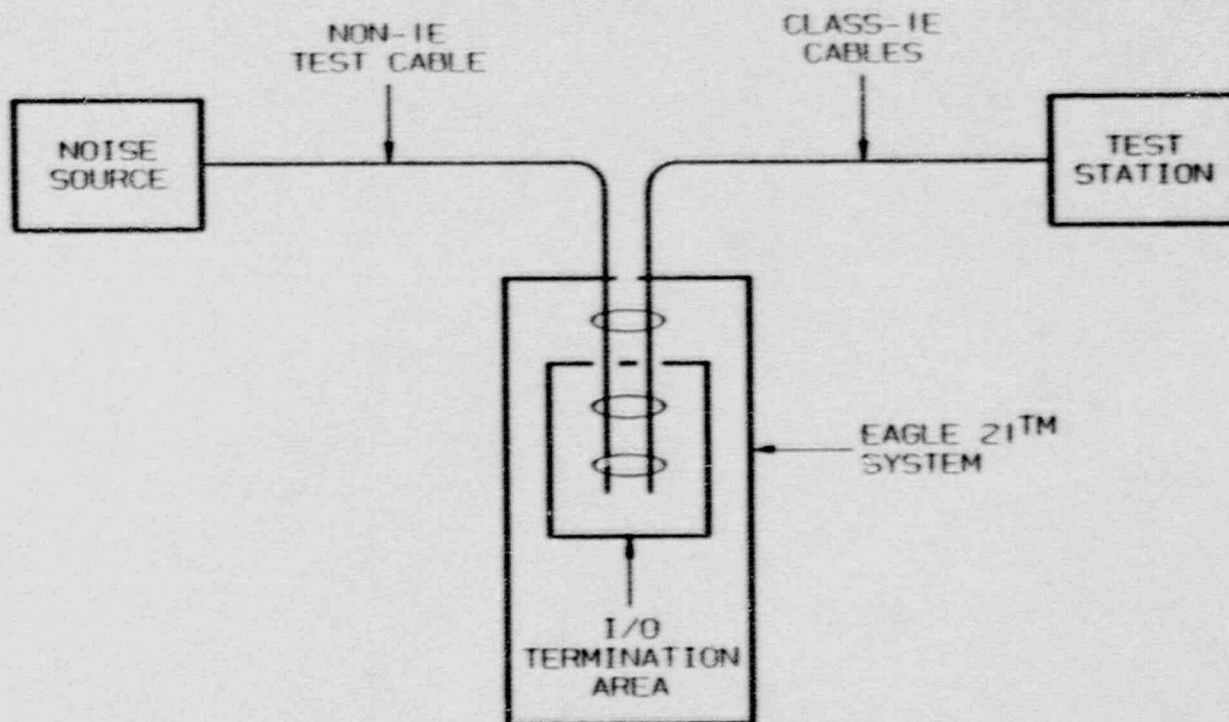


Figure 5-2. Noise Test Setup (Direct Coupled) Used for Crosstalk and Static Noise Tests

The radiated random noise characteristics are as follows:

Peak value: 20 V

Frequency: 20 kHz - 10 MHz

Figure 5-3 shows the random noise source test setup.

5.1.3 Crosstalk Noise - Chattering Relay Test

A dc and an ac relay were used to generate a radiated crosstalk noise. The relays were set in a "chattering" or "buzzer" mode by wiring the normally closed relay contacts in series with the relay coil. The following types of relays were used during the crosstalk noise-chattering relay test:

- o Relay with a 118 Vac coil, 0.3 amp nominal
- o Relay with a maximum rating of 600 Vdc, 125 Vdc coil, 0.22 amp nominal

Figure 5-4a shows the dc crosstalk noise source -- chattering relay test setup. Figure 5-4b shows the ac crosstalk noise source -- chattering relay test setup.

5.1.4 Military Specification Noise Test

Military specification noise testing was performed using switched cycling noise sources with the characteristics of Noise Sources No. 1 and No. 2 in Military Specification MIL-N-19900B.

The characteristics for Noise Source No. 1 were:

Voltage: 115 Vdc

Inductance: 3 H

Resistance: 500 ohm

037-A-24435-11

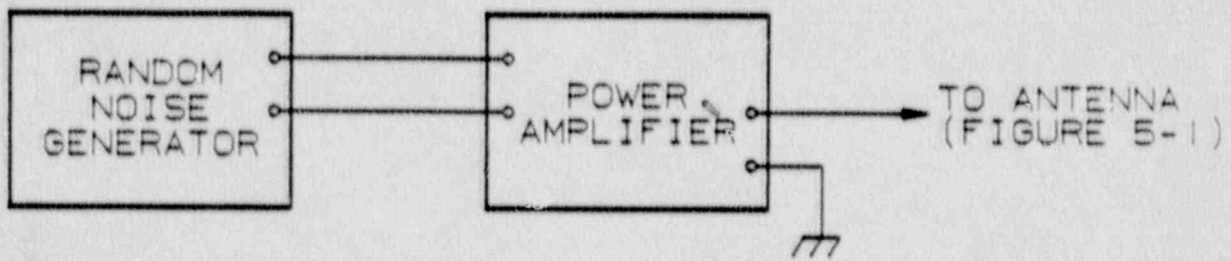


Figure 5-3. Random Noise Source Test Setup

037-A-24435-12

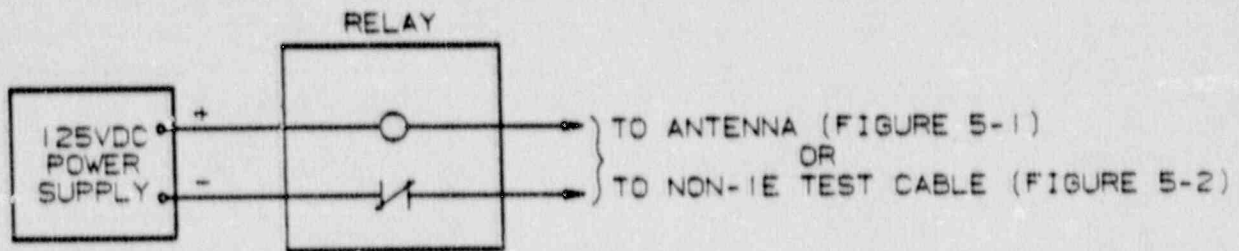


Figure 5-4a. Crosstalk Noise -- Chattering dc Relay Test Setup

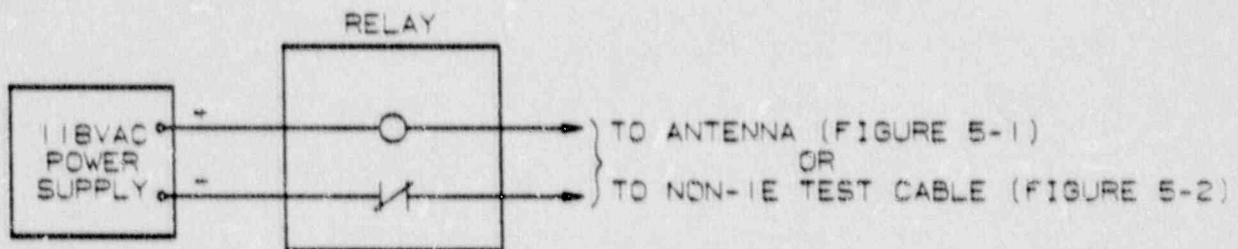


Figure 5-4b. Crosstalk Noise -- Chattering ac Relay Test Setup

The characteristics for Noise Source No. 2 were:

Voltage: 115 Vac
Inductance: 10 mH
Resistance: 2 ohm

Repetition rate for both noise sources was 10 on-off cycles per minute.

Figure 5-5 shows the military specification noise source test setup.

5.1.5 High Voltage Transient Noise Test

This noise source was generated from a surge transient generator []_c coupled to an isolation network box []_c.
The high voltage transient noise characteristics are in accordance with IEEE-472-1974 as follows:

E_{CREST} : 3.3 kV
Surge Frequency: 1.25 MHz
Time to $1/2 E_{CREST}$ = 6.4 μ s
Repetition rate: 120 Hz

Figure 5-6 shows the high voltage transient noise source test setup.

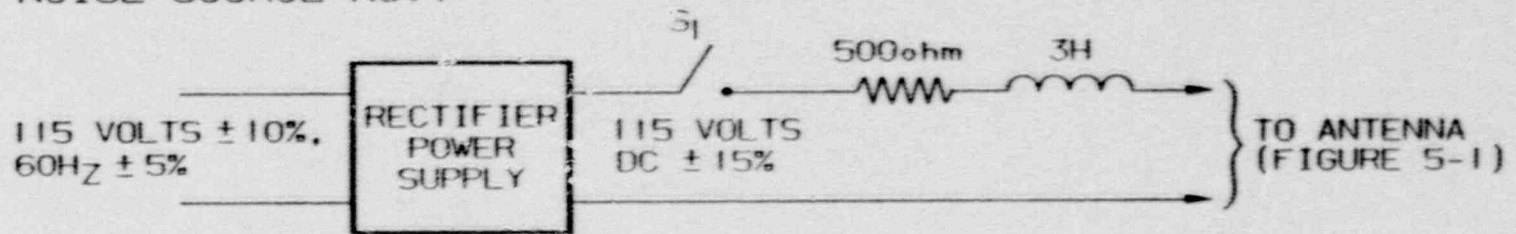
5.1.6 Static Noise Test

This noise source was generated using a step-up transformer []_c. A value of 580 Vrms at 60 Hz was injected into the non-1E test cable and into the antenna assembly.

Figure 5-7 shows the static noise test setup.

037-A-24435-13

NOISE SOURCE NO. 1



NOISE SOURCE NO. 2

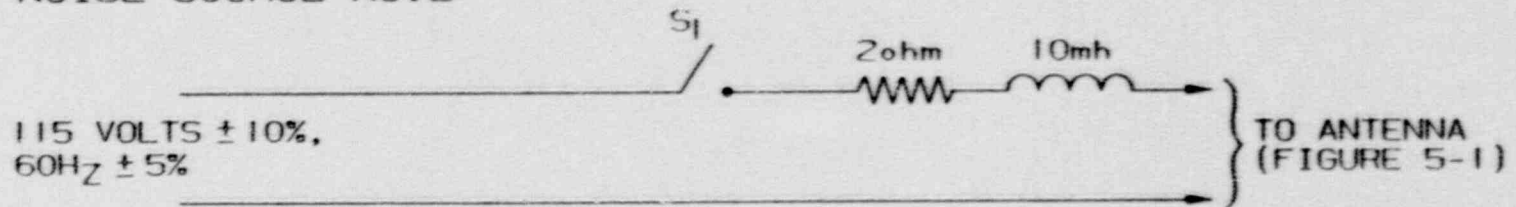


Figure 5-5. Military Specification Noise Sources

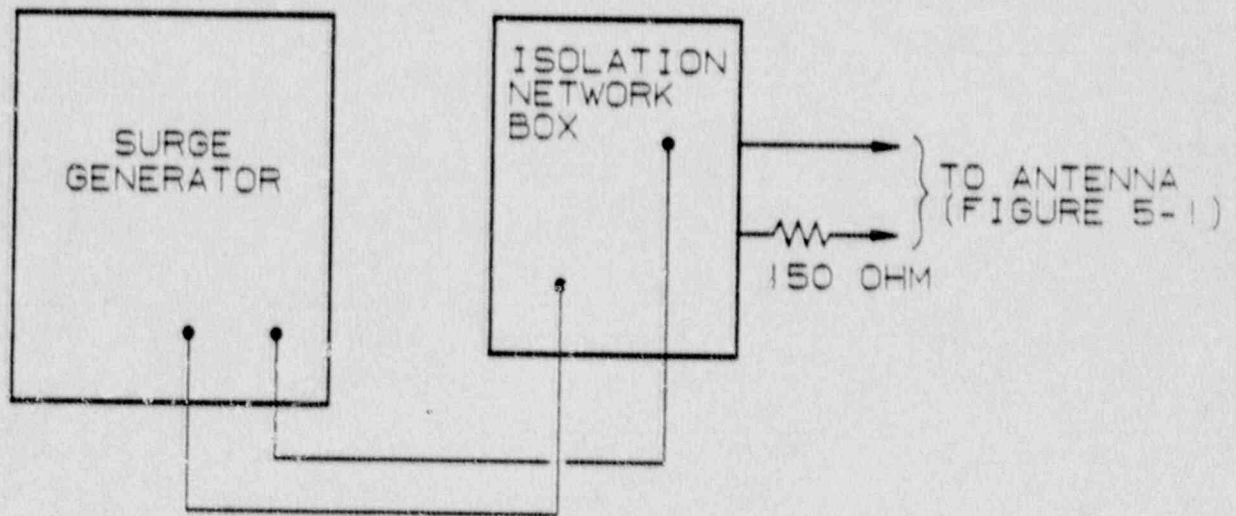


Figure 5-6. High Voltage Transient Noise Source Test Setup

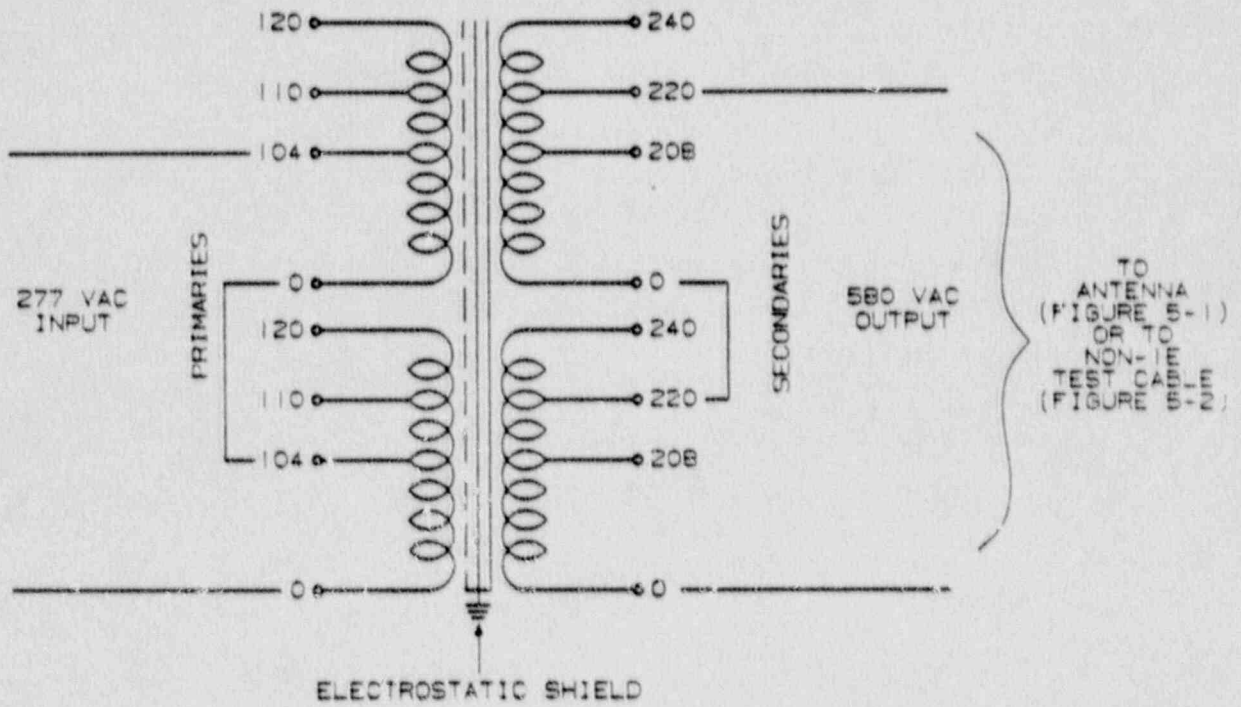


Figure 5-7. Static Noise Source Test Setup

5.2 FAULT TESTS

The purpose of the fault tests is to demonstrate that credible faults injected into the non-1E system do not propagate across the class non-1E to class 1E isolation barrier or from channel to channel within the Eagle 21™ process rack. These tests are designed to verify that the Eagle 21™ system isolation devices are in compliance with IEEE-279-1971, IEEE-384-1981, IEEE-603-1980, and Nuclear Regulatory Guide 1.75 Rev. 2 concerning the physical independence of class 1E circuits and class 1E/non-1E interaction.

5.2.1 Test Outline

Maximum credible fault voltages were determined to be 580 Vac and 250 Vdc per previous protection system tests (7300 system, QDPS, etc.). In addition, 125 Vac and 125 Vdc tests were performed where applicable. A fault was considered applicable only if the fault challenged the nominal voltage or current ratings of the channel under test. For cases where 125 Vac and 125 Vdc tests were considered not applicable, 580 Vac and 250 Vdc tests were performed thus enveloping the lower voltage tests.

Fault voltages were applied line to ground and line to line (ungrounded) into the isolator terminals. Tables 5-1a and 5-1b list tests performed by board type. Figures 5-8a and 5-8b show the ac and dc fault connections. Positive and negative dc voltage line-to-ground faults were applied.

5.2.2 Test Implementation

Ac fault voltages were generated using a 7.5 KVA isolation transformer []_c. Figures 5-9 and 5-10 show the transformer connections used.

Dc fault voltages were generated using a 250 V, 20 A dc power supply []_c. Two external 3300 μ f capacitors were added to increase the potential energy available for fault application (See figure 5-11).

TABLE 5-1a
 LINE TO GROUND
 FAULT TESTS PERFORMED

<u>Isolator Board Type</u>	<u>Faults Applied</u>
Partial Trip Output, Energized	125 Vdc, 125 Vac, 250 Vdc, 580 Vac
Partial Trip Output, Deenergized	250 Vdc, 580 Vac
Digital Contact Output, NO, Energized	250 Vdc, 580 Vac
Digital Contact Output, NC, Energized	250 Vdc, 580 Vac
Current Loop Output, 10-50 mA	125 Vac, 125 Vdc, 250 Vdc, 580 Vac

TABLE 5-1b
 LINE TO LINE
 FAULT TESTS PERFORMED

<u>Isolator Board Type</u>	<u>Faults Applied</u>
Partial Trip Output, Energized	125 Vac, 125 Vdc, 250 Vdc, 580 Vac
Partial Trip Output, Deenergized	250 Vdc, 580 Vac
Digital Contact Output, NO, Energized	125 Vac, 125 Vdc, 250 Vdc, 580 Vac
Digital Contact Output, NC, Energized	250 Vdc, 580 Vac
Digital Contact Output, NO, Deenergized	250 Vdc, 580 Vac
Digital Contact Output, NC, Deenergized	125 Vac, 125 Vdc, 250 Vdc, 580 Vac
Current Loop Output 10-50 mA	125 Vac, 125 Vdc, 250 Vdc, 580 Vac

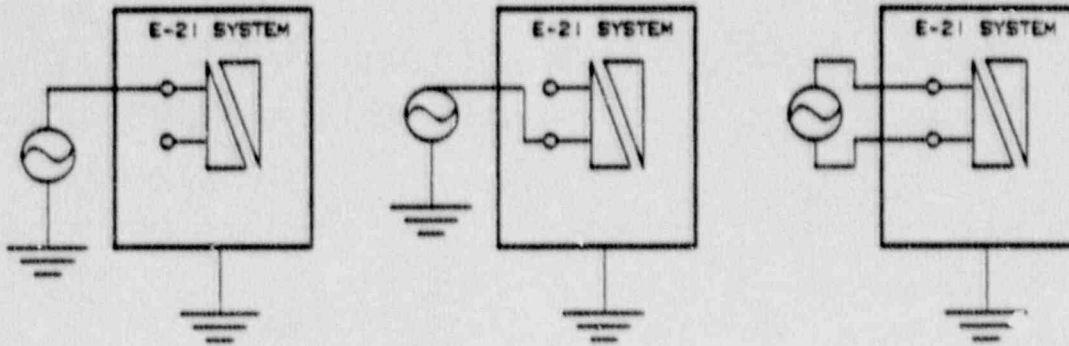


Figure 5-8a. Ac Fault Connections

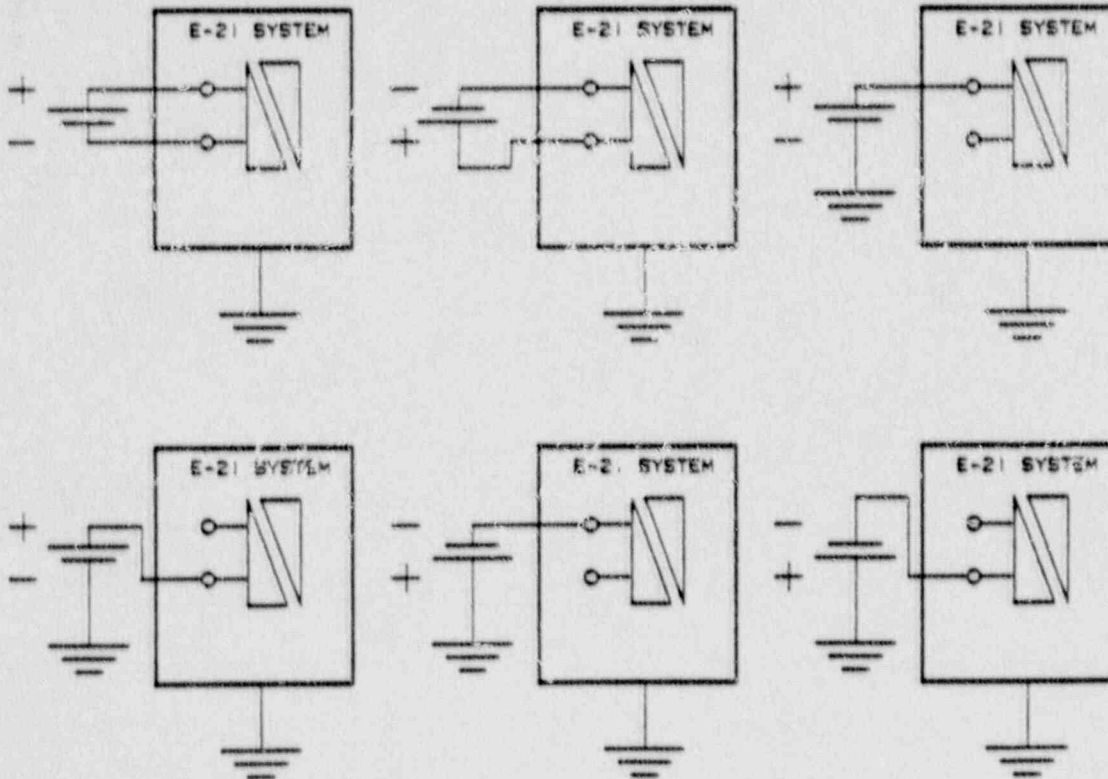


Figure 5-8b. Dc Fault Connections

037-A-24435-22

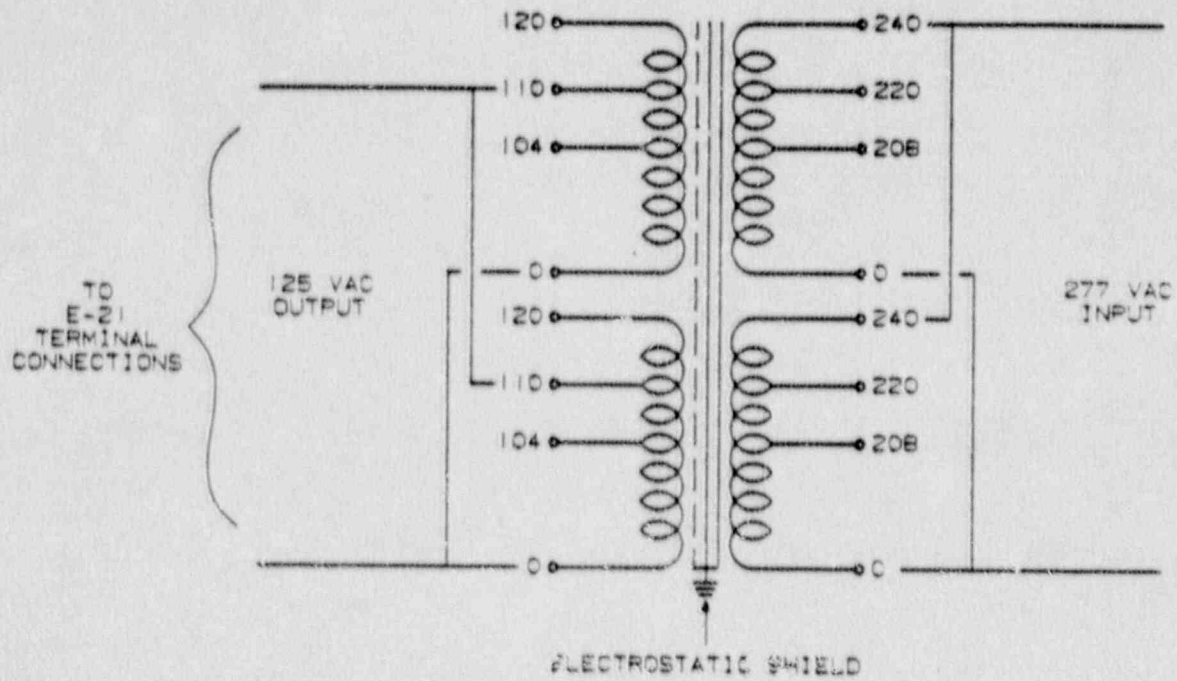


Figure 5-9. Transformer Connection for the 125 Vac Fault Source

037-A-24435-1B

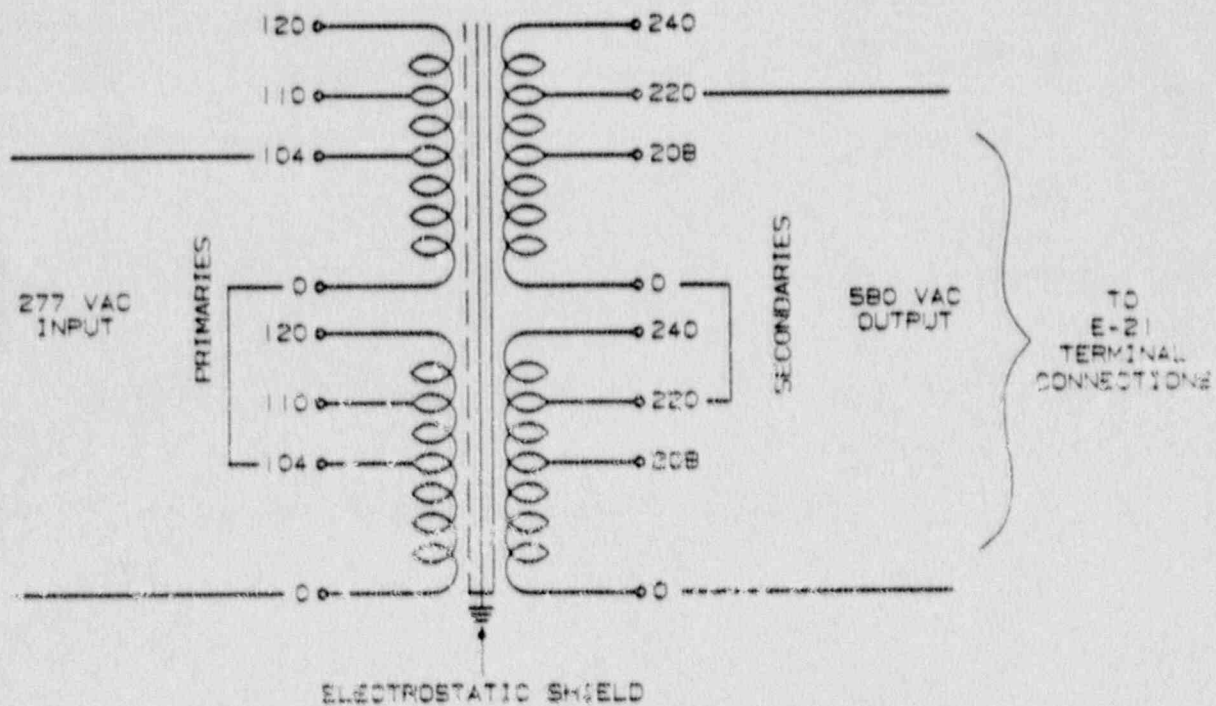


Figure 5-10. Transformer Connection for the 580 Vac Fault Source

037-24435-20

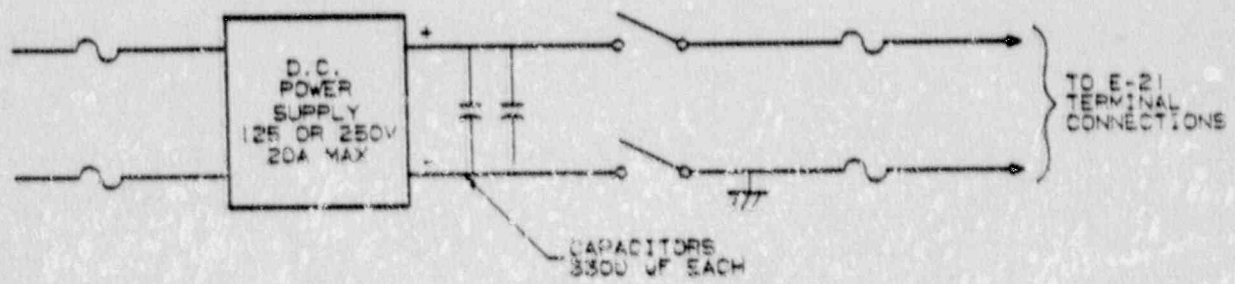


Figure 5-11. Dc Power Supply Fault Connections

Each fault test consisted of a 1-minute pretest run, a 1-minute application of fault and a 1-minute post-test run. Repairs required following each fault test were recorded noting all failed components.

For a detailed description of the fault test setup, see section 6.2.2.

For detailed test sequence, channel monitoring, and system external connection information, see the fault test procedure in Appendix C.

5.3 SURGE WITHSTAND CAPABILITY (SWC) TEST

The SWC tests were conducted under normal operating conditions of the system in accordance with IEEE 472-1974. The purpose of this test was to determine: (1) the protective actions of the Eagle 21™ system are not affected by application of the surge withstand test wave to the designated class non-1E to class 1E isolators, (2) that no component failures occurred, and (3) that no change in channel calibrations occurred due to the application of the surge withstand test wave.

5.3.1 Test Outline

All system inputs/outputs were surge tested in the common and transverse modes including the system power supply input circuitry.

Each of the following system interfaces were tested:

- o Digital Contact Output (NO and NC configurations), class non-1E/1E isolator
- o Partial Trip Output (energized and deenergized conditions), class non-1E/1E isolator
- o Current Loop Output 10-50 mA, class non-1E/1E isolator
- o Current Loop Input (4-20 mA, 10-50 mA, with and without loop power supply)
- o WR RTD Input

- o WR RTD Input (0-10 volt application)
- o NR RTD Input
- o Cabinet AC power feed

5.3.1.1 Common Mode Test

For this test, one terminal of the test generator was connected to each system input or output connection group. The other terminal of the test generator was connected to the ground of the surge generator (See figure 5-12a).

5.3.1.2 Transverse Mode Test

For this test, the terminals of the test generator were connected to the high and low of each system input or output signal pair (See figure 5-12b).

5.3.2 Test Implementation

The surge withstand capability test was carried out by using a surge generator [] and an isolation network [].

The SWC test wave generated was in accordance with IEEE-472-1974 and had the following characteristics:

- $E_{CREST} = 2.5kV$
- Surge Frequency = 2.25 MHz
- Time to $1/2 E_{CREST} = 6.4 \mu s$
- Repetition Frequency = 120 Hz

Each SWC test run consisted of a 2-minute pretest run, 2-second application of the SWC test wave, and a 2-minute post-test run.

Figure 5-12c shows a schematic diagram of the equipment connections which were implemented during the SWC test.

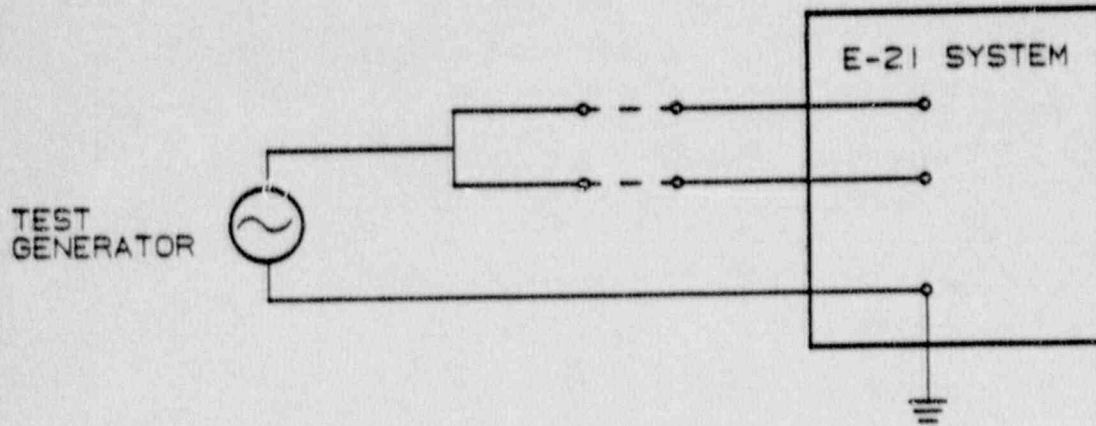


Figure 5-12a. Common Mode Surge Withstand Capability Test Connection

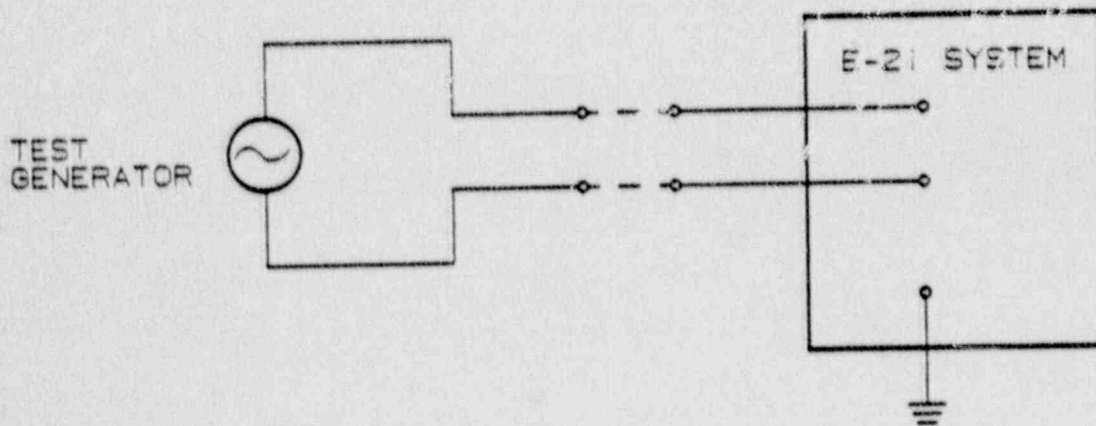


Figure 5-12b. Transverse Mode Surge Withstand Capability Test Connection



c

Figure 5-12c. Block Diagram of Surge Withstand Capability (SWC) Test

A detailed description of the SWC test implementation is given in the SWC Test Setup Description, section 6.2.3.

For detailed test sequence, channel monitoring, and system external connection information, see the SWC test procedure in appendix C.

5.4 RADIO FREQUENCY INTERFERENCE (RFI) SUSCEPTIBILITY TEST

The purpose of this RFI susceptibility test was to evaluate the performance of the system when subjected to electromagnetic fields such as those generated from portable radio transceivers or any other devices that generate continuous-wave radiated electromagnetic energy.

5.4.1 Test Methodology

The RFI susceptibility tests were conducted in accordance with SAMA Standard PMC 33.1-1978. The classes of field strengths the system was subjected to were 3 V/m and 10 V/m over the entire frequency range of 20 MHz to 1 GHz.

Two types of tests were performed. In the first, referred to as a "modulation" test, a computer-controlled sweep of the signal generator was utilized, [

] b, c In the second test, referred to as a "keying" test, the signal generator output was turned on and off at 1-second intervals and with very short rise and fall times to simulate the keying of a transceiver.

5.4.2 Test Location

The tests were carried out in a shielded enclosure (anechoic chamber) [

] c

5.4.3 Test Equipment

Two types of antennae were used during the testing. A biconical antenna covered frequencies ranging from 20 MHz to 160 MHz, and a log periodic antenna covered frequencies ranging from 160 MHz to 1 GHz.

Two power amplifiers were used to cover the whole frequency range. The first amplifier covered 20 MHz to 500 MHz; the second amplifier covered 500 MHz to 1 GHz.

[

]

b,c

5.4.4 Test Procedure

Calibration testing was conducted to generate a calibration data file for the control computer for the signal generator. Once calibration testing was completed, modulation and keying tests were performed on the system.

A detailed description of the radio frequency interference test implementation is given in the Radio Frequency Interference Test Setup Description (section 6.2.4).

For detailed test sequence, channel monitoring, and system external connection information, see the Radio Frequency Interference test procedure in appendix C.

5.4.5 Calibration Test

The calibration data files were generated for 3 V/m and 10 V/m over the entire frequency band (20 MHz to 1 GHz), for both vertical and horizontal polarizations, for use in implementing the modulation and keying tests. Figure 5-14 is a photo of the anechoic chamber showing the log periodic antenna in the horizontal polarization calibration [

].c

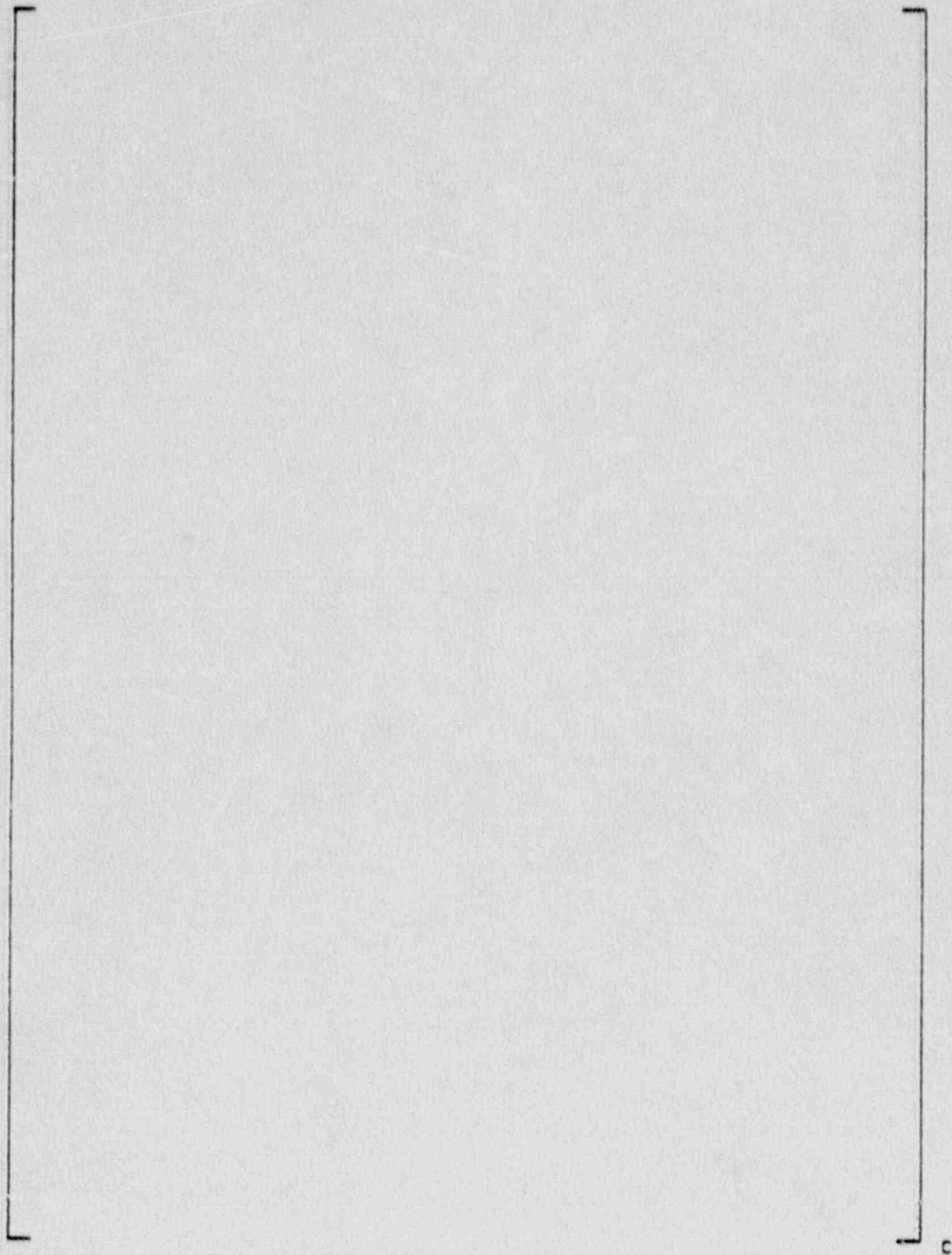


Figure 5-13. Radio Frequency Interference Equipment Test Setup

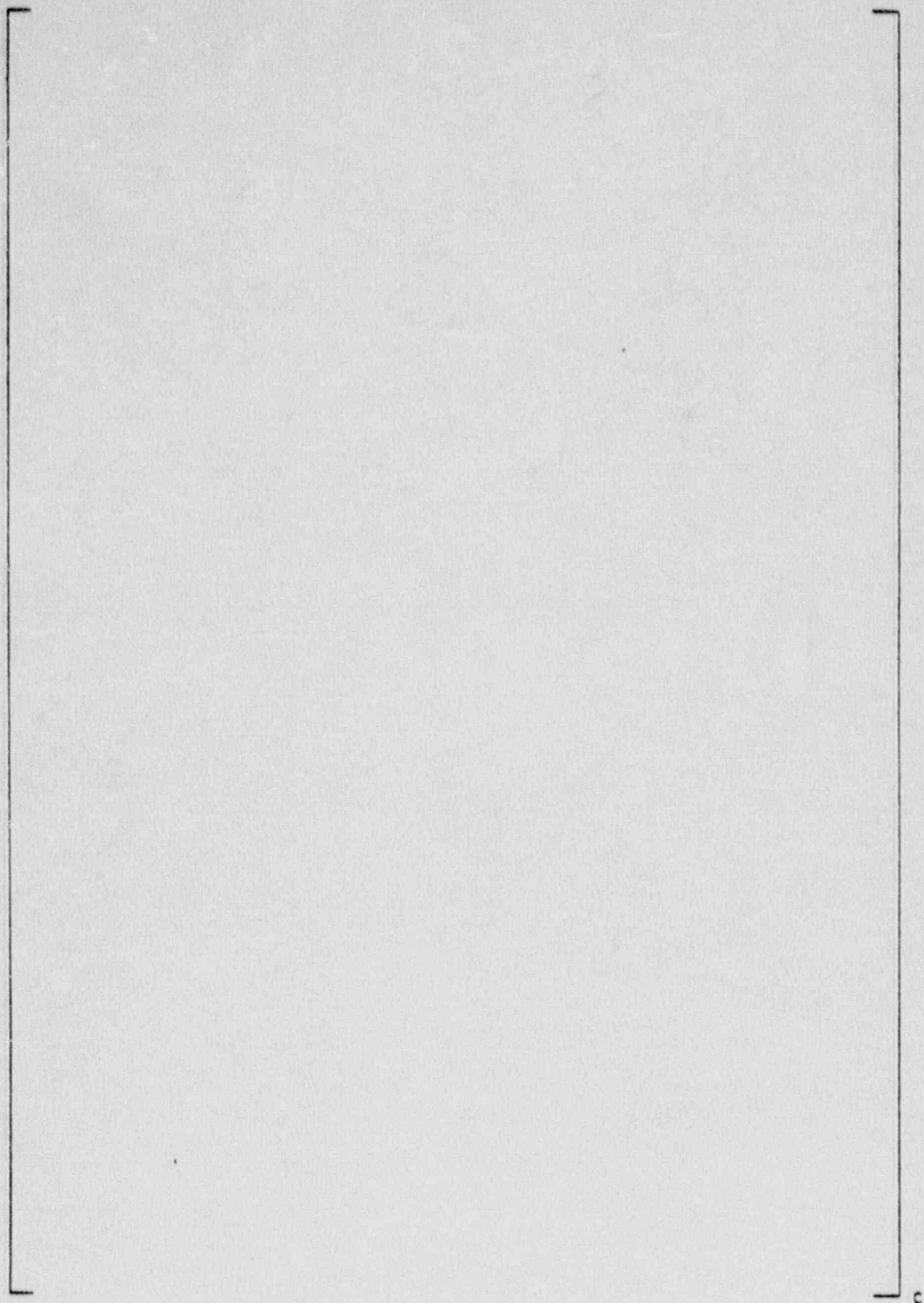


Figure 5-14. Radio Frequency Field Calibration

[

]

b,c

5.4.6 Modulation Test

[

]

b,c

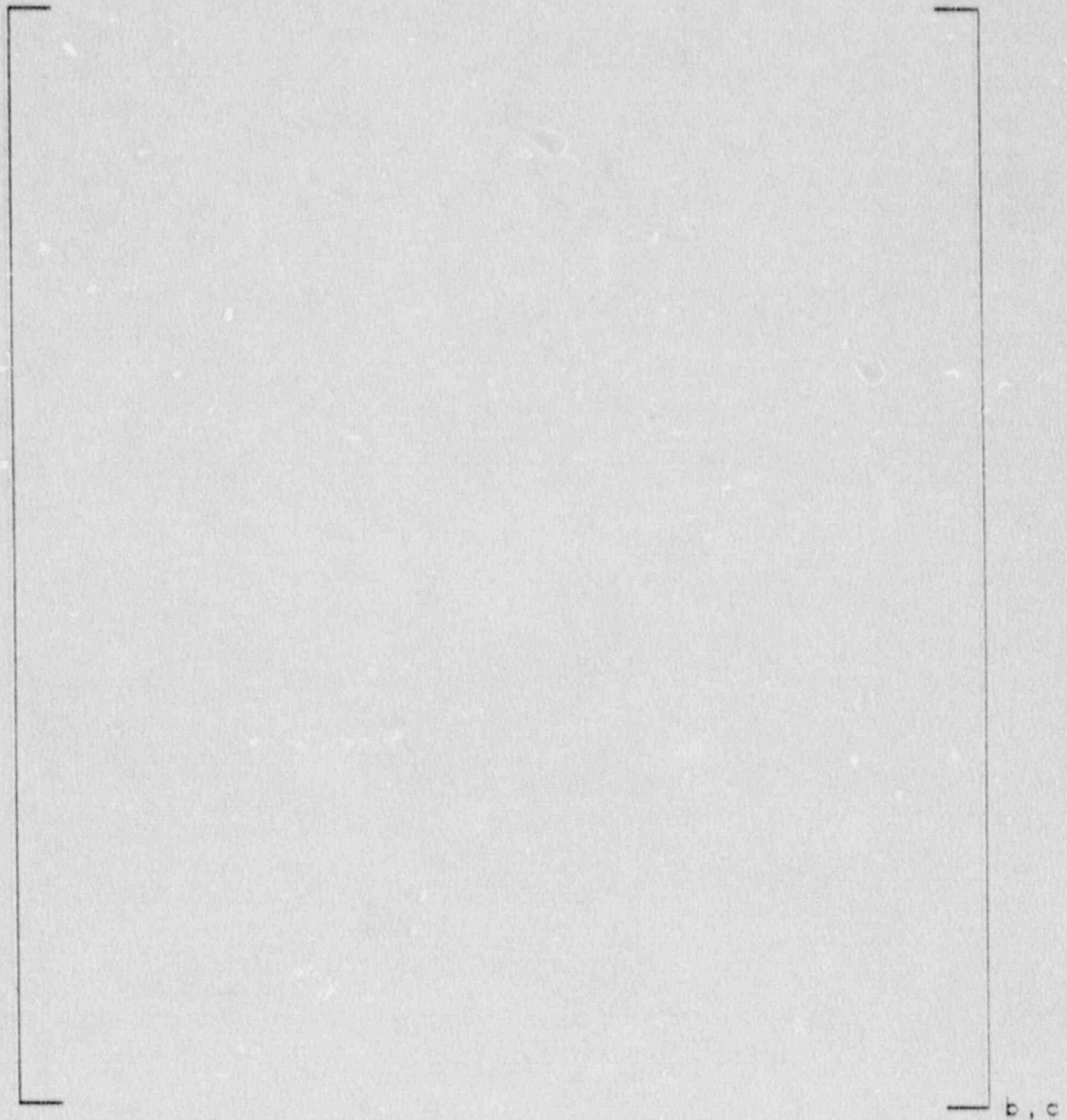


Figure 5-15. Block Diagram of Radio Frequency Interference Calibration Tests

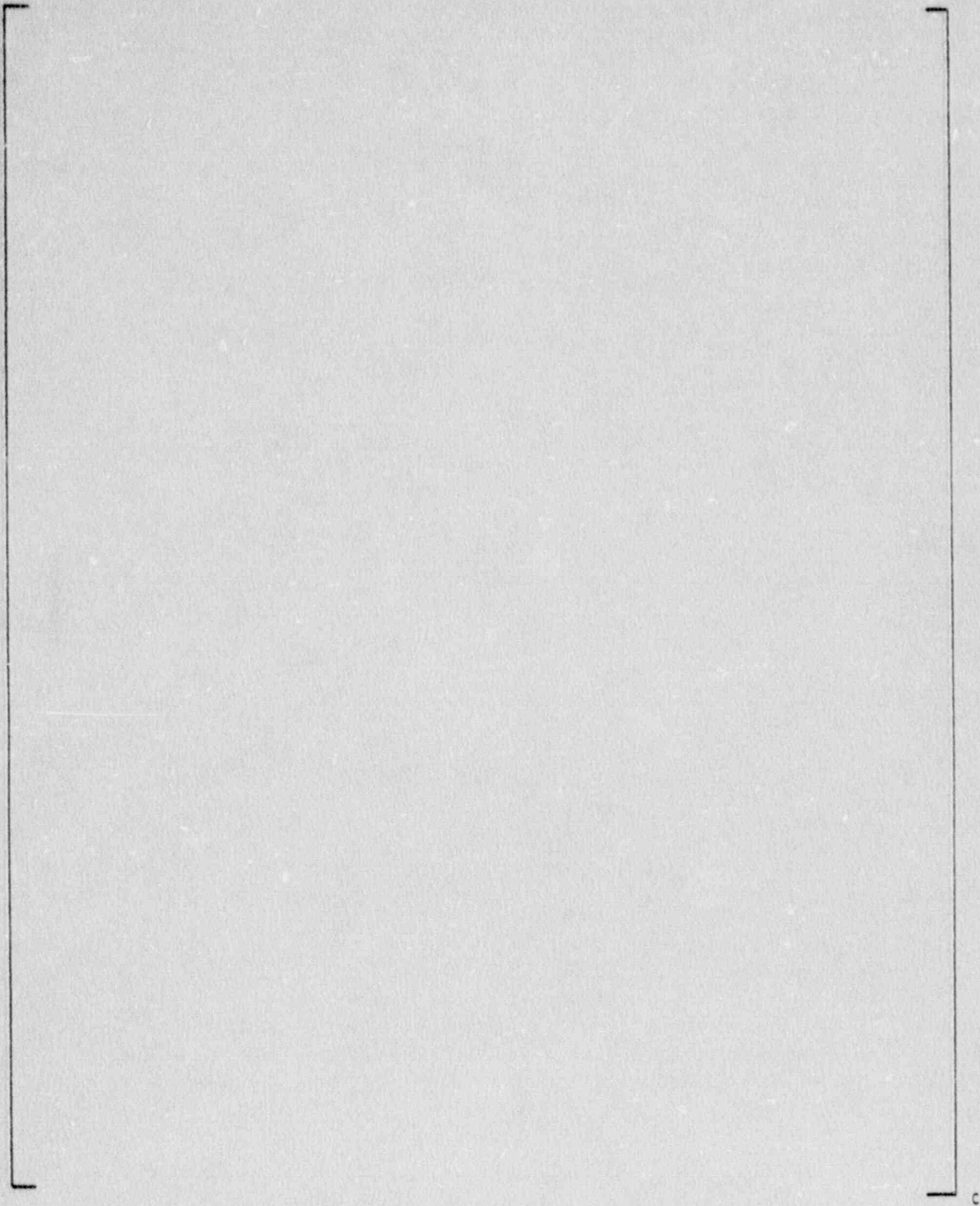


Figure 5-16. Cabinet Subject to Radio Frequency Field

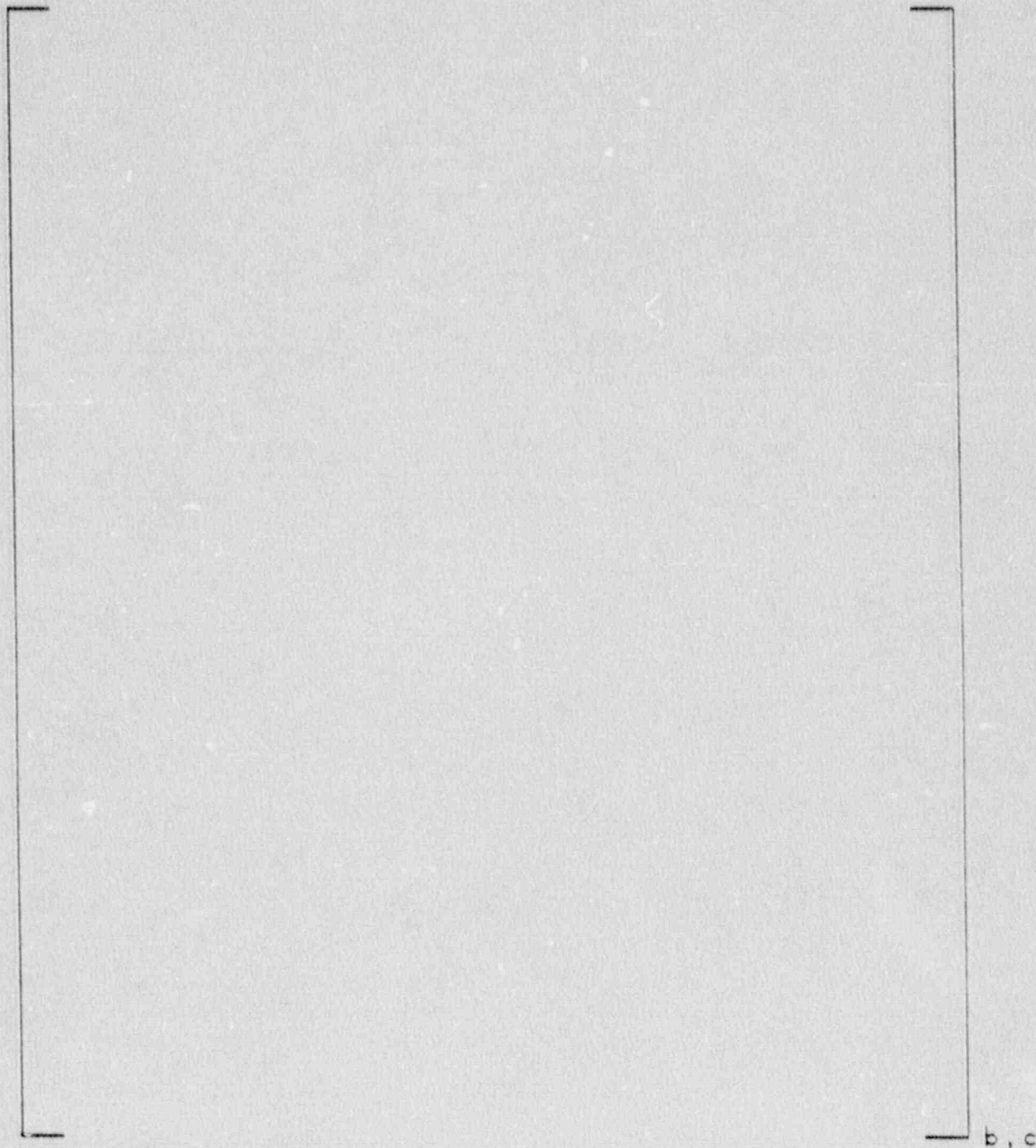


Figure 5-17. Block Diagram of Radio Frequency Interference Modulation Tests

[

A detailed description of the RFI test implementation is given in the RFI Test Setup Description, Section 6.2.4.

For detailed test sequence, channel monitoring, and system external connection information, see the RFI test procedure in Appendix C.

5.4.7 Keying Test

The keying test frequency selection was performed manually. The most susceptible points, as determined by the modulation tests, were subjected to the keying test. At least three data points per octave were tested. Table 5-2 shows the keying test frequencies.

]

TABLE 5-2
KEYING TEST FREQUENCIES

b,c

[

]

b,c

During the keying test, only the front of the cabinet was targeted, because this was considered to be the "most susceptible side" to the RF field. Vertical and horizontal polarizations were implemented.

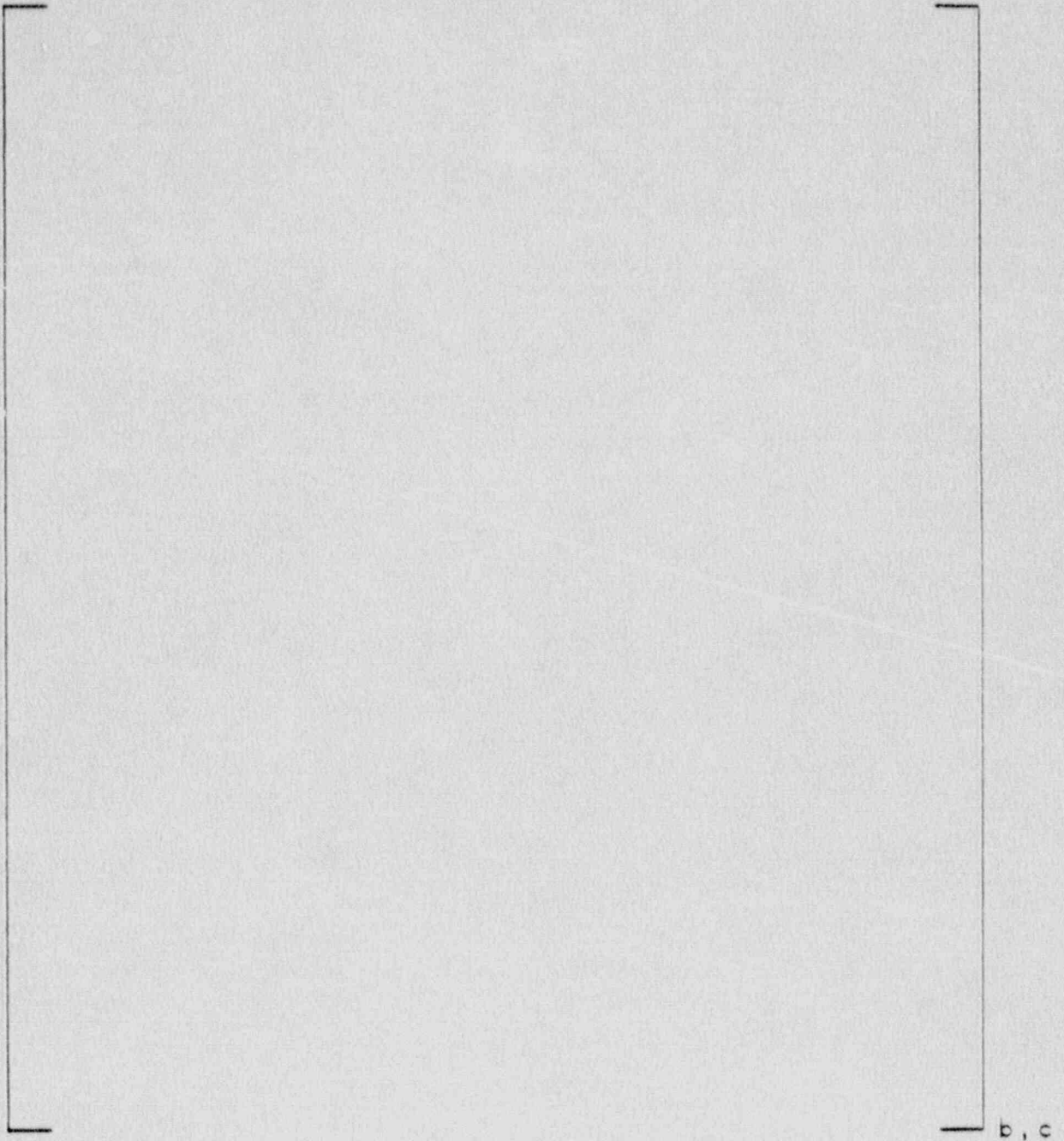


Figure 5-18. Block Diagram of Radio Frequency Interference Keying Tests

SECTION 6

TEST SETUP AND MONITORING

6.1 TEST SETUP

The test setup consisted of an input/output simulator and recording test station. Test equipment included a data logger, tape recorder strip chart recorder, voltmeter, and an oscilloscope. Figure 6-1 shows the cabinet and field cable setup. Figure 6-2 shows the test equipment setup. Figure 6-3 is a test configuration block diagram.

6.1.1 System Connections

Forty-foot field cables were routed from the test station through the cabinet top entry and were terminated at the field terminal blocks. Cable shields were terminated at the field terminal blocks and left open at the test station per standard wiring practice. All cables were bundled together (1E and non-1E) upon entry into the cabinet. System external connection diagrams are provided in section 3.

6.1.2 Simulated Input Signals

Input signals were simulated in a manner which replicates, as close as possible, actual plant sensors. The listing below gives signal type, simulation method, and circuit figure reference:

<u>Input Signal Type</u>	<u>Simulation Method</u>	<u>Figure</u>
0 - 10V	Voltage source	N/A
4-20 mA/10-50 mA	Transmitter	6-4
Wide Range RTD	Potentiometer	6-5
Narrow Range RTD	Precision resistor network	6-6

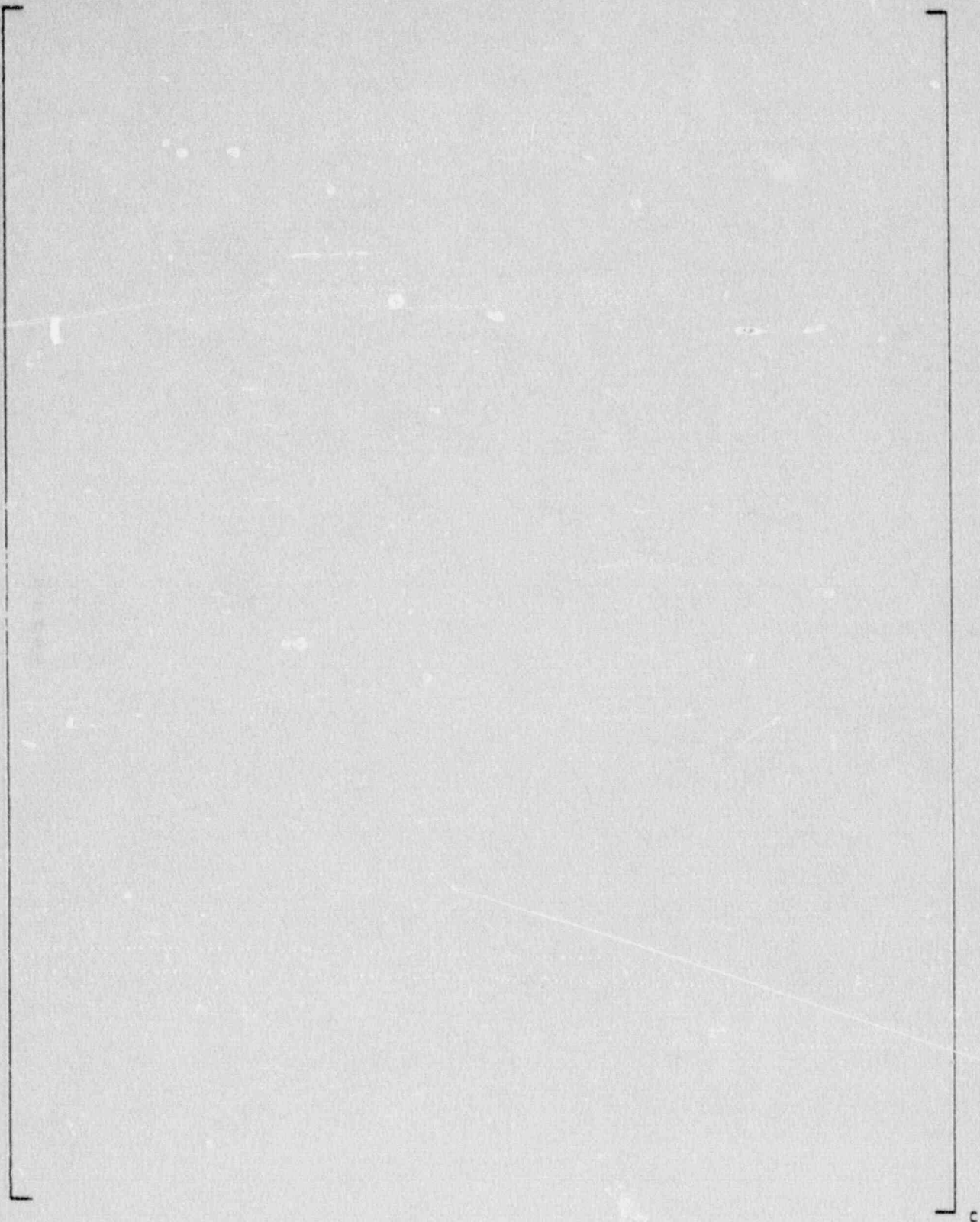


Figure 6-1. Cabinet and Field Cable Setup

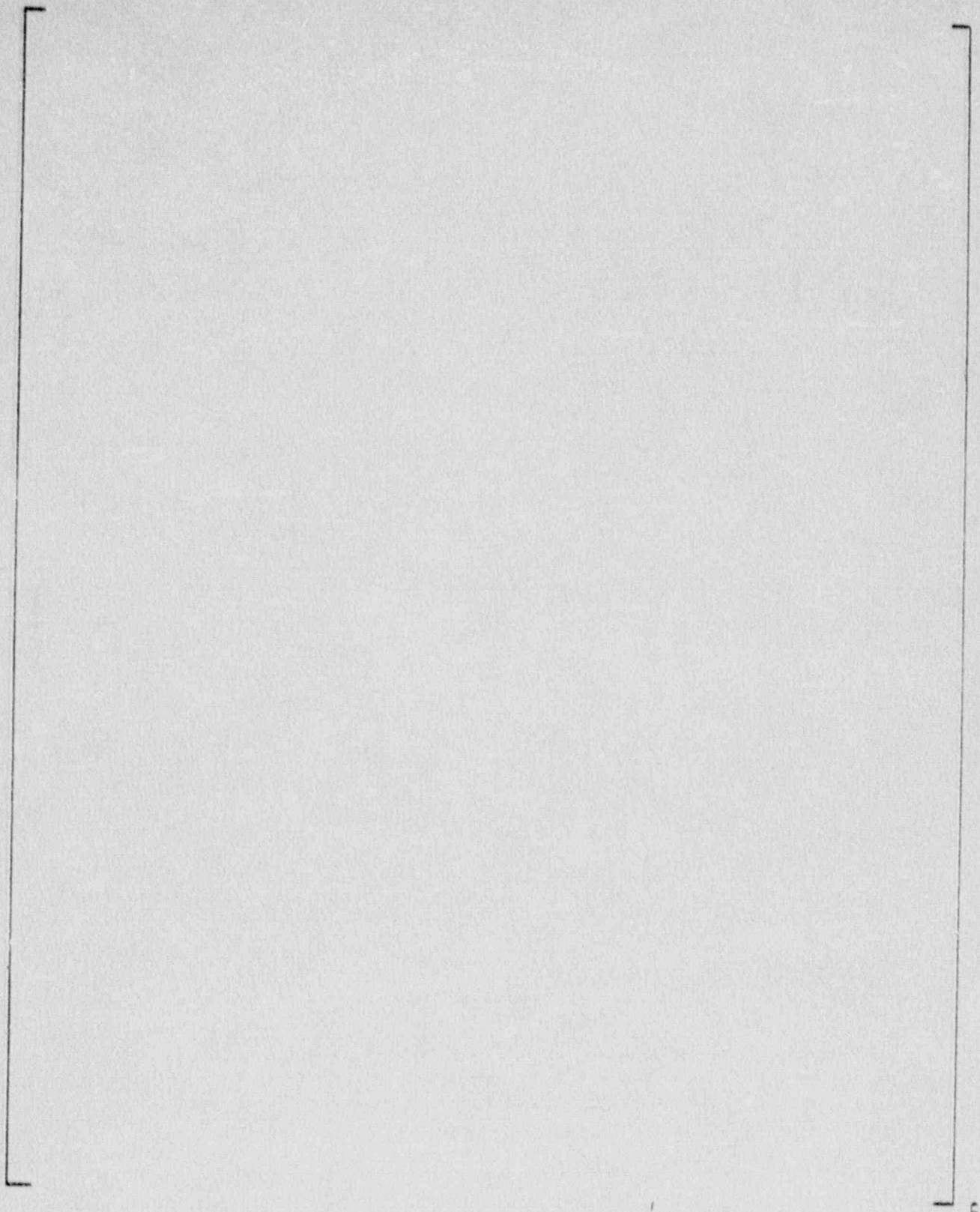


Figure 6-2. Test Equipment Setup

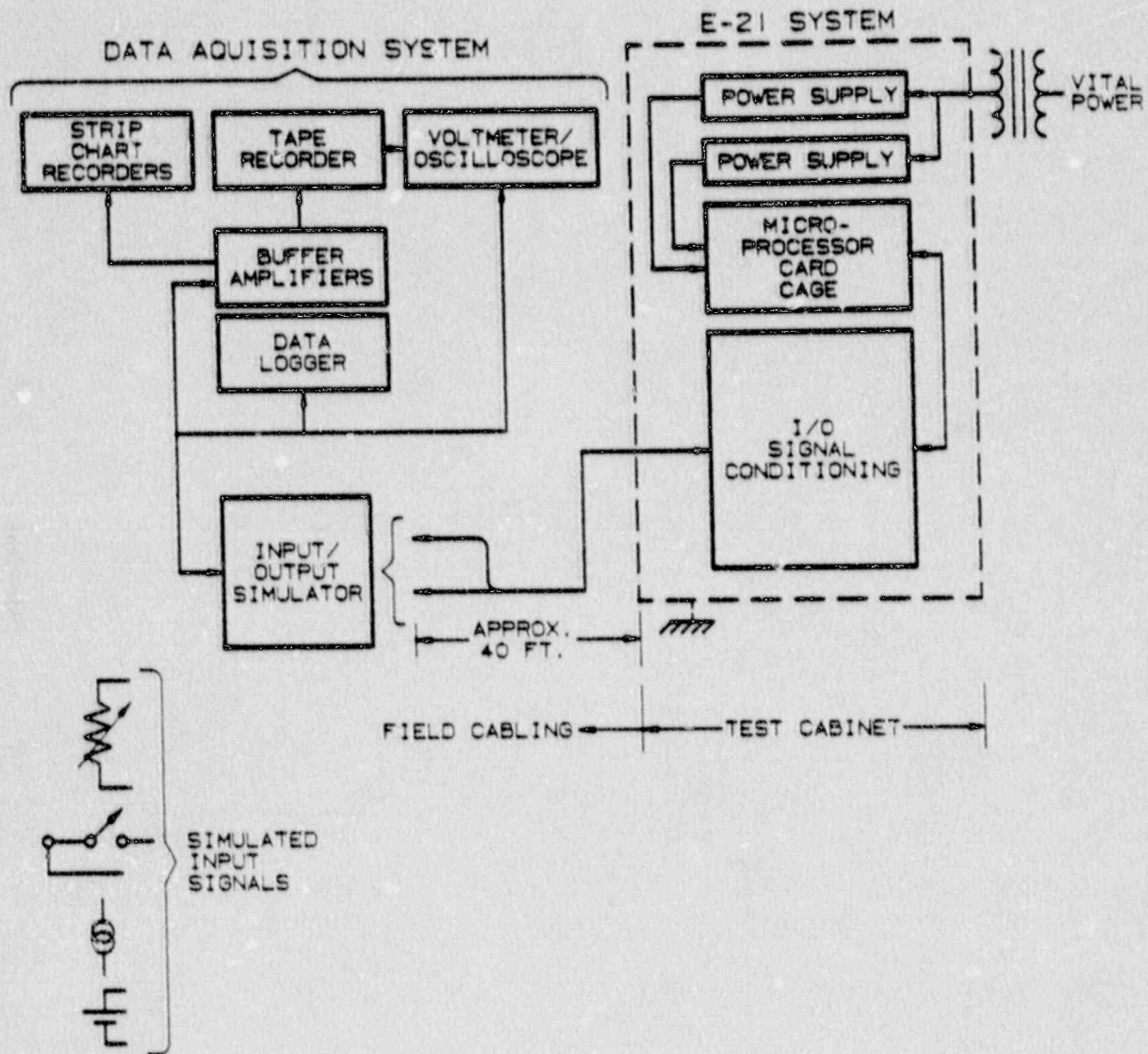


Figure 6-3. Test Configuration Block Diagram

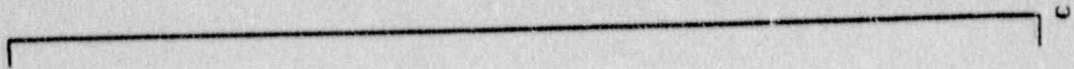


Figure 6-4. 4-50 mA Transmitter

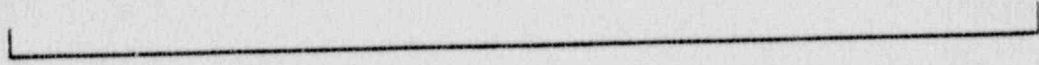




Figure 6-5. Wide Range Resistance Temperature Detector (RTD)

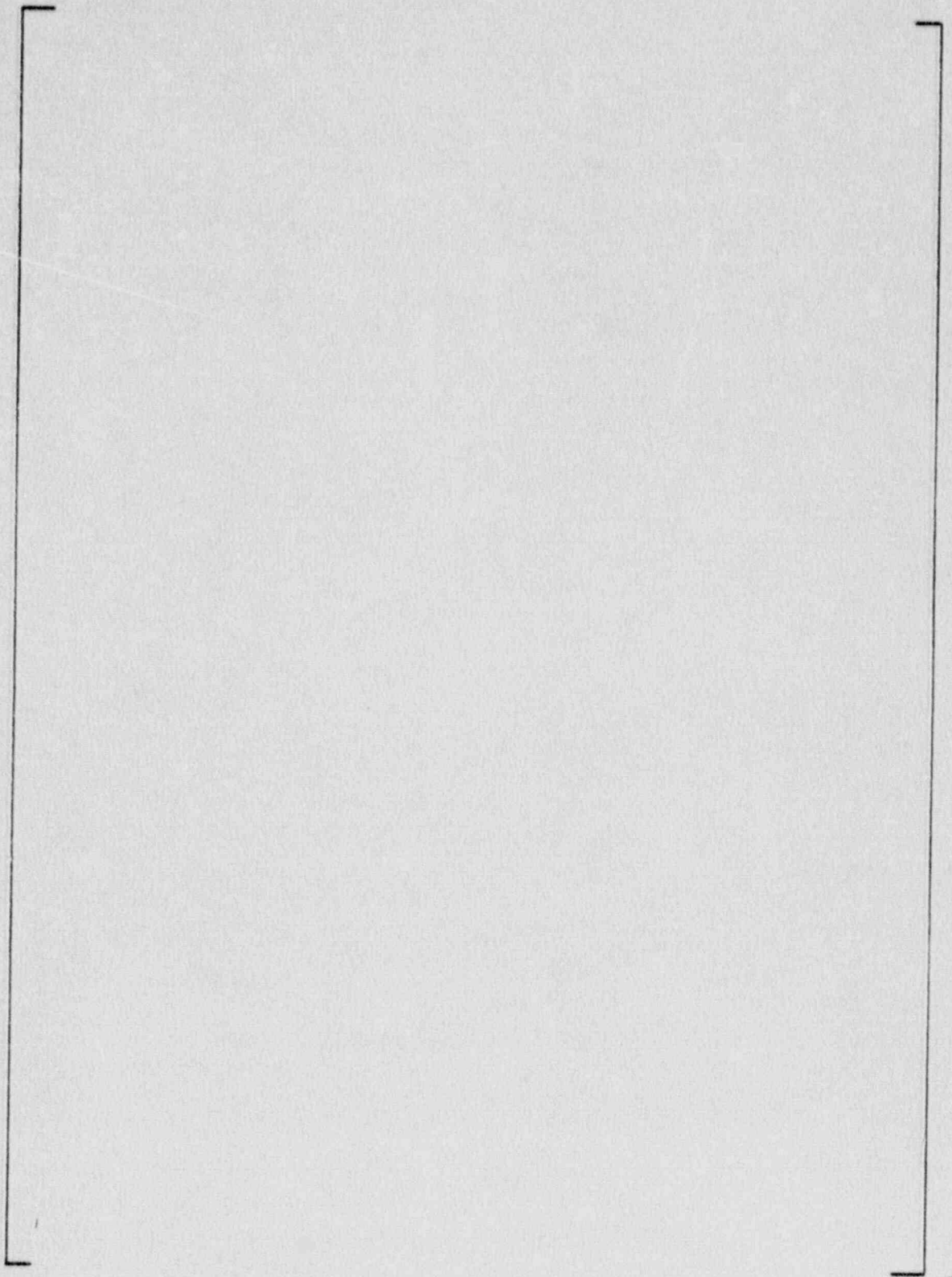


Figure 6-6. Narrow Range Resistance Temperature Detector (RTD)

Actual simulated input values for each test are specified in the test procedures, appendix C.

6.1.3 Data Acquisition System

The data acquisition system provided a record of cabinet performance during each test. The data acquisition system consisted of a tape recorder, strip chart recorder and a data logger.

The listing below gives output signal type, monitoring method, and circuit figure reference:

<u>Output Signal Type</u>	<u>Monitoring Method</u>	<u>Figure</u>
10 - 50 mA	resistor	6-7
Trip Output	120 Vac detector, status light	6-8
Contact Output	voltage/resistor	6-9

Actual output points monitored for each test are specified in the test procedures, appendix C.

6.1.3.1 Tape Recorder

A 14-channel FM tape recorder was used to provide a permanent record of system performance before, during and after each abnormal event (noise, surge, RFI, etc.). [

]b,c

Tape recorder monitored signals were processed through buffer amplifiers.

6.1.3.2 Data Logger

The digital data logger was used for pre-test and post-test verification of system status. Prior to each test, it was used to generate a printout for all

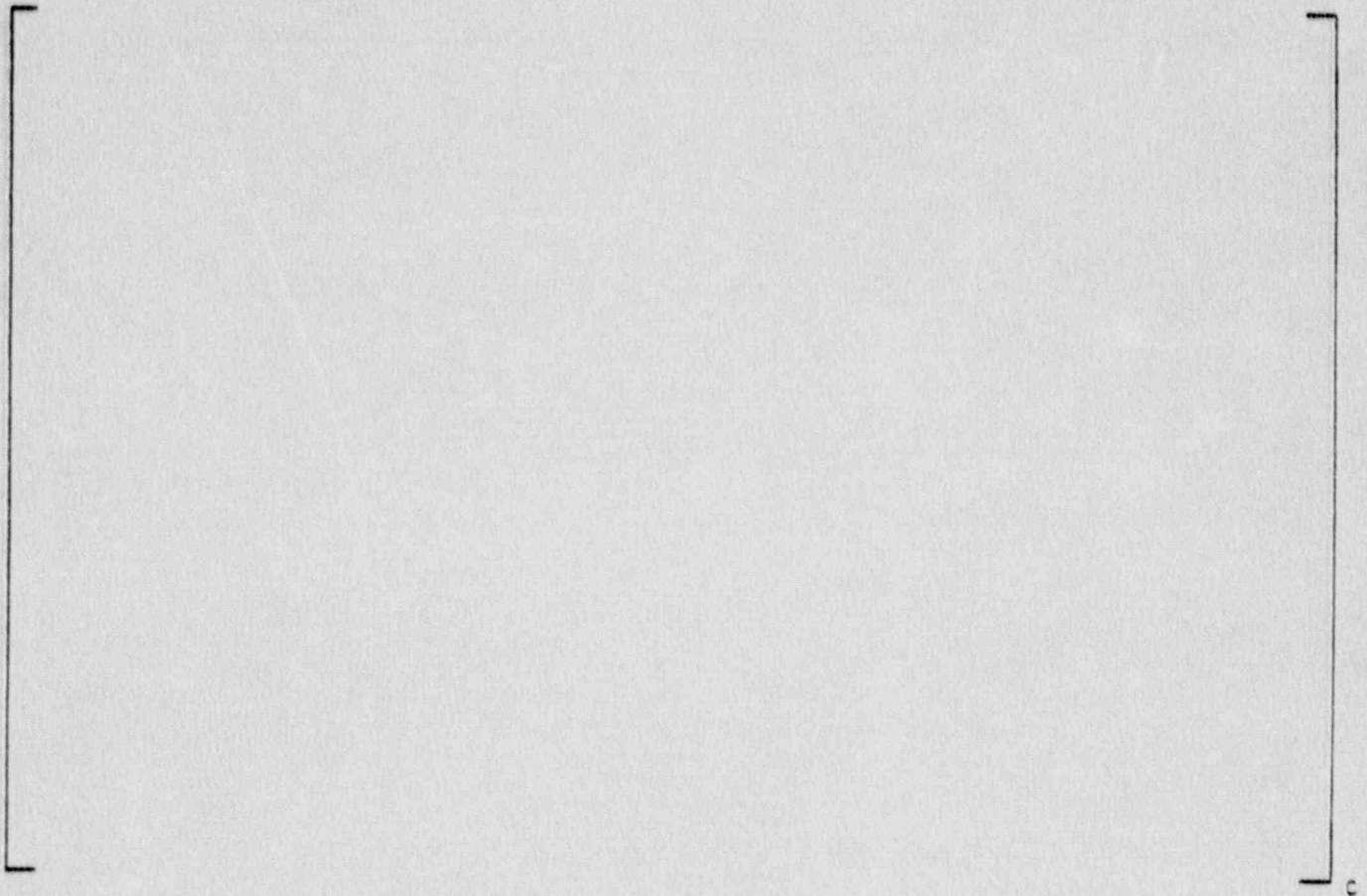


Figure 6-7. 10-50 mA Current Loop Output Monitoring

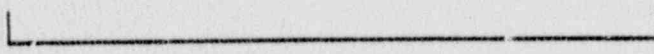
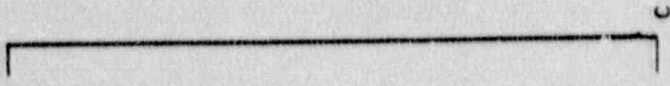


Figure 6-8. Trip Output Monitoring

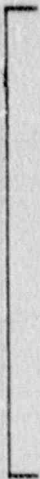


Figure 6-9. Contact Output Monitoring

monitored channels to verify that system performance was normal. After each test, another printout of the data for all monitored channels was generated to verify that system performance had not degraded during testing. These printouts were then attached to the backs of the data sheets. To prevent noise spikes caused by periodic data sampling, the data logger was not connected during testing.

6.1.3.3 Strip Chart Recorder

Two 8-channel strip chart recorders were used as a continuous monitor of system performance before, during, and after each abnormal event. An event marker was used to mark the beginning and end of each abnormal event. The monitored signals were processed through buffer amplifiers. [

]b,c

6.2 TEST MONITORING

The tests were monitored in accordance with the acceptance criteria outlined in section 7. Selected system input/output points were monitored to measure system performance during the noise, fault, surge, and radio frequency interference testing. The man-machine interface (MMI) terminal was disconnected during the test runs. The MMI connection can be construed as an additional antenna. During actual plant operation, the MMI is only connected during cabinet testing and only one protection set is allowed in test at a time. Thus, the MMI connection is not considered common mode [

]b,c The MMI was connected periodically to trouble-shoot and interrogate input signal processing performance.

Specific data points monitored were determined by the particular test being performed. In general, points monitored were chosen to best monitor overall Eagle 21™ system performance.

Data sheets, strip chart recorder printouts, data logger printouts, and tape recorder log sheets were utilized to record data. Data sheets are attached at the end of this section for information.

6.2.1 Noise Test Setup Description

Eagle 21™ system input/output performance, while subjected to the noise tests described in section 5.1, was monitored in the following manner:

- o Analog outputs -- Four analog output channels were monitored continuously during the noise tests. The channels monitored replicated signals processed by current loop, wide range RTD, and narrow range RTD input signal conditioning boards. Thus, system analog input/output processing performance was measured.
- o Digital outputs -- A single variable NR RTD (Thot3) was chosen to toggle all six Delta T/Tavg System trip outputs. All six trip output channels were toggled utilizing the variable RTD circuit shown in Figure 6-6. The control relay was cycled continuously during pre-test, test and post-test runs [

].^{b,c} The Delta T/Tavg system inputs were set just below and above the trip output toggle point (.2% or less). The Delta T/T_{avg} system utilizes current loop, NR RTD and 0-10 volt analog input signals to generate partial trip output signals (see section 3 for system block diagrams). Thus, any significant degradation in system input signal processing would result in a trip output status failure. A normally open contact output channel was also monitored. The contact output was normally energized throughout the test.

Trip output status was monitored continuously during the noise tests using a strip chart recorder.

Analog/digital channels adjacent to the non-1E channel under test were chosen for monitoring to emulate worst case system configuration. See figure 6-10 for the noise test data sheet.

EAGLE 21st NOISE TEST REPORT

TEST TYPE/PROCEDURE NUMBER (REV) _____

DATE _____

NOISE INJECTION CHANNEL NUMBER/TAG NO. _____

DATA LOGGER PRINTOUT:
(PRETEST/POST-TEST).

BISTABLE PERFORMANCE (PASS/FAIL): _____

REMARKS/OBSERVATIONS:

ANALOG OUTPUT NAME/TAG NO.	PRETEST		NOISE APPLIED		DC
	DC VALUE	P-P NOISE	DC VALUE	P-P NOISE	%DEV

PZR VAP/T454A

NR TEMP/T441L

NR TEMP/T441K

WR PRE/P408B

TAPE SET:

TAPE FOOTAGE:

(PRE-TEST/TEST/POST-TEST)

REMARKS/OBSERVATIONS:

PERFORMED BY/DATE:

Figure 6-10. Noise Test Data Sheet

6.2.2 Fault Test Setup Description

Eagle 21™ system performance, while subjected to the fault tests described in section 5.2, was monitored in the following manner:

- o Channels adjacent (left, right, top, bottom) to the channel under test were chosen for monitoring.
- o Minimum physical separation between the channel under test and adjacent channels was provided. Cabinet configuration was altered to provide minimum physical separation for the digital contact output board tests.
- o The channel under test was continuously monitored immediately prior to the fault application, disconnected from the data acquisition system (DAS) during fault application, and reconnected to the DAS upon removal of the fault.

Following the test, all necessary repairs were recorded noting all component failures and channel operability was verified.

Figure 6-11 is the fault test data sheet.

6.2.3 Surge Withstand Capability (SWC) Test Setup Description

Eagle 21™ system input/output performance, while subjected to the SWC tests described in section 5.3, was monitored in the following manner:

- o Analog outputs -- Four analog output channels were monitored continuously during the surge tests. The channels monitored replicated signals processed by current loop, wide range RTD, and narrow range RTD input signal conditioning boards. Thus, system analog input/output processing performance was measured.

I/O Module _____

Procedure Rev. _____

Date _____

Test # _____

TYPE

SHORT CIRCUIT _____, AC _____, DC _____

COMMON MODE _____ GROUND CONNECTED TO VOLTS PLUS _____ MINUS _____ GROUND

LINE TO LINE _____ VOLTS (+) TO (+) _____ (+) TO (-) _____
VOLTS (-) TO (+) _____ (-) TO (-) _____

TEST INJECTION POINT _____ TEST CONDITION _____

I/O CARD TYPE _____ POINT # _____

PRE-TEST

DATA LOGGER VERIFICATION* _____ PRINT OUTPUT # _____

SYSTEM STATUS _____

REMARKS AND TEST OBSERVATION _____

DISCONNECT DATA LOGGER _____

TEST

TAPE RECORDER FOOTAGE BEGIN _____ END _____ SET # _____
SPEED _____ TIME: (START): _____ (STOP): _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATION _____

POST-TEST

DATA LOGGER DATA VERIFICATION* PRINT OUTPUT # _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATION _____

PERFORMED _____ REVIEWED _____

Figure 6-11. Fault Test Data Sheet

- o Digital outputs -- A single variable NR RTD (Thot3) was chosen to toggle all six Delta T/Tavg system trip outputs. All six trip output channels were toggled utilizing the variable RTD circuit shown in Figure 6-6. The control relay was cycled continuously during pre-test, test, and post-test runs [

].^{b,c} The Delta T/Tavg system inputs were set just below and above the trip output toggle point (.2% or less). The Delta T/T_{avg} system utilizes current loop, NR RTD and 0-10 volt analog input signals to generate partial trip output signals (see section 3 for system block diagrams). Thus, any significant degradation in system input signal processing would result in a trip output status failure. The control relay was not cycled during the partial trip module tests to ensure that the channel in test remained in one state (energized/deenergized) during the application of the surge.

Trip output status was monitored continuously during the noise tests using a strip chart recorder.

The following test methods were utilized to best measure system performance:

- o Input/output channels adjacent to the output channel under test were monitored.
- o During application of the surge test wave, the strip chart recorder chart speed was increased to improve resolution.
- o Analog output channels replicating input channels under test were monitored.

Figure 6-12 is the Surge Test Data Sheet.

SURGE TEST DATA SHEET

Procedure Rev. _____
DATE _____
TEST # _____

TYPE _____

TRANSVERSE MODE _____

COMMON MODE _____

TEST INJECTION POINT _____ I/O CARD TYPE _____ POINT # _____

PRE-TEST

DATA LOGGER VERIFICATION PRINT OUTPUT # _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATION _____

DISCONNECT DATA LOGGER _____

TEST

TAPE RECORDER FOOTAGE BEGIN _____ END _____ SET # _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATIONS: _____

POST-TEST

DATA LOGGER DATA VERIFICATION* PRINT OUTPUT # _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATION: _____

PERFORMED _____ REVIEWED _____

Figure 6-12. Surge Test Data Sheet

6.2.4 Radio Frequency Interference Test Setup Description

Eagle 21™ system input/output performance, while subjected to RFI, was monitored in the following manner:

- o Analog outputs -- Four analog output channels were monitored continuously during the RFI test. The channels monitored replicated signals processed by current loop, wide-range RTD, and narrow-range RTD input signal conditioning boards. Thus, system analog input/output processing performance was measured.
- o Digital outputs -- A single variable NR RTD (Thot3) was chosen to toggle all six Delta T/T_{avg} System trip outputs. All six trip output channels were toggled utilizing the variable RTD circuit shown in Figure 6-6. The control relay was cycled at the start of each frequency run, measuring trip output performance during the RFI event. The Delta T/T_{avg} system inputs were set just below and above the trip output toggle point (.2% or less). The Delta T/T_{avg} system utilizes current loop, NR RTD and 0-10 volt analog inputs to generate partial trip output signals (see section 3 for system block diagrams). Thus, any significant degradation in system input signal processing would result in a trip output status failure. A normally open contact output channel was also monitored. The contact output was normally energized throughout the test.

In addition to continuous monitoring via the strip chart recorder, trip output status was also sampled by the control computer before, during, and after energization of the control relay. Any discrepancies between actual and expected trip output status were flagged by an error message. See figures 6-13 and 6-14 for RFI modulation and keying test data sheets. Figure 6-15 is the Tape Recorder Log Sheet.

RADIO FREQUENCY INTERFERENCE TEST DATA

TARGET: (CABINET POSITION)
 CALIBRATION FILE:
 FIELD STRENGTH LEVEL: (V/m)
 TYPE OF ANTENNA: (LOG PERIODIC OR BICONICAL)
 ANTENNA POLARIZATION: (HORIZONTAL OR VERTICAL)

DATE: _____

TEST PERFORMED BY: _____

REVIEWED BY: _____

TAPE NAME:
 TAPE SET:

TAPE RECORDER START AT: (FOOT)

FREQUENCY: (MHZ)

(DATE)
 (TIME)

EVENT	DIG/INPUT
1	00 0011 (EXPECTED TRIP OUTPUT PATTERN)
2	11 1100
3	00 0011

REMARKS:

FREQUENCY: (MHZ)

(DATE)
 (TIME)

EVENT	DIG/INPUT
1	00 0011
2	11 1100
3	00 0011

REMARKS:

FREQUENCY: (MHZ)

(DATE)
 (TIME)

ERROR IN THE CHANGING CONDITION OF BISTABLE STATUS (TRIP OUTPUT ERROR MESSAGE)

EVENT	DIG/INPUT
1	00 0011
2	11 1101
3	00 0011

REMARKS:

ENDING TAPE RECORDER FOOTAGE FOR THIS SET OF DATA: (FOOT)

Figure 6-13. RFI Modulation Test Data Sheet

RADIO FREQUENCY INTERFERENCE TEST DATA

TARGET: (CABINET POSITION)
 FIELD STRENGTH LEVEL: (V/M)
 TYPE OF ANTENNA: (LOG PERIODIC OR BICONICAL)
 ANTENNA POLARIZATION: (HORIZONTAL OR VERTICAL)

DATE: _____

TEST PERFORMED BY: _____

REVIEWED BY: _____

TAPE NAME:

TAPE SET:

TAPE RECORDER START AT: (FOOT)

FREQUENCY: (MHZ)

(DATE)
(TIME)

(EXPECTED TRIP OUTPUT PATTERN)	EVENT	(FIRST KEY CYCLE)	(SECOND KEY CYCLE)
		DIG [K-OFF] INPUT	DIG [K-ON] INPUT
	1	00 0011	00 0011
	2	11 1100	11 1100

REMARKS:

FREQUENCY: (MHZ)

(DATE)
(TIME)

EVENT	DIG [K-OFF] INPUT	DIG [K-ON] INPUT
	1	00 0011
2	11 1100	11 1100

REMARKS:

FREQUENCY: (MHZ)

(DATE)
(TIME)

EVENT	DIG [K-OFF] INPUT	DIG [K-ON] INPUT
	1	00 0011
2	11 1100	11 1100

REMARKS:

ENDING TAPE RECORDER FOOTAGE FOR THIS SET OF DATA: (FOOT)

Figure 6-14. RFI Keying Test Data Sheet

SECTION 7

ACCEPTANCE CRITERIA

7.1 DESCRIPTION

The general acceptance criterion for the 1E safety-related system is that the system shall remain operational before, during, and after any one of the abnormal events described in Section 5 and listed below. Specific acceptance criteria for the noise, fault, surge withstand capability, and radio frequency interference tests are defined in the following paragraphs.

7.1.1 Noise Test Acceptance Criteria

The Eagle 21™ system shall remain operational and maintain protective action before, during, and after any credible noise event described in section 5.1.

7.1.2 Fault Test Acceptance Criteria

The Eagle 21™ system shall remain operational and maintain protective action before, during, and after the application of any credible faults as described in section 5.2. Faults shall not propagate across the class non-1E to class 1E isolation barrier or from channel to channel.

7.1.3 Surge Withstand Capability Test Acceptance Criteria

The Eagle 21™ system shall remain operational and maintain protective action before, during, and after application of the surge withstand test wave to the designated class non-1E to class 1-E isolators as described in section 5.3. In addition, no component damage or shift in calibration exceeding the specified accuracy of the board under test shall occur due to the application of the surge withstand test wave to any cabinet input/output excluding the test panel and MMI communications connections.

7.1.4 Radio Frequency Interference Test Acceptance Criteria

The Eagle 21™ system shall remain operational (i.e., continuous microprocessor operation) while exposed to the radio frequency interference tests described in section 5.4.

SECTION 8 TEST RESULTS

The results of the system noise, fault, surge, and RFI tests are based on the acceptance criteria defined in Section 7. System performance during these abnormal events is described in the ensuing sections. The results are reported in tabular format at the end of this section.

B.1 NOISE TEST RESULTS

Tables 8-1a through 8-1g report the results of the noise tests. Analog output noise in all cases was coupled wire-to-wire from the non-1E cabling to the 1E cabling or directly into the analog output channel. The noise did not affect analog input or digital output signal processing. Thus, protective action was maintained before, during, and after all credible noise events. In all cases the analog output signals returned to normal upon removal of the noise signal.

The test effects column of tables 8-1a through 8-1g reports the worst-case analog output signal shift for each test run.

A system performance summary is given below for each type of noise test:

<u>Noise Test</u>	<u>Worst Case Shift in Analog Output Signals</u>	<u>Results in Table</u>
Random	[]
Ac Chattering Relay		
Dc Chattering Relay		
Mil-Spec Noise #1		
Mil-Spec Noise #2		
High Voltage Transient		
Static		

The ac noise sources (ac chattering relay and Mil-spec noise #2) produced spiking on the analog output signal and an increase in the background noise level. There was no recorded shift in the nominal dc value. The random high-voltage transient and dc chattering relay noise sources produced a shift in nominal dc value and an increase in background noise level.

8.2 FAULT TEST RESULTS

Tables 8-2a and 8-2b report the results of the line-to-ground and the line-to-line fault tests. Class-1E isolation was maintained in all cases. Damage was limited to components located on the non-1E side of the isolator or the non-1E side of the isolation device. Analog output noise recorded was coupled wire-to-wire and was limited to a spike upon fault application in isolated instances. No effects were observed on the system input processing or trip/contact output processing subsystems. Thus, protective action was maintained before, during, and after fault application. Sections 8.2.1 and 8.2.2 summarize the test results of the final board designs (see section 3 for drawing references). Section 8.2.3 describes the board modifications required and tables 8-2a and 8-2b report the test results of the original board designs.

8.2.1 Line-to-Ground Fault

System Performance Summary:

<u>Board Type</u>	<u>Fault Voltage</u>	<u>Effects on Adjacent Channels</u>	<u>Damage</u>		
Current Loop Output 10-50 mA	125 Vac	[]		
	125 Vdc				
	250 Vdc				
	580 Vac				
Digital Contact Output	125 Vac			[]
	125 Vdc				
	250 Vdc				
	580 Vac				
			b,c		

<u>Board Type</u>	<u>Fault Voltage</u>	<u>Effects on Adjacent Channels</u>	<u>Damage</u>
Partial Trip Output	125 Vac 125 Vdc 250 Vdc 580 Vac	[] b,c

8.2.2 Line-to-Line Fault

System Performance Summary:

<u>Board Type</u>	<u>Fault Voltage</u>	<u>Effects on Adjacent Channels</u>	<u>Damage</u>
Current Loop Output 10-50 mA	125 Vac 125 Vdc 250 Vdc 580 Vac	[] b,c
Digital Contact Output	125 Vac 125 Vdc 250 Vdc 580 Vac		

<u>Board Type</u>	<u>Fault Voltage</u>	<u>Effects on Adjacent Channels</u>	<u>Damage</u>
Partial Trip Output	125 Vac 125 Vdc 250 Vdc 580 Vac	[] b,c

MOV = Metal Oxide Varistor
SSR = Solid State Relay

8.2.3 Board Modifications Required

During fault testing of the original contact output and partial trip output board designs, failures in transient suppression devices (metal oxide varistors, MOV) caused component rupture and damage to adjacent channel circuitry. Since the fault test acceptance criteria (section 7) state that adjacent channels shall not be affected by faults applied to a non-1E channel, modifications were required. Applicable fault retests were performed following the board modifications. The modifications by board type are summarized below.

8.2.3.1 Partial Trip Output (EPT) Board

The original EPT board design utilized line-to-ground and line-to-line MOVs []_{b,c} These MOVs failed and ruptured causing adjacent channel damage upon application of 250 Vdc and 580 Vac line-to-line and line-to-ground faults.

Design changes implemented to prevent MOV rupture are as follows. [

For more information concerning the EPT modifications see Appendix A.]_{b,c}

8.2.3.2 Digital Contact Output (ECO) Board

The original ECO board design utilized line-to-line MOVs []_{b,c} These MOVs failed and ruptured upon application of a 580 Vac line-to-line fault. Although there was no recorded degradation in adjacent channel performance, MOV material was sprayed on adjacent channel circuitry. Since the EPT board experienced adjacent channel failure due to MOV rupture, a design change was implemented to prevent MOV rupture. [

]_{b,c}

8.3 SURGE WITHSTAND CAPABILITY (SWC) TEST RESULTS

Table 8-3 reports the results of the SWC tests. No component failures occurred and there was no recorded changes in channel calibrations due to application of the SWC test wave. Protective action was maintained before, during, and after application of the SWC test wave to the designated class non-1E to class 1E isolators. Analog output noise recorded was coupled through the associated input signal conditioning channel while the surge was applied. Noise was radiatively, and conductively, coupled into the input

channel. This conclusion is substantiated by the fact that noise was recorded on the channel under test as well as on adjacent channels. Trip output status failures were caused by noise coupled through the NR RTD input channels. Since the trip outputs are a function of the NR RTD inputs, erroneous trip outputs did occur. In no case was a false triggering of a partial trip or contact output hardware module recorded. In all cases these modules provided the appropriate outputs per loop calculation processor request. Thus, adverse system performance was limited to the analog I/O processing subsystem. In all cases, the analog I/O processing subsystem returned to normal operation upon removal of the SWC test wave. The loop processor subsystem maintained continuous operation before, during, and after all SWC test cases.

The test effect column of Table 8-3 reports the maximum recorded shift from nominal of an analog output signal for a specified test.

8.3.1 Common Mode Tests

System Performance Summary:

<u>Type of I/O Board</u>	<u>Worst-Case Shift in Analog Output Signals</u>	<u>Component Damage, Calibration Shift</u>		
Wide-Range RTD Input	[] b,c		
Narrow-Range RTD Input				
WR RTD 0-10V Input				
Current Loop Input 10-50 mA, Active				
Current Loop Input 10-50 mA, Passive				
Current Loop Input 4-20 mA, Active				
Current Loop Output 10-50 mA				
[] b,c	

<u>Type of I/O Board (cont)</u>	<u>Worst Case Shift in Analog Output Signals</u>	<u>Component Damage, Calibration Shift</u>
AC Input, Cabinet Power Partial Trip Output Digital Contact Output	[] b,c

8.3.2 Transverse Mode Tests

System Performance Summary:

<u>Type of I/O Board</u>	<u>Worst Case Shift in Analog Output Signals</u>	<u>Component Damage, Calibration Shift</u>
Wide-Range RTD Input Narrow-Range RTD Input WR RTD 0-10V Input Current Loop Input 10-50 mA, Active Current Loop Input 10-50 mA, Passive Current Loop Input 4-20 mA, Active Current Loop Output, 10-50 mA Ac Input, Cabinet Power Partial Trip Output Digital Contact Output	[] b,c

8.3.3 Board Modifications/Retest

The digital contact output and partial trip output boards experienced failures during the fault tests. See section 8.2 for a report on the required board modifications. These modifications were made to the transient voltage suppression circuitry on these boards.

The contact output board was retested to verify compliance with IEEE-472-1974. Only transverse mode transient suppression across open contacts was affected by the the modifications. Retests S57 and S58 were performed following the modifications to verify board performance.

The partial trip output board common and transverse mode transient suppression circuitry was modified. An analysis was performed (appendix A) in lieu of retesting and supports the original SWC tests, S13-S16.

8.4 RADIO FREQUENCY (RF) INTERFERENCE TEST RESULTS

Tables 8-4a and 8-4b report the results of the RF modulation and keying tests. In general, analog output noise recorded was coupled through the associated input signal conditioning channel. At isolated low frequencies (100 MHz or less) some noise was coupled directly into the analog output channel. Trip output status failures were caused by noise coupled through the NR RTD input channels. Since the trip outputs are a function of the NR RTD inputs, erroneous trip outputs did occur. In no case was a false triggering of a partial trip or contact output hardware module recorded. In all cases, these modules provided the appropriate outputs per loop calculation processor request. Thus, adverse system performance was limited to the analog I/O processing subsystem. In all cases the analog I/O processing subsystem returned to normal operation upon removal of the RF field. The loop processor subsystem maintained continuous operation before, during, and after all modulation and keying test cases.

The two noise coupling paths (input and output) produced different recorded noise characteristics. The noise coupled through the inputs was most severe at the start and end of each frequency test run. The noise consisted of a spike upon application of the RF field, followed by a period of reduced noise, and ending with a spike upon removal of the RF field. The keying test results summary reports the worst-case transient analog output signal shifts. Noise coupled directly into the analog output channel produced a shift in the nominal dc value and an increase in the background noise level throughout the affected frequency test run.

An additional test was performed to confirm that the noise coupled through the input channel was radiatively coupled and not conductively coupled. The RF signal generator was used to inject an ac coupled RF signal directly into the NR RTD input board with a nominal dc voltage applied to the input. The man-machine interface terminal was monitored during the noise injection and no effect on the input signal was observed. [

] b,c

The test effect column of Tables B-4a and B-4b reports the maximum recorded shift from nominal of an analog output signal over the frequency range specified and reports the frequencies at which trip output status failures occurred.

8.4.1 Modulation Tests

System Performance Summary:

<u>Frequency Band</u>	<u>Worst-Case Shift in Analog Output Signals</u>
20 - 160 MHz 160 - 500 MHz 500 - 1000 MHz	[] b,c
[]	[] b,c

8.4.2 Keying Tests

System Performance Summary:

<u>Frequency Band</u>	<u>Worst-Case Shift in Analog Output Signals</u>
20 - 160 MHz 160 - 500 MHz 500 - 1000 MHz	[]] b,c
[]] b,c

8.4.3 Cabinet Modifications Required

Modifications were made to the Eagle 21™ cabinet to improve system immunity to RFI. [

] b,c There modifications were made prior to the recording of final data shown in tables 8-4a and 8-4b.

TABLE 8-1a
RANDOM NOISE TESTS
(ANTENNA COUPLED)

<u>Test Number</u>	<u>Type of I/O Board</u>	<u>Test Effect</u>
N1	Partial Trip Output	<div style="border: 1px solid black; width: 300px; height: 100px; margin: auto;"></div> b,c
N2	10-50 mA Current Loop Output	
N3	Digital Contact Output NO, OC	
N4	Digital Contact Output NO, SC	
N5	Digital Contact Output NC, OC	
N6	Digital Contact Output NC, SC	

AOS = Analog Output Signal Shifts OC = Open Circuit NO = Normally Open
 TOF = Trip Output Failures SC = Short Circuit NC = Normally Closed

TABLE 8-1b
AC CROSSTALK NOISE TESTS - CHATTERING RELAYS

Test Number	Type of I/O Board	Test Effect
N7	Partial Trip Output, Ant Co.	<div style="display: flex; align-items: center; justify-content: center;"> <div style="border-left: 1px solid black; border-right: 1px solid black; border-top: 1px solid black; border-bottom: 1px solid black; width: 100px; height: 100px; margin-right: 10px;"></div> <div style="text-align: center;">b,c</div> </div>
N8	Partial Trip Output, Dir Co.	
N9	10-50 mA Current Loop Output, Ant Co.	
N10	10-50 mA Current Loop Output, Dir Co.	
N11	Digital Contact Output, NO, OC, Ant Co.	
N12	Digital Contact Output, NO, SC, Ant Co.	
N13	Digital Contact Output, NO, Dir Co.	
N14	Digital Contact Output, NC, OC, Ant Co.	
N15	Digital Contact Output, NC, SC, Ant Co.	

AOS = Analog Output Signal Shifts	OC = Open Circuit	NO = Normally Open	Ant Co. = Antenna Coupled
TOF = Trip Output Failures	SC = Short Circuit	NC = Normally Closed	Dir Co. = Direct Coupled

8-12

TABLE 8-1c
DC CROSSTALK NOISE TESTS - CHATTERING RELAYS

<u>Test Number</u>	<u>Type of I/O Board</u>	<u>Test Effect</u>
N16	Partial Trip Output, Ant Co.] b,c
N17	Partial Trip Output, Dir Co.	
N18	10-50 mA Current Loop Output, Ant Co	
N19	10-50 mA Current Loop Output, Dir Co.	
N20	Digital Contact Output, NO, OC, Ant Co.	
N21	Digital Contact Output, NO, SC, Ant Co.	
N22	Digital Contact Output, NO, Dir Co.	
N23	Digital Contact Output, NC, OC, Ant Co.	
N24	Digital Contact Output, NC, SC, Ant Co.	

AOS = Analog Output Signal Shifts OC = Open Circuit NO = Normally Open Ant Co. = Antenna Coupled
 TOF = Trip Output Failures SC = Short Circuit NC = Normally Closed Dir Co. = Direct Coupled

8-13

TABLE 8-1d
 MILITARY SPECIFICATION
 NOISE SOURCE #1 TESTS
 (ANTENNA COUPLED)

<u>Test Number</u>	<u>Type of I/O Board</u>	<u>Test Effect</u>
N25	Partial Trip Output	[] b,c
N26	10-50 mA Current Loop Output	
N27	Digital Contact Output, NO, OC	
N28	Digital Contact Output, NO, SC	
N29	Digital Contact Output, NC, OC	
N30	Digital Contact Output, NC, SC	

AOS = Analog Output Signal Shifts
 TOF = Trip Output Failures

OC = Open Circuit
 SC = Short Circuit

NO = Normally Open
 NC = Normally Closed

8-14

TABLE 8-1e
MILITARY SPECIFICATION
NOISE SOURCE #2 TESTS
(ANTENNA COUPLED)

<u>Test Number</u>	<u>Type of I/O Board</u>	<u>Test Effect</u>
N31	Partial Trip Output	<div style="display: flex; align-items: center; justify-content: center;"> <div style="border-left: 1px solid black; border-right: 1px solid black; height: 200px; margin-right: 5px;"></div> <div style="margin-right: 5px;">b,c</div> </div>
N32	10-50 mA Current Loop Output	
N33	Digital Contact Output, NO, OC	
N34	Digital Contact Output, NO, SC	
N35	Digital Contact Output, NC, OC	
N36	Digital Contact Output, NC, SC	

OC = Open Circuit
SC = Short Circuit

NO = Normally Open
NC = Normally Closed

8-1e

TABLE 8-1f
HIGH VOLTAGE TRANSIENT NOISE TESTS
(ANTENNA COUPLED)

Test Number	Type of I/O Board	Test Effect
N37	Partial Trip Output	[] b,c
N38	10-50 mA Current Loop Output	
N39	Digital Contact Output, NO, OC	
N40	Digital Contact Output, NO, SC	
N41	Digital Contact Output, NC, OC	
N42	Digital Contact Output, NC, SC	
AOS = Analog Output Signal Shifts TOF = Trip Output Failures		OC = Open Circuit SC = Short Circuit NO = Normally Open NC = Normally Closed

8-16

TABLE 8-1g
STATIC NOISE TESTS

<u>Test Number</u>	<u>Type of I/O Board</u>	<u>Test Effect</u>
N43	Partial Trip Output, Ant Co.] b,c
N44	Partial Trip Output, Dir Co.	
N45	10-50 mA Current Loop Output, Ant Co.	
N46	10-50 mA Current Loop Output, Dir Co.	
N47	Digital Contact Output, NO, OC, Ant Co.	
N48	Digital Contact Output, NO, SC, Ant Co.	
N49	Digital Contact Output, NO, Dir Co.	
N50	Digital Contact Output, NC, OC, Ant Co.	
N51	Digital Contact Output, NC, SC, Ant Co.	

OC = Open Circuit
SC = Short Circuit

NO = Normally Open
NC = Normally Closed

Ant Co. = Antenna Coupled
Dir Co. = Direct Coupled

8-17

TABLE B-2a
LINE-GROUND FAULT TESTS

Test No.	Voltage Level	Type of I/O Board	Test Connections	Effects on Adjacent Channels	Damage
F1	125 VAC	Current Loop Output, 10-50 mA	H to +		
F2	125 VAC	Current Loop Output, 10-50 mA	H to -		
F3	125 VDC	Current Loop Output, 10-50 mA	+ to +		
F4	125 VDC	Current Loop Output, 10-50 mA	+ to -		
F5	125 VDC	Current Loop Output, 10-50 mA	- to +		
F6	125 VDC	Current Loop Output, 10-50 mA	- to -		
F7	250 VDC	Current Loop Output, 10-50 mA	+ to +		
F8	250 VDC	Current Loop Output, 10-50 mA	+ to -		
F9	250 VDC	Current Loop Output, 10-50 mA	- to +		
F10	250 VDC	Current Loop Output, 10-50 mA	- to -		
F11	580 VAC	Current Loop Output, 10-50 mA	H to +		
F12	580 VAC	Current Loop Output, 10-50 mA	H to -		
F13	250 VDC	Digital Contact Output, EN	+ to NO		
F14	250 VDC	Digital Contact Output, EN	+ to NC		
F15	250 VDC	Digital Contact Output, EN	- to NO		
F16	250 VDC	Digital Contact Output, EN	- to NC		
F17	580 VAC	Digital Contact Output, EN	H to NO		
F18	580 VAC	Digital Contact Output, EN	H to NC		
F19	125 VAC	Partial Trip Output, EN	H to LO		
F20	125 VAC	Partial Trip Output, EN	H to HI		
F21	125 VDC	Partial Trip Output, EN	+ to LO		
F22	125 VDC	Partial Trip Output, EN	- to LO		
F23	125 VDC	Partial Trip Output, EN	+ to HI		
F24	125 VDC	Partial Trip Output, EN	- to HI		
*F25	250 VDC	Partial Trip Output, EN	- to HI		
*F26	250 VDC	Partial Trip Output, EN	+ to HI		

8-18

b,c

TABLE B-2a (Continued)
LINE-GROUND FAULT TESTS

Test No.	Voltage Level	Type of I/O Board	Test Connections	Effects on Adjacent Channels	Damage
*F27	250 VDC	Partial Trip Output, EN	+ to L0	[]
*F28	250 VDC	Partial Trip Output, EN	- to L0		
F29	250 VDC	Partial Trip Output, DEN	+ to HI		
F30	250 VDC	Partial Trip Output, EN	+ to HI		
F31	250 VDC	Partial Trip Output, EN	- to HI		
F32	250 VDC	Partial Trip Output, DEN	- to HI		
F33	250 VDC	Partial Trip Output, EN	- to L0		
F34	250 VDC	Partial Trip Output, DEN	- to L0		
F35	250 VDC	Partial Trip Output, EN	+ to L0		
F36	250 VDC	Partial Trip Output, DEN	+ to L0		
F37	580 VAC	Partial Trip Output, EN	H to L0		
F38	580 VAC	Partial Trip Output, DEN	H to L0		
F39	580 VAC	Partial Trip Output, EN	H to HI		
F40	580 VAC	Partial Trip Output, DEN	H to HI		

b,c

* - Tests of original partial trip output board design

EN = energized
DEN = Deenergized

NO = Normally Open
NC = Normally Closed

8-19

TABLE B-2b
LINE-TO-LINE TESTS

Test No.	Voltage Level	Type of I/O Board	Test Connections	Effects on Adjacent Channels	Damage
F41	125 VAC	Current Loop Output, 10-50 mA	H to +, N to -	[]
F42	125 VDC	Current Loop Output, 10-50 mA	+ to +, - to -		
F43	125 VDC	Current Loop Output, 10-50 mA	- to +, + to -		
F44	250 VDC	Current Loop Output, 10-50 mA	+ to +, - to -		
F45	250 VDC	Current Loop Output, 10-50 mA	- to +, + to -		
F46	580 VAC	Current Loop Output, 10-50 mA	H to +, N to -		
F47	250 VDC	Digital Contact Output, EN	+ to NC, - to C		
F48	250 VDC	Digital Contact Output, EN	- to NC, + to C		
*F49	580 VAC	Digital Contact Output, EN	H to NC, N to C		
F50	125 VAC	Digital Contact Output, EN	H to NO, N to C		
F51	125 VDC	Digital Contact Output, EN	+ to NO, - to C		
F52	125 VDC	Digital Contact Output, EN	- to NO, + to C		
F53	250 VDC	Digital Contact Output, EN	+ to NO, - to C		
F54	250 VDC	Digital Contact Output, EN	- to NO, + to C		
F55	580 VAC	Digital Contact Output, EN	H to NO, N to C		
F56	250 VDC	Digital Contact Output, DEN	+ to NO, - to C		
F57	250 VDC	Digital Contact Output, DEN	- to NO, + to C		
*F58	580 VAC	Digital Contact Output, DEN	H to NO, N to C		
F59	125 VAC	Digital Contact Output, DEN	H to NC, N to C		
F60	125 VDC	Digital Contact Output, DEN	+ to NC, - to C		
F61	125 VDC	Digital Contact Output, DEN	- to NC, + to C		
F62	250 VDC	Digital Contact Output, DEN	+ to NC, - to C		
F63	250 VDC	Digital Contact Output, DEN	- to NC, + to C		
F64	580 VAC	Digital Contact Output, DEN	H to NC, N to C		
F65	580 VAC	Digital Contact Output, DEN	H to NO, N to C		

8-20

b.c

TABLE B-2b (continued)
LINE-TO-LINE TESTS

Test No.	Voltage Level	Type of I/O Board	Test Connections	Effects on Adjacent Channels	Damage
F66	580 VAC	Digital Contact Output, EN	H to MC, N to C		
F67	125 VAC	Partial Trip Output, EN	H to HI, N to LO		
F68	125 VDC	Partial Trip Output, EN	+ to HI, - to LO		
F69	125 VDC	Partial Trip Output, EN	+ to LO, - to HI		
F70	250 VDC	Partial Trip Output, DEN	+ to LO, - to HI		
F71	250 VDC	Partial Trip Output, DEN	+ to HI, - to LO		
F72	250 VDC	Partial Trip Output, EN	+ to LO, - to HI		
F73	250 VDC	Partial Trip Output, EN	+ to HI, - to LO		
F74	580 VAC	Partial Trip Output, DEN	H to HI, N to LO		
F75	580 VAC	Partial Trip Output, EN	H to HI, N to LO		

circuit

** - Tests of original digital contact output Board Design

EN: energized

NO = Normally Open

DEN: Deenergized

NC = Normally Closed

b.c

TABLE B-3
SURGE WITHSTAND CAPABILITY (SWC) TESTS

Test No.	Test Mode	Type of I/O Board	Test Connections	Test Effect
S 1	COM	Digital Contact Output, EN	NO/C]
S 2	TRANS	Digital Contact Output, EN	NO/C	
S 3	COM	Digital Contact Output, DEN	NO/C	
S 4	TRANS	Digital Contact Output, DEN	NO/C	
S 5	COM	Digital Contact Output, EN	NC/C	
S 6	TRANS	Digital Contact Output, EN	NC/C	
S 7	COM	Digital Contact Output, DEN	NO/C	
S 8	TRANS	Digital Contact Output, DEN	NO/C	
S 9	COM	Digital Contact Output, EN	NO/NC	
S10	COM	Digital Contact Output, DEN	NO/NC	
S11	TRANS	Digital Contact Output, EN	NO/NC	
S12	TRANS	Digital Contact Output, DEN	NO/NC	
S13	COM	Partial Trip Output, EN	H/N	
S14	TRANS	Partial Trip Output, EN	H/N	
S15	COM	Partial Trip Output, DEN	H/N	
S16	TRANS	Partial Trip Output, DEN	H/N	
S17	COM	Current Loop Output, 10-50 mA	+/-	
S18	TRANS	Current Loop Output, 10-50 mA	+/-	
S19	COM	Current Loop Output, 10-50 mA	+/-	
S20	TRANS	Current Loop Output, 10-50 mA	+/-	
S21	COM	Wide Range RTD Input	V+, V-, I+, I-	
S22	TRANS	Wide Range RTD Input	V+, V-	
S23	TRANS	Wide Range RTD Input	I+, I-	
S24	TRANS	Wide Range RTD Input	V+, I-	
S25	TRANS	Wide Range RTD Input	V+, I+	
S26	TRANS	Wide Range RTD Input	V-, I-	
S27	TRANS	Wide Range RTD Input	V-, I+	
S28	COM	Wide Range RTD Input	V+, V-, I+, I-	
S29	TRANS	Wide Range RTD Input	V+, V-	
S30	TRANS	Wide Range RTD Input	I+, I-	
S31	COM	Narrow Range RTD Input	V+, V-, I+, I-	
S32	TRANS	Narrow Range RTD Input	V+, V-	
S33	TRANS	Narrow Range RTD Input	I+, I-	
*S34	COM	Narrow Range RTD Input	V+, V-, I+, I-	

d.c

TABLE 8-3 (continued)
SURGE WITHSTAND CAPABILITY (SWC) TESTS

Test No.	Test Mode	Type of I/O Board	Test Connections	Test Effect
*S35	TRANS	Narrow Range RTD Input	V+, V-	b.c
*S36	TRANS	Narrow Range RTD Input	I+, I-	
S37	COM	Narrow Range RTD Input	V+, V-, I+, I-	
S38	TRANS	Narrow Range RTD Input	V+, V-	
S39	TRANS	Narrow Range RTD Input	I+, I-	
*S40	COM	Narrow Range RTD Input	V+, V-, I+, I-	
*S41	TRANS	Narrow Range RTD Input	V+, V-	
*S42	TRANS	Narrow Range RTD Input	I+, I-	
**S43	COM	Narrow Range RTD Input	V+, V-, I+, I-	
S44	COM	WR RTD 0-10V Input	+/-	
S45	TRANS	WR RTD 0-10V Input	+/-	
S46	COM	Current Loop Input, 10-50 mA, act	LS+/LI+	
S47	COM	Current Loop Input, 10-50 mA, act	LS+, LI+, LS, LI-	
S48	TRANS	Current Loop Input, 10-50 mA, act	LS+, LS-	
S49	TRANS	Current Loop Input, 10-50 mA, act	LI+, LI-	
S50	TRANS	Current Loop Input, 10-50 mA, act	LS+, LI+	
S51	COM	Current Loop Input, 10-50 mA, pass	LI+, LI-	
S52	TRANS	Current Loop Input, 10-50 ma, pass	LI+, LI-	
S53	COM	Current Loop Input, 4-20 mA, act	LI+, LI-	
S54	TRANS	Current Loop Input, 4-20 mA, act	LI+, LI-	
S55	COM	AC Input, Cabinet Power	H/N	
S56	TRANS	AC Input, Cabinet Power	H/N	
+S57	TRANS	Digital Contact Output, EN	NC/C	
+S58	TRANS	Digital Contact Output, DEN	NO/C	

- * = Tests performed at 60 HZ repetition rate
- ** = Test performed at 50 HZ repetition rate
- + = Retests required due to modifications made during fault testing

AOS: Analog Output Signal Shifts
TOF: Trip Output Failures

NO = Normally Open
NC = Normally Closed
LS = Loop Supply
LI = Loop Input
EN = Energized
DEN = Deenergized
act = Active
pass = Passive

TABLE B-4a
 RADIO FREQUENCY MODULATION TEST RESULTS
 (ALL RESULTS WITH CABINET DOORS CLOSED)

Test No.	Field Strength	Frequency Band(MHz)	Antenna Type	Polarization	(Cabinet Side) Target	Test Effect
RF 1	3 V/m	20 - 160	BICONICAL	VERT	FRONT	b.c
RF 2	3 V/m	20 - 160	BICONICAL	HORZ	FRONT	
RF 3	3 V/m	160 - 500	LOG PERIODIC	HORZ	FRONT	
RF 4	3 V/m	500 - 1000	LOG PERIODIC	HORZ	FRONT	
RF 5	3 V/m	160 - 500	LOG PERIODIC	VERT	FRONT	
RF 6	3 V/m	500 - 1000	LOG PERIODIC	VERT	FRONT	
RF 7	3 V/m	20 - 160	BICONICAL	HORZ	RIGHT	
RF 8	3 V/m	160 - 500	LOG PERIODIC	VERT	RIGHT	

AOS = Analog Output Signal Shifts
 TOF = Trip Output Failures

TABLE B-4a (Continued)
 RADIO FREQUENCY MODULATION TEST RESULTS
 (ALL RESULTS WITH CABINET DOORS CLOSED)

Test No.	Field Strength	Frequency Band(MHz)	Antenna Type	Polarization	(Cabinet Side) Target	Test Effect
RF 9	3 V/m	500 - 1000	LOG PERIODIC	VERT	RIGHT] d.c
RF 10	3 V/m	20 - 160	BICONICAL	VERT	LEFT	
RF 11	3 V/m	500 - 1000	LOG PERIODIC	HORZ	LEFT	
RF 12	3 V/m	160 - 500	LOG PERIODIC	HORZ	LEFT	
RF 13	3 V/m	500 - 1000	LOG PERIODIC	HORZ	REAR	
RF 14	3 V/m	160 - 500	LOG PERIODIC	VERT	REAR	
RF 15	3 V/m	500 - 1000	LOG PERIODIC	VERT	REAR	
RF 16	3 V/m	160 - 500	LOG PERIODIC	HORZ	REAR	
RF 17	3 V/m	20 - 160	BICONICAL	VERT	REAR	
RF 18	3 V/m	20 - 160	BICONICAL	HORZ	REAR	
RF 19	10 V/m	20 - 160	BICONICAL	HORZ	FRONT	
RF 20	10 V/m	500 - 1000	LOG PERIODIC	HORZ	FRONT	
RF 21	10 V/m	160 - 500	LOG PERIODIC	HORZ	FRONT	

8-25

TABLE B-4a (Continued)
 RADIO FREQUENCY MODULATION TEST RESULTS
 (ALL RESULTS WITH CABINET DOORS CLOSED)

Test No.	Field Strength	Frequency Band(MHz)	Antenna Type	Polarization	(Cabinet Side) Target	Test Effect
RF 22	10 V/m	500 - 1000	LOG PERIODIC	VERT	FRONT]
RF 23	10 V/m	160 - 500	LOG PERIODIC	VERT	FRONT	
RF 24	10 V/m	20 - 160	BICONICAL	VERT	FRONT	
RF 25	10 V/m	20 - 160	BICONICAL	HORZ	RIGHT	
RF 26	10 V/m	160 - 500	LOG PERIODIC	VERT	RIGHT	

d.c

8-26

TABLE 8-4a (Continued)
 RADIO FREQUENCY MODULATION TEST RESULTS
 (ALL RESULTS WITH CABINET DOORS CLOSED)

Test No.	Field Strength	Frequency Band(MHZ)	Antenna Type	Polarization	(Cabinet Side) Target	Test Effect
RF 27	10 V/m	500 - 1000	LOG PERIODIC	VERT	RIGHT]
RF 28	10 V/m	20 - 160	BICONICAL	VERT	LEFT	
RF 29	10 V/m	160 - 500	LOG PERIODIC	HORZ	LEFT	
RF 30	10 V/m	500 - 1000	LOG PERIODIC	HORZ	LEFT	
RF 31	10 V/m	20 - 160	BICONICAL	HORZ	REAR	
RF 32	10 V/m	20 - 160	BICONICAL	VERT	REAR	

b,c

8-27

TABLE B-4a (Continued)
 RADIO FREQUENCY MODULATION TEST RESULTS
 (ALL RESULTS WITH CABINET DOORS CLOSED)

Test No.	Field Strength	Frequency Band(MHZ)	Antenna Type	Polarization	(Cabinet Side) Target	Test Effect
RF 33	10 V/m	500 - 1000	LOG PERIODIC	HORZ	REAR	b.c
RF 34	10 V/m	500 - 1000	LOG PERIODIC	VERT	REAR	
RF 35	10 V/m	160 - 500	LOG PERIODIC	VERT	REAR	
RF 36	10 V/m	160 - 500	LOG PERIODIC	HORZ	REAR	

8-28

TABLE 8-4b
 RADIO FREQUENCY KEYING TEST RESULTS
 (ALL RESULTS WITH CABINET DOORS CLOSED)

Test No.	Field Strength	Frequency Band(MHZ)	Antenna Type	Polarization	(Cabinet Side) Target	Test Effect
RF 37	3 V/m	20 - 160	BICONICAL	HORZ	FRONT	
RF 38	3 V/m	160 - 500	LOG PERIODIC	HORZ	FRONT	
RF 39	10 V/m	160 - 500	LOG PERIODIC	HORZ	FRONT	
RF 40	10 V/m	20 - 160	BICONICAL	HORZ	FRONT	
RF 41	10 V/m	500 - 1000	LOG PERIODIC	HORZ	FRONT	
RF 42	3 V/m	20 - 160	BICONICAL	VERT	FRONT	
RF 43	3 V/m	160 - 500	LOG PERIODIC	VERT	FRONT	
RF 44	10 V/m	160 - 500	LOG PERIODIC	VERT	FRONT	
RF 45	10 V/m	20 - 160	BICONICAL	VERT	FRONT	
RF 46	10 V/m	500 - 1000	LOG PERIODIC	VERT	FRONT	

b.c

AOS = Analog Output Signal Shifts
 TOF = Trip Output Failure

8-29

SECTION 9

CONCLUSION

The Eagle 21™ system performance satisfied the acceptance criteria stated in section 7. The microprocessor subsystem maintained continuous operation while subjected to the abnormal events described in section 5.

Analog output signal noise coupled wire-to-wire or through the analog output channel has no effect on the protective action of the plant protection system since the Eagle 21™ does not use analog output signals for protection signal transmission. Analog output signals are used as interfaces to the plant control and monitoring equipment (e.g., computer, post-accident monitoring system (PAMS)).

9.1 NOISE TESTS

The protective action of the Eagle 21™ system was not affected by noise injected into or adjacent to class non-1E wiring. Analog output signal noise recorded was coupled wire-to-wire or through the analog output channel. Possible analog output noise effects on plant class non-1E systems and PAMS are summarized as follows:

- o The AC noise sources (AC chattering relay, Mil-Spec noise source #1) generated noise spikes on the analog output signal. No change in the nominal DC value of the analog output signal was recorded. These noise spikes will not affect slow responding monitoring equipment.
- o The DC and high voltage transient noise sources produced a shift in the nominal DC value of the analog output signal of 0.5% or less. Since the accuracy requirements of the plant monitoring systems are large compared to the observed effects, these effects are considered minimal.

9.2 FAULT TESTS

The protective action of the Eagle 21™ system was not affected by the injection of credible faults into the designated class non-1E to class 1E isolators. Analog output signal noise recorded was coupled wire to wire and consisted of a noise spike of 0.88% or less upon fault application. No change in the nominal DC value of the analog output signal was recorded. These noise spikes will not affect monitoring equipment.

9.3 SURGE WITHSTAND CAPABILITY (SWC) TESTS

The protective action of the Eagle 21™ system was not affected by the application of the surge withstand test wave to the designated class non-1E to class-1E isolators. In addition, no component damage occurred and no changes in channel calibrations were recorded due to the application of the surge withstand test wave to any cabinet input/output under test.

9.4 RADIO FREQUENCY INTERFERENCE TESTS

The Eagle 21™ system remained operational while exposed to radio frequency interference (RFI) . Analog input/output processing and protective action functions were affected but demonstrated full recovery upon removal of the RFI. To avoid protection system perturbations, Westinghouse recommends that the Eagle 21™ system equipment room(s) be "zoned" to prohibit the use of transceivers in the 20-700 MHz band.

APPENDIX A
PARTIAL TRIP OUTPUT BOARD SURGE WITHSTAND CAPABILITY ANALYSIS

Performed by: R. Nero, Westinghouse

During the fault testing portion of the qualification test for EAGLE-21M, it was necessary to modify the output circuitry of the EPT I/O board. Since the modification did not affect the portion of circuitry that was designed to handle high frequency oscillatory surges, the SWC tests (IEEE-472-1974) were not rerun on the EPT I/O board.

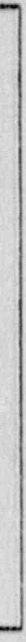
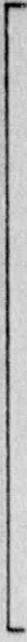
The modification involved suppresser devices on the output. [

]c



c

To substantiate the decision not to rerun the SWC tests (IEEE-472-1974) on the EPT I/O board, analysis was performed with a circuit analysis program []_{b,c}. The analysis confirms that the passive surge network attenuates the surge well below the requirements. The analysis was run worst case for both the common mode and differential mode surge conditions. Worst case for both modes is that no MOVs are installed, all outputs are deenergized, and the outputs are not loaded.



c

c

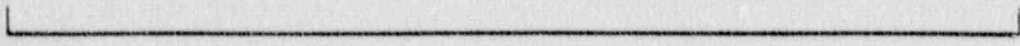
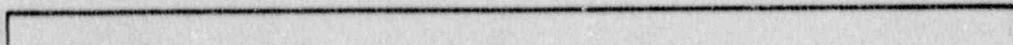


Figure A-1. EPI Common Mode Equivalent Circuit

Figure A-2. EPT Common Mode SMC Test Response



Figure A-3. EPI Differential Mode Equivalent Circuit

Figure A-4. EPT Differential Mode SMC Test Response

A-8

APPENDIX B
EAGLE 21TH SIGNAL CONDITIONING AND MICROPROCESSOR PRINTED CIRCUIT BOARDS

TABLE OF CONTENTS

<u>Section</u>	<u>Title</u>	<u>Page</u>
B.1	Signal Conditioning Boards	B-3
B.1.1	Eagle Analog Input (EAI) Signal Conditioning Board	B-3
B.1.2	Eagle RTD Input (ERI) Signal Conditioning Board	B-6
B.1.3	Eagle Partial Trip (EPT) Signal Conditioning Board	B-9
B.1.4	Eagle Contact Output (ECO) Signal Conditioning Board	B-11
B.1.5	Eagle Analog Output (EAO) Signal Conditioning Board	B-13
B.2	Microprocessor Boards	B-15
B.2.1	Digital Filter Processor (DFP) Board	B-15
B.2.2	Analog-to-Digital Converter (ADC) Board	B-17
B.2.3	Loop Calculation Processor (LCP) Board	B-18
B.2.4	Loop Processor Subsystem Digital Input/Output (LPSDIO) Board	B-19
B.2.5	Digital-to-Analog Converter (DAC) Board	B-21
B.2.6	Loop Processor Subsystem Data Link Handler (DLH) Board	B-22
B.2.7	Tester Subsystem Data Link Handler (DLH) Board	B-23
B.2.8	Test Sequence Processor (TSP) Board	B-25
B.2.9	High Precision Digital-to-Analog Converter (HPDAC) Board	B-26
B.2.10	Tester Subsystem Digital Input/Output (TSDIO) Board	B-28

B.1 Signal Conditioning Boards

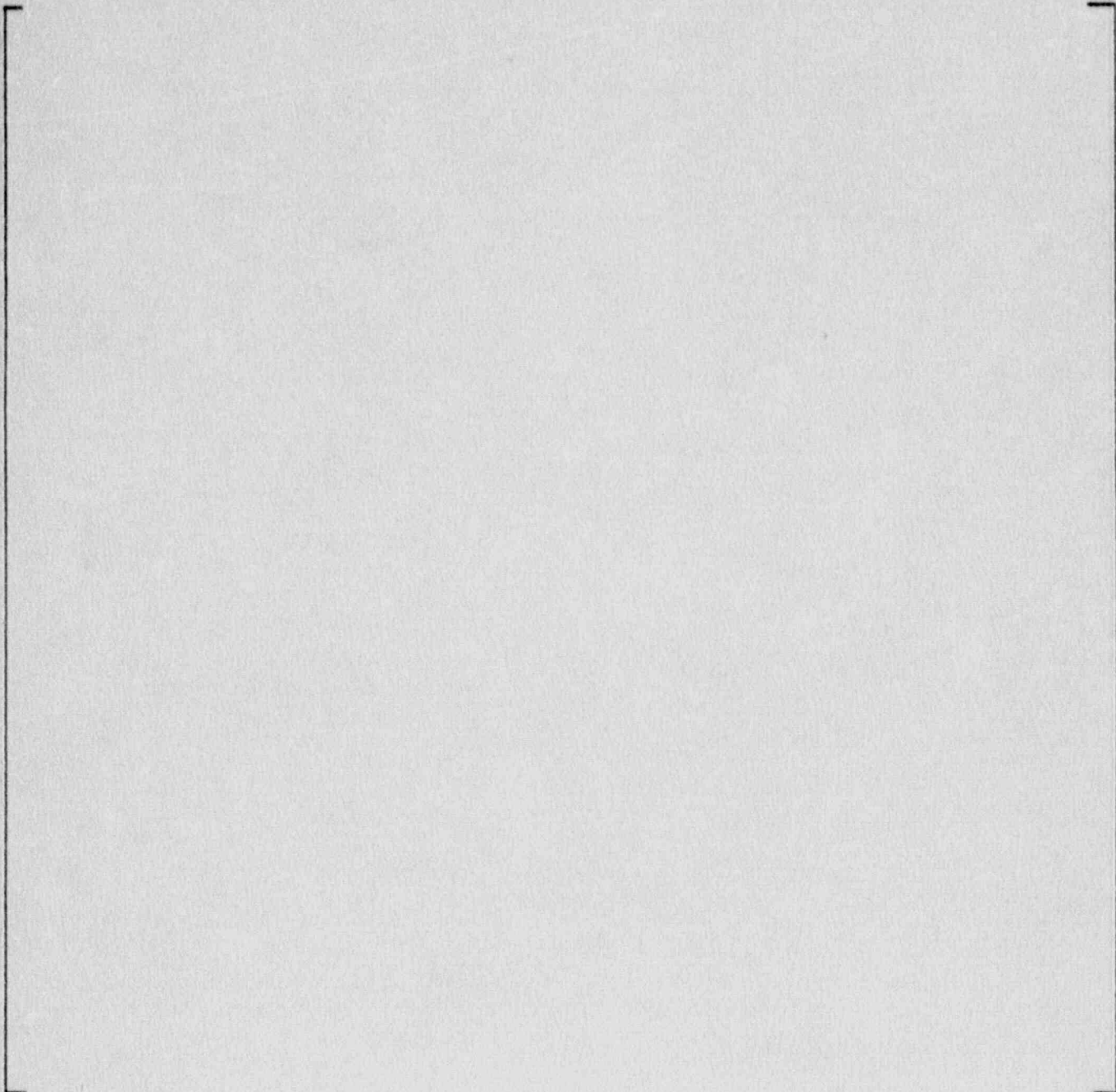
B.1.1 Eagle Analog Input (EAI) Signal Conditioning Board

B.1.1.1 Functional Description

The EAI board is classified as 1E protection-grade equipment, but since it receives inputs from protection-grade transmitters and supplies outputs to the protection-grade loop processor subsystem, it is not a class 1E isolation barrier.

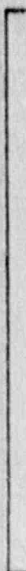
B.1.1.2 Performance Specifications

B.1.1.2.1 Analog Input Characteristics --



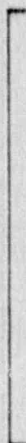
b, c

B.1.1.2.2 Loop Supply Characteristics --



b, c

B.1.1.2.3 Power Supply Requirements --



b, c

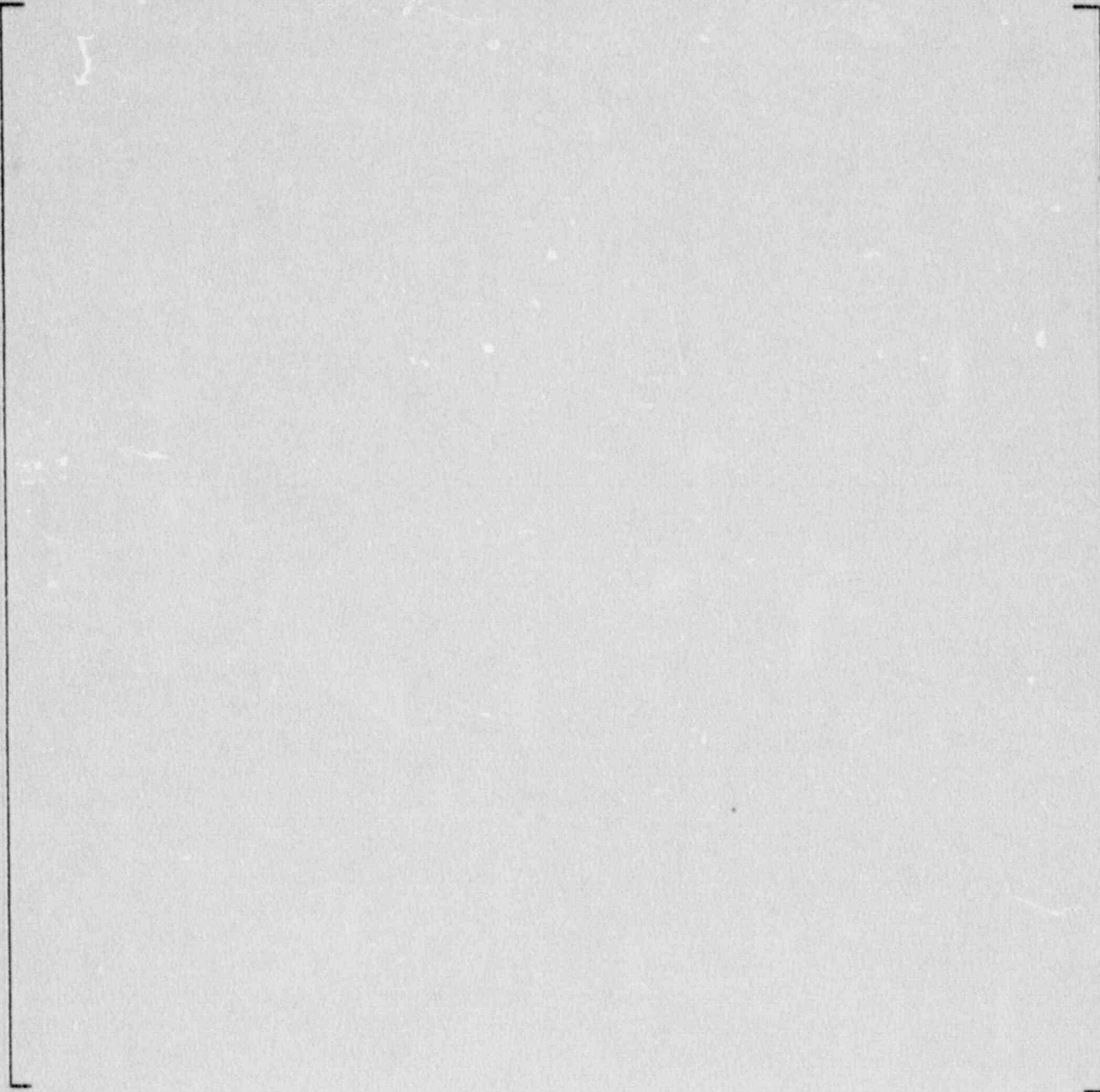
B.1.2 Eagle RTD Input (ERI) Signal Conditioning Board

B.1.2.1 Functional Description

The ERI boards are classified as 1E protection-grade equipment, but since they receive inputs from protection-grade RTDs and supply outputs to the protection-grade loop processor subsystem, they are not class 1E isolation barriers.

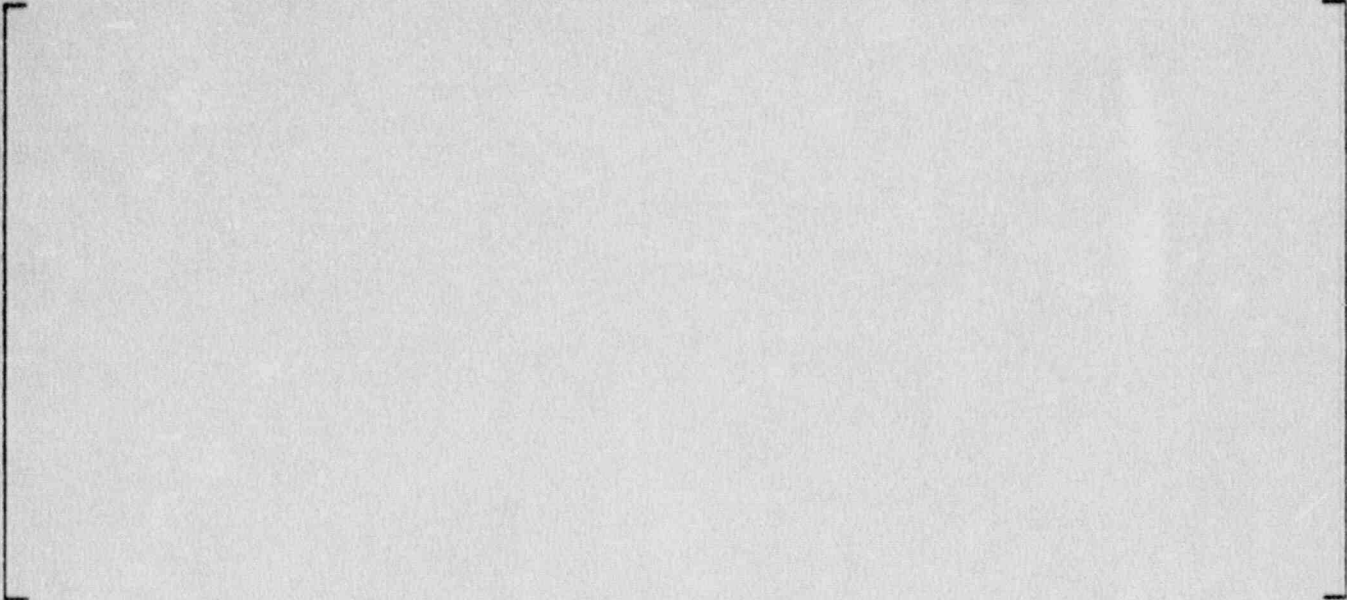
B.1.2.2 Performance Specifications

B.1.2.2.1 Analog Input Characteristics --



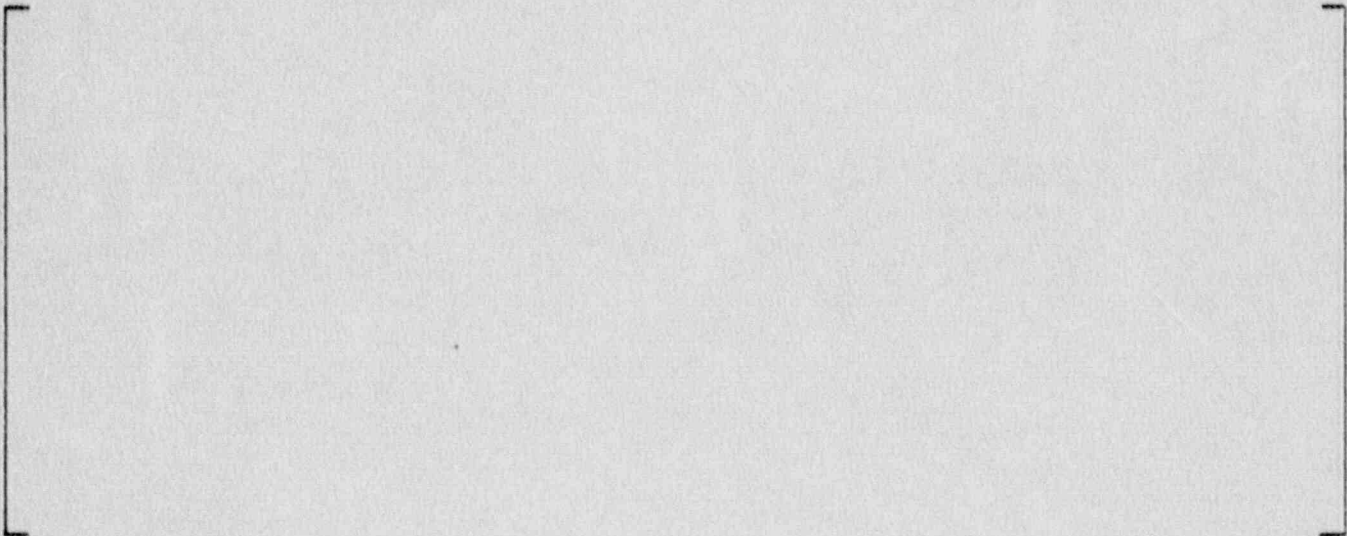
b,c

B.1.2.2.2 RTD Reference Characteristics --



b, c

B.1.2.2.3 Power Supply Requirements --



b, c

B.1.3 Eagle Partial Trip (EPT) Signal Conditioning Board

B.1.3.1 Functional Description

[The four EPT channels are fail-safe in that the failure of the loop processor subsystem causes the channels to trip after a brief time-out period.]_c In most applications, the EPT receives input signals from the class 1E LPS and sends output signals to the class 1E voting logic systems (SSPS or relay logic). In these applications it is not a class 1E isolation barrier. However the EPT has been classified as a class 1E isolation barrier for possible future applications.

B.1.3.2 Performance Specifications

B.1.3.2.1 Digital Output Characteristics --



b, c

B.1.3.2.2 Power Supply Requirements --



b, c

B.1.4 Eagle Contact Output (ECO) Signal Conditioning Board

B.1.4.1 Functional Description

[

]

c

2. Provides class 1E isolation between the protection cabinet and the control systems that receive the contact signals

[

]

c

B.1.4.2 Performance Specifications

B.1.4.2.1 Contact Output Characteristics --



b, c

B.1.4.2.2 Power Supply Requirements --



b, c

B.1.5 Eagle Analog Output (EAO) Signal Conditioning Board

B.1.5.1 Functional Description

[] c

2. Provides class 1E isolation for current loop signals sent to field receivers such as control board indicators and process control loops

[] c

B.1.5.2 Performance Specifications

B.1.5.2.1 Analog Output Characteristics --



b, c

B.1.5.2.2 Power Supply Requirements --

b, c

B.2 Microprocessor Boards

B.2.1 Digital Filter Processor (DFP) Board

B.2.1.1 Functional Description

b, c

]

B.2.1.2 Performance Specifications

B.2.1.2.1 Power Supply Requirements --

]

B.2.2 Analog to Digital Converter (ADC) Board

B.2.2.1 Functional Description

]

[

]

b,c

B.2.2.2 Performance Specifications

B.2.2.2.1 Compatibility --

[

]

b,c

B.2.2.2.2 Power Supply Requirement --

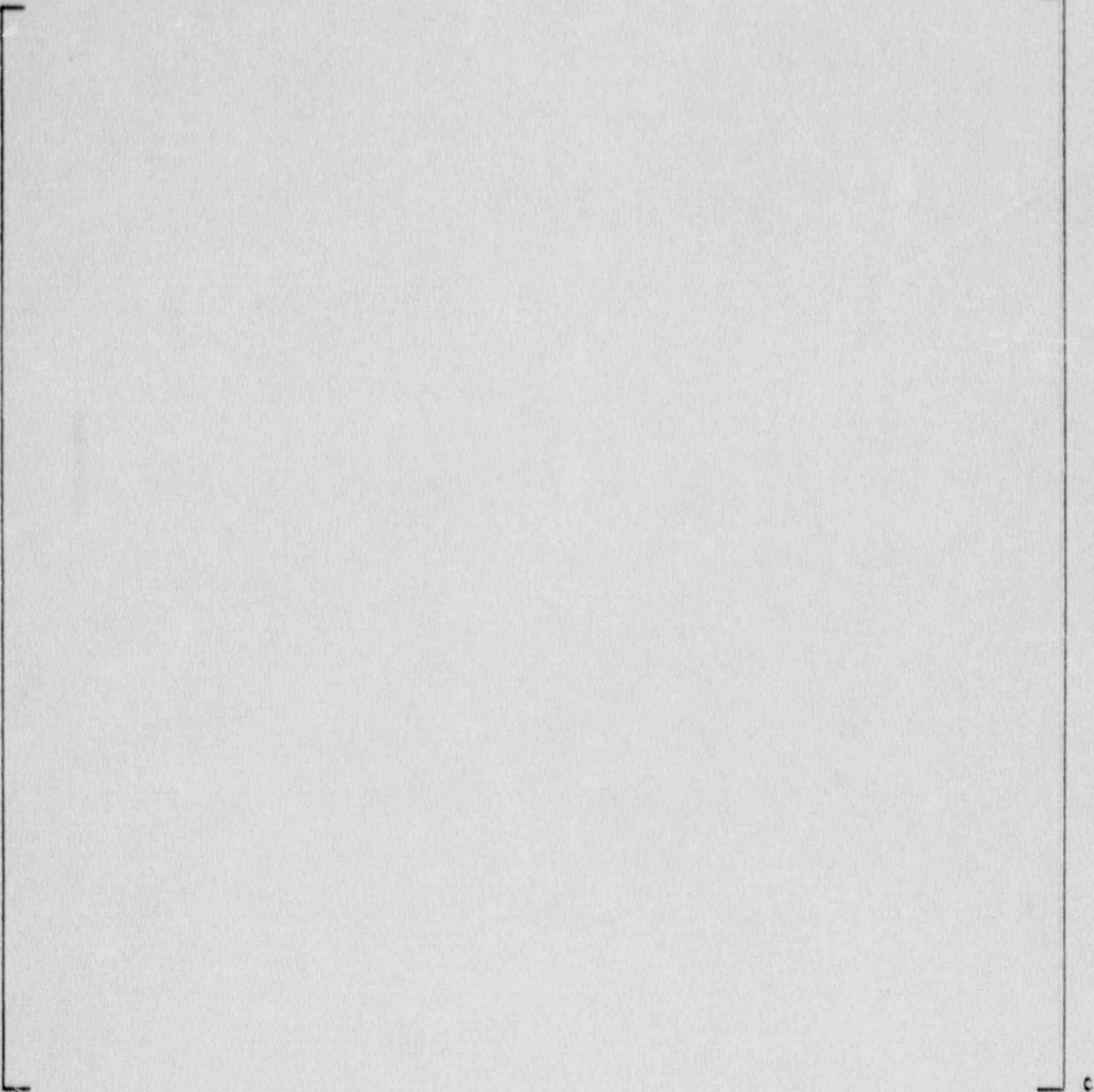
[

]

b,c

B.2.3 Loop Calculation Processor (LCP) Board

B.2.3.1 Functional Description



B.2.3.2 Performance Specifications

B.2.3.2.1 Power Supply Requirements --

[] b,c

B.2.4 Loop Processor Subsystem Digital Input/Output (LPSDIO) Board

B.2.4.1 Functional Description

[] c

[] c

B.2.4.2 Performance Specifications

B.2.4.2.1 Power Supply Requirements --

[] b,c

B.2.5 Digital-to-Analog Converter (DAC) Board

B.2.5.1 Functional Description

[] c



c

B.2.5.2 Performance Specifications

B.2.5.2.1 Electrical Specifications --



b, c

[] b,c

B.2.5.2.2 Power Supply Requirements

[] b,c

B.2.6 Loop Processor Subsystem Data Link Handler (DLH) Board

B.2.6.1 Functional Description

[] c

[] c

B.2.6.2 Performance Specification

B.2.6.2.1 Power Supply Requirement (as shipped) --

[] b,c

B.2.7 Tester Subsystem Data Link Handler (DLH) Board

B.2.7.1 Functional Description

[] c

[

]

c

B.2.7.2 Performance Specification

B.2.7.2.1 Power Supply Requirement (as shipped) --

[

]

b,c

B.2.8 Test Sequence Processor (TSP) Board

B.2.8.1 Functional Description

[

]

c



c

B.2.8.2 Performance Specifications

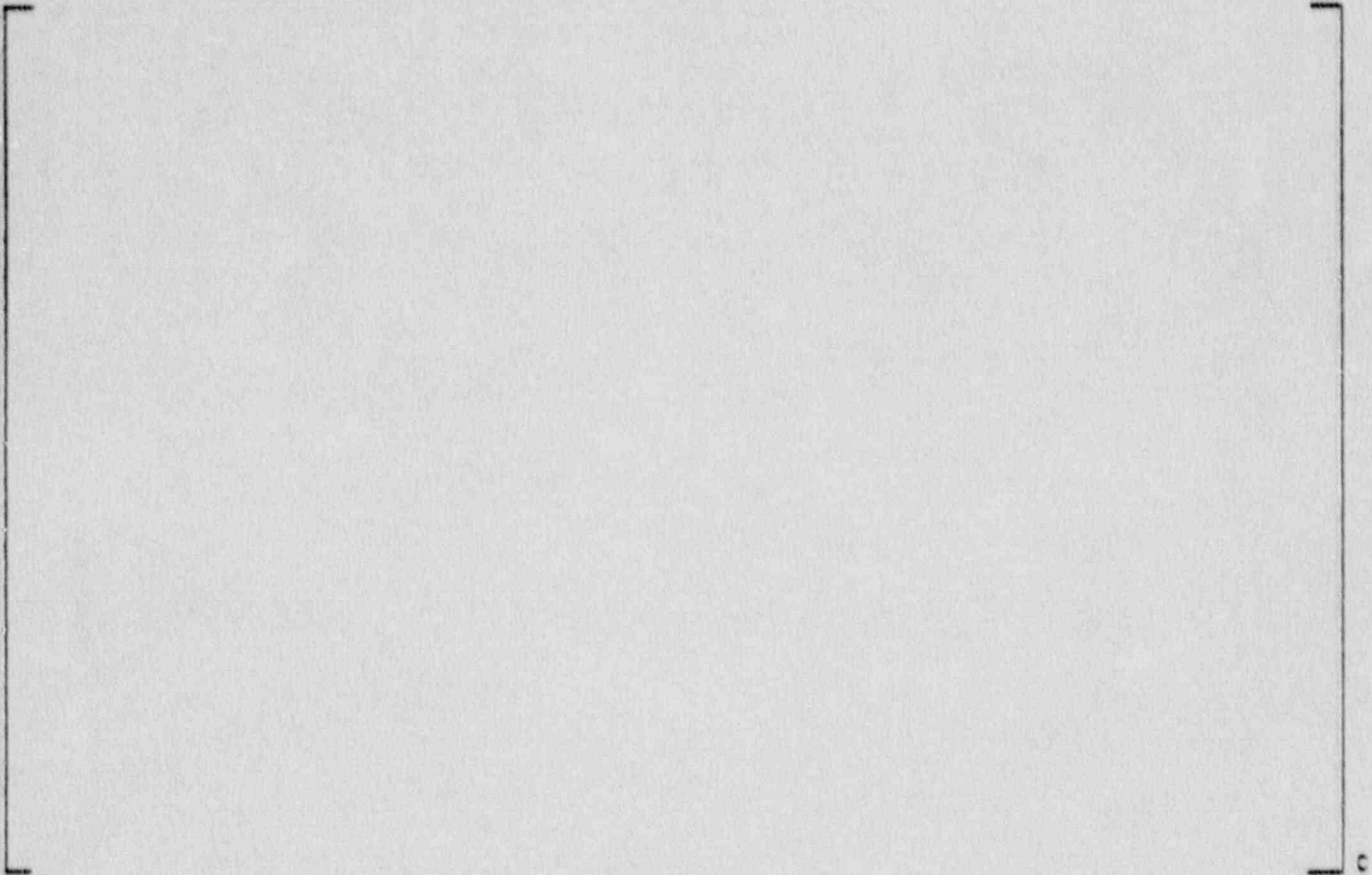
B.2.8.2.1 Power Supply Requirements --



b,c

B.2.9 High Precision Digital-to-Analog Converter (HPDAC) Board

B.2.9.1 Functional Description



B.2.9.2 Performance Specifications

B.2.9.2.1 Electrical Specifications --



[] b,c

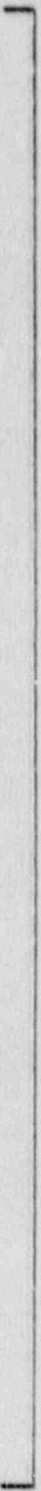
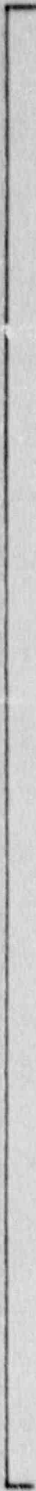
B.2.9.2.2 Power Supply Requirements

[] b,c

B.2.10 Test Subsystem Digital Input/Output (TSDIO) Board

B.2.10.1 Functional Description

[] c



c

B.2.10.2 Performance Specifications

B.2.10.2.1 Power Supply Requirements --

[]
b,c

APPENDIX C
TEST PROCEDURES

JPD 111687-0

DATE
11/16/87

REVISION NO.
0

NOISE TEST PROCEDURE
FOR
EAGLE-21 PROTECTION
SYSTEM

1.0 INTRODUCTION

This procedure details the electrical interference "noise" tests to be applied to the Eagle-21 protection system.

These tests will consist of applying the following noise sources to the antenna/non-class 1E wiring and measuring the effects on system input/output processing.

- o Random Noise
- o Crosstalk Noise
- o Mil N19900 Noise
- o High Voltage Transient Noise
- o Static Noise

The test configuration is documented in Attachment B.

2.0 PREPARATION FOR TEST

2.1 Connect the field cabling to sensor simulation, load simulation, and contact output loads per Attachments B, C and table 1-1.

2.2 Obtain system baseline data:

2.2.1 System baseline data will be taken to verify system operation. Input voltage and current and resistance values corresponding to 0 - 100% of scale in 25% increments and record. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.

2.2.2 Set signal inputs per table 1-1. Adjust analog input signals, using the MMI to obtain the expected engineering unit values specified in table 1-1. Using figure B-6 as a reference, adjust the variable RTD channel per the following procedure:

- o Open the manual switch input to the variable RTD board.

- o Adjust the high adjust potentiometer so that channel TE-441A3 reads $618.261 \pm .375$ Deg f on the MMI.
- o Verify that the TAVG MMI reading equals $589.740 + .2$ Deg f. Verify the following actual bistable output status:

TS/441C = Not Tripped
TS/441G = Not Tripped
TS/441D = Not Tripped
TS/441H = Not Tripped
TS/442D = Tripped
TS/442G = Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Close the manual switch input to the variable RTD board.
- o Adjust the low adjust potentiometer so that channel TE-441A3 reads $615.501 \pm .375$ Deg f on the MMI.
- o Verify that the Delta T MMI reading equals $104.237 - .3$ PU. Verify the following actual bistable output status:

TS/1441C = Tripped
TS/1441G = Tripped
TS/1441D = Tripped
TS/1441H = Tripped
TS/1442D = Not Tripped
TS/1442G = Not Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Open the manual switch input to the variable RTD board and record the results. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.
- 2.2.3 Set the function generator output to the variable RTD board (see figure B-3) in the positive square wave pulse mode with a 0-5 volt amplitude at .05HZ and a duty cycle of approximately 10%.
- 2.2.4 Close the recorder start switch and verify that the trip output signals switch upon receipt of the function generator switch signal (positive square wave pulse).

3.0 NOISE TEST PROCEDURE SEQUENCE

The noise test sequence described below will be followed for each noise test type specified in Sections 4.0 through 8.0.

3.1 Pretest

Obtain a data logger printout of "normal" analog input/output and digital output values.

3.2 Disconnect data logger and verify "antenna" connections and configuration for each injection point per Attachment A.

3.3 Connect the noise source and verify the readiness of the data acquisition system. Enter identifying records in tape recorder log and noise test data sheet (figure 1-6). Follow the test specific instructions given in Sections 4 through 8.

3.4 Disconnect the data logger, close the recorder start switch, start the tape recorder and record 2 minutes of pretest data. Simultaneously energize the noise sources and close the event marker switch. Record 2 minutes of data with the noise source applied. Observe the strip chart recorder and record and analog output signal deviations

and/or trip output status failures. A trip output status failure is defined as a failure of a trip output signal to switch upon receipt of the switch signal from the test station. Remove the noise source and open the event marker switch. Record 2 minutes of post test data and open the recorder start switch and stop the tape recorder.

- 3.5 Obtain a data logger printout and confirm system recovery by comparing to pretest data. Record any discrepancies.
- 3.6 With the system confirmed to be in the pretest condition, proceed to the next test.

4.0 RANDOM NOISE TEST

- 4.1 Connect the []_{b,c} random noise generator to the ENI 240L power amplifier as shown in figure 1-1. Connect the center conductor of the power amplifier to one conductor of the antenna. Terminate the cabinet end of the antenna to an unused internal block connection.
- 4.2 Follow the instructions given for antenna coupled tests given in Table A-2a. Follow the test sequence described in Section 3 for each channel designated in Table A-2a.

5.0 CROSSTALK NOISE TEST

- 5.1 Connect the 125 volt DC chattering relay to the antenna assembly as shown in figure A-2a. Short the cabinet end of the antenna across an unused terminal block connection. Terminate and load the non-1E test cable as specified in Table A-2a.
- 5.2 Follow the test sequence described in Section 3 for each channel designated in Table A-2a.
- 5.3 Repeat 5.1 and 5.2 above using a 118V AC chattering relay. (figure 1-2b)

- 5.4 Disconnect the cabinet end of the antenna and terminate across the first set of terminals shown in Table A-2b. Disconnect the isolator wiring and short the wires specified in Table A-2b.
- 5.5 Follow the test sequence described in Section 3 for each channel designated in table A-2b.
- 5.6 Repeat 5.4 and 5.5 above using a 125 volt DC chattering relay. (figure 1-2b)

6.0 MIL N19900 NOISE TEST

- 6.1 Connect "noise source 1" to the antenna assembly as shown in figure 1-3. Short the cabinet end of the antenna across an unused terminal block connection. Terminate and load the non-1E test cable as specified in Table A-2a.
- 6.2 Follow the test sequence described in Section 3 for each channel designated in Table A-2a.
- 6.3 Repeat 6.1 and 6.2 above using "noise source 2." (see figure 1-3)

7.0 SURGE TRANSIENT GENERATOR

- 7.1 Connect the []_{b,c} surge generator and []_{b,c} isolation network as shown in figure 1-4. Terminate the cabinet end of the antenna across 150 ohms. Terminate and load the non-1E test cable as specified in Table A-2a.
- 7.2 Follow the test sequence described in Section 3 for each channel designated in Table A-2a.

8.0 STATIC NOISE TEST

- 8.1 Connect the 580 VAC static noise source to the antenna assembly as shown in figure 1-5. Terminate the cabinet end of the antenna across two separate (open circuit) unused terminal block connections. Terminate and load the non-1E test cable as specified in Table A-2a.
- 8.2 Follow the test sequence described in Section 3 for each channel designated in Table A-2a.
- 8.3 Disconnect the cabinet end of the antenna and terminate across the first set of terminals shown in table A-2b. Disconnect the isolator wiring at the termination frame and open circuit the wires as specified in table A-2b.
- 8.4 Follow the test sequence described in Section 3 for each channel designated in table A-2b.

(See figure 5-3 of WCAP test report)

Figure 1-1 Random Noise Test Connections

(See figure 5-4a of WCAP test report)

Figure 1-2a Crosstalk Noise - Chattering dc Relay Test Connections

(See figure 5-4b of WCAP test report)

Figure 1-2b Crosstalk Noise - Chattering ac Relay Test Connections

(See figure 5-5 of WCAP test report)

Figure 1-3 Military Specification Noise Sources

(See figure 5-6 of WCAP test report)

Figure 1-4 High Voltage Transient Noise Test Connections

C-13

3137N:4

(See figure 5-7 of WCAP test report)

Figure 1-5 Transformer Connection for the 580 Vac Static Noise Source

9.0 ACCEPTANCE CRITERIA

9.1 Description

The acceptance criteria for the Eagle 21 (1E Safety Related System) is that the system shall maintain protective actions before, during and after the injection of credible noise into or adjacent to the class non-1E wiring.

TABLE 1-1
SIMULATED INPUT SIGNAL

Channel Name	Channel Tag #	Terminal Block	Terminal Connection			I/O Board Location	I/O Board Connection			Simulator Signal	Expected Signal in E.U.
			H1	Lo	Hh		H1	Lo	Hh		
1. Neutron Flux Lower Ion	NY-441A	13-C	4	5	8	13T-4	0	13	9.00	10.00 ± .005	
2. Neutron Flux Upper Ion	NY-441B	13-C	1	2	3	13T-4	2	8	4.04 volt	20.00 ± .005	
3. Pressurizer Pressure	PY/450Q	13-H	-	-	-	13T-8	11	12	14	30.75 mA	2235 ± 1.00
4. Cold Leg Temperature	TE-441B	13-B	1,2	4,3	5	13T-8	6,3	7,4	1	425.000 ohms	302.70 ± .375
5. Cold Leg Temperature	TE-440B	13-B	7,8	10,9	11	13T-8	8,11	9,12	14	425.000 ohms	302.70 ± .375
6. Hot Leg Temperature	TE-441A1	13-A	1,2	4,3	5	13T-5	6,3	7,4	1	447.302 ohms	616.041 ± .375
7. Hot Leg Temperature	TE-441A2	13-A	7,8	10,9	11	13T-5	8,11	9,12	14	447.302 ohms	616.041 ± .375
8. Hot Leg Temperature	TE-441A3	13-C	8,9	11,10	12	13T-5	20,17	21,18	15	xx ohms	± XX
9. Steam Generator Level Loop 2	LY-302'	13-E	1	2	3	13T-2	8	11	14	30 mA	25 ± .120%
10. Steam Generator Level Loop 3	LY-303	13-E	4	5	8	13T-2	20	17	15	40 mA	75 ± .120%
11. RCS Wide Range Pressure	PT-408	13-H	1	2	3	13T-8	20	18	15	12 mA	1500 ± 3.70
12. Pressurizer Vapor Temp	TE-454	13-D	1,2	4,3	5	13T-4	20,17	21,18	15	400 OHMS	400.200 ± 1.05
13. Residual Heat Removal Pump Discharge Temp	TE-812	13-D	8,9	11,10	12	13T-4	22,25	23,20	20	300 OHMS	200.400 ± 1.05

NOTE: - YX - Variable RTD input, set nominally at 447.175 ohms (615.502 Deg F) for the low resistance reading and 448.204 ohms (616.281 Deg F) for the high resistance reading. See step 2.3.2 for details.

EAGLE-21 NOISE TEST REPORT

TEST TYPE/PROCEDURE NUMBER(REV) _____

DATE _____

NOISE INJECTION CHANNEL NUMBER/TAG NO. _____

DATA LOGGER PRINTOUT: _____
(PRETEST/POST-TEST)

BISTABLE PERFORMANCE (PASS/FAIL): _____

REMARKS/OBSERVATIONS:

ANALOG OUTPUT NAME/TAG NO.	PRETEST		NOISE APPLIED		
	DC VALUE	P-P NOISE	DC VALUE	P-P NOISE	%DEV

PZR VAP/T454A

NR TEMP/T441L

NR TEMP/T441K

WR PRE/P408B

TAPE SET:

TAPE FOOTAGE:
(PRETEST/TEST/POST-TEST)

REMARKS/OBSERVATIONS:

PERFORMED BY/DATE:

Figure 1-6. Noise Test Data Sheet

ATTACHMENT A
NOISE INJECTION "ANTENNA" CONNECTIONS

NOTE: The antenna for noise injection is to be a 40 foot length of unshielded, non-twisted two conductor cable bundled to the non-class 1E test cable. The class non-1E test cable shall consist of a non-shielded twisted pair cable. The antenna and class non-1E cabling is separated from the class-1E cabling outside the protection cabinet. The antenna, class-1E and class non-1E cabling are all bundled together inside the protection cabinet. See figures B-1 and B-2 for antenna placement.

This attachment contains the following tables:

- o Table A-1a - Noise Injection Field Connections
(Antenna Coupled)

- o Table A-1b - Noise Injection Field Connections
(Direct Coupled)

TABLE A-1a

NOISE INJECTION FIELD CONNECTION (Antenna Coupled)

Channel #	I/O Description	Channel Tag #	Terminal Block	CONNECT NON-1E TEST CABLE TO			Isolator Type	I/O Board Location/ Channel #	CONNECT LOAD TO NON-1E TEST CABLE
				Hi	Lo	Sh			
1.	Bistable Partial Trip	ITS/442G	13-M	1	2		Class non 1E/1E Isolation Barrier	13T-10/1	40 Watt Light Bulb
2.	Analog Output	IPY/408A	13-N	4	5	6	Class non 1E/1E Isolation Barrier	13T-16/2	600 OHMS
3.	Contact Output (No)	ITY/441A	13-M	7	8		Class non 1E/1E Isolation Barrier	13T-12/2	Open Circuit
4.	Contact Output (NC)	ITY/441A	13-M*	7	8		Class non 1E/1E Isolation Barrier	13T-12/2	Open Circuit
5.	Contact Output (No)	TY/441A	13-M	7	8		Class non 1E/1E Isolation Barrier	13T-12/2	Short Circuit
6.	Contact Output (Nc)	TY/441A	13-M*	7	8		Class non 1E/1E Isolation Barrier	13T-12/2	Short Circuit

*Move wire terminated on 13T-12-6 to 13T-12-7 to test NC configuration.

C-20

TABLE A-1b

NGISE INJECTION FIELD CONNECTION (Direct Coupled)

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect Antenna to Hi Lo	Isolator Type	I/O Board Location/ Channel #	DISCONNECT WIRES AT TERMINATION FRAME
1.	Bistable Partial Trip	ITS/442G	13-M	1 2	Class non Isolation Barrier 1E/1E	13T-10/1	2, 3
2.	Analog Output	IPY/408A	13-N	4 5	Class non Isolation Barrier 1E/1E	13T-16/2	5, 7
3.	Contact Output	ITY/441A	13-M	7 8	Class non Isolation Barrier 1E/1E	13T-12/2	5, 6

C-21

ATTACHMENT B
FIELD CONNECTIONS AND SIMULATION

This attachment contains the following figures:

- o Figure B-1 Noise Test Setup (Antenna Coupled)
- o Figure B-2 Noise Test Setup (Direct Coupled)
- o Figure B-3 Strip Chart Recorder/Function Generator Connections
- o Figure B-4 4-50 mA Transmitter
- o Figure B-5 Wide Range Resistance Temperature Detector
- o Figure B-6 Narrow Range Resistance Temperature Detector
- o Figure B-7 10-50 mA Current Loop Output Monitoring
- o Figure B-8 Contact Output Monitoring Connection
- o Figure B-9 Partial Trip Output Monitoring

Cabinet Configuration Information:

The cabinet under test, Qualification Unit 2, is an exact replica of Watts Bar Nuclear Power Station Protection Rack 13. The following drawings document the cabinet configuration. Copies of these drawings will be included as part of the final test report.

<u>Drawing Description</u>	<u>Drawing Number/Rev.</u>
Terminal Block Wiring Diagram, Protection Set 4	1-47043 PW-13, rev. 3E
Process Control Block Diagram, Delta T/T _{AVG} System	108D408 sh. 10, rev. 11
Process Control Block Diagram, W.R. S.G. Level	108D408 sh. 34, rev. 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temp.	108D408 sh. 38, rev. 4

Process Control Block Diagram,
RHR Pump Discharge Temp

108D408 sh. 39, rev. 5

Process Control Block Diagram,
RCS Wide Range Pressure

108D408 sh. 43, rev. 1

Eagle-21 Schematic Diagrams,
Rack 13 Protection Set 4

1856E69 sh. 2, rev. 2

(See figure 5-1 of WCAP test report)

Figure B-1 Noise Test Setup (Antenna Coupled)

(See figure 5-2 of WCAP test report)

Figure B-2 Noise Test Setup (Direct Coupled)

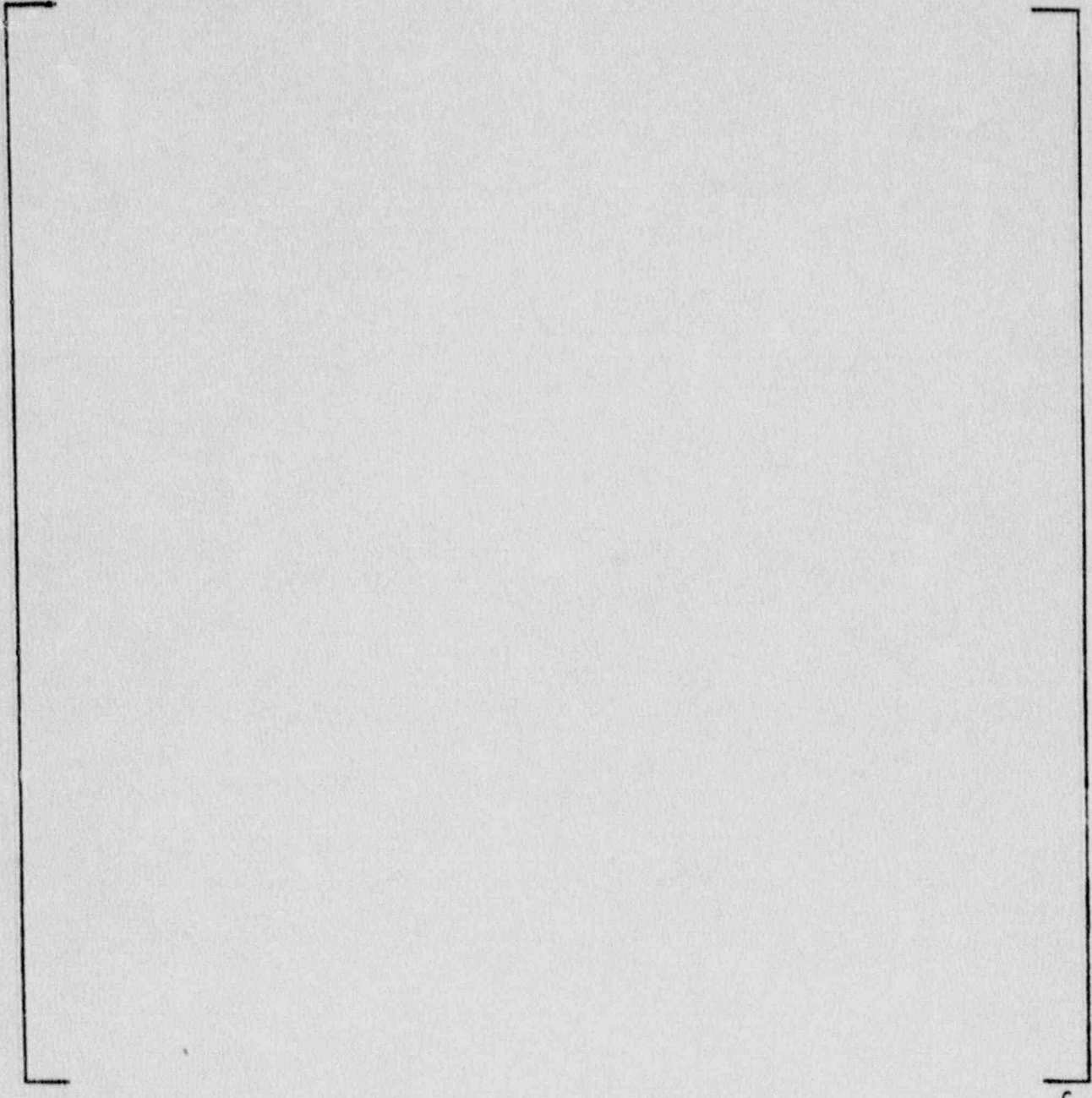


Figure B-3 Strip Chart Recorder/Function Generator Connections

(See figure 6-4 of WCAP test report)

Figure B-4 4-50 mA Transmitter

C-28

3137N:4

(See figure 6-5 of WCAP test report)

Figure B-5 Wide Range Resistance Temperature Detector (RTD)

(See figure 6-6 of WCAP test report)

Figure B-6 Narrow Range Resistance Temperature Detector

(See figure 6-7 of WCAP test report)

Figure B-7 10-50 mA Current Loop Output Monitoring

(See figure 6-9 of WCAP test report)

Figure B-8 Contact Output Monitoring

(See figure 6-8 of WCAP test report)

Figure B-9 Partial Trip Output Monitoring

ATTACHMENT C
TRANSIENT DATA RECORDING SYSTEM CONNECTIONS

This attachment contains the following:

- o Table C-1 Tape Recorded Data**
- o Table C-2 Data Logger Recorded Data**
- o Table C-3 Strip Chart Recorded Data**

TABLE C-1
TAPE RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer Amplifier Gain
				Hi	Lo	Sh	
1.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
2.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
3.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
4.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
5.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
6.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
7.	Contact Output	ITY/441	13-M	5	6		.02
8.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
9.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
10.	Analog Input I/E	IPY/458Q	*				10
11.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
12.	Analog Input I/E	IPY/408	*				20
13.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
14.	Function Generator Sig.	N/A	**				.05

*Measure current across 20 ohm transmitter test resistor. See figure B-4.

**Monitor function generator output signal. See figure B-3.

TABLE C-2
DATA LOGGER RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection		
				Hi	Lo	Sh
6.	Analog Input E/E	INY/441B	13-C	1	2	3
7.	Analog Input E/E	INY/441A	13-C	4	5	6
9.	Contact Output	ITY/441	13-M	5	6	
10.	Contact Output	ITY/441A	13-M	7	8	
22.	Analog Output E/I	ITY/441L	13-P	10	11	12
23.	Analog Output E/I	ITY/454A	13-G	4	5	6
24.	Analog Output E/I	ITY/441K	13-P	7	8	9
25.	Analog Output E/I	ILY/502B	13-K	1	4	5
26.	Analog Output E/I	IPY/408B	13-N	7	8	11
27.	Analog Output E/I	ILY/503B	13-K	7	10	11
35	Analog Input I/E	IPY/458Q	*			
36	Analog Input I/E	ILY/502	*			
37	Analog Input I/E	ILY/503	*			
38	Analog Input I/E	IPY/408	*			

*Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE C-3
STRIP CHART RECORDED

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer*** Amplifier Gain
				Hi	Lo	Sh	
1.	Function Generator Sig.	N/A	**				.05
2.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
3.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
4.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
5.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
6.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
7.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
9.	Contact Output	ITY/441	13-M	5	6		.02
10.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
11.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
12.	Analog Input I/E	IPY/458Q	*				10
13.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
14.	Analog Input I/E	IPY/408	*				20
15.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

** Monitor function generator output signal. See figure B-3.

*** Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

JPD 111687-1

DATE
11/16/87

REVISION NO.
0

FAULT TEST PROCEDURE
FOR
EAGLE-21 PROTECTION
SYSTEM

C-39

4301N:4

1.0 INTRODUCTION

This procedure details the electrical fault tests to be applied to the Eagle-21 protection system.

These tests will consist of applying fault voltages to the Eagle-21 system isolation devices. Tests are summarized by isolator board type below:

LINE TO GROUND FAULT TEST PERFORMED

<u>Isolator Board</u>	<u>Faults Applied</u>
Partial Trip Output, Energized	125 Vdc, 125 Vac, 250 Vdc, 580 Vac
Partial Trip Output, Deenergized	250 Vdc, 580 Vac
Digital Contact Output, NO, Energized	250 Vdc, 580 Vac
Digital Contact Output, NC, Energized	250 Vdc, 580 Vac
Current Loop Output	125 Vac, 125 Vdc, 250 Vdc, 580 Vac

LINE TO LINE FAULT TESTS PERFORMED

<u>Isolator Board</u>	<u>Faults Applied</u>
Partial Trip Output, Energized	125 VAC, 125 Vdc, 250 Vdc, 580 Vac
Partial Trip Output, Deenergized	250 Vdc, 580 Vac
Digital Contact Output, NO, Energized	125 Vac, 125 Vdc, 250 Vdc, 580 Vac
Digital Contact Output, NC, Energized	250 Vdc, 580 Vac
Digital Contact Output, NO, Deenergized	250 Vdc, 580 Vac
Digital Contact Output, NC, Deenergized	125 Vac, 125 Vdc, 250 Vdc, 580 Vac
Current Loop Output 10-50 mA	125 VAC, 125 Vdc, 250 Vdc, 580 Vac

The test configuration is documented in Attachment B.

2.0 PREPARATION FOR TEST

2.1 Connect the field cabling to sensor simulation, load simulation, and contact output loads per Attachment B and table 1-1.

2.2 Obtain system baseline data:

2.2.1 System baseline data will be taken to verify system operation. Input voltage and current and resistance values corresponding to 0 - 100% of scale in 25% increments and record. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.

2.2.2 Set signal inputs per table 1-1. Adjust analog input signals, using the MMI to obtain the expected engineering unit values specified in table 1-1. Using figure B-6 as a reference, adjust the variable RTD channel per the following procedure:

- o Open the manual switch input to the variable RTD board.
- o Adjust the high adjust potentiometer so that channel TE-441A3 reads $618.261 \pm .375$ Deg f on the MMI.
- o Verify that the TAVG MMI reading equals $589.740 \pm .2$ Deg f. Verify the following actual bistable output status:

TS/441C = Not Tripped

TS/441G = Not Tripped

TS/441D = Not Tripped

TS/441H = Not Tripped

TS/442D = Tripped

TS/442G = Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Close the manual switch input to the variable RTD board.
- o Adjust the low adjust potentiometer so that channel TE-441A3 reads 615.501+/- .375 Deg f on the MMI.
- o Verify that the Delta T MMI reading equals 104.237-.3PU. Verify the following actual bistable output status:

TS/1441C = Tripped
TS/1441G = Tripped
TS/1441D = Tripped
TS/1441H = Tripped
TS/1442D = Not Tripped
TS/1442G = Not Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Open the manual switch input to the variable RTD board and record the results. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.

2.2.3 Set the function generator output to the variable RTD board (see figure B-3) in the positive square wave pulse mode with a 0-5 volt amplitude at .05HZ and a duty cycle of approximately 10%.

2.2.4 Close the recorder start switch and verify that the trip output signals switch upon receipt of the function generator switch signal (positive square wave pulse).

3.0 FAULT TEST PROCEDURE SEQUENCE

The fault test sequence described below will be followed for each isolator board type specified in Sections 4.0 through 6.0.

3.1 Pretest

Obtain a data logger printout of "normal" analog input/output and digital output values.

- 3.2 Disconnect data logger and verify "antenna" connections and configuration for each injection point per Attachment A.
- 3.3 Connect the fault voltage source and verify the readiness of the data acquisition system. Enter identifying records in tape recorder log and noise test data sheet (figure 1-6). Follow the test specific instructions given in Sections 4 through 6.
- 3.4 Disconnect the data logger, close the recorder start switch, start the tape recorder and record 1 minute of pretest data. Disconnect the test station from the channel under test. Simultaneously energize the fault voltage source and close the event marker switch. Record 1 minute of data with the fault voltage source applied. Observe the strip chart recorder and record any analog output signal deviations and/or trip output status failures. A trip output status failure is defined as a failure of a trip output signal to switch upon receipt of the switch signal from the test station. Remove the fault voltage source and open the event marker switch. Reconnect the test station to the channel under test. Record 1 minute of post test data and open the recorder start switch and stop the tape recorder.
- 3.5 Obtain a data logger printout and confirm system recovery by comparing to pretest data. Record any discrepancies. If channel under test or adjacent channels are inoperable and damaged following fault application, channel(s) must be repaired. Record all

component and/or board (i.e., blown/damaged PC track) repairs required to return channel under test or adjacent channel to operation. If board is damaged see note in Appendix A for guidance.

- 3.6 If the fault voltage source breaker is tripped the fault test is invalid. Increase the fault voltage source breaker current rating and repeat the test.
- 3.7 With the system confirmed to be in the pretest condition, proceed to the next test.

4.0 CURRENT LOOP OUTPUT BOARD TEST

- 4.1 Configure the []_{b,c} transformer as a 125 VAC fault voltage source (figure 1-1). Monitor the channels designated per tables C-1a, C-2a and C-2b.
- 4.2 Connect the transformer secondary hot lead to the terminal connection of the EAO channel under test as specified in table A-1a. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth ground (third prong of the AC power feed).
- 4.3 Follow the test sequence in section 3 for each test specified in table A-1a for the EAO channel under test.
- 4.4 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 4.5 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-1b.
- 4.6 Follow the test sequence in section 3 for each test specified in table A-1b for the EAO channel under test.

- 4.7 Connect the []_{b,c} DC power supply as a 125 VDC fault voltage source (figure 1-2).
- 4.8 Connect the DC power supply positive and negative leads to the terminal connection of the EAO channel under test as specified in table A-2a.
- 4.9 Follow the test sequence described in section 3 for each test specified in table A-2a for the EAO channel under test.
- 4.10 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-2b.
- 4.11 Follow the test sequence in section 3 for each test specified in table A-2b for the EAO channel under test.
- 4.12 Connect the []_{b,c} DC power supply as a 250 VDC fault voltage source (figure 1-2).
- 4.13 Connect the DC power supply positive and negative leads to the terminal connection of the EAO channel under test as specified in table A-3a.
- 4.14 Follow the test sequence described in section 3 for each test specified in table A-3a for the EAO channel under test.
- 4.15 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-3b.
- 4.16 Follow the test sequence in section 3 for each test specified in table A-3b for the EAO channel under test.
- 4.17 Configure the []_{b,c} transformer as a 580 VAC fault voltage source (figure 1-3).

- 4.18 Connect the transformer secondary hot lead to the terminal connection of the EAO channel under test as specified in table A-4a. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth ground (third prong of the AC power feed).
- 4.19 Follow the test sequence described in section 3 for each test specified in table A-4a for the EAO channel under test.
- 4.20 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 4.21 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-4b.
- 4.22 Follow the test sequence in section 3 for each test specified in table A-4b for the EAO channel under test.

5.0 DIGITAL CONTACT OUTPUT BOARD TEST

- 5.1 Configure the []_{b,c} transformer as a 125 VAC fault voltage source (figure 1-1). Monitor the channels designated per table C-1b, C-2b, C-3b.
- 5.2 Connect the transformer secondary hot and neutral leads to the terminal connection of the ECO channel under test as specified in table A-1b.
- 5.3 Follow the test sequence in section 3 for each test specified in table A-1b for the ECO channel under test.
- 5.4 Connect the []_{b,c} DC power supply as a 125 VDC fault voltage source (figure 1-2).

- 5.5 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-2b.
- 5.6 Follow the test sequence in section 3 for each test specified in table A-2b for the ECO channel under test.
- 5.7 Connect the []_{b,c} DC power supply as a 250 VDC fault voltage source (figure 1-2).
- 5.8 Connect the DC power supply positive and negative leads to the terminal connection of the ECO channel under test as specified in table A-3a.
- 5.9 Follow the test sequence described in section 3 for each test specified in table A-3a for the ECO channel under test.
- 5.10 Connect the DC power supply positive and negative terminal leads to the terminal connection of the channel under test as specified in table A-3b.
- 5.11 Follow the test sequence in section 3 for each test specified in table A-3b for the ECO channel under test.
- 5.12 Configure the []_{b,c} transformer as a 580 VAC fault voltage source (figure 1-3).
- 5.13 Connect the transformer secondary hot lead to the terminal connection of the ECO channel under test as specified in table A-4a. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth ground (third prong of the AC power feed).
- 5.14 Follow the test sequence described in section 3 for each test specified in table A-4a for the ECO channel under test.

- 5.15 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 5.16 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-4b.
- 5.17 Follow the test sequence in section 3 for each test specified in table A-4b for the ECO channel under test.

6.0 PARTIAL TRIP OUTPUT BOARD TEST

- 6.1 Configure the []_{b,c} transformer as a 125 VAC fault voltage source (figure 1-1). Monitor the channels designated per tables C-1c, C-2c, C-3c.
- 6.2 Connect the transformer secondary hot lead to the terminal connection of the EPT channel under test as specified in table A-1a. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth ground (third prong of the AC power feed).
- 6.3 Follow the test sequence in section 3 for each test specified in table A-1a for the EPT channel under test.
- 6.4 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 6.5 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-1b.

- 6.6 Follow the test sequence in section 3 for each test specified in table A-1a for the EPT channel under test.
- 6.7 Connect the []_{b,c} DC power supply as a 125 VDC fault voltage source (figure 1-2).
- 6.8 Connect the DC power supply positive and negative leads to the terminal connection of the EPT channel under test as specified in table A-2a.
- 6.9 Follow the test sequence described in section 3 for each test specified in table A-2a for the EPT channel under test.
- 5.10 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-2b.
- 6.11 Follow the test sequence in section 3 for each test specified in table A-2b for the EPT channel under test.
- 6.12 Connect the []_{b,c} DC power supply as a 250 VDC fault voltage source (figure 1-2).
- 6.13 Connect the DC power supply positive and negative lead the terminal connection of the EPT channel under test as specified in table A-3a.
- 6.14 Follow the test sequence described in section 3 for each test specified in table A-3a for the EPT channel under test.
- 6.15 Connect the DC power supply positive and negative leads to the terminal connection of the channel under test as specified in table A-3b.
- 6.16 Follow the test sequence in section 3 for each test specified in Table A-3b for the EPT channel under test.

- 6.17 Configure the []_{b,c} transformer as a 580 VAC fault voltage source (figure 1-3).
- 6.18 Connect the transformer secondary hot lead to the terminal connection of the EPT channel under test as specified in table A-4a. Connect the transformer secondary neutral lead to the primary neutral. Ensure that this connection is earth ground (third prong of the AC power feed).
- 6.19 Follow the test sequence described in section 3 for each test specified in table A-4a for the EPT channel under test.
- 6.20 Disconnect the transformer secondary neutral/primary neutral connection. Verify that the secondary neutral is not connected to earth ground (third prong of AC power feed).
- 6.21 Connect the transformer secondary hot and neutral leads to the terminal connection of the channel under test as specified in table A-4b.
- 6.22 Follow the test sequence in section 3 for each test specified in table A-4b for the EPT channel under test.

(See figure 5-9 of WCAP test report)

Figure 1-1 Transformer Connection for the 125 VAC Fault Source

(See figure 5-11 of WCAP test report)

Figure 1-2 DC Power Supply Connections

(See figure 5-10 of WCAP test report)

Figure 1-3 Transformer Connection for the 580 VAC Fault Source

7.0 ACCEPTANCE CRITERIA

7.1 Description

The acceptance criteria for the Eagle 21 (1E Safety Related System) is that the system shall remain operational and maintain protective actions before, during and after the application of credible fault voltages. Faults shall not propagate across the Class non-1E to Class 1E isolation barrier or from channel to channel.

TABLE 1-1
SIMULATED INPUT SIGNAL

Channel Name	Channel Tag #	Terminal Block	BI	Terminal Connection	I/O Board Location	BI	Lo	Hi	I/O Board Connection	BI	Lo	Hi	Stimulator Signal	Expected Signal in G.U.
1. Bottom Flux Lower Lim	BT-441A	13-C	4	5	6	137-4			13	0			9.00	10.00 ± .005
2. Bottom Flux Upper Lim	BT-441B	13-C	1	2	3	137-4			8	2			4.04 volt	20.00 ± .005
3. Pressurizer Pressure	PT-456Q	13-B	-	-	-	137-6			12	11			30.75 PSI	2295 ± 1.00
4. Cold Leg Temperature	TE-441B	13-B	1,2	4,3	5	137-6			7,4	0,3			425.000 ohms	502.70 ± .075
5. Cold Leg Temperature	TE-440Q	13-B	7,8	10,9	11	137-6			10	9,11			0.25.000 ohms	502.70 ± .075
6. Hot Leg Temperature	TE-441B1	13-A	1,2	4,3	5	137-5			7,4	0,3			407.902 ohms	010.001 ± .075
7. Hot Leg Temperature	TE-441B2	13-A	7,8	10,9	11	137-5			10	0,11			447.502 ohms	010.001 ± .075
8. Hot Leg Temperature	TE-441B3	13-C	8,9	11,10	12	137-5			13	20,17			no ohms	± 50
9. Steam Generator Level Loop 2	LT-302	13-E	1	2	3	137-2			14	0			20 PSI	25 ± .1000
10. Steam Generator Level Loop 3	LT-303	13-E	4	5	6	137-2			15	20			40 PSI	75 ± .1000
11. RCS Wide Range Pressure	PT-408	13-B	1	2	3	137-0			15	20			18 PSI	1500 ± 0.70
12. Pressurizer Vapor Temp	TE-456	13-D	1,2	4,3	5	137-4			15	20,17			400 OHMS	400.000 ± 1.05
13. Recirculation Heat Exchanger Pump Discharge Temp	TE-012	13-D	9,8	11,10	12	137-4			20	22,25			300 OHMS	200.000 ± 1.05

NOTE: - EX - Variable STD input, set normally at 447.175 ohms (015.502 Ohm f) for the low resistance reading and 448.294 ohms (016.261 Ohm f) for the high resistance reading. See step 2.3.2 for details.

I/O Module _____

Procedure Rev. _____

Date _____

Test # _____

TYPE

SHORT CIRCUIT _____, AC _____, DC _____

COMMON MODE _____ GROUND CONNECTED TO VOLTS PLUS _____ MINUS _____ GROUND

LINE TO LINE _____ VOLTS (+) TO (+) _____ (+) TO (-) _____
VOLTS (-) TO (+) _____ (-) TO (-) _____

TEST INJECTION POINT _____ TEST CONDITION _____

I/O CARD TYPE _____ POINT # _____

PRE-TEST

DATA LOGGER VERIFICATION* _____ PRINT OUTPUT # _____

SYSTEM STATUS _____

REMARKS AND TEST OBSERVATION _____

DISCONNECT DATA LOGGER _____

TEST

TAPE RECORDER FOOTAGE BEGIN _____ END _____ SET # _____
SPEED _____ TIME: (START): _____ (STOP): _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATION _____

POST-TEST

DATA LOGGER DATA VERIFICATION* PRINT OUTPUT # _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATION _____

PERFORMED _____ REVIEWED _____

Figure 1-4. Fault Test Data Sheet

ATTACHMENT A
FAULT VOLTAGE SOURCE CONNECTIONS

NOTE: If the isolator board is damaged (i.e., blown/damaged PC track) during fault testing an alternate channel must be chosen for testing. The Data Recording System Connections, Appendix C must be modified to ensure that Channels adjacent (left, right, top, bottom) to the channel under test are monitored. Record in a permanent record book any changes made to the test connections specified in this Appendix and the recording connections specified in Appendix C.

This attachment contains the following tables:

- o Table A-1a - 125 VAC Line-to-Ground Fault Connections
- o Table A-1b - 125 VAC Line-to-Line Fault Connections
- o Table A-2a - 125 VDC Line-to-Ground Fault Connections
- o Table A-2b - 125 VDC Line-to-Line Fault Connections
- o Table A-3a - 250 VDC Line-to-Ground Fault Connections
- o Table A-3b - 250 VDC Line-to-Line Fault Connections
- o Table A-4a - 580 VAC Line-to-Ground Fault Connections
- o Table A-4b - 580 VAC Line-to-Line Fault Connections

TABLE A-1a
125 VAC LINE-TO-GROUND FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Connect Transformer Secondary Hot Lead To		Isolator Type	I/O Board Location/ Channel #
			Terminal Block	Connection		
* 1.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	1	Class non IE/IE Isolation Barrier	13T-9/1
* 2.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	2	Class non IE/IE Isolation Barrier	13T-9/1
3.	Current Loop Output (EAO)	ITY/441N	13-R	5	Class non IE/IE Isolation Barrier	13T-14/4
4.	Current Loop Output (EAO)	ITY/441N	13-R	4	Class non IE/IE Isolation Barrier	13T-14/4

* Disconnect Function Generator input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

C-58

TABLE A-1b
125 VAC LINE-TO-LINE FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect Transformer to Connections		Isolator Type	I/O Board Location/ Channel #
* 1.	Bistable Partial Trip (EPT) Energized	ITS/441C	13-L	1	2	Class non 1E/1E Isolation Barrier	13T-9/1
2.	Current Loop Output (EAO)	ITY/441N	13-R	4	5	Class non 1E/1E Isolation Barrier	13T-14/4
3.	Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
4.	Digital Contact Output (ECO), Deenergized, NC	ITY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	13T-12/2

* Disconnect function generation input to variable RTD channel (Figure B-1) and use manual switch to control partial trip output condition during fault application.

** Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

C-59

TABLE A-2a
125 VDC LINE-TO-GROUND FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Positive	Negative	Isolator Type	I/O Board Location/ Channel #
* 1.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	1	G	Class non IE/IE Isolation Barrier	13T-9/1
* 2.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	2	G	Class non IE/IE Isolation Barrier	13T-9/1
* 3.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	G	1	Class non IE/IE Isolation Barrier	13T-9/1
* 4.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	G	2	Class non IE/IE Isolation Barrier	13T-9/1
5.	Current Loop Output (EAO)	ITY/441N	13-R	4	G	Class non IE/IE Isolation Barrier	13T-14/4

G = Earth ground (third prong of AC power feed)

* Disconnect function generator input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

TABLE A-2a (Continued)

125 VDC LINE-TO-GROUND FAULT CONNECTIONS

Channel #	i/O Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
6.	Current Loop Output (EAO)	ITY/441N	13-R	5	G	Class non IE/IE Isolation Barrier	13T-14/4
7.	Current Loop Output (EAO)	ITY/441N	13-R	G	4	Class non IE/IE Isolation Barrier	13T-14/4
8.	Current Loop Output (EAO)	ITY/144N	13-R	G	5	Class non IE/IE Isolation Barrier	13T-14/4

G = Earth ground (third prong of AC power feed)

C-61

TABLE A-2b
125 VDC LINE-TO-LINE FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
* 1.	Bistable Partial Trip (EPT) Energized	ITS/441C	13-L	1	2	Class non IE/IE Isolation Barrier	13T-9/1
* 2.	Bistable Partial Trip (EPT) Energized	ITS/441C	13-L	2	1	Class non IE/IE Isolation Barrier	13T-9/1
3.	Current Loop Output (EAO)	ITY/441P	13-T	4	5	Class non IE/IE Isolation Barrier	13T-14/4
4.	Current Loop Output (EAO)	ITY/441N	13-R	5	4	Class non IE/IE Isolation Barrier	13T-14/4
5.	Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	7	8	Class non IE/IE Isolation Barrier	13T-12/2

* Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

** Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

C-62

TABLE A-2b (Continued)

125 VDC LINE-TO-LINE FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	DC Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
6.	Digital Contact Output (ECO), Deenergized, NC	ITY/441A	13-M**	7	8	Class non IE/IE Isolation Barrier	13T-12/2
7.	Digital Contact Output (ECO) Energized, NO	ITY/441A	13-M	8	7	Class non IE/IE Isolation Barrier	13T-12/2
8.	Digital Contact Output (ECO) Deenergized, DC	ITY/441A	13-M**	8	7	Class non IE/IE Isolation Barrier	13T-12/2

** Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

C-63

TABLE A-3a

250 VDC LINE-TO-GROUND FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
* 1.	Bistable Partial Trip (EPT) Energized	ITS/441C	13-L	1	G	Class non IE/IE Isolation Barrier	13T-9/1
* 2.	Bistable Partial Trip (EPT) Energized	ITS/144C	13-L	2	G	Class non IE/IE Isolation Barrier	13T-9/1
* 3.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	G	1	Class non IE/IE Isolation Barrier	13T-9/1
* 4.	Bistable Partial Trip (EPT), Energized	ITS/441C	13-L	G	2	Class non IE/IE Isolation Barrier	13T-9/1
* 5.	Bistable Partial Trip (EPT), Deenergized	ITS/441C	13-L	1	G	Class non IE/IE Isolation Barrier	13T-9/1
* 6.	Bistable Partial Trip (EPT), Deenergized	ITS/441C	13-L	2	G	Class non IE/IE Isolation Barrier	13T-9/1

G - Earth Ground (third prong of AC power feed)

* Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

TABLE A-3a (Continued)

250 VDC LINE-TO-GROUND FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
* 7.	Bistable Partial Trip (EPT) Deenergized	ITS/441C	13-L	G	1	Class non 1E/1E Isolation Barrier	13T-9/1
* 8.	Bistable Partial Trip (EPT) Deenergized	ITS/441C	13-L	G	2	Class non 1E/1E Isolation Barrier	13T-9/1
9.	Current Loop Output (EAO)	ITY/441N	13-R	4	G	Class non 1E/1E Isolation Barrier	13T-14/4
10.	Current Loop Output (EAO)	ITY/441N	13-R	5	G	Class non 1E/1E Isolation Barrier	13T-14/4
11.	Current Loop Output (EAO)	ITY/441N	13-R	G	4	Class non 1E/1E Isolation Barrier	13T-14/4
12.	Current Loop Output (EAO)	ITY/441N	13-R	G	5	Class non 1E/1E Isolation Barrier	13T-14/4

G - Earth Ground (third prong of AC power feed)

* Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

TABLE A-3a (Continued)

250 VDC LINE-TO-GROUND FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	DC Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
13.	Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	7	G	Class non 1E/1E Isolation Barrier	13T-12/2
14.	Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	G	7	Class non 1E/1E Isolation Barrier	13T-12/2
15.	Digital Contact Output (ECO), Energized, NC	ITY/441A	13-M**	7	G	Class non 1E/1E Isolation Barrier	13T-12/2
16.	Digital Contact Output (ECO), Energized, NC	ITY/441A	13-M**	G	7	Class non 1E/1E Isolation Barrier	13T-12/2

G = Earth Ground (third prong of AC power feed)

** Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

C-66

TABLE A-3b
250 VDC LINE-TO-LINE FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	DC Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
* 1.	Bistable Partial Trip (EPT) Energized	ITS/441C	13-L	1	2	Class non IE/IE Isolation Barrier	13T-9/1
* 2.	Bistable Partial Trip (EPT) Energized	ITS/144C	13-L	2	1	Class non IE/IE Isolation Barrier	13T-9/1
* 3.	Bistable Partial Trip (EPT), Deenergized	ITS/441C	13-L	1	2	Class non IE/IE Isolation Barrier	13T-9/1
* 4.	Bistable Partial Trip (EPT), Deenergized	ITS/441C	13-L	2	1	Class non IE/IE Isolation Barrier	13T-9/1
5.	Current Loop Output (EAO)	ITY/441N	13-R	4	5	Class non IE/IE Isolation Barrier	13T-14/4
6.	Current Loop Output (EAO)	ITY/441N	13-R	5	4	Class non IE/IE Isolation Barrier	13T-14/4

* Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

C-67

TABLE A-3b (Continued)
250 VDC LINE-TO-LINE FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect DC Positive	Power Supply Negative	Isolator Type	I/O Board Location/Channel #
7.	Digital Contact Output (ECO) Energized, NO	ITY/441A	13-M	7	8	Class non Isolation Barrier 1E/1E	13T-12/2
8.	Digital Contact Output (ECO) Deenergized, NC	ITY/144A	13-M**	7	8	Class non Isolation Barrier 1E/1E	13T-12/2
9.	Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	8	7	Class non Isolation Barrier 1E/1E	13T-12/2
10.	Digital Contact Output (ECO) Deenergized, NC	ITY/441A	13-M*	8	7	Class non Isolation Barrier 1E/1E	13T-12/2
11.	Digital Contact Output (ECO), Deenergized, NO	ITY/441A	13-M	7	8	Class non Isolation Barrier 1E/1E	13T-12/2

* Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

** Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

C-68

TABLE A-3b (Continued)

250 VDC LINE-TO-LINE FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect Positive	DC Power Supply Negative	Isolator Type	I/O Board Location/ Channel #
12.	Digital Contact Output (ECO) Energized, NC	ITY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
13.	Digital Contact Output (ECO) Deenergized, NO	ITY/144A	13-M	8	7	Class non 1E/1E Isolation Barrier	13T-12/2
14.	Digital Contact Output (ECO), Energized, NC	ITY/441A	13-M**	8	7	Class non 1E/1E Isolation Barrier	13T-12/2

** Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

C-69

TABLE A-4a
580 VAC LINE-TO-GROUND FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect Transformer Secondary Hot Lead to Connection	Isolator Type	I/O Board Location/ Channel #
* 1.	Bistable Partial Trip (EPT) Energized	ITS/441C	13-L	1	Class non 1E/1E Isolation Barrier	13T-9/1
* 2.	Bistable Partial Trip (EPT) Energized	ITS/144C	13-L	2	Class non 1E/1E Isolation Barrier	13T-9/1
* 3.	Bistable Partial Trip (EPT), Deenergized	ITS/441C	13-L	1	Class non 1E/1E Isolation Barrier	13T-9/1
* 4.	Bistable Partial Trip (EPT), Deenergized	ITS/441C	13-L	2	Class non 1E/1E Isolation Barrier	13T-9/1
5.	Current Loop Output (EAO)	ITY/441N	13-R	4	Class non 1E/1E Isolation Barrier	13T-14/4
6.	Current Loop Output (EAO)	ITY/441N	13-R	5	Class non 1E/1E Isolation Barrier	13T-14/4

* Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

C-70

TABLE A-4: (Continued)

580 VAC LINE-TO-GROUND FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect Transformer Secondary Hot Lead to Connection	Isolator Type	I/O Board Location/ Channel #
7.	Digital Contact Output (ECO) Energized, NO	ITY/441A	13-M	7	Class non IE/IE Isolation Barrier	13T-12/2
8.	Digital Contact Output (ECO) Energized, NC	ITY/144A	13-M**	7	Class non IE/IE Isolation Barrier	13T-12/2

** Move wire terminated on 13T-12-6 to 12-T-12-7 to test NC configuration.

C-71

TABLE A-4b
580 VAC LINE-TO-LINE FAULT CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect Transformer to Connection		Isolator Type	I/O Board Location/ Channel #
* 1.	Bistable Partial Trip (EPT) Energized	ITS/441C	13-L	1	2	Class non IE/IE Isolation Barrier	13T-9/1
* 2.	Bistable Partial Trip (EPT) Deenergized	ITS/144C	13-L	1	2	Class non IE/IE Isolation Barrier	13T-9/1
3.	Current Loop Output (EAO)	ITY/441N	13-R	4	5	Class non IE/IE Isolation Barrier	13T-14/4
4.	Digital Contact Output (ECO), Energized, NO	ITY/441A	13-M	7	8	Class non IE/IE Isolation Barrier	13T-14/4
5.	Digital Contact Output (ECO), Deenergized, NC	ITY/441A	13-M**	7	8	Class non IE/IE Isolation Barrier	13T-12/2
6.	Digital Contact Output (ECO), Deenergized, NO	ITY/441A	13-M	7	8	Class non IE/IE Isolation Barrier	13T-12/2
7.	Digital Contact Output (ECO) Energized, NC	ITY/441A	13-M**	7	8	Class non IE/IE Isolation Barrier	13T-12/2

* Disconnect function generation input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during fault application.

** Move wire terminated on 13-T-12-6 to 13-T-12-7 to test NC configuration.

ATTACHMENT B
FIELD CONNECTIONS AND SIMULATION

See test procedure JPD-111687-0 figures B-3 through B-9 for input simulation and input/output monitoring connections.

Cabinet Configuration Information:

The cabinet under test, Qualification Unit 2, is an exact replica of Watts Bar Nuclear Power Station Protection Rack 13. The following drawings document the cabinet configuration. Copies of these drawings will be included as part of the final test report.

<u>Drawing Description</u>	<u>Drawing Number/Rev.</u>
Terminal Block Wiring Diagram, Protection Set 4	1-47043 PW-13, rev. 3E
Process Control Block Diagram, Delta T/T _{AVG} System	108D408 sh. 10, rev. 11
Process Control Block Diagram, W.R. S.G. Level	108D408 sh. 34, rev. 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temp.	108D408 sh. 38, rev. 4
Process Control Block Diagram, RHR Pump Discharge Temp	108D408 sh. 39, rev. 5
Process Control Block Diagram, RCS Wide Range Pressure	108D408 sh. 43, rev. 1
Eagle-21 Schematic Diagrams, Rack 13 Protection Set 4	1856E69 sh. 2, rev. 2

ATTACHMENT C
TRANSIENT DATA RECORDING SYSTEM CONNECTIONS

This attachment contains the following:

- o Table C-1a Tape Recorded Data, Current Loop Output Test
- o Table C-1b Tape Recorder Data, Digital Contact Output Test
- o Table C-1c Tape Recorder Data, Partial Trip Output Test

- o Table C-2a Data Logger Recorded Data, Current Loop Output Test
- o Table C-2b Data Logger Recorder Data, Digital Contact Output Test
- o Table C-2c Data Logger Recorder Data, Partial Trip Output Test

- o Table C-3a Strip Chart Recorded Data, Current Loop Output Test
- o Table C-3b Strip Chart Recorder Data, Digital Contact Output Test
- o Table C-3d Strip Chart Recorder Data, Partial Trip Output Test

TABLE C-1a
TAPE RECORDED DATA, CURRENT LOOP OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer Amplifier Gain
				Hi	Lo	Sh	
1.	Analog Output E/I	ITY/441L	13-P	10	11	12	10
2.	Analog Output E/I	ITY/503A	13-J	10	11	12	10
3.	Analog Output E/I	ITY/502A	13-J	7	8	9	10
4.	Analog Output E/I	ITY/441Q	13-S	1	2	3	10
5.	Analog Output E/I	ITY/441G	13-H	1	4	5	10
6.	Analog Output E/I	ITY/441F	13-J	1	4	5	10
7.	Analog Output E/I	ITY/502B	13-K	1	4	5	10
8.	Analog Output E/I	ITY/442C	13-F	9	11	12	10
9.	Analog Output E/I	ITY/441M	13-R	1	2	3	10
10.	Analog Output E/I	ITY/441P	13-R	7	8	9	10
11.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
12.	Analog Output E/I	ITY/503B	13-K	7	10	11	10
13.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
14.	Analog Output E/I	ITY/454B	13-F	1	2	3	10

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

** Monitor function generator output signal. See figure B-3.

TABLE C-1b
TAPE RECORDED DATA, DIGITAL CONTACT OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer Amplifier Gain
				Hi	Lo	Sh	
1.	Bistable Partial Trip	ITS/442D	13-M	3	4		.05
2.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
3.	Contact Output	ITY/441C	13-M	11	12		.02
4.	Contact Output	ITY/441D	13-M	9	10		.02
5.	Analog Output E/I	ITY/441G	13-H	1	4	5	10
6.	Analog Output E/I	ITY/441F	13-J	1	4	5	10
7.	Contact Output	ITY/441	13-M	5	6		.02
8.	Analog Output E/I	ITY/442C	13-G	1	2	3	10
9.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
10.	Analog Output E/I	ITY/441H	13-P	1	2	3	10
11.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
12.	Analog Output E/I	ITY/441J	13-P	4	5	6	10
13.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
14.	Function Generator Sig.	N/A	**				.05

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

** Monitor function generator output signal. See figure B-3.

Note: For ECO test move EPT board and termination frame wiring from T-10 to T-11.

TABLE C-1c
TAPE RECORDED DATA, PARTIAL TRIP OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer Amplifier Gain
				Hi	Lo	Sh	
1.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
2.	Bistable Partial Trip	ITS/442D	13-M	3	4		.05
3.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
4.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
5.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
6.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
7.	Analog Input I/E	IPY/408	*				20
8.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
9.	Analog Input I/E	IPY/458Q	*				10
10.	Analog Output E/I	ITY/441G	13-H	1	4	5	10
11.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
12.	Analog Output E/I	ILY/503B	13-K	7	10	11	10
13.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
14.	Function Generator Sig.	N/A	**				.05

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

** Monitor function generator output signal. See figure B-3.

TABLE C-2a
DATA LOGGER RECORDED DATA, CURRENT LOOP OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection		
				Hi	Lo	Sh
6.	Analog Input E/E	INY/441B	13-C	1	2	3
7.	Analog Input E/E	INY/441A	13-C	4	5	6
21.	Analog Output E/I	ITY/441L	13-P	10	11	12
22.	Analog Output E/I	ITY/441M	13-R	1	2	3
23.	Analog Output E/I	ITY/442C	13-F	9	11	12
24.	Analog Output E/I	ITY/442G	13-G	1	2	3
25.	Analog Output E/I	ITY/441G	13-H	1	4	5
26.	Analog Output E/I	ITY/441E	13-H	7	10	11
27.	Analog Output E/I	ITY/441F	13-J	1	4	5
28.	Analog Output E/I	ITY/441P	13-R	7	8	9
29.	Analog Output E/I	ITY/441Q	13-S	1	2	3
30.	Analog Output E/I	ITY/502B	13-K	1	4	5
31.	Analog Output E/I	ITY/503A	13-J	10	11	12
32.	Analog Output E/I	ITY/502A	13-J	7	8	9
33.	Analog Output E/I	ITY/503B	13-K	7	10	11
34.	Analog Output E/I	ITY/454B	13-F	1	2	3
35	Analog Input I/E	IPY/458Q	*			
36	Analog Input I/E	ILY/502	*			
37	Analog Input I/E	ILY/503	*			
38	Analog Input I/E	IPY/408	*			

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE C-2b
DATA LOGGER RECORDED DATA, DIGITAL CONTACT OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection		
				Hi	Lo	Sh
6.	Analog Input E/E	INY/441B	13-C	1	2	3
7.	Analog Input E/E	INY/441A	13-C	4	5	6
9.	Contact Output	ITY/441	13-M	5	6	
10.	Contact Output	ITY/441A	13-M	7	8	
11.	Contact Output	ITY/441C	13-M	11	12	
12.	Contact Output	ITY/441B	13-M	9	10	
22.	Analog Output E/I	ITY/441E	13-F	5	6	7
23.	Analog Output E/I	ITY/442C	13-F	9	11	12
24.	Analog Output E/I	ITY/442G	13-G	1	2	3
25.	Analog Output E/I	ITY/441G	13-H	1	4	5
26.	Analog Output E/I	ITY/441E	13-H	7	10	11
27.	Analog Output E/I	ITY/441F	13-J	1	4	5
28.	Analog Output E/I	ITY/441H	13-P	1	2	3
29.	Analog Output E/I	ITY/441J	13-P	4	5	6
35.	Analog Input I/E	IPY/458Q	*			
36.	Analog Input I/E	ILY/502	*			
37.	Analog Input I/E	ILY/503	*			
38.	Analog Input I/E	IPY/408	*			

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE C-2c
DATA LOGGER RECORDED DATA, PARTIAL TRIP OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection		
				Hi	Lo	Sh
6.	Analog Input E/E	INY/441B	13-C	1	2	3
7.	Analog Input E/E	INY/441A	13-C	4	5	6
21.	Analog Output E/I	ITY/441L	13-P	10	11	12
22.	Analog Output E/I	ITY/441M	13-R	1	2	3
23.	Analog Output E/I	IPY/408B	13-N	7	8	9
24.	Analog Output E/I	ITY/442G	13-G	1	2	3
25.	Analog Output E/I	ITY/441G	13-H	1	4	5
26.	Analog Output E/I	ITY/441E	13-H	7	10	11
27.	Analog Output E/I	ITY/441F	13-J	1	4	5
28.	Analog Output E/I	ITY/441P	13-R	7	8	9
29.	Analog Output E/I	ITY/441Q	13-S	1	2	3
30.	Analog Output E/I	ITY/502B	13-K	1	4	5
31.	Analog Output E/I	ITY/503A	13-J	10	11	12
32.	Analog Output E/I	ITY/502A	13-J	7	8	9
33.	Analog Output E/I	ITY/503B	13-K	7	10	11
34.	Analog Output E/I	ITY/454B	13-F	1	2	3
35.	Analog Input I/E	IPY/458Q	*			
36.	Analog Input I/E	ILY/502	*			
37.	Analog Input I/E	ILY/503	*			
38.	Analog Input I/E	IPY/408	*			

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE C-3a
STRIP CHART RECORDED, CURRENT LOOP OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer*** Amplifier Gain
				Hi	Lo	Sh	
1.	Analog Output E/I	ITY/454B	13-F	1	2	3	10
2.	Analog Output E/I	ITY/441L	13-P	10	11	12	10
3.	Analog Output E/I	ILY/503A	13-J	10	11	12	10
4.	Analog Output E/I	ILY/502A	13-J	7	8	9	10
5.	Analog Output E/I	ITY/441Q	13-S	1	2	3	10
6.	Analog Output E/I	ITY/441G	13-H	1	4	5	10
7.	Analog Output E/I	ITS/441F	13-J	1	4	5	10
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
9.	Analog Output E/I	ILY/502B	13-K	1	4	5	10
10.	Analog Output E/I	ITY/442C	13-F	9	11	12	10
11.	Analog Output E/I	ITY/441M	13-R	1	2	3	10
12.	Analog Output E/I	ITY/441P	13-R	7	8	9	10
13.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
14.	Analog Output E/I	ILY/503B	13-K	7	10	11	10
15.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

** Monitor function generator output signal. See figure B-3.

*** Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

TABLE C-3b
STRIP CHART RECORDED, DIGITAL CONTACT OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer*** Amplifier Gain
				Hi	Lo	Sh	
1.	Function Generator Sig.	N/A	**				.05
2.	Bistable Partial Trip	ITS/442D	13-M	3	4		.05
3.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
4.	Contact Output	ITY/441C	13-M	11	12		.02
5.	Contact Output	ITY/441B	13-M	9	10		.02
6.	Analog Output E/I	ITY/441G	13-H	1	4	5	10
7.	Analog Output E/I	ITY/441F	13-J	1	4	5	10
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
9.	Contact Output	ITY/441	13-M	5	6		.02
10.	Analog Output E/I	ITY/442C	13-G	1	2	3	10
11.	Analog Output E/I	ITY/441E	13-H	1	2	3	10
12.	Analog Output E/I	ITY/441H	13-P	1	2	3	10
13.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
14.	Analog Output E/I	ITY/441J	13-P	4	5	6	10
15.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

- * Measure current across 20 ohm transmitter test resistor. See figure B-4.
- ** Monitor function generator output signal. See figure B-3.
- *** Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

TABLE C-3c
STRIP CHART RECORDED, PARTIAL TRIP OUTPUT TEST

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer*** Amplifier Gain
				Hi	Lo	Sh	
1.	Function Generator Sig.	N/A	**				.05
2.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
3.	Bistable Partial Trip	ITS/442D	13-M	3	4		.05
4.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
5.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
6.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
7.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
9.	Analog Input I/E	IPY/408	*				20
10.	Analog Output E/I	IPY/408B	13-M	7	8	9	10
11.	Analog Input I/E	IPY/458Q	*				10
12.	Analog Output E/I	ITY/441G	13-H	1	4	5	10
13.	Analog Output E/I	ITY/442G	13-G	1	2	3	10
14.	Analog Output E/I	ILY/503B	13-K	7	10	11	10
15.	Analog Output E/I	ITY/441E	13-H	7	10	11	10
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

- * Measure current across 20 ohm transmitter test resistor. See figure B-4.
- ** Monitor function generator output signal. See figure B-3.
- *** Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

JPD 111687-2

DATE
11/16/87

REVISION NO.
0

SURGE WITHSTAND CAPABILITY TEST PROCEDURE
FOR
EAGLE-21 PROTECTION
SYSTEM

1.0 INTRODUCTION

This procedure details the Surge Withstand Capability (SWC) tests to be performed on the Eagle-21 protection system.

These tests will consist of applying the surge withstand test wave to the following system interfaces and measuring the effects on system input/output processing.

- o Digital Contact Output (NO and NC configurations), class non-1E/1E isolator
- o Partial Trip Output (energized and deenergized conditions), class non-1E/1E isolator
- o Current Loop Output 10-50 mA, class non-1E/1E isolator
- o Current Loop Input (4-20 mA, 10-50 mA, with and without loop power supply)
- o WR RTD Input
- o WR RTD Input (0-10 volt application)
- o NR RTD Input
- o Cabinet AC power feed

The test configuration is documented in Attachments B and C.

2.0 PREPARATION FOR TEST

2.1 Connect the field cabling to sensor simulation, load simulation, and contact output loads per Attachments B, C and table 1-1.

2.2 Obtain system baseline data:

2.2.1 System baseline data will be taken to verify system operation. Input voltage and current and resistance values corresponding to 0 - 100% of scale in 25% increments and record. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.

2.2.2 Set signal inputs per table 1-1. Adjust analog input signals, using the MMI to obtain the expected engineering unit values specified in table 1-1. Using figure B-6 in Noise Test Procedure JPD-111687-0 as a reference, adjust the variable RTD channel per the following procedure:

- o Open the manual switch input to the variable RTD board.
- o Adjust the high adjust potentiometer so that channel TE-441A3 reads $618.261 \pm .375$ Deg f on the MMI.
- o Verify that the TAVG MMI reading equals $589.740 + .2$ Deg f. Verify the following actual bistable output status:

TS/441C = Not Tripped
TS/441G = Not Tripped
TS/441D = Not Tripped
TS/441H = Not Tripped
TS/442D = Tripped
TS/442G = Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Close the manual switch input to the variable RTD board.
- o Adjust the low adjust potentiometer so that channel TE-441A3 reads $615.501 \pm .375$ Deg f on the MMI.
- o Verify that the Delta T MMI reading equals $104.237 - .3$ PU. Verify the following actual bistable output status:

TS/1441C = Tripped
TS/1441G = Tripped
TS/1441D = Tripped
TS/1441H = Tripped

TS/1442D = Not Tripped

TS/1442G = Not Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Open the manual switch input to the variable RTD board and record the results. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.

2.2.3 Set the function generator output to the variable RTD board (see figure B-3 in Noise Test Procedure JPD-111687-0) in the positive square wave pulse mode with a 0-5 volt amplitude at .05HZ and a duty cycle of approximately 10%.

2.2.4 Close the recorder start switch and verify that the trip output signals switch upon receipt of the function generator switch signal (positive square wave pulse).

3.0 SWC TEST PROCEDURE SEQUENCE

The SWC test sequence described below will be followed for each noise test type specified in Sections 4.0 and 5.0.

3.1 Pretest

Obtain a data logger printout of "normal" analog input/output and digital output values.

3.2 Disconnect data logger. Configure the []_{b,c} and []_{b,c} isolation network as shown in figure 1-3. Set the surge generator at 120 HZ repetition rate, 3.3 KV crest voltage and timed output with a 3 second duration.

- 3.3 Connect the isolation network line out connection to the channel under test and verify the readiness of the data acquisition system. Enter identifying records in tape recorder log and surge test data sheet (figure 1-4). Follow the test specific instructions given in sections 4 and 5.
- 3.4 Disconnect the data logger, close the recorder start switch, start the tape recorder and record 2 minutes of pretest data. Increase strip chart speed to 25 mm/sec. Simultaneously energize the surge generator and close the event marker switch. Monitor the surge waveform on the oscilloscope and deenergize the event marker upon removal of the surge. Decrease chart speed to 100 mm/min. Observe the strip chart recorder and record and analog output signal deviations and/or trip output status failures. A trip output status failure is defined as a failure of a trip output signal to switch upon receipt of the switch signal from the test station. Record 2 minutes of post test data. Open the recorder start switch and stop the tape recorder.
- 3.5 Obtain a data logger printout and confirm system recovery by comparing to pretest data. Record any discrepancies. Record any component damage incurred.
- 3.6 With the system confirmed to be in the pretest condition, proceed to the next test.

4.0 COMMON MODE SWC TEST

- 4.1 Connect the []_{b,c} isolation network line out terminals to the designated terminal block connections as specified in Table A-1a. Use hook-up wire to make connections and minimize lead length.
- 4.2 Connect the surge generator "High" output to surge transient input 1 of the isolation network. Connect the surge generator "Low" output to the ground connector of the isolation network.

- 4.3 Connect the surge generator chassis ground to the isolation network ground.
- 4.4 Set the isolation network mode switch to the "Common Mode" position.
- 4.5 Follow the test sequence described in section 3 for each channel designated in Table A-1a.

5.0 TRANSVERSE MODE SWC

- 5.1 Connect the []_{b,c} isolation network line and terminal to the designated terminal block connections as specified in Table A-1b. Use hook-up wire to make connections and minimize lead length.
- 5.2 Connect the surge generator "High" output to surge transient input 1 of the isolation network. Connect the surge generator "Low" output to surge generator transient input 2 of the isolation network.
- 5.3 Connect the surge generator chassis ground to the isolation network ground.
- 5.4 Set the isolation network mode switch to the "Transverse Mode" position.
- 5.5 Follow the test sequence described in Section 3 for each channel designated in table A-1b.

6.0 ACCEPTANCE CRITERIA

6.1 Description

The acceptance criteria for the Eagle 21 (1E Safety Related System) is that the system shall remain operational and maintain protective actions before, during and after application of the surge withstand test wave to designated class non-1E to class 1-E isolators. In addition, no component damage or change in channel calibration shall occur due to the application of the SWC test wave to any cabinet input/output excluding the test panel and MMI communication connection.

(See figure 5-12a of WCAP test report)

Figure 1-1 Common Mode SWC Test Connections

(See figure 5-12b of WCAP test report)

Figure 1-2 Transverse Mode SWC Test Connections

(See figure 5-12c of WCAP test report)

Figure 1-3 Block Diagram of SWC Test

SURGE TEST DATA SHEET

Procedure Rev. _____
DATE _____
TEST # _____

TYPE

TRANSVERSE MODE _____

COMMON MODE _____

TEST INJECTION POINT _____ I/O CARD TYPE _____ POINT # _____

PRE-TEST

DATA LOGGER VERIFICATION PRINT OUTPUT # _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATION _____

DISCONNECT DATA LOGGER _____

TEST

TAPE RECORDER FOOTAGE BEGIN _____ END _____ SET # _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATION _____

POST-TEST

DATA LOGGER DATA VERIFICATION* PRINT OUTPUT # _____

SYSTEM STATUS: _____

REMARKS AND TEST OBSERVATION _____

PERFORMED _____ REVIEWED _____

Figure 1-4 Surge Test Data Sheet

TABLE 1-1
SIMULATED INPUT SIGNAL

Channel Name	Channel Tag #	Terminal Block	Terminal Connection			I/O Board Location	I/O Board Connection			Simulator Signal	Expect in E.U
			Hi	Lo	Sh		Hi	Lo	Sh		
1. Neutron Flux Lower Ion	NY-441A	13-C	4	5	6	13T-4	8	13		3.00	16.00
2. Neutron Flux Upper Ion	NY-441B	13-C	1	2	3	13T-4	2	6		4.84 volt	20.00
3. Pressurizer Pressure	PY/458Q	13-W	-	-	-	13T-6	11	12	14	38.75 MA	2235 ±
4. Cold Leg Temperature	TE-441B	13-B	1,2	4,3	5	13T-6	8,3	7,4	1	425.888 ohms	562.70
5. Cold Leg Temperature	TE-440B	13-B	7,8	10,9	11	13T-6	8,11	9,12	14	425.888 ohms	562.70
6. Hot Leg Temperature	TE-441A1	13-A	1,2	4,3	5	13T-5	6,3	7,4	1	447.302 ohms	616.04
7. Hot Leg Temperature	TE-441A2	13-A	7,8	10,9	11	13T-5	8,11	9,12	14	447.302 ohms	616.04
8. Hot Leg Temperature	TE-441A3	13-C	8,9	11,10	12	13T-5	20,17	21,18	15	xx ohms	± XX
9. Steam Generator Level Loop 2	LT-502	13-E	1	2	3	13T-2	8	11	14	20 MA	25 ±
10. Steam Generator Level Loop 3	LT-503	13-E	4	5	6	13T-2	20	17	15	40 MA	75 ±
11. RCS Wide Range Pressure	PT-408	13-W	1	2	3	13T-6	20	18	15	12 MA	1500 ±
12. Pressurizer Vapor Temp	TE-454	13-D	1,2	4,3	5	13T-4	20,17	21,18	15	400 OHMS	400.26
13. Residual Heat Removal Pump Discharge Temp	TE-612	13-D	8,9	11,10	12	13T-4	22,25	23,26	28	300 OHMS	280.40

NOTE: - XX - Variable RTD input, set nominally at 447.175 ohms (615.502 Deg f) for the low resistance reading and 448.284 ohms (618.261 Deg f) for the high resistance reading. See step 2.3.2 for details.

C-95

ATTACHMENT A
SWC TEST CONNECTIONS

NOTE: Use two isolation networks for Bistable Partial Trip and Cabinet AC power input common and transverse mode tests. Install isolation network No. 1 to protect the test lab AC power source. Install isolation network No. 2 to protect the test station trip output monitoring device. Disconnect isolation network "line in" connection during surge application for all transverse mode tests excluding the cabinet AC power input test.

This attachment contains the following tables:

- o Table A-1a - Common Mode SWC Test Connections
- o Table A-1b - Transverse Mode SWC Test Connections

TABLE A-1a
COMMON MODE SWC TEST CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	CONNECT LINE-OUT TO		Isolator Type	I/O Board Location/ Channel #
				Terminal Connection Hi	Terminal Connection Lo		
*1.	Bistable Partial Trip, Energized	ITS/442G	13-M	1	2	Class non IE/IE Isolation Barrier	13T-10/1
*2.	Bistable Partial Trip, Deenergized	ITS/442G	13-M	1	2	Class non IE/IE Isolation Barrier	13T-10/1
3.	Analog Output	IPY/408A	13-N	4	5	Class non IE/IE Isolation Barrier	13T-16/2
4.	Contact Output (No), Energized	ITY/441A	13-M	7	8	Class non IE/IE Isolation Barrier	13T-12/2
5.	Contact Output (NC), Energized	ITY/441A	13-M**	7	8	Class non IE/IE Isolation Barrier	13T-12/2
6.	Contact Output (No), Deenergized	TY/441A	13-M	7	8	Class non IE/IE Isolation Barrier	13T-12/2

* Disconnect function generator input to variable RTD channel (figure B-1) and use manual switch to control partial trip output condition during surge application.

**Move wire terminated on 13T-12-6 to 13T-12-7 to test NC configuration.

TABLE A-1a (Continued)
COMMON MODE SWC TEST CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	CONNECT LINE-OUT TO		Isolator Type	I/O Board Location/ Channel #
				Terminal Connection Hi	Terminal Connection Lo		
7.	Contact Output (NC), Deenergized	TY/441A	13-M**	7	8	Class non 1E/1E Isolation Barrier	13T-12/2
8.	WR RTD Input	ITY/612	13-D	8,9	11,10	N/A	13T-4/4
9.	NR RTD Input	ITY/441Y	13-A	7,8	10,9	N/A	13T-5/2
10.	Current Loop Input, Active***	IPY/458Q	13T-8	8,9	11,12	N/A	13T-8/2
11.	Current Loop Input Passive***	IPY/458Q	13T-8	11	12	N/A	13T-8/2
12.	Current Loop Input Active	IPY/408	13-N	1	2	N/A	13T-8/3
13.	WR RTD Input, 0-10 volt application	INY/441A	13-C	4	5	N/A	13T-4/2
14.	Cabinet AC Power Input	N/A	13-W	11	12	N/A	N/A
15.	Contact Output (NO/NC/C), Energized	ITY/441A	13-M	7	8	Class non 1E/1E Isolation Barrier	13T-12/2

**Move wire terminated on 13T-12-6 to 13T-12-7 to test NC configuration.

***Active operation utilizes on-board DC power supply. Passive operation utilizes external power supply.

TABLE A-1a (Continued)
COMMON MODE SWC TEST CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	CONNECT LINE-OUT TO		Isolator Type	I/O Board Location/ Channel #
				Terminal Connection Hi	Terminal Connection Lo		
16.	Contact Output (NO/NC/C), Deenergized	ITY/441A	13-M	7	8	Class non IE/1 Isolation Barrier	13T-12/2
17.	WR RTD Input	ITY/454	13-D	1,2	4,3	N/A	13T-4/3
18.	NR RTD Input	ITY/441X	13-A	1,2	4,3	N/A	13T-5/1
19.	Current Loop Input Active	IPY/458Q	13T-8	8	11	N/A	13T-8/2

001-5

TABLE A-1b
TRANSVERSE MODE SWC TEST CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect Line-Out		Isolator Type	I/O Board Location/ Channel #
				Hi	Lo		
*1.	Bistable Partial Trip, Energized	ITS/442G	13-M	1	2	Class non IE/IE Isolation Barrier	13T-10/1
*2.	Bistable Partial Trip, Deenergized	ITS/442G	13-M	1	2	Class non IE/IE Isolation Barrier	13T-10/1
3.	Analog Output	IPY/408A	13-N	4	5	Class non IE/IE Isolation Barrier	13T-16/2
4.	Contact Output (NO), Energized	ITY/441A	13-M	7	8	Class non IE/IE Isolation Barrier	13T-12/2
5.	Contact Output (NC), Energized	ITY/441A	13-M**	7	8	Class non IE/IE Isolation Barrier	13T-12/2
6.	Contact Output (NO), Deenergized	ITY/441A	13-M	7	8	Class non IE/IE	13T-12/2
7.	Contact Output (NC), Deenergized	ITY/441A	13-M**	7	8	Class non IE/IE Isolation Barrier	13T-12/2

C-101

TABLE A-1b (Continued)
TRANVERSE MODE SMC TEST CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect Line-Out		Isolator Type	I/O Board Location/ Channel #
				Hi	Lo		
8.	WR RTD Input	ITY/612	13-D	8	9	N/A	13T-4/4
9.	WR RTD Input	ITY/612	13-D	10	11	N/A	13T-4/4
10.	WR RTD Input	ITY/612	13-D	8	10	N/A	13T-4/4
11.	WR RTD Input	ITY/612	13-D	8	11	N/A	13T-4/4
12.	WR RTD Input	ITY/612	13-D	9	10	N/A	13T-4/4
13.	WR RTD Input	ITY/612	13-D	7	11	N/A	13T-4/4
14.	Current Loop Input, Active	IPY/458Q	13T-8	8	11	N/A	13T-8/2
15.	Current Loop Input, Active	IPY/458Q	13T-8	8	9	N/A	13T-8/2
16.	Current Loop Input, Active	IPY/458Q	13T-8	11	12	N/A	13T-8/2
17.	Current Loop Input, Passive	IPY/458Q	13T-8	8	9	N/A	13T-8/2
18.	Current Loop Input, Active	IPY/408	13-N	1	2	N/A	13T-8/3

C-102

TABLE A-1b (Continued)

TRANVERSE MODE SWC TEST CONNECTIONS

Channel #	I/O Description	Channel Tag #	Terminal Block	Connect Line-Out		Isolator Type	I/O Board Location/ Channel #
				Hi	Lo		
19.	WR RTD Input, 0-10 Volt Application	INY/441A	13-C	4	5	N/A	13T-4/2
20.	Cabinet AC Power Input	N/A	13-W	1	2	N/A	N/A
21.	Contact Output (NO/NC), Energized	ITY/441A	13-M	7	8	Class non IE/IE Isolation Barrier	13T-12/2
22.	Contact Output (NO/NC), Deenergized	ITY/441A	13-M	7	8	Class non IE/IE Isolation Barrier	13T-12/2
23.	WR RTD Input	ITY/454	13-D	2	3	N/A	13T-4/3
24.	WR RTD Input	ITY/454	13-D	1	4	N/A	13T-4/3
25.	NR RTD Input	ITY/441X	13-A	2	3	N/A	13T-5/1
26.	NR RTD Input	ITY/441X	13-A	1	4	N/A	13T-5/1
27.	NR RTD Input	ITY/441Y	13-A	9	10	N/A	13T-5/2
28.	NR RTD Input	ITY/441Y	13-A	8	11	N/A	13T-5/2

C-103

ATTACHMENT B
FIELD CONNECTIONS AND SIMULATION

See test procedure JPD-111687-0 figures B-3 through B-9 for input simulation and input/output monitoring connections.

Cabinet Configuration Information:

The cabinet under test, Qualification Unit 2, is an exact replica of Watts Bar Nuclear Power Station Protection Rack 13. The following drawings document the cabinet configuration. Copies of these drawings will be included as part of the final test report.

<u>Drawing Description</u>	<u>Drawing Number/Rev.</u>
Terminal Block Wiring Diagram, Protection Set 4	1-47043 PW-13, rev. 3E
Process Control Block Diagram, Delta T/T_{AVG} System	108D408 sh. 10, rev. 11
Process Control Block Diagram, W.R. S.G. Level	108D408 sh. 34, rev. 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temp.	108D408 sh. 38, rev. 4
Process Control Block Diagram, RHR Pump Discharge Temp	108D408 sh. 39, rev. 5
Process Control Block Diagram, RCS Wide Range Pressure	108D408 sh. 43, rev. 1
Eagle-21 Schematic Diagrams, Rack 13 Protection Set 4	1856E69 sh. 2, rev. 2

ATTACHMENT C
TRANSIENT DATA RECORDING SYSTEM CONNECTIONS

This attachment contains the following:

- o Table C-1 Tape Recorded Data
- o Table C-2 Data Logger Recorded Data
- o Table C-3 Strip Chart Recorded Data

TABLE C-1
TAPE RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer Amplifier Gain
				Hi	Lo	Sh	
1.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
2.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
3.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
4.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
5.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
6.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
7.	Contact Output	ITY/441	13-M	5	6		.02
8.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
9.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
10.	Analog Input I/E	IPY/458Q	*				10
11.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
12.	Analog Input I/E	IPY/408	*				20
13.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
14.	Function Generator Sig.	N/A	**				.05

*Measure current across 20 ohm transmitter test resistor. See figure B-4.

**Monitor function generator output signal. See figure B-3.

TABLE C-2
DATA LOGGER RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection		
				Hi	Lo	Sh
6.	Analog Input E/E	INY/441B	13-C	1	2	3
7.	Analog Input E/E	INY/441A	13-C	4	5	6
9.	Contact Output	ITY/441	13-M	5	6	
10.	Contact Output	ITY/441A	13-M	7	8	
22.	Analog Output E/I	ITY/441L	13-P	10	11	12
23.	Analog Output E/I	ITY/454A	13-G	4	5	6
24.	Analog Output E/I	ITY/441K	13-P	7	8	9
25.	Analog Output E/I	ILY/502B	13-K	1	4	5
26.	Analog Output E/I	IPY/408B	13-N	7	8	11
27.	Analog Output E/I	ILY/503B	13-K	7	10	11
35	Analog Input I/E	IPY/458Q	*			
36	Analog Input I/E	ILY/502	*			
37	Analog Input I/E	ILY/503	*			
38	Analog Input I/E	IPY/408	*			

*Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE C-3
STRIP CHART RECORDED

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer*** Amplifier Gain
				Hi	Lo	Sh	
1.	Function Generator Sig.	N/A	**				.05
2.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
3.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
4.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
5.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
6.	Bistable Partial Trip	ITS/441H	13-I	7	8		.05
7.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
9.	Contact Output	ITY/441	13-M	5	6		.02
10.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
11.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
12.	Analog Input I/E	IPY/458Q	*				10
13.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
14.	Analog Input I/E	IPY/408	*				20
15.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

** Monitor function generator output signal. See figure B-3.

*** Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

JPD 111687-3

DATE
11/16/87

REVISION NO.
0

RADIO FREQUENCY INTERFERENCE TEST PROCEDURE
FOR
EAGLE-21 PROTECTION
SYSTEM

4274N:4

C-111

1.0 INTRODUCTION

This procedure details the Radio Frequency Interference (RFI) tests performed on the Eagle-21 protection system.

These tests will consist of exposing the Eagle-21 protection system to a known electromagnetic field and measuring the effects on system input/output processing. Tests are to be conducted per the intent of SAMA standard PMC 33.1-1978, Class 1 and 2, bands a, b and c.

The test configuration is documented in Attachments A and B.

2.0 PREPARATION FOR TEST

2.1 Locate the Eagle-21 cabinet in the anechoic chamber. Position the cabinet such that the cabinet is 1 meter from the transmitting antenna and the center of the microprocessor card cage is 59-1/2 inches from the anechoic chamber floor.

Connect the cabinet bus bar to the test facility ground plane via a short bonding cable.

2.2 Connect the field cabling to sensor simulation, load simulation, and contact output loads per Attachments B and Table 1-1. Input/output signal cabling shall be run in exposed vashed cable trays.

2.3 Obtain system baseline data:

2.3.1 System baseline data will be taken to verify system operation. Input voltage and current and resistance values corresponding to 0 - 100% of scale in 25% increments and record. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.

2.3.2 Set signal inputs per table 1-1. Adjust analog input signals, using the MMI to obtain the expected engineering unit values specified in table 1-1. Using figure B-6 in Noise Test Procedure JPD-111687-0 as a reference, adjust the variable RTD channel per the following procedure:

- o Open the manual switch input to the variable RTD board.
- o Adjust the high adjust potentiometer so that channel TE-441A3 reads $618.261 \pm .375$ Deg f on the MMI.
- o Verify that the TAVG MMI reading equals $589.740 \pm .2$ Deg f. Verify the following actual bistable output status:

TS/441C = Not Tripped
TS/441G = Not Tripped
TS/441D = Not Tripped
TS/441H = Not Tripped
TS/442D = Tripped
TS/442G = Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Close the manual switch input to the variable RTD board.
- o Adjust the low adjust potentiometer so that channel TE-441A3 reads $615.501 \pm .375$ Deg f on the MMI.
- o Verify that the Delta T MMI reading equals $104.237 \pm .3$ PU. Verify the following actual bistable output status:

TS/1441C = Tripped
TS/1441G = Tripped
TS/1441D = Tripped

TS/1441H = Tripped
TS/1442D = Not Tripped
TS/1442G = Not Tripped

Obtain a printout of the Delta T/TAVG system analog inputs, analog test points and comparator information MMI screens.

- o Open the manual switch input to the variable RTD board and record the results. Obtain MMI printout of analog input information and record analog input/output readings via data logger printout.

2.3.3 Using the []_{b,c} Control Computer request a baseline test run of at least 5 data points. Verify that the trip output signals switch upon receipt of the control relay switch signal.

3.0 RFI MODULATION TEST PROCEDURE SEQUENCE

The RFI test sequence described below will be followed for each frequency test run specified in Sections 4.0 through 6.0. See figure 1-1 for a modulation test block diagram.

3.1 Pretest

Obtain a data logger printout of "normal" analog input/output and digital output values.

3.2 Disconnect data logger and verify "antenna" connections and configuration for each frequency run as specified in sections 4.0 through 6.0.

3.3 Initiate a modulation test run via the []_{b,c} control computer. Enter configuration data as prompted by the control computer. Configuration data is specified in sections 4.0 through 6.0 for each

test run. Ready the []_{b,c} Control Computer by entering the calibration file name for the appropriate frequency test run as specification in sections 4.0 through 6.0. Enter the identifying records in the tape recorder log. Simultaneously enter the test run start command via the []_{b,c} control computer and start the tape recorder. The frequency test run will automatically execute until completion without operator intervention. Upon completion of the frequency test run stop the tape recorder and record the ending tape footage.

- 3.4 Review the strip chart recorder printouts and the control computer data sheets and record any analog output signal deviation and/or trip output status failures. Using the MMI investigate any input/output signal processing anomalies to determine cause.
- 3.5 If significant abnormal system performance is measured, calibration file information for the affected frequency should be examined. If the drive signal for the RF signal generator at the affected frequencies is significantly higher than the adjacent frequency signal levels, repeat the affected frequency test at a signal level consistent with adjacent frequencies.
- 3.6 Obtain a data logger printout and confirm system recovery by comparing to pretest data. Record any discrepancies.
- 3.7 With the system confirmed to be in the pretest condition, proceed to the next test.

4.0 20-160 MHZ FREQUENCY RUN

- 4.1 Mount the beconical antenna to the antenna tripod/coupler assembly. Ensure that the antenna center-line is 59-1/2 inches from the anechoic chamber floor and 1 meter from the Eagle-21 cabinet. Connect the []_{b,c} power amplifier to the antenna coupler assembly input.

4.2 Follow the test sequence described in Section 3 for each frequency run specified below:

<u>Cabinet Position</u>	<u>Field Strength</u>	<u>Antenna Polarization</u>	<u>Calibration File</u>
Front	3 v/m	Vert	104A
Front	3 v/m	Horz	101A
Rear	3 v/m	Vert	104A
Rear	3 v/m	Horz	101A
Left side	3 v/m	Vert	104A
Right side	3 v/m	Horz	101A
Front	10 v/m	Horz	102A
Front	10 v/m	Vert	105A
Rear	10 v/m	Horz	102A
Rear	10 v/m	Vert	105A
Left side	10 v/m	Vert	105A
Right side	10 v/m	Horz	102A

5.0 160-500 MHZ FREQUENCY RUN

5.1 Mount the log periodic antenna to the antenna tripod/coupler assembly. Ensure that the antenna center-line is 59-1/2 inches from the anechoic chamber floor and 1 meter from the Eagle-21 cabinet. Connect the []_{b,c} power amplifier to the antenna coupler assembly input.

5.2 Follow the test sequence described in Section 3 for each frequency run specified below:

<u>Cabinet Position</u>	<u>Field Strength</u>	<u>Antenna Polarization</u>	<u>Calibration File</u>
Front	3 v/m	Vert	204A
Front	3 v/m	Horz	201A
Rear	3 v/m	Vert	204A
Rear	3 v/m	Horz	201A

Left side	3 v/m	Horz	201A
Right side	3 v/m	Vert	204A
Front	10 v/m	Horz	202A
Front	10 v/m	Vert	205A
Rear	10 v/m	Horz	202A
Rear	10 v/m	Vert	205A
Left side	10 v/m	Horz	202A
Right side	10 v/m	Vert	205A

6.0 160-500 MHZ FREQUENCY RUN

- 6.1 Mount the log periodic antenna to the antenna tripod/coupler assembly. Ensure that the antenna center-line is 59-1/2 inches from the anechoic chamber floor and 1 meter from the Eagle-21 cabinet. Connect the []_{b,c} power amplifier to the antenna coupler assembly input.
- 6.2 Follow the test sequence described in Section 3 for each frequency run specified below:

<u>Cabinet Position</u>	<u>Field Strength</u>	<u>Antenna Polarization</u>	<u>Calibration File</u>
Front	3 v/m	Vert	304A
Front	3 v/m	Horz	301A
Rear	3 v/m	Vert	304A
Rear	3 v/m	Horz	301A
Left side	3 v/m	Horz	301A
Right side	3 v/m	Vert	304A
Front	10 v/m	Horz	302A
Front	10 v/m	Vert	305A
Rear	10 v/m	Horz	302A
Rear	10 v/m	Vert	305A
Left side	10 v/m	Horz	302A
Right side	10 v/m	Vert	305A

7.0 KEYING TESTS

The keying tests will be performed exposing the most susceptible side of the equipment as determined from the modulation tests. At least three frequency data points per octave must be chosen.

Frequencies which generated input/output processing anomalies during the modulation test should be chosen. If no anomalies occurred over a given octave frequency data points should be evenly spaced. Follow the test sequence below for each keying frequency data point. See figure 1-2 for a keying test block diagram.

- 7.1 Obtain a data logger printout of "normal" analog input/output and digital output values.
- 7.2 Disconnect the data logger and verify proper "antenna" connections for the data point chosen.
- 7.3 Initiate a keying test run via the []_{b,c} Control Computer. Enter configuration data as prompted by the control computer. Manually enter the frequency and amplitude into the RF signal generator using appropriate calibration file information. Manually start the strip chart recorders, the tape recorder and trigger the IBM control computer. The []_{b,c} Control Computer will then automatically execute the keying test. Repeat the above sequence for each selected keying test data point.

Note: Follow the guidelines as stated for the modulation test in step 3.5.

(See figure 5-17 of WCAP test report)

Figure 1-1 Block Diagram of Radio Frequency
Interference Modulation Tests

(See figure 5-18 of WCAP test report)

Figure 1-2 Block Diagram of Radio Frequency
Interference Keying Tests

8.0 ACCEPTANCE CRITERIA

8.1 Description

The acceptance criteria for the Eagle 21 (IE Safety Related System) is that the system shall remain operational while exposed to radio frequency interference and demonstrate recovery upon removal of radio frequency interference.

TABLE 1-1
SIMULATED INPUT SIGNAL

Channel Name	Channel Tag #	Terminal Block	Terminal Connection		I/O Board Location	I/O Board Connection		Simulator Signal	Expected Signal in g.u.
			Ht	Lo		Ht	Lo		
1. Neutron Flux Lower Ion	RY-441A	13-C	4	5	13T-4	9	13	3.00	18.00 ± .095
2. Neutron Flux Upper Ion	RY-441B	13-C	1	2	13T-4	2	6	4.84 volt	28.00 ± .095
3. Pressurizer Pressure	PT/450Q	13-M	-	-	13T-6	11	14	36.75 MA	2235 ± 1.00
4. Cold Leg Temperature	TE-441B	13-B	1,2	4,3	13T-6	6,3	7,4	425.866 ohms	562.70 ± .375
5. Cold Leg Temperature	TE-440B	13-B	7,8	10,9	13T-6	8,11	9,12	425.866 ohms	562.70 ± .375
6. Hot Leg Temperature	TE-441A1	13-A	1,2	4,3	13T-5	6,3	7,4	447.392 ohms	616.041 ± .375
7. Hot Leg Temperature	TE-441A2	13-A	7,8	10,9	13T-5	8,11	9,12	447.392 ohms	616.041 ± .375
8. Hot Leg Temperature	TE-441A3	13-C	6,9	11,10	13T-5	20,17	21,18	xx ohms	± XX
9. Steam Generator Level Loop 2	LT-502	13-E	1	2	13T-2	8	11	20 MA	25 ± .120X
10. Steam Generator Level Loop 3	LT-503	13-E	4	5	13T-2	20	17	40 MA	75 ± .120X
11. RCS Wide Range Pressure	PT-408	13-M	1	2	13T-8	20	18	12 MA	1500 ± 3.76
12. Pressurizer Vapor Temp	TE-454	13-D	1,2	4,3	13T-4	20,17	21,18	400 OHMS	400.200 ± 1.05
13. Residual Heat Removal Pump Discharge Temp	TE-612	13-D	6,9	11,10	13T-4	22,25	23,26	300 OHMS	260.406 ± 1.05

NOTE: - XX - Variable RTD input, set nominally at 447.175 ohms (615.502 Deg F) for the low resistance reading and 448.284 ohms (618.261 Deg F) for the high resistance reading. See step 2.3.2 for details.

RADIO FREQUENCY INTERFERENCE TEST DATA

TARGET: (CABINET POSITION)
 CALIBRATION FILE:
 FIELD STRENGTH LEVEL: (V/m)
 TYPE OF ANTENNA: (LOG PERIODIC OR BICONICAL)
 ANTENNA POLARIZATION: (HORIZONTAL OR VERTICAL)

DATE: _____

TEST PERFORMED BY: _____

REVIEWED BY: _____

TAPE NAME:
 TAPE SET:

TAPE RECORDER START AT: (FOOT)

FREQUENCY: (MHZ)

(DATE)
 (TIME)

EVENT	DIG/INPUT
1	00 0011 (EXPECTED TRIP OUTPUT PATTERN)
2	11 1100
3	00 0011

REMARKS:

FREQUENCY: (MHZ)

(DATE)
 (TIME)

EVENT	DIG/INPUT
1	00 0011
2	11 1100
3	00 0011

REMARKS:

FREQUENCY: (MHZ)

(DATE)
 (TIME)

ERROR IN THE CHANGING CONDITION OF BISTABLE STATUS (TRIP OUTPUT ERROR MESSAGE)

EVENT	DIG/INPUT
1	00 0011
2	11 1101
3	00 0011

REMARKS:

ENDING TAPE RECORDER FOOTAGE FOR THIS SET OF DATA: (FOOT)

Figure 1-3. RFI Modulation Test Data Sheet

RADIO FREQUENCY INTERFERENCE TEST DATA

TARGET: (CABINET POSITION)
 FIELD STRENGTH LEVEL: (V/M)
 TYPE OF ANTENNA: (LOG PERIODIC OR BICONICAL)
 ANTENNA POLARIZATION: (HORIZONTAL OR VERTICAL)

DATE: _____

TEST PERFORMED BY: _____

REVIEWED BY: _____

TAPE NAME:
 TAPE SET:

TAPE RECORDER START AT: (FOOT)

FREQUENCY: (MHZ)

(DATE)
 (TIME)

(EXPECTED TRIP
 OUTPUT PATTERNS)

EVENT	(FIRST KEY CYCLE) DIG [K-OFF] INPUT	(SECOND KEY CYCLE) DIG [K-ON] INPUT
1	00 0011	00 0011
2	11 1100	11 1100

REMARKS:

FREQUENCY: (MHZ)

(DATE)
 (TIME)

EVENT	DIG [K-OFF] INPUT	DIG [K-ON] INPUT
1	00 0011	00 0011
2	11 1100	11 1100

REMARKS:

FREQUENCY: (MHZ)

(DATE)
 (TIME)

EVENT	DIG [K-OFF] INPUT	DIG [K-ON] INPUT
1	00 0011	00 0011
2	11 1100	11 1100

REMARKS:

ENDING TAPE RECORDER FOOTAGE FOR THIS SET OF DATA: (FOOT)

Figure 1-4. RFI Keying Test Data Sheet

ATTACHMENT A
FIELD CONNECTIONS AND SIMULATION

This attachment contains the following figures:

- o Figure A-1 Control Computer(s)/Test Station Connections

See test procedure JPD-111687-0 figures B-4 through B-9 for input simulation and input/output monitoring connections.

Cabinet Configuration Information:

The cabinet under test, Qualification Unit 2, is an exact replica of Watts Bar Nuclear Power Station Protection Rack 13. The following drawings document the cabinet configuration. Copies of these drawings will be included as part of the final test report.

<u>Drawing Description</u>	<u>Drawing Number/Rev.</u>
Terminal Block Wiring Diagram, Protection Set 4	1-47043 PW-13, rev. 3E
Process Control Block Diagram, Delta T/T _{AVG} System	108D408 sh. 10, rev. 11
Process Control Block Diagram, W.R. S.G. Level	108D408 sh. 34, rev. 8
Process Control Block Diagram, Pressurizer Liquid/Vapor Temp.	108D408 sh. 38, rev. 4
Process Control Block Diagram, RHR Pump Discharge Temp	108D408 sh. 39, rev. 5

Process Control Block Diagram,
RCS Wide Range Pressure

108D408 sh. 43, rev. 1

Eagle-21 Schematic Diagrams,
Rack 13 Protection Set 4

1856E69 sh. 2, rev. 2

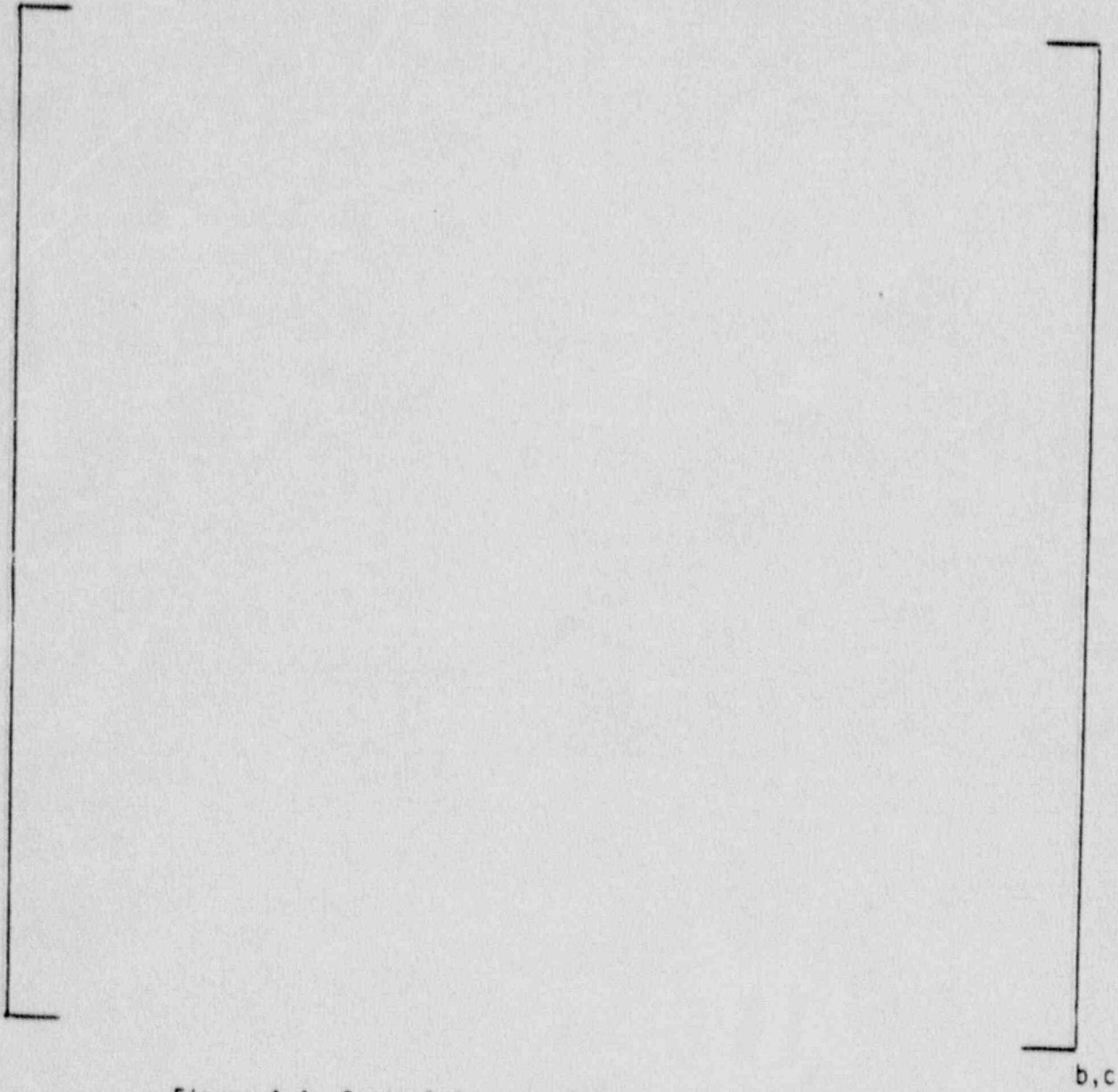


Figure A-1 Control Computer(s)/Test Station Connections

ATTACHMENT B
TRANSIENT DATA RECORDING SYSTEM CONNECTIONS

This attachment contains the following:

- o Table B-1 Tape Recorded Data
- o Table B-2 Data Logger Recorded Data
- o Table B-3 Strip Chart Recorded Data

TABLE B-1
TAPE RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer Amplifier Gain
				Hi	Lo	Sh	
1.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
2.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
3.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
4.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
5.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
6.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
7.	Contact Output	ITY/441	13-M	5	6		.02
8.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
9.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
10.	Analog Input I/E	IPY/458Q	*				10
11.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
12.	Analog Input I/E	IPY/408	*				20
13.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
14.	Function Generator Sig.	N/A	**				.05

*Measure current across 20 ohm transmitter test resistor. See figure B-4.

**Monitor function generator output signal. See figure B-3.

TABLE B-2
DATA LOGGER RECORDED DATA

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection		
				Hi	Lo	Sh
6.	Analog Input E/E	INY/441B	13-C	1	2	3
7.	Analog Input E/E	INY/441A	13-C	4	5	6
9.	Contact Output	ITY/441	13-M	5	6	
10.	Contact Output	ITY/441A	13-M	7	8	
22.	Analog Output E/I	ITY/441L	13-P	10	11	12
23.	Analog Output E/I	ITY/454A	13-G	4	5	6
24.	Analog Output E/I	ITY/441K	13-P	7	8	9
25.	Analog Output E/I	ILY/502B	13-K	1	4	5
26.	Analog Output E/I	IPY/408B	13-N	7	8	11
27.	Analog Output E/I	ILY/503B	13-K	7	10	11
35	Analog Input I/E	IPY/458Q	*			
36	Analog Input I/E	ILY/502	*			
37	Analog Input I/E	ILY/503	*			
38	Analog Input I/E	IPY/408	*			

*Measure current across 20 ohm transmitter test resistor. See figure B-4.

TABLE B-3
STRIP CHART RECORDED

Channel #	Recorded Signal	Tag #	Terminal Block	Terminal Connection			Buffer*** Amplifier Gain
				Hi	Lo	Sh	
1.	Function Generator Sig.	N/A	**				.05
2.	Bistable Partial Trip	ITS/442D	13M	3	4		.05
3.	Bistable Partial Trip	ITS/442G	13-M	1	2		.05
4.	Bistable Partial Trip	ITS/441C	13-L	1	2		.05
5.	Bistable Partial Trip	ITS/441D	13-L	3	4		.05
6.	Bistable Partial Trip	ITS/441H	13-L	7	8		.05
7.	Bistable Partial Trip	ITS/441G	13-L	5	6		.05
8.	Analog Input E/E	INY/441B	13-C	1	2	3	2.0
8a.	Keying Signal	N/A	****				.05
9.	Contact Output	ITY/441	13-M	5	6		.02
10.	Analog Output E/I	ITY/454A	13-G	4	5	6	10
11.	Analog Output E/I	ITY/441L	13-K	7	10	11	10
12.	Analog Input I/E	IPY/458Q	*				10
13.	Analog Output E/I	ITY/441K	13-K	1	4	5	10
14.	Analog Input I/E	IPY/40B	*				20
15.	Analog Output E/I	IPY/408B	13-N	7	8	9	10
16.	Analog Input E/E	INY/441A	13-C	4	5	6	2.0

* Measure current across 20 ohm transmitter test resistor. See figure B-4.

** Monitor function generator output signal. See figure B-3.

*** Adjust buffer amplifier and/or strip chart recorder bias controls to obtain approximately mid-scale readings for analog input/output signals and full swing for digital output signal 0 to 1 transition.

**** Monitor analog input INY/441B for modulation tests. Monitor control signal to keying relay for keying tests.

APPENDIX D
TEST EQUIPMENT LIST

Table D-1 describes the test equipment.

TABLE D-1
TEST EQUIPMENT LIST

--

b,c

TABLE D-1
TEST EQUIPMENT LIST

b,c

TABLE D-1
TEST EQUIPMENT LIST

--

b,c

TABLE D-1
TEST EQUIPMENT LIST

--

20



b, c