ILLINOIS POWER COMPANY

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500 SOUTH 27TH STREET, DECATUR, ILLINOIS 62525

December 14, 1981

Mr. James R. Miller, Chief
Standardization & Special Projects Branch
Division of Licensing
Office of Nuclear Reactor Regulation
U. S. Nuclear Regulatory Commission
Washington, D. C. 20555

Dear Mr. Miller:

Clinton Power Station Unit 1
Docket No. 50-461

The attached material is being provided as we agreed on December 11, 1981 with Rick Kendall. This response was found to be satisfactory and closes this item which had been identified as confirmatory from previous NRC review of CPS FSAR Chapter 7.

Sincerely,

J. D. Geier
Manager
Nuclear Station Engineering

JPO/lt

Attachments

cc: J. H. Williams, NRC Clinton Project Manager
H. H. Livermore, NRC Resident Inspector
R. Kendall, NRC ICSB

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The basic elements of the decision making logic of the NSPS are standard MIL grade CMOS logic elements, in dual in-line epoxy packages, mounted on multilayer printed circuit cards.

CMOS logic was chosen for the NSPS application because of its high noise immunity compared to other types of solid state devices. With the CMOS devices powered by 12 vdc, it takes an input greater than approximately 4 volts to switch the output on a low to high transition, and less than approximately 8 volts to switch on a high to low transition. Thus, noise spikes of considerable magnitude can be tolerated on the input lines without causing erroneous logic states. As a comparison, TTL logic which must be operated at +5V has a low to high minimum threshold of approximately .7 volt.

Numerous design techniques have been utilized to reduce the possibility of any significant electrical noise being coupled into the logic circuitry. All inputs and outputs that leave the NSPS cabinets are buffered and isolated, and internal wiring is routed to prevent "crosstalk" or radiated electromagnetic interference.

Specifically, prevention of electromagnetic conducted interference is accomplished in the following ways.

Power Lines: Conduction of EMI via power lines to the logic elements is prevented by the use of switching power supplies which are specified by the manufacturer to have a maximum noise spike of 62 mv. In addition, each logic card has single pole filters on the power input to remove any remaining high frequency noise.

Input signal lines: Inputs from other separation divisions, and from nondivisional sources are processed through optical isolators which are also filtered on the input side. Inputs from same-division sources such as the control room panels or field sources are processed through Digital Signal Conditioners (DSC's) which are filtered and optically coupled. Inputs to trip units are current loops and therefore not vulnerable to EMI.

Output signal lines: Outputs to actuated devices pass through load drivers which have pulse transformer coupling between input and output stages. Outputs to other logic elements in other divisions pass through optical isolators.

Internal wiring: Interconnections between logic cards is on a backplane of wire wrapped terminals. The connections are made point to point so that groups of wires do not run in parallel for long distances. Power wiring is routed as far from signal wiring as possible. The high current wiring of the drives to the pilot valve solenoids is run in conduit, as is the wiring for utility services (lighting).

Card layout: All signal inputs at the card level are buffered by a 100 K ohm resistor. The use of ground planes over large areas of the boards also insures electrically quiet circuitry.

All standards of good practice were applied during the design and construction of the solid state safety system to prevent any problem with EMI.