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Power Regulator for Direct Heating of Material with Inverse Resistance-Temperature Properties

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HIGHLIGHTS

An ac power regulator was designed for loads with inverse resistance-temperature properties. It is equipped with an integrated-circuit, analog multiplier for power computation. Its output power accuracy, achieved by automatic zero correction of the multiplier drift, is ±1% full scale over a range from 0 to 4 kW. Power is controlled by symmetrical phase firing of inverse-parallel SCRs; series inductance maintains loop stability when the load resistance is very low, reduces the current waveform crest factor, lowers the harmonic power content, inherently limits the load current, reduces the di/dt, and practically eliminates the rf noise often generated by phase-fired equipment. This report describes the design details for the current feedback, multiplier, error integrator, conduction angle control, and SCR firing circuits.

CONTENTS

1. INTRODUCTION

Direct electrical heating of material with a negative temperature coefficient is possible with a power supply that provides a controlled current or a controlled power output. In many applications, especially those that involve materials research, power control and regulation is preferred because power density is an explicit thermodynamic parameter, whereas current density is not. In the past, the implementation of power regulators was discouraged by the unavailability of electronic multipliers with acceptable performance at reasonable cost. In recent years, this situation changed as modular and monolithic, integrated-circuit analog multipliers became available that are suitable for ac or dc power controllers. With these devices for power computation, a regulated power system need be no more elaborate or expensive than a regulated voltage or current system of comparable size.

A power regulator was designed to deliver a full-range load power of 4 kW av from a single-phase, 120-V, 60-Hz source, using symmetrical conduction angle control (phase firing) of inverse-parallel SCRs. This configuration is versatile and performs well at less cost for the power circuit components when compared to a dc output system. Its transient response approaches one or two cycles, and its output can be transformer coupled if the load requirements do not match the available feeder circuit capabilities.

In addition to simplicity, the single phase ac circuit with symmetrical conduction angle control provides the unique advantage of having zero-output intervals occurring periodically at twice the source voltage frequency (assuming the maximum conduction angle in each direction is

limited to less than 180°). During these zero-power intervals, automatic offset correction techniques are applied to reduce the average power output error associated with zero shifts in the analog multiplier circuit.[1] With this technique, the ac regulator performance can equal or exceed a comparable dc unit in terms of steady state accuracy of the averaged output.

Whether one employs ac or dc, the regulation of power in loads having an inverse resistivity-temperature characteristic can present special closed-loop stability problems. This is especially true when the load is a semiconducting material with a very large temperature coefficient. For example, the resistivity of uranium dioxide, which is the material for which the apparatus described here was developed,[2-4] decreases almost five decades between room temperature and the melting temperature.[5] With this type of load, the small-signal gain of a power control loop can increase from a relatively low value when power is first applied to a very high value after the load reaches temperature. Instability can occur at either extreme.

For a simple controller with a fixed source voltage and with no series element other than the SCRs and resistive load, a low load resistance means a high loop gain, which can lead to instability because of a shrinking phase margin and a violation of the Nyquist criterion. This type of high-gain instability, which can occur in many types of ac controllers incorporating conduction angle control, has been the subject of several investigations using various circuit models and analysis techniques.[6-12] Generally such a system becomes unstable if the closed-loop damping time constant is less than one-half the sampling period.[8]

Possibly this type of instability was responsible for the high-temperature runaway reported by Wrona et al.[13]

At the other extreme, when the load is cooler, its resistance may be large, and the loop gain will be low if the source voltage is fixed. At low gains, another type of instability can occur as a direct result of the inverse temperature-resistance and other thermodynamic properties of the load. Oscillating frequencies associated with this low-gain instability will generally be low (<1 Hz) and inversely related to the effective thermal time constant of the load.

To cover the broadest possible range of load resistance and to maintain loop stability, we added series inductance to the power circuit. This expedient effectively limits the loop gain when the load resistance is low and provides a number of other benefits, such as crest factor reduction of the load current waveform.

Always a nuisance, high crest factors can be particularly troublesome in constant power controllers because the rms load current must increase when the rms load voltage decreases. With conduction angle control and a purely resistive power circuit impedance, constant power to a decreasing load resistance requires a decrease of the conduction angle, even when the rms current must increase. This situation leads to high peak currents and crest factors which impose undue dynamic range requirements on the feedback and measurement circuitry — especially the analog multiplier.

The addition of inductance in series with the load circuit provides a simple, but effective remedy. With the inductance values shown, the power circuit in Fig. 1 behaves as a voltage source

when the load resistance is high and as a current source when the load resistance is low. This and other advantages for using series inductance in the power circuit with conduction angle control of load power are analyzed further in subsequent sections of this report.

2. DESIGN

2.1 Power Circuit

The power circuit and a diagram of the measurement and control functions are given in Fig. 1. For source power, a connection is usually made between one phase and the neutral of a 100-A (or larger), 120-V, three-phase, four-wire feeder system. The input current is supplied by four parallel branches; the current feedback signal for power computation and control is derived from only one branch. This arrangement permits the full-scale power calibration to be changed by closing the appropriate number of circuit breakers. Calibrations used are 1, 2, 3, and 4 kW full scale for one, two, three, or four circuits, respectively. The current splitting also minimizes the flux in the current transformer core, which permits the use of smaller cores. The current measurement circuit can handle up to 25 A rms (typically 50 A peak), which is equal to a maximum load current of 100 A rms if all input circuits are used. Equal splitting of the total load current among the active input circuits is maintained by a 6-mH inductor in each branch.

Controllers using phase firing for conduction angle control in mainly resistive power circuits often exhibit objectionable di/dt and radio-frequency noise generated at each instant of firing. This problem is virtually nonexistent for the circuit described here because the

series inductance inherently limits the di/dt to levels that are about the same as for purely sinusoidal load current waveforms.

The maximum conduction angles for the SCRs and load current are limited to about 135° to provide periodic intervals for automatic zero correction in the power measurement circuit. This limitation also aids in holding the SCRs "on" if the load resistance is high. The maximum power circuit voltage (total across load and inductance) with 135° conduction is about 95% of the input source voltage.

2.2 Current Feedback Circuit

A current transformer is used to develop the load current feedback signal because this method permits earth grounding at the source and/or load points. As indicated in Fig. 2, a total current reduction of 5000 is provided by cascaded transformer stages, each of which is hand wound on 36-mm-OD, toroidal ferrite cores. This two-stage arrangement is especially suitable for experimental and developmental work because the current ratio can be quickly altered by adjusting the second-stage primary turns.

A current-to-voltage conversion impedance of 1000 Ω is provided by the input stage (IC1) feedback resistor. Also, this stage improves the low-frequency response of the transformer by providing a very low input impedance. Since this stage has a very high (nearly open loop) dc gain, a low-drift amplifier is required for IC1.

Low-frequency components of the phase-fired load waveform that are attenuated by the current transformers are partially restored by IC2 acting as a simple pole-zero active filter. This technique extends the overall low-frequency response to below 1 Hz which is sufficient for good reproduction of the 60 Hz phase-fired waveform.

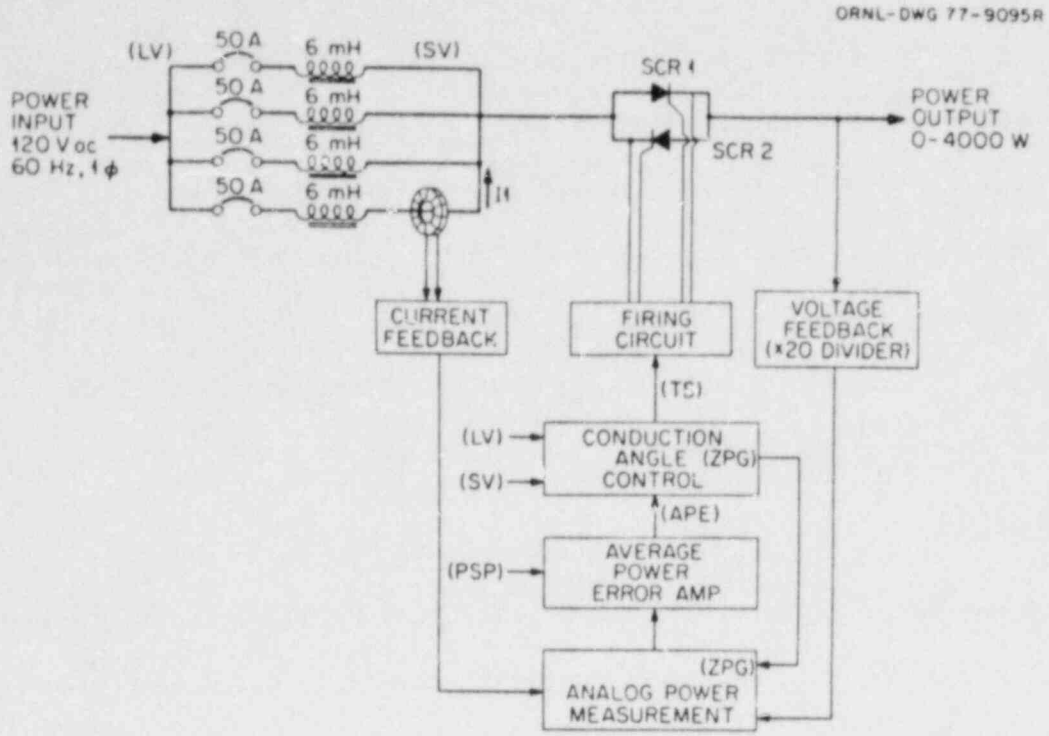


Fig. 1. General system diagram.

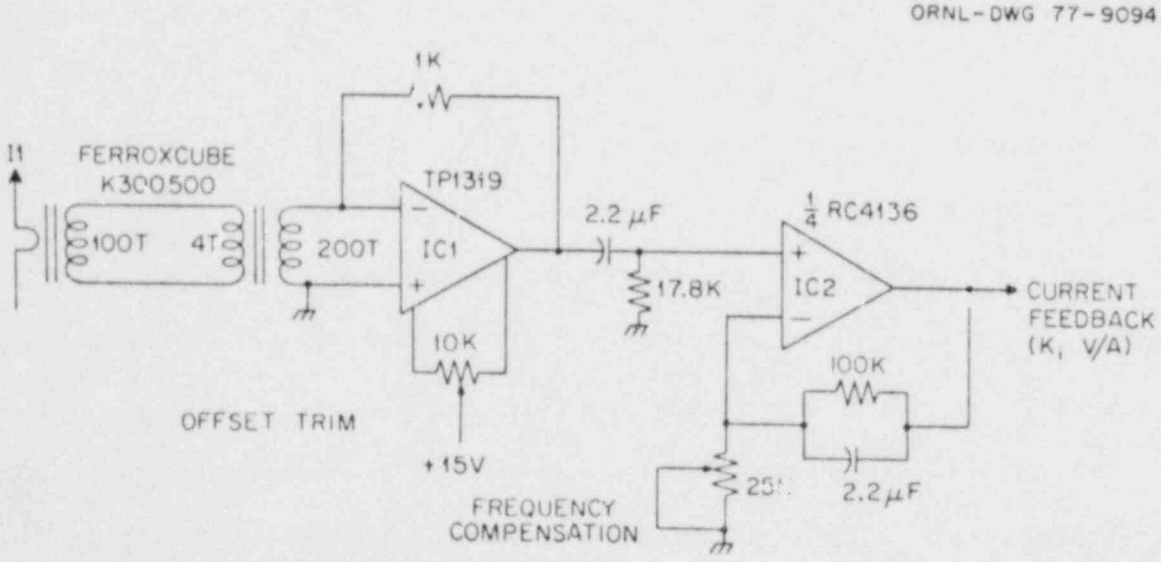


Fig. 2. Current feedback circuit.

2.3 Power Measurement Circuit

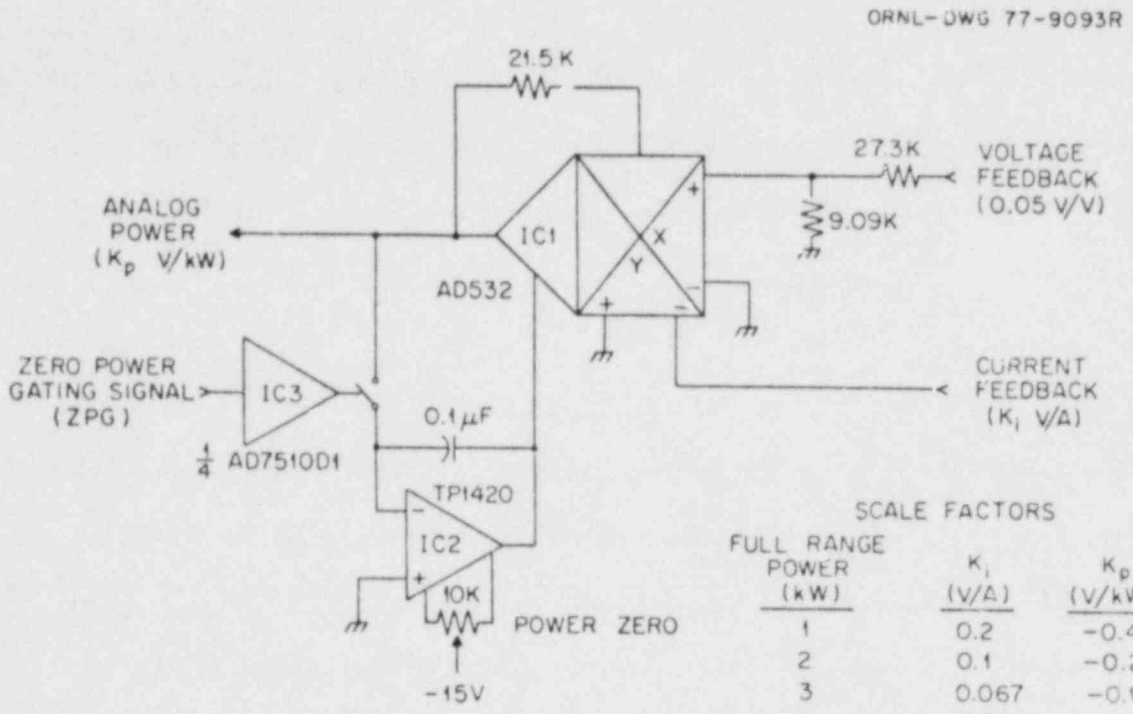
Load voltage (voltage across series inductance not included) and load current feedback signals are fed to an integrated circuit analog multiplier that produces the time domain load power signal. The dc component of this signal is directly proportional to the time averaged real load power in accordance with the scale factors given in Fig. 3. The multiplier is inverting, i.e., real load power gives a negative multiplier output.

Since the load in the authors' application is mainly resistive (the series inductance is not considered to be in the load), the average load power, Pav, and peak load power, Ppk, are related by

$$Ppk = (CF)^2 Pav \ , \tag{1}$$

where CF is the crest factor for the load current waveform. Load power will not be properly measured or regulated unless the peak amplitude of the multiplier signal is maintained below the nominal 12-V saturation level of the multiplier. As seen in Fig. 3, the multiplier output corresponding to full-range average power is 0.4 V. When this and the 12-V saturation level are combined with Eq. (1), the maximum crest factor for proper operation at 100% power is $\sqrt{30}$, or 5.5. This requirement would be difficult to meet without the smoothing effect and crest factor reduction contributed by the series inductance.

The maximum multiplier inputs referred to the load are 800 V (peak) and 200 A (peak), if all input branch circuits are used. The high-voltage rating was required to accommodate a separate power stage (not described



SCALE FACTORS

FULL RANGE POWER (kW)	K_i (V/A)	K_p (V/kW)
1	0.2	-0.4
2	0.1	-0.2
3	0.067	-0.133
4	0.05	-0.1

Fig. 3. Multiplier circuit.

in this paper) so that a 500 V ac source could be used and no scale factor switching would be required when the source is changed from 500 to 120 V ac.

The maximum SCR conduction angle is limited to 135°, i.e., a zero-power interval of at least 45° always follows the turn-off of each SCR. These periodic, zero-power intervals are unique with phase fired ac controllers, and represent a distinct advantage because they permit the employment of automatic zero-correction techniques for stabilizing key stages such as the multiplier used here.

With no external stabilization, the dc output drift of the multiplier is typically 0.7 mV/°C, or about 7 W/°C (for the 4-kW, full-scale range), which is totally inconsistent with an overall accuracy requirement of ±1% full scale. With automatic zero-correction implemented with IC2 and IC3, the effective multiplier drift stability is equal to the stability of IC2, which is more than 200 times better than the stability of the multiplier alone.

Zero correction is achieved by sampling the multiplier output via a CMOS analog switch (IC3 in Fig. 3) which is gated "on" during each zero-power interval by a 2.1-msec pulse that is generated by the conduction angle control circuit. During sampling, the multiplier output is compared with zero by IC2, which drives the AD532, offset-adjust terminal to achieve a zero balance. Between samples, the zero balance is maintained by storage on the IC2 feedback capacitor.

2.4 Average Power Error Amplifier

The time domain power signal generated by the analog multiplier is compared to a dc level that represents setpoint power by converting each signal to a current and integrating the difference with a common operational amplifier designated as IC1 in Fig. 4. The polarities are such that the integrator output, APE, becomes positive when the measured power exceeds the setpoint power. In normal operation, the APE signal is between 0 and +10 V dc, with the latter corresponding to zero SCR conduction.

Integrator on/off characteristics are controlled by the CMOS logic input PSP, which is high for "stop power" and low for "start." Instant turn-off when PSP goes high is ensured by D2 in Fig. 4 which clamps APE to the CMOS logic high level. A high PSP signal also closes CMOS switch IC3, and causes the integrating capacitor to assume a charge state of +15 V dc, which is 5 V beyond the SCR cutoff level. Thus, when PSP goes low to start power flow, the APE signal must decrease from an initial high level at a rate determined by the integrating capacitor and the integrator input current.

Diode D1 (Fig. 4) clamps the integrator output at -0.6 V dc and reduces the time required for the loop to recover from a maximum conduction condition which occurs when the load power is voltage or current limited.

2.5 Conduction Angle Control

Proper conduction angles for the power SCRs are generated by a logic control circuit (Fig. 5) that produces a trigger signal for the SCR firing circuits. The main output of this circuit is a 60-Hz square

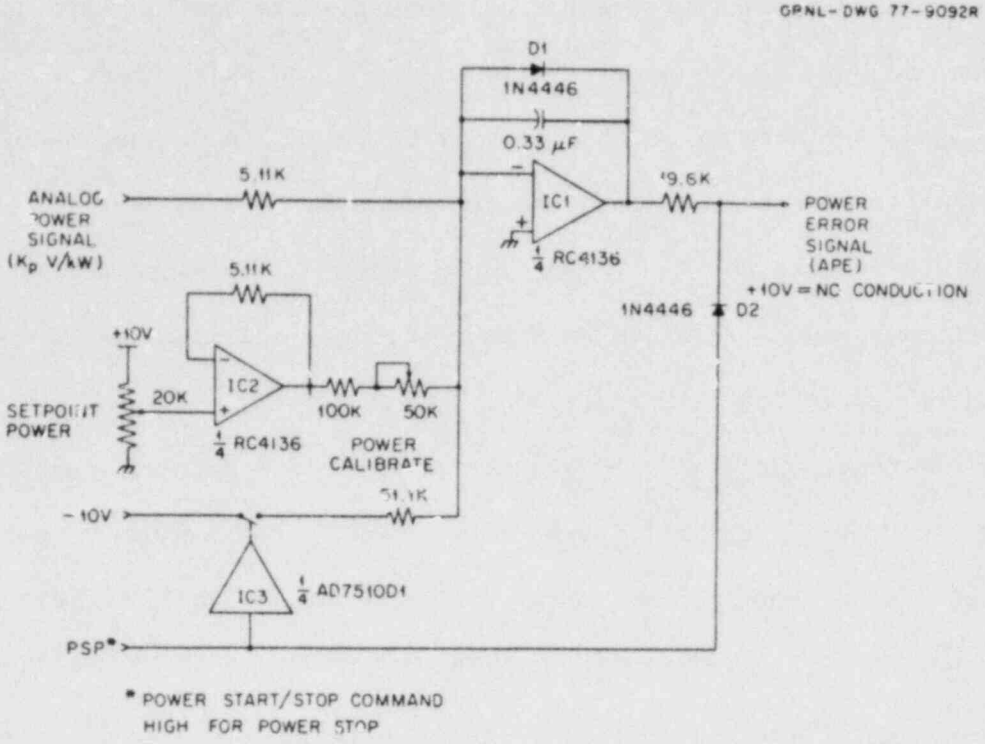


Fig. 4. Error amplifier circuit.

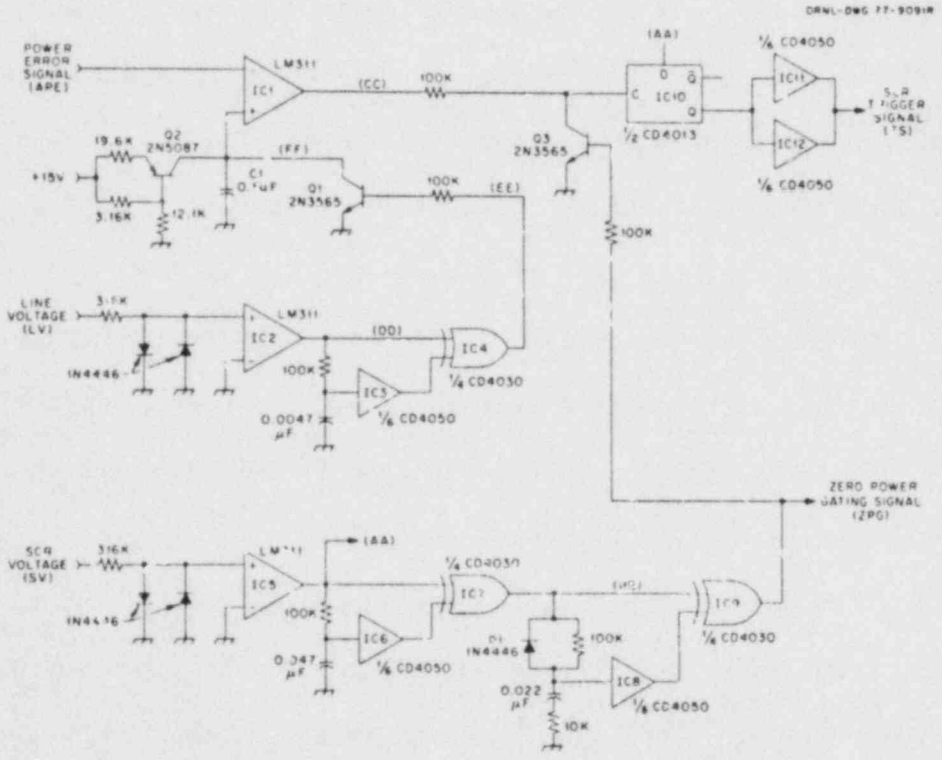


Fig. 5. Conduction angle control circuit.

wave (TS) which ultimately triggers SCR1 (see Fig. 1) on its positive transition and SCR2 on its negative transition. The phase of this trigger signal defines the phase of the load current and always lags the phase of the source voltage; more lag produces less conduction (and therefore less power) for a given load condition. This phase lag of the SCR trigger signal relative to source voltage is designated as the firing angle, α, in the literature.[14]

The two most popular firing schemes are the inverse cosine and the constant-α scheme.[7] The latter scheme was used by the authors primarily because of its ease of implementation and also because the inverse-cosine approach has no particular merit unless load voltage is the controlled parameter. When the power supply is regulating, the firing angle will change proportionately from 180 to 0°, and the conduction angle will increase from 0 to 135° max as the average power error signal, APE, decreases from +10 to -0 V dc. In Fig. 5, this control is implemented by a comparator (IC1) which makes a positive transition each time a sawtooth time base, FF, crosses the APE input level (illustrated by a typical timing diagram, Fig. 6). The 120-Hz, 0- to 10-V sawtooth is produced by Q2 as it charges C1, and is reset by Q1 which is pulsed on for 0.3 msec each time the source voltage crosses zero. The positive transitions produced by IC1 serve as clock pulses for flip-flop IC10, which in turn produces the square-wave SCR trigger signal, TS.

If APE is greater than +10 V, the output of IC1 is low, and there are no clock transitions; therefore, no firing pulses are generated, i.e., no power flows to the load. This condition prevails after the control electronics are energized and until the PSP logic input to Fig. 4 is brought low to initiate power flow (firing). To initiate firing, the

PSP input is forced low, allowing the APE signal to decrease from the +15-V clamp position at a rate dependent on the setpoint power, as previously described. As APE passes below +10 V, SCR firing commences, and the conduction angle increases from zero until the measured and setpoint powers balance. This arrangement ensures a smooth buildup of load power, and is often called "soft starting."

The maximum conduction angle for each SCR is limited to 135° by saturation of Q3 which clamps the flip-flop clock for a period of 2.1 msec immediately after each SCR turns off. This clamping pulse is generated by cascaded, exclusive or one-shots (IC7 and IC9), which are triggered from a square-wave signal synchronized in phase with SCR turn off. This signal, AA, is generated by IC5; it is derived from the SCR voltage (labeled SV in Fig. 1).

Voltage SV follows the load voltage when either SCR is conducting; it follows the line voltage when both SCRs are off. Thus, because of the phase lag between load voltage (current) and line voltage, SV must sharply change polarity at the turn off time of each SCR (illustrated by a timing diagram, Fig. 7). These transitions are accurately discerned by IC5 acting as a simple zero-crossing detector.

Although the CMOS exclusive OR gate with an RC delay and buffer in one input makes a convenient one-shot, it is slightly asymmetric (i.e., the widths of successive pulses are not equal) because hysteresis is inherent with the input characteristics of CMOS gates. To ensure good load waveform symmetry, the off times for both SCRs must be equal, which means that the widths of all gating pulses applied to Q3 must be equal. To accomplish this with CMOS gates, cascaded one-shots are used. The

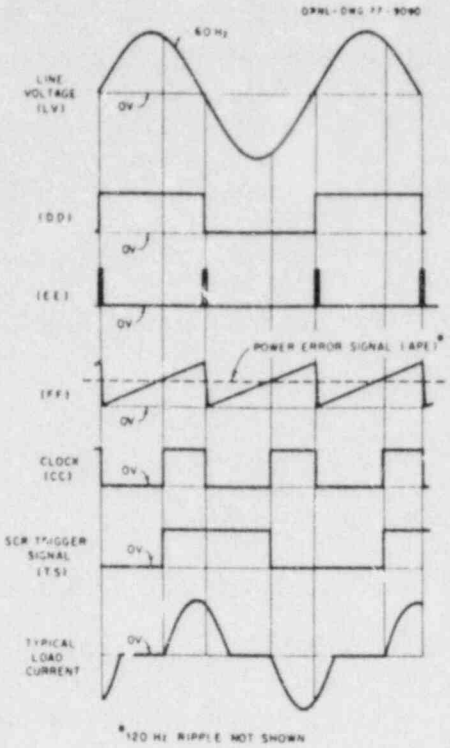


Fig. 6. Timing diagram for proportional control.

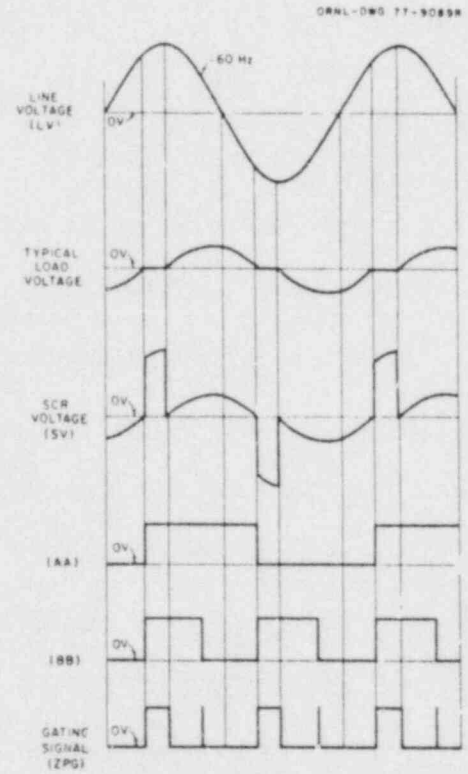


Fig. 7. Timing diagram for maximum conduction operation.

first (IC7) is timed for about 4 msec, and essentially serves to double the output frequency of IC5. This results in a square wave, BB, which makes a positive transition when either SCR turns off. When applied to the second one-shot (IC9), these transitions produce the 2.1-msec pulses required for clamping Q3. At the negative transitions, the second one-shot produces only a narrow spike because of the rectifying action of D1. These spikes are of no consequence in clocking IC10, because they occur before the flip-flop, D input transition.

These 2.1-msec pulses, ZPC, also serve as gating pulses for the automatic, multi lier zero circuit previously described.

An exclusive OR one-shot (IC4) is also used to reset the 120-Hz sawtooth time base, FF. In this application, the asymmetry is tolerable because the pulse width (0.3 msec) is small compared with the total period.

2.6 SCR Firing Circuits

Firing pulses for the main SCRs (SCR1 and SCR2, Fig. 1) are generated by half-wave rectifier circuits (Fig. 8). Energy to fire SCR1 during positive line voltage is supplied by C1, which is charged to about 170 V dc during the preceding negative half-cycle of line voltage. Similarly, energy to fire SCR2 during negative line voltage is supplied by C2, which is charged during the preceding positive half-cycle. With this arrangement, adequate firing energy for SCR1 is being stored while SCR2 is conducting, and vice versa.

Capacitors C1 and C2 are discharged by alternate firing of smaller SCRs (type 2N4172), which are triggered by a differentiated version of

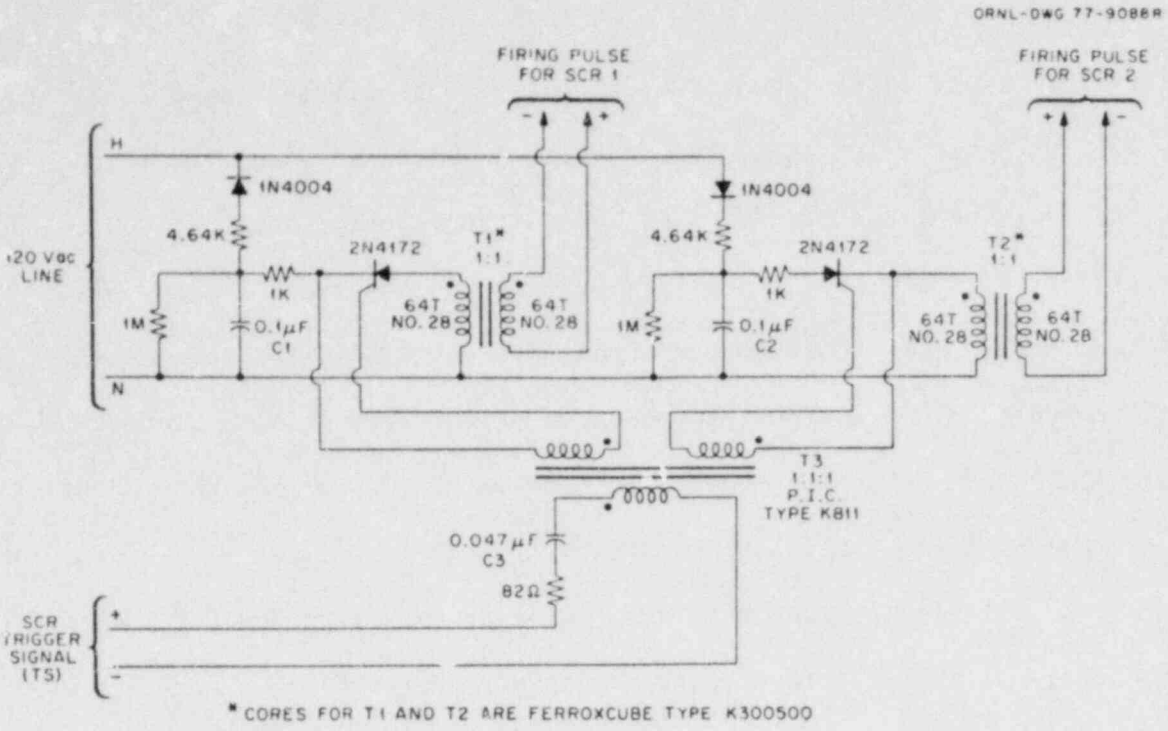


Fig. 8. Firing circuit.

trigger signal TS (see Fig. 6) via pulse transformer T3. Positive and negative transitions of TS initiate the discharge of C1 and C2, respectively.

Control of power for the 120-V ac firing circuit provides a convenient and reliable method of interlocking the regulator for safety purposes.

3. DISCUSSION

3.1 Accuracy and Rangeability

When operated within a calibrated power range,* the output power error is less than ±1% of full scale at any power setpoint, and less

* Only one of the four selectable power ranges can be calibrated accurately. Accuracy of the other three depends on inductor matching, which is ±10%.

than ±2% of the reading for setpoints between 10 and 100% of full scale. This accuracy is maintained over a reasonable temperature range (15 to 35°C) by automatic zero correction of the multiplier output offset, as already described.

To use zero-correction techniques, we restrict the conduction angle to 135°, which obviously requires some sacrifice in maximum power output and load rangeability--especially on the low resistance end. As illustrated by the curves in Fig. 9, the load resistance to which full power (4 kW) can be delivered ranges from about 0.45 to 2.5 Ω with the 135° limit, whereas the range would be 0.1 to 3.5 Ω with full 180° conduction.

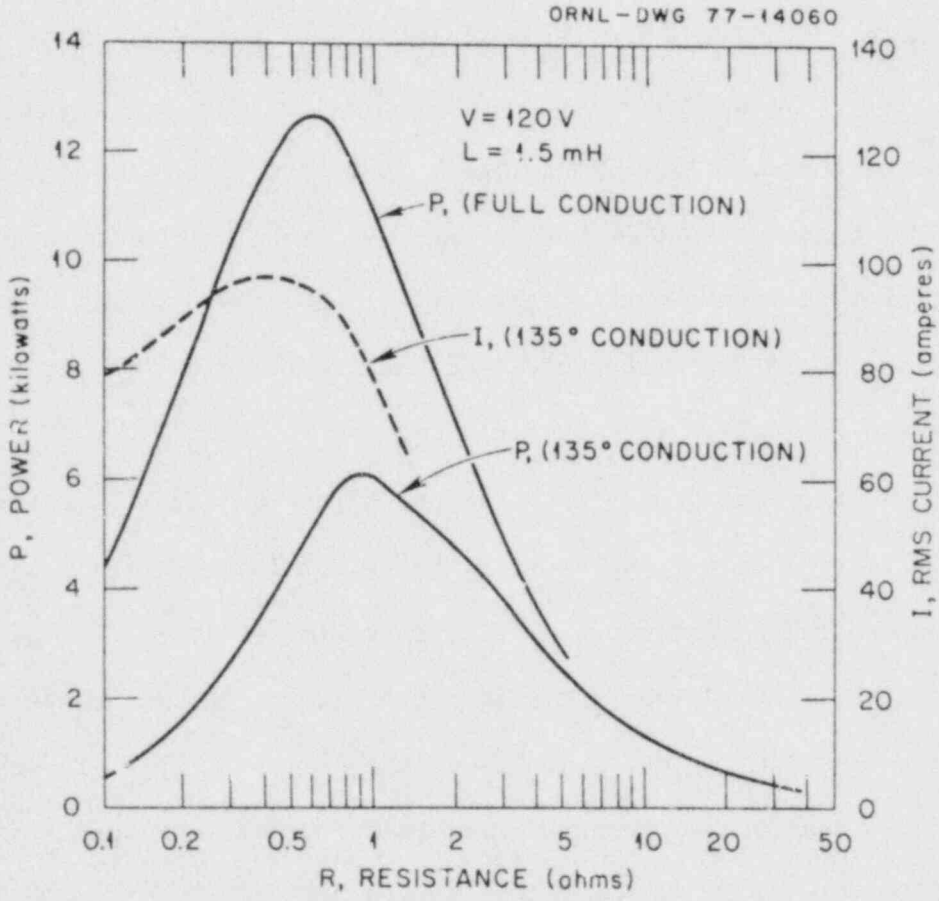


Fig. 9. Power regulator output characteristics.

Another curve in Fig. 9 illustrates how the current for 135° conduction is inherently limited to slightly under 100 A rms, which is well within the SCR capabilities. Both the current and power curves in Fig. 9 were obtained by interpolation of the data given by Khalifa et al.,[14] using the simplifying approximation that

$$\alpha = \phi + 45° \ , \tag{2}$$

where α is the firing angle, and ϕ is the 60-Hz impedance phase angle of the power circuit. The series inductance is 1.5 mH, and the source voltage is 120 V.

When constant power is used for direct heating of a load with inverse resistivity-temperature properties, the load resistance characteristically decreases monotonically as the temperature rises. For $\phi = 0$, this load resistance characteristic requires a monotonically decreasing conduction angle and, therefore, a higher and higher current waveform crest factor if power is constant. As previously mentioned, this circumstance is completely avoided when the power circuit is inductive, in which case the conduction angle first decreases and then increases as the load resistance monotonically decreases from high to low values.

In terms of dynamic range requirements of the multiplier, the most desirable situation is for the crest factor to be low when the regulator output approaches full-scale power. The inductive power circuit is very effective in this regard when the load resistance is low and near-maximum conduction is required to supply full-scale power. The typical, maximum-conduction, current waveform has a crest factor of <2 and appears as shown in Fig. 10.

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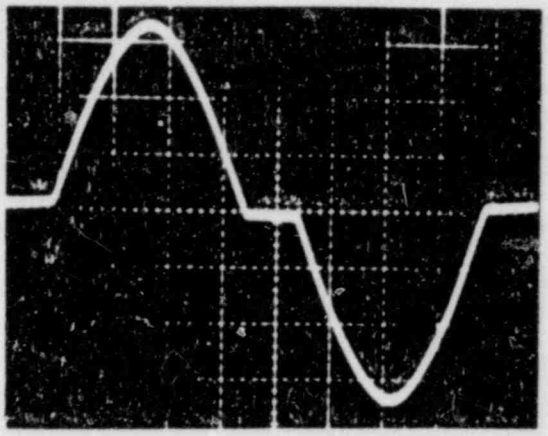

Fig. 10. Typical maximum (135°) conduction current waveform.

Still another advantage of the inductive power circuit is the reduction in harmonic power content. For the same source voltage and real-load power, the inductive circuit generally shows a lower harmonic contribution than the $\phi = 0$ case. Consider, for example, a typical situation where $\phi = 0$ and the total per unit rms current is 0.35. The required conduction angle for this case would be 52°, and harmonics would contribute about 60% of the total power.[14] If, on the other hand, inductance is added to increase ϕ to 57.6°, a longer conduction angle is required to supply the same power, and the harmonic power content is reduced from 60 to <10%. This aids in minimizing core losses in the feeder source transformer, and in the load coupling transformer if one is required.

3.2 Closed-Loop Response Time

Reasonable approximations for the closed-loop response time and predictions of frequency stability are possible by analysis of small-signal behavior in the neighborhood of a quiescent operating state. With an assumption that IC1 in Fig. 4 is ideal (infinite forward gain and input impedance), the time constant of small-signal, closed-loop response can be expressed by

$$\tau = [A_{o1}]^{-1} = [1.07|\partial P/\partial\alpha|]^{-1} , \qquad (3)$$

where A_{o1} is the small-signal loop gain at a frequency of 1 radian/sec. The 1.07 factor represents the aggregate 1 radian/sec gain for the multiplier, integrator, and conduction angle control circuits. The $\partial P/\partial\alpha$ factor is the dc power circuit gain, i.e., the load power response to a small change in the SCR firing angle. Equation (3) includes neither the low-frequency effects associated with load thermodynamics nor the high-frequency effects associated with the sampling nature of phase-fired regulators.

The phase shift introduced by the sampling effect becomes significant at frequencies approaching the sampling frequency, and the loop becomes unstable if the response time in Eq. (3) is shorter than about 4.2 msec (1/2 the sampling period).[8] The shortest time constant and greatest tendency for instability arise when the loop gain and $\partial P/\partial\alpha$ are maximum.

These maxima can be estimated by expressing the small-signal power circuit gain as

$$\partial P/\partial\alpha = 2V \cos\phi \, (P/R)^{1/2} \, \partial f/\partial\alpha , \qquad (4)$$

where V is the source voltage; P, load power; R, load resistance; ϕ, 60-Hz power circuit, impedance phase angle; α, firing angle; and f, per unit rms load current. The latter factor is defined by

$$I = f\ V\ (R)^{-1}\ \cos\phi\ . \tag{5}$$

Since $\partial f/\partial\alpha$ is not a strong function of ϕ or α, the maximum $\partial P/\partial\alpha$ must nearly coincide with the maximum for $\cos\phi\ (P/R)^{1/2}$. This occurs at $\phi = 45°$ and P = 4 kW, which in conjunction with V = 120 V and $\partial f/\partial\alpha \cong -0.008\ \text{deg}^{-1}$ (ref. 14), results in

$$\left|\partial P/\partial\alpha\right|_{max} \cong 114 \tag{6}$$

and

$$\tau_{min} \cong 8.2\ \text{msec} \tag{7}$$

for the minimum closed-loop response time.

The response should be slower for other operating conditions, such as for lower load power or for $R \neq \omega L$. One example is given in Fig. 11, which is the current response for a 0- to 500-W step change in setpoint and a 0.25-Ω load.

In practice, the power regulator has been used mainly to heat stacks of 5-mm-OD UO_2 pellets with various total lengths from 40 to about 100 mm. These loads are initially heated with at least two other high-voltage power supply stages to achieve surface temperatures of about 1000 K and a load resistance in a range from 10 to 50 Ω. The regulator described here is utilized to insert powers of 200 to 300 W/cm length, which is

surficient to achieve significant center melting (~3100 K) of the UO_2 pellets within about 30 sec. During this insertion, the load resistance typically decreases to 0.2 to 0.5 Ω.

When the load resistance is relatively high, we have observed two types of unstable behavior. By far, the more common of the two is for the load to completely "drop-out" because its power-resistance characteristic falls beyond the maximum power curve (135°) given in Fig. 9; i.e., the heat loss for a particular temperature-resistance state exceeds the maximum regulator output. This condition may exist when the regulator is first energized (the load temperature being previously elevated by other equipment), or it may be triggered by load restructuring or by a shift in heat transfer properties.

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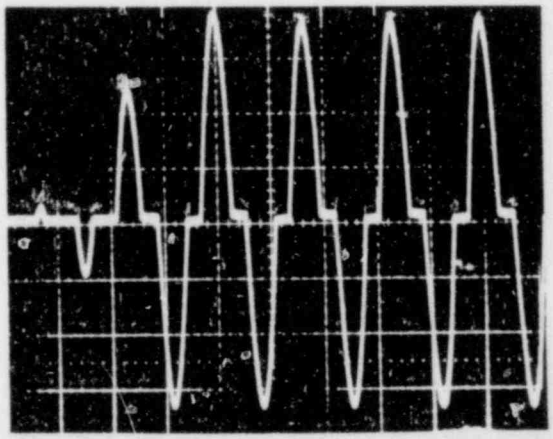

Fig. 11. Load current response for setpoint power stepped from 0 to 500 W and 0.25 Ω load resistance.

On a few occasions, when operating at high resistance ($R > 25\ \Omega$) and low power we have observed low-amplitude-limit cycle behavior. Under these conditions, the loop gain is very low (P/R and $\partial f/\partial \alpha$ are small) and the closed-loop response time is several seconds long. We suspect that this unstable mode is precipitated when the magnitudes of the loop response and load thermal response times are comparable. Although unwanted, this unstable mode is not destructive, because any excursion toward higher temperature is self-limiting; i.e., the unstable condition only applies when the gain is critically low.

Although the power regulator was developed specifically for heating materials with large negative coefficients of resistivity, it is equally suitable for constant power heating of loads with zero or positive coefficients. The latter are generally less demanding in terms of dynamic range and loop stability.

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