HF Controls

HFCONTROLS CONTROL SYSTEM

HFC-6000 FPGA Control System

VV0115

Test Specimen Design Description

VV901-300-10 Rev A

Effective Date 3 / 13 / 2017

Author: David Briner

Reviewer Jordan Mott

Approval Eugene O'Donnell

HF Controls

Revision History

Date	Revision	Author	Changes
03/13/2017	A	D. Briner	Initial Release

Table of Contents

Section 1.0

GENERAL INFORMATION

1.1 INTRODUCTION

This document provides a detailed description of the hardware components that make up a HFC-6000 FPGA control system for qualifying as a generic controller system for safety-related systems.

1.2 REFERENCES

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Application in Nuclear Power Plants, 1996
VV901-300-09	VV0115 Qualification Master Test Plan, Rev. A
RS901-000-01	HFC-6000 Product Line Specification, Rev. J
DS002-000-01	C-Link Protocol Design Spec Appendix 1 F-Link, Rev A
DS901-001-99	FPC08 G-Link Gateway Software Design Specification, Rev A
710060-01	VV0115 Seismic Rack Assembly, Rev. A
710061-01	VV0115 Power Distribution Panel Assembly, Rev A
710063-01	VV0115 Loop Layout FPGA EQ, Rev B
710064-01	VV0115 Wire List, Rev B
710065-01	VV0115 Cable Connection FPGA EQ, Rev D
710066-01	VV0115 Power Distribution Test Equipment Assembly, Rev D
710067-01	VV0115 Front/Rear Terminal Board Assembly, Rev B
710068-01	VV0115 Inside Center Right Terminal Board Assembly, Rev A
710069-01	VV0115 Inside Center Left Terminal Board Assembly, Rev B
500673-04	VV0115 Tie Bar Weldment TB Front Panel, Rev A
500674-20	VV0115 Front Panel Fabrication, Terminal Board, Rev A
TP901-115-06	VV0115 TSAP Validation Test Procedure, Rev A

1.3 ABBREVIATIONS AND ACRONYMS

BOE	Burst of Events
BOM	Bill of Materials
CON	Connector to cable card installed at rear of backplane I/O card slot
CRC	Cyclical Redundancy Check
DIP	Dual In-line Package
DSP	Digital Signal Processor
ELPC	Ethernet Low Pin Count
EWS	Engineering Workstation
FLINK	FPGA RS485 Communication Link
HAS	Historical Archiving System
HFC	HF Controls/Doosan HF Controls
HIFR	PC based HW/SW that captures dynamic data from the test set
HPAT	HFC Programmable Automated Tester
ICL	Intercommunication Link
I/O	Input/Output
LAN	Local Area Network
DGLS	Diesel Generator Load Sequencer
LED	Light Emitting Diode
MCL	Master Configuration List
MCRT	Microsoft CRT (Display) software
NRC	Nuclear Regulatory Commission
PCB	Printed Circuit Board
PROM	Programmable Read Only Memory
RACK	Same as “Chassis”
RIF	Redundancy Interface
RQ	Request Information
RTD	Resistance Temperature Detector
SOE	Sequence of Events
TC	Thermocouple
TSAP	Test System Application Program. A “synthetic application” used to check/verify the PLC functionality needed to support the qualification test program.
VGA	Video Graphics Array

Section 2.0

COMPONENT OVERVIEW

2.1 GENERAL

The FPGA system is configured using selected HFC-6000 components to create a fully functional control system complete with system software and a test system application program (TSAP). This control system constitutes the Test Specimen for EPRI TR 107330 qualification. The main components to be qualified include HFC-6000 controller PCBs, I/O PCBs, Gateway PCBs and power supplies. The core platform of this system is based on the HFC-6000 system which has been qualified through the ERD111 project. The core platform consists of 19" wide chassis for insertion of controller and I/O cards and bulk power supplies (24VDC). The FPGA system is updated with enhanced power-up diagnostics and, run-time diagnostics.

2.2 TEST SYSTEM HARDWARE CONFIGURATION

Figure 1 illustrates a condensed layout of the Test Specimen and indicates the boundary between the safety-related and non-safety-related portions of the system. Figure 2 illustrates the overall layout of the Test Specimen. Only the safety related portion of the system is subjected to the qualification tests described in the VV901-300-09 VV0115 Qualification Master Test Plan.

The Test Specimen is composed of two 19-inch card chassis with nearly identical controllers and I/O cards. The only differences between the two racks are:

[

]

The test system consists of three main parts. The first part (safety related) is two chassis(rack) which have two FCPU/FCPUX controller cards in each rack resulting in each rack containing redundant controllers. The 2nd part is a non-redundant controller located outside of the FPGA test frame in a third rack. This controller consists of a single HFC-FPC08 and set of older HFC-6000 DSP I/O cards that are used to simulate inputs into and read outputs from the FPGA test set. This third rack (simulator) is referred to as the HPAT. All 3 controllers communicate through the non-safety C-Link. The 3rd part consists of the EWS/MCRT/HIFR workstation which serves as an operator interface and data logging station.

The HFC-6000 FPGA test specimen hardware supports three serial communication links:

- F-Link is the redundant RS485 communication path between the FCPUX and the FPGA I/O cards. [

]

[ ], which may be located in the same chassis as the controller, an expander chassis, a local I/O chassis, or a combination of local and remote chassis. When configured to communicate with a remote I/O chassis, a redundant fiber-optic link serves as the communication medium to ensure electrical isolation from non-class 1E equipment.

- G-Link is the redundant RS485 communication path between the FCPUX's and the FPC08's residing in a single rack. [

]

- A redundant Communication Link (C-Link) provides the communication links with a gateway HFC-FPC08. The network is an Ethernet LAN that employs a deterministic, proprietary protocol that uses a "Master for Moment (MFM)" token passing method, to enable broadcast transfer from the controller to the PC workstations. The HFC-FPC08 prohibits direct communication from the PC EWS workstation to the FCPUX controller.

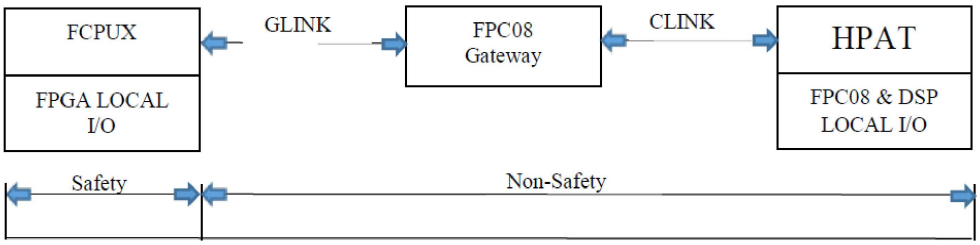

Figure 1 – Safety and Non-Safety Boundary

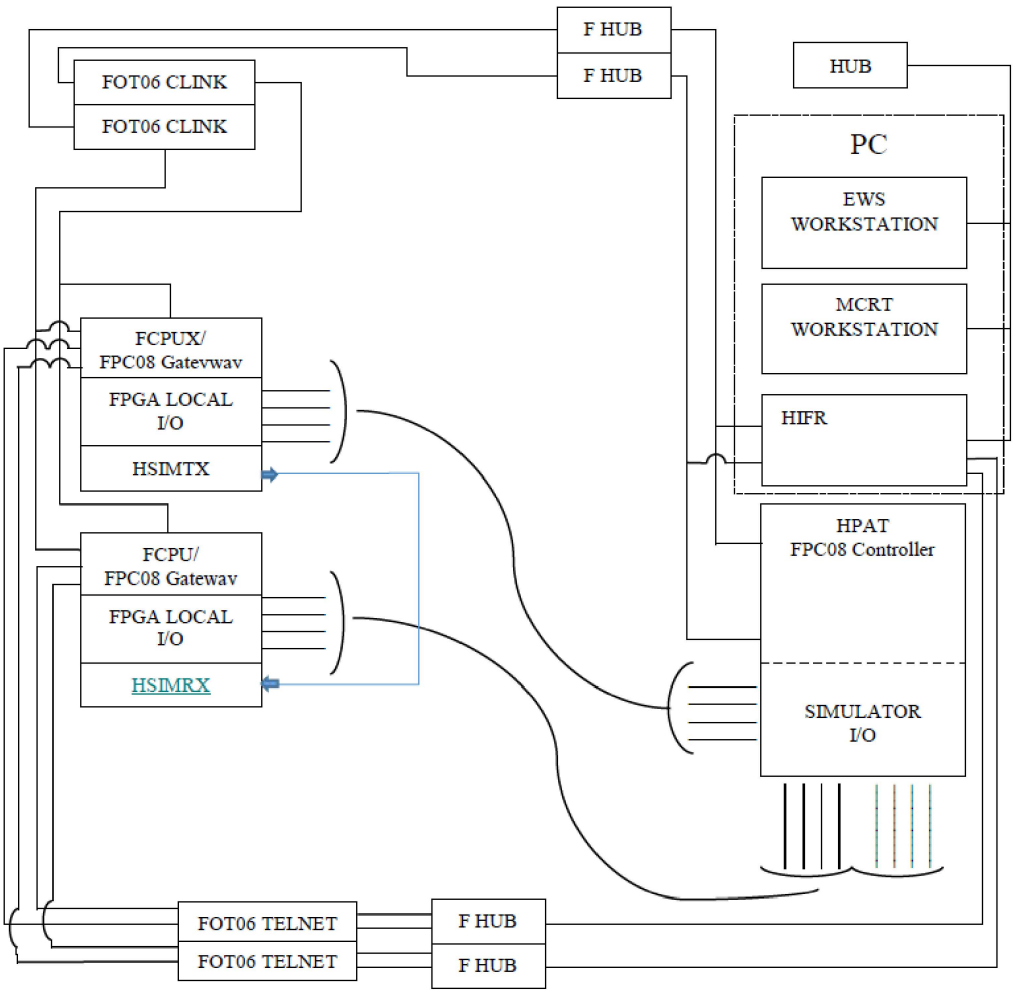

Figure 2 – TUV TMR Test Specimen System Arrangement

F HUB = Fiber to CAT5 Ethernet HUB

2.2.1 MODULAR CARD CHASSIS

The hardware is housed in modular card chassis with slots for 14 cards. Each modular card chassis is designed for installation in a standard 19-inch equipment cabinet to permit direct installation in existing cabinet assemblies. The controller racks 14 slots can be used for controller cards and I/O cards with no particular slot designated for any particular card type. [

] Two identical chassis are configured for this system but PCB's installed in these chassis differ. All backplane assemblies provide traces for the FLINK and power lines; connectors on the backplane provides the interface for connecting field I/O cable harnesses and power source cables. The arrangement of all card chassis is designed to facilitate routing of bundled signal wires from the interface with I/O cards designed to interface with termination card assemblies. Power distribution and fusing are integral to each chassis, and a retrofit installation can be accomplished by mounting the chassis in an

existing cabinet, connecting the power supply to the facility AC power source, and routing the I/O wires to the appropriate field terminals.

2.2.2 HARDWARE COMPONENTS

The HFC-6000 FPGA hardware components to be qualified in the test specimen are listed in Table 1. See Section 5.0 for a complete master configuration list.

Table 1 – HFC-6000 FPGA System Qualifying Components

Designation	Function
HFC-FCPU	Master Controller (see paragraph below)
HFC-FCPUX	Master Controller (see paragraph below)
HFC-FPUA	16-Point Analog Input Card (4 to 20mA)
HFC-FPUM	8-Point 3-Wire RTD Input Card, 100-ohm Platinum (see paragraph below)
HFC-FPUM2	8-Point 3-Wire RTD Input Card, 100-ohm Platinum (see paragraph below)
HFC-FPUL	8-Point E-Type Thermocouple Input Card 0-500 deg C
HFC-FPUAO	8-Point Analog Output Card (4 to 20 mA)
HFC-FPUD02	32-Point Discrete Input Card (48VDC input)
HFC-FPUD01	16-Point Form C Relay Outputs + 16-Point Discrete Inputs
HFC-FPC08	Communication Gateway Controller with VGA (see paragraph below)
HFC-FPC08	Communication Gateway Controller without VGA (see paragraph below)
HFC-HSIM	High Speed Interface Module (see paragraph below)

The I/O board assembly naming convention can be understood by reading section 3.5 of RS901-000-01.

HFC-HSIM TX transmits bit data from physical location A to physical location B. The HFC-HSIM TX is connected to a HFC-HSIM RX assembly via fiber optic cable. The TX and RX HFC-HSIM PCB's are identical to each other both in hardware and in FPGA. The difference between TX and RX function is made via DIP switch configuration on the HFC-HSIM PCB.
The only hardware difference in TX and RX implementation comes from the installation of a HFC-HSIMCON RX card at the rear of the backplane slot where the HFC-HSIM RX resides. And similarly the installation of a HFC-HSIMCON TX card at the rear of the backplane slot where the HFC-HSIM TX resides. Bit data transmitted over the fiber link is used to transfer I/O point status from one controller to another controller while maintaining electrical isolation between the two locations.

The HFC-FCUX is an updated version of the HFC-FCPU. The major differences between the two versions are the FCPUX no longer has onboard DO's and DI's and the

FCPUX has a larger FPGA size than the FCPU. The HFC-FPCU is not intended to be supported for future projects, the FCPUX is an active product.

The HFC-FPUM2 is an improved version of the FPUM in regards to input I/O channel hardware design. The HFC-FPUM is not intended to be supported for future projects, the FPUM2 is an active product.

The HFC-FPUA is advertised as a 4-20ma assembly even though the hardware supports input from 0 to 20ma.

The HFC-FPC08 was designed with a VGA chip and VGA port for interfacing an external VGA monitor. This VGA chip has since become obsolete and has been removed from the latest FPC08 BOM part stuffing. However the latest FPC08 design still has the VGA chip shown on the schematic and artwork (pcb) layout. The use of "FPC" in the FPC08 board name stands for Flat Panel Controller. In the VV0115 FPC08 implementation, the FPC08 in not being used as a flat panel controller. The FPC08's function in this system is to transfer system application and PCB status information from the safety system to the Operator Workstation.

The HFC-FCPU/FCPUX' s function is to run a DGLS application, read and write status information from I/O cards, and the transfer I/O card status information to the FPC08.

2.2.3 HFC-6000 FPGA TEST SYSTEM ARRANGEMENT

The arrangement of the test system is the same as previous qualification systems such as ERD111 and ERD1192. Reference Loop Logic Drawing 71006301Q sheet 2. There are two racks of FPGA I/O and controller boards mounted in a sturdy frame. The two racks are referred to as Remote 1(rack 1) and Remote 2 (rack 2). The frame is open and as such has no doors or exterior walls. Mounted in this frame is also termination cards, power supply rack, fan tray rack and fiber optic repeater cards (HFC-FOT06). A panel mounted on the top of the frame contains supporting hardware such as breakers, surge arrestors, EMI filters, terminal blocks and a fuse block.

External to this frame is a simulation rack (Remote 3 HPAT) that contains a FPC08 (controller version) and various DSP I/O cards used for simulation. This rack has its own separate power supply. This rack has its output I/O points wired to remote 1 and 2 input I/O points. This rack has its input I/O points wired to remote 1 and 2 output I/O points. All remote 3 DI points are also SOE points.

A computer is used by the test technician to actuate specific tests, log test data and view current operational status of the test system. This computer is the EWS/MCRT/HIFR all in one.

Reference drawing 71006501Q. The communication link between these devices consists of CAT5 Ethernet cables and fiber optic cables. Each communication path (except HSIM) is redundant. FPC08's in remote 1 and 2 connect to HFC-FOT06's via CAT5 cables (copper). From the FOT06's, fiber connects remote 1 and 2 to fiber/cat5 converters at the remote 3 location. CAT5 cables are connected to the EWS and remote 3 FPC08s,

Remote 1 and 2 are typically located inside a test chamber for EMI/RFI and environmental testing while remote 3 and the EWS are located outside of the chamber. Fiber and copper cables connect the system together via small portals in the wall of the test chamber.

2.2.4 I/O CARDS ASSEMBLIES

The hardware design for each I/O card assembly includes primary and secondary FLINK ports, Control FPGA, Diagnostic FPGA, I/O channels and LED status displays. The onboard software is composed of FPGA and flash memory programming files. The software for each card type provides a scan algorithm that provides specific support for the hardware interface on that card.

2.2.5 C-LINK HARDWARE

The C-Link is a redundant data highway that enables data transfer throughout the system. When an installation includes controllers installed in multiple cabinets, each cabinet includes a separate fiber-optic transceiver card. The controller in the cabinet uses the fiber-optic transceiver card via the FPC08 to send data to the C-Link. If a single cabinet contains more than one controller, all FPC08's in that cabinet are connected to one another in a redundant communication link. Each C-Link processor is configured as a single physical node on the redundant C-Link. The C-Link for the qualification system consists of two nodes that enable one-way communication with the PC workstations via a gateway/isolator hub. Node 1 is at the Remote 1, Remote 2 location. Node 2 is the Remote 3 location.

2.2.6 DIGITAL/ANALOG LOGIC CONTROL

There is no way to activate specific logic tests in the FCPU/FCPUX's application directly from the EWS. Activation of Remote 3 DO's and AO's are the only way to activate the FCPUX logic tests. Remote 3 I/O is hard wired to Remote 1 and 2 DI's and AI's. Logic in the FCPUX is designed such that upon activation of certain inputs, corresponding tests are activated. The MCRT graphic pages are configured to invoke the technician's commands/signals to the application running in the Remote 3 FPC08 controller. All simulated algorithms are implemented in the controller application. The HPAT is configured for SOE logging using HFC-SBC04A DI's and other I/O points for simulated loops are supported by HFC-DO16J's (DO), HFC-AO8FD's (AO), and HFC-AI16FD's (AI).

2.2.7 TEST SPECIMEN SYSTEM POWER DISTRIBUTION

Reference drawing 71006601Q. The test frame includes a power supply rack which contains two sets of 24VDC power supplies. The rack and power supplies are the same models used in ERD111 and ERD1192 testing. Each set of power supplies outputs are wire OR'd so that failure or removal of one power supply does not power down the system. One set of power supplies provide operating power to the two racks for the controllers and I/O cards, fan tray, and HFC-FOT06's. The +24-vdc power lines are diode auctioneered on each card in the chassis to produce onboard logic power. The +24-vdc power is referenced to a common instrument ground. The other set of wire OR'd 24VDC power supplies provides field contact interrogation (excitation) power for FPUD02 DI's. A DIP switch option on the FPUD02 permits selection of either isolated or common configurations for the excitation power.

2.2.8 NON-CLASS 1E EQUIPMENT

2.2.8.1 EWS/MCRT Workstation

The EWS/MCRT workstation consists of a suite of software utilities installed on a PC workstation to support the development and maintenance of application software, system maintenance, diagnostics, and fault isolation for HFC control systems.

The workstation provides the normal operator interface for the control systems. It is equipped with a suite of software utilities that provide interactive graphics, alarm displays, overall system status displays, historical logging (HAS), SOE logging and data archiving functions. The interactive graphics displays provide software controls for entering command inputs for both digital and analog control loops with or without the touch screen function. Such command inputs can operate in parallel with physical control modules, or they can be used to replace existing mechanical controls. The operator can choose to have multiple displays operating simultaneously or to vector from one display to another based on status messages that appear on screen. In addition, the historical archiving software provides the capability of generating a regular log of system point values. The resulting database provides an archive that can be used for generating the plant operation reports.

2.2.8.2 System Tester/Simulator (HPAT)

The system tester/simulator consists of a non-redundant HFC-FPC08 controller and HFC-6000 I/O rack with the HFC-6000 DSP series card types. The HPAT provides hardware and software components needed to support SOE logging and closed-loop testing of several test specimen functions.

Section 3.0

TEST SPECIMEN CONFIGURATION

3.1 INTRODUCTION

This section defines the type of hardware components to be included in the Test Specimen.

3.2 TEST SPECIMEN EQUIPMENT

The overall arrangement of the Test Specimen is described in Section 2 of this document.

- At least one of each module type to be qualified, including I/O modules, controllers, ancillary devices, and additional modules needed for comprehensive testing of the FPGA configuration.

- Maximum available discrete and analog I/O channels of the qualifying components are used for operability and prudency testing.

- 2 controller chassis of nearly identical I/O cards (Reference Section 2.2) and controller cards are used.

- Terminal card support for distributing simulated field signals to I/O card channels.

Refer to the Master Configuration List (MCL) in section 5.0 of this document for the complete list of the hardware components included in this test specimen. Additional components may be included to support I/O requirements of the particular control logic functions selected for inclusion in the TSAP. The hardware components that make up the HPAT controller and its I/O are excluded from the MCL.

Section 4.0

TEST SPECIMEN SOFTWARE

4.1 INTRODUCTION

The software installed on the Test Specimen includes a separate executive FPGA program on each I/O card and FCPU/FXPUX, operating system software installed on the HFC-FPC08, and the TSAP. The TSAP on the FCPU/FCPUX is installed in flash memory. The Remote 3 FPC08 controller also has a simulator application program installed into memory, but his application is not part of the test specimen.

4.2 OPERATING SYSTEM SOFTWARE

The HFC-FCPU/FCPUX and all FPGA I/O cards contain two FPGAs. One FPGA is the "control" FPGA and the other FPGA is the "diagnostic" FPGA. The un-programmed control and diagnostic FPGA devices themselves are identical on each card type but the two devices are programmed with different object codes. The two FPGAs monitor each other for correct operation and if a fault is detected by either one of the FPGAs, the FPGA w/o the fault can put the board into a failsafe mode. FPGAs come in different memory sizes and since the memory/gate size requirement is different based on board function type, not all FPGA boards use the same FPGA size.

The FLINK uses the "Master-for-a-Moment" (MFM) token passing method to ensure orderly transfer of link access from one board to the next. Both control and diagnostic FPGAs are able to receive data from the connected redundant F-Link but only the control FPGA is able to transmit the broadcast data during its mastership over the F-Link.

4.2.1 I/O CARD SOFTWARE

Each I/O card contains a non-user modifiable FPGA program which contains an algorithm that controls its particular scan processing function and communication sequence with the FCPU/FCPUX. Specific functions performed by this software include the following:

- Run a set of initialization tests following power up or manual reset.
- Configure redundant RS485 serial interfaces with the FLINK.
- Accept and validate messages from the controller card
- Maintain internal fault status
- Create and send status messages to the controller card.
- Run the appropriate I/O scan (unique for each card type)
- AI cards run periodic calibration cycles to correct for amplifier drift.
- AI cards test each input for over range/under range status.

4.2.2 MAIN CONTROLLER SOFTWARE

Each HFC-FCPU/FCPUX controller card contains a FPGA program which contains a user modifiable application algorithm and a non-user modifiable platform algorithm that controls its particular scan processing function and communication sequence with the FCPU/FCPUX. Major controller functions are as follows:

- Run a set of initialization tests following power up or manual reset.
- Configure two RS485 serial interfaces with the FLINK.
- Send and receive I/O card status and I/O point status from FPGA I/O cards.
- Run the TSAP software at least once in each cycle and update system status
- Monitor internal status for fault conditions.
- Configure two RS485 serial interfaces with the GLINK.
- Send I/O card status, I/O point status and FCPU/FCPUX status to the FPC08.
- Manage the transfer of equalization status information between a redundant pair of the FCPU/FCPUX via the RIF.

4.2.3 HFC-FPC08 GATEWAY SOFTWARE

The FPC08 also contains a FPGA, but has no companion monitoring FPGA like the other boards in this system. Major controller functions are as follows:

- Configure two RS485 serial interfaces with the GLINK.
- Receive I/O card status, I/O point status and FCPU/FCPUX status from the FCPU/FCPUX.
- Configure redundant serial interfaces with the C-Link. The C-Link on the primary FPC08 broadcasts current system data to the EWS while the secondary FPC08 functions as a hot spare.
- Transfers I/O board status and I/O point status from the FCPU/FCPU to the EWS.
- [

]

4.3 APPLICATION PROGRAM SOFTWARE

4.3.1 TSAP SOFTWARE

The TSAP resides in nonvolatile memory of the FCPU/FCPUX controllers. This application software consists of configuration tables that define the internal architecture of the system and specific analog and digital algorithms for test control system functions. The overall scope of the TSAP includes the following:

- Configuration for all analog and digital I/O cards are included in the test specimen. This table contains the link address for each configured card on the FLINK and identifies the point types associated with each card.
- RQ configuration table that determines the content of data that are "listened for" and sent on the C-Links.
- Sequential equation statements capable of exercising the following minimum functions for analog control:
  - CQ4 blocks for analog processing.
  - Bistable monitors to detect analog alarm states
  - Multi-input signal select function
  - Characterize function
  - Standard arithmetic functions
  - Conversion between floating point and fixed point

The TSAP application software includes basic required support for tests such as the timer test, response time test and BOE test. In addition to the support logic for these tests there is also added logic support a typical DGLS application. The DGLS application is not required but is added to provide an additional visual, graphical and empirical confidence the TSAP software and hardware is working ok.

- Sequential equation statements to exercise the standard Boolean functions including the following:
  - Multi-input AND
  - Multi-input OR
  - Time on delay
  - Time off delay
  - Pulse
  - Set/Reset memory
  - Reflash alarm function
- Sequential equation statements to support specific operability and prudency tests.
- Specific logic to support open & closed loop testing.

Refer to VV0115 TSAP Validation Test Procedure TP901-115-06 for further information on specific TSAP algorithms.

4.3.2 HPAT APPLICATION SOFTWARE

The HPAT application resides in nonvolatile memory of the Remote 3 HFC-FPC08 controller included as part of the tester assembly. This software is configured to support the following functions:

- SOE logging of significant test points controlled by the HFC-FPUD01 output channels
- Specific control signals to support the timer test, response time test, BOE test.

Section 5.0

MASTER CONFIGURATION LIST (MCL)

[

]

[

]