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SUBJECT: Forwards responses to open items addressed at NRC review of ESF load sequencer.

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December 3, 1981
ANPP-19591 - JMA/JWR

Mr. R. L. Tedesco
Assistant Director for Licensing
Division of Licensing
Office of Nuclear Reactor Regulation
U.S. Nuclear Regulatory Commission
Washington, D.C. 20555

Subject; Palo Verde Nuclear Generating Station
(PVNGS) Units 1, 2 and 3
Docket Nos. STN-50-528/529/530
File: 81-056-026; G.1.10

Dear Mr. Tedesco:

The PVNGS ESF load sequencer was discussed with the NRC staff representative at a meeting held in San Diego, California on October 19 and 20, 1981.

Attached are APS' responses to the open items from that meeting (Attachment 1) and conference notes from the meeting (Attachment 2).

Evaluation results regarding Items E and I will be provided in the near future.

Please contact me if you have any further questions.

Very truly yours,

JMAllen for

E. E. Van Brunt, Jr.
APS Vice President,
Nuclear Projects
ANPP Project Director

EEVBJr/JWR/av
Attachment
cc: J. Kerrigan (w/a)
P. Hourihan (w/a)
A. C. Gehr (w/a)

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STATE OF ARIZONA)
) ss.
COUNTY OF MARICOPA)

I, John M. Allen, represent that I am Nuclear Engineering Manager of Arizona Public Service Company, that the foregoing document has been signed by me for Edwin E. Van Brunt, Jr., Vice President Nuclear Projects, on behalf of Arizona Public Service Company with full authority so to do, that I have read such document and know its contents, and that to the best of my knowledge and belief, the statements made therein are true.

John M Allen
John M. Allen

Sworn to before me this 3RD day of December, 1981.

Connie Lou Armstrong
Notary Public

My Commission expires:

June 24, 1983

ATTACHMENT 1

RESOLUTION OF OPEN ITEMS ADDRESSED AT
NRC DESIGN REVIEW OF ESF LOAD SEQUENCER

Action A

Provide documentation of the rationale used to develop the design demonstration tests and why the testing was used in lieu of a sneak circuit analysis.

Response

The design demonstration tests were performed in response to the PVNGS Units 4 and 5 SER which required detailed analyses to show that there are no credible sneak circuits or common failure mode in the sequencer design that could render both onsite and offsite power sources unavailable.

Because the sequencer design incorporates a microprocessor based system, it was determined that a classic sneak circuit analysis was not applicable to this type of system. It was further determined that a rigorous test program on actual hardware was more comprehensive than a sneak circuit analysis to verify the integrity of the design since it involved analysis of sequencer performance integrated with the onsite and offsite power systems design, as well as detailed circuit implementation design.

Since acceptance testing had already demonstrated that no sneak paths resulted in undesirable system outputs for the design basis scenarios of LOCA with and without loss of offsite power (LOP) and for the LOP only condition, additional testing of other input scenarios was considered appropriate to demonstrate that the design had no sneaks or common mode faults which would result in undesirable system action. The tests were then set up to test input scenarios in the time intervals of: inputs occuring before and coincident with a loss of offsite power and inputs subsequent to an LOP before sequencing, during sequencing and following completion of sequencing.

Samples of input signals and input signal combinations were tested to verify proper execution of the system software in determining the proper mode of operation or an appropriate change in mode. The software logic responds only to select combinations of inputs for the specific modes and ignores all other combinations. These "don't cares" make the software logic very simple and easy to test for all combinations once a sample of "don't cares" has been tested. It has been verified that these samples exercised the software code such that all input and input combination scenarios will not cause undesirable sequencer response. These tests were completed satisfactorily and demonstrated that the sequencer system will perform as designed and verified no sneak circuits or common failure modes render both onsite and offsite power sources unavailable.

Action B

Review the "system stall" circuit design and consider annunciation to the operator or delete the system interconnection and implement separate watchdog hardware.

Response

The BOP ESF load sequencer design is being revised to provide control room annunciation to the operator whenever system stall occurs. Any software changes that are made to the auto-test program will be independently reviewed to ensure no affect on the sequencer program.

Action C

Commit to a license condition that software changes cannot be made under 10 CFR 50.59.

Response

All changes to BOP ESFAS sequencer software will be transmitted to the NRC. Software changes will not be made under 10 CFR 50.59.

Action D

Commit to the use of auto-testing. The auto-testing need not be running all of the time, but at a frequency commensurate with the desired reliability.

Response

It is our intent to run the BOP ESFAS in the auto-test mode continuously. As was discussed at the meeting, placing a channel in bypass prohibits auto-testing. We have reviewed our design reliability goal of .9999 and have determined that this goal can be exceeded if testing is performed on a weekly basis. We, therefore, will auto-test at least once a week. In the event that auto-testing cannot be performed, we will provide complete BOP ESFAS system testing in at least one sequencer mode on a monthly basis. Because complete system testing is a more rigorous test, monthly testing is sufficient to maintain our reliability goal.

Action E

Review the detectability of optical isolator failure to isolate and commit to testing of the isolation capability with a method and frequency based on hardware failure modes.

Response

A review of optical isolator failure mechanisms and methods of detecting failures is still in process. A response will be provided later.

Action F

Commit to including the ESF load sequencer in the diesel generator availability technical specification.

Response

The ESF load sequencer will be included in the diesel generator technical specification.

Action G

Commit to reporting inadvertent operation of the load sequencer as an LER.

Response

We will report all inadvertent operations of the load sequencer as an LER.

Action H

Provide a list of periodic testing that will be performed on the system and commit to providing operating procedures, maintenance procedures, and technical specifications prior to fuel load.

Response

In addition to weekly or monthly tests identified in the response to Action D, the BOP ESFAS system will be fully tested at least every 18 months at the time of refueling. These tests will include testing of all sequencer modes and ESFAS logic circuits. Sequencer timing will also be checked as a part of this test.

Action I

(This item resulted from telephone conversations with the NRC subsequent to the NRC Design Review Meeting.) Perform an independent design verification and validation of the ESF load sequencer software.

Response

The design demonstration tests discussed under response to Action A provided sufficient confidence levels in the system that additional verification and validation of the system software is considered unnecessary. However, in light of the NRC's persistence in this area, APS is proceeding to have the BOP ESFAS sequencer software independently verified and validated. Results of this independent review will be submitted to the NRC staff as soon as it becomes available.