APPENDIX E

TECHNICAL SPECIFICATION PAGES

WITH PROPOSED CHANGES INDICATED

Add the following Inserts where indicated on the attached Technical Specification page markups.

INSERT A

"4.4.1.1.3 Each reactor coolant system recirculation loop pump speed controller shall be demonstrated OPERABLE at least once per 24 months by verifying that the average rate of change of pump speed is:

a. Less than or equal to 10% of rated pump speed per second increasing, and

b. Less than or equal to 10% of rated pump speed per second decreasing."

INSERT B

". . . recirculation pump speed and flow . . ."

INSERT C

The Supply System will add the following sentence to the Bases upon approval of the proposed changes to the Technical Specifications: *"The response times assume a 60 Hz output frequency from the adjustable speed drives (ASDs)."*

3/4.2 POWER DISTRIBUTION LIMITS

3/4.2.7 STABILITY MONITORING - TWO LOOP OPERATION

LIMITING CONDITION FOR OPERATION

3.2.7 The stability monitoring system shall be operable* and the decay ratio of the neutron signals shall be less than .75 when operating in the region of APPLICABILITY.

APPLICABILITY: OPERATIONAL CONDITION 1, with two recirculation loops in operation and THERMAL POWER/core flow conditions which lay in Region C of Figure 3.2.7-1.

ACTION:

a. With decay ratios of any two (2) neutron signals greater than or equal to 0.75 or with two (2) consecutive decay ratios on any single neutron signal greater than or equal to 0.75:

As soon as practical, but in all cases within 15 minutes, initiate action to reduce the decay ratio by either decreasing THERMAL POWER with control rod insertion or increasing core flow ~~with recirculation flow control valve manipulation~~. The starting ~~or shifting~~ of a recirculation pump for the purpose of decreasing decay ratio is specifically prohibited.

b. With the stability monitoring system inoperable and when operating in the region of APPLICABILITY:

As soon as practical, but in all cases within 15 minutes, initiate action to exit the region of APPLICABILITY by either decreasing THERMAL POWER with control rod insertion or increasing core flow ~~with recirculation flow control valve manipulation~~. The starting ~~or shifting~~ of a recirculation pump for the purpose of exiting the region of APPLICABILITY when the stability monitoring system is inoperable is specifically prohibited. Exit the region of APPLICABILITY within one (1) hour.

SURVEILLANCE REQUIREMENTS

4.2.7.1 The provisions of Specification 4.0.4 are not applicable.

4.2.7.2 The stability monitoring system shall be demonstrated operable* within one (1) hour prior to entry into the region of APPLICABILITY.

4.2.7.3 Decay ratio and peak-to-peak noise values calculated by the stability monitoring system shall be monitored when operating in the region of APPLICABILITY.

*Verify that the stability monitoring system data acquisition and calculational modules are functioning, and that displayed values of signal decay ratio and peak-to-peak noise are being updated. Detector levels A and C (or B and D) of one LPRM string in each of the nine core regions (a total of 18 LPRM detectors) shall be monitored. A minimum of four (4) APRMs shall also be monitored.

3/4.2 POWER DISTRIBUTION LIMITS

3/4.2.8 STABILITY MONITORING - SINGLE LOOP OPERATION

LIMITING CONDITION FOR OPERATION

3.2.8 The stability monitoring system shall be operable* and the decay ratio of the neutron signals shall be less than .75 when operating in the region of APPLICABILITY.

APPLICABILITY: OPERATIONAL CONDITION 1, with one recirculation loop in operation and THERMAL POWER/core flow conditions which lay in Region C of Figure 3.2.8-1.

ACTION:

a. With decay ratios of any two (2) neutron signals greater than or equal to 0.75 or with two (2) consecutive decay ratios on any single neutron signal greater than or equal to 0.75:

   As soon as practical, but in all cases within 15 minutes, initiate action to reduce the decay ratio by either decreasing THERMAL POWER with control rod insertion or increasing core flow ~~with recirculation flow control valve manipulation.~~ The starting ~~or shifting~~ of a recirculation pump for the purpose of decreasing decay ratio is specifically prohibited.

b. With the stability monitoring system inoperable and when operating in the region of APPLICABILITY:

   As soon as practical, but in all cases within 15 minutes, initiate action to exit the region of APPLICABILITY by decreasing THERMAL POWER with control rod insertion. Exit the region of APPLICABILITY within one (1) hour.

SURVEILLANCE REQUIREMENTS

4.2.8.1 The provisions of Specification 4.0.4 are not applicable.

4.2.8.2 The stability monitoring system shall be demonstrated operable* within one (1) hour prior to entry into the region of APPLICABILITY.

4.2.8.3 Decay ratio and peak-to-peak noise values calculated by the stability monitoring system shall be monitored when operating in the region of APPLICABILITY.

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*Verify that the stability monitoring system data acquisition and calculational modules are functioning, and that displayed values of signal decay ratio and peak-to-peak noise are being updated. Detector levels A and C (or B and D) of one LPRM string in each of the nine core regions (a total of 18 LPRM detectors) shall be monitored. A minimum of four (4) APRMs shall also be monitored.

3/4.4 REACTOR COOLANT SYSTEM

3/4.4.1 RECIRCULATION SYSTEM

RECIRCULATION LOOPS

LIMITING CONDITION FOR OPERATION

3.4.1.1 Two reactor coolant system recirculation loops shall be in operation.

APPLICABILITY: OPERATIONAL CONDITIONS 1* and 2*.

ACTION:

a. With one reactor coolant system recirculation loop not in operation:

1. Verify that the requirements of LCO 3.2.6 and LCO 3.2.8 are met, or comply with the associated ACTION statements.

2. Verify that THERMAL POWER/core flow conditions lay outside Region B of Figure 3.4.1.1-1.

   With THERMAL POWER/core flow conditions which lay in Region B of Figure 3.4.1.1-1, as soon as practical, but in all cases within 15 minutes, initiate action to exit Region B by either decreasing THERMAL POWER with control rod insertion or increasing core flow ~~with flow control valve manipulation.~~ Within 1 hour exit Region B. The starting ~~or shifting~~ of a recirculation pump for the purpose of exiting Region B is specifically prohibited.

3. Within 4 hours:

   a) ~~Place the recirculation flow control system in the Local Manual (Position Control) mode, and~~ Deleted

   b) Increase the MINIMUM CRITICAL POWER RATIO (MCPR) Safety Limit per Specification 2.1.2, and,

   c) Reduce the Maximum Average Planar Linear Heat Generation Rate (MAPLHGR) for General Electric fuel limit to the single recirculation loop operation limit specified in the Core Operating Limits Report, and

   d) Reduce the volumetric flow rate of the operating recirculation loop to $\leq$ 41,725** gpm.

*See Special Test Exception 3.10.4.

**This value represents the actual volumetric recirculation loop flow which produces 100% core flow at 100% THERMAL POWER. This value was determined during the Startup Test Program.

LIMITING CONDITION FOR OPERATION (Continued)

ACTION: (Continued)

e) Perform Surveillance Requirement 4.4.1.1.2 if THERMAL POWER is ≤ 25%*** of RATED THERMAL POWER or the recirculation loop flow in the operating loop is ≤ 10%*** of rated loop flow.

4. The provisions of Specification 3.0.4 are not applicable.

5. Otherwise, be in at least HOT SHUTDOWN within the next 12 hours.

b. With no reactor coolant system recirculation loops in operation, immediately initiate measures to place the unit in at least HOT SHUTDOWN within the next 6 hours.

SURVEILLANCE REQUIREMENTS

4.4.1.1.1 With one reactor coolant system recirculation loop not in operation, at least once per 8 hours verify that:

a. Deleted ~~The recirculation flow control system is in the Local Manual (Position Control) mode, and~~

b. The volumetric flow rate of the operating loop is ≤ 41,725 gpm.**

**This value represents the actual volumetric recirculation loop flow which produces 100% core flow at 100% THERMAL POWER. This value was determined during the Startup Test Program.

***Final values were determined during Startup Testing based upon actual THERMAL POWER and recirculation loop flow which will sweep the cold water from the vessel bottom head preventing stratification.

SURVEILLANCE REQUIREMENTS (Continued)

c. Core flow is greater than or equal to 39% of rated core flow when core THERMAL POWER is greater than the limit specified in Figure 3.4.1.1-1.

4.4.1.1.2 With one reactor coolant system recirculation loop not in operation, within no more than 15 minutes prior to either THERMAL POWER increase or recirculation loop flow increase, verify that the following differential temperature requirements are met if THERMAL POWER is $\leq$ 25%*** of RATED THERMAL POWER or the recirculation loop flow in the operating recirculation loop is $\leq$ 10%*** of rated loop flow:

a. $<$ 145°F between reactor vessel steam space coolant and bottom head drain line coolant,

b. $\leq$ 50°F between the reactor coolant within the loop not in operation and the coolant in the reactor pressure vessel, and

c. $\leq$ 50°F between the reactor coolant within the loop not in operation and the operating loop.

The differential temperature requirements of Specification 4.4.1.1.2b. and c. do not apply when the loop not in operation is isolated from the reactor pressure vessel.

4.4.1.1.3 Each reactor coolant system recirculation loop flow control valve shall be demonstrated OPERABLE at least once per 18 months by:

a. Verifying that the control valve fails "as is" on loss of hydraulic pressure (at the hydraulic control unit), and

b. Verifying that the average rate of control valve movement is:

1. Less than or equal to 11% of stroke per second opening, and

2. Less than or equal to 11% of stroke per second closing.

Add INSERT A

***Final values were determined during Startup Testing based upon actual THERMAL POWER and recirculation loop flow which will sweep the cold water from the vessel bottom head preventing stratification.

REACTOR COOLANT SYSTEM

JET PUMPS

LIMITING CONDITION FOR OPERATION

3.4.1.2 All jet pumps shall be OPERABLE.

APPLICABILITY: OPERATIONAL CONDITIONS 1 and 2.

ACTION:

With one or more jet pumps inoperable, be in at least HOT SHUTDOWN within 12 hours.

SURVEILLANCE REQUIREMENTS

NOTES

The provisions of Specification 4.0.4 are not applicable provided the surveillance is:

1. Performed within 4 hours after the associated recirculation loop is in operation.

2. Performed within 24 hours after exceeding 25% of RATED THERMAL POWER.

These notes are applicable to both surveillance 4.4.1.2.1 and 4.4.1.2.2.

4.4.1.2.1 Each of the above required jet pumps shall be demonstrated OPERABLE at least once per 24 hours by determining recirculation loop flow, total core flow and diffuser-to-lower plenum differential pressure for each jet pump and verifying that no two of the following conditions occur when both recirculation loops are operating.

a. The indicated recirculation loop flow differs by more than 10% from the established ~~flow control valve position loop flow~~ characteristics for two recirculation loop operation. ← Add INSERT B

b. The indicated total core flow differs by more than 10% from the established total core flow value derived from two recirculation loop flow measurements.

c. The indicated diffuser-to-lower plenum differential pressure of any individual jet pump differs from established two recirculation loop operation patterns by more than 20%.

4.4.1.2.2 During single recirculation loop operation, each of the above required jet pumps shall be demonstrated OPERABLE at least once per 24 hours by verifying that no two of the following conditions occur:

a. The indicated recirculation loop flow in the operating loop differs by more than 10% from the established single ~~recirculation flow control valve position loop flow~~ characteristics. ← Add INSERT B

b. The indicated total core flow differs by more than 10% from the established total core flow value derived from single recirculation loop flow measurements.

c. The indicated diffuser-to-lower plenum differential pressure of any individual jet pump differs from established single recirculation loop patterns by more than 20%.

TABLE 3.6.3-1 (Continued)

PRIMARY CONTAINMENT ISOLATION VALVES

VALVE FUNCTION AND NUMBER	VALVE GROUP(a)	MAXIMUM ISOLATION TIME (Seconds)
a. Automatic Isolation Valves (Continued)		
Equipment Drain (Radioactive)	4	15
EDR-V-19 EDR-V-20		
Floor Drain (Radioactive)	4	15
FDR-V-3 FDR-V-4		
Fuel Pool Cooling/Suppression Pool Cleanup	4	35
FPC-V-149 FPC-V-153(f) FPC-V-154(f) FPC-V-156		
~~Reactor Recirculation Hydraulic Control(e)(l)~~	~~4~~	~~15~~
~~HY-V-17A,B~~ ~~HY-V-18A,B~~ ~~HY-V-19A,B~~ ~~HY-V-20A,B~~ ~~HY-V-33A,B~~ ~~HY-V-34A,B~~ ~~HY-V-35A,B~~ ~~HY-V-36A,B~~		
Traversing Incore Probe	4	5
TIP-V-1,2,3,4,5 TIP-V-15		

This entire page to be deleted from Technical Specifications per G02-93-256, dated 10/21/93 (TAC M88163).

TABLE 3.6.3-1 (Continued)

PRIMARY CONTAINMENT ISOLATION VALVES

VALVE FUNCTION AND NUMBER	VALVE GROUP(a)	MAXIMUM ISOLATION TIME (Seconds)
d. Other Containment Isolation Valves (Continued)		
Radiation Monitoring		N.A.
PI-V-X72f/1 PI-V-X73e/1		
Transversing Incore Probe System		N.A.
TIP-V-6 TIP-V-7,8,9,10,11(e)		

This entire page to be deleted from Technical Specifications per GO2-93-256, dated 10/21/93 (TAC M88163).

TABLE NOTATIONS

*But greater than 3 seconds.
#Provisions of Technical Specification 3.0.4 are not applicable.

(a) See Technical Specification 3.3.2 for the isolation signal(s) which operate each group.
(b) Valve leakage not included in sum of Type B and C tests.
(c) May be opened on an intermittent basis under administrative control.
(d) Not closed by SLC actuation signal.
(e) Not subject to Type C Leak Rate Test.
(f) Hydraulic leak test at 1.10 P_a.
(g) Not subject to Type C test. Test per Technical Specification 4.4.3.2.2
(h) Tested as part of Type A test.
(i) May be tested as part of Type A test. If so tested, Type C test results may be excluded from sum of other Type B and C tests.
(j) Reflects closure times for containment isolation only.
(k) During operational conditions 1, 2 & 3 the requirement for automatic isolation does not apply to RHR-V-8. Except that RHR-V-8 may be opened in operational conditions 2 & 3 provided control is returned to the control room, with the interlocks reestablished, and reactor pressure is less than 135 psig.
(l) The isolation logic associated with the reactor recirculation hydraulic control containment isolation valves need not meet single failure criteria for OPERABILITY for a period ending no later than May 15, 1995.

3/4.3.4 RECIRCULATION PUMP TRIP ACTUATION INSTRUMENTATION

The anticipated transient without scram (ATWS) recirculation pump trip system provides a means of limiting the consequences of the unlikely occurrence of a failure to scram during an anticipated transient. The response of the plant to this postulated event falls within the envelope of study events in General Electric Company Topical Report NEDO-10349, dated March 1971, and NEDO-24222, dated December 1979.

The end-of-cycle recirculation pump trip (EOC-RPT) system is a part of the reactor protection system and is an essential safety supplement to the reactor trip. The purpose of the EOC-RPT is to recover the loss of thermal margin which occurs at the end-of-cycle. The physical phenomenon involved is that the void reactivity feedback due to a pressurization transient can add positive reactivity to the reactor system at a faster rate than the control rods add negative scram reactivity. Each EOC-RPT system trips both recirculation pumps, reducing coolant flow in order to reduce the void collapse in the core during two of the most limiting pressurization events. The two events for which the EOC-RPT protective feature will function are closure of the turbine throttle valves and fast closure of the turbine governor valves.

A fast closure sensor from each of two turbine governor valves provides input to the EOC-RPT system; a fast closure sensor from each of the other two turbine governor valves provides input to the second EOC-RPT system. Similarly, a position switch for each of two turbine throttle valves provides input to one EOC-RPT system; a position switch from each of the other two throttle valves provides input to the other EOC-RPT system. For each EOC-RPT system, the sensor relay contacts are arranged to form a 2-out-of-2 logic for the fast closure of turbine governor valves and a 2-out-of-2 logic for the turbine throttle valves. The operation of either logic will actuate the EOC-RPT system and trip both recirculation pumps.

Each EOC-RPT system may be manually bypassed by use of a keyswitch which is administratively controlled. The manual bypasses and the automatic Operating Bypass at less than 30% of RATED THERMAL POWER are annunciated in the control room. The EOC-RPT System instrumentation that provides a trip signal measures first stage turbine pressure to initiate a trip signal. The safety analysis requiring an EOC-RPT bases initial conditions on rated power and specifies turbine bypass operability at greater than or equal to 30% of rated thermal power. Because first stage pressure can vary depending on operating conditions, the qualifying notes describing when the turbine bypass feature is to disabled specify a turbine first stage pressure corresponding to less than 30% RTP (turbine first stage pressure is dependent on the operating parameters of the reactor, turbine, and condenser). Therefore, because a value for turbine first stage pressure cannot be precisely fixed and because pressure measurement initiates the trip the Technical Specification refers to a pressure associated with a specific Rated Thermal Power value rather than a value for pressure.

The EOC-RPT system response time is the time assumed in the analysis between initiation of valve motion and complete suppression of the electric arc, i.e., 190ms, less the time allotted for sensor response, i.e., 10ms, and less the time allotted for breaker arc suppression determined by test, as correlated to manufacturer's test results, i.e., 83ms, and plant preoperational test results. Add INSERT C

Operation with a trip set less conservative than its Trip Setpoint but within its specified Allowable Value is acceptable on the basis that the difference between each Trip Setpoint and the Allowable Value is equal to or less than the drift allowance assumed for each trip in the safety analyses.

ATTACHMENT 1

Attachment 1 contains the detailed responses to the staff questions

The following information provides the Supply System responses to the staff questions from Reference 1. The question numbers and question statements from the Reference 1 enclosure are duplicated for convenience and tracking.

Question 1

What are the sources of power for the GE-FANUC system?

Response

The GE-FANUC control system for the RRC system ASD is located in main control room panel E-CP-H13/P634. The 120 VAC power to the H13/P634 panel is supplied from a critical bus. The FANUC Input/Output (I/O) signal communication panel, E-CP-RRC/ASD/1, is located in the ASD building. The 120 VAC supply to the local ASD panel (E-CP-RRC/ASD/1) is powered from E-PP-ASD1/4 circuits 5 and 6. The E-PP-ASD1/4 panel is fed from two redundant uninterruptible power supply (UPS) units (RRC-IN-ASD/1A and 1B). If one UPS power source fails, the control system will automatically switch to the alternate source.

Question 2

Explain how the GTO chopping technique works to eliminate harmonic frequencies to the motor which could create resonance. What are the consequences if the chopping technique fails? What indication is given in the control room of a GTO failure?

Response

The ASD can be divided into two parts: (1) the silicon controlled rectifier (SCR) source (rectifying AC into DC) bridge and (2) the gate turn-off (GTO) load (inverting DC back into a variable AC) bridge. The SCR source bridge is used to regulate the torque producing current to the motor. The GTO load bridge uses a pulse width modulation (PWM) technique to regulate the fundamental frequency and power factor to the motor. By inserting chops (or pulses) at predetermined angles in the output square wave form of the GTO inverter, the PWM technique can eliminate selected harmonics in the ASD output. This chopping method has been programmed into the ASD control to eliminate the following harmonics:

Range of Fundamental Frequency (Hz)	Harmonic Eliminated
5 - 7	23-25
7 - 12	17-19
12 - 17	11-13
17 - 25	7-11
25 - 32	5-7
32 - 42	5
42 - Max.	None

If a failure in the chopping software were to remove the chopping function when the pump speed was less than 42 Hz, pump vibration levels could increase. As described in Appendix B of Reference 2, the monitoring equipment would detect excessive vibration.

A GTO failure would initiate either an ASD alarm or fault which will be annunciated in the main control room. A GTO failure indication will be displayed at the local ASD printer and on the Video Display Unit (VDU) in the main control room at panel H13/P602.

Question 3

Describe surveillance/periodic testing to be performed which will assure that harmonic current from the adjustable speed drive will be maintained within established limits at safety as well as non-safety buses.

Response

There are no plans to perform surveillance or periodic testing of the harmonic currents. The baseline test performed in June, 1995 indicated 3.7 percent voltage total harmonic distortion (THD) on the "A" RRC loop and 5.2 percent on the "B" RRC loop. The testing was performed at 30 Hz. In addition, during Power Ascension Testing the harmonics will be monitored and compared to previous results.

The safety related loads are fed from normal transformer one (TR-N1) and are isolated from the harmonics effect. The equipment connected to SH-5 and SH-6 buses is not safety related. In addition, the windings of normal transformer two (TR-N2) mitigate the effects of the harmonics. The gate circuits are the primary source of the harmonic voltages. A failure in the gate circuits would cause an increase in the harmonic level. It would also cause a channel trip and be annunciated in the control room. Therefore, no additional surveillance or periodic testing is deemed necessary.

Question 4

Given that the harmonic currents generated are kept within a 5 percent limit by harmonic filters, will there be any resonant conditions generated which could produce currents greater than the electrical equipment is designed to?

Response

The design of the ASD system does not include harmonic filters immediately downstream of the power source to the ASD. Filters were not considered necessary for this installation because the THD was acceptable. The motor filter capacitors act as harmonic filters on the motor side of the ASD. Harmonic filters upstream of the ASD equipment will only be installed if future operating conditions indicate a need for additional filtering. During normal plant operation, the SH-5 and SH-6 buses are connected to TR-N2 and the safety related loads are connected to TR-N1. Thus, there is no interconnection between the non-safety related SH-5 and SH-6 buses and

the safety related buses. As discussed in the response to Question 5 (below), the equipment on the critical buses, SM-4, SM-7 and SM-8, will not be affected by the harmonics since the THD voltage levels on the buses that supply this equipment are expected to be less than 0.5 percent. The primary loads on the SH-5 and SH-6 buses are non-safety related transformers and motors, which are tolerant of harmonics even above 5 percent. The effect of harmonics on these types of loads generally only results in a reduction in expected life due to additional winding heating. Also, the secondary windings of TR-N2 will attenuate the harmonic voltages for the SH-5 and SH-6 loads.

Question 5

At WNP-2, have electrical, instrumentation, and control system equipment been designed to operate satisfactorily with a harmonic voltage of 5 percent superimposed on the input voltage by operation of the proposed adjustable speed drive?

Response

At WNP-2 the electrical, instrumentation, and control system equipment have not been specifically designed for use with harmonic voltages.

General Electric performed a harmonic analysis on the WNP-2 6.9 KV electrical system to determine the extent of the harmonics imposed on the system and their effects on electrical equipment connected to SH-5 and SH-6. The GE report of the analysis concluded that TR-N2 and the startup transformer (TR-S) are to be derated 30% and 31%, respectively, based on their forced oil and air rating.

As a proactive measure, a design specification has been developed for a harmonic filter. The filter may be necessary if future additional loads to TR-N2 and TR-S are calculated to exceed the new ratings. There is no derating of the motor loads connected to either TR-N2 or TR-S. The report concluded that the equipment on the critical buses will not be affected by the harmonics since the THD voltage levels on the buses that supply this equipment are expected to be less than 0.5 percent.

Question 6

Have the harmonic filters been designed and sized for the harmonic current generated from the adjustable speed drive as well as the harmonic current from the power supply system for all modes of plant operation.

Response

As discussed in Question 4, the modification does not include harmonic filters.

Question 7

With the harmonic filters inoperable and the adjustable drive speed at 100 percent, what is the harmonic distortion contribution from the variable speed drive?

Response

As discussed in the responses to Questions 4 and 5, the ASD system at WNP-2 does not include harmonic filters. Therefore, the harmonic distortion data presented in Appendix B, page 4, of Reference 2 provides the 100 percent load contribution from the ASD system.

Question 8

It is stated in Appendix B, page 22 [*sic*], that the onsite operational testing of the ASDs was performed in June 1995 (during a plant outage). During the testing, the highest voltage total harmonic distortion was 5.2 percent as measured at SM-6 [*sic*]. This value exceeds the 5 percent value established in IEEE-519. What effects does this have on the remaining loads on bus SM-6 [*sic*]? Are there any other tests done on the ASDs since then? If so, please provide the test results. If not, how many tests are planned in the near future?

Response

Note: The discussion of the onsite operational testing appears in Appendix B, page 3 of 22, and includes THD data for the SH-5 and SH-6 buses. It is assumed that this question refers to the SH-6 bus discussed on page 3 of the Appendix.

The SH-5 and SH-6 buses are the 6.9 KV power supply for the ASDs. The SM-1, SM-2, and SM-3 buses are the 4.16 KV power supplies for the safety related buses. Appendix B, page 3, (3rd paragraph, 2nd sentence), of the Reference 2 submittal incorrectly indicated that the SH-6 bus was the safety related SM-7 bus power supply and the SM-1 bus was the ASD power supply (the parenthetical statements following "SH-6" and after "SM-1" were interchanged). The SH-6 bus is actually the ASD power supply and the SM-1 bus is actually the safety related SM-7 bus power supply. The other references to the ASD and safety related bus power supplies are correct.

As discussed in the response to Question 4, the primary loads on the SH-5 and SH-6 buses are non-safety related transformers and motors. The effect of harmonics on these types of loads generally only results in a reduction in expected life due to additional winding heating. Also, the secondary windings of TR-N2 will attenuate the harmonic voltages for the SH-5 and SH-6 loads.

There has been no additional harmonics testing since June, 1995. During the Power Ascension Test the harmonics will be monitored.

Question 9

Appendix B, page 4, provides the results of an analysis in percentage of total harmonic distortion in startup as well as in generation mode. Please explain the last three columns of tables on this page.

Response

The last three columns of each of the two tables in Appendix B, page 4, are the electric current (I) total harmonic distortion (THD I) analysis results for the startup and generation modes of plant operation.

In the startup mode, the SH-5 and SH-6 buses (ASD power supplies) are connected to the "X" winding of TR-S and the SM-1, SM-2, and SM-3 buses (safety related bus power supplies) are connected to the "Y" winding of TR-S. The primary (or high side) winding of TR-S is designated as the "H" winding. The THD I data for the TR-S windings (with respect to the various ASD channel operating modes) are contained in the last three columns of the startup mode table. The columns labeled "THD I" in conjunction with "TRS-X," "TRS-Y," and "TRS-H" contain the THD I data analyzed to be at the "X," "Y," and "H" windings of TR-S, respectively.

In the generation mode, the main generator supplies power to the main step-up transformers (TR-M) which, in turn, supply power to the Bonneville Power Administration 500 KV grid system. In this mode, the main generator also supplies power to TR-N1 and TR-N2. The SH-5 and SH-6 buses are connected to TR-N2 and the SM-1, SM-2, and SM-3 buses are connected to TR-N1 in the generation mode. The columns labeled "THD I" in conjunction with "TR-N2" and "TR-M" contain the THD I data analyzed for TR-N2 and TR-M secondary (low side) windings, respectively. The column labeled "THD I" in conjunction with "TR-N1 (Pri)" contains the THD I data analyzed for TR-N1 primary (high side) winding.

Also, in the startup mode table in Appendix B, page 4, 20, 40 and 60 percent load rows represent the startup mode condition. The analytical data support a speed increase to 60 percent during the startup mode without reaching the 5 percent limiting value (recommended in IEEE-519) on any bus.

Question 10

It is stated in Appendix B, page 2, that the adjustable speed operation affects RPT breaker performance. Since the ASDs vary the frequency of the power supplied to the motor, the opening time of the breaker will vary inversely with the supplied voltage, i.e., if the system is operating at 15 HZ the opening time of the RPT breakers increases to 20 cycles (assuming normal opening time of the breaker to be 5 cycles). With this delay in opening time, are these breakers still properly coordinated with the containment electrical penetration conductors for all possible short circuit conditions, including maximum available fault current? Your response should also include the coordinated fault-current-versus-time curves for these penetrations.

Response

This response divides the question into two parts. What effect will operating at 15 Hz have on the EOC-RPT breaker opening time? Are the containment electrical penetration conductors protected from all possible short circuit conditions?

This installation has no adverse effect on the EOC-RPT breaker opening time. The EOC-RPT system is required to be operable above 30 percent rated thermal power. The current EOC-RPT system trips the 60 Hz power supply to the RRC pumps by opening the EOC-RPT breakers, transferring the pumps to the 15 Hz power supply. Following the installation of the ASD, an EOC-RPT signal will still open the EOC-RPT breakers, tripping the RRC pumps. However, the pumps will no longer transfer to another power supply. The opening time of the EOC-RPT breaker is not a direct inverse function of the frequency. The breaker opening time includes the mechanical spring opening time plus the arc quenching capability. The mechanical spring opening time is constant and independent of frequency. The arc quenching varies inversely with the frequency. Consequently, it was conservative for the transient analysis to assume the entire opening time was inversely proportional to frequency.

The current limiting function and the short circuit protection for the penetrations are discussed below. The relay fault current vs time curves showing the ASD application are still being developed. Preliminary checks have shown that the points in question are to the left of the 1000 MCM damaged time (i^2t) curve. With no points to the right of this curve, the operating conditions are then bounded.

The containment penetration conductor protection is still provided by the RRA and RRB breakers (primary feeder breakers for the ASD) and backed up by the SH-5 and SH-6 feeder breakers. Since these breakers still operate in the 60 Hz portion of the system, opening time is not impacted due to the 15 Hz operation downstream of the ASD. Additional protection is provided however, from the volts/hz, over current, and voltage balance relays that have the sensors located downstream of the ASD but trip the RRA and RRB breakers. The over current relays fed from the current sensors connected upstream of the ASD equipment satisfy the Technical Specification requirements for containment penetration conductor protection. The ASD installation improves the over current protection by:

1. providing higher impedance between power source and load;

2. isolating the penetration from 6.9 KV motor fault current contribution;

3. the ASD current limiting design function.

The cable penetrations for the RRC pump motor consist of one 1000 MCM copper conductor per phase. To protect a cable penetration against a through-fault current level estimated at 1916 amps (RMS), the RRA, RRB, SH-5, and SH-6 circuit breakers must interrupt the fault in 1000 seconds or less. The tripping time required to protect the cable penetration is well within the tripping time of these breakers.

The capability for the cable penetration to withstand the capacitor discharge current of 30,000 amps is around 2.6 seconds. The capacitor discharge currents will dissipate within 2 to 3 cycles (30 - 50 ms).

The ASD is a current source type drive. That is, the ASD is designed to maintain the operating current required by the motor, even if the load impedance changes. Upon a short-circuit fault, the ASD current can surge up to 2.5 times its operating current. But the iterative scan function of the microprocessor will regulate the fault current back down by reducing its output voltage.

The operating current at each of the ASD terminals is 726 amps @ 63 Hz. The expected short-circuit current surge from the ASD is:

726 amps x 2.5 = 1815 amps (RMS)

Each ASD channel has an instantaneous trip which is set at:

1.7 x 654 amps (Drive Base current) = 1112 amps (RMS)

Upon a short-circuit fault greater than 1112 amps, the ASD will interrupt the fault within 20 msec.

In the 12 pulse mode, the ASD fault contribution to a fault on the 6.9 KV bus will be:

1815 amps x 2 x (3800/7200) = 1916 amps (RMS)

where: 2 = number of ASD channels;

3800/7200 = transformer ratio

In addition to the ASD short-circuit current contribution, the motor filter capacitors located at the ASD terminals will also discharge a current into the fault. This capacitor peak discharge current may be as large as 30,000 amps. Since this peak discharge current should dissipate to a safe value within 2 to 3 cycles, it will not have a detrimental impact on the cable penetrations for the RRC pump motor circuits.

Question 11

Provide a schematic diagram that shows all the protective devices used for the ASD system.

Response

The schematic diagram is included as Attachment 2.

Question 12

The change from 18 month to 24 month surveillance interval and some of the accident analysis sections refer to the high reliability of the FANUC and MEM units. The numbers are given as "per demand."

a. Provide a description of this term as it relates to the startup and normal operation of the ASDs.

b. Provide the information which forms the basis for those reliability numbers.

Response

a. The system failure probabilities of 1.25 E-06 and 4.26 E-06 per system demand that were calculated for the recirculation flow control system GE-FANUC control logic and the entire ASD system, respectively. The "per demand" phrase refers to the situation where the system is in a state of readiness to perform its function (shutdown or operating at steady state) and a demand is made on the system to change state (e.g., startup, runback, operator demand for a higher or lower speed).

The "per demand" numbers given consider both the probability that the GE-FANUC or ASD MEM will not respond to the demand and the probability of random failure. The analysis considers faults occur when there is a demand placed on the system. The "per demand" type of analysis is typically used for standby systems that must respond on demand.

b. The reliability numbers were taken from GE proprietary reliability analysis report NEDC-32232P, "WNP-2 Reactor Recirculation Adjustable Speed Drive (ASD) System Reliability Analysis," prepared by GE Nuclear Energy and dated August, 1993. The non-proprietary Executive Summary from this document is included as Attachment 3 and describes the methodology. The failure rate information in this analysis was derived from manufacturer information and industrial failure rate information. This analysis also analyzed the system on a parts count basis and calculated a single channel failure rate of 6.85 E-05 per hour, which was considered low. The parts count approach is conservative since it assumes that all component failures lead to system unavailability. The calculated control logic and system availability were calculated to be 99.9998 percent and 99.9994 percent, respectively.

Additional reliability numbers for ASDs are found in EPRI TR-101140, "Adjustable Speed Drives Application Guide," dated December, 1992. This report indicates a mean time between failure (MTBF) for an ASD with dual channels of 120,000 hours.

GE Drive Systems indicates a 352,000 hour MTBF for a drive and a drive availability for a 12 pulse dual channel system of 99.97 percent based on field performance (see Attachment 4).

Question 13

Are all of the alarms listed in Table 2 of Appendix B [*sic*] annunciated in the control room?

Response

The two hardwired alarms from each ASD channel annunciated in the control room are "ASD ALARM" and "ASD FAULT." The alarms listed in Table 2, Appendix C, page 6, of the Reference 2 submittal are displayed on the VDU mounted in the H13/P602 panel in the main control room.

Question 14

Does the logic provide for continued acceleration if there is a failure of one of the ASD channels between 2 and 15 Hz?

Response

During normal startup, the master channel alone (6 pulse operation) will go through the normal startup sequence until a minimum speed of 15 Hz is reached. Once the minimum speed is reached, the slave channel starts, synchronizes with the running channel, and the system goes into 12 pulse operation. If the master channel fails during the startup, the slave channel will synchronize with the running motor and continue the startup sequence. However, the ASD will only be capable of 6 pulse operation at 15 Hz. There is a 0.5 second delay associated with the slave channel such that the slave channel starts approximately 0.5 seconds after the initial start.

If a slave channel failure occurs during startup with the master channel operating, the master channel would continue the startup sequence. Since the slave channel design precludes synchronizing with the running motor at 15 Hz to provide 12 pulse operation, the master channel would continue in only 6 pulse operation. A failure of either the master or slave channel will be indicated to the control room operators by a fault annunciation and the GE-FANUC automatically limits the maximum speed to 52 Hz for single channel operation.

Question 15

Describe the loss of one ASD in more detail. Is the change of the remaining ASD to 52 HZ instantaneous (as fast as the sense and command can perform it) or is it ramped at the pump coast down rate? Given that a single ASD has torque capability of 52 HZ, are there any effects on the system as a result of motoring at 60 HZ down to 52 HZ? Is the ASD maximum frequency limiter changed at the same time?

Response

While operating in the 12 pulse mode above 52 Hz, a loss of one ASD channel results in the following system responses:

- The speed reference of the GE-FANUC controls and the maximum speed limit of the operating ASD channel immediately drops to 52 Hz;

- Upon transferring from the 12 to 6 pulse mode on the loss of one ASD channel, the remaining ASD channel will begin operating in the current limit mode. The current to the RRC pump motor will be reduced approximately 70 percent. The motor will begin to ramp down in speed to 52 Hz, but not as fast as its natural coast down rate of the pump/motor. Just before reaching 52 Hz, the motor current load will be below the current limit of the ASD channel. At 52 Hz the motor will be operating at current and voltage consistent for that operating speed. Thus, there would be no adverse effects on the system as a result of motoring from 60 Hz to 52 Hz.

Question 16

Provide the FANUC and MEM operation, maintenance and installation manuals or the following excerpts. Particular items of interest include the self diagnostics (what parameters are monitored), the manufacturers claimed environmental parameters (temperature, humidity, etc.), automatic actions taken upon a diagnostic result.

Response

The specified items of interest are addressed in Attachment 5. The requested information is contained in the attached documents as follows:

ASD MEM Unit

- Environmental parameters are defined in GEK-103111, sheet 2-1.

- Diagnostics and action taken are described in GEK-103111, sheets 7-1 through 7-15.

GE-FANUC System

- Environmental parameters for the CPU are defined in GFK-0555, sheet 5. These environmental parameters are typical of all the GE-FANUC components.

- Diagnostics and action taken are described in GFK-0265, sheets 2-52 through 2-57, and sheets 3-1 through 3-35.

Question 17

Are there any alarms or indications in the control room of problems with the FANUC and MEM other than microprocessor interrupt?

Response

Refer to the response to Question 13 for the alarms and indications associated with the ASD MEM unit. The other FANUC alarms include Bus A, B, and C Genius I/O Trouble, operating limit conditions - ASD Channel Failure, Rx Level Low, Recirc A or B High Flow Delta, Delta T Cavitation.

Question 18

Describe the quality controls of the manufacturing process. Were the devices under a QA program including software QA, V&V, and configuration management? Is an error and change reporting mechanism in place to assure that WNP-2 is informed of changes/errors in the products? Has WNP-2 or an industry group performed any QA audits of the vendors?

Response

QA Program

The ASD, including the software, was manufactured under a GE quality assurance (QA) program. Verification and validation (V&V) and configuration control practices were performed according to industrial standards. However, these practices do not necessarily comply with the NRC standards for a 10 CFR 50, Appendix B QA program, as described in EPRI TR-102348, "Guideline on Licensing Digital Upgrades," and NRC Regulatory Guide 1.152, "Criteria for Programmable Digital Computer System Software in Safety Related Systems of Nuclear Power Plants." The 10 CFR 50 Appendix B QA program was not deemed necessary due to the non-safety related ASD application at WNP-2.

The GE FANUC hardware was manufactured by GE Fanuc Automation North America, Inc in Charlottesville, Virginia. The FANUC hardware was manufactured under a quality control management program which was standard for the industry in 1992, when the equipment was shipped to WNP-2.

Configuration management

The software for the GE Drive System (GEDS) control is a standard firmware design which cannot be modified in the field by the user. The software can be roughly divided into the categories of "background" and "foreground." The foreground consists of the interrupt driven, real time tasks such as firing calculations and regulator calculations, and phase locked loops. The background consists of tasks such as the monitor, fault/alarm logging, and the control start/stop sequencing. The control tune-up variables for a specific drive are stored in EEPROM memory using a terminal connected to an RS 232 port on the microprocessor card.

The software is made up of modules which were developed, tested and verified through operating experience over the last 8 to 10 years for the GTO-induction motor drive control system. These modules and the resulting object code are stored in a unique job space on the GEDS VAX computer (VAX is a Digital Equipment Corporation product line). The object code has a unique "catalog" number which is used by manufacturing to access the proper data for "burning" (permanently programming) the EEPROMs necessary for loading the control microprocessor board.

If it is necessary to revise the software to correct errors or to provide new standard functions, a new revision is created which is downward compatible with all earlier revisions. All previous modules are preserved by the system. Once the product released to the customer, the software is archived under the control of the GE VAX system manager.

The procedure for creating and maintaining software, controlling viruses, software security, and releasing software is described in the GEDS Requisition Engineering Procedures and Work Instructions "controlled documents" established to comply with International Organization for Standardization (ISO) 9000 Standards.

The GE FANUC software was configured at GE-NE in San Jose, California. The software, which can be modified in the field by the user, was designed under the GE-NE quality control program. The software was independently verified and tested with actual GE FANUC hardware and simulated I/Os. The software sent to the Supply System is a controlled document. A copy of the software is stored on a VAX computer in San Jose. If any changes are made to the software during installation or testing, a revised controlled document will be issued by GE. If GE identifies changes needed following installation and testing, the Supply System will be notified.

Error and change reporting

For the GEDS, an error and change reporting mechanism is in place to correct errors and make changes as described above. A Field Change Notice is issued to Product Service to order and ship new PROMs to the job site to correct identified problems.

Because the WNP-2 FANUC hardware is registered with GE Fanuc, the Supply System will be advised of any errors or changes to the GE FANUC hardware.

QA audits

Neither the Supply System nor Philadelphia Electric Company Energy (for the Peach Bottom plant) have performed a QA audit of GEDS or GE-FANUC. As indicated above, the GEDS QA program was reviewed by an independent third party agency in order to meet ISO 9000 requirements.

Question 19

Provide the company names and factory locations of the designers and manufacturers of the FANUC and MEM.

Response

The MEM unit was manufactured and configured at GEDS in Salem, Virginia. The GE-FANUC was manufactured by GE-FANUC Automation in Charlottesville, Virginia and configured by GE-NE in San Jose, California.

Question 20

Is there any indication to the operator when the limiting functions in the FANUC or MEM override the operator's demand?

Response

There are annunciator alarms in the control room which communicate to the operator the ASD is in a "limit mode." The following limits are annunciated: Channel Failure; Rx Level Low; Delta T Cavitation; Recirc A or B High Flow Delta; Feedwater Pump Trip.

Question 21

Are the ASD over frequency relays separate from the MEM?

Response

Yes, the ASD over frequency relays are separate from the MEM. Two types of over speed protection are provided.

1. A separate electromagnetic frequency relay is mounted on the 6.9 KV bus which feeds the RRC pump motor. If the frequency to the motor is greater than the relay trip setting, the relay will trip the ASD feeder breaker (RRA(B)) and the RPT breaker (4A(B)). Refer to Figure 2B, Appendix C, page 3, of the Reference 2 submittal for the electrical bus and breaker configurations.

2. An over speed trip is incorporated into each ASD channel MEM unit. If the frequency at ASD output terminals exceeds the over speed trip setting, the ASD channel will be automatically tripped.

Question 22

Verify that there are no changes to the safety related RTP [*sic*].

Response

There are no changes incorporated in this plant modification that impact the safety function or safety related status of the EOC-RPT. The following is a summary of the operational changes to the EOC-RPT design.

One change to the EOC-RPT design was to use existing spare contacts to send a pre-trip signal to the ASDs to initiate shutdown of the ASDs in parallel with the opening of the EOC-RPT breakers. Isolation between the safety related circuits and the non-safety related ASD pre-trip signal is accomplished by using existing electrical isolation relay contacts.

A second change is related to the operating envelope (i.e., from operating only on a 60 Hz basis to a 15 - 63 Hz basis). The effects of ASD variable speed operation on EOC-RPT breaker timing is discussed in Appendix B, pages 2, 11, 12, and 18 of the Reference 2 submittal.

Currently a trip signal to the EOC-RPT breakers will reduce the pump speed to 15 Hz. Following installation of the ASD system, the EOC-RPT trip will shutdown the RRC pumps. This is similar to the BWR/4 design.

ATTACHMENT 2

Attachment 2 is a schematic diagram showing the protective devices used for the ASD system

ATTACHMENT 3

Attachment 3 is an excerpt from the ASD system Reliability Report

1.0 EXECUTIVE SUMMARY

This analysis provides the basis for the reliability evaluation of the Reactor Recirculation Adjustable Speed Drive (ASD) System and its GE-FANUC controls for the Washington Public Power Supply System (Supply System) WNP-2 plant.

Reliability analysis includes an estimate of probability that an event (e.g., failure of ASD) will occur and an assessment of the consequential effects on plant availability should it occur. It is important that the probability of occurrence of ASD System failure be low.

This analysis was performed in two phases. The first phase encompassed a Failure Modes and Effects Analysis (FMEA) for the critical ASD System components. This ASD System FMEA provided a qualitative evaluation and assessment of the critical ASD System components and the significance of their corresponding failure modes. The Parts-Count Method was used to calculate the single channel failure rate of 6.85E-05 per hour, which is considered low. This conservative approach uses random component failure rates and assumes that any single component failure will lead to a complete ASD channel failure.

The second phase was conducted using the CAFTA (Computer Aided Fault Tree Analysis) computer program that quantitatively evaluates failure probabilities, their significance and the overall system unavailability (Reference 11). Two fault trees were developed and analyzed for the GE-FANUC control logic and the entire ASD System design, respectively. Failure probabilities of 1.25E-06 and 4.26E-06 per system demand were calculated for the GE-FANUC control logic and the entire ASD System, respectively. These failure probabilities are considered low for a non-safety system, and translate into a high ASD System availability of 99.9998 and 99.9994 percent, respectively, based on a system Mean Time To Repair (MTTR) of 24 hours and five hundred ASD System demands per year.

The study concludes that both the Reactor Recirculation ASD System and the GE-FANUC control logic design provide high system availability and more than adequately meet the reliability standards based on established industry guidelines and practices for comparable non-safety systems. No credible failure modes were found that could affect WNP-2 plant safety assumptions for the LOCA, ATWS, Transient and Stability design basis analyses. Furthermore, the ASD reliability system design analyses support the 10CFR50.59 and 10CFR50.92 safety evaluations included in the WNP-2 Recirculation Pump Adjustable Speed Drive Licensing Report (Reference 1).

ATTACHMENT 4

Attachment 4 is an excerpt from the vendor field performance reliability study

Reliability Report
for
Adjustable Speed AC Drives

The best practice to determine the reliability of the power conversion and control for adjustable speed ac drives has been to accumulate field performance on operating systems. It is a more accurate and meaningful method to establish failure rate and MTBF. This has been done and the results are tabulated for each installation site for control and power devices. Each control unit is an operating power converter and control, ie a six pulse system or one channel of a dual channel 12 pulse system. Power device units are individual SCR or GTO devices, and are not included in the control unit data.

The other major components in the drive system are not included in the report. These include transformer, motor, link inductor and switchgear. There were no failures of these components in the field data submitted. Also there were no control unit failures from the redundant cooling systems.

There is a fairly wide range of failure rates in the data submitted. This might be rationalized by a number of factors:

1 - Factory quality variance
2 - User maintenance practices
3 - Reporting accuracy
4 - Operating environment
5 - Data interpretation

The notable factors from the above are:

1 - Site B was shipped in 11/88 with a new design for the electronic control module with one half the printed circuit boards as in the other sites. Site F had thyristors from a different vendor than the other sites.

2&3 - Site C submitted the most comprehensive maintenance report.

4 - Site C is installed in a control room that is not air conditioned as are the other sites. Site C had air filters to minimize dirt laden air into the force ventilated power controller.

5 - Power device failures from poor gate drive were not counted.

The failure rate and MTBF for the total experience at six sites represents a reasonably accurate measure of equipment performance to be expected - on the average. The six sites represent 15 percent of the total GE LCI and IMD drive population in service.

All of the sites except B had redundant systems, either 12 pulse dual channel or six pulse with hot standby. All sites had N + 1 thyristors and redundant cooling systems. A unit failure did not represent a drive failure on the redundant systems. The data submitted identifies four instances where the fan drive tripped. On a drive basis the failure rate was;

Unit HRS = 1408×10^3

Failures = 4

Failure rate = 2.8×10^{-6} hours

MTBF = 352,000 hours/40 years

The data submitted for Sites C and F showed the highest failure rate but had no drive trips.

In summary the failure data from operating systems in a real world environment represents an accurate and meaningful measurement of equipment performance to be expected. In the GE case, the control failure rate should decrease with the decrease in printed circuit board count and the continually increasing quality which comes with standardization.

The field performance data submitted from sites C and E included repair time. The results of this accumulated data show a MTTR (mean time to repair) of 10 hours(4 hours when parts are available). Some of the repair times exceeded 24 hours which suggests that parts were not available at the site. MTTR predictions based on parts available would be significantly lower. Again, the MTTR prediction of 10 hours represents actual experience in a real world environment which presents a meaningful measurement to use in equipment availability predictions.

Based on MTBF and MTTR the single channel availability is:

$$A = \frac{1}{1 + \frac{MTTR}{MTBF}} \times 100 = 99.97\%$$

And the drive availability for a 12 pulse dual channel or 6 pulse hot standby will be 99.997% as demonstrated in the field.

Definitions

Failure rate (lambda) = failures per million hours

MTBF = 1/lambda

Adjustable Speed AC Drive
Failure Rate Data

CONTROL

SITE	UNITS	UNIT HRS. (10^3)	FAILURES	RATE (10^{-6}HRS)	MTBF (10^3HRS/YRS)
A	4	192.7	7	36.3	27.5/3.1
B	2	57.8	0	0	-
C	10	624.0	29	46.5	21.5/2.5
D	8	455.5	9	19.8	50.5/5.8
E	22	799.8	14	17.5	57.0/6.5
F	8	461.0	21	45.6	21.9/2.5
Total	54	2590.8	80	30.9	32.4/3.7

POWER DEVICES

SITE	UNITS	UNIT HRS. (10^6)	FAILURES	RATE (10^{-6}HRS)	MTBF (10^6HRS/YRS)
A	144	6.94	1	0.144	6.9/788
B	120	1.74	0	0	-
C	504	32.38	6	0.185	5.4/616
D	432	24.6	1	0.041	24.4/2785
E	1398	49.72	1	0.020	50.0/5708
F	432	16.60	5	0.301	3.3/379
Total	3000	131.98	14	0.106	9.4/1076

ATTACHMENT 5

Attachment 5 includes excerpts from the vendor installation, maintenance, and operation manuals

TAB 2

SYSTEM PARAMETERS

Speed Range
0 - 1980 rpm. (66Hz.)

Acceleration/Deceleration

As required up to 10%/Sec within maximum drive capacity.

Environment

Altitude:	3300 feet above mean sea level
Temperature Range:	0°C to 40°C (Indoor) 50°(Outdoor)
Humidity Range:	5% to 95% relative humidity

Temperature and humidity conditions, including their relative rate of change, should be controlled such that there is no moisture condensation in or on the control equipment.

A-C Source Power

6900 volts, 3-phase, 60 hertz
Maximum steady-state voltage variation: ± %
Mva short circuit at drive source terminals: 485
Maximum frequency variation: ± 2%

Torque Requirements:

Pump curve. Load torque proportional to speed squared with maximum torque at 1980rpm at 11,200 hp.

Altitude and Temperature

All indoor equipment is suitable for operation in an ambient temperature not to exceed 40° C, 0 to 95 percent relative humidity with frequent interchange of air.

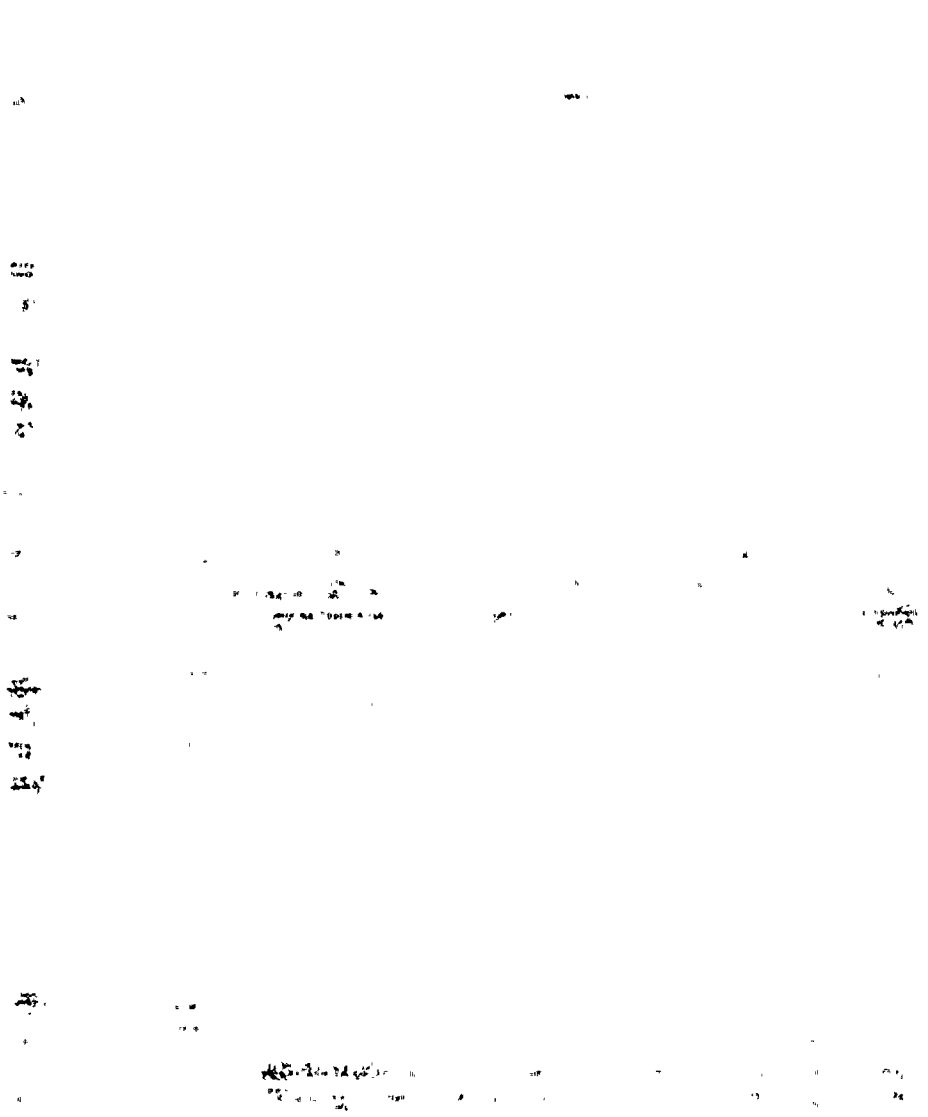
Air Quality

Ventilating air quality shall be maintained such that:

Hydrogen Chlorides do not exceed 4 PPB.
Hydrogen Sulfides do not exceed 4 PPB.
Chorines do not exceed 2 PPB.
Sulphur Dioxides do not exceed 4 PPB.
Chlorine Dioxides do not exceed 4 PPB.

Induction Motor (Existing)

Rated Power	: 8900 Horsepower
Stator Voltage	: 6600 volts, 3-phase, 60 Hz.
Synchronous Speed	: 1800 RPM
Service Factor	: 1.15
Weight (lb)	: 60,000
Wk^2 (lb-ft^2)	: 21,500
Locked Rotor	: 1200 (pump)
Load	: Pump Curve



CHAPTER 7

DIAGNOSTICS AND TROUBLESHOOTING

7-1. INTRODUCTION

Included in the drive power and electronic circuitry is a multi-layered diagnostic and troubleshooting capability. The main elements of this capability are the following:

1. Self testing of critical microcomputer system elements every time the control is reset or power applied.
2. A memory type fault monitor which displays the cause of shutdown in a printed message at the printer.
3. Lights and test points on front of cards provide the following information:

   a. Attenuated system bus voltages and currents on test points allow a check of magnitude and phasing.
   b. Gate pulse signals to converter bridge available at test points.
   c. Neon cell voltage indicating lights across each thyristor in power converters for indications of shorted cells.
   d. Overcurrent, overvoltage, and overspeed indicating lights in electronics module.
   e. Card front lights indicate status of all switching input and outputs to/from electronics module.

4. Gate-test-mode allows checkout of analog signal conditioning circuitry, microprocessor firing control, and cell gate signal integrity while off-line.
5. Serial monitor software which allows examination of system memory, inputs, and outputs (Chapter 5).
6. Capability to store diagnostic lists of system variables preceding and following fault conditions. (Chapter 4).

7-2. CONTROL SELF TEST

7-3. BASIC STRUCTURE

The self test routines are PLM86 procedures which may be executed by the HMPG resident in the Structured Control Electronics Module (SEM/MEM) to test individual PWB's and functions. These routines are executed upon power-up if the TEST switch on the NLCB is in the up position. These routines may also be run when the drive is in a non-RUN condition by operator commands received via a terminal connected to the HMPG's RS-232 port or by depressing a test switch. The function of the self test is to test most of the control panel for the Structured GTO-IMD, with great emphasis placed on the testing of the PWB's in the SEM/MEM.

Testing of the panel begins by performing tests of the hardware elements within a neighborhood of the HMPG'S microprocessor and continues to tests of increasingly remote hardware. All of the tests incorporated within the self test may be classed into 3 groups:

1. PWB-Specific tests
2. Paired PWB tests
3. Panel-level tests

7-4. PWB-SPECIFIC TESTS

A great amount of effort has been placed on performing tests that will pinpoint problems on specific PWB's first. In this manner, if any easily diagnosed problem exists, it will be clearly spelled out to the operator, instead of vaguely fined by a list of possible solutions. Testing such as these comprise the PWB-Specific test group.

7-5. PAIRED PWB TESTS

Tests which depend on the operation of several PWB's are classed within the Paired-PWB group. Diagnostic messages for failures of these tests will indicate a functional problem and also a list of possible solutions which may be general in nature.

CAUTION

Self test exercises the output relays; therefore, the output terminal boards should be disconnected from the I/O module, and/or source and load breakers should be racked-out and drive stopped.

7-6. PANEL-LEVEL TESTS

Panel-level tests also require correct operation of several PWB's or modules, however, these tests are segregated to allow the user to perform either a module-level test (involving only the control SEM/MEM) or a complete panel-level test which would include this last category of procedures. From a practical point of view, the sequence of testing within the control SEM progresses in the following manner

1. HMPG
2. HLCB
3. HAIA
4. NSFC (source-master)
5. NSFC (load)
6. NSFC (source-slave)
7. NLCB
8. NLIB (source)
9. NLIB (load)
10. HISA
11. HRDA
12. NAIF

Further tests which include PWB's outside the SEM/MEM, progress in the following sequence:

1. Cables leading from the SEM/MEM.
2. The I/O Module.

7-7. EXECUTING THE TESTS

The self-test routing may be initiated by resetting (toggle TP1 (RESET) to TP2 (DCOM) the HMPG with the TEST switch (on the NLCB) in the UP position. The entire test is completed in approx. 20 seconds. At its completion, status information will be printed out at the door-mounted printer. In the present product, the entire self-test routing is executed; however, provisions for executing small sections of the code are in place.

Upon completion of the self-test, the drive will operate in the gate-test-mode. To return to normal operation, the NLCB's test switch must be returned to the normal position and the HMPG must be reset (Toggle TP1 (RESET) to TP2 (DCOM)).

CAUTION

Self test exercises the output relays; therefore, the output terminal boards should be disconnected form the I/O module, and/or source and load breakers should be racked-out drive stopped.

NOTE

If the VBol setting at NCCD is greater than 10.5 Vdc then set down to 10.5Vdc before executing self test. Return to original setting when self test is done.

3. DIAGNOSING FAILURES

As mentioned above, failure of any of the self test procedures will produce a diagnostic message on the door-mounted printer. The format of the diagnostic message is:

DATE TIME FAILED
(aabb) DURING TEST OF: aa=TEST NUMBER
description of test bb=SUBTEST NUMBER

PROBLEM: problem statement

POSSIBLE SOLUTION:
solution 1
solution 2
solution 3

Usually, a failure can easily be diagnosed by the problem statement. At least on solution will be suggested in the print out. It is suggested that trouble-shooting be performed at the PWB level (Replace the PWB not its component). Although the diagnostic messages may indicate more specific failures, it is not recommended the PWB components be replaced or repaired (always write or attach the diagnostic to the card).

The TEST NUMBER and SUB-TEST NUMBER uniquely define a failure within the self test procedure. The TEST NUMBER is incremented from 1 to 31 (hex) as the tests progress. For different test numbers. the SUB-TEST ameter will vary from 1 up to the number of sub-test within that major test. The Description of Tests section that lows details the complete self test procedure according to the TEST NUMBER and SUB-TEST NUMBER parameters

7-8.1. Description of Tests.

The following lists all tests available with sub-test information:

TEST	DESCRIPTION
0	HMPGROMTST: Reads all of ROM memory (F000:0 to FFFF).Possible failures are:
.1	-BusHog error
.2	-Read error
1	HMPGRAMTST: Reads all of RAM memory (0:0 to 0:3FFF). Possible failures are:
.1	-BusHog error
.2	-Read error
.3	-Write error
2	HMPGINTRTST
.1	-Verifies control and data lines to HMPG's 8259
3	HMPG_TMR
.1	-Verifies addr lines & data bits 6 & 7
.2	-Verifies addr lines & data bits 6 & 7
.3	-Verifies addr lines & data bits 6 & 7
.4	-Verifies data bits 5-0 with walking 1 pattern
.5	-Verifies that all outputs are free to toggle.
.6	-FOR TMRO: Checks for null count=1
.7	-FOR TMRO: Loads TMR; checks for null count = 0
.8	-FOR TMRO: Verify TMR time out
.9	-FOR TMR1: Verify TMR reloads
.A	-FOR TMR1: Checks for null count = 1
.B	-FOR TMR1: Loads TMR; checks for null count = 0
.C	-FOR TMR1: Verify TMR time out
.D	-FOR TMR1: Verify TMR reloads
.E	-FOR TMR2: Checks for null count = 1
.F	-FOR TMR2: Loads TMR; checks for null count = 0
.10	-FOR TMR2: Verify TMR time out
.11	-FOR TMR2: Verify TMR reloads
4.	HMPG_S10_PRES
.1	-Check that USART trans and rec buffers are empty
5. .1	-Verifies software reset of STALL circuit
.2	Initiate stall timer; checks for no STALL after 100
.3	Verifies STALL asserted after 1.5 seconds.
6	HMPG_INTR
.1	- Verify operation of BusHog interrupt.
.2	- Verify that BusHog doesn't occur for legitimate read.
.3	-Verify operation of Time Tic interrupt.
7	DMPB
.1	-Checks that Write Enable Switch is not asserted.
.2	-Checks for no BusHog during EEPROM reads
.2	-Checks for expected pattern in EEPROM.
8	HLCB_PRES
.1	-Enables IMOK; checks for 0IMOK = 0
.2	-Disables IMOK;.checks for OIMOK = 0
9	HLCB_DAK
.1	Checks for no BusHog during reads of HLCB.
A	HLCB_TMR_U22
.1	-Verifies addr lines & data bits 6 & 7
.2	-Verifies addr lines & data bits 6 & 7
.3	-Verifies addr lines & data bits 6 & 7
.4	-Verifies data bits 5-0 with walking 1 pattern
.5	-Verifies that all outputs are free to toggle.
.6	-FOR TMRO: Checks for null count = 1
.7	-FOR TMRO: Loads TMR; checks for null count = 0
.8	-FOR TMR0: Verify TMR time out
.9	-FOR TMR0: Verify TMR reloads
.A	-FOR TMR1: Checks for null count = 0
.B	-FOR TMR1: Loads TMR: checks for null count = 0
.C	-FOR TMR1: Verify TMR time out
.D	-FOR TMR1: Verify TMR reloads
.E	-FOR TMR2: Checks for null count = 1
.F	-FOR TMR2: Loads TMR; checks for null count = 0
.10	-FOR TMR2: Verify TMR time out
.11	-FOR TMR2: Verify TMR reloads

TEST	DESCRIPTION
B	HLCB_TMRU23
.1	-Verifies addr lines & data bits 6 & 7
.2	-Verifies addr lines & data bits 6 & 7
.3	-Verifies addr lines & data bits 6 & 7
.4	-Verifies data bits 5-0 with walking 1 pattern
.5	-Verifies that all outputs are free to toggle.
.6	-FOR TMRO: Checks for null count = 1
.7	-FOR TMRO: Loads TMR; checks for null count = 0
.8	-FOR TMR0: Verify TMR time out
.9	-FOR TMR0: Verify TMR reloads
.A	-FOR TMR1: Checks for null count = 1
.B	-FOR TMR1: Loads TMR: checks for null count = 0
.C	-FOR TMR1: Verify TMR time out
.D	-FOR TMR1: Verify TMR reloads
.E	-FOR TMR2: Checks for null count = 1
.F	-FOR TMR2: Loads TMR; checks for null count = 0
.10	-FOR TMR2: Verify TMR time out
.11	-FOR TMR2: Verify TMR reloads
.12	-FOR TRM2: Initialize to Mode 0; verify status
.13	-FOR TMR2: Load with 10 ms, verify status.
.14	-FOR TMRS: After 4 ms, verify status.
.15	-FOR TMR2: After 15 ms, verify time out.
.16	-FOR TMR2: Check that count = 0.
C	HLCB_INTR_PRES
.1	-Verify addr and data lines to HLCB's 8259.
D	HLCB_SIO
.1	-Initialize and check status of HLCB's 8251.
.2	-Verify that single byte of data is send, by sensing status.
.3	-Verify transfer of data pattern.
E	HAIA_DAK
.1	-Checks for no BusHog during reads of HAIA.
.2	-Checks for no BusHog during writes to HAIA.

TEST	DESCRIPTION
F	HAIA_PRES
.1	-Checks that HAIA is present by reading single bit.
10	HAIA_TMR
.1	-Verifies addr lines & data bits 6 & 7
.2	-Verifies addr lines & data bits 6 & 7
.3	-Verifies addr lines & data bits 6 & 7
.4	-Verifies data bits 5-0 with walking 1 pattern
.5	-Verifies that all outputs are free to toggle.
.6	-FOR TMRO: Checks for null count = 1
.7	-FOR TMRO: Loads TMR; checks for null count = 0
.8	-FOR TMR0: Verify TMR time out
.9	-FOR TMR0: Verify TMR reloads
.A	-FOR TMR1: Checks for null count = 1
.B	-FOR TMR1: Loads TMR; checks for null count = 0
.C	-FOR TMR1: Verify TMR time out
.D	-FOR TMR1: Verify TMR reloads
.E	-FOR TMR2: Checks for null count = 1
.F	-FOR TMR2: Loads TMR; checks for null count = 0
.10	-FOR TMR2: Verify TMR time out
.11	-FOR TMR2: Verify TMR reloads
11	HAIA_CONVERSION
.1	-Start A/D conversion; check that BUSY = 1.
.2	-Check that IDAVAL = 0
.3	-Wait for conversion to complete; check that BUSY = 0.
.4	-Check that IDAVAL = 1.
12	HAIA_PSUPPLY
.1	-Check that N15 supply is read correctly.
.2	-Check that P15 supply is read correctly.
13	NSFC_S_PRES
.1	Set IMOK true; read back IMOK signal.
.2	Set IMOK false; read back IMOK signal.
14	NSFC_S_TMR_PRES
.1	-Verifies addr lines & data bits 6 & 7
.2	-Verifies addr lines & data bits 6 & 7
.3	-Verifies addr lines & data bits 6 & 7
.4	-Verifies data bits 5-0 with walking 1 pattern
.5	-Verifies that all outputs are free to toggle.

TEST	DESCRIPTION
15	NSFC_S_TMODE
.1	-FOR TMRO: Checks for null count = 1
.2	-FOR TMRO: Loads TMR; checks for null count = 0
.3	-FOR TMR0: Verify TMR time out
.4	-FOR TMR0: Verify TMR reloads
.5	-FOR TMR1: Checks for null count = 1
.6	-FOR TMR1: Loads TMR; checks for null count = 0
.7	-FOR TMR1: Verify TMR time out
.8	-FOR TMR1: Verify TMR reloads
.9	-perform operations to set pulse train to 0; verify
.A	-In TEST Mode, write all on pattern, expect echo of same.
.B	-In TEST Mode, walk 1 thru primary & firing latch.
.C	-In TEST Mode, see if pulse train is stuck low.
.D	-In TEST Mode, see if pulse train is stuck high.
.E	-In TEST Mode, check that pulse train is toggling.
16	NSFC_L_PRES
.1	-Set IMOK true; read back IMOK signal.
.2	-Set IMOK false; read back IMOK signal.
17	NSFC_L_TMR_PRES
.1	-Verifies addr lines & data bits 6 & 7
.2	-Verifies addr lines & data bits 6 & 7
.3	-Verifies addr lines & data bits 6 & 7
.4	-Verifies data bits 5-0 with walking 1 pattern
.5	-Verifies that all outputs are free to toggle.
18	NSFC_L_TMODE
.1	-FOR TMRO: Checks for null count = 1
.2	-FOR TMRO: Loads TMR; checks for null count = 0
.3	-FOR TMR0: Verify TMR time out
.4	-FOR TMR0: Verify TMR reloads
.5	-FOR TMR1: Checks for null count = 1
.6	-FOR TMR1: Loads TMR; checks for null count = 0
.7	-FOR TMR1: Verify TMR time out
.8	-FOR TMR1: Verify TMR reloads
.9	-perform operations to set pulse train to 0; verify
.A	-In TEST Mode, write all on pattern, expect echo of same.
.B	-In TEST Mode, walk 1 thru primary & firing latch.
.C	-In TEST Mode, see if pulse train is stuck low.
.D	-In TEST Mode, see if pulse train is stuck high.
.E	-In TEST Mode, check that pulse train is toggling.
19	NSFC_SRC_SLAVE_PRES
.1	-Set IMOK true; read back IMOK signal.
.2	-Set IMOK false; read back IMOK signal.
1A	NSFC_SRC_SLAVE_TMR_PRES
.1	-Verifies addr lines & data bits 6 & 7
.2	-Verifies addr lines & data bits 6 & 7
.3	-Verifies addr lines & data bits 6 & 7
.4	-Verifies data bits 5-0 with walking 1 pattern
.5	-Verifies that all outputs are free to toggle.
1B	NSFC_SRC_SLAVE_TMODE
.1	-FOR TMRO: Checks for null count = 1
.2	-FOR TMRO: Loads TMR; checks for null count = 0
.3	-FOR TMR0: Verify TMR time out
.4	-FOR TMR0: Verify TMR reloads
.5	-FOR TMR1: Checks for null count = 1
.6	-FOR TMR1: Loads TMR; checks for null count = 0
.7	-FOR TMR1: Verify TMR time out
.8	-FOR TMR1: Verify TMR reloads
.9	-Perform operations to set pulse train to 0; verify
.A	-In TEST Mode, write all on pattern, expect echo of same.
.B	-In TEST Mode, walk 1 thru primary & firing latch.
.C	-In TEST Mode, see if pulse train is stuck low.
.D	-In TEST Mode, see if pulse train is stuck high.
.E	-In TEST Mode, check that pulse train is toggling.
1C	NSFC_S_PLL
.1	-FOR TMR2: Enables PLL; checks for null count = 1.
.2	-FOR TMR2: Loads TMR; checks for null = 0

TEST	DESCRIPTION
.3	-FOR TMR2: Verify TMR time out.
.4	-FOR TMR1: Verify TMR reloads.
1D	NSFC_L_PLL
.1	-FOR TMR2: Enables PLL; checks for null count = 1.
.2	-FOR TMR2: Loads TMR; checks for null = 0
.3	-FOR TMR2: Verify TMR time out.
.4	-FOR TMR1: Verify TMR reloads.
1E	NSFC_SRC_SLAVE_PLL
.1	-FOR TMR2: Enables PLL; checks for null count = 1.
.2	-FOR TMR2: Loads TMR; checks for null = 0
.3	-FOR TMR2: Verify TMR time out.
.4	-FOR TMR1: Verify TMR reloads.
1F	ROLL_CALL
.1	-Test for ribbon cable connecting HAIA-(JA) to SEM(JG)
.2	-Enable NLCB IMOK; check for IMOK true.
.3	-Disable NLCB IMOK; check for IMOK false.
.4	-Enable NLIBS IMOK; check for IMOK true.
.5	-Disable NLIBS IMOK; check for IMOK false.
.6	-Enable NLIBL IMOK; check for IMOK true.
.7	-Disable NLIBL IMOK; check for IMOK false.
20	NLCB_DIFF_AMPS
.1	-Test for 0 volts at REFO.
.2	-Test for 0 volts at TREFO.
.3	-Test for 0 volts at 12PREFO.
.4	-Inject current in REFO circuit; test for change in output.
.5	-Inject current in TREFO circuit; test for change in output.
.6	-Inject current in 12PREFO circuit; test for change in output.
.7	-Test for 0 volts at SPD (speed).
.8	-Reset existing faults; test for IOSP (over-speed) = 0.

TEST	DESCRIPTION
21	HLCB_SQ_WAVES
.1	-Check for absence of square waves with oscillator off.
.2	-Check for any square waves with oscillator on.
.3	-Check for source VA, VB, VC square waves. Check for any source flux waves.
.4	-Check for SRC VA flux wave.
.5	-Check for SRC VB flux wave.
.6	-Check for SRC VC flux wave.
.7	-Check SRC phase sequence.
.8	-Check for load VA, FB, VC square waves. Check for any source flux waves.
.9	-Check for load VA flux wave.
.A	-Check for load VB flux wave.
.B	-Check for load VC flux wave.
.C	-Check load phase sequence.
22	NLIB_S_ANALOG
.1	-Reset existing faults; verify UV & not OV condition.
.2	-Verify not SUPPression condition.
.3	-Verify 1UV70 = 0.
.4	-Test C17 for time delay. (Overvoltage circuit).
.5	-Test C17 for time delay. (Overvoltage circuit).
.6	-Test for 0 volts at IFBS.
.7	-Test for 0 volts at FLUX BAS.
.8	-Inject current in source current condition circuit. Detect change in IFBS.
.9	-Detect change in FLUX BAS.
.A	-For FLUX BAS: Check level of positive offset.
.B	-For FLUX BAS: Check level of positive peak
.C	-For FLUX BAS: Check level of negative peak.
23	NLIB_L_ANALOG
.1	-Reset existing faults; verify UV & not OV condition.
.2	-Verify not SUPPression condition.
.3	-Verify 1UV70 = 0.
.4	-Test C17 for time delay. (Overvoltage circuit).
.5	-Test C17 for time delay. (Overvoltage circuit).
.6	-Test for 0 volts at IFBL.

TEST	DESCRIPTION
.7	-Test for 0 volts at FLUX BAL.
.8	-Inject current in source current condition circuit. Detect change in IFBL.
.9	-Detect change in FLUX BAL.
.A	-For FLUX BAL: Check for 0 volts dc offset.
.B	-For FLUX BAL: Check level of positive peak
.C	-For FLUX BAL: Check level of negative peak.
.D	-For FLUX CBL: Check for 0 volts offset.
.E	-For FLUX CBL: Check level of positive peak.
.F	-For FLUX CBL: Check level of negative peak.
.10	-For FLUX ACL: Check for 0 Volts dc offset.
.11	-For FLUX ACL: Check level of positive peak.
.12	-For FLUX ACL: Check level of negative peak.
.13	-Turn off TST2 signal, verify 10LTCH is 1 (latched).
.14	-Verify 1KILLLD = 1.
.15	-Reset faults, verify 10VLTCH is 0.
.16	-Verify 1KILLLD = 0.
24	NCCD_ANALOG
.1	-Verify 1GNDF2 = 0.
.2	-Verify 0IFLT = 1.
.3	-Verify 10VLTCB = 0.
.4	-Verify 1KILLD = 0.
.5	-Verify 1CAPFLT = 0.
.6	-Verify 0CIBERR = 1.
.7	-Verify IFB(-) is approximately 0.0 VDC.
.8	-Take OTST1 low, verify OIFLT is still 0IFLT IS 0.
.A	-Verify 1GNDF2 is 0.
.B	-Verify 0CIBERR is 0.
.C	-Turn off source current, verify 0IFLT is 1.
.D	-Verify 1GNDF2 is 0.
.E	-Verify 0CIBERR is 1.
.F	-Turn on load current signal, verify 0IFLT is 0.
.10	-Turn off load current, verify 0IFLT is 1. Also set 0TST1 high.
.11	-Turn off TST2 signal, verify 10VLTCH is 1.
.12	-Verify 1KILLLD = 1.
.13	-Turn off TST2 signal, verify 10VLTCH is 1 (latched).
.14	-Verify 1KILLLD = 1.
.15	-Reset faults, verify 10VLTCH is 0.
.16	-Verify 1KILLLD = 0.
25	HMPG_INTR
.1	-Enable test oscillator; verify occurrence of source zero crossing interrupt (slave intr 0).
.2	-Verify frequency of source zero crossing intr.
.3	-Enable test oscillator; verify occurrence of load zero crossing interrupt (slave intr 1).
.4	-Verify frequency of load zero crossing intr.
.5	-Verify occurrence of source firing interrupt.
.6	-Verify occurrence of load firing interrupt.
26	NLCB_SPEED
.1	-Enable test oscillator; verify speed circuits reads 55 Hz.
.2	-Verify no overspeed condition.
27	HISA_PRES
.1	-Disable IMOK; verify by reading back bit.
.2	-Enable IMOK; verify by reading back bit.
28	CABLE_CONT
.1	-Tests for continuity in ribbon cable from SEMJA to I/O Module.
.2	-Tests for continuity in ribbon cable from SEM, JK to I/O Module.
.3	-Tests for continuity in ribbon cable from SEM, JH to I/O Module.
.4	-Tests for continuity in ribbon cable from SEM, JB to Door Module.
29	HISA_IO
.1	-Set all inputs from I/O Module high; verify by reading back inputs to HISA.
.2	-Set all inputs from I/O Module low; verify by reading back inputs to HISA.
2A	NCCD_XDCD_FDBK_OK
.1	-Check #DDCDS in XDCD against EEPROM variable XDCD configuration E.

TEST	DESCRIPTION
.2	-Check CPS is OK - have output voltage
.3	-Check that GTO gate drivers are in "off" position.
2B	HMPG_INTERRUPT 7
.1	-Check master interrupt 7
2C	Load NSFC Pulse train
.1	-Check load side NSFC pulse train.
2D	P105_SUPPLY
.1	-Check that 105 volt dc power supply is OK.
2E	HROA_1A_IO -In sequence, pick-up single relays on the HROA in slot 1A of the I/O module. Expect feedback signal to indicate change.
.1	-Force all HROA(1A) relays to drop-out; verify by feedback.
.2	-Force 105 Vdc relays to pick-up; verify by feedback.
.3	-Drop out 105 Vdc relays, wait 40 ms, verify by feedback.
.4	-Pick-up single 28 V relay; verify by feedback.
.5	-Drop-out all relays; verify by feedback.
.6	-Pick-up single 28 V relay; verify by feedback.
.7	-Drop-out all relays; verify by feedback.
.8	-Pick-up single 28 V relay; verify by feedback.
.9	-Drop-out all relays; verify by feedback.
.A	-Pick-up single 28 V relay; verify by feedback.
.B	-Drop-out all relays; verify by feedback.
2F.	HROA_1B_IO: In sequence, pick-up single relays on the HROA in slot 1B of the I/O module. Expect feedback signal to indicate change.
.1	-Force all HROA(1A) relays to drop-out; verify by feedback.
.2	-Force 105 Vdc relays to pick-up; verify by feedback.
.3	-Drop out 105 Vdc relays, wait 40 ms, verify by feedback.
.4	-Pick-up single 28 V relay; verify by feedback.
.5	-Drop-out all relays; verify by feedback.
.6	-Pick-up single 28 V relay; verify by feedback.
.7	-Drop-out all relays; verify by feedback.
.8	-Pick-up single 28 V relay; verify by feedback.
.9	-Drop-out all relays; verify by feedback.
.A	-Pick-up single 28 V relay; verify by feedback.
.B	-Drop-out all relays; verify by feedback.
.C	-Pick-up single 28 V relay; verify by feedback.
.D	-Drop-out all relays; verify by feedback.
.E	-Pick-up single 28 V relay; verify by feedback.
.F	-Drop-out all relays; verify by feedback.
30	NLCB_R_DVR
.1	-Verify presence of HROA in slot 1B of I/O module.
.2	-Verify presence of HROA in slot 1A of I/O Module.
.3	-Force relay drivers on NLCB on; verify response from I/O Module via feedback
.4	-Force relay drivers on NLCB on; verify response from I/O Module via feedback
31	DOOR_MOD_PRES
.1	-Test for CTS asserted.
.2	-Test for DSR asserted.
32	NAIF_DAK
.1	-Checks for no BUSHOG during reads of NAIF.
33	NAIF_A_TO_BUSY_OK
.1	-Verify not busy
.2	-Convert and verify busy
.3	-Wait 1 second, verify not busy
34	NAIF_A_TO_D_OK
.1	-Input 5.082 $\pm$30mVdc, reading should be between 4.952 and 5.212
.2	-Input 2.503 $\pm$30mVdc, reading should be between 2.373 and 2.633
.3	-Input 0.0 $\pm$030mVdc, reading should be between -0.130 and 0.130
.4	-Input -2.498 $\pm$30mVdc, reading should be between -2.628 and -2.368

TEST DESCRIPTION

.5 -Input -4.999 ±30mVdc, reading should be between -5.129 and -4.869

35 NAIF_D_TO_OK

.1 Check D/A I, Input voltages as outline on 1E .1 to .5 and check for d/a conversion by A/D that already checked.

.2 Check D/A 2

.3 Check D/A 3

.4 Check D/A 4

.5 Check D/A 5

.6 Check D/A 6

.7 Check D/A 7

.8 - Check D/A 8

After the microcomputers have successfully powered up and/or self-test operations have finished successfully, the printer can then display faults/alarms as described below.

7.9 FAULT/ALARM MONITOR

Built into the electronics software module are fault/alarm monitors.

7-10 FAULT DETECTION

In the event of a fault condition, the IMD will shut down and a fault indication will appear on the SEM/MEM. The cause of the shutdown will be displayed on the printer terminal located on the control panel door. If more than one fault has occurred, the fault finder will store and print the subsequent faults (up to 10 total).

To reset the control after a fault condition, it is necessary to press the reset switch on the HLCB card in the SEM/MEM or the reset pushbutton on the control panel door. But first record the fault/alarm/relay status, and I/O states. If the fault condition is clear, the fault light will go out after a door reset, and stay out when the reset is completed.

Consult the system elementary ladder diagram for a complete list of faults. Most of the faults are standard and are defined in the following paragraphs, along with suggested corrective action.

MASTER SLAVE UNBALANCE - Indicates that there is an unbalance between the torque or excitation current commands for the two channels of a dual channel drive. See TORQUE, EXCITATION COMMAND UNBALANCE alarms for details. This fault is an optional feature selected by setting bit 10 of tuneup SQOPT2 to a "1".

COOLANT PRESSURE LOW OR PUMP LOSS - Indicates low differential coolant pressure across power converter bridges or loss of both pump starters for an excessive time period. In the absence of other indications check for presence of pump power, that pumps are rotating, and check operation of differential pressure switch.

SOURCE LOW LINE - Indicates that the source voltage has dropped below 70% of nominal for an excessive period of time. This function will also detect single phasing of the source. Time limit is set by protective tuneup parameter PTSUVT. Investigate reason for loss of voltage.

LINK OVERVOLTAGE - Indicates an overvoltage across the load dc bus. Overvoltage is set by pot VBOL on the

NCCD card and the feedback is derived from the load bridge attenuators on the NATL board. This alarm indicates that the dc link has been interrupted while there is still current in the link inductor. This can happen due to simultaneous turn off of all GTOs, an open circuit in the inverter bridge, or an open circuit in the ac buses to the motor.

The following should be checked:

1) Perform control self test.

2) Perform gate test mode to insure that all GTO gating signals are present.

3) Check for loose bus or cable connections in the bridges, dc inductor circuit, capacitor panel, and all output power cables.

4) Check for proper wipe or open poles on the output breaker / contactor, if supplied.

SOURCE-OVERCURRENT, SOURCE BACKUP OVERCURRENT - Indicates an overcurrent as detected by the source bridge accts. These faults are symptoms of many possible failures. The backup overcurrent is a hardware protective backing up the software overcurrent protective. The current feedback signals and the hardware overcurrent detectors are located on the NLIB boards in the electronics module. Check all SCRs and GTOs for shorts, perform control self test, and perform gate test.

LOAD OVERCURRENT, LOAD BACKUP OVERCURRENT - Same as above except detected from inverter bridge accts.

SOURCE, LOAD PLL - Indicates that the source or load phase locked loop has lost lock with the source or load voltages, respectively. The source and load PLLs operate from crossovers of the source and load integrated terminal voltages (flux). This failure is most often caused by a failure in the voltage feedback attenuator circuits in the bridges. Perform control self test, gate test, check NATL attenuator boards for open connectors or resistors, and check continuity of associated circuits.

STACK OVERFLOW - Indicates that the microprocessor is unable to complete its interrupt driven operations in a normal amount of time, resulting in excessive stack buildup. Proceed as for MICROPROCESSOR ALARM.

SOURCE DIFF CURRENT - On drives with a series 12 pulse source, this fault indicates an unbalance between the source bridge currents. Since the bridges are in series their currents should be balanced at all times. Perform self test, perform gate test, check for shorted SCRs, and check acct circuits for open wires or connectors.

SOURCE OVERVOLTAGE - Indicates source voltage is excessive (threshold typically set at 1.2 p.u.). Investigate reason for excessive voltage. If no reason found, perform control self test.

P70 GATING SUPPLY UNDERVOLTAGE - Indicates loss of 70 volt gating supply for source bridge(s) or a blown fuse in one of the HPTK gating boards. Output of P70 supply should be approximately 85 vdc when drive is not running. Check HPTK fuses and input / output fuses for 70 volt gating supply.

P105 SUPPLY UNDERVOLTAGE - Indicates loss of 105 vdc supply for i/o module contact input circuits. Check voltage at i/o module, check for external shorts in field wiring, and replace the 105 vdc supply (on i/o module) if necessary.

LOAD OVERVOLTAGE - Indicates excessive output voltage (threshold typically set at 1.2 p.u.). Perform self test and recheck tuneup settings.

OVERSPEED - Actually an indication of overfrequency derived from the hardware "speed" circuitry on the NLCB board. The NSFC and NLIB boards are involved as well. Normally set to 1.05 p.u. of maximum drive frequency. Perform self test. If overspeed occurs at start up from rest, it is likely to be due to defective load attenuator circuits.

GROUND FAULT - Indicates a ground somewhere between (and including) the source isolation transformer and the ac output buses (including the motor if there is no output transformer). May also indicate a failed output ac bus attenuator. A shorted capacitor may also result in an indication of a ground fault. Check each phase of capacitor bank for shorts. If none of the above, megger transformer, bridges, dc link inductor, and output ac buses.

COOLANT TEMPERATURE HIGH OR H/E BLOWER LOSS - Indicates one or both of the following:

1) The coolant temperature has exceeded the fault level, normally set to 158 degrees Fahrenheit.

2) Heat exchanger fan(s) have failed (on a liquid to air heat exchanger) or the heat exchanger fan(s) are no longer running.

For systems with air cooled heat exchangers, check that cooling fans are operating and that heat exchanger is not blocked. For systems with liquid to liquid heat exchangers, check for adequate service (cooling) water flow.

COOLANT RESISTANCE - Indicates that the coolant resistivity has dropped to a critically low level. Resistivity fault level is normally set at .2 megohm - centimeter. Replace mixed bed deionizer filter, run cooling system until resistivity increases above .2 megohm - cm, and restart drive.

COOLANT LEVEL - Indicates that coolant is below the low level float switch in the coolant reservoir. Add coolant and check for leaks.

CHOPPER PS UNDERVOLTAGE OR P28 LOW - Indicates 120 vac, 400 Hz output from the chopper power supply or the 28 vdc from the electronic module supply is low for an excessive time (software set, not adjustable). Check chopper supply input voltage, output voltage, and protective fuses. Note that failure of the chopper circuit on the NHFA board can result in low output voltage, especially under load. Check P28 volt bus on electronic module power supply. Since this supply is unregulated, the power supply transformer adjustment tap should be set to give the maximum output voltage (approximately 31 vdc).

XDCD CONFIGURATION ERROR - Indicates a mismatch between the number of GTOs programmed into DRVCFG setting and the analog signal returned from the XDCD board (on control panel sidewall) to the NCCD board indicating the number of GTO gate driver circuits per bridge leg. Perform self test and check that the number of GTOs programmed into DRVCFG is correct.

SOURCE REVERSE PHASE SEQUENCE - Indicates incorrect phase sequence as sensed on source bridge ac buses. Depends on voltage feedback signals from the source attenuators beginning with the NATL board in the source bridge.

DESYNC FAILURE - On drives with synchronize / bypass capability, this fault indicates that the bypass breaker / contactor has failed to open when commanded to do so during a transfer from across the line to variable speed operation (de-synchronization).

GTO GATE DRIVER FAULT - Indicates failure of a GTO or GTO gate driver in the load bridge. Observe LEDs on the XDCD card on the control panel sidewall and the red LEDs on the GTO gate drivers to locate the failed unit(s). Check GTOs for shorts with a DVM. If any shorted GTOs are found, check the associated snubber diodes for shorts. If no shorted GTOs are found, check fiber optic cables / connections and / or change out gate driver cards, and perform self test.

7-11. ALARM DETECTION

Alarms are conditions which are cause for concern but which do not warrant immediate shutdown of the drive but should be investigated as soon as possible. A composite alarm signal is generally supplied to operate a light on the control panel door, a remote annunciator supplied by the user, or both.

Some of the alarms will vary from one installation to the next, so the software ladder diagram section of the system elementary must be consulted for a complete list of. The following alarms are standard (if applicable) and so will be defined here.

ALARMS:

USER DEFINED ALARM - Indicates an alarm condition from a user defined interlock. Not always supplied or used.

COOLANT PRESSURE LOW OR PUMP LOSS - Indicates low differential coolant pressure across power converter bridges or loss of both pump starters. In the absence of other indications check for presence of pump power, and check operation of differential pressure switch in pump panel.

LOSS OF START PERMISSIVE - This is an optional alarm indication that the start permissive contact supplied by the user is open.

I/O ADDRESSING PROBLEM - Indicates that memory or i/o associated with the microprocessor has failed to respond when addressed. Can also be caused by inadvertent user input of a non existent memory location from the terminal. Perform self test of drive at the earliest convenience. If the problem is not identified by the self test, begin systematic substitution of digital boards one at a time.

MICROPROCESSOR INTERRUPT - Indicates that an improper interrupt of the microprocessor has occurred. Perform self test of drive at the earliest convenience. Check equipment for loose connections, arcing or other abnormal sources of electrical noise. If the problem is not identified otherwise, begin systematic substitution of digital boards in the following order: VRSA (HMPG/DMPB/PROMS), HLCB, NSFC, HAIA.

LOSS OF SPEED CONTROL - Indicates that speed is not following the speed reference. This usually occurs because the drive is overloaded and in current limit. If this is the case, reduce load. If the overload was temporary, reset and continue.

GTO GATE DRIVER ALARM - Indicates failure of a GTO or GTO gate driver in the load bridge. Observe LEDs on the XDCD card on the control panel sidewall and the red LEDs on the GTO gate drivers in the load bridge to locate the failed unit(s). Check GTOs for shorts with a DVM. If any shorted GTOs are found, check the associated snubber diodes for shorts. If no shorted GTOs are found, check fiber optic cables / connections and / or change out gate driver cards, and perform self test.

LOSS OF SPEED REFERENCE - Indicates that the 4-20 ma speed reference has gone below 4 ma. If the 4-20 ma reference circuit is used with a 2-10 volt reference, this alarm indicates that the reference has gone below 2 volts. Check continuity of the external (user) reference circuit. Perform self test of drive at the earliest convenience. If the problem is not identified by the self test, begin systematic substitution of boards one at a time, starting with the NLCB board.

GTO FREEZE - Indicates a condition resulting in a momentary protective "freeze" or halt of GTO firing. (If GTOs are gated off at a current higher than their rating, they will fail.) The "freeze" circuit is located on the NCCD board in the electronics module. A "freeze" is caused by one of three conditions:

1) An overcurrent condition, threshold set by the OVRI pot on the NCCD board. Currents from both source and load accts are checked against the OVRI setting.

2) Low chopper power supply voltage as sensed on the NCCD board. In this case low chopper supply voltage alarm might also be reasonably expected.

3) Low P28 vdc bus from the PSFF power supply module.

To troubleshoot this condition, follow steps given for SOURCE OVERCURRENT and LOAD OVERCURRENT faults. Check if P28 vdc bus is low. Check that chopper supply output voltage is 120 - 130 vac.

BRIDGE FILTER FUSE - Indicates that protective fuses for 2kv source bridge ac bus MOVs are blown. Not applicable to drives with a 4kv source bridge. Check fuses at the earliest convenience.SOURCE LINE DIP - Indicates a momentary dip of the source voltage to less than 70% of nominal. Investigate reason for loss of voltage, reset, and continue.

SOURCE LINE DIP - Indicates a momentary dip of the source voltage to less than 70% of nominal. Investigate reason for loss of voltage, reset, and continue.

LOSS OF RUN PERMISSIVE - This is an optional alarm indication that the run permissive contact supplied by the user is open.

BAD EEPROM INITIALIZATION - Indicates that an attempted download of data from PROM to EEPROM has failed. This is checked only during a hard reset or power up and when test point TIN0 on the HLCB board is tied to DCOM to initiate a download.

Upon receipt of this alarm while attempting a download of EPROM to EEPROM, check the following:

1) Check that the write enable switch on the microprocessor daughter board DMPB is on.

2) Perform a control self test.

COOLANT TEMPERATURE HIGH OR H/E BLOWER LOSS - Indicates one or both of the following:

1) The coolant temperature has exceeded the alarm level, normally set to 140 degrees Fahrenheit. When this happens, the backup heat exchanger fan, if supplied, will normally come on.

2) A heat exchanger fan has failed resulting in a switchover to the backup fan, if supplied.

For systems with air cooled heat exchangers, check that cooling fans are operating and that heat exchanger is not blocked. For systems with liquid to liquid heat exchangers, check for adequate service (cooling) water flow.

COOLANT RESISTANCE LOW - Indicates that the coolant resistivity has decreased below the alarm level of 1 megohm - centimeter. Replace mixed bed deionizer filter as soon as possible.

SYNCH TRANSFER FAILURE - On drives having synchronize / transfer across the line capability, this alarm indicates that the bypass breaker / contactor has not closed within the allocated time limit after being commanded to close by the drive. The time delay is the sum of tuneup settings SYBCP and SYBCA.

In the event of this alarm, check the following:

1) Check that the bypass breaker / contactor is racked in, has control power available, and all its close permissives are met.

2) Check that the close bypass relay (CBC) in the drive control panel is picking up.

3) Check continuity of the circuit between the CBC interlock and the bypass breaker / contactor.

4) Check that the status interlock (52A) back from the bypass breaker / contactor is functioning properly and check continuity of the circuit back to the drive control.

SYNCHRONIZING MATCH FAILURE - On drives with synchronize / transfer across the line capability, this alarm indicates that the drive has failed to synchronize / transfer within the allocated time limit. Time is set by tuneup SQT7.

In the event of this alarm, check the following:

1) Check that drive is not overloaded / in current limit and thus unable to reach top speed.

2) Check that incoming line voltage is not low.

P70 GATING SUPPLY VOLTAGE DIP - Indicates a temporary dip of 70 volt gating supply for the source bridge SCR firing circuits. An undervoltage detector is built into each of the HPTK gating boards in the source bridge. Unless this alarm is followed up by a GATING SUPPLY UNDERVOLTAGE FAULT, it is probably due to a control power dip. The appropriate action in this case is to reset and continue.

TORQUE COMMAND UNBALANCE - On dual channel drives, the torque command from the "A" channel (master) speed regulator is sent as a torque reference to the "B" channel (slave) as a +/- 10 volt analog signal. The "B" channel performs an a/d conversion on the torque signal so that it can be used by the digital control. The digitized signal is also converted-back to analog +/- 10 volt and sent back to the "A" channel (master). The master digitizes the returned signal and compares it with the signal being sent. If there is a mismatch of more than 100 counts (.1 PU), an alarm is generated.

In the event this alarm is generated, the following checks should be made:

1) Perform self test of both channels at the earliest convenience.

2) Check continuity of interconnecting wiring between drive channels.

3) Check for loose ribbon cable connectors on electronics module and i/o module.

Replace the NISA card in the electronics module.

EXCITATION COMMAND UNBALANCE - Same as TORQUE COMMAND UNBALANCE except that the signal is the command for motor excitation (magnetizing) current originating from the "A" channel (master) flux regulator.

MOTOR OVERTEMPERATURE - This is an optional alarm indication of motor overtemp from an externally supplied monitor.

CHOPPER POWER SUPPLY VOLTAGE DIP - Indicates 120 vac, 400 Hz output from the chopper power supply or the 28 vdc from the electronic module supply is low. Check chopper supply input voltage, output voltage, and protective fuses. Note that failure of the chopper circuit on the NHFA board can result in low output voltage, especially when under load. Check P28 volt bus on electronic module power supply. Since this supply is unregulated, the power supply transformer adjustment tap (located in the power supply) should be set to give the maximum output voltage (approximately 31 vdc).

7-12. GATE-TEST-MODE

7-12.1. General. The gate test mode allows off-line testing of much of the analog signal conditioning, microprocessor firing control, and gate pulse generation circuitry. In the gate-test-mode,a local test oscillator supplies 3 phase, approximately 60 Hz signals in place of the attenuated bus signals from the source and load bridges. The electronic control can then lock onto these signals and generate signals to "dry fire" the thyristors in both bridges. Thyristor gate pulses may then be examined for proper magnitude and phasing. Firing may be adjusted between advance and retard limit for each bridge. In the gate-test-mode, the control produces pulse train firing.

To perform the following tests, a dual channel oscilloscope with voltage probes and a current probe is required.

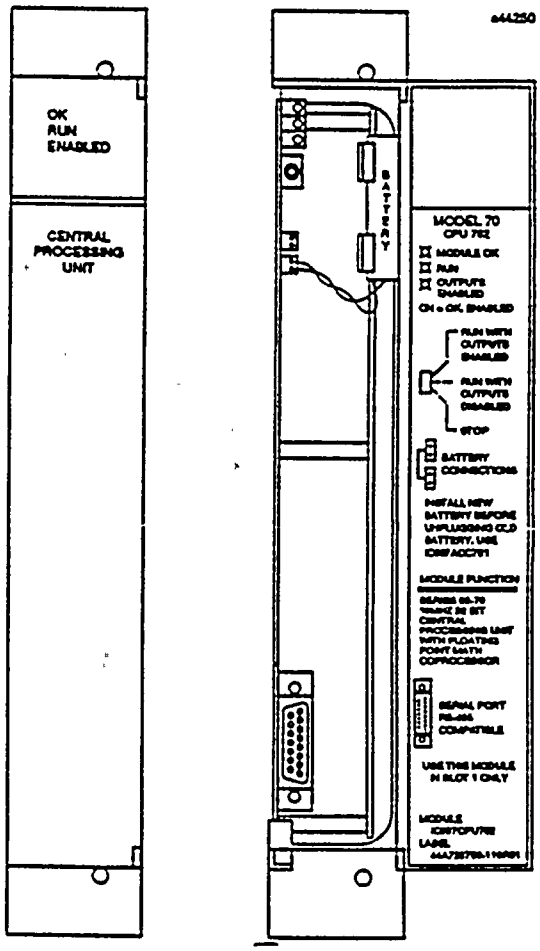
Series 90™-70
Programmable Controller

GFK-0555
September, 1990

Central Processing Unit, 32-Bit, 16 MHz
Expandable, Floating Point
IC697CPU782

Features

- Supports floating point calculations.
- Single slot CPU.
- 12K inputs and outputs (any mix).
- Up to 8K analog I/O.
- 0.4 microseconds per boolean function.
- 16 MHz, 80386DX microprocessor.
- Supports Genius™ and Series 90-70 I/O.
- Programmed by Logicmaster™ 90.
- Supports up to 512 Kbytes of battery-backed expansion memory in the same slot.
- Configurable data and program memory.
- Battery-backed calendar clock.
- Three position operation mode switch.
- Password controlled access.
- Three status LEDs.
- Software configuration (No DIP switches or jumpers).
- Reference information inside front door.



Functions

The CPU 782 is a single slot PLC CPU which allows floating point calculations. The CPU 782 is programmed and configured by Logicmaster 90 programming software to perform real time control of machines, processes and material handling systems.

The CPU 782 communicates with I/O and smart option modules over the rack mounted backplane (IC697CHS750, 790, 791) by way of the VME C.1 Standard format.

Supported option modules include GEnet LAN, Programmable Coprocessor, Access 90™ Display Coprocessor, Graphics Display Coprocessor, Genius I/O Bus Controller, and all Series 90-70 discrete and analog I/O modules. Program and data memory for the CPU 782 is available by the attachment of an expansion memory board with either 128, 256 or 512 Kbytes battery-backed CMOS RAM.

Operation of this module may be controlled by the three position switch or remotely by an attached programmer and Logicmaster 90 software. The status of a CPU is indicated by the three green LEDs on the front of the module.

Installation

- Installation should not be attempted without referring to the Series 90-70 PLC Installation and Operation Manual (See Reference 5).
- Align the expansion memory and CPU connectors.
- Align the captive screws on the memory board with the standoffs already installed on the CPU.
- Push the memory board onto the CPU connector ensuring the mating screws remain aligned with their respective standoff.
- Screw each memory board screw into the standoffs with a #1 Phillips screwdriver, firmly tightening each.
- Connect the battery to either of the battery connectors on the module.
- Put toggle switch in the STOP position.
- Make sure rack power is off.
- Install in slot 1 of rack 0. (See Figure 1)
- Turn on power.

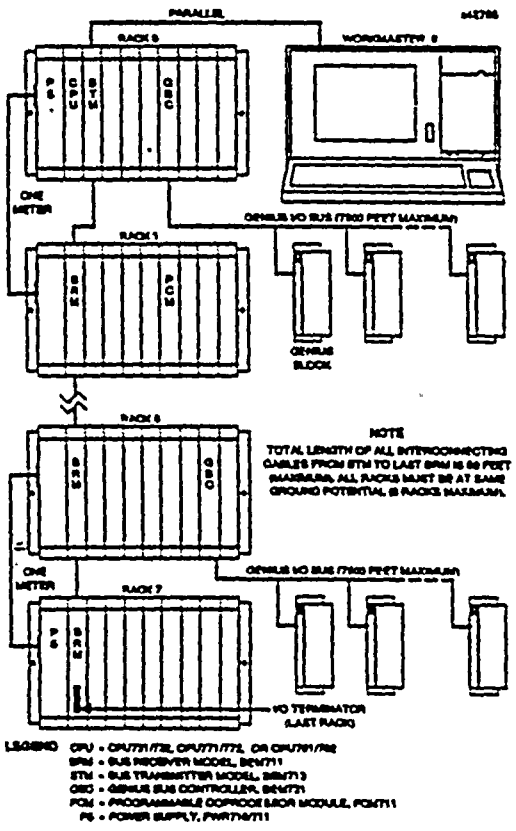


Figure 1. Series 90-70 PLC System Diagram

The module should power up and blink the top LED. When the diagnostics have completed successfully, the top LED stays on and the middle and bottom LEDs are off. The CPU is now ready to be programmed. After the program has been verified the toggle switch may be moved to the appropriate operation mode position. The LEDs indicate the position of the toggle switch and the state of the program.

Installation of a CMOS expansion memory board on the CPU will require initialization of the CPU with the programmer (See Reference 5).

Expansion Memory

The CPU 782 must have a CMOS RAM expansion memory board. The CMOS expansion memory board provides CMOS RAM memory of 128K, 256K or 512 Kbytes. The battery which supports this memory is located on the main CPU board housing. (See Figure 2)

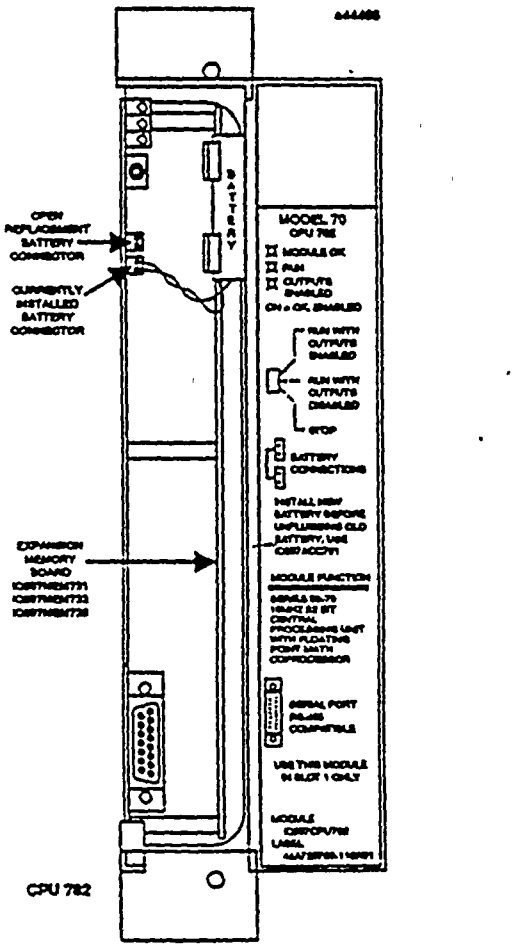


Figure 2. CPU 782 - Location of Major Features

Programmer Connection, Parallel

For a parallel interface the programmer is connected to the top port on the Bus Transmitter Module (IC697BEM713) as shown in Figure 1. Consult Reference 1 for a description of programming functions.

Serial Port

The 15-pin D-connector provides the connection to an RS-485 compatible serial port as shown in Figure 3. This port provides a serial connection to a Work Station Interface board installed in the programming computer.

The serial connection can also be made from the serial port on the CPU to the serial port on the programming computer, or other serial device, through the GE Fanuc RS-422/RS-485 to RS-232 Converter (IC690ACC900). This connection can be made with available cables or you may build cables to fit the needs of your application. For more information on serial communications, see references 5 and 6.

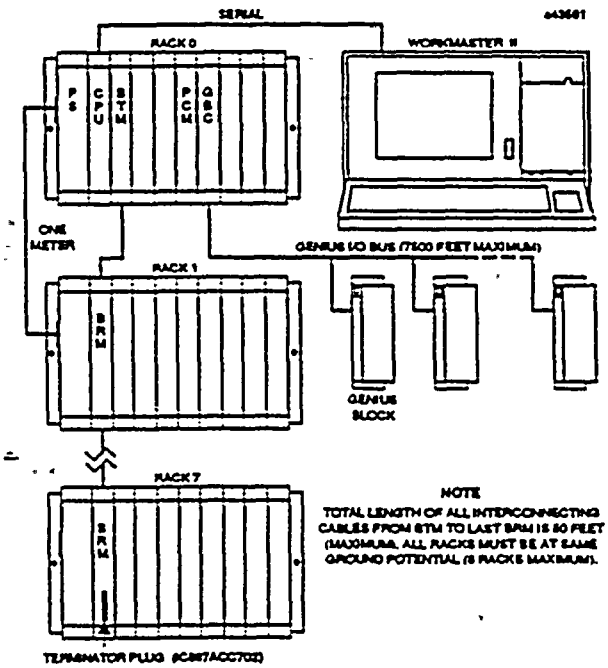


Figure 3. System Configuration, Serial Connection to Programmer

Multidrop Configuration

Following are the cable and connector requirements, and a wiring diagram for connecting a Workmaster II, Workmaster, or other compatible computer to Series 90 PLCs in an 8-wire multidrop, serial data configuration. A maximum of 8 PLCs may be included in a multidrop configuration.

The 15-pin serial port connector for the Series 90-70 PLC is located on the CPU. The 37-pin serial port connector is located on the Work Station Interface board installed in the computer. The cable type for these connections should be 24 AWG, 30V computer grade. Extra flexible construction is recommended for short lengths.

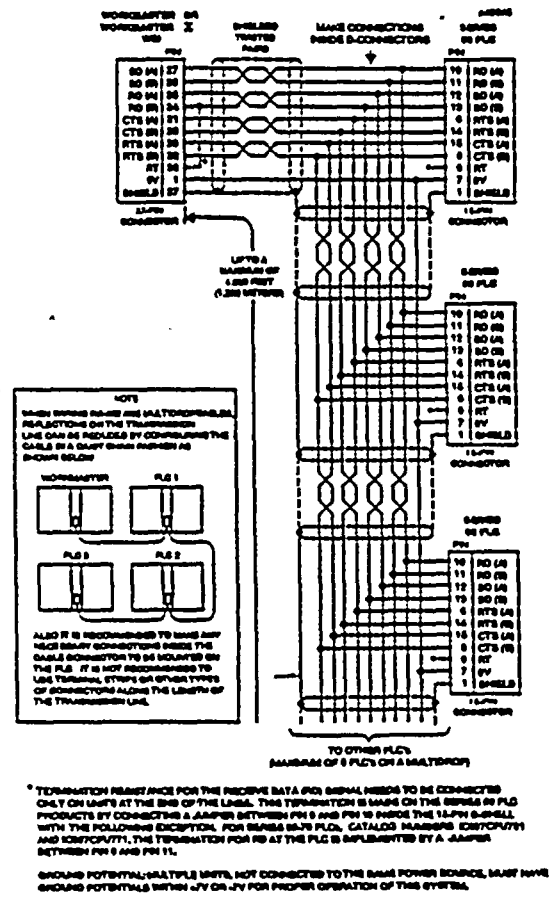


Figure 4. Series 90 PLC 8-Wire Multidrop, Serial Data Configuration

Configuration

The Model 70 CPU and I/O system is configured with Logicmaster 90 programming software. There are no DIP switches or jumpers used to configure the system. The CPU verifies the actual module and rack configuration at power-up and periodically during operation. The actual configuration must be the same as the programmed configuration. Deviations are reported to the CPU alarm processor function for configured fault response. Consult Reference 1 for a description of configuration functions.

Batteries

A lithium battery (IC697ACC701) is installed as shown in Figure 2. This battery maintains program and data memory when power is removed and operates the calendar clock. Be sure to install the new battery before removing the old battery. If during power-up diagnostics a low battery is detected the Module OK LED (top) will not stay on. Specific indication of a low battery state is detailed in Ref. 5.

Removing a Module

The instructions below should be followed when removing a module from its slot in a rack.

- Grasp the board firmly at the top and bottom of the board cover with your thumbs on the front of the cover and your fingers on the plastic clips on the back of the cover.
- Squeeze the rack clips on the back of the cover with your fingers to disengage the clip from the rack rail and pull the board firmly to remove it from the backplane connector.
- Slide the board along the card guide and remove it from the rack.

Table 1. References

Reference	Title	GFK No.
1	Logicmaster™ 90 Programming Software User's Manual	GFK-0263
2	Logicmaster™ 90 Reference Manual	GFK-0265
3	Programmable Coprocessor Module User's Manual	GFK-0255
4	Programmable Coprocessor Module Reference Manual	GFK-0487
5	Series 90™-70 PLC Installation and Operation Manual	GFK-0262

Table 2. Specifications

Battery	
Shelf life	10 years at 20° C
Memory retention	6 months nominal without applied power.
Environmentals	
Operating temperature	0° to 60° C (32° to 140° F)
Storage temperature	-40 to 85° C (-40° to 185° F)
Humidity	5-95% non-condensing.
Vibration	3.5 mm, 5-9 Hz; 1.0 G 9-150 Hz
Shock	15 g's for 11 msec
Current required from 5V Bus	1.6 Amps (includes expansion memory)
Time of Day Clock accuracy	± 3.5 seconds per day maximum
Elapsed Time Clock (internal timing) accuracy	± .01% maximum
Serial Port	
RS422/485 compatible	Programmer Serial Attachment
Complies with standards	
IEC	435, 380
JIS	C 0912, JIS C 0911
DIN	435, 380
UL	508, 1012
CSA	C22.2 No. 142, C22.2
NEMA/ICS	2-230.40
ANSI/IEEE	C-37.90A-1978
VDE	805, 806, 871-877
FCC	15J Part A
VME	System designed to support the VME standard C.1

Table 3. Ordering Information

Description	Catalog Number
CPU 782, 16 MHz, 32 Bit Expandable, Floating Point	IC697CPU782
128 Kbyte, 32-Bit CMOS Expansion Memory	IC697MEM731
256 Kbyte, 32-Bit CMOS Expansion Memory	IC697MEM733
512 Kbyte, 32-Bit CMOS Expansion Memory	IC697MEM735
Lithium Battery	IC697ACC701

SECTION 7
Series 90-70 PLC I/O System

The Series 90-70 PLC I/O system provides the interface between the Series 90-70 PLC and user-supplied devices and equipment. The I/O system supports both rack-type Model 70 I/O and the Genius I/O system. In addition to supporting these two I/O subsystems, the I/O system will also support Subnet Global Memory and PCMs. A Genius I/O Bus Controller (GBC) module provides the interface between the Series 90-70 PLC CPU and a Genius I/O bus.

The I/O structure for the Series 90-70 PLC is shown in the following figure.

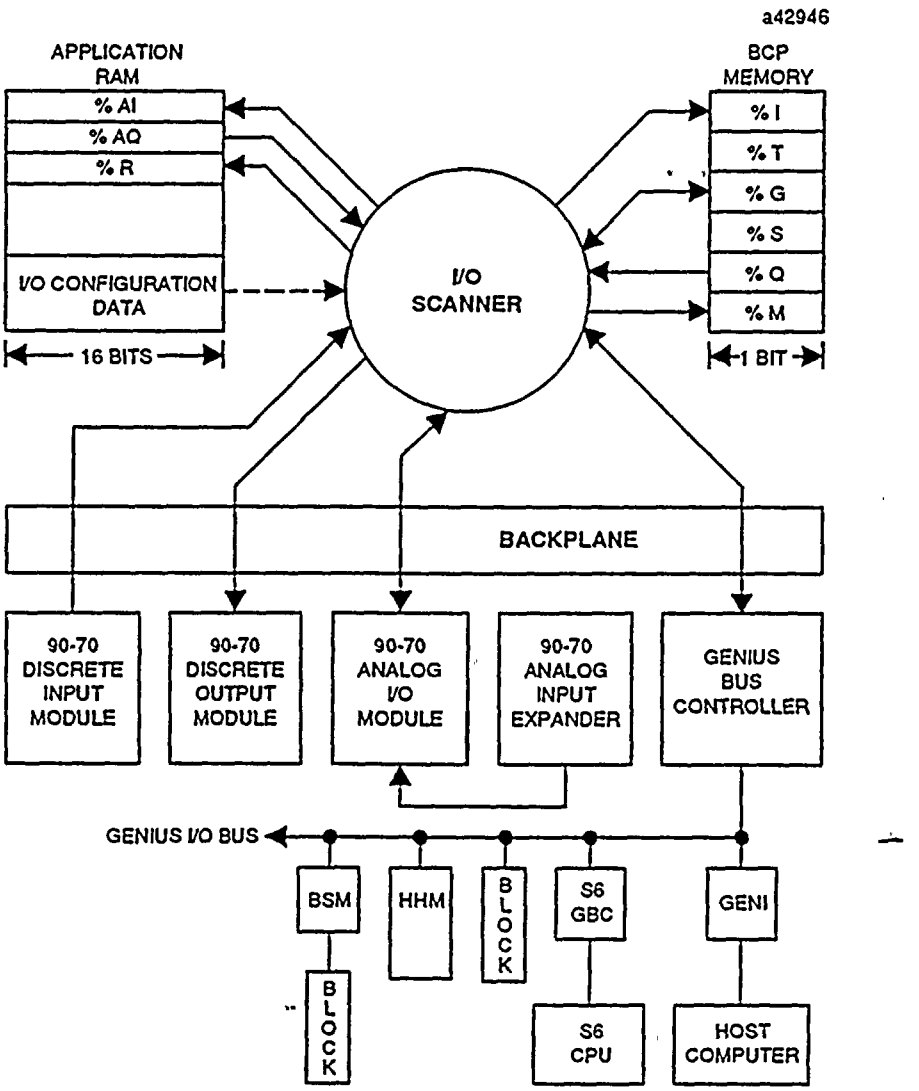


Figure 2-5. Series 90-70 PLC I/O Structure

Model 70 I/O Modules

There are five types of Series 90-70 PLC input/output modules, listed in the following table. This table provides the catalog number, applicable data sheet number, number of I/O points, module description, and configuration parameters for each module. The configuration parameters listed are for every module of a type, unless otherwise noted.

Table 2-11. Model 70 I/O Module Types

Catalog Number	Data Sheet	I/O Points	Description [1]	Configuration Parameters
			Discrete Input	
IC697MDL240	GFK-0375	16	Input 120 VAC 16 Point Isolated	Interrupt Enable (all)
IC697MDL241	GFK-0376	16	Input 240 VAC 16 Point Isolated	Interrupt Transition (all)
IC697MDL250	GFK-0084	32	Input 120 VAC 32 Point	Filter Speed (all)
IC697MDL650	GFK-0080	32	Input 24 VDC 32 Point	
IC697MDL651	GFK-0377	32	Input TTL 32 Point	
IC697MDL652	GFK-0378	32	Input 12 VDC 32 Point Pos/Neg Logic	Logic Sense [2]
IC697MDL653	GFK-0379	32	Input 24 VDC 32 Point Pos/Neg Logic	Logic Sense [2]
IC697MDL654	GFK-0380	32	Input 48 VDC 32 Point Pos/Neg Logic	Logic Sense [2]
			Discrete Output	
IC697MDL340	GFK-0082	16	Output 120 VAC 2A 16 Point	
IC697MDL341	GFK-0382	12	Output 120/240 VAC 2A 12 Point Isol	Output Default (all)
IC697MDL350	GFK-0081	32	Output 120 VAC 0.5A 32 Point	
IC697MDL740	GFK-0086	16	Output 24/48 VDC 2A 16 Point	
IC697MDL750	GFK-0085	32	Output 24/48 VDC 0.5A 32 Point	
IC697MDL752	GFK-0381	32	Output 12 VDC 0.5A 32 Point	
IC697MDL753	GFK-0383	32	Output 5/48 VDC 0.5A 32 Point Neg Log	
IC697MDL940	GFK-0384	16	Output Signal Relay	
			Analog Input [3]	
IC697ALG230	GFK-0385	8 Ch	Input High Level Analog 8 Channel	Per Channel Config
IC697ALG440	GFK-0386	16 Ch	Expander Analog-Current 16 Channel	Board Config.
IC697ALG441	GFK-0387	16 Ch	Expander Analog-Voltage 16 Channel	Board Config.
			Analog Output	
IC697ALG320	GFK-0388	4 Ch	Output Analog-Voltage/Current 4 Channel	Per Channel Config
			Option Modules	
IC697APU700	GFK-0393	-	High Speed Counter	-

[1] Some of the I/O modules listed above may not be available at the time this manual is printed. For current availability, consult your GE Fanuc PLC distributor or local GE Fanuc sales representative.

[2] Logic sense parameter only for discrete DC modules described as having +/- logic. Rest of parameters listed are for all input modules.

[3] Parameter listed is for board on same line.

I/O Data Mapping

Discrete inputs and outputs are stored as bits in the BCP Bit Cache memory. Analog I/O is stored in the application RAM allocated for that purpose. Analog data is always stored in the demultiplexed state, with each channel requiring one word (16 bits).

Default Conditions

Upon power-up, Model 70 discrete input modules default to the first input on the module not interrupting and the input filter being slow speed. The configuration utility provides the ability to specify that the first input may be an interrupt input and for the filter speed to be fast or slow. If changed by the user, new defaults are applied when the board is configured by the CPU during the power-up process or whenever else the module may go through configuration.

Model 70 discrete output modules default to all outputs off. The configuration utility provides the ability to specify whether the CPU transitions from RUN/ENABLED to RUN/DISABLED or STOP modes. It also applies this default information when the system halts.

Genius I/O

Information relative to using Genius I/O in a Series 90-70 PLC system is presented in the following paragraphs. For specific information on Genius I/O block types, configuration, and setup, refer to the Genius I/O System User's Manual, GEK-90486.

Genius I/O Bus Configuration

The Bus Controller used in the Series 90-70 PLC controls a single Genius I/O bus. Any type of Genius I/O block may be attached to the bus.

In the I/O fault table, the rack, slot bus, module, and I/O point number are given for a fault. Bus number one refers to the bus on the single-channel GBC.

Genius I/O Data Mapping

Genius I/O discrete inputs and outputs are stored as bits in the Bit Cache memory. Genius I/O analog data is stored in the application RAM allocated for that purpose (%AI and %AQ). Analog data is always stored one channel per one word (16 bit).

An analog grouped module consumes (in the input and output data memories) only the amount of data space required for the actual inputs and outputs. For example, the Genius I/O 115 VAC Grouped Analog Block, IC660CBA100, has four inputs and two outputs; it consumes four words of Analog Input memory (%AI) and two words of Analog Output memory.

A discrete grouped module, each point of which is configurable with the Hand-Held Monitor (HHM) to be input, output, or output with feedback, consumes an amount in both discrete input memory (%I) and discrete output memory (%Q) equal to its physical size. Therefore, the 8 I/O 115 VAC Discrete Grouped Block (IC660CBD100) requires 8 bits in the %I memory and 8 bits in the %Q memory, regardless of how the block is configured.

There are four Genius I/O blocks assigned to the analog memories:

- 6-Channel Analog Grouped Block.
- 6-Channel Thermocouple Block.
- 6-Channel RTD Block.
- 4-Channel Strain Gauge/mV Analog Input Block.

The Thermocouple, RTD and Strain Gauge blocks are also referred to as Low-Level Analog Input blocks.

Analog Grouped Block

The Analog Grouped block contains four analog input channels and two analog output channels. When a block gets its turn on the Genius I/O Bus, it broadcasts the data for all four input channels in one broadcast control message. Then, when the Bus Controller gets its turn, it sends the data for both output channels to the block in a directed control message.

Low-Level Analog Blocks

Unlike the Analog Grouped block, the low-level analog blocks are input-only blocks. All have six channels except the Strain-Gauge block, which has four.

Default Conditions

Genius I/O blocks have a number of default conditions that may be set using the Genius I/O Hand-Held Monitor. These defaults include:

- Report faults.
- Range select.
- Analog input and output scaling.
- Input filter time.
- Alarm input mode.
- Output hold last state.
- Output default.

These defaults are stored in EEPROM in the block itself. The Series 90-70 PLC configuration utility supports the changing of only a small subset of these defaults. For more information, refer to the Genius I/O System User's Manual, GEK-90486.

Through the COMMREQ function block, the application program can request the Bus Controller to change any default condition on a specific block. However, this change will only be accepted by the block if it is not in CONFIG PROTECT mode. If CONFIG PROTECT mode is set, only the Hand-Held Monitor can be used to change the defaults. The format of the COMMREQ function block for Genius I/O is described in the Genius Bus Controller User's Manual, GFK-0398.

Diagnostic Data Collection

Diagnostic data in a Series 90-70 PLC I/O system is obtained in one of two ways:

1. If an I/O module has an associated Bus Controller, then the Bus Controller provides the module's diagnostic data for the CPU.
2. If an I/O module is a Model 70 I/O module, then the CPU's I/O Scanner subsystem generates the diagnostic bits based on the data provided by the I/O module.

Diagnostic data is not maintained by the Series 90-70 PLC for foreign I/O (not GE Fanuc) modules. Any diagnostic information provided by those boards must be specifically accessed by the application program using the VME Read and VME Write function blocks.

The diagnostic bits are derived from the diagnostic data sent from the I/O modules to their I/O controllers. Diagnostic bits always indicate the current fault status of the associated module. Bits are set when faults occur and are cleared when faults are cleared.

Discrete I/O Diagnostic Information

Diagnostic information is maintained by the Series 90-70 PLC for each discrete I/O point. Two memory blocks are allocated in application RAM for discrete diagnostic data. One is associated with %I memory and the other with %Q memory. One bit of diagnostic memory is associated with each I/O point. This bit indicates the validity of the associated I/O data. Each discrete point has a fault reference available that may be interrogated using two special contacts: a fault contact (-[FAULT]-) and a no-fault contact (-[NOFLT]-). The PLC only collects this fault data if enabled to do so through the configuration software. The following table shows the state of the fault and no-fault contacts.

Condition	[FAULT]	[NOFLT]
Fault Present	ON	OFF
Fault Absent	OFF	ON

Analog I/O Diagnostic Data

Diagnostic information is made available by the PLC CPU for each analog channel associated with Model 70 analog input modules, Model 70 analog output modules, Genius analog blocks, and Subnet objects. Two memory blocks are allocated for analog diagnostic data. One is associated with %AI analog input memory and the other with %AQ analog output memory. One byte of diagnostic memory is allocated for each analog I/O channel. Since each analog I/O channel uses two bytes of %AI and %AQ memory, the diagnostic memory is half the size of the data memory.

The analog diagnostic data contains both diagnostics and process data with the process data being the High Alarm and Low Alarm bits. The diagnostic data is referenced with the -[FAULT]- and -[NOFLT]- contacts. The process bits are referenced with the -[HIALR]- and -[LOALR]- contacts. The memory allocation for analog diagnostic data is one byte per word of analog input and analog output allocated by the user. When an analog fault contact is referenced in the application program, the PLC does an Inclusive OR on all the bits in the diagnostic byte except the process bits. The alarm contact is closed if any diagnostic bit is ON and OFF, only if all bits are OFF.

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Global Data Communications

The Series 90-70 PLC supports the sharing of data between multiple PLC systems that share a common Genius I/O bus. This mechanism provides a means for the automatic and repeated transfer of %G, %I, %Q, %AI, %AQ, and %R data. No special application programming is required to use global data since it is integrated into the I/O scan. All GE Fanuc PLCs that have Genius I/O capability can send global data to a Series 90-70 PLC and can receive data from a Series 90-70 PLC. Logicmaster 90 configuration software is used to configure the receiving and transmitting of global data on a Genius I/O bus.

Chapter 3
Fault Explanation and Correction

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This chapter is an aid to troubleshooting a Series 90-70 PLC system using Logicmaster 90 software. It explains the fault descriptions, which appear in the PLC fault table, and the fault categories, which appear in the I/O fault table.

Each fault explanation in this chapter lists the fault description for the PLC fault table or the fault category for the I/O fault table. Find the fault description or fault category corresponding to the entry on the applicable fault table displayed on your programmer screen. Beneath it is a description of the cause of the fault along with instructions to correct the fault.

Chapter 3 contains the following sections:

Section	Title	Description	Page
1	Fault Handling	Describes the type of faults that may occur in the Series 90-70 PLC and how they are displayed in the fault tables. Descriptions of the PLC and I/O fault table displays are also included, as well as how to access additional fault information by pressing CTRL-F.	3-2
2	PLC Fault Table Explanations	Provides a fault description of each PLC fault and instructions to correct the fault.	3-8
3	I/O Fault Table Explanations	Provides a description of each I/O fault and instructions to correct the fault.	3-24

Additional information on the fault tables may be found in chapter 5, *PLC Control and Status*, in the Programming Software User's Manual, GFK-0263.

For information on system status/fault references, refer to chapter 2, section 3, *Program Organization and User Data*.

Fault Response

Fault response refers to the ability of a fault to have its fault action changed. Those faults which can have their fault action changed are called configurable faults. Those which cannot are called non-configurable faults. Non-configurable faults are either fatal or informational. Also, non-configurable faults do not cause application available references to be set and cannot have alarm blocks associated with the detection of the fault. Some non-configurable faults also have other effects associated with them. Generally, these effects control the changing of the CPU's execution mode (STOP, RUN/DISABLED, RUN/ENABLED). An example of such an effect is the disabling of I/O when a NULL System Configuration is detected in the system.

PLC Fault Table

The PLC fault table displays PLC faults such as password violations, PLC/configuration mismatches, parity errors, and communications errors. For example:

```
|I/O    |CPU    |STATUS |       |       |       |SETUP  |FOLDER |UTILTY |PRINT
1plcrun 2passwd 3plcflt 4io flt 5plcmem 6       7       8       9clear 10zoom

>

                        P L C   F A U L T   T A B L E

TOP FAULT DISPLAYED: 00003                  TABLE LAST CLEARED: 04-24 13:13:19
      TOTAL FAULTS: 00003                   ENTRIES OVERFLOWED: 00000
                                                PLC DATE/TIME: 04-24 13:16:35

  FAULT                                                          DATE    TIME
 LOCATION                        FAULT DESCRIPTION               M-D   H: M: S
-------- ------------------------------------------------------ ----- --------
0.1      Low battery signal                                     04-24 13:16:24
0.2      System configuration mismatch                          04-24 13:13:53
0.1      Application stack overflow                             04-24 13:13:20

LD:       STOP/FAULT                ONLINE  L4 ACC: WRITE LOGIC  CONFIG-EQUAL
C:\LM90\LESSON                    PRG: LESSON
REPLACE
```

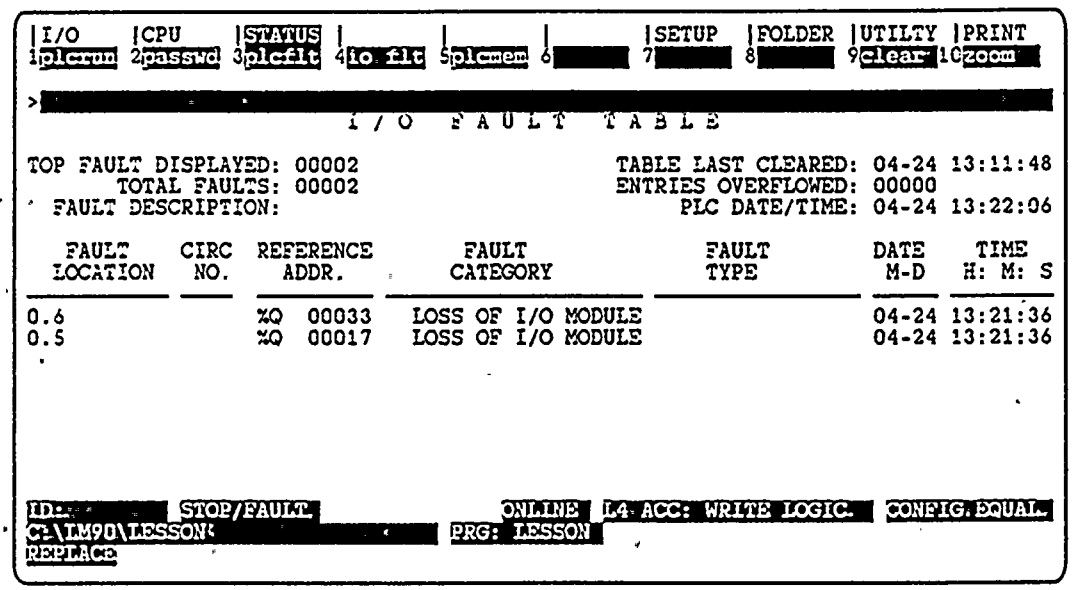
To display a screen similar to the one shown above, press PLC Fault (F3) from the PLC Control and Status menu or from another PLC functions screen. The programmer may be in any operating mode. However, if the programmer is in Off-Line mode, no faults are displayed. In On-Line or Monitor mode, PLC fault data is displayed. In On-Line mode, faults can be cleared (this may be password protected).

Field	Description
Top Fault Displayed	The index of the PLC fault currently at the top of the fault display is shown on the first line of this screen.
Total Faults	The total number of faults since the table was last cleared.
Table Last Cleared	The date and time faults were last cleared from the fault table. This information is maintained by the PLC.
Entries Overflowed	The number of entries lost because the fault table has overflowed since it was cleared. The PLC fault table can contain up to 16 faults.
PLC Time/Date	The current date and time. This is also maintained by the PLC.

For more information on the PLC fault table, refer to the chapter 5, *PLC Control and Status*, in the Programming Software User's Manual, GFK-0263.

I/O Fault Table

The I/O fault table displays I/O faults such as circuit faults, address conflicts, forced circuits, and I/O bus faults. For example:



To display a screen similar to the one shown above, press I/O Fault (F4) from the PLC Control and Status menu or from another PLC functions screen. The programmer may be in any operating mode. However, if the programmer is in Off-Line mode, no faults are displayed. In On-Line or Monitor mode, PLC fault data is displayed. In On-Line mode, faults can be cleared (this feature may be password protected).

Field	Description
Top Fault Displayed	The index of the I/O fault currently at the top of the fault display is shown on the first line of this screen.
Total Faults	The total number of faults since the table was last cleared.
Fault Description	An explanation of the fault that is currently highlighted in the I/O fault table.
Table Last Cleared	The date and time faults were last cleared from the fault table. This information is maintained by the PLC.
Entries Overflowed	The number of entries lost because the fault table has overflowed since it was cleared. The I/O fault table can contain up to 32 faults.
PLC Time/Date	The current date and time. This is also maintained by the PLC.

For more information on the I/O fault table, refer to the chapter 5, *PLC Control and Status*, in the Programming Software User's Manual, GFK-0263.

Displaying User-Defined Faults

User-defined faults can be logged in the PLC or I/O fault table. When a user-defined fault occurs, it is logged in the appropriate fault table as "Application Msg(error_code):" and may be followed by a descriptive message up to 24 characters. All characters in the descriptive message can be defined by the user. Although the message must end with the null character (e.g., ASCII value 16x00), the null character does not count as one of the 24 characters. If the message contains more than 24 characters, only the first 24 characters are displayed.

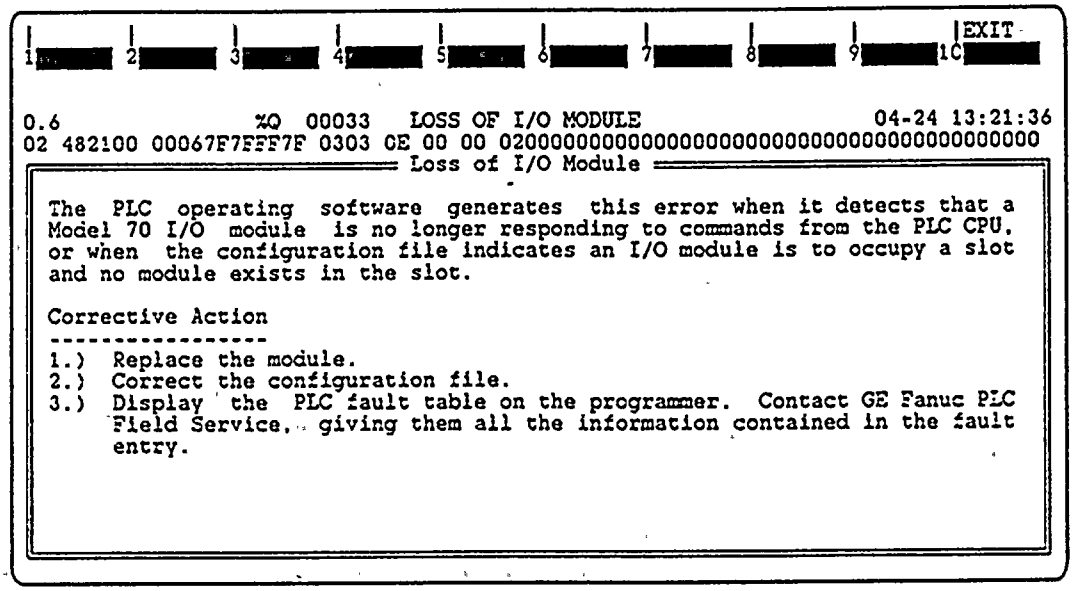
The following example PLC fault table contains a user-defined fault with error code 87.

```
|PROGRM |TABLES |STATUS |       |       |LIB    |SETUP  |FOLDER |UTILTY |PRINT
1plcrun 2passwd 3plcflt 4io flt 5plcmem 6blkmem 7refsiz 8sweep  9clear 10zoom
>

                          P L C   F A U L T   T A B L E

TOP FAULT DISPLAYED: 00001                    TABLE LAST CLEARED: 04-24 13:42:38
      TOTAL FAULTS: 00001                     ENTRIES OVERFLOWED: 00000
                                                   PLC DATE/TIME: 04-24 13:43:06

  FAULT                                FAULT                          DATE    TIME
 LOCATION                            DESCRIPTION                      M-D   H: M: S
-------- ------------------------------------------------------------ ------ --------
0.1      Application Msg(87): This is a user fault                    04-24 13:42:51




ID:       RUN/OUT EN   5ms SCAN  ONLINE  L4 ACC: WRITE LOGIC  LOGIC-EQUAL-
C:\LM90\LESSON                  PRG: LESSON
REPLACE
```

For more information on user-defined faults, refer to the chapter 5, *PLC Control and Status*, in the Programming Software User's Manual, GFK-0263.

Accessing Additional Fault Information

The PLC and I/O fault tables contain basic information about the faults listed in each table. Additional information about a particular fault can be displayed by positioning the cursor on that fault in the appropriate table and pressing the Zoom (F10) softkey. Information about the error code, default action, description of the error, and appropriate corrective action is displayed on a screen similar to this one for a Loss of I/O Module error.



NOTE

A hexadecimal dump of the fault can also be displayed by pressing CTRL-F from this screen.

The last entry, *Correction*, for each fault explanation in this chapter lists the action(s) to be taken to correct the fault. Note that the corrective action for some of the faults includes the statement:

```
Display the PLC Fault Table on the Programmer.  Contact GE Fanuc Field
Service, giving them all the information contained in the fault entry.
```

This second statement means that you must tell Field Service both the information readable directly from the fault table *and* the hexadecimal information you see when you press CTRL-F. Field Service personnel will then give you further instructions for the appropriate action to be taken.

For more information on interpreting faults, refer to Appendix B, *Interpreting Fault Tables Using Logicmaster 90 Software.*

SECTION 2
PLC Fault Table Explanations

Each fault explanation contains a fault description and instructions to correct the fault. Many fault descriptions have multiple causes. In these cases, the error code, displayed with the additional fault information obtained by pressing CTRL-F, is used to distinguish different fault conditions sharing the same fault description. The error code is the first two hexadecimal digits in the fifth group of numbers, as shown in the following example.

```
01    000000    01030100    0902    0200    000000000000
                                          |__ Error Code (first two hex
                                              digits in fifth group)
```

Some faults can occur because random access memory on either the PLC CPU board or the expansion memory board has failed. These same faults may also occur because the system has been powered off and the battery voltage is (or was) too low to maintain memory. To avoid excessive duplication of instructions when corrupted memory may be a cause of the error, the correction simply states:

```
Perform the corrections for Corrupted Memory.
```

This means:

1. If the system has been powered off, replace the battery. Battery voltage may be insufficient to maintain memory contents.
2. Replace the expansion memory board. Integrated circuits on the memory board may be failing.
3. Replace the PLC CPU board. The integrated circuits on the PLC CPU board may be failing.

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The following table enables you to quickly find a particular fault explanation in this section. Each entry is listed as it appears on the programmer screen.

Fault Description	Page Number
Loss of, or Missing, Rack	3-10
Loss of, or Missing, Option Module	3-11
Addition of, or Extra, Rack	3-12
Reset of, Addition of, or Extra, Option Module	3-12
System Configuration Mismatch	3-13
System Bus Error	3-15
PLC CPU Hardware Failure	3-15
Module Hardware Failure	3-16
Option Module Software Failure	3-16
Program Block Checksum Failure	3-17
Low Battery Signal	3-17
Constant Sweep Time Exceeded	3-18
PLC System Fault Table Full	3-18
I/O Fault Table Full	3-18
Application Fault	3-19
Non-Configurable Faults	3-19
System Bus Failure	3-20
No User Program on Power-Up	3-20
Corrupted User Program on Power-Up	3-20
Window Completion Failure	3-21
Password Access Failure	3-21
Null System Configuration for RUN Mode	3-21
PLC CPU System Software Failure	3-22
Too Many Bus Controllers	3-23
Communications Failure During Store	3-23
Run Mode Store Failure	3-23

Configurable Faults

Configurable faults can have their fault action (fatal or diagnostic) changed. The CPU uses the fault action specified by the configurator utility; this may be the default action or a fault action chosen by the user. In this section, the default fault action is listed for configurable faults.

Loss of, or Missing, Rack

The Fault Group Loss of, or Missing Rack (Group 1) occurs when the system cannot communicate with an expansion rack because the BTM in the main rack failed, the BRM in the expansion rack failed, power failed in the expansion rack or the expansion rack was configured in the configuration file but did not respond during power-up. The default fault action for this group is Fatal.

Error Code:	1
Name:	Rack Lost
Description:	The PLC operating software (System Configurer) generates this error when the main rack can no longer communicate with an expansion rack. The error is generated for each expansion rack that exists in the system.
Correction:	(1) Power off the system. Verify that both the BTM and the BRM are seated properly in their respective racks and that all cables are properly connected and seated. (2) Replace the cables. (3) Replace the BRM. (4) Replace the BTM.
Error Code:	2
Name:	Rack Not Responding
Description:	The PLC operating software (System Configurer) generates this error when the configuration file is stored from the programmer indicates that a particular expansion rack should be in the system, but none responds for that rack number.
Correction:	(1) Check rack number jumper behind power supply, first on missing rack and then on all other racks, for duplicated rack numbers. (2) Update the configuration file if a rack should not be present. (3) Add the rack to the hardware configuration if a rack should be present and one is not. (4) Power off the system. Verify that both the BTM and the BRM are seated properly in their respective racks and that all cables are properly connected and seated. (5) Replace the cables. (6) Replace the BRM. (7) Replace the BTM.

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Loss of, or Missing, Option Module

The Fault Group Loss of, or Missing Option Module (Group 4) occurs when a GEnet, PCM, BTM, or BRM fails to respond. The failure may occur at power-up if the module is missing or during operation if the module fails to respond. The default fault action for this group is Diagnostic.

Error Code:	3
Name:	Bus Transmitter Module Found in Expansion Rack
Description:	The PLC operating software (System Configurer) generates this error when a Bus Transmitter Module is found in an expansion rack.
Correction:	Power off the system and remove the BTM from the expansion rack.
Error Code:	16h
Name:	Analog Expander located to the left of the Base Converter module.
Description:	An Analog Expander module has been placed in a rack to the left of its Base Converter module.
Correction:	Power off the system. Move the Analog Expander module to the right of the Base Converter module.
Error Code:	19
Name:	Lost Analog Expander module
Description:	Base Converter module has lost communications with the Analog Expander module.
Correction:	(1) Verify wiring linking Base Converter module with the Analog Expander module. (2) Replace the Analog Expander module. (3) If all Analog Expanders lost, replace the Base Converter module.
Error Code:	2C, 2D
Name:	Option Module Soft Reset Failed
Description:	PLC CPU unable to re-establish communications with option module after soft reset.
Correction:	(1) Try soft reset a second time. (2) Replace the option module. (3) Power off the system. Verify that both the BTM and BRM are seated properly in their respective racks and that all cables are properly connected and seated. (4) Replace the cables. (5) Replace the BRM. (6) Replace the BTM. (7) Report failure to GE Fanuc PLC Field Service.
Error Code:	FF
Name:	Option Module Communications Failed
Description:	PLC CPU generates this error when communications to the option module has failed.
Correction:	(1) Check the bus for abnormal activity. (2) Replace the intelligent option module to which the request was directed. (3) Check the parallel programmer cable for proper attachment.
Error Code:	All Others
Name:	Module Failure During Configuration
Description:	The PLC operating software (CPU VME Communications) generates this error when a module fails during power-up or configuration store.
Correction:	(1) Power off the system. Replace the module located in that rack and slot. (2) If the board is located in an expansion rack, verify BTM/BRM cable connections are tight and the modules are seated properly; verify the addressing of the expansion rack. (3) Replace the BTM. (4) Replace the BRM. (5) Replace the rack.

Addition of, or Extra, Rack

The Fault Group Addition of, or Extra Rack (Group 5) occurs when a configured expansion rack with which the PLC CPU could not communicate comes on-line or is powered on, or an unconfigured rack is found. The default fault action for this group is **Diagnostic.**

Error Code:	1
Name:	Extra Rack
Correction:	(1) Check rack jumper behind power supply for correct setting. (2) Update the configuration file to include the expansion rack. (3) Remove the expansion rack from the hardware configuration. Note: No correction necessary if rack was just powered on.

Reset of, Addition of, or Extra, Option Module

The Fault Group **Reset of, Addition of, or Extra Option Module** (Group 8) occurs when an option module (PCM, BTM, etc.) comes on-line, is reset, or a module is found in the rack but none is specified in the configuration. The default fault action for this group is **Diagnostic.**

Error Code:	1
Name:	Extra Option Module
Correction:	(1) Update the configuration file to include the module. (2) Remove the module from the system.
Error Code:	2
Name:	Module Restart Complete
Description:	Restart of module is complete.
Correction:	None
Error Code:	3
Name:	LAN Interface Restart Complete, Running Utility
Description:	The LAN Interface module has restarted and is running a utility program.
Correction:	Refer to the LAN Interface Module Manual, GFK-0533.

System Configuration Mismatch

The Fault Group Configuration Mismatch (Group 11) occurs when the module occupying a slot is different from that specified in the configuration file. The default fault action is Fatal. When the I/O Scanner generates the mismatch because of a Genius block, the second byte in the *Fault Extra Data* field contains the bus address of the mismatched block.

Error Code:	2
Name:	Genius I/O Block Number Mismatch
Description:	The PLC operating software (I/O Scanner) generates this fault when the configured and physical Genius I/O blocks have different model numbers.
Correction:	(1) Replace the Genius I/O block with one corresponding to configured module. (2) Update the configuration file.
Error Code:	4
Name:	I/O Type Mismatch
Description:	The PLC operating software (I/O Scanner) generates this fault when the physical and configured I/O types of Genius grouped blocks are different.
Correction:	(1) Remove the indicated Genius module and install the module indicated in the configuration file. (2) Update the Genius module descriptions in the configuration file to agree with what is physically installed.
Error Code:	7
Name:	Daughter Board Mismatch
Description:	The PLC operating software (Service Request Processor) generates this error when the configuration file indicates one size memory daughter (expansion) board should be on the PLC CPU, and a different size is actually present.
Correction:	(1) Replace the module. (2) Replace the daughter board with the size indicated in the configuration file. (3) Update the configuration file to agree with the size of the daughter board actually installed on the PLC CPU.
Error Code:	8
Name:	Analog Expander Mismatch
Description:	The PLC operating software (Service Request Processor) generates this error when the configured and physical Analog Expander modules have different model numbers.
Correction:	(1) Replace the Analog Expander module with one corresponding to configured module. (2) Update the configuration file.
Error Code:	9
Name:	Genius I/O Block Size Mismatch
Description:	The PLC operating software (Service Request Processor) generates this error when block configuration size does not match the configured size.
Correction:	Reconfigure the block.
Error Code:	A
Name:	Unsupported Feature
Description:	Configured feature not supported by this revision of the module.
Correction:	(1) Update the module to a revision that supports the feature. (2) Change the module configuration.

Error Code:	B
Name:	Revision A of BTM Not in Right-Most Slot
Description:	The BTM (Revision A version) is not the right-most module in the rack.
Correction:	(1) Move the BTM to the right of all other modules in the rack. (2) Upgrade the BTM to a newer version (Revision B, or higher).
Error Code:	E
Name:	LAN Duplicate MAC Address
Description:	This LAN Interface module has the same MAC address as another device on the LAN. The module is off the network.
Correction:	(1) Change the module's MAC address. (2) Change the other device's MAC address.
Error Code:	F
Name:	LAN Duplicate MAC Address Resolved
Description:	Previous duplicate MAC address has been resolved. The module is back on the network. This is an informational message.
Correction:	None required.
Error Code:	10
Name:	LAN MAC Address Mismatch
Description:	MAC address programmed by softswitch utility does not match configuration stored from Logicmaster 90 software.
Correction:	Change MAC address on softswitch utility or in Logicmaster 90 configuration software.
Error Code:	11
Name:	LAN Softswitch/Modem mismatch
Description:	Configuration of LAN module does not match modem type or configuration programmed by softswitch utility.
Correction:	(1) Correct configuration of modem type. (2) Consult LAN Interface manual for configuration setup.
Error Code:	17
Name:	Invalid Memory Reference
Description:	Memory references in the logic program exceed that which is available.
Correction:	Update the configuration file and store it to the PLC.
Error Code:	All Others
Name:	Module and Configuration Do Not Match
Description:	The PLC operating software (System Configurer) generates this fault when the module occupying a slot is not of the same type that the configuration file indicates should be in that slot.
Correction:	(1) Replace the module in the slot with one of the type that the configuration file indicates is in that slot. (2) Update the configuration file.

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System Bus Error

The Fault Group System Bus Error (Group 12) occurs when the PLC CPU receives the non-configurable interrupt bus error from the bus system. The default fault action is Diagnostic.

Error Code:	4
Name:	Unrecognized VME Interrupt Source
Description:	The PLC operating software (Operating System) generates this error when a module generates an interrupt not expected by the CPU (unconfigured or unrecognized).
Correction:	(1) Ensure that all modules configured for interrupts have corresponding interrupt declarations in the program logic. (2) Ensure that no third-party VME module is generating interrupts on the IRQ6 and IRQ7 lines.
Error Code:	All Others
Name:	System Bus Error
Description:	The PLC operating software (Operating System) generates this fault when it has detected an error signal on the VME backplane, such as a parity error.
Correction:	(1) Ensure that all expansion rack cables are properly connected and seated. (2) Take action to minimize system noise.

PLC CPU Hardware Failure

The Fault Group PLC CPU Hardware (Group 13) occurs when the PLC CPU detects a hardware failure, such as a RAM failure or a communications port failure. When the failure is a RAM failure, the address of the failure is stored in the first four bytes of the *Fault Extra Data* field.

When a PLC CPU Hardware failure occurs, the PLC OK LED will flash on and off to indicate that the failure was not serious enough to prevent programmer communications to retrieve the fault information. The default fault action for this group is Fatal.

Error Code:	6Eh
Name:	Time-of-Day Clock Not Battery-Backed
Description:	The battery-backed value of the time-of-day clock has been lost.
Correction:	(1) Replace the battery. Do not remove power from the main rack until replacement is complete. Reset the time-of-day clock using Logicmaster 90 software. (2) Replace the module.
Error Code:	All Others
Correction:	Replace the module.

Module Hardware Failure

The Fault Group **Module Hardware Failure** (Group 14) occurs when the PLC CPU detects non-fatal hardware failure on any module in the system, e.g., a serial port failure on a PCM. The default fault action for this group is **Diagnostic.**

Error Code:	1A0
Name:	Missing 12 Volt Power Supply
Description:	A power supply that supplies 12 volts is required to operate the LAN Interface module.
Correction:	(1) Install/replace a GE Fanuc 100 watt power supply. (2) Connect an external VME power supply that supplies 12 volts.
Error Code:	1C2 - 1C6
Name:	LAN Interface Hardware Failure
Description:	Refer to the LAN Interface Module Manual, GFK-0533, for a description of these errors.
Error Code:	All Others
Name:	Module Hardware Failure
Description:	A module hardware failure has been detected.
Correction:	Replace the affected module.

Option Module Software Failure

The Fault Group **Option Module Software Failure** (Group 16) occurs when a non-recoverable software failure occurs on a PCM. It is also generated when the identification data read from a module indicates that the module is a GE Fanuc module but the module type is not a supported GE Fanuc type. The default fault action for this group is **Fatal.**

Error Code:	1
Name:	Unsupported Board Type
Description:	The PLC operating software (System Configurer) generates this fault when the identification data read from a board indicates that the board is a GE Fanuc board but the type of board is not one of the GE Fanuc board types.
Correction:	(1) Upload the configuration file and verify that the software recognizes the board type in the file. If there is an error, correct it, download the corrected configuration file and retry. (2) Display the PLC fault table on the programmer. Contact GE Fanuc PLC Field Service, giving them all the information contained in the fault entry.
Error Code:	2, 3
Name:	COMMREQ Frequency Too High
Description:	COMMREQs are being sent to a module faster than it can process them. —
Correction:	Change the PLC program to send COMMREQs to the affected module at a slower rate, or monitor the completion status of each COMMREQ before sending the next.
Error Code:	4
Name:	More Than One BTM in a Rack
Description:	There is more than one BTM present in the rack.
Correction:	Remove one of the BTMs from the rack; there can only be one in a CPU rack.
Error Code:	191, 195
Name:	LAN Interface Software Failure
Description:	Refer to the LAN Interface Module Manual, GFK-0533, for a description of these errors.
Error Code:	All Others
Name:	Option Module Software Failure
Description:	Software failure detected on an option module.
Correction:	(1) Reload software into the indicated module. (2) Replace the module.

Program Block Checksum Failure

The Fault Group Program Block Checksum Failure (Group 17) occurs when the PLC CPU detects error conditions in program blocks received by the PLC. It also occurs when the PLC CPU detects checksum errors during power-up verification of memory or during RUN mode background checking. In all cases, the ***Fault Extra Data*** field of the PLC fault table record contains the name of the program block in which the error occurred. The default fault action for this group is Fatal.

Error Code:	All
Name:	Program Block Checksum Failure
Description:	The PLC operating software generates this error when a program block is corrupted.
Correction:	(1) Clear PLC memory and retry the store. (2) Display the PLC fault table on the programmer. Contact GE Fanuc PLC Field Service, giving them all the information contained in the fault entry.

Low Battery Signal

The Fault Group Low Battery Signal (Group 18) occurs when the PLC CPU detects a low battery on the PLC CPU board, the PLC CPU memory daughter board, or a module such as the PCM reports a low battery condition. The default fault action for this group is Diagnostic.

Error Code:	0
Name:	Failed Battery Signal
Description:	The CPU module (or other module having a battery) battery is dead.
Correction:	Replace the battery. Do not remove power from the rack until replacement is complete.

Error Code:	1
Name:	Low Battery Signal
Description:	A battery on the CPU or other module has a low signal.
Correction:	Replace the battery. Do not remove power from the rack until replacement is complete.

Constant Sweep Time Exceeded

The Fault Group **Constant Sweep Time Exceeded** (Group 19) occurs when the PLC CPU operates in Constant Sweep Time mode and it detects that the sweep has exceeded the constant sweep timer. The fault extra data contains the name of the program in eight bytes. The default fault action for this group is **Diagnostic.**

Error Code:	0
Correction:	(1) Increase constant sweep time. (2) Remove logic from application program.

PLC System Fault Table Full

The Fault Group **PLC System Fault Table Full** (Group 20) occurs when the PLC CPU places the 16th entry in the PLC fault table. To avoid loss of additional faults, clear the earliest entry from the table. The default fault action for this group is **Diagnostic.**

Error Code:	0
Correction:	Clear the PLC fault table.

I/O Fault Table Full

The Fault Group **I/O Fault Table Full** (Group 21) occurs when the PLC CPU places the 32nd entry in the I/O fault table. To avoid loss of additional faults, clear the earliest entry from the table. The default fault action for this group is **Diagnostic.**

Error Code:	0
Correction:	Clear the I/O fault table.

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Application Fault

The Fault Group Application Fault (Group 22) occurs when the PLC CPU detects a fault in the user program. The default fault action for this group is **Diagnostic.**

Error Code:	1
Name:	Indirect Address Out of Range
Description:	The PLC operating software generates this error when one of the parameters to a function block is an indirect reference (i.e., the parameter is an address within that memory type which contains the parameter value) and the contents of the indirect reference are out of range for the memory type. For example, consider a system with 500 %R registers defined. This fault would be generated if the parameter address were %R00100, and the contents of %R00100 were greater than 500 or zero. The Fault Extra Data field contains in the first two bytes the offset address of where the call was made, the segment selector and offset (reference) in the next four bytes, and the name of the program block in which the function call resides in the next eight bytes.
Correction:	(1) Correct the indirect reference. (2) Increase the number of registers available, if possible.
Error Code:	2
Name:	Software Watchdog Timer Expired
Description:	The PLC operating software generates this error when the watchdog timer expires. The PLC CPU stops executing the user program and enters STOP mode. The only recovery is to cycle power to the PLC CPU. Examples causing timer expiration: Looping, via jump, very long program, etc.
Correction:	(1) Determine what caused the expiration (logic execution, external event, etc.) and correct. (2) Use the system service function block to restart the watchdog timer.
Error Code:	5
Name:	COMMREQ Wait Mode Not Supported
Description:	The module receiving the COMMREQ does not support wait mode COMMREQs.
Correction:	Use no-wait mode COMMREQs.
Error Code:	6
Name:	COMMREQ Bad Task ID
Description:	The task selected by the COMMREQ does not exist on the option module.
Correction:	Correct the task ID.
Error Code:	7
Name:	Application Stack Overflow
Description:	Program block call depth has exceeded the PLC capability.
Correction:	Adjust application program to reduce nesting.
Error Code:	8 - D
Name:	LAN Interface Application Faults
Description:	Refer to the LAN Interface Module Manual, GFK-0533, for a description of these errors.
Error Code:	0E
Name:	External Block Run-Time Error
Description:	A non-user generated error occurred during execution of an external block.
Correction:	Decode the hexadecimal CTRL-F data displayed by Logicmaster 90 software into ASCII text to determine the exact error condition. Then, correct the specific problem in the external block.
Error Code:	0F
Name:	SORT Interrupt Error
Description:	A SORT function executed in a timed or I/O interrupt at the same time a SORT function was executing in the main program.
Correction:	Do not use the SORT function in both an interrupt and in the main program.

Non-Configurable Faults

The fault action of **Non-Configurable Faults** cannot be changed. **Fatal** faults cause the PLC to enter a form of STOP mode at the end of the sweep in which the error occurred. **Diagnostic** faults are logged and corresponding fault contacts are set. **Informational** faults are simply logged in the PLC fault table.

System Bus Failure

The Fault Group System Bus Failure (Group 128) occurs when the PLC CPU software receives the non-configurable interrupt bus failure from the bus system. The default fault action for this group is Fatal.

Error Code:	1
Name:	Bus Grant Failure
Description:	The PLC operating software (Operating Software) generates this error when the PLC CPU was unable to obtain control of the VME bus when required.
Correction:	(1) Ensure that any non-GE Fanuc boards which can become bus masters are relinquishing control of the VME bus when requested to do so by the PLC CPU. (2) Replace the PLC CPU module.

No User Program on Power-Up

The Fault Group No User Program on Power-Up (Group 129) occurs when the PLC CPU powers up with its memory preserved but no user program exists in the PLC. The PLC CPU detects the absence of a user program on power-up; the controller stays in STOP mode, performing the STOP mode sweep until a valid program is downloaded. The default fault action for this group is Informational.

Correction:	Download an application program before attempting to go to RUN mode.

Corrupted User Program on Power-Up

The Fault Group Corrupted User Program on Power-Up (Group 130) occurs when the PLC CPU detects corrupted user RAM. The PLC CPU will remain in STOP mode until a valid user program and configuration file are downloaded. The default fault action for this group is Fatal.

Error Code:	1
Name:	Corrupted User RAM on Power-Up
Description:	The PLC operating software (Operating Software) generates this error when it detects corrupted user RAM on power-up.
Correction:	(1) Reload the configuration file, user program, and references (if any). (2) Replace the battery on the PLC CPU. (3) Replace the expansion memory board on the PLC CPU. (4) Replace the PLC CPU.
Error Code:	2
Name:	Illegal Boolean OpCode Detected
Description:	The PLC operating software (Operating Software) generates this error when it detects a bad instruction in the user program.
Correction:	(1) Restore the user program and references, if any. (2) Replace the expansion memory board on the PLC CPU. (3) Replace the PLC CPU.
Error Code:	6
Name:	Corrupted Remote I/O Scanner EEPROM
Description:	The configuration in the Remote I/O Scanner EEPROM was found to be corrupted at power-up.
Correction:	Restore the Remote I/O Scanner configuration.

Window Completion Failure

The Fault Group Window Completion Failure (Group 131) is generated by the end-of-sweep processing software in the PLC. The fault extra data contains the name of the task that was executing when the error occurred. The default fault action for this group is **Informational.**

Error Code:	0
Name:	Window Completion Failure
Description:	The PLC operating software generates this error when the PLC is operating in Constant Sweep Time mode and the constant sweep time was exceeded before the programmer window could complete processing for its allotted time.
Correction:	Increase the constant sweep timer value.

Password Access Failure

The Fault Group Password Access Failure (Group 132) occurs when the PLC CPU receives a request to change to a new privilege level and the password included with the request is not valid for that level. The default fault action for this group is **Informational.**

Error Code:	0
Correction:	Retry the request with the correct password.

Null System Configuration for RUN Mode

The Fault Group Null System Configuration for RUN Mode (Group 134) occurs when the PLC transitions from STOP to one of the RUN modes and a configuration file is not present. The transition to RUN is permitted, but no I/O scans occur. The effect of this fault is to perform the function of a Suspend I/O. The default fault action for this group is **Informational.**

Error Code:	0
Correction:	Download a configuration file.

PLC CPU System Software Failure

Faults in the Fault Group **PLC CPU System Software Failure** (Group 135) are generated by the operating software of the Series 90-70 PLC CPU. They occur at many different points of system operation. When a **Fatal** fault occurs, the PLC CPU *immediately* transitions into a special Error Sweep mode. The only activity permitted when the PLC is in this mode is communications with the programmer. The only method of clearing this condition is to cycle power on the PLC. The default fault action for this group is **Fatal.**

Error Code:	14, 27
Name:	Corrupted PLC Program Memory
Description:	The PLC operating software generates these errors when certain PLC operating software problems occur. These should *not* occur in a production system.
Correction:	(1) Display the PLC fault table on the programmer. Contact GE Fanuc PLC Field Service, giving them all the information contained in the fault entry. (2) Perform the corrections for corrupted memory.
Error Code:	52
Name:	Backplane Communications Failed
Description:	The PLC operating software (Service Request Processor) generates this error when it attempts to comply with a request that requires backplane communications and receives a rejected mail response.
Correction:	(1) Check the bus for abnormal activity. (2) Replace the intelligent option module to which the request was directed. (3) Check parallel programmer cable for proper attachment.
Error Code:	5A
Name:	User Shut Down Requested
Description:	The PLC operating software (function blocks) generates this informational alarm when SVCREQ #13 (User Shut Down) executes in the application program.
Correction:	None required. Information-only alarm.
Error Code:	7B
Name:	Remote I/O Scanner Communications Heartbeat Failure
Description:	Refer to the Remote I/O Scanner User's Manual, GFK-0579, for a description of this error.
Error Code:	All Others
Name:	PLC CPU Internal System Error
Description:	An internal system error has occurred that should not occur in a production system.
Correction:	Display the PLC fault table on the programmer. Contact GE Fanuc PLC Field Service, giving them all the information contained in the fault entry.

Too Many Bus Controllers

The Fault Group Too Many Bus Controllers (Group 136) occurs when the the I/O Scanner portion of the PLC operating software detects that more than the maximum number (32) of bus controllers have been defined. The PLC CPU itself is a bus controller for the Model 70 I/O present in the system. The default fault action for this group is Fatal.

NOTE

Genius bus controllers which are configured for redundant and non-redundant blocks count as two bus controllers.

Correction:	(1) Determine which modules are bus controllers and remove the extra ones. (2) Delete a bus controller from the configuration file and store the file to the PLC CPU. (3) If bus controllers have been moved from one slot in the rack to a different slot and this error did not occur before the move, cycle power on the rack. No module should be inserted with power applied to rack. (4) Display the PLC fault table on the programmer. Contact GE Fanuc PLC Field Service, giving them all the information contained in the fault entry.

Communications Failure During Store

The Fault Group Communications Failure During Store (Group 137) occurs during the store of program blocks and other data to the PLC. The stream of commands and data for storing program blocks and data starts with a special start-of-sequence command and terminates with an end-of-sequence command. If communications with the programming device performing the store is interrupted or any other failure occurs which terminates the load, this fault is logged. As long as this fault is present in the system, the controller will not transition to RUN mode.

This fault is *not* automatically cleared on power-up; the user must specifically order the condition to be cleared. The default fault action for this group is Fatal.

Error Code:	0
Correction:	Clear the fault and retry the download of the program or configuration file.

Run Mode Store Failure

Error Code:	1
Description:	Communications was lost, or power went out during a run mode store. The new program was not activated and was deleted.
Correction:	Perform the run mode store again. This fault is diagnostic.
Error Code:	2
Description:	Communications was lost, or power went out during the cleanup of old blocks during a run mode store. The new program is installed, and the remaining blocks were cleaned up.
Correction:	None required. This fault is informational.
Error Code:	3
Description:	Communications was lost, or power went out in the middle of a run mode store.
Correction:	Delete and restore the program. This error is fatal.

SECTION 3
I/O Fault Table Explanations

The I/O fault table reports data about faults in three classifications. In descending order, these fault classifications are:

- Fault category.
- Fault type.
- Fault description.

All faults have a fault category, but a fault type and fault group may not be listed for every fault. Additional information, referred to as Fault Specific Data, can be accessed by pressing CTRL-F while the I/O fault table is displayed on the programmer screen. This section is organized by fault category.

The following table enables you to quickly find a particular fault explanation in this section. Each entry is listed as it appears on the programmer screen.

Fault Description	Page Number
Circuit Fault	3-27
Discrete Fault	3-28
Analog Fault	3-29
Low-Level Analog Fault	3-30
GENA Fault	3-30
Loss of IOC	3-31
Addition of IOC	3-31
Loss of I/O Module	3-31
Addition of I/O Module	3-32
Extra I/O Module	3-32
Loss of Block	3-32
Addition of Block	3-33
Extra Block	3-33
I/O Bus Fault	3-33
Module Fault	3-34
IOC Software Fault	3-34
IOC Hardware Failure	3-35
Forced and Unforced Circuit	3-35
Block Switch	3-35

The following table describes the information provided with each fault category.

Table 3-2. Fault Category Descriptions

Fault Category	Fault Type	Fault Description	Fault Specific Data
Circuit Fault	Discrete Fault	Loss of User Side Power	Circuit Configuration *
		Short Circuit in User Wiring	Circuit Configuration *
		Sustained Overcurrent	Circuit Configuration *
		Low or No Current Flow	Circuit Configuration *
		Switch Temperature Too High	Circuit Configuration *
		Switch Failure	Circuit Configuration *
		Point Fault	Circuit Configuration *
		Output Fuse Blown	Circuit Configuration *
	Analog Fault	Input Channel Low Alarm	Circuit Configuration *
		Input Channel High Alarm	Circuit Configuration *
		Input Channel Under Range	Circuit Configuration *
		Input Channel Over Range	Circuit Configuration *
		Input Channel Open Wire	Circuit Configuration *
		Output Channel Under Range	Circuit Configuration *
		Output Channel Over Range	Circuit Configuration *
		Invalid Data	Circuit Configuration *
		Expansion Channel Not Responding	Circuit Configuration *
	Low-Level Analog Fault	Input Channel Low Alarm	Circuit Configuration *
		Input Channel High Alarm	Circuit Configuration *
		Input Channel Under Range	Circuit Configuration *
		Input Channel Over Range	Circuit Configuration *
		Input Channel Open Wire	Circuit Configuration *
		Wiring Error	Circuit Configuration *
		Internal Fault	Circuit Configuration *
		Input Channel Shorted	Circuit Configuration *
		Invalid Data	Circuit Configuration *
	GENA Fault	GENA Circuit Fault	GENA Fault Byte 2
	Remote I/O Scanner Fault	Remote I/O Scanner Circuit Fault	Byte 1: Circuit Type Byte 2: I/O Type
Loss of IOC			Timeout Unexpected State Unexpected Mail Status VME Bus Error
Addition of IOC			
Loss of I/O Module			
Addition of I/O Module			
Extra I/O Module			—
Loss of Block	Fault Not Specified	Communications Lost	
Addition of Block			
Extra Block			
I/O Bus Fault	Bus Fault Bus Outputs Disabled		
Global Memory Fault			Subnet Group Number Global Variable Name

*) Refer to table on next page.

Table 3-2. Fault Category Descriptions - Continued

Fault Category	Fault Type	Fault Description	Fault Specific Data
Module Fault	Headend Fault	EPROM or NVRAM Failure Calibration Memory Failure Shared Ram Failure Configuration MisMatch Watchdog Timeout Output Fuse Blown	
IOC Software Fault			
IOC Hardware Failure			
Forced Circuit			Block Configuration * Discrete/Analog Indication*
Unforced Circuit			Block Configuration * Discrete/Analog Indication*

* Refer to table below.

Three types of fault specific data occur in more than one fault category; they are block configuration, circuit configuration, and analog/discrete indication. The codings are shown in the following table.

Value	Description
	Circuit Configuration
1	Circuit is an input.
2	Circuit is an output.
3	Circuit is an output with feedback.
	Block Configuration
1	Block is configured for inputs only.
2	Block is configured for outputs only.
3	Block is configured for inputs and outputs (grouped block).
	Discrete/Analog Indication
1	Block is a discrete block.
2	Block is an analog block.

Circuit Fault

The Fault Category **Circuit Fault** has four fault types. Three of the four fault types have fault descriptions. Fault specific data is available for all faults. Circuit fault applies specifically to Genius I/O modules. The default fault action is **Diagnostic**. The following table describes the circuit fault category.

Table 3-3. Circuit Fault Category Descriptions

Fault Category	Fault Type	Fault Description	Fault Specific Data
Circuit Fault	Discrete Fault	Loss of User Side Power	Circuit Configuration
		Short Circuit in User Wiring	Circuit Configuration
		Sustained Overcurrent	Circuit Configuration
		Low or No Current Flow	Circuit Configuration
		Switch Temperature Too High	Circuit Configuration
		Switch Failure	Circuit Configuration
		Point Fault	Circuit Configuration
		Output Fuse Blown	Circuit Configuration
	Analog Fault	Input Channel Low Alarm	Circuit Configuration
		Input Channel High Alarm	Circuit Configuration
		Input Channel Under Range	Circuit Configuration
		Input Channel Over Range	Circuit Configuration
		Input Channel Open Wire	Circuit Configuration
		Output Channel Under Range	Circuit Configuration
		Output Channel Over Range	Circuit Configuration
		Invalid Data	Circuit Configuration
		Expansion Channel Not Responding	Circuit Configuration
	Low-Level Analog Fault	Input Channel Low Alarm	Circuit Configuration
		Input Channel High Alarm	Circuit Configuration
		Input Channel Under Range	Circuit Configuration
		Input Channel Over Range	Circuit Configuration
		Input Channel Open Wire	Circuit Configuration
		Wiring Error	Circuit Configuration
		Internal Fault	Circuit Configuration
		Input Channel Shorted	Circuit Configuration
		Invalid Data	Circuit Configuration
	Remote Fault	Remote I/O Scanner Fault	

Discrete Fault

Discrete Fault has eight fault descriptions. More than one condition may be present in a particular reporting of the fault.

Name:	Loss of User Side Power
Description:	The Genius Bus Controller generates this error when there is a power loss on the field wiring side of a Genius I/O block.
Correction:	Correct the power failure.
Name:	Short Circuit in User Wiring
Description:	The Genius Bus Controller generates this error when it detects a short circuit in the user wiring of a Genius block. A short circuit is defined as a current level greater than 20 amps.
Correction:	Fix the cause of the short circuit.
Name:	Sustained Overcurrent
Description:	The Genius Bus Controller generates this error when it detects a sustained current level greater than 2 amps in the user wiring.
Correction:	Fix the cause of the over current.
Name:	Low or No Current Flow
Description:	The Genius Bus Controller generates this error when there is very low or no current flow in the user circuit.
Correction:	Fix the cause of the condition.
Name:	Switch Temperature Too High
Description:	The Genius Bus Controller generates this error when the Genius block reports a high temperature in the Genius Smart Switch.
Correction:	(1) Ensure that the block is installed to provide adequate circulation. (2) Decrease the ambient temperature surrounding the block.
Name:	Switch Failure
Description:	The Genius Bus Controller generates this error when the Genius block reports a failure in the Genius Smart Switch.
Correction:	Replace the Genius I/O block.
Name:	Point Fault
Description:	The PLC operating system generates this error when it detects a failure of a single I/O point on a Genius I/O module.
Correction:	Replace the Genius I/O block.
Name:	Output Fuse Blown
Description:	The PLC operating system generates this error when it detects a blown fuse on a Genius I/O output block.
Correction:	(1) Determine and repair the cause of the fuse blowing, and replace the fuse. (2) Replace the block.

Analog Fault

Analog Fault has nine fault descriptions. More than one condition may be present in a particular reporting of the fault.

Name:	Input Channel Low Alarm
Description:	The Genius Bus Controller generates this error when the Genius analog module reports a low alarm on an input channel.
Correction:	Correct the condition causing the low alarm.
Name:	Input Channel High Alarm
Description:	The Genius Bus Controller generates this error when the Genius analog module reports a high alarm on an input channel.
Correction:	Correct the condition causing the high alarm.
Name:	Input Channel Under Range
Description:	The Genius Bus Controller generates this error when the Genius analog module reports an under-range condition on an input channel.
Correction:	Correct the problem causing the condition.
Name:	Input Channel Over Range
Description:	The Genius Bus Controller generates this error when the Genius analog module reports an over-range condition on an input channel.
Correction:	Correct the problem causing the condition.
Name:	Input Channel Open Wire
Description:	The Genius Bus Controller generates this error when the Genius analog module detects an open wire condition on an input channel.
Correction:	Correct the problem causing the condition.
Name:	Output Channel Under Range
Description:	The Genius Bus Controller generates this error when the Genius analog module reports an under-range condition on an output channel.
Correction:	Correct the problem causing the condition.
Name:	Output Channel Over Range
Description:	The Genius Bus Controller generates this error when the Genius analog module reports an over-range condition on an output channel.
Correction:	Correct the problem causing the condition.
Name:	Invalid Data
Description:	The Genius Bus Controller generates this error when it detects invalid data from a Genius analog input block.
Correction:	Correct the problem causing the condition.
Name:	Expansion Channel Not Responding
Description:	The PLC operating software (I/O Scanner) generates this error when data from an expansion channel on a multiplexed analog input board is not responding.
Correction:	(1) Check wiring to the module. (2) Replace the module.

Low-Level Analog Fault

Low-Level Analog Fault has nine fault descriptions. More than one condition may be present in a particular reporting of the fault.

Name:	Input Channel Low Alarm
Description:	The Genius Bus Controller generates this error when the Genius analog module reports a low alarm on an input channel.
Correction:	Correct the condition causing the low alarm.
Name:	Input Channel High Alarm
Description:	The Genius Bus Controller generates this error when the Genius analog module reports a high alarm on an input channel.
Correction:	Correct the condition causing the high alarm.
Name:	Input Channel Under Range
Description:	The Genius Bus Controller generates this error when the Genius analog module reports an under-range condition on an input channel.
Correction:	Correct the problem causing the condition.
Name:	Input Channel Over Range
Description:	The Genius Bus Controller generates this error when the Genius analog module reports an over-range condition on an input channel.
Correction:	Correct the problem causing the condition.
Name:	Input Channel Open Wire
Description:	The Genius Bus Controller generates this error when the Genius analog module detects an open wire condition on an input channel.
Correction:	Correct the problem causing the condition.
Name:	Wiring Error
Description:	The Genius Bus Controller generates this error when the Genius analog module detects an improper RTD connections or thermocouple reverse junction fault.
Correction:	Correct the problem causing the condition.
Name:	Internal Fault
Description:	The Genius Bus Controller generates this error when the Genius analog module reports a cold junction sensor fault on a thermocouple block or an internal error in an RTD block.
Correction:	Correct the problem causing the condition.
Name:	Input Channel Shorted
Description:	The Genius Bus Controller generates this error when it detects an input channel shorted on a Genius RTD or Strain Gauge Block.
Correction:	Correct the problem causing the condition.
Name:	Invalid Data
Description:	The Genius Bus Controller generates this error when it detects invalid data from a Genius analog input block.
Correction:	Correct the problem causing the condition.

GENA Fault

The GENA Fault has no fault descriptions associated with it. GENA Fault Byte 2 is the first byte of the fault specific data.

Description:	The Genius I/O operating software generates this error when it detects a failure in a GENA block attached to the Genius I/O bus.
Correction:	Replace the GENA block.

Loss of IOC

The Fault Category Loss of IOC has no fault types or fault descriptions associated with it. The default fault action is Fatal.

Name:	Loss of or Missing IOC
Description:	The PLC operating software generates this error when it cannot communicate with an I/O Controller and an entry for the IOC exists in the configuration file.
Correction:	(1) Verify that the module in the slot/bus address is the correct module. (2) Review the configuration file and verify that it is correct. (3) Replace the module. (4) Display the PLC fault table on the programmer. Contact GE Fanuc PLC Field Service, giving them all the information contained in the fault entry.

Addition of IOC

The Fault Category Addition of IOC has no fault types or fault descriptions associated with it. The default fault action for this category is Diagnostic.

Name:	Addition of IOC
Description:	The PLC operating software generates this error when an IOC which has been faulted returns to operation or when an IOC is found in the system and the configuration file indicates that no IOC is to be in that slot.
Correction:	(1) No action is necessary if faulted module is in a remote rack and is returning due to a remote rack power cycle. (2) Update the configuration file or remove the module.

Loss of I/O Module

The Fault Category Loss of I/O Module applies to Model 70 I/O discrete and analog modules. There are no fault types or fault descriptions associated with this category. The default fault action is Diagnostic.

Name:	Loss of I/O Module
Description:	The PLC operating software generates this error when it detects that a Model 70 I/O module is no longer responding to commands from the PLC CPU, or when the configuration file indicates an I/O module is to occupy a slot and no module exists in the slot.
Correction:	(1) Replace the module. (2) Correct the configuration file. (3) Display the PLC fault table on the programmer. Contact GE Fanuc PLC Field Service, giving them all the information contained in the fault entry.

Addition of I/O Module

The Fault Category **Addition of I/O Module** applies to Model 70 discrete and analog I/O modules. There are no fault types or fault descriptions associated with this category. The default fault action is **Diagnostic.**

Name:	Addition of I/O Module
Description:	The PLC operating software generates this error when an I/O module which had been faulted returns to operation.
Correction:	(1) No action necessary if module was removed or replaced, or remote rack was power cycled. (2) Update the configuration file or remove the module.

Extra I/O Module

The Fault Category **Extra I/O Module** applies only to Model 70 I/O modules. There are no fault types or fault descriptions associated with this category. The default fault action is **Diagnostic.**

Name:	Extra I/O Module
Description:	The PLC operating software generates this error when it detects a Model 70 I/O module in a slot which the configuration file indicates should be empty.
Correction:	(1) Remove the module. (It may be in the wrong slot.) (2) Update and restore the configuration file to include the extra module.

Loss of Block

The Fault Category **Loss of Block** applies to Genius blocks. There are no fault types or fault descriptions associated with this category. The default fault action is **Diagnostic.**

Name:	Loss of Block
Description:	The PLC operating software generates this error when it receives a Loss of Block fault from a Genius Bus Controller, but the reason for the loss is unspecified.
Correction:	(1) Verify power and wiring to the block. (2) Replace the block.

Name:	Loss of Block - A/D Communications Fault
Description:	The Genius I/O operating software generates this error when it detects a loss of communications with a Genius I/O block.
Correction:	(1) Verify power and serial bus wiring to the block. (2) Replace the block.

Addition of Block

The Fault Category **Addition of Block** applies only to Genius blocks. There are no fault types or fault descriptions associated with this category. The default fault action is **Diagnostic.**

Name:	Addition of Block
Description:	The Genius operating software generates this error when it detects that a Genius block which stopped communicating with the controller starts communicating again.
Correction:	Informational only. None required.

Extra Block

The Fault Category **Extra Block** applies only to Genius I/O blocks. There are no fault types or fault descriptions associated with this category. The default fault action is **Diagnostic.**

Name:	Extra Block
Description:	The PLC operating software generates this error when it detects a Genius I/O block on the bus at a serial bus address which the configuration file should not have a block.
Correction:	(1) Remove or reconfigure the block. (It may be at the wrong serial bus address.) (2) Update and restore the configuration file to include the extra block.

I/O Bus Fault

The Fault Category **I/O Bus Fault** has two fault types associated with it. The default fault action is **Diagnostic.**

Name:	Bus Fault
Description:	The Genius Bus Controller operating software generates this error when it detects a failure with a Genius I/O bus.
Correction:	(1) Determine the reason for the bus failure and correct it. (2) Replace the Genius Bus Controller.
Name:	Bus Outputs Disabled
Description:	The Genius Bus Controller operating software generates this error when it times out waiting for the PLC CPU to perform an I/O scan.
Correction:	(1) Replace the PLC CPU. (2) Display the PLC fault table on the programmer. Contact GE Fanuc PLC Field Service, giving them all the information contained in the fault entry.
Name:	SBA Conflict
Description:	The Genius Bus Controller detected a conflict between its serial bus address and that of another device on the bus.
Correction:	Adjust one of the conflicting serial bus addresses.

Module Fault

The Fault Category **Module Fault** has one fault type, headend fault, and eight fault descriptions. No fault specific data is present. The default fault action for this category is **Diagnostic.**

Name:	Configuration Memory Failure
Description:	The Genius Bus Controller generates this error when it detects a failure in a Genius block's EEPROM or NVRAM.
Correction:	Replace the Genius block's electronics module.
Name:	Calibration Memory Failure
Description:	The Genius Bus Controller generates this error when it detects a failure in a Genius block's calibration memory.
Correction:	Replace the Genius block's electronics module.
Name:	Shared RAM Fault
Description:	The Genius Bus Controller generates this error when it detects an error in a Genius block's shared RAM.
Correction:	Replace the Genius block's electronics module.
Name:	Watchdog Timeout
Description:	The PLC operating system generates this error when it detects that a Model 70 input module watchdog timer has expired.
Correction:	Replace the Model 70 input module.
Name:	Output Fuse Blown
Description:	The PLC operating system generates this error when it detects a blown fuse on a Model 70 output module.
Correction:	(1) Determine and repair the cause of the fuse blowing, and replace the fuse. (2) Replace the module.
Name:	Module Fault
Description:	An internal failure has been detected in a module.
Correction:	Replace the affected module.

IOC Software Fault

The Fault Category **IOC Software Fault** applies to any type of I/O Controller. There are no fault types or fault descriptions associated with it. The default fault action is **Fatal.**

Name:	Datagram Queue Full, Read/Write Queue Full
Description:	Too many datagrams or read/write requests have been sent to the Genius Bus Controller.
Correction:	Adjust the system to reduce the request rate to the Genius Bus Controller.
Name:	Response Lost
Description:	The Genius Bus Controller is unable to respond to a received datagram or read/write request.
Correction:	Adjust the system to reduce the request rate to the Genius Bus Controller.

IOC Hardware Failure

The Fault Category IOC Hardware Failure has no fault types or fault descriptions. The default fault action is Diagnostic.

Description:	The Genius operating software generates this error when it detects a hardware failure in the Bus Communication hardware or a baud rate mismatch.
Correction:	(1) Verify that the baud rate set in the configuration file for the Genius Bus Controller agrees with the baud rate programmed in every block on the bus. (2) Change the configuration file and restore it, if necessary. (3) Replace the Genius Bus Controller. (4) Selectively remove each block from the bus until the offending block is isolated and replace it.

Forced and Unforced Circuit

The Fault Categories Forced Circuit and Unforced Circuit report point conditions and therefore are not technically faults. They have no fault types or fault descriptions. These reports occur when a Genius I/O point was forced or unforced with the Hand-Held Monitor. The default fault action is Informational.

Fault Specific Data contains data as shown below.

Byte Number	Description
1	Block Configuration
2	Analog/Discrete Information

Block Switch

The Fault Category Block Switch has no fault types or fault descriptions. The default fault action is Diagnostic.

Name:	Block Switch
Description:	The PLC generates this error when a Genius block on redundant Genius buses switches from one bus to another.
Correction:	(1) No action is required to keep the block operating. (2) The bus that the block switched from needs to be repaired. (a) Verify the bus wiring. (b) Replace the I/O controller. (c) Replace the Bus Switching Module (BSM).