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TOSHIBA CORPORATION
NED

NRW-FPGA-Based I&C System Qualification Project

Unit Detailed Design Specification

Title:

OPRM Unit Detailed Design Specification for Power Range Neutron Monitor

Customer Name	None
Project Name	NRW-FPGA-Based I&C System Qualification Project
Item Name	OPRM Equipment
Item Number	C51
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Open Items

No.	Document Section	Description	Measures / Solutions	Responsible Group	Due Date	Status
1	General	RTM for OPRM unit DDS have not been issued.	NICSD issued RTM (FC51-3704-1007 Rev.0).	NED NICSD	Jan.13.2012	Close
2	Sec.6.1.3 Sec.6.2.3	Explanation for “guide key” is insufficiency.	NICSD added the figure for “guide key” in OPRM unit DDS (FC51-3702-1000 Rev.1).	NICSD	Jan.13.2012	Close

Table of Contents

Acronyms

ABA	Amplitude Based detection Algorithm
ABWR	Advanced Boiling Water Reactor
AC	Alternating Current
APRM	Average Power Range Monitor
AWG	American Wire Gauge
BSL	Back SLot
CI	Communication Interface
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DC	Direct Current
DDS	Detailed Design Specification
EDS	Equipment Design Specification
EEPROM	Electronically Erasable and Programmable Read Only Memory
ELCS	ESF Logic & Control System
ESF	Engineered Safety Features
FD	Flat Display
FG	Frame Ground
FMEA	Failure Mode Effect Analysis
FPGA	Field Programmable Gate Array
FSL	Front SLot
GRA	Growth Rate detection Algorithm
HMI	Human-Machine Interface
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
JCS	Japanese Cable makers' association Standard
LED	Light Emitting Diode
LPRM	Local Power Range Monitor
LSB*	Least Significant Bit
MCR	Main Control Room
MSB*	Most Significant Bit
MTBF	Mean Time Between Failures
MTTR	Mean Time To Repair
NED	Nuclear Energy Systems and Services Division
NICSD	Nuclear Instrumentation and Control Systems Department
NMS	Neutron Monitoring System
NQ	Nuclear Quality standard
OPRM	Oscillation Power Range Monitor
PBDA	Period Based Detection Algorithm
PFC	Power Factor Correction module
PICS	Plant Information and Control System
PRNM	Power Range Neutron Monitor
PSSL	Power Supply SLot
RPS	Reactor Protection System
RTM	Requirements Traceability Matrix
SOE	Sequence of Event
SRAM	Static Random Access Memory
TDR	Transient Data Recorder
UL	Underwriters Laboratories Inc.
UL	Upper Left
UR	Upper Right
LL	Lower Left
LR	Lower Right
V&V	Verification and Validation
VW	Vertical Wire

(Note*:MSB and LSB shown in section 6 show bit position of data information except parity and alarm information.)

1. Scope

This document describes equipment design specifications for the Oscillation Power Range Monitor (OPRM) unit which is part of the Power Range Neutron Monitor (PRNM) subsystem.
The PRNM which described in this document is developed for Advanced Boiling Water Reactor (ABWR) plants.
Requirements for the unit design includes applicable documents, system outline, configuration and structure of product, development elements/ functional specifications, external interface specifications, performance, initializing process, self diagnosis function, environmental requirements and parts list.
This Unit Detailed Design Specification (DDS) is based on requirements from Equipment Design Specification (EDS) (Reference 2.2 (1)) and the traceability of the requirements between Unit DDS and EDS are confirmed in Requirements Traceability Matrix (RTM).

2. Applicable Documents

2.1. Applicable Regulations, Codes and Standards

Following codes and standards are applicable to the OPRM unit to the extent specified herein.

(1) IEC 60603-2-1995 Connectors for frequencies below 3 MHz for use with printed boards - Part 2: Detail specification for two-part connectors with assessed quality, for printed boards, for basic grid of 2.54 mm (0.1 in) with common mounting features Amendment No.1 (2000)
(2) UL94-2003 Standard for Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
(3) UL224-1999 Extruded Insulating Tubing
(4) UL758-2004 Standard for Appliance Wiring Material
(5) JCS1236-2001 Woven copper wire
(6) TOSHIBA NICSD NQ-2005 Preparation Procedure for Detailed Design Specification
(7) TOSHIBA NICSD NQ-2036 Procedure for Design Control
(8) EPRI TR-107330 Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety related Applications in Nuclear Power Plants, December 1996
(9) IEEE 802.3 2008 Ethernet

Note: The latest revision of the NICSD NQ-standard is applicable.

2.2. Reference Documents

(1) TOSHIBA NICSD FC51-3002-1000 Rev.3 Equipment Design Specification for Power Range Neutron Monitor (EDS)

3. System Outline

The OPRM is a functional subsystem of the Average Power Range Monitor (APRM). There are four OPRM channels, with each OPRM as part of the each APRM channel.

Figure 4-1 of EDS (Reference 2.2(1)) shows an overall configuration of the PRNM for one division.

The OPRM unit monitors neutron flux oscillation.
The OPRM unit receives the 52 Local Power Range Monitor (LPRM) Levels (Total 52 detectors) from 4 LPRM units and forms 44 OPRM Cell configurations to monitor the neutron flux behavior of all regions of the core. Each OPRM Cell represents a combination of four LPRM signals selected from the LPRM strings at the four corners of a four-by-four fuel bundle square region. For locations near the periphery where one corner of the square does not include an LPRM string, the OPRM Cells use the inputs from the remaining three LPRM strings.
For each Cell, the peak to average value of the OPRM signal is determined to evaluate the amplitude of oscillation and to be used in the setpoint algorithm. The OPRM trip protection algorithm consists of trip logic depending on signal oscillation amplitude, a signal oscillation period, and signal oscillation growth rate.
If one of Cell fulfills one of algorithm, the OPRM unit generates a trip signal.

Bypass of one APRM channel also bypass one corresponding OPRM channel. The OPRM unit also receives the APRM Level and the Core Flow Level from the APRM unit and the trip algorithms are automatically bypassed if APRM Level is less than 30% (initial setpoint) or Core Flow Level is grater than 60% (initial setpoint).

The OPRM unit generates trip, alarm and inoperative signal to Reactor Protection System (RPS) by way of the Relay units. The OPRM also generates various outputs to the Plant Information and Control System (PICS), Sequence of Event (SOE) and Transient Data Recorder (TDR) via Non-Safety-Related Communication Interface (CI) and Engineered Safety Features (ESF) Logic & Control System Flat Display (ELCS FD) via Safety-Related CI.

The OPRM units in every division have the same functions.

3.1. New Design or Verified Design

The OPRM unit is newly designed for ABWR. The OPRM unit is verified by Verification and Validation (V&V) activity.

3.2. Difference from Verified Design

There are no verified designs.

3.3. New Technology to be Adopted

There is no specific new technology for the OPRM unit in this project.

4. Configuration and Structure of Product

4.1. Hardware Component Configuration

The OPRM unit consists of the unit chassis and the modules with different functions. The unit chassis includes a middle plane which consists of a front middle plane and a rear middle plane. The front middle plane is a print circuit board with connectors for connecting with the front modules. The rear middle plane is a print circuit board with connectors for connecting with the rear modules. The middle plane, which has no active device, logic device, Central Processing Unit (CPU) or FPGA device, performs Direct Current (DC) power distribution and the signal communication between the modules.

(1) The OPRM unit has a chassis structure on which multiple modules can be mounted adopting modular design to support module replacement in the field.
(2) The dimensions of the OPRM unit shall be as follows (excluding protrusion).
Height (H)
Width (W)
Depth (D)
(3) The mass of the OPRM unit shall be
(4) The OPRM unit has connectors on the rear panel as shown in Figure 4-2.

4.1.1. Unit Chassis Requirements

The OPRM unit chassis shall be designed as follows.
(1) Structural Specification
External Dimensions
Mass
Material
(2) Electrical Specification
Grounding Terminal
Grounding
Middle plane –
Side plate –
(3) Front Middle Plane Specification
External Dimensions
Material
Connector
With front module:
C-type 96-pin (socket contact),
With rear middle plane:
C-type 96-pin (socket contact),
(4) Rear Middle Plane Specification
External Dimensions
Material
Connector
With rear module:
C-type 96-pin (socket contact),
With power supply module:
H-type 15-pin (socket contact),
With front middle plane:
C-type 96-pin (pin contact),

(pin contact/with shroud)
R-type 96-pin (pin contact), [ ]a,c

(5) Middle Plane Circuit Connection
The middle plane circuit design shall be performed in accordance with pin assignment described in Section 6.4.

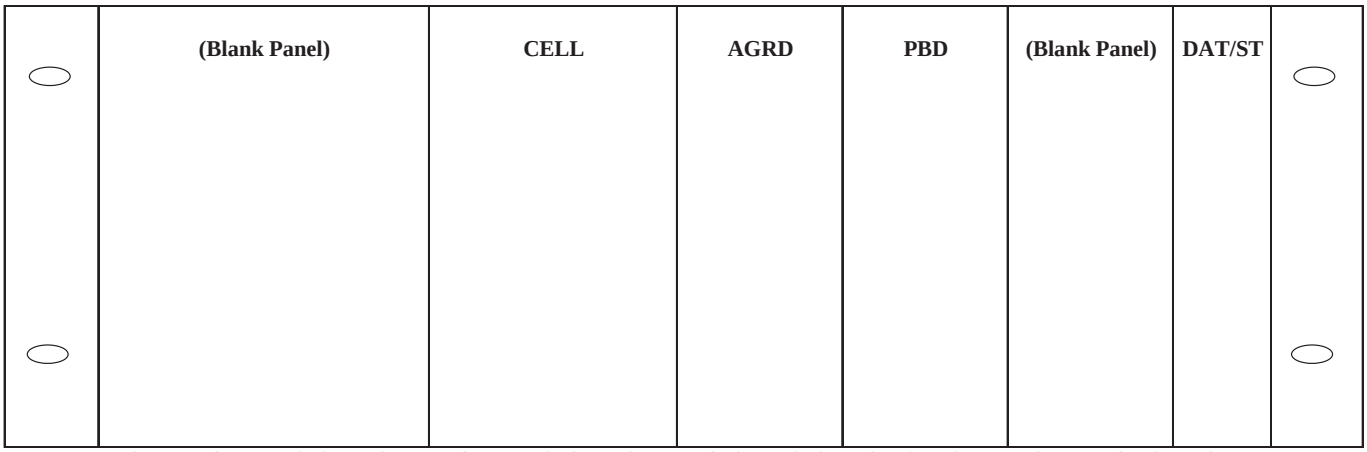
(6) Wire
Used Wire [ ]a,c
Detail wires specifications are described in Table 4-1 equivalent.

Table 4-1 Wire Specification for Unit Chassis

	Use part	Equivalent type	Specification	Voltage resistance	Rated voltage	Rated temperture	Remark
Grounding Line	[ ]a,c						

4.1.2. Module Configuration

The OPRM unit is configured by modules shown in Figure 4-1, Figure 4-2, Table 4-2 and Table 4-3.
The OPRM unit shall be configured as shown in Figure 4-1 and Figure 4-2.
Each module is mounted in FSL shown in Figure 4-1.

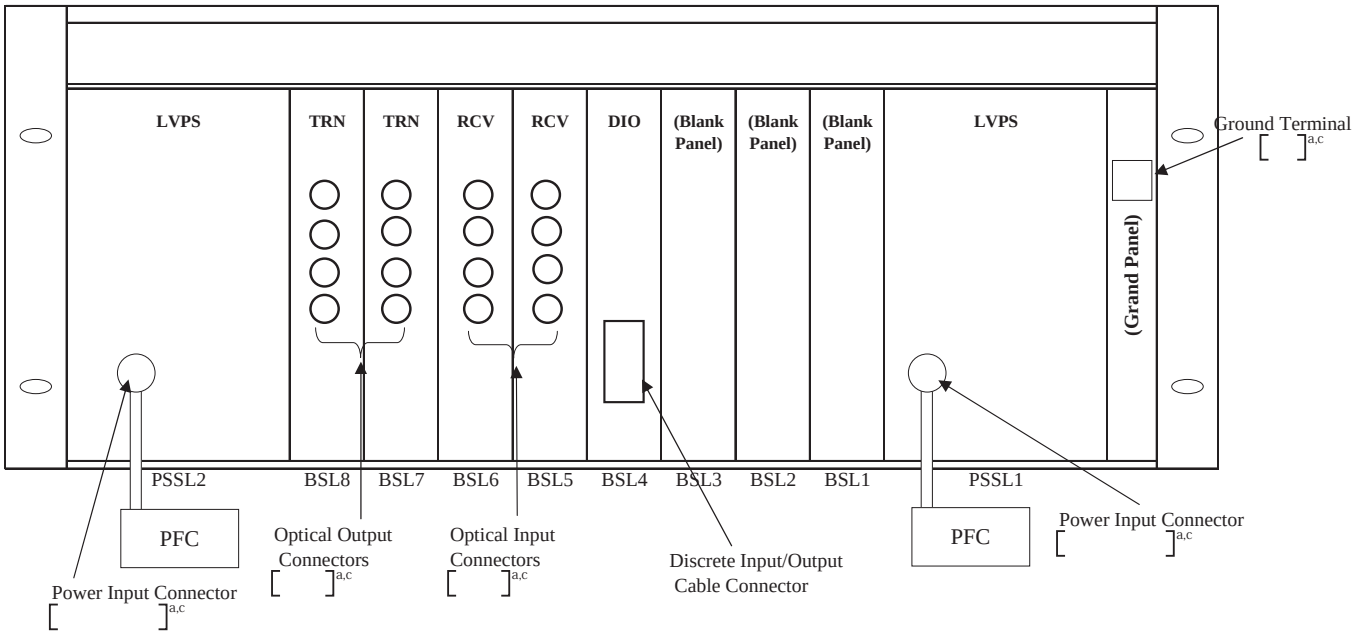


Note: The signage in a figure is an object for explanation, and differs from the actual signage.
*FSL: Front SLot

Figure 4-1 Front Module Configuration Diagram

Table 4-2 Front Module Configuration

Slot ID	Module Name	Description
FSL1	-	Blank panel
FSL2		
FSL3		
FSL4		
FSL5 to 7	CELL	LPRM Levels are converted to Normalized Oscillation Signal.
FSL8 to 9	AGRD	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.
FSL10 to 11	PBD	Period-Based Detection Algorithm judgment is performed.
FSL12	-	Blank panel
FSL13		
FSL14	DAT/ST	Power status are indicated on the front panel. Input status are indicated on the front panel. Data are multiplexed.



*PSSL: Power Supply Slot
BSL: Back Slot

**: Unused port shall use cover.

Figure 4-2 Rear Module Configuration Diagram

Table 4-3 Rear Module Configuration

Slot ID	Module Name	Description
PSSL 1	LVPS	+5V, ±15V are supplied each module. (LVPS1)
BSL 1	-	Blank Panel
BSL 2	-	Blank Panel
BSL 3	-	Blank Panel
BSL 4	DIO	Discrete input are received from the Relay unit.
		Discrete output are provided to the Relay unit.
BSL 5	RCV	LPRM Unit Data are received form LPRM unit.
BSL 6	RCV	APRM Unit Data are received form APRM unit.
BSL 7	TRN	OPRM Unit Data are transmitted to ELCS and PICS.
BSL 8	TRN	OPRM Unit Data are transmitted to TDR, SOE and PC.
PSSL 2	LVPS	+5V, ±15V are supplied each module. (LVPS2)
External	Power Factor Correction module (PFC)	Input line filter for LVPS module.

4.1.3. General Requirement for Modules

The general requirements for each module are shown below.

(1) Following modules in the OPRM unit shall use Non-Rewritable FPGA.
Details of modules are described in Section 5.2.

- CELL module
- AGRD module
- PBD module
- DAT/ST module
- TRN module
- RCV module

(2) The coating shall be applied to the both sides* of all print circuit boards of each module for water resistance and preventing a whisker. (* excluding the portion which automatic coating cannot be applied)
Coating Material [ ]a,c

(3) OPRM unit has many types of modules. Each module has the different specification.

1. Module Type [ ]a,c

Dimensions	Width	[ ]a,c
	Height	[ ]a,c
	Depth	[ ]a,c
	(Front handles are not included.)	
Body Material	Front panel: [ ]	a,c
Board Material	[ ]	a,c
Connector	C-type 96-pin (pin contact), [ ]	a,c
Applicable Module	DAT/ST module	

2. Module Type [ ]a,c

Dimensions	Width	[ ]a,c
	Height	[ ]a,c
	Depth	[ ]a,c
	(Front handles are not included.)	
Body Material	Front panel: [ ]	a,c
Board Material	[ ]	a,c
Connector	C-type 96-pin (pin contact), [ ]	a,c
Applicable Module	AGRD module, PBD module	

3. Module Type [ ]a,c

Dimensions	Width	[ ]a,c
	Height	[ ]a,c
	Depth	[ ]a,c
	(Front handles are not included.)	
Body Material	Front panel: [ ]	a,c
Board Material	[ ]	a,c
Connector	C-type 96-pin (pin contact), [ ]	a,c
Applicable Module	CELL module	

4. Module Type [ ]a,c

Dimensions	Width	[ ]a,c
	Height	[ ]a,c
	Depth	[ ]a,c
	(Front handles are not included.)	
Body Material	Front panel: [ ]	a,c (*1)
*1: Front Panel Surface Treatment of RCV module and TRN module is [ ]		a,c
Board Material	[ ]	a,c
Connector	C-type 96-pin (pin contact), [ ]	a,c
Applicable Module	TRN module, RCV module, DIO module	

5. Module Type [ ]a,c

Dimensions	Width	[ ]a,c
	Height	[ ]a,c
	Depth	[ ]a,c
	(Front handles are not included.)	
Body Material	Front panel: [ ]a,c	
Board Material	[ ]a,c	
Connector	H-type 15-pin (pin contact), [ ]a,c	
Applicable Module	LVPS module	

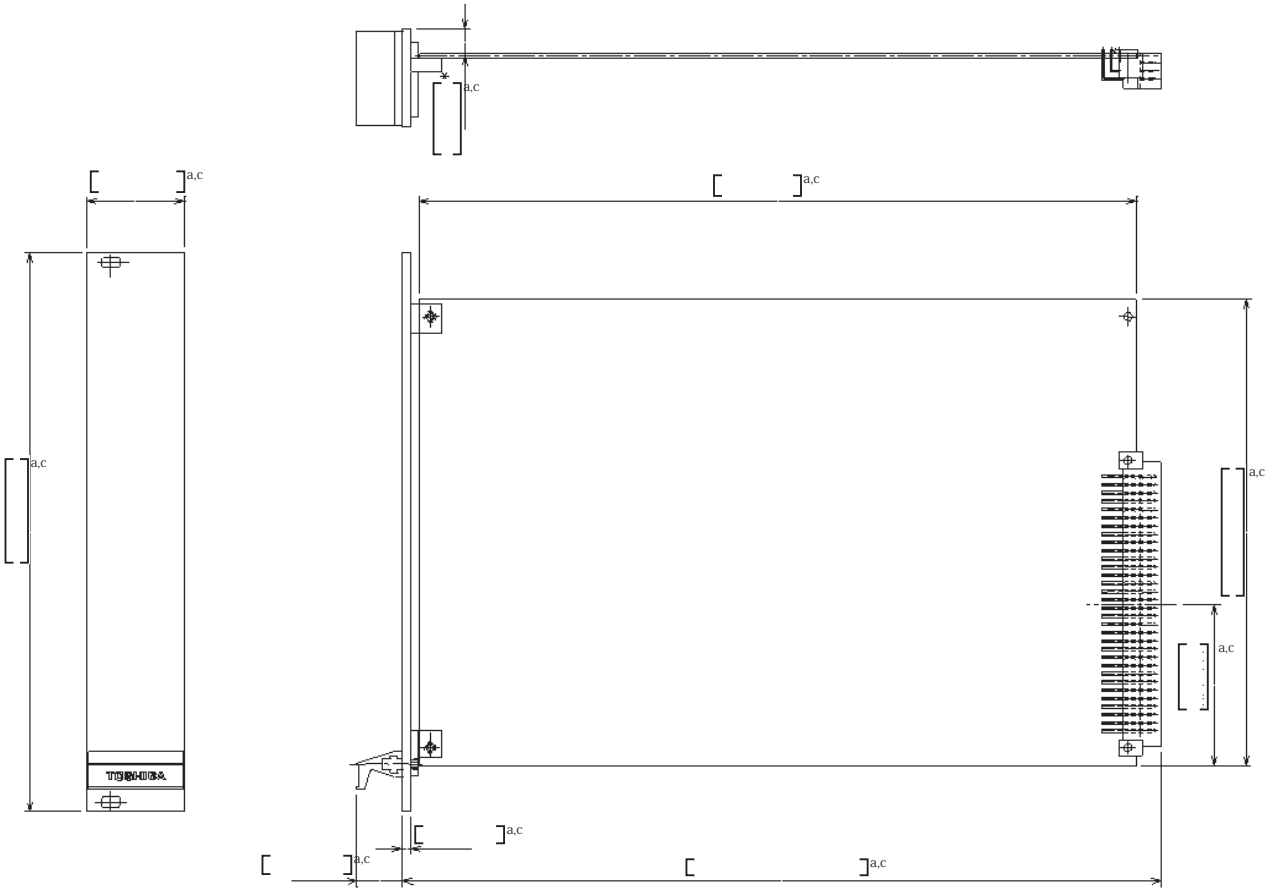
(4) Wire

Used Wire [ ]a,c

Detail wires specifications are described in Table 4-4 equivalent.

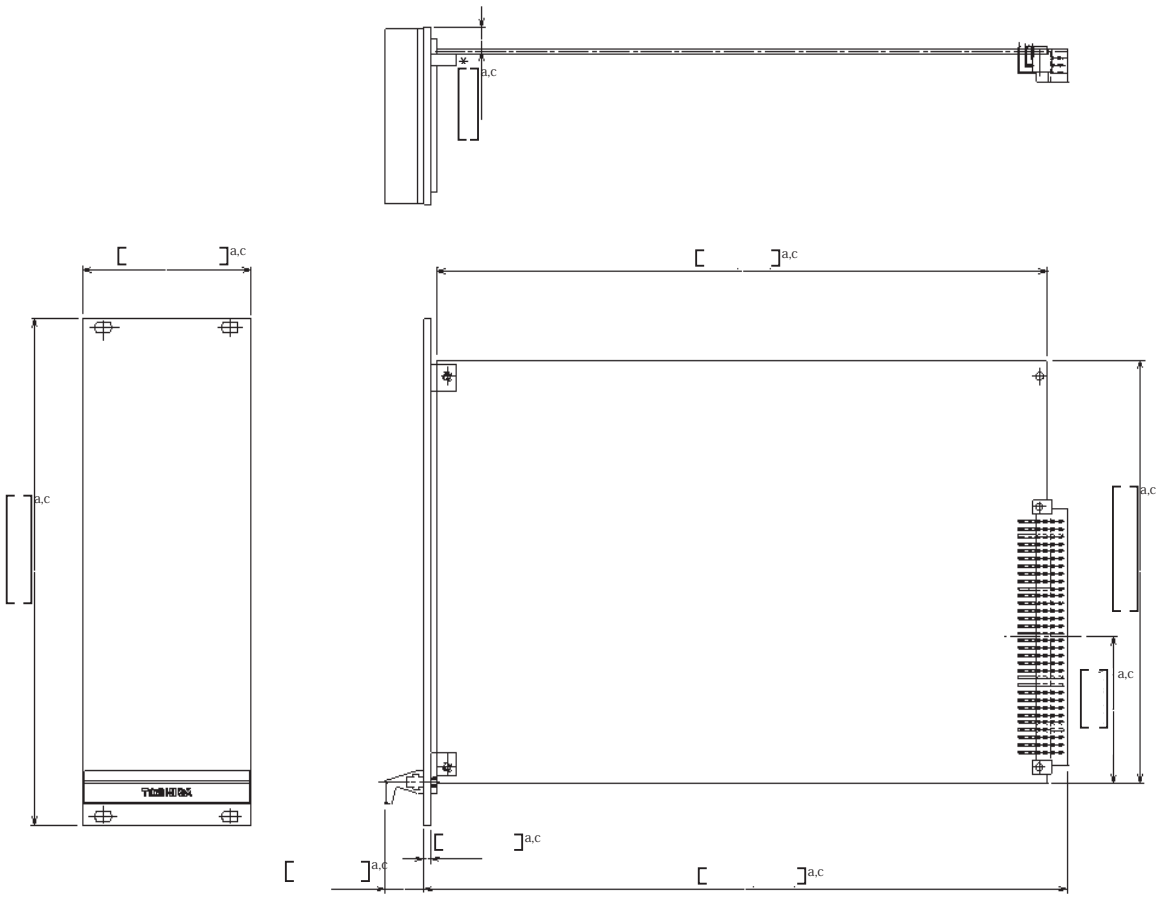
Table 4-4 Wire Specification for Modules

	Use part	Equivalent type	Specification	Voltage resistance	Rated voltage	Rated temperture	Remark
Between board and front panel	[ ]a,c						
Between board and connector							



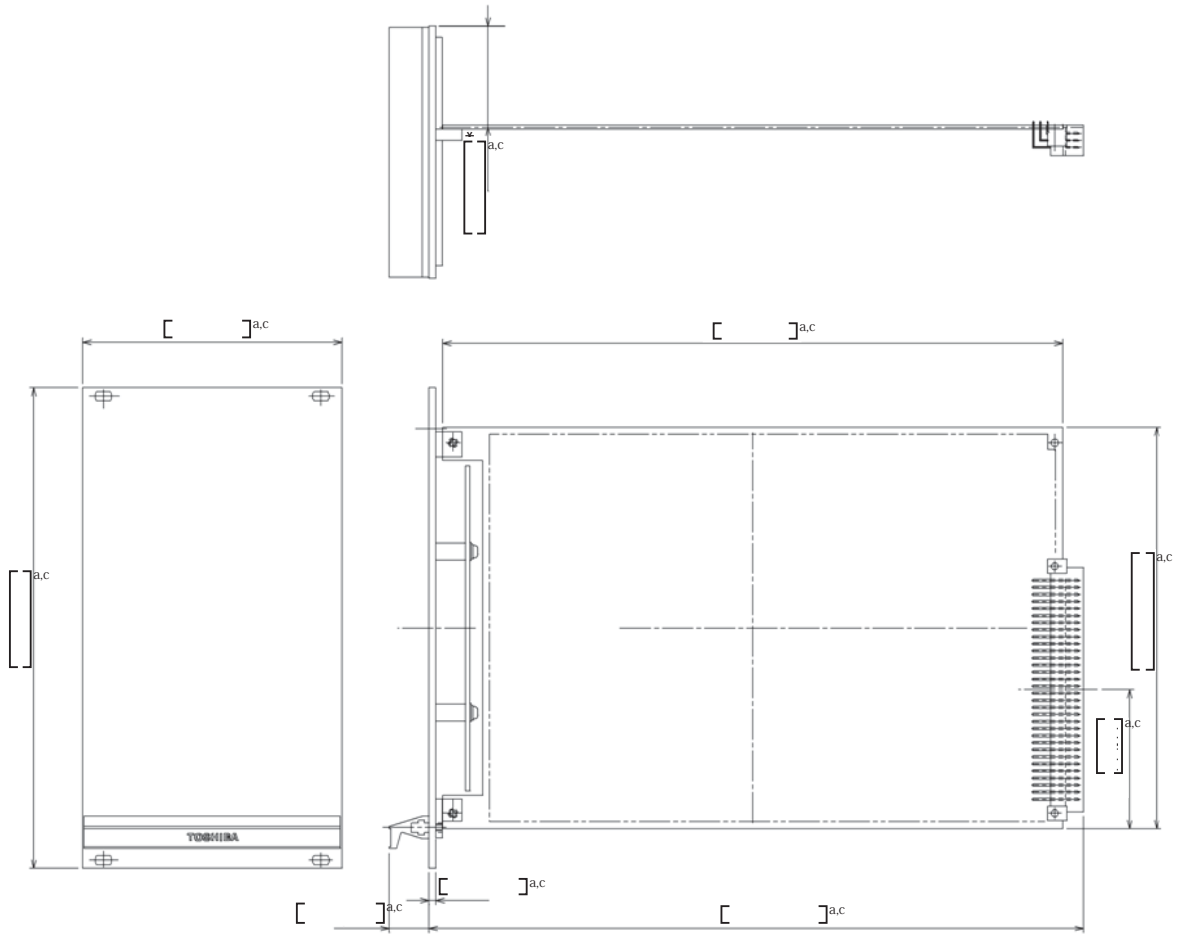
*From center of the board.

Figure 4.3 Outline Drawing of Type[ ]a,c



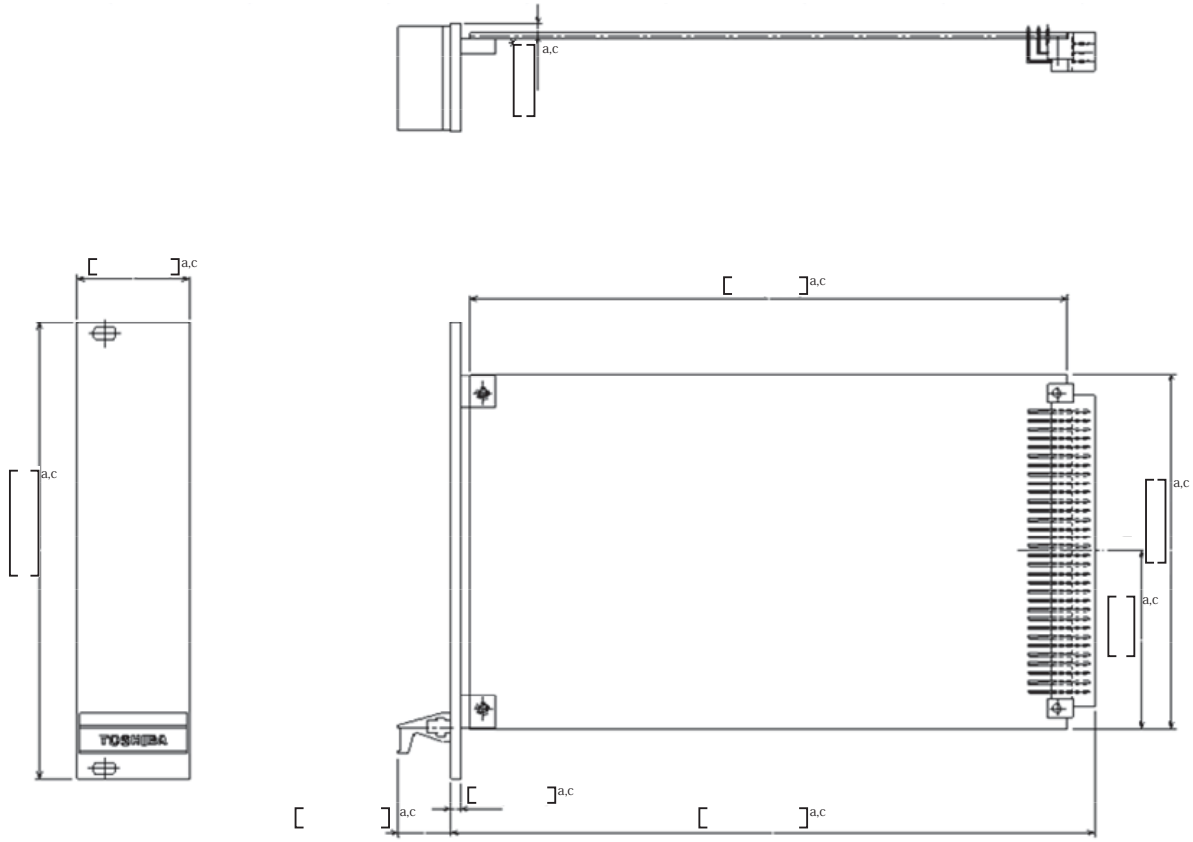
*From center of the board.

Figure 4.4 Outline Drawing of Type[ ]a,c



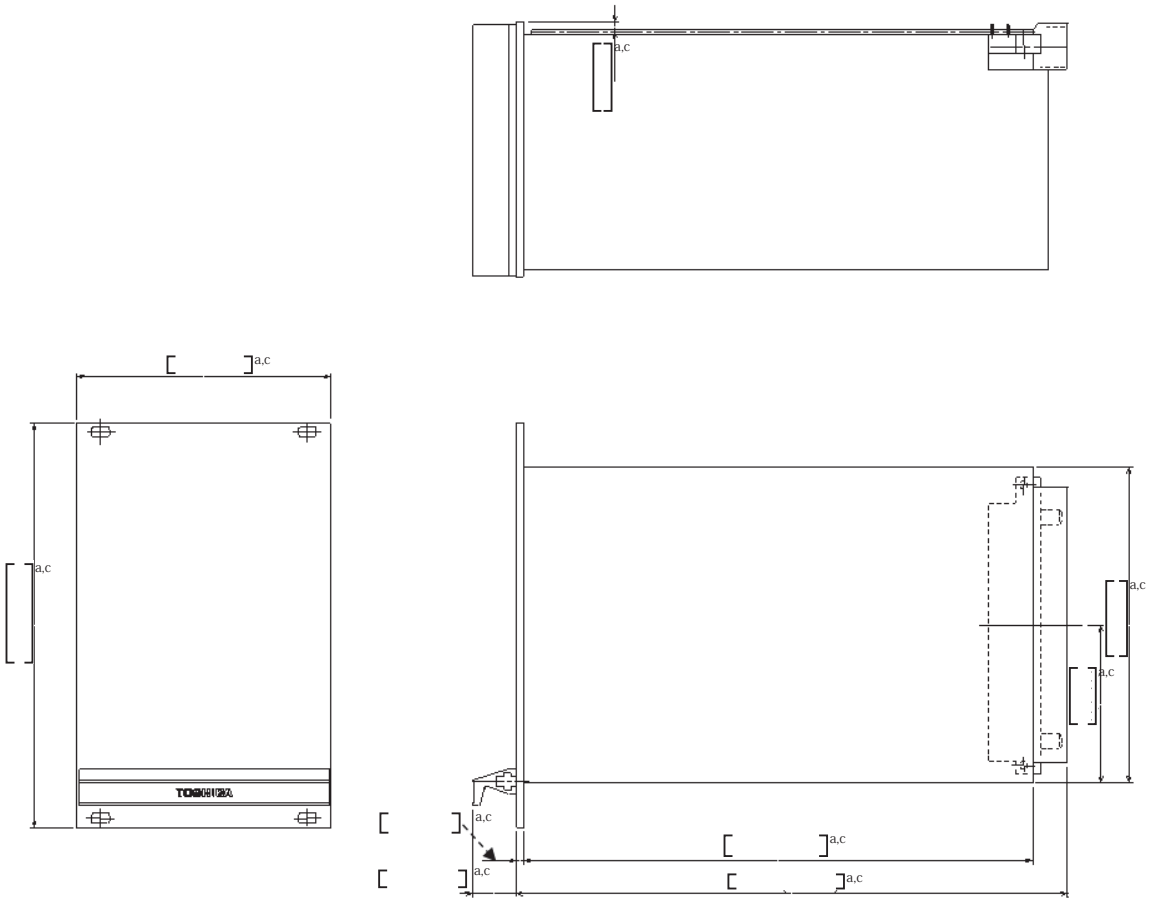
*From center of the board.

Figure 4.5 Outline Drawing of Type [ ]a,c



*From center of the board.

Figure 4.6 Outline Drawing of Type [ ]a,c



*From center of the board.

Figure 4.7 Outline Drawing of Type[ ]a,c

4.1.4. Module Mass

The module mass shall be designed as follows.

(1) CELL Module [ ]a,c
(2) AGRD Module [ ]a,c
(3) PBD Module [ ]a,c
(4) DAT/ST Module [ ]a,c
(5) LVPS Module [ ]a,c
(6) DIO Module [ ]a,c
(7) TRN Module [ ]a,c
(8) RCV Module [ ]a,c

4.2. Power Supply Configuration

The OPRM unit has two internal power supplies (LVPS modules) for redundancy. LVPS module can be used with external Power Factor Correction module (PFC). PFC receives Alternating Current (AC) voltage from an external AC power supply. The AC voltage is converted into DC voltage (about) by PFC. PFC supplies DC voltage to an LVPS module. The DC voltage (about) from PFC is converted into DC voltage (+5VDC, +15VDC,-15VDC) by the LVPS module. LVPS module supplies the other modules inside the unit with the DC voltage (+5VDC, +15VDC,-15VDC). The detail requirement for the LVPS module is described in Section 5.2.8.

(1) The OPRM unit shall have two internal power supplies (LVPS modules) for redundancy.
(2) A single power supply unit shall have the capability to supply the power which needs for unit operation.
(3) One power supply failure shall not influence to other power supply.

4.2.1 Unit Power Supply Input

(1) The power rating for the OPRM unit shall be designed as follows.
A) Input Voltage 220VDC
B) Input Current [ ]a,c

4.2.2 Module Power Supply Input

The power rating for each module shall be designed as follows:

(1) CELL Module
+5VDC±5% [ ]a,c
+15VDC±5% N/A
-15VDC±5% N/A

(2)AGRD Module
+ 5VDC±5% [ ]a,c
+15VDC±5% N/A
-15VDC±5% N/A

(3) PBD Module
+ 5VDC±5% [ ]a,c
+15VDC±5% N/A
-15VDC±5% N/A

(4) DAT/ST Module
+ 5VDC±5% [ ]a,c
+15VDC±5% N/A
-15VDC±5% N/A

(5) DIO Module
+ 5VDC±5% [ ]a,c
+15VDC±5% N/A

-15VDC±5%	N/A

(6) TRN Module

+ 5VDC±5%	[ ]a,c
+15VDC±5%	N/A
-15VDC±5%	N/A

(7) RCV Module

+ 5VDC±5%	[ ]a,c
+15VDC±5%	N/A
-15VDC±5%	N/A

5. Development Elements and Functional Specifications

In this project, there are no development elements for the OPRM unit.
This section focuses on the functional specifications for the OPRM unit. The functional requirements for the OPRM unit are described in Section 5.2.2.3 of EDS for PRNM (Reference 2.2(1)). As described in Section 4.1, the OPRM unit adopts modular design. The functions of the OPRM unit are accomplished by combination of each module function. The block diagram for OPRM unit processing is shown in Figure 5-1 including descriptions of each module's functions. Functions of the OPRM unit are divided into the safety-related and non-safety-related functions which are defined in the EDS (Reference 2.2(1)). Section 5.1 describes the functional requirements for the OPRM unit. The functional requirements for each module are described in Section 5.2.

5.1. Functional Specifications for Unit

5.1.1. Description of Safety-Related Functions

The OPRM unit has the following safety-related functions:

(1) Generate the following signals:
- Neutron flux oscillation

(2) Generate the following trip signals, as the OPRM functions and provide to the Relay unit:
- Growth Rate-Based Trip (GRA Trip)
- Amplitude-Based Maximum Trip (ABA Trip)
- Period-Based Trip (PBDA Trip)
- OPRM Inoperative

(3) Provide the data signals, bypass state, trip state, annunciator, and operation state to the ELCS FD.

5.1.2. Description of Non-Safety-Related Functions

The OPRM has the following non-safety-related functions:

(1) Provide data signals including recording transient data, and trip indications to the following external systems via Non-Safety-related Interface:
- PICS
- TDR and SOE

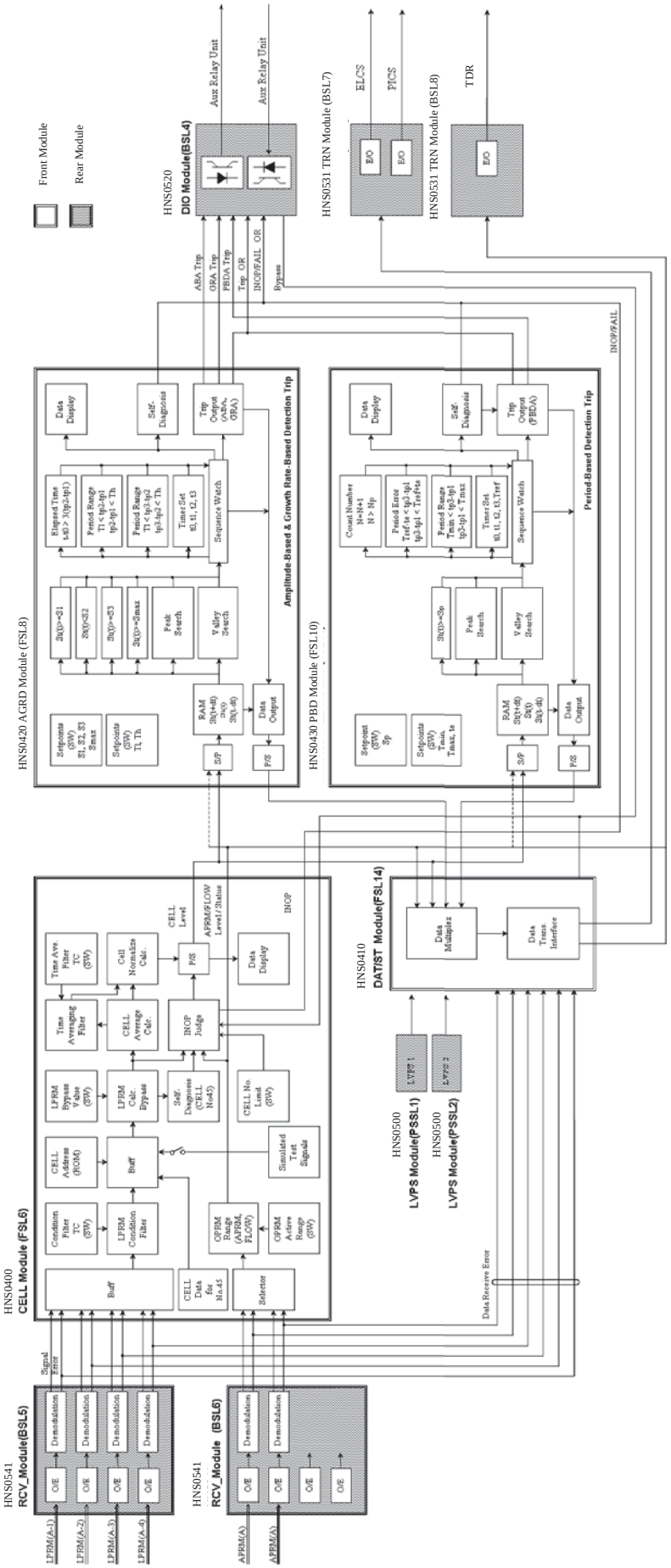


Figure 5-1 OPRM Unit Block Diagram

5.1.3. OPRM Signal Processing

The OPRM unit performs the following signal processing.

1. The OPRM unit shall receive LPRM Level from the four LPRM units via the RCV module.
2. The OPRM unit shall calculate the LPRM Levels assigned to each Cell using the signal processing function of the CELL module described in Section 5.2.1 to find Normalized Oscillation Signal.
3. The OPRM unit shall generate ABA Trip when any of the Normalized Oscillation Signals for each Cell meets the Amplitude Based Detection Algorithm trip condition.
4. The OPRM unit shall generate GRA Trip when any of the Normalized Oscillation Signals for each Cell meets the Growth Rate-Based Algorithm trip condition.
5. The OPRM unit shall generate PBDA Trip when any of the Normalized Oscillation Signals for each Cell meets the Period Based Detection Algorithm trip condition.
6. OPRM unit shall generate OPRM Trip signal when ABA Trip or GRA Trip or PBDA Trip is detected.
7. The OPRM unit shall receive APRM Level, Core Flow Level, and APRM Unit Data from an APRM unit via the RCV module.
8. The OPRM unit shall use the APRM Level and Flow Level as described in Section 5.2.1 to perform an OPRM Automatic Bypass judgment in the CELL module.The OPRM unit shall generate the minor failure signal when any of the CELL, AGRD, PBD or DAT/ST modules generates a minor failure signal.The OPRM unit shall generate the inoperative signal when any of the CELL, AGRD, or PBD modules generates an inoperative signal.
11. The Normalized Oscillation Signal and OPRM Alarm signals shall be connected to the each module via middle planes described in Section 6.3 and Section 6.4.
12. Discrete signals described in Section 6.2.3 shall be provided to external system from the DIO module.
13. Transmission data described in Sections 6.2.1 and 6.2.2 shall be provided to external system from the TRN module.

5.1.4. OPRM Unit Operation Mode

The OPRM unit shall have three operation modes which can set CELL module, AGRD module and PBD module. The Operation modes of CELL module, AGRD module and PBD module shall be OP, STANDBY and CAL. The operation mode of CELL module, AGRD module and PBD module are described in Sections 5.2.1, 5.2.2 and 5.2.3.

5.1.5. Trip and Alarm Generation

Trip and Alarm generation functions are described in Sections 5.2.2 and 5.2.3.

5.1.6. Trip and Alarm Reset Requirements

Trip and Alarm reset functions are described in Sections 5.2.2 and 5.2.3.

5.1.7. Panel Display of OPRM Unit

Panel displays of OPRM unit are described in Sections 5.2.1, 5.2.2, 5.2.3, .5.2.4, 5.2.5 and 5.2.6.
The OPRM unit shall provide indications of the Growth Rate-Based Trip, Amplitude-Based Maximum Trip, and Period-Based Trip signals against test signals, while the OPRM unit is bypassed.

5.1.8. Setpoint Adjustment Function

The setpoints of OPRM unit and its adjustment functions are described in Sections 5.2.1, 5.2.2 and 5.2.3.

5.2. Functional Requirements for Modules

5.2.1. CELL Module

The CELL module is inserted into the OPRM unit. The CELL module is required to have the following functions.

1. Input

LPRM Unit Data Input

The CELL module shall receive the LPRM Unit Data from RCV module via middle plane described in Section 6.3.1.

APRM Unit Data Input

The CELL module shall receive the APRM Unit Data from RCV module via middle plane described in Section 6.3.2.

LPRM Unit Data Input Error Signal Input

The CELL module shall receive the LPRM unit input error signal from RCV module via middle plane described in Section 6.3.9.

APRM Unit Data Input Error Signal Input

The CELL module shall receive the APRM unit input error signal from RCV module via middle plane described in Section 6.3.10.

APRM Bypass Signal Input

The CELL module shall receive the APRM Bypass signal from DIO module via middle plane described in Section 6.3.11.

OPRM Inoperative Signal Input

The CELL module shall receive the OPRM Inoperative signal from PBD module via middle plane described in Section 6.3.12.

Low Voltage Power Input

The CELL module shall receive DC power from LVPS module via middle plane.
Input power is described in Section 4.2.2.

2. Output

OPRM Cell Data Output

The CELL module shall provide the OPRM Cell Data to AGRD, PBD and DAT/ST modules via middle plane described in Section 6.3.3.

OPRM Calculation Data Output

The CELL module shall provide the OPRM calculation data to DAT/ST module via middle plane described in Section 6.3.4.

OPRM Inoperative Signal Output

The CELL module shall provide the OPRM Inoperative signal to AGRD, PBD, DAT/ST and DIO modules using [ ]a,c in the middle plane described in Section 6.3.12.

OPRM Minor Failure Signal Output

The CELL module shall provide the OPRM Minor Failure signal to AGRD, PBD, DAT/ST and DIO modules using [ ]a,c in the middle plane described in Section 6.3.13.

CELL Module Input Data Error Signal Output

The CELL module shall provide the CELL module input data error signal to DAT/ST module via middle plane described in Section 6.3.14.
The CELL module shall generate the CELL Module Input Data Error Signal at following Conditions.

- Timeout error is detected.

[ ]a,c

OPRM Automatic Bypass Signal Output

The CELL module shall provide the OPRM Automatic Bypass signal to DIO module via middle plane described in

Section 6.3.15.

APRM Unit Data Select Signal Output

The CELL module shall provide the APRM Unit Data Select Signal to DAT/ST module via middle plane described in Section 6.3.16.

3. Function

OPRM Automatic Bypass Function

The CELL module generates an OPRM Automatic Bypass signal by the logical sum of the following conditions.

A) The CELL module shall compare the APRM Level and the OPRM Region APRM Level setpoint, and if the APRM Level is less than the OPRM Region APRM Level setpoint, generate an OPRM Automatic Bypass signal.
B) The CELL module shall compare the Core Flow Level and the OPRM Region Core Flow Level setpoint, and if the Core Flow Level is more than the OPRM Region Core Flow Level setpoint, generate an OPRM Automatic Bypass signal.

Normalized Oscillation Signal Calculation Function

The CELL module shall generate Normalized Oscillation Signal by following functions.

(1) Filtered Fluxes Calculation Circuit (Conditioning Filter Function)

A) The CELL module shall calculate Filtered Fluxes using the 2-pole butterworth filter and the cut-off frequency setpoint in order to filter out the background noise from each of the 52 LPRM Levels which received from LPRM units and 4 LPRM Levels which are 4 fixed test LPRM Levels. The test LPRM Levels are generated within the CELL module as test data.
B) The calculation A) shall be performed using the [ ]a,c stored in [ ]a,c.
C) Cut-off Frequency Setpoint shall be able to be set from [ ]a,c to [ ]a,c Hz.
D) Conditioning Filter Function shall operate at each LPRM Unit Data input cycle ([ ]a,c ms) from the LPRM unit.

(2) Averaged Filtered Flux Calculation Circuit

A) The CELL module shall assign LPRM Levels to the OPRM Cells in accordance with the OPRM Cell Information Table (See Figure 5-2, Table 5-1) stored in EEPROM.
Note: The OPRM unit for ABWR is configured with 44 Cells for the 52 LPRM Levels.
B) [ ]a,c
C) The CELL module shall calculate an Averaged Flux for each OPRM Cell.
Averaged Flux = Filtered Flux / Number of Active LPRMs
D) LPRM Levels meeting the following conditions shall be excluded from the calculation of Averaged Flux. (LPRM Bypass)
- LPRM Level is less than the lower limit setpoint.
- When inoperative (bypass) occurs in the LPRM unit.
- When a transmission error occurs in the LPRM unit.

E) The Number of Active LPRMs that have not been subject to the LPRM Bypass shall be defined as the Number of Active LPRMs in a Cell.
F) The Cell(s) with Number of LPRMs less than the Minimum Number of Active LPRMs shall be excluded from trip judgment. (OPRM Cell Bypass)

(3) Time Averaged Flux Calculation Circuit

A) The CELL module shall calculate the Time Averaged Flux using the 2-pole butterworth filter and the Time Average Filter Cut-Off Frequency Setpoint for each of the Averaged Flux in [ ]a,c Cells.
B) The CELL module shall carry out the calculation A) using the time averaged filter calculation constant stored in EEPROM.
C) Time Average Filter Cut-off Frequency Setpoint shall be able to be set between [ ]a,c and [ ]a,c Hz

(4) Normalized Oscillation Signal Calculation Circuit

A) A Normalized Oscillation Signal shall be calculated by dividing "Averaged Flux" by "Time Averaged Flux" for each OPRM Cell.
Normalized Oscillation Signal = Averaged Flux / Time Averaged Flux

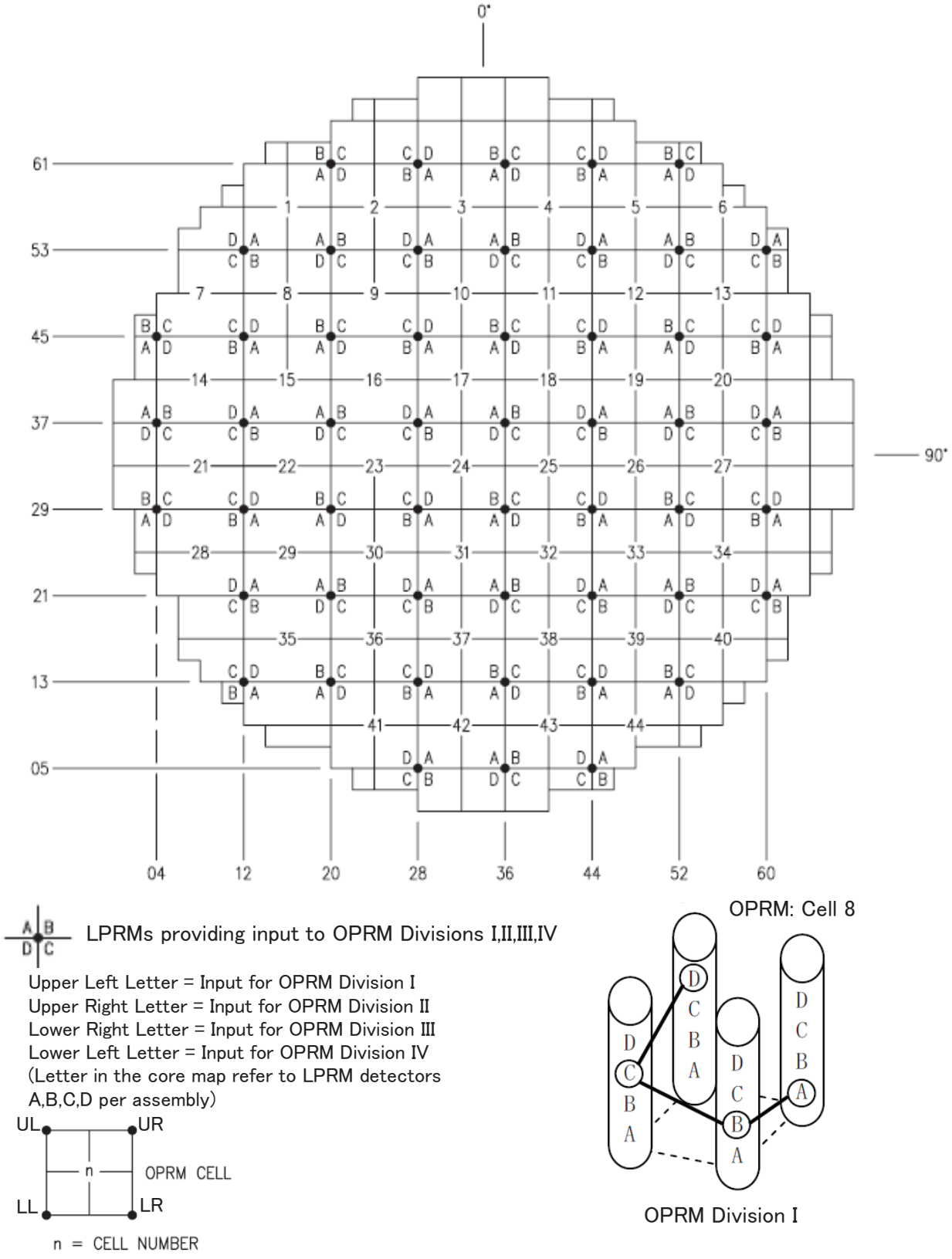


Figure 5-2 Core Map and OPRM Cell

Table 5-1-1 Assignment of LPRM Detectors to APRM Unit and OPRM Unit

		Division	Ⅰ	Ⅱ	Ⅲ	Ⅳ			Division	Ⅰ	Ⅱ	Ⅲ	Ⅳ
		LPRM	A1	B1	C1	D1			LPRM	A2	B2	C2	D2
Detector		LPRM Detector Location	Axial Position				Detector		LPRM Detector Location	Axial Position			
Unit Input Connecter	CH1	20-61	B	C	D	A	Unit Input Connecter	CH14	28-61	C	D	A	B
	CH2	52-61	B	C	D	A		CH15	36-53	A	B	C	D
	CH3	12-53	D	A	B	C		CH16	20-45	B	C	D	A
	CH4	44-53	D	A	B	C		CH17	52-45	B	C	D	A
	CH5	28-45	C	D	A	B		CH18	04-37	A	B	C	D
	CH6	60-45	C	D	A	B		CH19	12-37	D	A	B	C
	CH7	36-37	A	B	C	D		CH20	44-37	D	A	B	C
	CH8	20-29	B	C	D	A		CH21	28-29	C	D	A	B
	CH9	52-29	B	C	D	A		CH22	60-29	C	D	A	B
	CH10	12-21	D	A	B	C		CH23	36-21	A	B	C	D
	CH11	44-21	D	A	B	C		CH24	20-13	B	C	D	A
	CH12	28-13	C	D	A	B		CH25	52-13	B	C	D	A
	CH13	36-05	A	B	C	D		CH26	44-05	D	A	B	C

		Division	Ⅰ	Ⅱ	Ⅲ	Ⅳ			Division	Ⅰ	Ⅱ	Ⅲ	Ⅳ
		LPRM	A3	B3	C3	D3			LPRM	A4	B4	C4	D4
Detector		LPRM Detector Location	Axial Position				Detector		LPRM Detector Location	Axial Position			
Unit Input Connecter	CH27	36-61	B	C	D	A	Unit Input Connecter	CH40	44-61	C	D	A	B
	CH28	28-53	D	A	B	C		CH41	20-53	A	B	C	D
	CH29	60-53	D	A	B	C		CH42	52-53	A	B	C	D
	CH30	12-45	C	D	A	B		CH43	04-45	B	C	D	A
	CH31	44-45	C	D	A	B		CH44	36-45	B	C	D	A
	CH32	20-37	A	B	C	D		CH45	28-37	D	A	B	C
	CH33	52-37	A	B	C	D		CH46	60-37	D	A	B	C
	CH34	04-29	B	C	D	A		CH47	12-29	C	D	A	B
	CH35	36-29	B	C	D	A		CH48	44-29	C	D	A	B
	CH36	28-21	D	A	B	C		CH49	20-21	A	B	C	D
	CH37	60-21	D	A	B	C		CH50	52-21	A	B	C	D
	CH38	12-13	C	D	A	B		CH51	36-13	B	C	D	A
	CH39	44-13	C	D	A	B		CH52	28-05	D	A	B	C

Table 5-1-2 Assignment of LPRM CH to OPRM Cell

Cell No.	UL*	UR*	LL*	LR*	Cell No.	UL*	UR*	LL*	LR*
	LPRM CH in Division**					LPRM CH in Division**			
1	–	1	3	41	23	32	45	8	21
2	1	14	41	28	24	45	7	21	35
3	14	27	28	15	25	7	20	35	48
4	27	40	15	4	26	20	33	48	9
5	40	2	4	42	27	33	46	9	22
6	2	–	42	29	28	34	47	–	10
7	–	3	43	30	29	47	8	10	49
8	3	41	30	16	30	8	21	49	36
9	41	28	16	5	31	21	35	36	23
10	28	15	5	44	32	35	48	23	11
11	15	4	44	31	33	48	9	11	50
12	4	42	31	17	34	9	22	50	37
13	42	29	17	6	35	10	49	38	24
14	43	30	18	19	36	49	36	24	12
15	30	16	19	32	37	36	23	12	51
16	16	5	32	45	38	23	11	51	39
17	5	44	45	7	39	11	50	39	25
18	44	31	7	20	40	50	37	25	–
19	31	17	20	33	41	24	12	–	52
20	17	6	33	46	42	12	51	52	13
21	18	19	34	47	43	51	39	13	26
22	19	32	47	8	44	39	25	26	–

*: Refer to Figure 5-2.
**: Refer to Table 5-1-1.

Filtering Initialization Circuit

A) The CELL module shall set Filtered Flux be equal to Time Averaged Flux and initialize "Normalized Oscillation Signal" to 1.0 at the following conditions.
   - When the Number of Active LPRMs changes
   - OPRM Cell Bypass cancellation occurs
   - OPRM Automatic Bypass cancellation occurs
   - OPRM Inoperative cancelation occurs
   - APRM Bypass cancellation occurs

B) The CELL module shall take the logical sum of conditions shown above and generate a filtering initialization requirement.

Algorithm Initialization Function

A) The CELL module shall generate the algorithm initialization requirement at the following conditions.
   - When the Number of Active LPRMs changes
   - During OPRM Cell Bypass
   - During OPRM Automatic Bypass
   - When OPRM Inoperative cancelation occurs
   - When APRM Bypass cancellation occurs

B) The CELL module shall take the logical sum of signals shown above and generate an algorithm initialization requirement.

OPRM Alarm Judgment Function

(1) OPRM Minor Failure Signal Output

A) The CELL module shall generate OPRM Minor Failure signal at the following conditions.

[ ]a,c

B) The CELL module shall take the logical sum of signals shown above and generate an OPRM Minor Failure signal.

C) The front panel of the CELL module shall show the occurrence of OPRM Minor Failure.

D) The alarm indication of OPRM Minor Failure shall not be cleared even after all the signal generation conditions are cleared.

E) The alarm indication of the CELL module shall be cleared by push button operation on the CELL module front panel.

F) The CELL module shall provide the OPRM Minor Failure signal to the middle plane.

(2) OPRM Inoperative Signal Output

A) The CELL module shall generate OPRM Inoperative signal described at the following conditions.

[ ]a,c

B) The CELL module shall take the logical sum of signals shown above and generate an OPRM Inoperative signal.

C) The front panel of the CELL module shall show the occurrence of OPRM Inoperative.

D) The alarm indication of OPRM Inoperative shall not be cleared even after all the signal generation conditions are cleared.

E) The alarm indication of the CELL module shall be cleared by push button operation on the CELL module front panel.

F) The CELL module shall provide the OPRM Inoperative signal to the middle plane.

Unit Operation Test Function

When the CELL module mode is CAL, this function shall conduct functional test.

Note: This function is to check the algorithm operation of LPRM Bypass, OPRM Cell Bypass, OPRM Automatic Bypass,

and ABA, GRA, PBDA Trips.

[a,c

]

4. Human-Machine Interface (HMI)

Numerical Display

A) CELL module shall indicate the numerical values listed below depending on the selected mode on the front panel numerical display (4 digits 7-segment Light Emitting Diode (LED)).

B) CELL module shall have 7 numerical displays which are the “Amp/%/Count”, “APRM/PARAMETER1”, “fa/FLOW/St TEST No./CAL/PARAMETER2”, “Upper Left (UL)”, “Upper Right (UR)”, “Lower Left (LL)” and “Lower Right (LR).”

C) The indicating items which are shown on the displays shall be selected using push buttons shown on Table 5-9.

Table 5-2 Display Item of CELL Module (1/2)

Mode	7 Segment LED					Status Display LED							
	Amp/%/Count	UL	UR	LL	LR	St	APRM	FLOW	CELL Count	Filtered Flux			
										UL BYP	UR BYP	LL BYP	LR BYP
All Mode	[a,c]												

*: Display Range

Table 5-2 Display Item of CELL Module (2/2)

Mode	7 Segment LED						Status Display LED				
	APRM/PARAMETER1	Upper Position: fa/FLOW/St TEST No./CAL/PARAMETER2 Lower Position: CELL No.	UL	UR	LL	LR	TEST St	TEST Filtered FLUX	TEST APRM/ FLOW	fa	PARAMETER
OP, STANDBY	[redacted]										
CAL											

a,c

Table 5-3 Setpoint Range of Display Item

Display Item	Range	Initial Setpoint
[redacted]		

a,c

Alarm Display and Reset Function

A) The CELL module shall indicate the alarms required in Table 5-4 on the front panel LED.
B) The alarm LEDs shall be latched.
C) The lighted alarm LED shall be reset by push button shown on Table 5-9.

Table 5-4 Alarm LED of CELL Module

Indication Item	Color
[redacted]	

a,c

Status Display and Reset Function

A) The CELL module shall indicate the statuses required in Table 5-5 on the front panel LED.
B) The lighted alarm LED shall be reset by changing the status.

Table 5-5 Status LED of CELL Module

Indication Item	Color
[ ]a,c	

Mode Selection and Reset Function

A) The CELL module shall have the Operation Mode/Sub-Mode required in Table 5-6.
B) The CELL module shall switch the Operation Mode with key switch on the front panel.
C) The CELL module shall change the Sub-Mode by push buttons shown on Table 5-9.

Table 5-6 Mode/Sub-mode of CELL Module

Mode	Sub-Mode : Action
OP	[ ]a,c
STANDBY	
CAL	

D) The CELL module shall indicate mode information required in Table 5-7 on the front panel LED.

Table 5-7 Mode LED of CELL Module

Indication Item	Color
[ ]a,c	

Parameter Setting

A) Following parameters shall be set by [ ]a,c on the printed circuit board.
B) Each setpoint and parameter adjustment function of CELL module shall be designed to avoid any [ ]a,c. The initial setpoint and setpoint range is shown in Table 5-3.

Table 5-8 Parameters Setting of CELL Module on the Printed Circuit Board

Parameter Name
a,c

C) Time Average Filter Cut-off Frequency shall be set by push buttons shown on Table 5-9.
D) To adjust setpoint, mode selection or alarm reset operation, the CELL module shall have the following buttons on the front panel.

Table 5-9 Parameters Setting of CELL Module on the Front Panel

Button Name	Purpose
a,c	

5.2.2. AGRD Module

The AGRD module is inserted into the OPRM unit. The AGRD module is required to have the following function.

1. Input

OPRM Cell Data Input

The AGRD module shall receive OPRM Cell Data from CELL module via middle plane described in Section 6.3.3.

OPRM Inoperative Signal Input

The AGRD module shall receive the OPRM Inoperative signal from CELL module using [ ]a,c in the middle plane described in Section 6.3.12.

OPRM Minor Failure Signal Input

The AGRD module shall receive the OPRM Minor Failure signal from CELL module using [ ]a,c in the middle plane described in Section 6.3.13.

Low Voltage Power Input

The AGRD module shall receive DC power from LVPS module via middle plane.
Input power is described in Section 4.2.2.

2. Output

AGRD Calculation Data Output

The AGRD module shall provide AGRD Calculation Data to DAT/ST module via middle plane described in Section 6.3.5.

OPRM Inoperative Signal Output

The AGRD module shall provide the OPRM Inoperative signal to PBD, DIO and DAT/ST module using [ ]a,c in the middle plane described in Section 6.3.12.

OPRM Minor Failure Signal Output

The AGRD module shall provide the OPRM Minor Failure signal to PBD, DIO and DAT/ST module using [ ]a,c in the middle plane described in Section 6.3.13.

OPRM Trip Signal Output

The AGRD module shall provide the trip signal to PBD, DIO and DAT/ST module using [ ]a,c in the middle plane described in Section 6.3.17, when ABA Trip or GRA Trip occurs in any of the 44 OPRM Cells.

ABA Trip Output

The AGRD module shall provide the ABA Trip signal to DIO module via middle plane described in Section 6.3.18, when ABA Trip occurs in any of the 44 OPRM Cells.

GRA Trip Output

The AGRD module shall provide the GRA Trip signal to DIO module via middle plane described in Section 6.3.19, when GRA Trip occurs in any of the 44 OPRM Cells.

Trip Judgment Status (ABA) Signal Output

The AGRD module shall provide the trip judgment status (ABA) signal to DIO module via middle plane described in Section 6.3.21, when over (or equal to) the ABA and GRA Threshold Setpoint flag in the Amplitude Based Detection Algorithm occurs in any of the 44 OPRM Cells.

Trip Judgment Status (GRA) Signal Output

The AGRD module shall provide the trip judgment status (GRA) signal to DIO module via middle plane described in Section 6.3.22, when over (or equal to) the ABA and GRA Threshold Setpoint flag in the Growth Rate-Based Detection Algorithm occurs in any of the 44 OPRM Cells.

3. Function

Amplitude Based Detection Algorithm

The Amplitude Based Detection Algorithm shall perform the following trip judgment process for 44 Normalized Oscillation Signals in series [ ]a,c, starting with a Normalized Oscillation Signal of the first Cell which was input from the CELL module via middle plane. A flowchart of the judgment process is shown in Figure5-3.

(1)[ ]a,c

The AGRD module shall initialize the ABA logic. The AGRD module shall add the time (dt) to the time (t). The AGRD module shall reset the following processing results of :

[ ]a,c

(2)[ ]a,c

The AGRD module shall judge whether the Normalized Oscillation Signal (St(t)) at the time (t) is greater than or equal to the Threshold Setpoint (S1).

If the judgment is successfully made, the AGRD module shall substitute the time (t) for the base time 1(t0) and [ ]a,c to conduct the process in (3).

If the judgment is not successfully made, the AGRD module shall [ ]a,c to repeat the judgment in (2).

(3)[ ]a,c

As shown in Figure 5-5, the AGRD module shall [ ]a,c

[ ]a,c

[ ]a,c

[ ]a,c to conduct the process in (4).

[ ]a,c the AGRD module shall [ ]a,c to repeat the [ ]a,c as described in (3).

(4)[ ]a,c

As shown in Figure 5-6, the AGRD module shall [ ]a,c

[ ]a,c

[ ]a,c to conduct the process in (5).

[ ]a,c the AGRD module shall [ ]a,c to repeat the [ ]a,c as described in (4).

(5)[ ]a,c

The AGRD module shall [ ]a,c

[ ]a,c

[ ]a,c

[ ]a,c to conduct the process in (6).

[ ]a,c the AGRD module shall go over all the processes again starting at the process in (1).

(6) Judgment for the ABA Within the Oscillation Period

The difference between tp2 and tp1 is assumed to be the “Time Between First Peak and Valley.” The AGRD module

shall judge whether the Time Between First Peak and Valley is greater than the Time Window for Minimum Threshold (T1) and less than the Time Window for Trip Setpoint (Th).
If the judgment is successfully made, the AGRD module shall [ ]a,c conduct the process in (7).
If the judgment is not successfully made, the AGRD module shall go over all the processes again starting at the process in (1).

(7) Preparatory Judgment for Amplitude
The AGRD module shall judge whether the Normalized Oscillation Signal (St(t)) is greater than or equal to the Threshold Setpoint (S1).
If the judgment is successfully made, the AGRD module shall [ ]a,c to conduct the process in (9).
If the judgment is not successfully made, the AGRD module shall conduct the process in (8).

(8) Continuation of Preparatory Judgment for Amplitude
The AGRD module shall judge whether the difference between the time (t) and the base time 1 (t0) is greater than a triplication of the Time Between First Peak and Valley.
If the judgment is successfully made, the AGRD module shall go over all the processes again starting at the process in (1).
If the judgment is not successfully made, the AGRD module shall add the time (dt) to the time (t) to conduct the process in (7).

(9) Judgment for the Maximum Amplitude Trip Setpoint
The AGRD module shall judge whether the Normalized Oscillation Signal (St(t)) at the time (t) is greater than or equal to the Maximum Amplitude Trip Setpoint (Smax).
If the judgment is successfully made, the AGRD module shall [ ]a,c and conduct the process in (12).
If the judgment is not successfully made, the AGRD module shall conduct the process in (10).

(10)[ ]a,c
[ ]a,c
=
[
]a,c to go over the processes again starting at the process in (4).
[ ]a,c the AGRD module shall conduct the process in (11).

(11) Continuation of Judgment for the Maximum Amplitude Trip Setpoint
The AGRD module shall judge whether the difference between the time (t) and the base time 1 (t0) is grater than a triplication of the Time Between First Peak and Valley.
If the judgment is successfully made, the AGRD module shall [ ]a,c to go over the processes again starting at the process in (3).
If the judgment is not successfully made, the AGRD module shall [ ]a,c and go over the processes starting at the process in (9).

(12)[ ]a,c
[ ]a,c
[
]a,c to conduct the process in (13).
[ ]a,c in (12).

(13) ABA Trip Judgment
The difference between tp3 and tp2 is assumed to be the “Time from Last Valley.” The AGRD module shall judge whether the Time from Last Valley is greater than the Time Window for Minimum Threshold (T1), and less than the Time Window for Trip Setpoint (Th).
If the judgment is successfully made, the AGRD module shall output an ABA Trip. The AGRD module shall [ ]a,c go over the processes again starting at the process in (4).
The trip shall be automatically reset after ABA and GRA Trip Hold Time if it is not output again.

If the judgment is not successfully made, the AGRD module shall substitute Tp3 for Tp1 and substitute P3 for P1 to go over the processes again starting at the process in (4).

Growth Rate-Based Detection Algorithm

The Growth Rate-Based Detection Algorithm shall perform the following trip judgment process for 44 Normalized Oscillation Signals in series [ ]a,c starting with a Normalized Oscillation Signal of the first Cell which was input from the CELL module via middle plane. A flowchart of the judgment process is shown in Figure 5-4.

(1)[ ]a,c

The AGRD module shall initialize the GRA logic. The AGRD module shall add the time (dt) to the time (t). The AGRD module shall reset the following processing results:

[ ]a,c

(2)[ ]a,c

The AGRD module shall judge whether the Normalized Oscillation Signal (St(t)) at the time (t) is greater than or equal to the Threshold Setpoint (S1).

If the judgment is successfully made, the AGRD module shall substitute the time (t) for the base time 1(t0) and [ ]a,c to conduct the process in (3).

If the judgment is not successfully made, the AGRD module shall [ ]a,c to repeat the judgment in (2).

(3)[ ]a,c

As shown in Figure 5-5, the AGRD module shall [

]a,c

[

]a,c to conduct the process in (4).

[ ]a,c the AGRD module shall [ ]a,c to repeat the [ ]a,c as [ ]a,c (3).

(4)[ ]a,c

As shown in Figure 5-6, the AGRD module shall [

]a,c

[

]a,c to conduct the process in (5).

[ ]a,c the AGRD module shall [ ]a,c to repeat the [ ]a,c as described in (4).

(5)[ ]a,c

The AGRD module shall [ ]a,c

[

]a,c to conduct the process in (6).

[ ]a,c the AGRD module shall go over all the processes again starting at the process in (1).

(6) Judgment for the GRA Within the Oscillation Period

The difference between (tp2) and (tp1) is assumed to be the "Time Between First Peak and Valley." The AGRD module shall judge whether the Time Between First Peak and Valley is greater than the Time Window for Minimum Threshold (T1) and less than the Time Window for Trip Setpoint (Th).
If the judgment is successfully made, the AGRD module shall [ ]a,c conduct the process in (7).
If the judgment is not successfully made, the AGRD module shall go over all the processes again starting at the process in (1).

(7) Preparatory Judgment for Amplitude
The AGRD module shall judge whether St(t) is greater than or equal to S1.
If the judgment is successfully made, the AGRD module shall [ ]a,c to conduct the process in (9).
If the judgment is not successfully made, the AGRD module shall conduct the process in (8).

(8) Continuation of Preparatory Judgment for Amplitude
The AGRD module shall judge whether the difference between the time (t) and the base time 1 (t0) is greater than a triplication of the Time Between First Peak and Valley.
If the judgment is successfully made, the AGRD module shall go over all the processes again starting at the process in (1).
If the judgment is not successfully made, the AGRD module shall add the time (dt) to the time (t) to conduct the process in (7).

(9) Judgment for Growth Rate
The AGRD module shall judge whether the Normalized Oscillation Signal (St(t)) at the time (t) is greater than or equal to the Growth Rate Amplitude Setpoint (S3).
It shall be noted that S3 shall be assumed to be a value obtained as follows:

S3 = (The First Peak Value (P1) – 1) x Growth Rate Factor (DR3) + 1.0.

If the judgment is successfully made, the AGRD module shall [ ]a,c to conduct the process in (12).
If the judgment is not successfully made, the AGRD module shall conduct the process in (10).

(10)[ ]a,c
[ ]a,c
[
[ ]a,c to go over the processes again starting at the process in (4).
[ ]a,c the AGRD module shall conduct the process in (11).

(11) Continuation of Judgment for the over (or equal to) the Growth Rate Amplitude Setpoint
The AGRD module shall judge whether the difference between the time (t) and the base time 1 (t0) is greater than a triplication of the Time Between First Peak and Valley.
If the judgment is successfully made, the AGRD module shall [ ]a,c to go over the processes again starting at the process in (3).
If the judgment is not successfully made, the AGRD module shall [ ]a,c and conduct the process in (9).

(12)[ ]a,c
[ ]a,c
[
[ ]a,c to conduct the process in (13).
[ ]a,c in (12).

(13) GRA Trip Judgment
The difference between tp3 and tp2 is assumed to be the "Time from Last Valley." The AGRD module shall judge whether the Time from Last Valley is greater than the Time Window for Minimum Threshold (T1) and less than the Time Window for Trip Setpoint (Th).
If the judgment is successfully made, the AGRD module shall output a GRA Trip. The AGRD module shall [ ]a,c

to conduct the process in (4).
The trip shall be automatically reset after ABA and GRA Trip Hold Time if it is not output again.

If the judgment is not successfully made, the AGRD module shall substitute Tp3 for Tp1 and substitute P3 for P1 to go over the processes again starting at the process in (4).

It shall be noted that the AGRD module shall perform both of the ABA and GRA processes concurrently using a separate sequence.
The AGRD module also shall, when algorithm initialization is requested, stop respective algorithms at the state of (1) without outputting and indicating the ABA Trip and GRA Trip.

OPRM Alarm Judgment Function

(1) OPRM Minor Failure Signal Output

A) The AGRD module shall generate OPRM Minor Failure signal at the following conditions.

[ ]a,c

B) AGRD module shall take the logical sum of signals shown above and generate an OPRM Minor Failure signal.
C) The front panel of the AGRD module shall show the occurrence of OPRM Minor Failure.
D) The alarm indication of OPRM Minor Failure shall not be cleared even after all the signal generation conditions are cleared.
E) The alarm indication of the AGRD module shall be cleared by push button operation on the AGRD module front panel.
F) The AGRD module shall provide the OPRM Minor Failure signal to middle plane.

(2) OPRM Inoperative Signal Output

A) The AGRD module shall generate OPRM Inoperative signal described at the following conditions.

[ ]a,c

B) The AGRD module shall take the logical sum of signals shown above and generate an OPRM Inoperative signal.
C) The front panel of the AGRD module shall show the occurrence of OPRM Inoperative.
D) The alarm indication of OPRM Inoperative shall not be cleared even after all the signal generation conditions are cleared.
E) The alarm indication of the AGRD module shall be cleared by push button operation on the AGRD module front panel.
F) The AGRD module shall provide the OPRM Inoperative signal to middle plane.

4. HMI

Numerical Display

A) AGRD module shall indicate the numerical values listed below depending on the selected mode on the front panel numerical display (4 digits 7-segment Light Emitting Diode (LED)).
B) AGRD module shall have 2 numerical displays which are the “PARAMETER1” and “Smax/PARAMETER2.”
C) The indicating items which are shown on the displays shall be selected using push buttons shown on Table 5-16.

Table 5-10 Display Item of AGRD Module

Mode	7 Segment LED		Status Display LED	
	PARAMETER1	Smax/PARAMETER2	Smax	PARAMETER
OP, STANDBY	[redacted]			
CAL				

a,c

Table 5-11 Setpoint Range of Display Item

Display Item	Range	Initial Setpoint
[redacted]		

a,c

Alarm Display and Reset Function

A) The AGRD module shall indicate the alarms required in Table 5-12 on the front panel LED.
B) The alarm LEDs shall be latched.
C) The lighted alarm LED shall be reset by push button shown on Table 5-16.

Table 5-12 Alarm LED of AGRD Module

Indication Item	Color
[redacted]	

a,c

Mode Selection and Reset Function

A) The AGRD module shall have the Operation Mode/Sub-Mode required in Table 5-13
B) The AGRD module shall switch the Operation Mode with key switch on the front panel.
C) [Deleted]

Table 5-13 Mode/Sub-mode of AGRD Module

Mode	Sub-Mode : Action
OP	[ ]a,c
STANDBY	
CAL	

D) The AGRD module shall indicate mode information required in Table 5-14 on the front panel LED.

Table 5-14 Mode LED of AGRD Module

Indication Item	Color
[ ]a,c	

Parameter Setting

A) Following parameters shall be set by [ ]a,c on the printed circuit board.

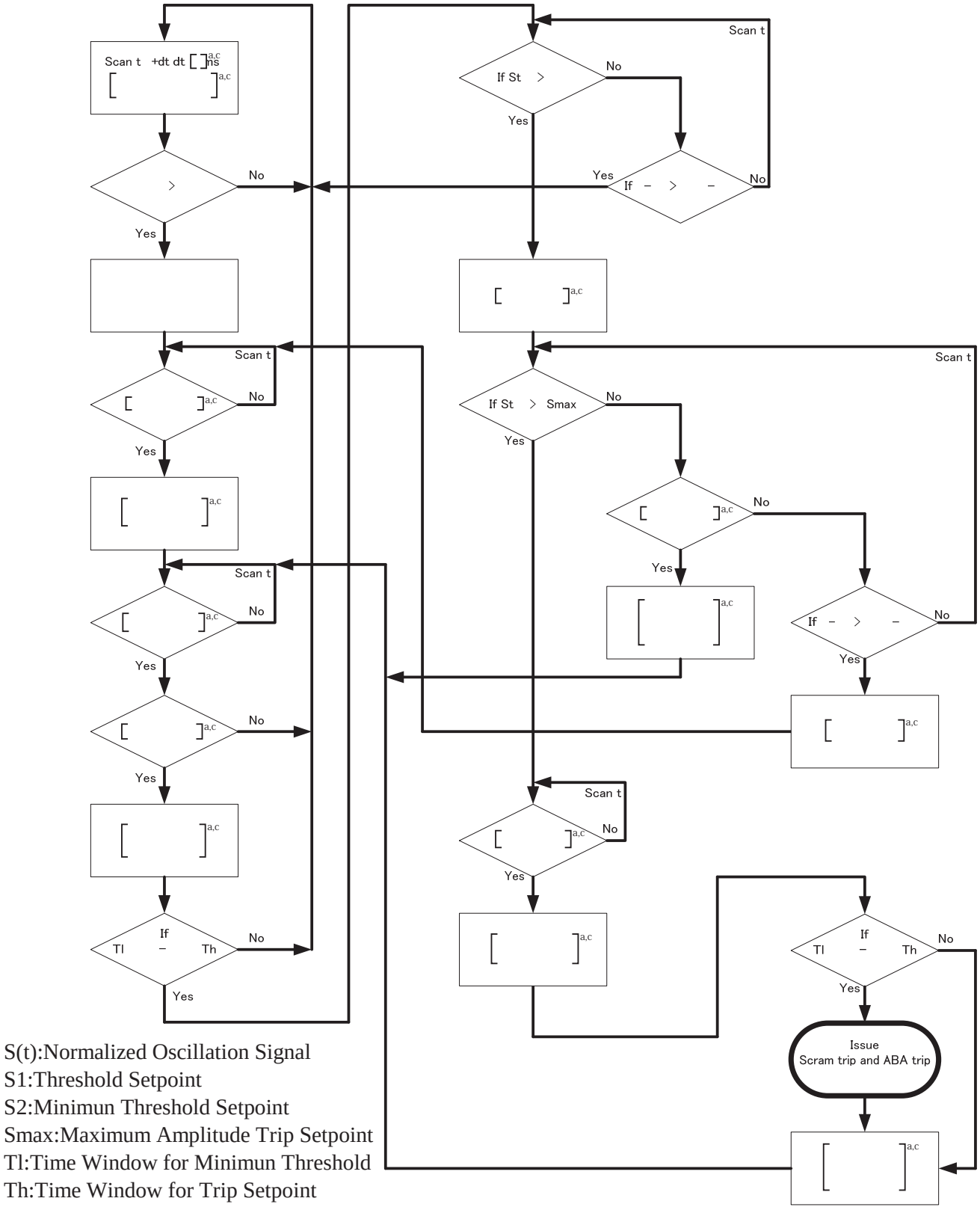
Table 5-15 Parameters Setting of AGRD Module on the Printed Circuit Board

Parameter Name
[ ]a,c

B) Maximum Amplitude Trip Setpoint shall be set by push buttons shown on Table 5-16.
C) Each setpoint and parameter adjustment function of AGRD module shall be designed to avoid any [ ]a,c. The initial setpoint and setpoint range is shown in Table 5-11.
D) To adjust setpoint, mode selection or alarm reset operation, the AGRD module shall have the following buttons on the front panel.

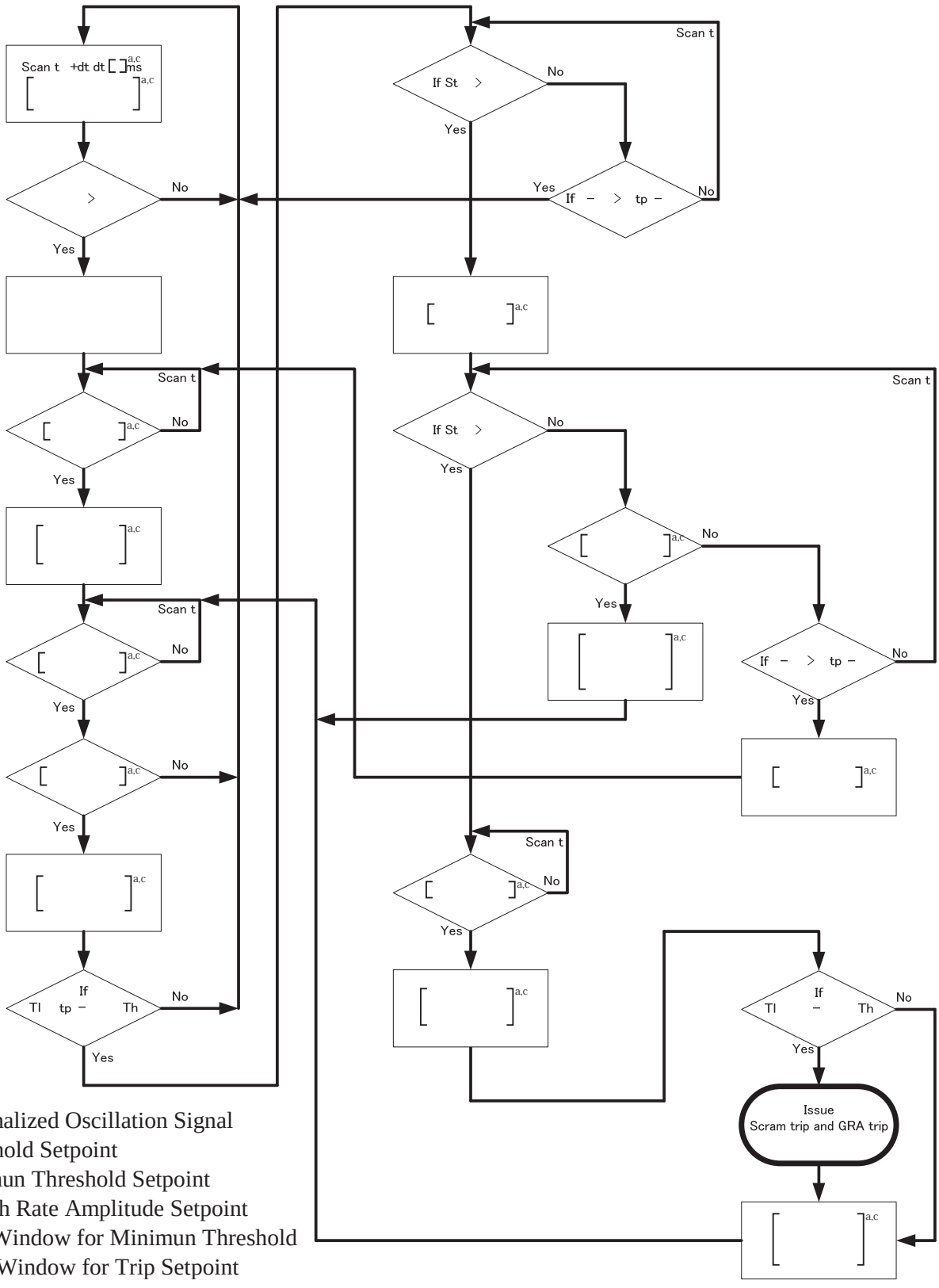
Table 5-16 Parameters Setting of AGRD Module on the Front Panel

Button Name	Purpose
[ ]a,c	



S(t):Normalized Oscillation Signal
S1:Threshold Setpoint
S2:Minimun Threshold Setpoint
Smax:Maximum Amplitude Trip Setpoint
Tl:Time Window for Minimun Threshold
Th:Time Window for Trip Setpoint

Figure 5-3 ABA Trip Judgment Flow Chart



S(t):Normalized Oscillation Signal
S1:Threshold Setpoint
S2:Minimun Threshold Setpoint
S3:Growth Rate Amplitude Setpoint
Tl:Time Window for Minimun Threshold
Th:Time Window for Trip Setpoint

Figure 5-4 GRA Trip Judgment Flow Chart

[a,c]

Figure 5-5 Peak Detection

[a,c]

Figure 5-6 Valley Detection

5.2.3. PBD Module

The PBD module is inserted into the OPRM unit. The PBD module is required to have the following functions.

1. Input

OPRM Cell Data Input

The PBD module shall receive the OPRM Cell Data from CELL module via middle plane described in Section 6.3.3.

OPRM Inoperative Signal Input

The PBD module shall receive the OPRM Inoperative signal from AGRD module using [ ]a,c in the middle plane described in Section 6.3.12.

OPRM Minor Failure Signal Output

The PBD module shall receive the OPRM Minor Failure signal from AGRD module using [ ]a,c in the middle plane described in Section 6.3.13.

OPRM Trip Signal Output

The PBD module shall receive the OPRM Trip signal from AGRD module using [ ]a,c in the middle plane described in Section 6.3.17.

Low Voltage Power Input

The PBD module shall receive DC power from LVPS module via middle plane.
Input power is described in Section 4.2.2.

2. Output

PBD Calculation Data Output

The PBD module shall provide the PBD Calculation Data to DAT/ST module via middle plane described in Section 6.3.6.

OPRM Inoperative Signal Output

The PBD module shall provide the OPRM Inoperative signal to CELL, DIO and DAT/ST module using [ ]a,c in the middle plane described in Section 6.3.12.

OPRM Minor Failure Signal Output

The PBD module shall provide the OPRM Minor Failure signal to DIO and DAT/ST module using [ ]a,c in the middle plane described in Section 6.3.13.

OPRM Trip Signal Output

The PBD module shall provide the OPRM Trip signal to DIO and DAT/ST module using [ ]a,c in the middle plane described in Section 6.3.17, when PBDA Trip occurs in any of the 44 OPRM Cells.

PBDA Trip Signal Output

The PBD module shall provide the PBDA Trip signal to DIO module via middle plane described in Section 6.3.20, when PBDA Trip occurs in any of the 44 OPRM Cells.

Trip Judgment Status (PBDA) Signal Output

The PBD module shall provide the Trip Judgment Status (PBDA) Signal to DIO module via middle plane described in Section 6.3.23, when "Start the Confirmation Count" occurs in any of the 44 OPRM Cells.

3. Function

Period Based Detection Algorithm

The Period Based Detection Algorithm shall perform the following trip judgment process for 44 Normalized Oscillation Signals in series [ ]a,c, starting with a Normalized Oscillation Signal of the first Cell which was input from the CELL module via middle plane. A flowchart of the judgment process is shown in Figure 5-7.

(1)[ ]a,c

The PBD module shall initialize the PBD logic. The PBD module shall add the time (dt) to the time (t). The PBD module shall clear the following results of operations:

[ ]a,c

(2)[ ]a,c

[

]a,c

[

]a,c to conduct the process in (3).

[ ]a,c to repeat the peak detection as described in (2).

(3)[ ]a,c

As shown in Figure 5-6, the PBD module shall [

]a,c

[

]a,c to conduct the process in (4).

[ ]a,c the PBD module shall [ ]a,c to repeat the Valley detection as described in (3).

(4)[ ]a,c

As shown in Figure 5-5, the PBD module shall [

]a,c

[

]a,c and substitute the difference between tp3 and tp1 for the period (T0) to conduct the process in (5).

[ ]a,c the PBD module shall [ ]a,c to repeat the peak detection as described in (4).

(5) Initial Confirmation Count Judgment

If the Confirmation Count (N) is greater than or equal to 1 (i.e., N ≥ 1), the PBD module shall conduct the process in (7).
If the Confirmation Count (N) is 0 (i.e., N < 1), the PBD module shall conduct the process in (6).

(6) Initial Peak Period Judgment

If there is T0 value between the Period Minimum Setpoint (Tmin) and the Period Maximum Setpoint (Tmax) that are set in the PBD module, the PBD module shall assume the previous period (Tref) to be “T0” and N to be “N+1” to conduct the process in (8).
If there is not T0 value between them, the PBD module shall [ ]a,c to go over all the processes again starting at the process in (3).

(7) Peak Period Judgment

If there is the current period (T0) between a value of the previous period (Tref) minus the Period Tolerance Setpoint (Te)

and a value of the previous period (Tref) plus the Period Tolerance Setpoint (Te), the PBD module shall assume the previous period (Tref) to be “T0” and N to be “N+1” to conduct the process in (8).
If there is not T0 value between those values, the PBD module shall assume N to be “0” and tp1 to be “tp3” to go over all the processes again starting at the process in (3).

(8)[ ]a,c
As shown in Figure 5-6,[

]a,c to conduct the process in (9).
[ ]a,c to repeat the [ ]a,c as described in (8).

(9)[ ]a,c
[

]a,c to conduct the process in (10).
[ ]a,c the PBD module shall go over all the processes again starting at the process in (1).

(10)[ ]a,c
[

]a,c to conduct the process in (11).
[ ]a,c the PBD module shall[ ]a,c to repeat the process above starting at (4).

(11) PBDA Trip Judgment
The PBD module shall compare the Normalized Oscillation Signal (St(t)) and the PBDA Amplitude Setpoint (Sp), and if (St(t)) is equal or greater than (Sp), assume that a trip condition is met and output the PBDA Trip, and then[ ]a,c
[ ]a,c to go over all the processes again starting at the process in (4).
If (St(t)) is less than (Sp), the PBD module shall[ ]a,c to conduct the process in (12).
The trip shall be automatically reset after PBDA Trip Hold Time if it is not output again.

(12)[ ]a,c
[

]a,c to conduct the process in (5).
[ ]a,c to conduct the process in (11).

It shall be noted that the PBD module shall, when algorithm initialization is requested, stop respective algorithms at the state of (1) without outputting and indicating the PBDA Trip.

OPRM Alarm Judgment Function
(1) OPRM Minor Failure Signal Output

A) The PBD module shall generate OPRM Minor Failure signal at the following conditions.
[ ]a,c
B) The PBD module shall take the logical sum of signals shown above and generate an OPRM Minor Failure signal.
C) The front panel of the PBD module shall show the occurrence of OPRM Minor Failure.
D) The alarm indication of OPRM Minor Failure shall not be cleared even after all the signal generation conditions are cleared.
E) The alarm indication of the PBD module shall be cleared by push button operation on the PBD module front panel.

F) The PBD module shall provide the OPRM Minor Failure signal to middle plane.

(2) OPRM Inoperative Signal Output

A) The PBD module shall generate the OPRM Inoperative signal described in Section 6.3.12 at the following conditions.

[ ]a,c

B) The PBD module shall take the logical sum of signals shown above and generate an OPRM Inoperative signal.
C) The front panel of the PBD module shall show the occurrence of OPRM Inoperative.
D) The alarm indication of OPRM Inoperative shall not be cleared even after all the signal generation conditions are cleared.
E) The alarm indication of the PBD module shall be cleared by push button operation on the PBD module front panel.
F) The PBD module shall provide the OPRM Inoperative signal to middle plane.

4. HMI

Numerical Display

A) PBD module shall indicate the numerical values listed below depending on the selected mode on the front panel numerical display (4 digits 7-segment Light Emitting Diode (LED)).
B) PBD module shall have 3 numerical displays which are the “Confirmation Count (N)”, “PARAMETER1” and “Terror/Np/PARAMETER2.”
C) The “Confirmation Count (N)” shall indicate a Confirmation Count of the Cell number in accordance with "Display Selected Cell Number" signal received from CELL module. Indication shall be available for values from 0 through 127.
D) The indicating items of “PARAMETER1” and “Terror/Np/PARAMETER2”, which are shown on the displays shall be selected using push buttons shown on Table 5-23.

Table 5-17 Display Item of PBD Module

Mode	7 Segment LED			Status Display LED		
	Confirmation Count (N)	PARAMETER1	Terror/Np/ PARAMETER2	Terror	Np	PARAMETER
OP, STANDBY	[ ]a,c					
CAL						

Table 5-18 Setpoint Range of Display Item

Display Item	Range	Initial Setpoint
[ ] a,c		

Alarm Display and Reset Function

A) The PBD module shall indicate the alarms required in Table 5-19 on the front panel LED.
B) The alarm LEDs shall be latched.
C) The lighted alarm LED shall be reset by push button shown on Table 5-23.

Table 5-19 Alarm LED of PBD Module

Indication Item	Color
[ ] a,c	

Mode Selection and Reset Function

A) The PBD module shall have the Operation Mode/Sub-Mode required in Table 5-20.
B) The PBD module shall switch the Operation Mode by key switch on the front panel.
C) [Deleted]

Table 5-20 Mode/Sub-mode of PBD Module

Mode	Sub-Mode : Action
OP	[ ] a,c
STANDB	
CAL	

D) The PBD module shall indicate the mode information required in Table 5-21 on the front panel LED.

Table 5-21 Mode LED of PBD Module

Indication Item	Color
[ ] a,c	

Parameter Setting

A) Following parameters shall be set by [ ]a,c on the printed circuit board.

Table 5-22 Parameters Setting of PBD Module on the Printed Circuit Board

Parameter Name
[ ]a,c

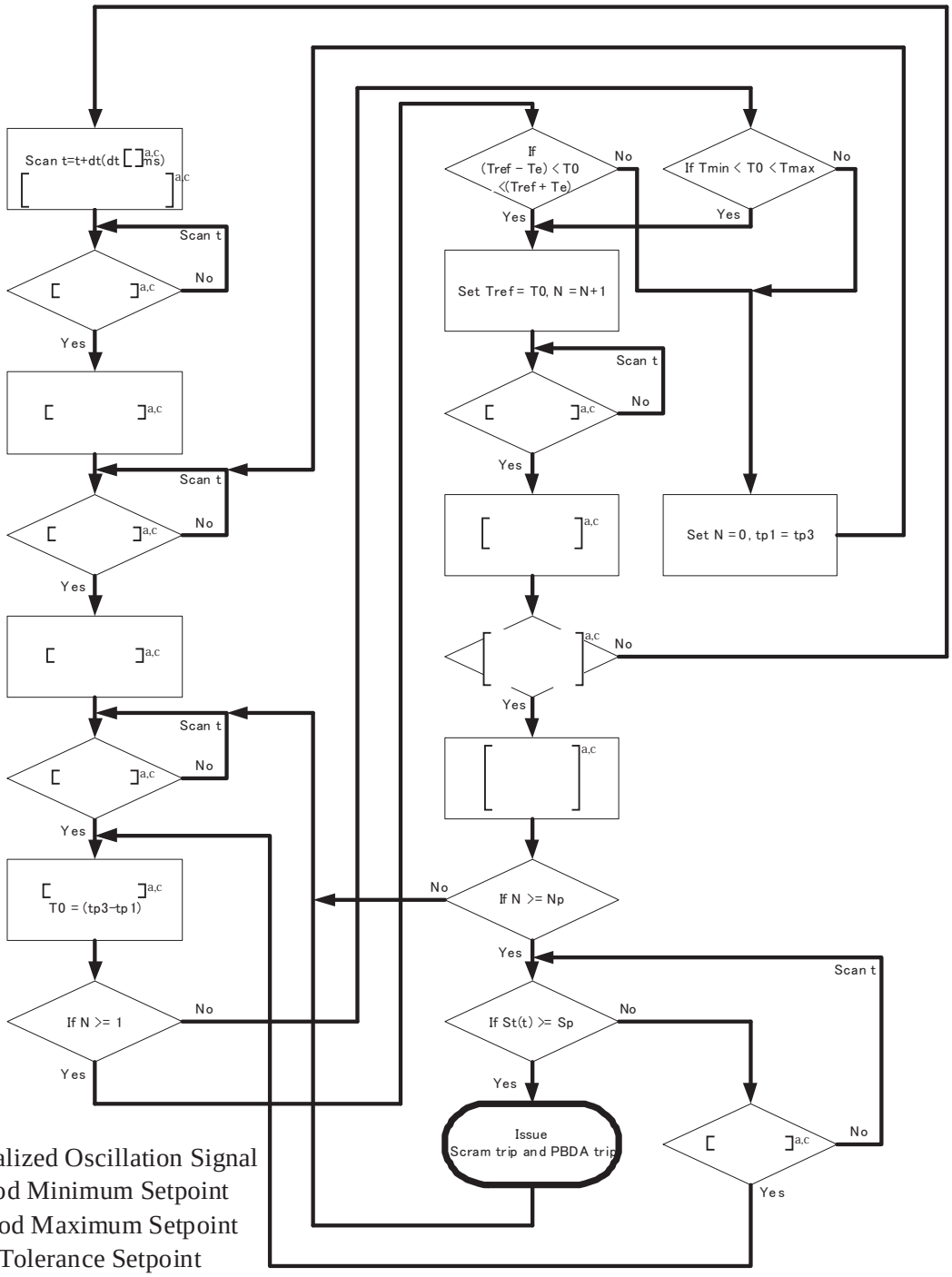
B) Period Tolerance Setpoint (Te) and Confirmation Count Trip Setpoint (Np) shall be set by push buttons shown on Table 5-23.

C) Each setpoint and parameter adjustment function of PBD module shall be designed to avoid [ ]a,c The initial setpoint and setpoint range is shown in Table 5-18.

D) To adjust setpoint, mode selection or alarm reset operation, the PBD module shall have the following buttons on the front panel.

Table 5-23 Parameters Setting of PBD Module on the Front Panel

Button Name	Purpose
[ ]a,c	



S(t):Normalized Oscillation Signal
Tmin:Period Minimum Setpoint
Tmax:Period Maximum Setpoint
Te:Period Tolerance Setpoint
Sp:Maximum Amplitude Trip Setpoint
Np:Confirmation Count Trip Setpoint

Figure 5-7 PBDA trip Judgment Flow Chart

5.2.4. DAT/ST Module

The DAT/ST module is inserted into the OPRM unit. The DAT/ST module is required to have the following function.

1. Input

OPRM Cell Data Input
The DAT/ST module shall receive OPRM Cell Data from CELL module via middle plane described in Section 6.3.3.

OPRM Calculation Data Input
The DAT/ST module shall receive OPRM Calculation Data from CELL module via middle plane described in Section 6.3.4.

AGRD Calculation Data Input
The DAT/ST module shall receive AGRD Calculation Data from AGRD module via middle plane described in Section 6.3.5.

PBD Calculation Data Input
The DAT/ST module shall receive PBD Calculation Data from PBD module via middle plane described in Section 6.3.6.

OPRM Inoperative Signal Input
The DAT/ST module shall receive OPRM Inoperative signal from PBD module using [ ]^{a,c} in the middle plane described in Section 6.3.12.

OPRM Minor Failure Signal Input
The DAT/ST module shall receive OPRM Minor Failure signal from PBD module using [ ]^{a,c} in the middle plane described in Section 6.3.13.

CELL Module Input Data Error Signal Input
The DAT/ST module shall receive CELL Module Input Data Error signal from CELL module via middle plane described in Section 6.3.14.

APRM Unit Data Select Signal Input
The DAT/ST module shall receive APRM Unit Data Select Signal from CELL module via middle plane described in Section 6.3.16.

OPRM Trip Signal Input
The DAT/ST module shall receive OPRM Trip signal from PBD module using [ ]^{a,c} in the middle plane described in Section 6.3.17.

Power Supply Error Monitoring Signal Input
The DAT/ST module shall receive Power Supply Error Monitoring signal from LVPS module via middle plane described in Section 6.3.24.

Low Voltage Power Input
The DAT/ST module shall receive DC power from LVPS module via middle plane.
Input power is described in Section 4.2.2.

2. Output

OPRM Multiplexed Data Output
The DAT/ST module shall provide OPRM Multiplexed Data to TRN module via middle plane described in Section 6.3.7.

OPRM Record Data Output
The DAT/ST module shall provide OPRM Record Data to TRN module via middle plane described in Section 6.3.8.

OPRM Minor Failure Signal Output
The DAT/ST module shall provide OPRM Minor Failure signal to DIO module using [ ]^{a,c} in the middle plane described in Section 6.3.13.

3. Function

OPRM Multiplexing

The operation data, the trip and OPRM Inoperative, and Minor Failure alarm information received from the CELL, AGRD and PBD modules shall be multiplexed to generate the OPRM multiplexed data and OPRM record data.

OPRM Alarm Judgment Function

(1) OPRM Minor Failure Signal Output

A) The DAT/ST module shall generate OPRM Minor Failure signal at the conditions.

[ ]a,c

B) The DAT/ST module shall take the logical sum of signals shown above and generate an OPRM Minor Failure signal.
C) The front panel of the DAT/ST module shall show the occurrence of OPRM Minor Failure.
D) The alarm indication of OPRM Minor Failure shall not be cleared even after all the signal generation conditions are cleared.
E) The alarm indication of the DAT/ST module shall be cleared by push button operation on the DAT/ST module front panel.
F) The DAT/ST module shall provide the OPRM Minor Failure signal to the middle plane.

4. HMI

Alarm Display and Reset Function

A) The DAT/ST module shall indicate the alarms required in Table 5-24 on the front panel LED.
B) The alarm LEDs shall be latched.
C) The lighted alarm LED shall be reset by push button “RESET.”

Table 5-24 Alarm LED of DAT/ST Module

Indication Item	Color
[ ]a,c	

Status Display and Reset Function

A) The DAT/ST module shall indicate the statuses required in Table 5-25 on the front panel LED.

Table 5-25 Status LED of DAT/ST Module

Indication Status	Color
[ ]a,c	

5.2.5. TRN Module

TRN module shall have 4 optical outputs.
TRN module receives signals of three-wire electrical communication link from middle plane, multiplexes, and provides them to the externals as an optical signal.

1. Input

OPRM Multiplexed Data Input

TRN module shall receive the OPRM Multiplexed Data from DAT/ST module via middle plane described in Section 6.3.7.

OPRM Record Data Input

TRN module shall receive the OPRM Record Data from DAT/ST module via middle plane described in Section 6.3.8.

Low Voltage Power Input

TRN module shall receive following DC power from LVPS module via the middle plane.
Input power is described in Section 4.2.2.

2. Output

External Output

TRN module shall provide external output data described in Sections 6.2.1 and 6.2.2 by optical transmission.

3. Function

Optical Conversion Function

A) TRN module shall add frame signal to the received signals of three-wire electrical communication link and convert them into to make an optical signal.

Unit Type and ID Addition Function

A) TRN module shall attach a set of Unit Type and ID information to the received signals of three-wire electrical communication link to distinguish them.
B) TRN module shall be able to set the Unit ID by digital switch on the printed circuit board.

Table 5-26-1 Unit ID of TRN Module

Module	OPRM unit Division	Module Port No. 1	2	3	4
		Unit ID			
TRN module (ELCS and PICS Output)	OPRM(I)	[			] a,c
	OPRM(II)				
	OPRM(III)				
	OPRM(IV)				
TRN module (TDR Output)	OPRM(I)				
	OPRM(II)				
	OPRM(III)				
	OPRM(IV)				]

*: Unit ID will be set at the time mounting to unit chassis.

CRC function

A) TRN module shall attach 32-bit CRC to the transmission data received from DAT/ST Module.

4. HMI

Status Display

TRN module shall display following status on the front panel by LED.

Table 5-26-2 Status Display of TRN Module

Status Display Item on the rear panel	LED Color
[	] a,c

5.2.6. RCV Module

RCV module shall have 4 optical inputs.
RCV module receives optical signals from externals and converts them into electric data, and provides them to middle plane.

1. Input

External Input

RCV module shall receive external input data described in Sections 6.1.1 and 6.1.2 by optical transmission.

Low Voltage Power Input

RCV module shall receive following DC power from LVPS module via the middle plane.
Input power is described in Section 4.2.2.

2. Output

LPRM Unit Data Output

RCV module shall provide LPRM Unit Data to CELL module via middle plane described in Section 6.3.1.

APRM Unit Data Output

RCV module shall provide APRM Unit Data to CELL module via middle plane described in Section 6.3.2.

LPRM Unit Data Input Error Signal Output

RCV module shall provide LPRM Unit Data input error signal to CELL module via middle plane described in Section 6.3.9.

APRM Unit Data Input Error Signal Output

RCV module shall provide APRM Unit Data input error signal to CELL module via middle plane described in Section 6.3.10

3. Function

Electrical Conversion Function

RCV module shall convert an optical signal into a serial signal by decoding the Manchester Code.

Transmission Error Check Function

A) RCV module shall detect the time-out, [ ]a,c of received optical signal.
B) RCV module shall preserve and provide the previous data in case of transmission error.
C) RCV module shall be able to set the Unit ID by digital switch on the printed circuit board.
D) RCV module shall detect multi-bit errors in received optical signal using 32-bit CRC.

Table 5-27-1 Unit ID of RCV Module

Module	OPRM unit Division	Module Port No. 1	2	3	4
		Unit ID			
RCV module (LPRM Input)	OPRM(I	[			]a,c
	OPRM(I				
	OPRM(III)				
	OPRM(I				
RCV Module (APRM Input)	OPRM(				
	OPRM(I				
	OPRM(III)				
	OPRM(I				

*: Unit ID will be set at the time mounting to unit chassis.

4. HMI

Status Display

RCV module shall display following status on the front panel by LED.

Table 5-27-2 Status Display of RCV Module

Status Display Item on the rear panel	LED Color
[	]a,c

5.2.7. DIO Module

DIO module shall have 4 discrete voltage inputs and 16 discrete voltage outputs.
DIO module shall receive CMOS level signals from middle plane, and send them to external, as non-contact output signals.
DIO module shall receive input signals from external system and convert them into CMOS level output signals.

1. Input

External Input

DIO module shall receive external input signals described in Section 6.1.3.

OPRM Inoperative Signal Input

DIO module shall receive the OPRM Inoperative signal from PBD module via middle plane described in Section 6.3.12.

OPRM Minor Failure Signal Input

DIO module shall receive the OPRM Minor Failure signal from DAT/ST module via middle plane described in Section 6.3.13.

OPRM Automatic Bypass Signal Input

DIO module shall receive the OPRM Automatic Bypass signal from CELL module via middle plane described in Section 6.3.15.

OPRM Trip Signal Input

DIO module shall receive the OPRM Trip signal from PBD module via middle plane described in Section 6.3.17.

ABA Trip Signal Input

DIO module shall receive the ABA Trip signal from AGRD module via middle plane described in Section 6.3.18.

GRA Trip Signal Input

DIO module shall receive the GRA Trip signal from AGRD module via middle plane described in Section 6.3.19.

PBDA Trip Signal Input

DIO module shall receive the PBDA Trip signal from PBD module via middle plane described in Section 6.3.20.

Trip Judgment Status (ABA) Signal Input

DIO module shall receive the Trip Judgment Status (ABA) signal from AGRD module via middle plane described in Section 6.3.21.

Trip Judgment Status (GRA) Signal Input

DIO module shall receive the Trip Judgment Status (GRA) signal from AGRD module via middle plane described in Section 6.3.22.

Trip Judgment Status (PBDA) Signal Input

DIO module shall receive the Trip Judgment Status (PBDA) signal from PBD module via middle plane described in Section 6.3.23.

Low Voltage Power Input

DIO module shall receive following DC power from LVPS module via the middle plane.
Input power is described in Section 4.2.2.

2. Output

External Output

DIO module shall provide external output signals described in Section 6.2.3.

APRM Bypass Signal Output

DIO module shall provide the APRM Bypass signal to CELL module via middle plane described in Section 6.3.11.

3. Function

Input and Output Isolation

A) DIO module shall insulate Complementary Metal Oxide Semiconductor (CMOS) level signals from output signals by

using Photo-MOS relays.
B) DIO module shall insulate the external input signals from CMOS level signals by using photo-couplers.

[ ]a,c Requirement
A) DIO module shall mount [ ]a,c at external input interface to protect input circuit when high voltage is being applied.
B) DIO module shall mount [ ]a,c at external output interface to protect output circuit when high voltage is being applied.

5.2.8. LVPS Module

LVPS module shall be a plug-in type unit power supply that receives AC power or DC power and supplies DC power to middle plane. LVPS module shall have three power outputs (DC 5V, +15V, -15V). LVPS module shall monitor the output voltage inside the power supply, and generate an alarm in case of failure.

1. Input

Rated Power Input

LVPS module shall receive following DC power from external.

A) Input Voltage [ ]a,c
B) Input Current [ ]a,c

LVPS module shall receive following AC power from external

C) Input Voltage [ ]a,c
D) AC Input Frequency [ ]a,c
E) Input Current [ ]a,c

2. Output

Rated DC Output

LVPS module shall provide following DC power to other modules in the OPRM unit.

[ ]a,c
[ ]a,c
[ ]a,c

Power Supply Error Monitoring Signal Output

LVPS module shall provide Power Supply Voltage Monitoring Signal Output to DAT/ST module via middle plane described in Section 6.3.24.

3. Function

Power Supply Voltage Monitoring Function

A) LVPS module shall monitor the both end of +5VDC output redundant diode to make sure anode voltage is lower than cathode voltage [ ]a,c of output voltage of +5VDC.
B) LVPS module shall monitor the both end of +15VDC output redundant diode to make sure anode voltage is lower than cathode voltage [ ]a,c of output voltage of +15VDC.
C) LVPS module shall monitor the both end of -15VDC output redundant diode to make sure cathode voltage is lower than anode voltage [ ]a,c of output voltage of -15VDC.
D) The LVPS module shall take the logical sum of signals shown above and generate a Power Supply Error Monitoring Signal.

Overvoltage Protection Function

A) LVPS module shall have overvoltage protection function.
B) LVPS module shall shut down the circuit when it detects overvoltage and its circuit recovers when the power is supplied to LVPS module.

Over Current Protection Function

A) LVPS module shall have over current protection function.
B) LVPS module shall use maximum current limiting method for over current protection and circuit recovers automatic.

Parallel Operation

A) LVPS module shall have diode at power supply output to prevent reverse current.

Voltage Adjustment Function

A) Output voltage of LVPS module shall be [ ]a,c

Voltage Monitor Function

A) LVPS module has [ ]a,c to monitor DC output voltage.

Fuse

A) LVPS module shall have a fuse to protect from inrush current.

Output Fluctuation

A) Output fluctuation of LVPS module shall be [ ]a,c of rated DC output voltage (Total fluctuation of input, load, and temperature fluctuations)

Drift

A) Drift of LVPS module shall be [ ]a,c of rated DC output voltage in 30 minutes to 8 hours.

Ripple

Ripple voltage of DC output voltage in LVPS module shall have following performances.

A) +5VDC [ ]a,c peak to peak MAX
B) +15VDC [ ]a,c peak to peak MAX
C) -15VDC [ ]a,c peak to peak MAX

Ripple Noise

Ripple noise of DC output voltage in LVPS module shall have following performances.

A) +5VDC [ ]a,c peak to peak MAX
B) +15VDC [ ]a,c peak to peak MAX
C) -15VDC [ ]a,c peak to peak MAX

Withstand Voltage

A) LVPS module shall withstand [ ]a,c for 1 minute between input terminal and output terminal.
B) LVPS module shall withstand [ ]a,c for 1 minute between input terminal and Frame Ground (FG).

Insulation Resistance

A) LVPS module shall have insulation resistance more than [ ]a,c between input terminal and FG at [ ]a,c.
B) LVPS module shall have insulation resistance more than [ ]a,c between input terminal and output terminal at [ ]a,c.
C) LVPS module shall have insulation resistance more than [ ]a,c between output terminal and FG at [ ]a,c.

4. HMI

Status Display

LVPS module shall display following status on the front panel by LED. The LED is automatic restoration.

Table 5-28 Display Item of LVPS Module

[ ]a,c

5. Connector

Power Input Connector

Power Input Connector shall have following specifications.

A) MS connector: [ ]a,c
B) Input Pin Assignment is described in Table 6-8-1.

5.2.9. PFC

The OPRM unit including PFC shall operate for AC input variations of [ ]a,c percent (voltage) and [ ]a,c (frequency) of nominal in accordance with EDS Section 5.2.2.3.11 (Reference 2.2(1)).

AC power input (PFC input)

A) Number of Input	1 (1 LVPS per 1 PFC)
B)Input power voltage range	AC90 to 150V
C)Power frequency range	[ ]a,c
D) Efficiency	[ ]a,c (at rated output)
E)Power Factor	[ ]a,c (at rated output)
F)Consumption current	[ ]a,c (at rated AC voltage: 100V)
G) Inrush Current	[ ]a,c

DC power output (to LVPS module)

A) Number of Output	1 (1 LVPS per 1 PFC)
B) Rated Output Voltage	220VDC
C) Rated Output Current	[ ]a,c
D) Output Voltage Setting Accuracy	[ ]a,c
E) Input Variation (AC90 to 150V)	[ ]a,c
F) Load Fluctuation ([ ]a,c)	[ ]a,c
G) Ripple	[ ]a,c

Withstand Voltage

A) PFC shall withstand [ ]a,c for 1 minute between AC input line and chassis.

Insulation Resistance

A) PFC module shall have insulation resistance more than [ ]a,c between AC input line and chassis at [ ]a,c.

Mass

A) [ ]a,c

Pin Assignment

See Figure 5-8.

[ ]a,c

Figure 5-8 Pin Assignment of PFC

6. Interface Specifications

6.1. Input Signal to Unit

6.1.1. LPRM Unit Data from LPRM Unit

(1) The OPRM unit shall have optical input transmission interfaces from LPRM units and the detail specifications are as follows:

A)	Signal Form	Optical serial signal
B)	Connector	[ ]a,c
C)	Connecting to	RCV module
D)	Number of Ports	[ ]a,c
E)	Transmission Code	Manchester Code
F)	Transmission Speed	[ ]a,c
G)	Transmission Cycle	[ ]a,c
H)	Transmission Distance	[ ]a,c
I)	Transmission Format	Figure 6-1
J)	Bit Configuration	Figure 6-2

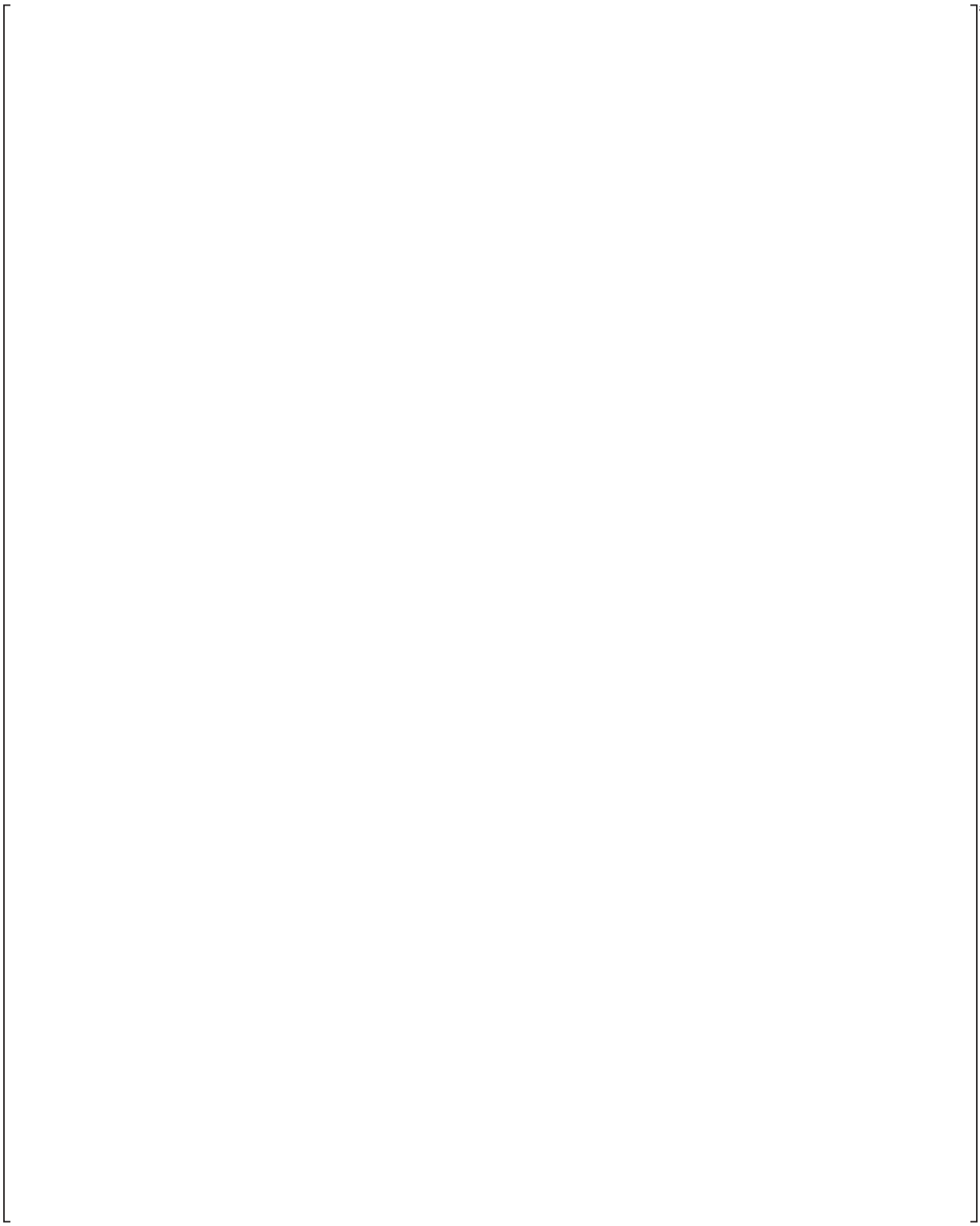


Figure 6-1 Transmission Format of Transmission Data from LPRM Unit

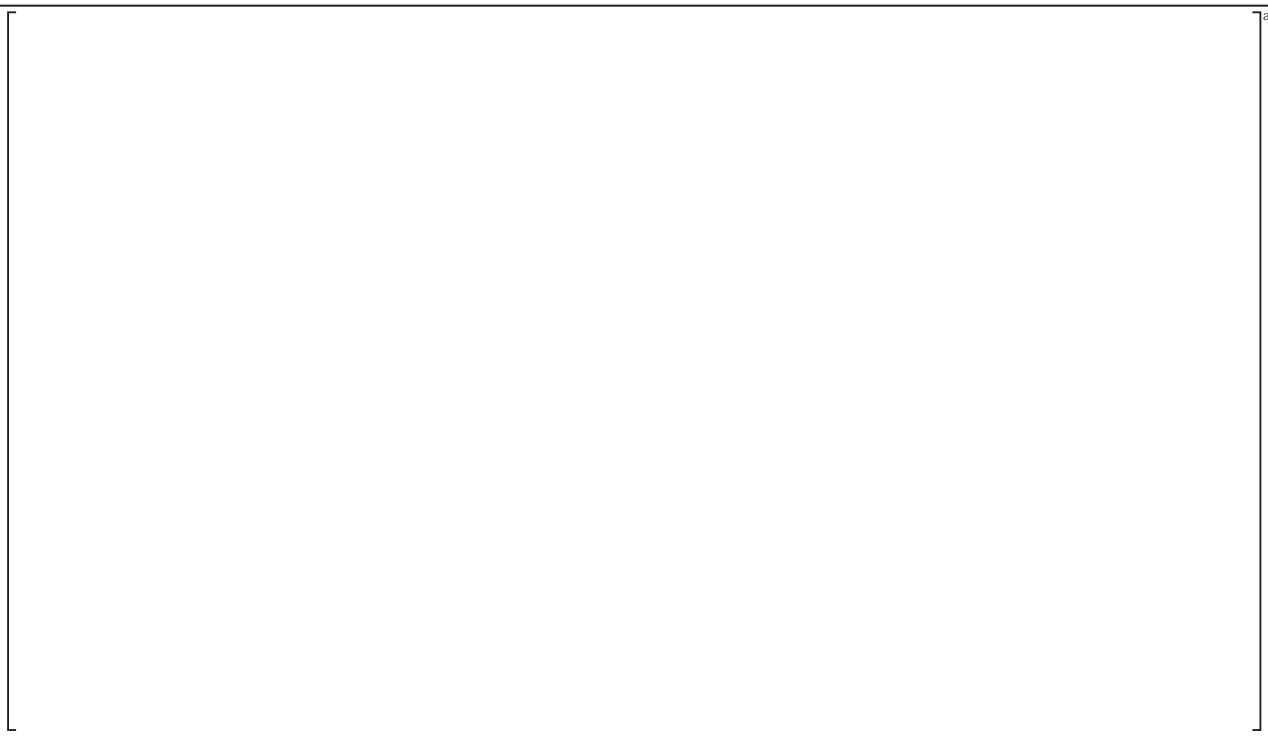


Figure 6-2 Bit Configuration of Transmission Data from LPRM Unit

6.1.2. APRM Unit Data from APRM Unit

(1) The OPRM unit shall have optical input transmission interfaces from APRM unit and the detail specifications are as follows:

A)	Signal Form	Optical serial signal
B)	Connector	[ ]a,c
C)	Connecting to	RCV module
D)	Number of Ports	[ ]a,c
E)	Transmission Code	Manchester Code
F)	Transmission Speed	[ ]a,c
G)	Transmission Cycle	[ ]a,c
H)	Transmission Distance	[ ]a,c
I)	Transmission Format	Figure 6-3
J)	Bit Configuration	Figure 6-4

a,c

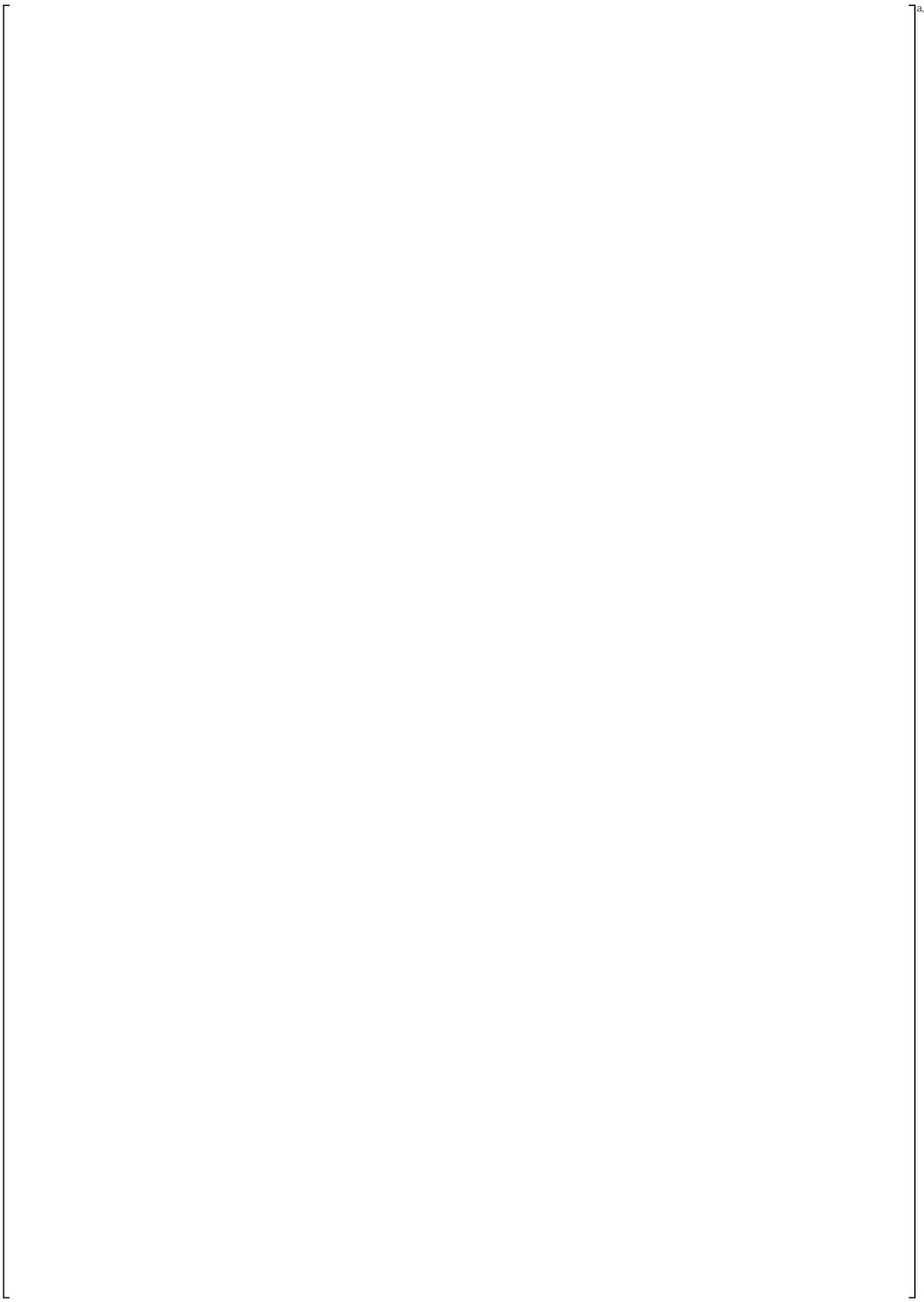


Figure 6-3 Transmission Format of Transmission Data of APRM Unit

a,c

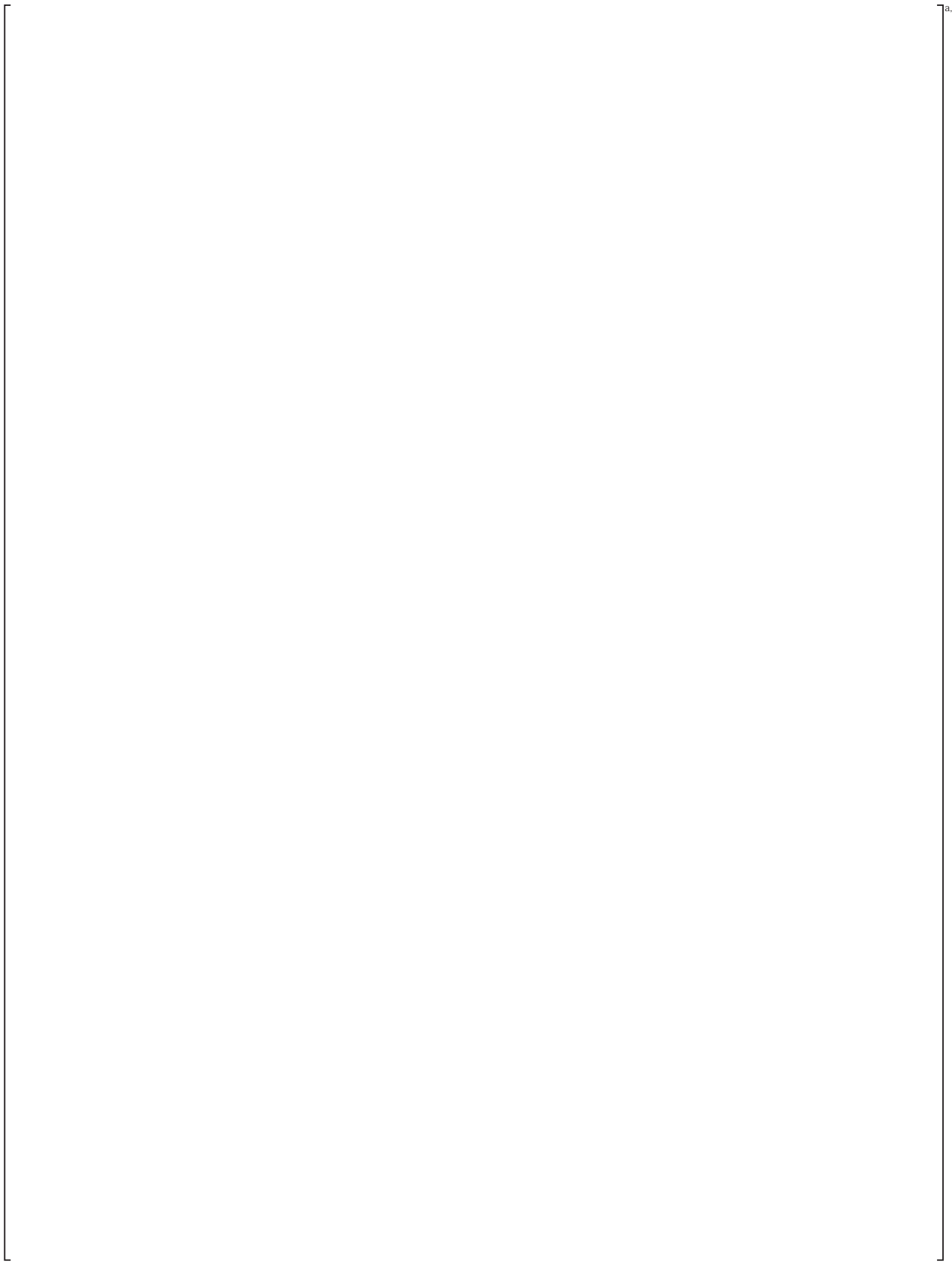


Figure 6-4 Bit Configuration of Transmission Data from APRM Unit

6.1.3. APRM Bypass Signal from Relay Unit

(1) The OPRM unit shall have discrete input transmission interface from the Relay unit and the detail specifications are as follows:

A)	Signal Form	Insulated-type, voltage contact input (Photo coupler)
B)	Logic Level	[a,c]
C)	Connecting to	DIO module
D)	Number of Cable	1
E)	Withstand Voltage	[a,c]
F)	Insulated Resistance	[a,c]
G)	Connector	[a,c]
H)	Guide Key	Thick guide key: 2, Thin guide key: 1
I)	Pin Assignment	Figure 6-5

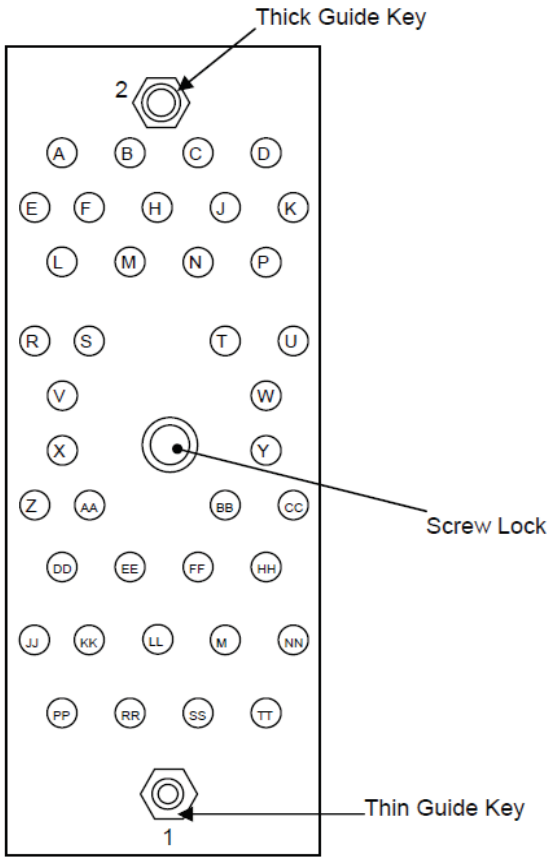


Figure 6-5-1 Discrete Input/Output Connector of DIO Module

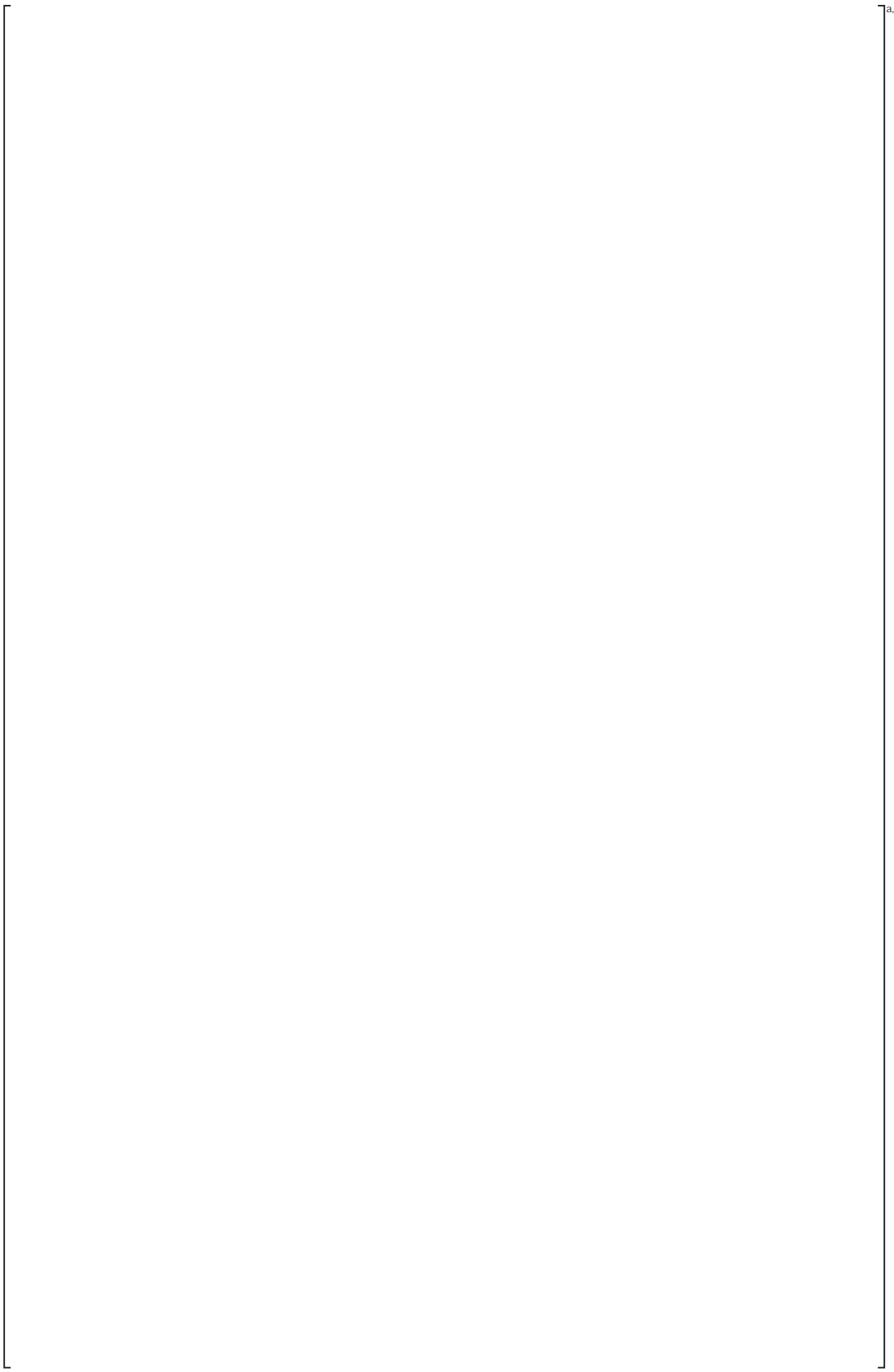


Figure 6-5-2 Pin Assignment of the Relay Unit Input and Output

6.1.4. Power Supply Input

See Section 5.2.8.

6.2. Output Signal from Unit

6.2.1. OPRM Multiplexed Data to ELCS and PICS

(1) The OPRM unit shall have optical output transmission interfaces to ELCS and PICS and the detail specifications are as follows:

A) Signal Form: Optical serial signal
B) Connector: [ ]a,c
C) Connecting to: TRN module
D) Number of Ports: [ ]a,c
E) Transmission Code: Manchester code
F) Transmission Speed: [ ]a,c
G) Transmission Cycle: [ ]a,c
[ ]a,c
H) Transmission Distance: [ ]a,c
I) Transmission Format: Figure 6-6
J) Bit Configuration: Figure 6-7

a,c

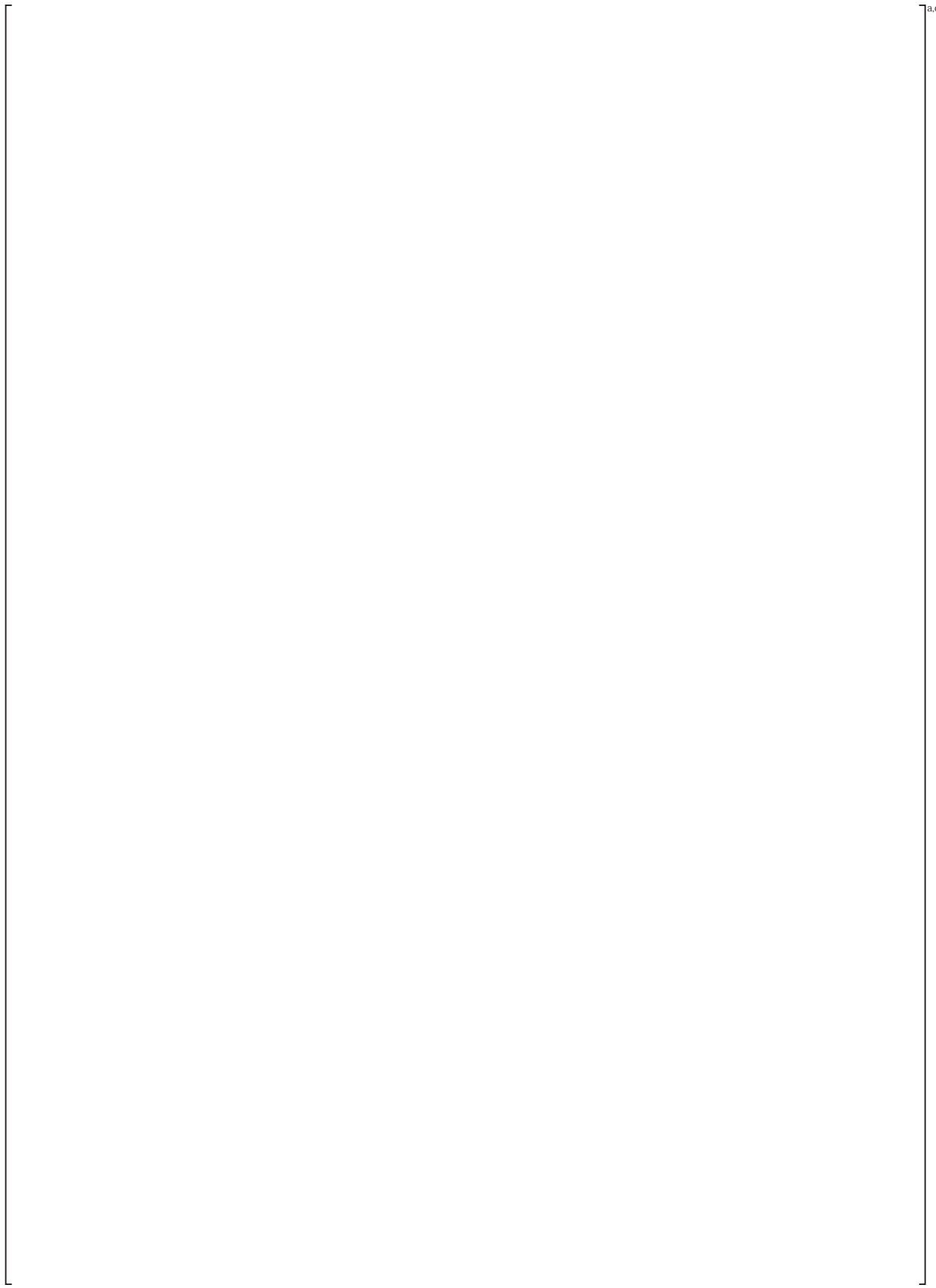


Figure 6-6 (1/2) Transmission Format of Transmission Data Output to ELCS and PICS

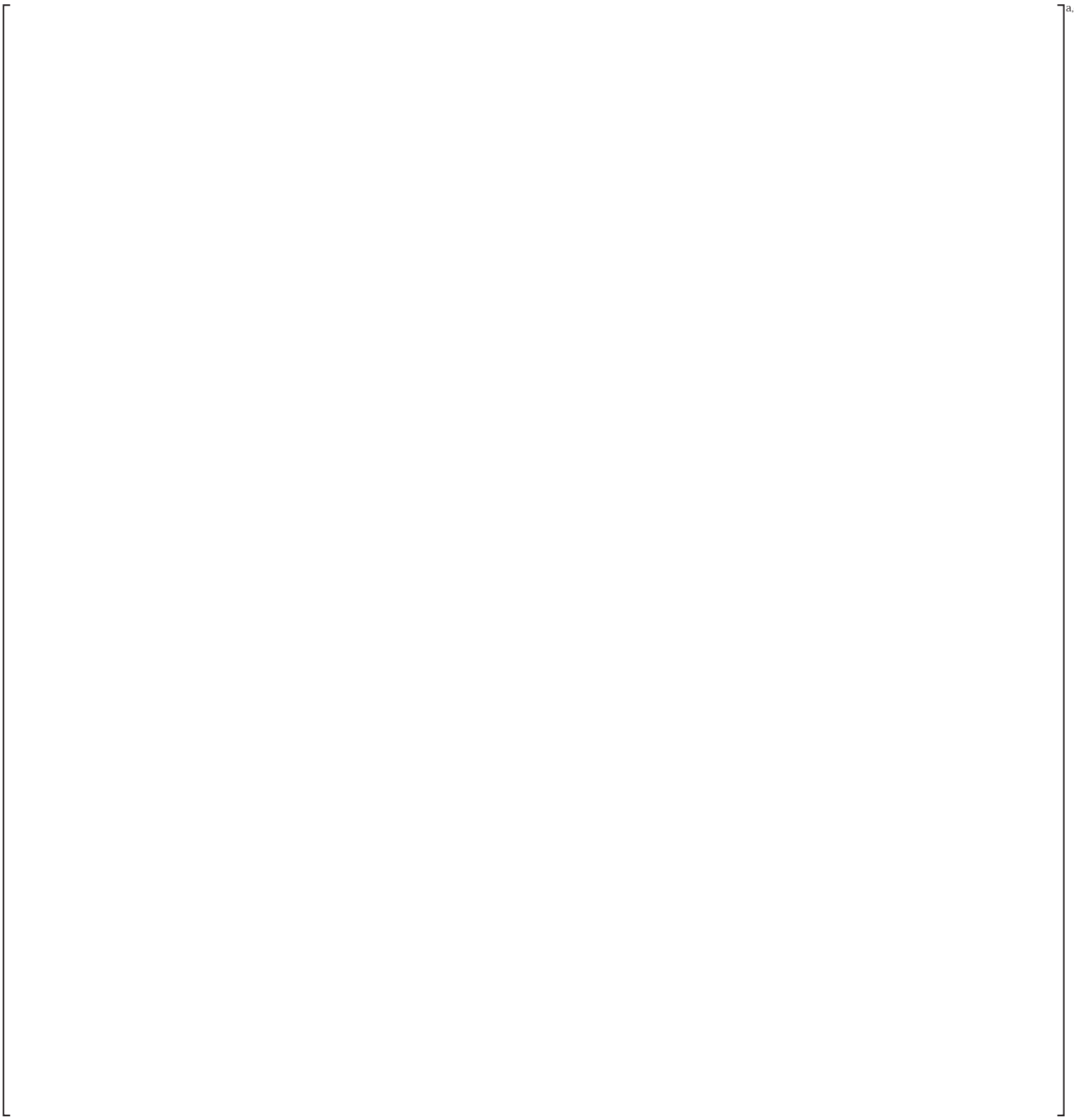


Figure 6-6 (2/2) Transmission Format of Transmission Data Output to ELCS and PICS

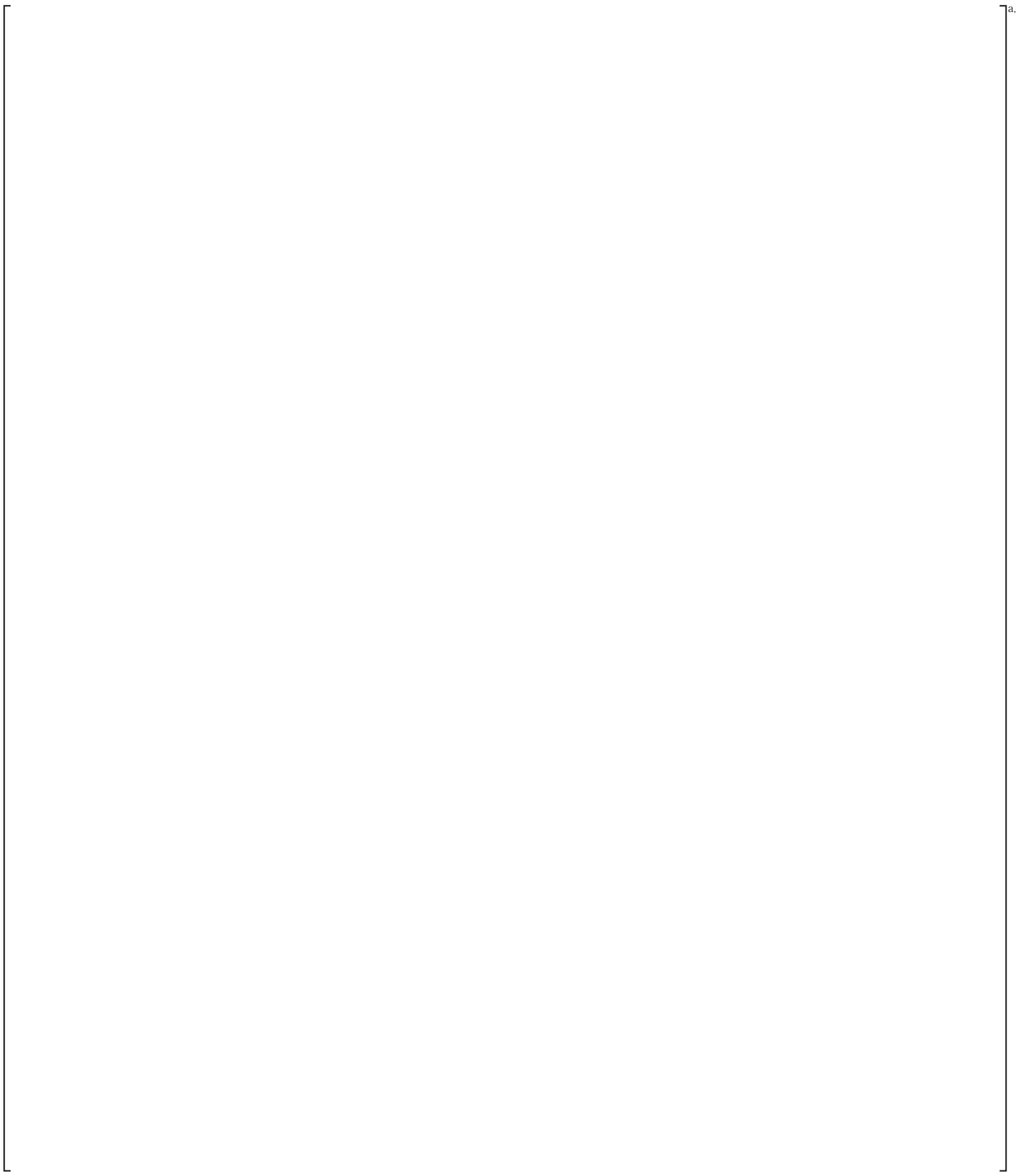


Figure 6-7(1/5) Bit Configuration of Transmission Data Output to ELCS and PICS

a,c

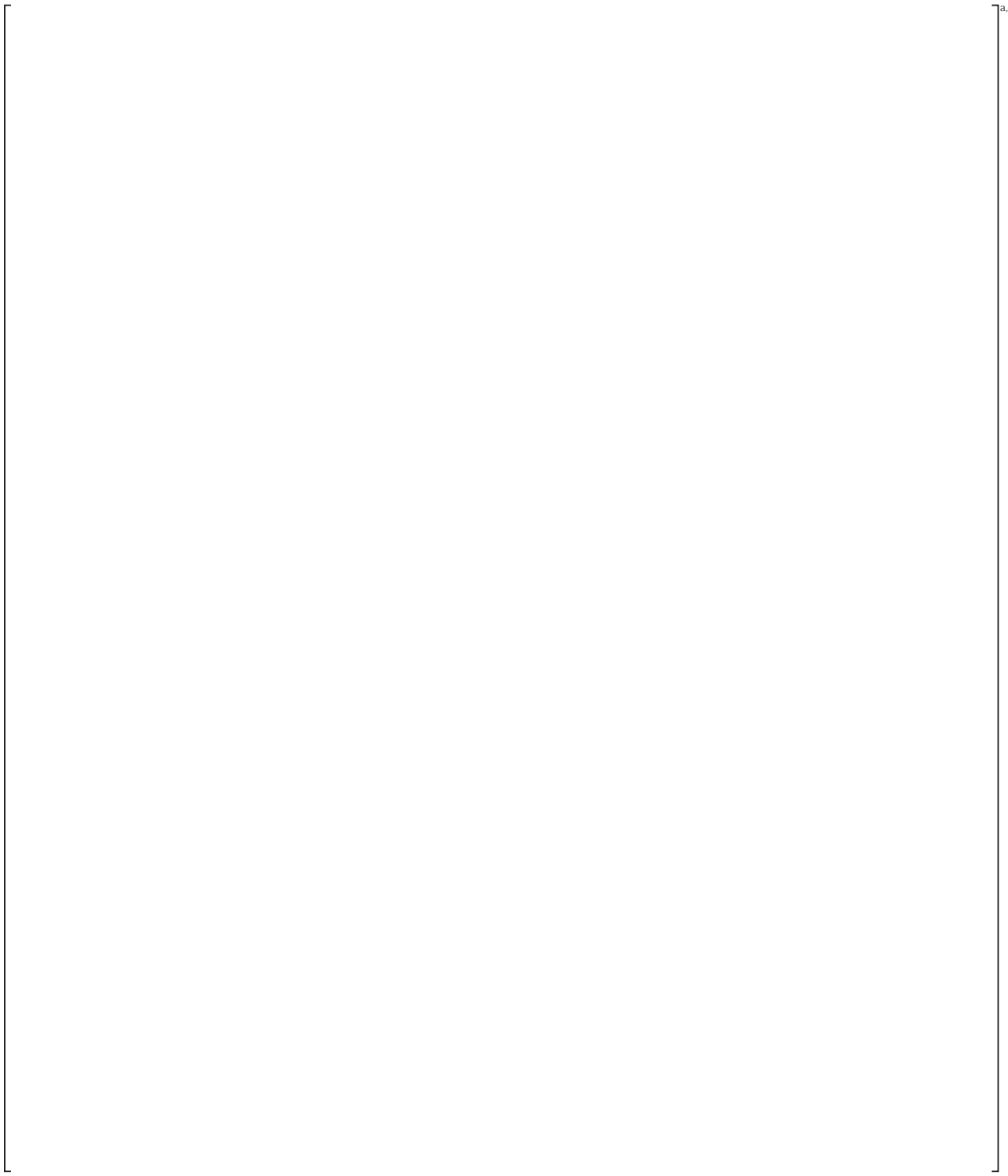


Figure 6-7(2/5) Bit Configuration of Transmission Data Output to ELCS and PICS

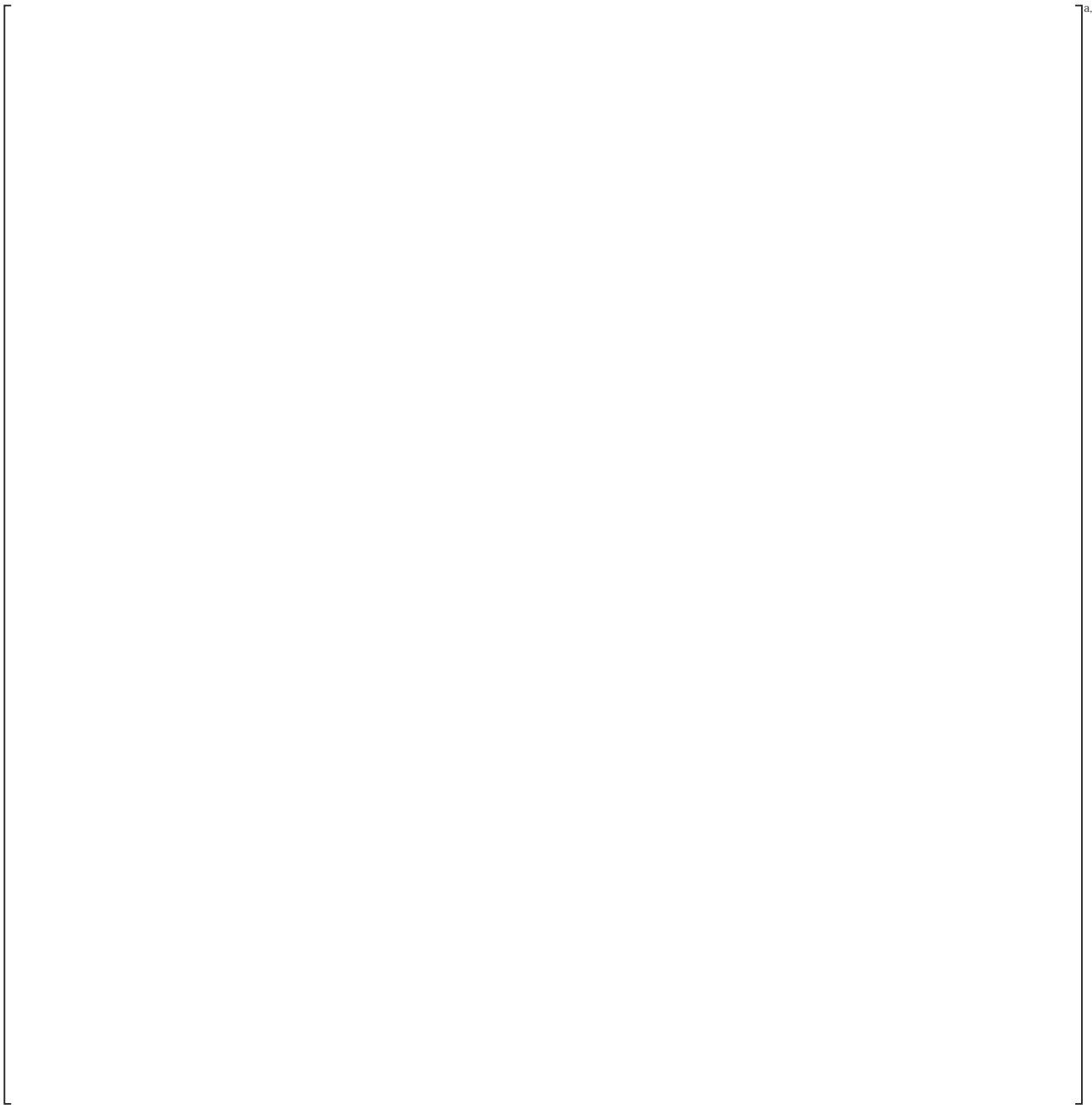


Figure 6-7(3/5) Bit Configuration of Transmission Data Output to ELCS and PICS

a,c

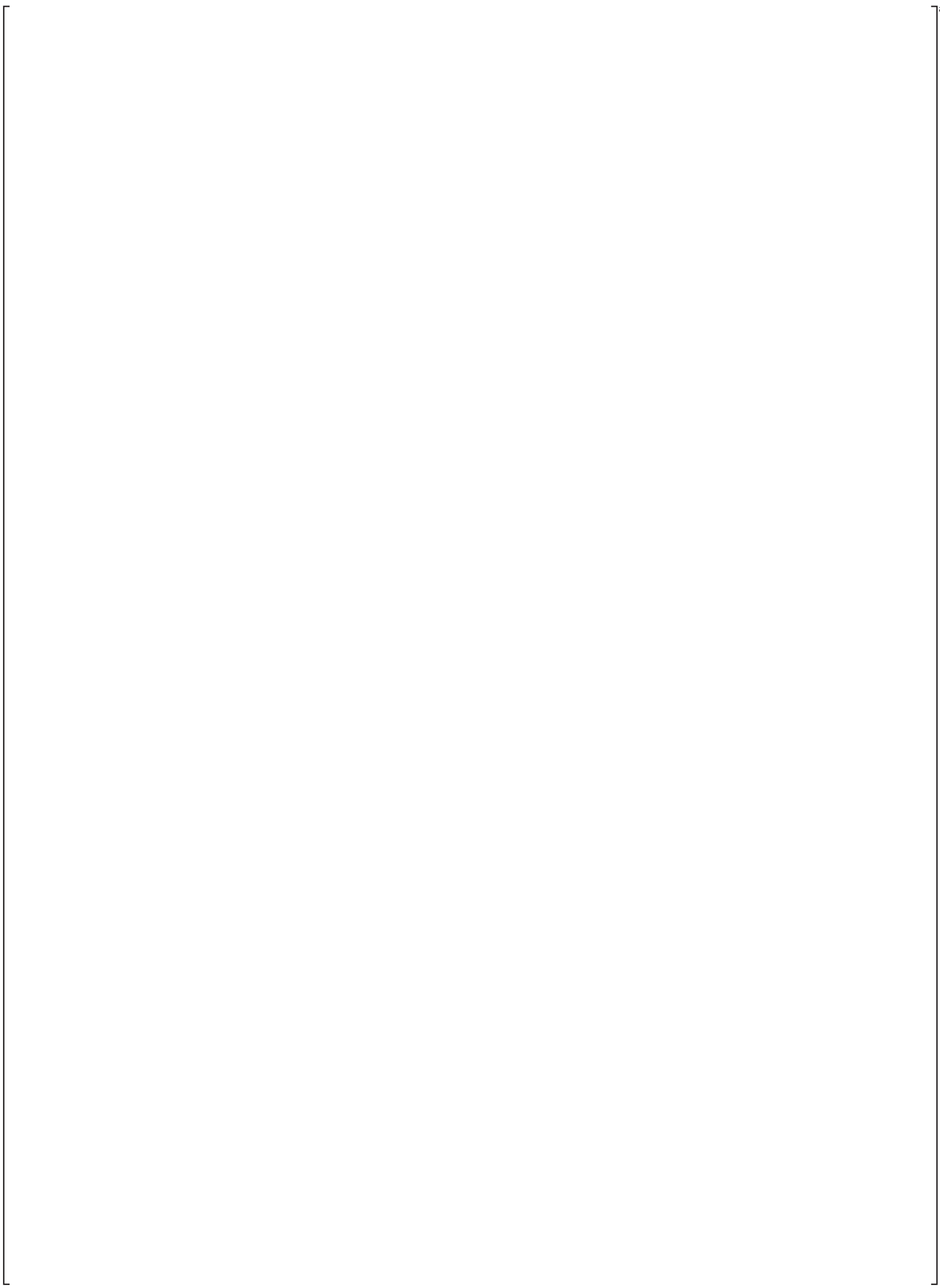


Figure 6-7(4/5) Bit Configuration of Transmission Data Output to ELCS and PICS

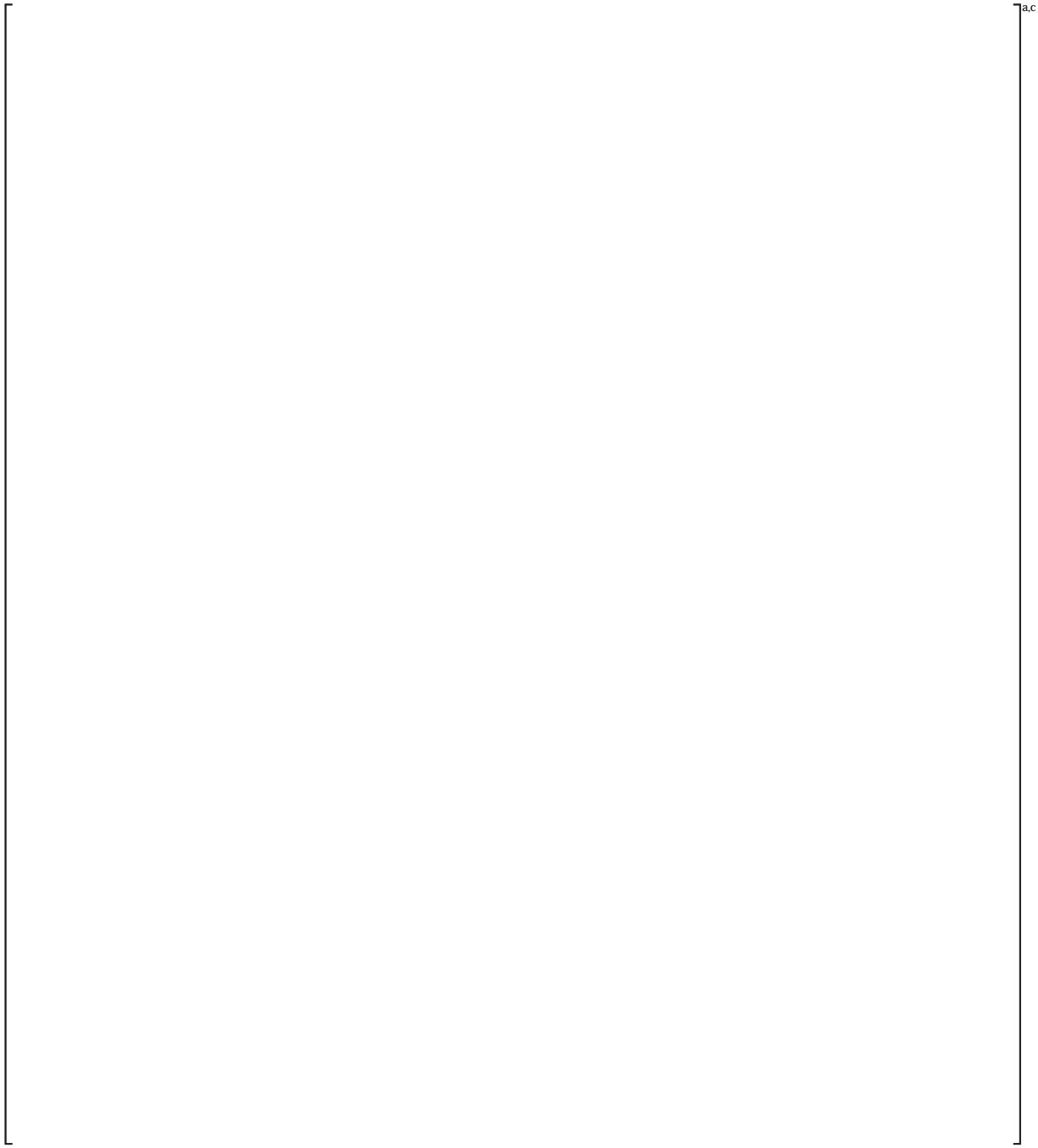


Figure 6-7(5/5) Bit Configuration of Transmission Data Output to ELCS and PICS

6.2.2. OPRM Record Data to TDR

(1) The OPRM unit shall have optical output transmission interfaces to TDR and the detail specifications are as follows:

A)	Signal Form	Optical serial signal
B)	Connector	[ ]a,c
C)	Connecting to	TRN module
D)	Number of Ports	[ ]a,c
E)	Transmission Code	Manchester code
F)	Transmission Speed	[ ]a,c
G)	Transmission Cycle	[ ]a,c [ ]a,c
H)	Transmission Distance	[ ]a,c
I)	Transmission Format	Figure 6-8
J)	Bit Configuration	Figure 6-9

a,c

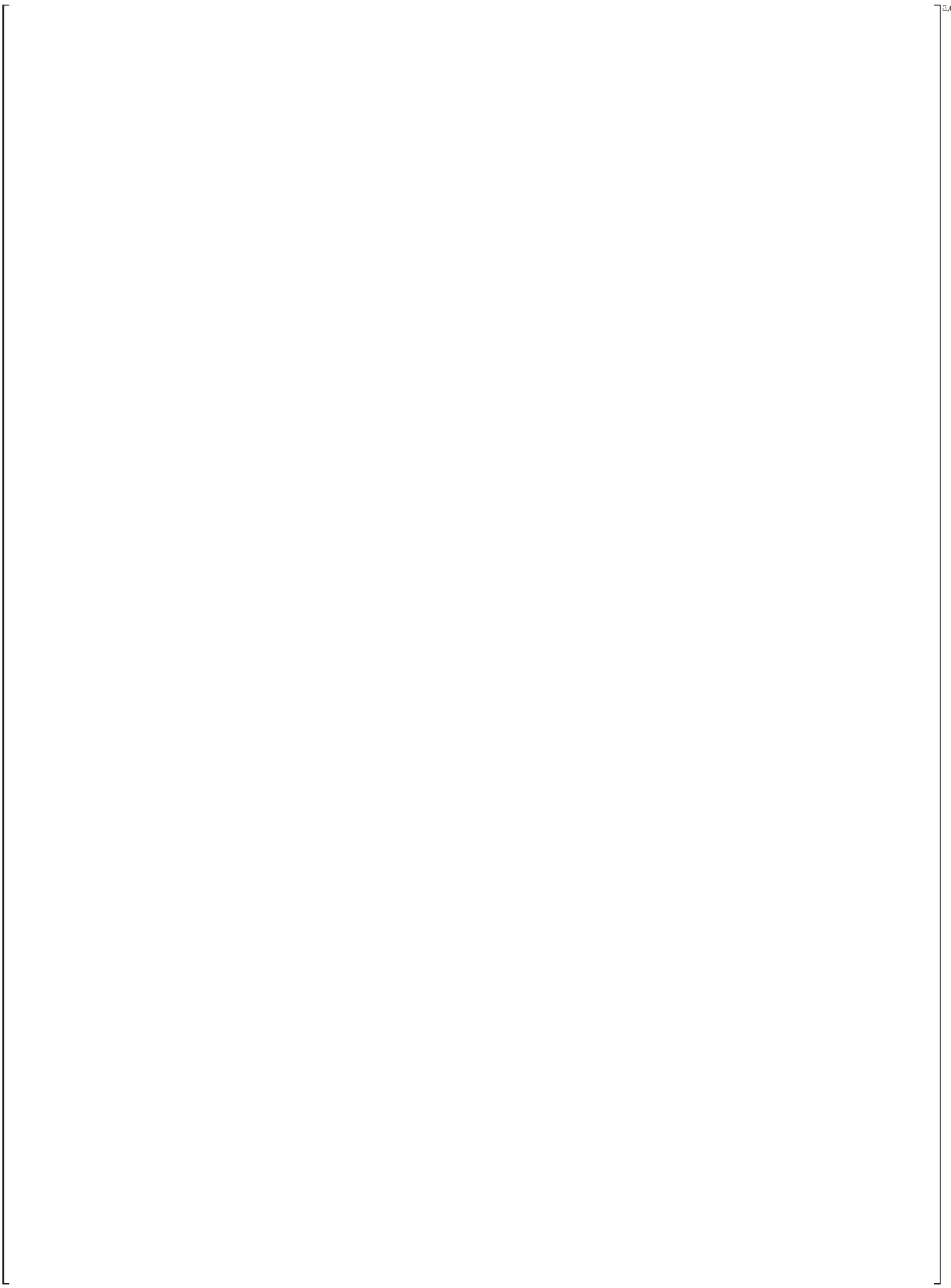


Figure 6-8(1/6) Transmission Format of Transmission Data Output to TDR

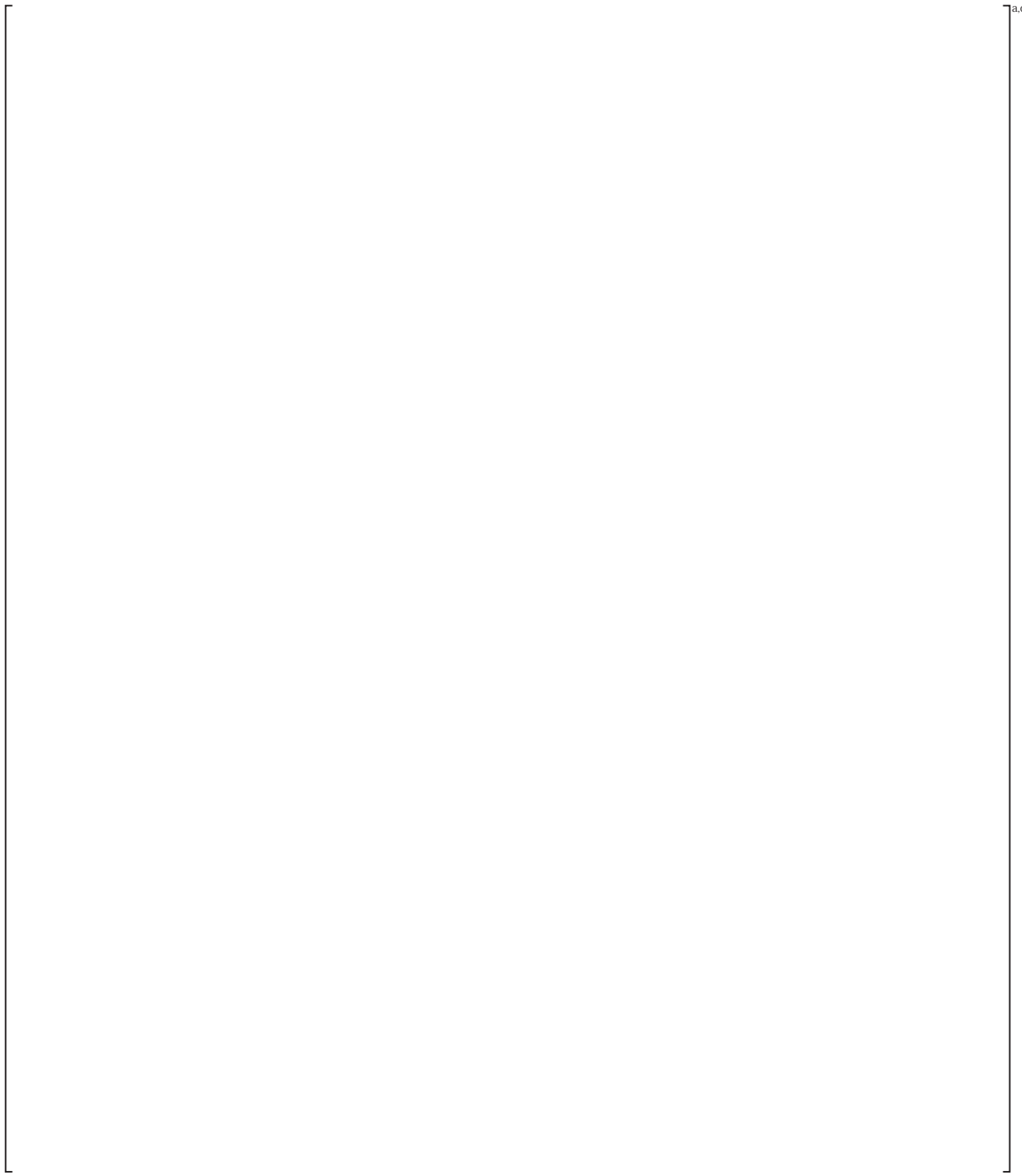


Figure 6-8(2/6) Transmission Format of Transmission Data Output to TDR

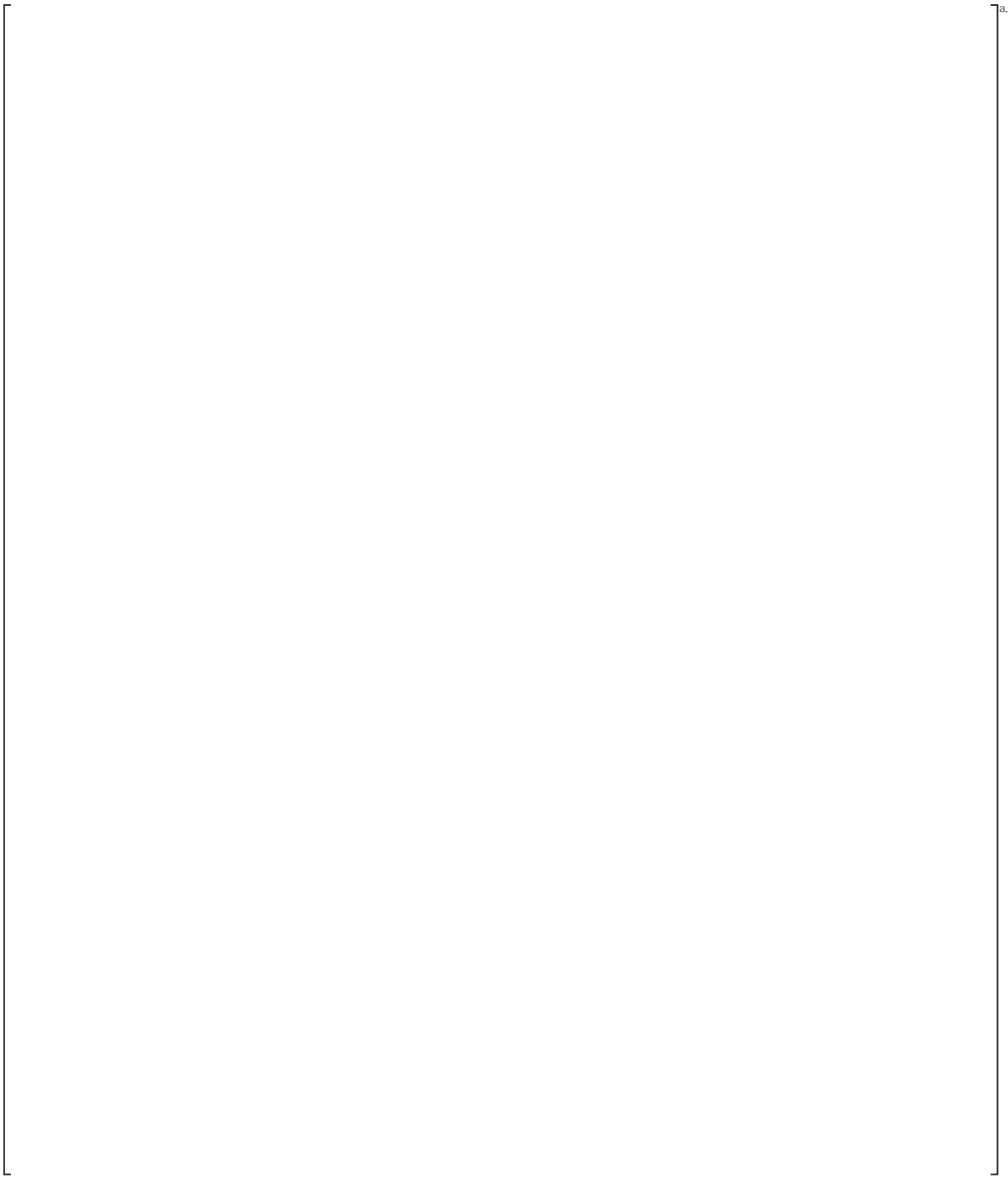


Figure 6-8(3/6) Transmission Format of Transmission Data Output to TDR

a,c

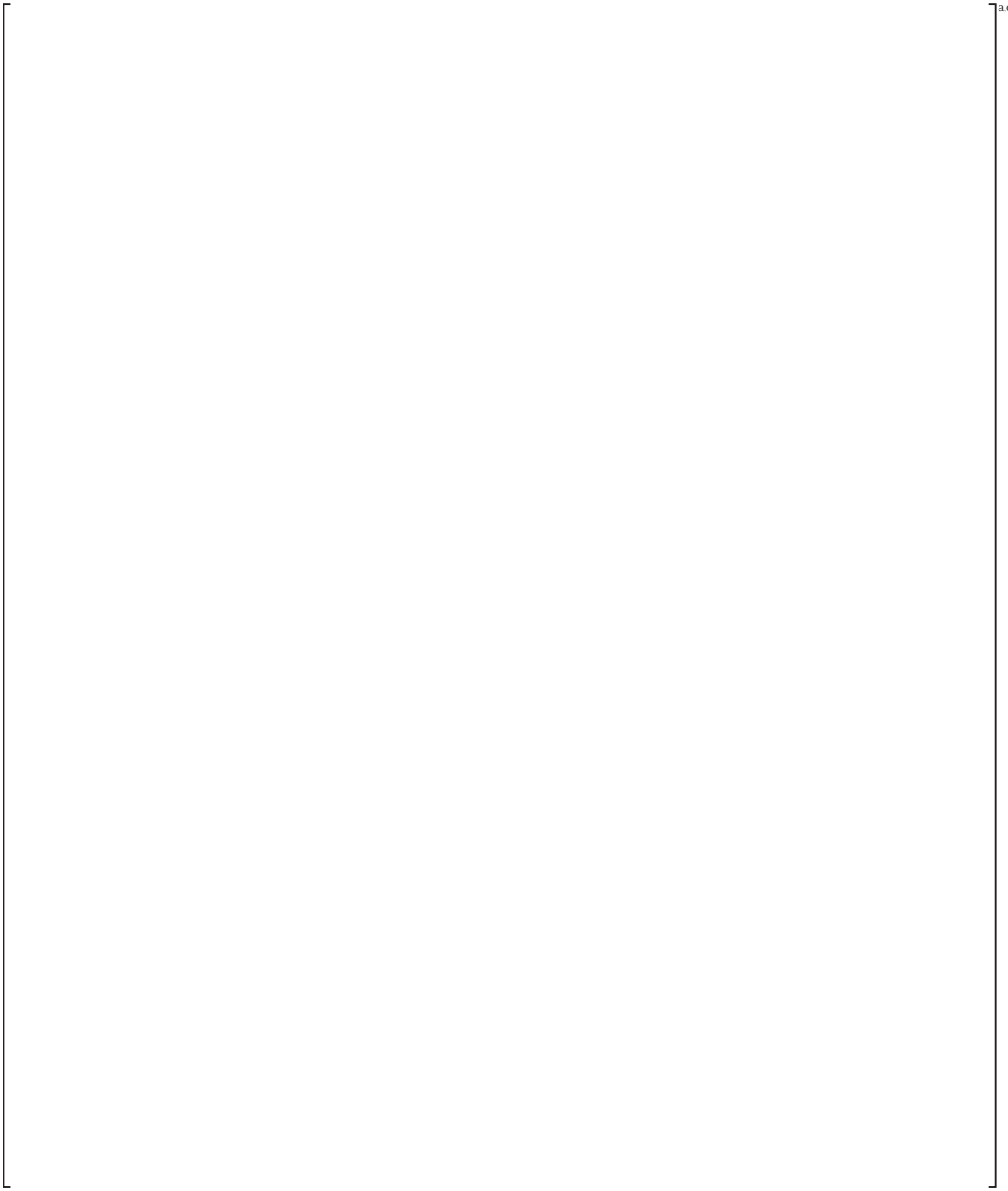


Figure 6-8(4/6) Transmission Format of Transmission Data Output to TDR

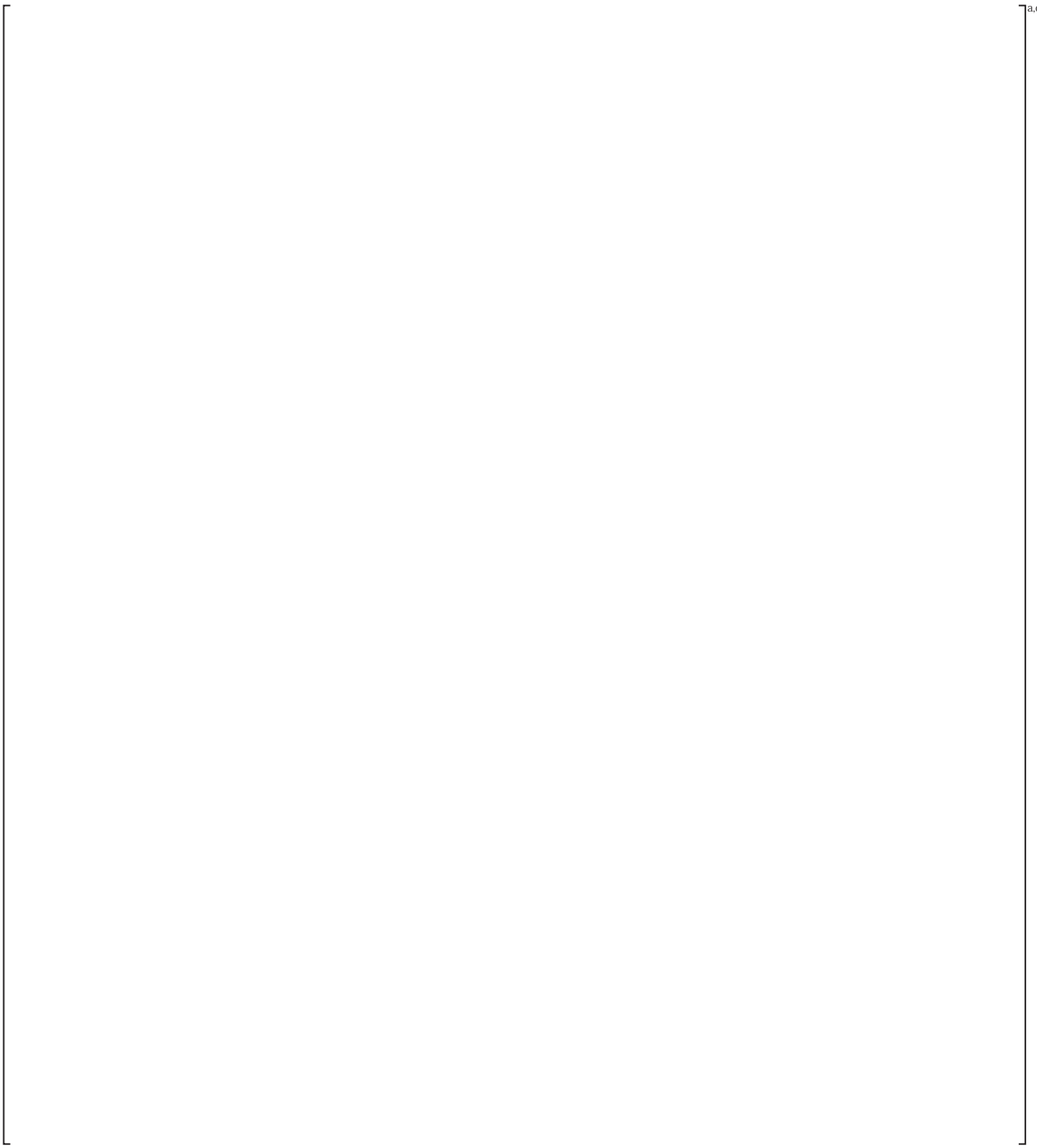


Figure 6-8(5/6) Transmission Format of Transmission Data Output to TDR

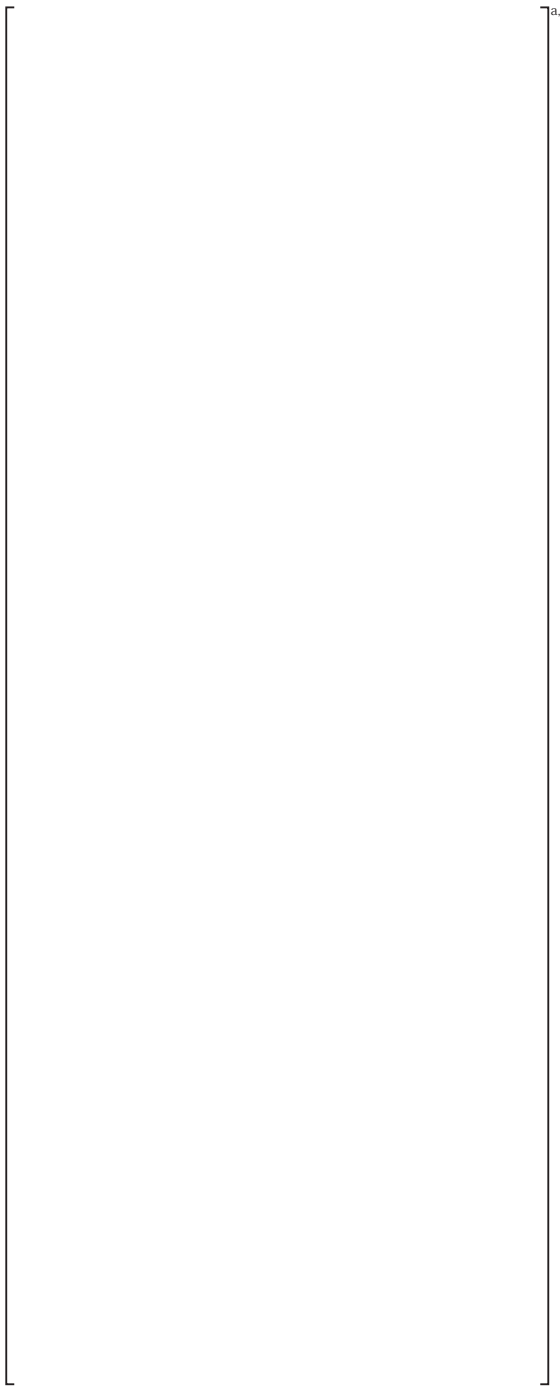


Figure 6-8(6/6) Transmission Format of Transmission Data Output to TDR

a,c

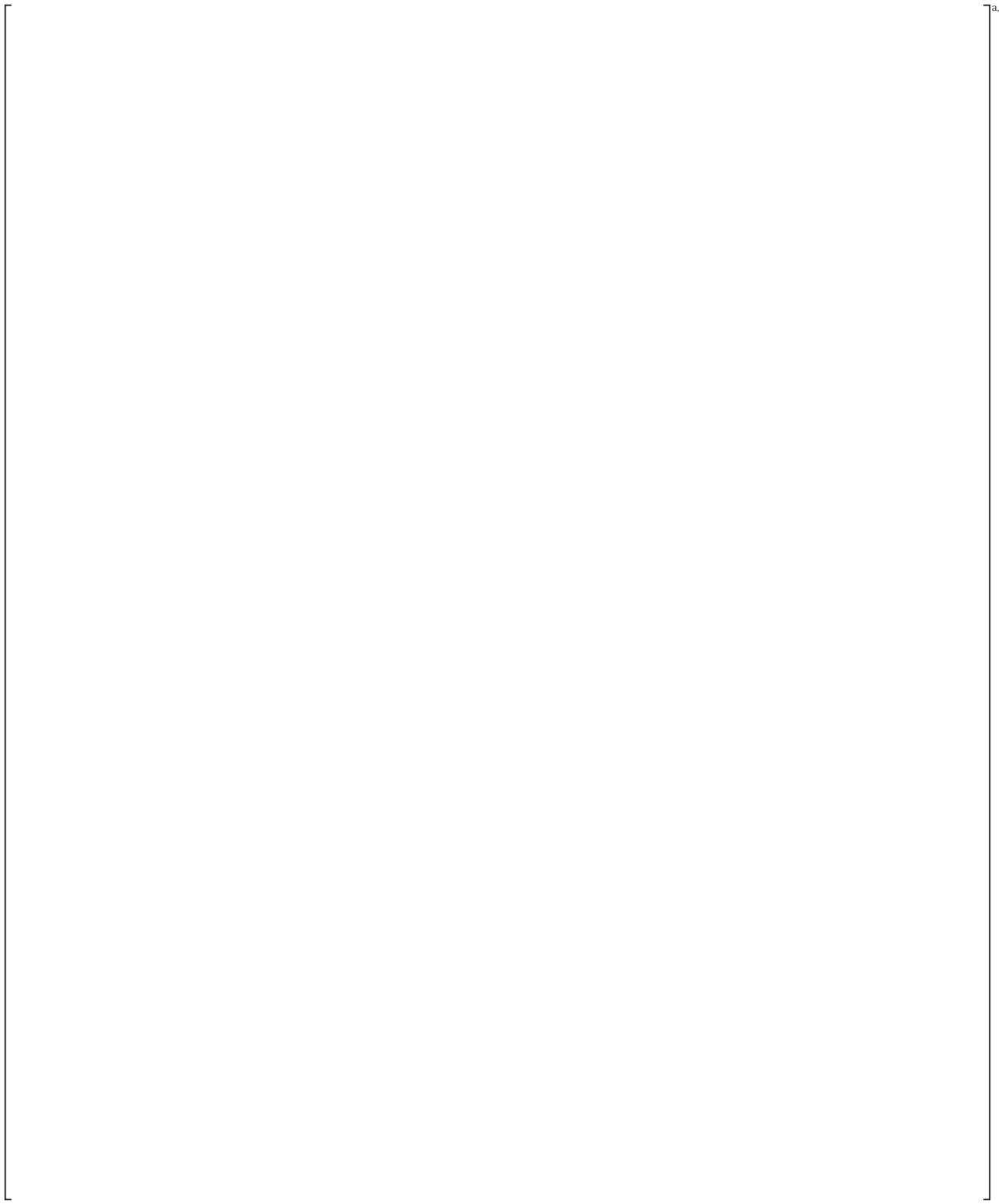


Figure 6-9(1/7) Bit Configuration of Transmission Data Output to TDR

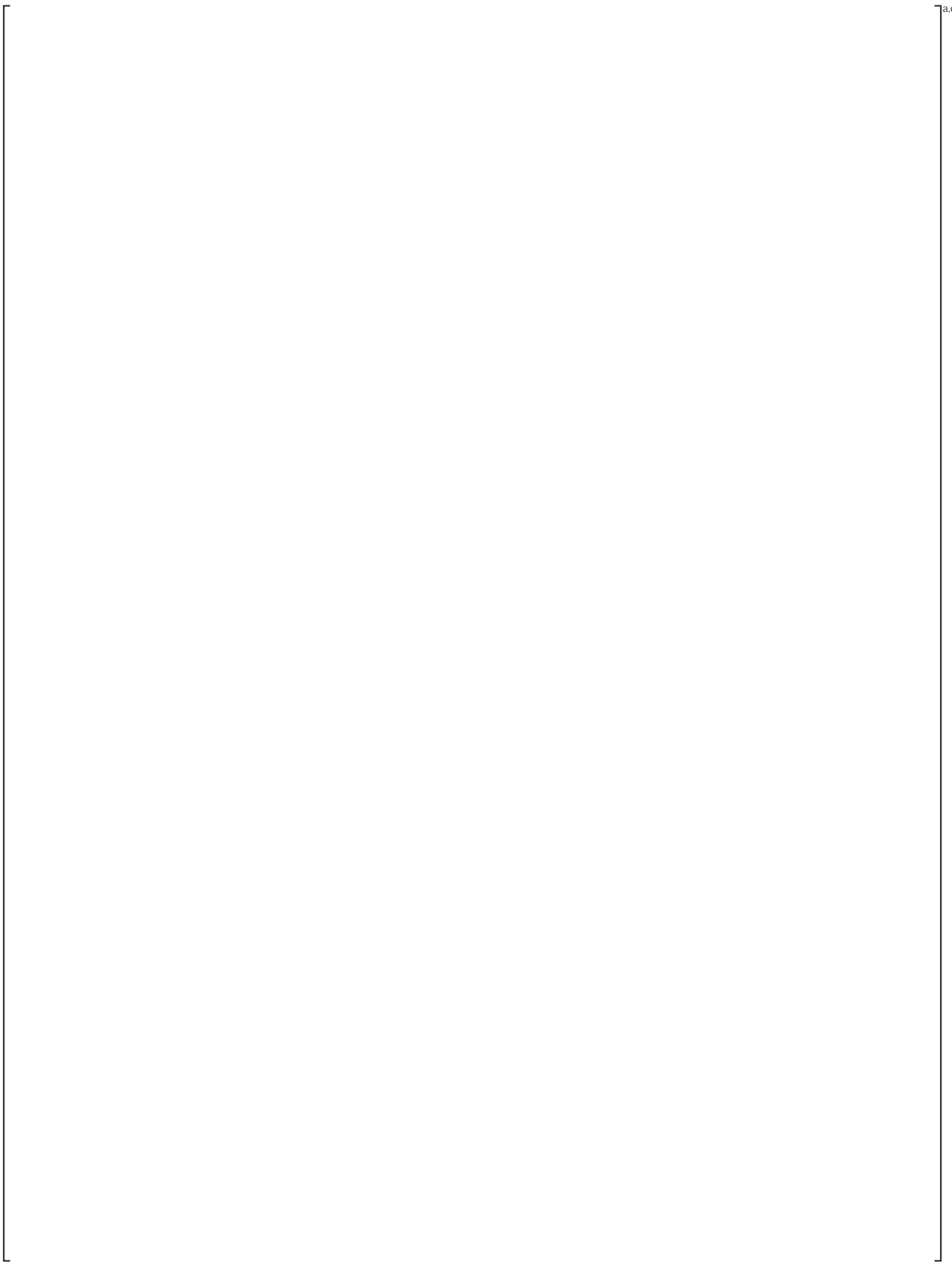


Figure 6-9(2/7) Bit Configuration of Transmission Data Output to TDR

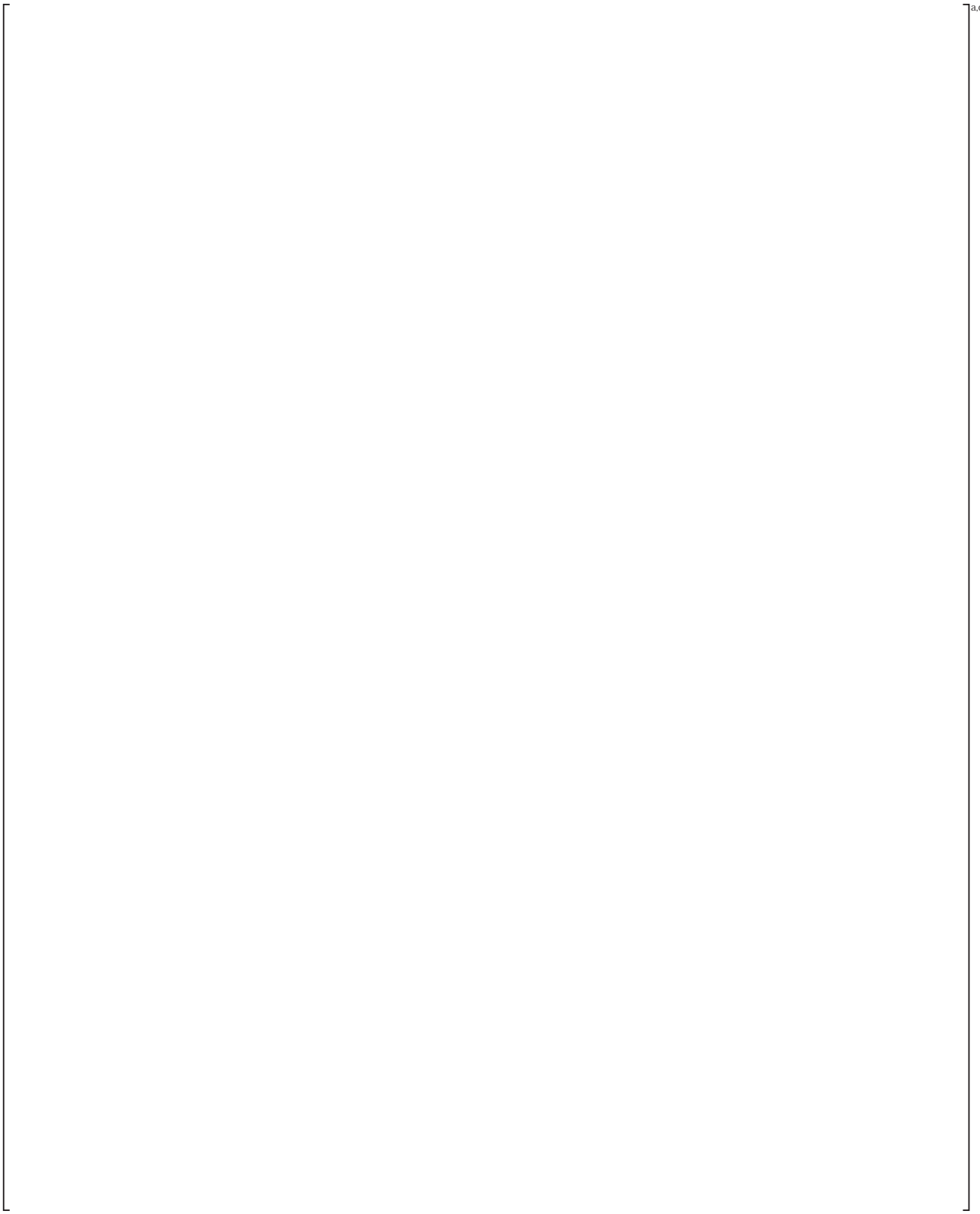


Figure 6-9(3/7) Bit Configuration of Transmission Data Output to TDR

a,c

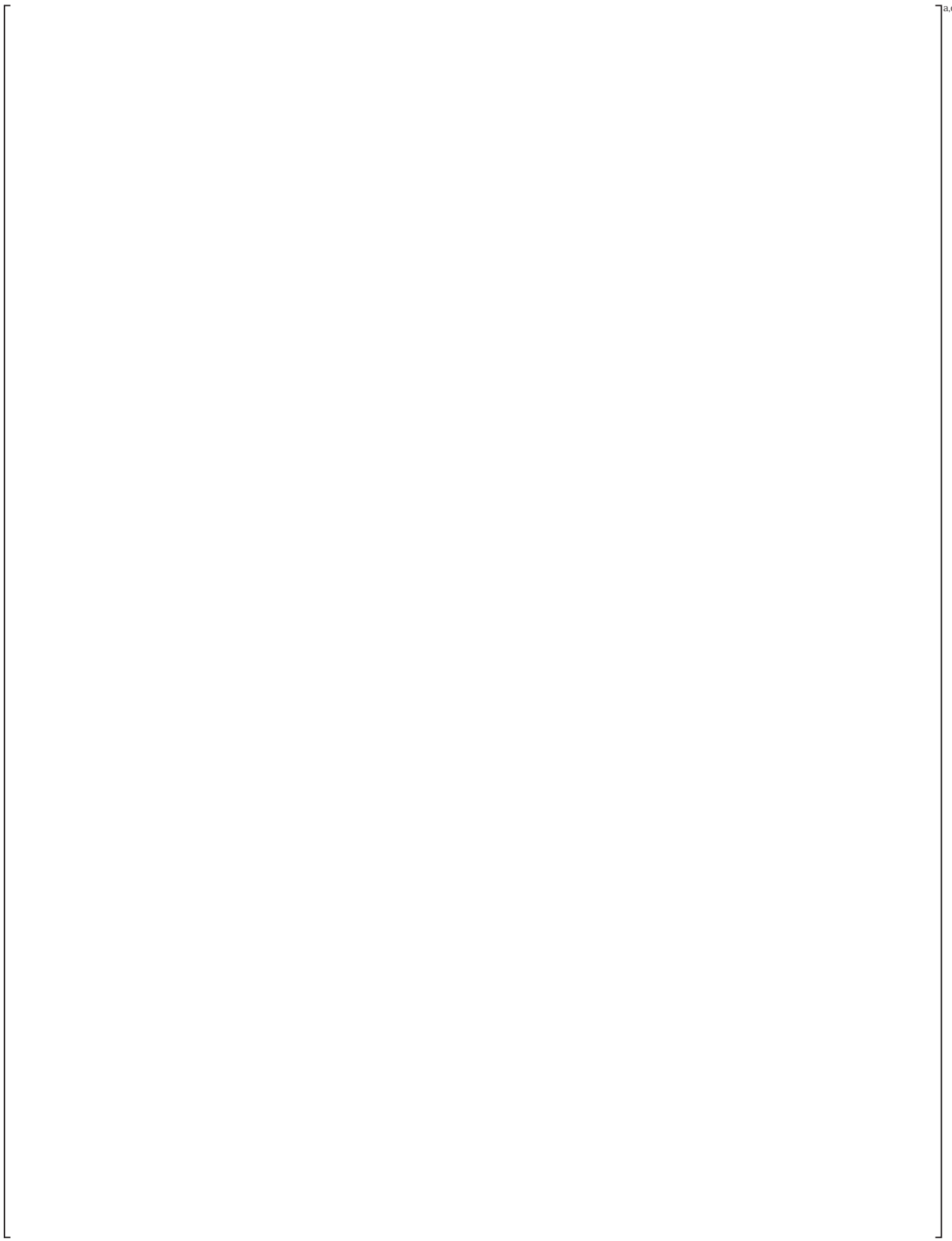


Figure 6-9(4/7) Bit Configuration of Transmission Data Output to TDR

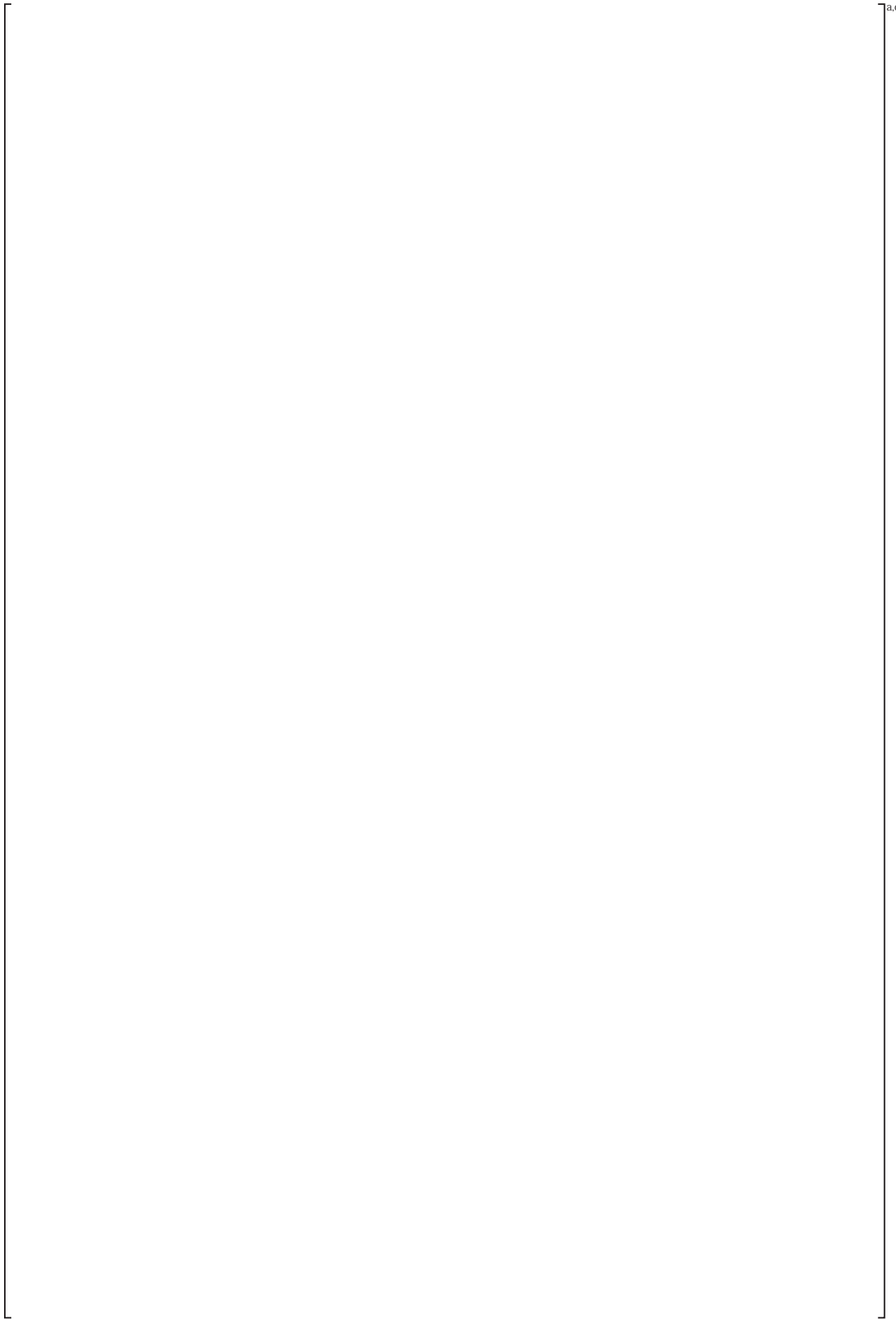


Figure 6-9(5/7) Bit Configuration of Transmission Data Output to TDR

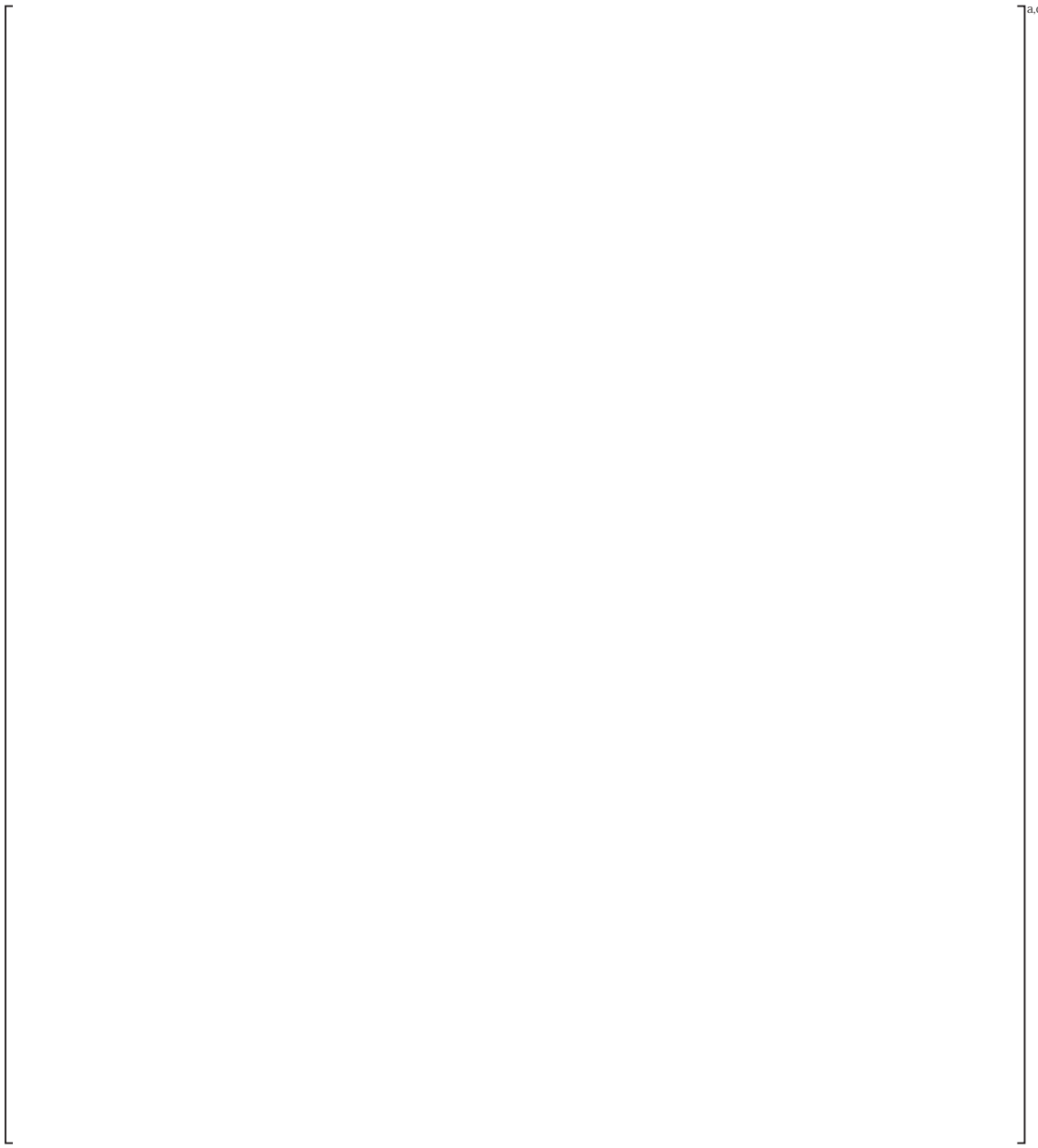


Figure 6-9(6/7) Bit Configuration of Transmission Data Output to TDR

[a,c]

Figure 6-9(7/7) Bit Configuration of Transmission Data Output to TDR

6.2.3. Transmission Signals to Relay Unit

(1) The OPRM unit shall have discrete output transmission interface to the Relay unit and the detail specifications are as follows:

A)	Signal Form	Insulated no-voltage contact output ([ ]a,c)
B)	Logic Level	Contact open ([ ]a,c) when a signal turns on. Contact close ([ ]a,c) when a signal turns off. < Exception > Contact open ([ ]a,c) when the “OPRM Automatic Bypass” signal turns off. Contact close ([ ]a,c) when the “OPRM Automatic Bypass” signal turns on.
C)	Number of Cable	1
D)	Applied Voltage	[ ]a,c
E)	Output Current	[ ]a,c
F)	Reset Form	Auto reset
G)	Withstand Voltage	[ ]a,c
H)	Insulated Resistance	[ ]a,c
I)	Connector	[ ]a,c
J)	Guide Key	Thick guide key: 2, Thin guide key: 1
K)	Pin Assignment	Figure 6-5

6.3. Data Transmission between Modules

6.3.1. LPRM Unit Data (From RCV Module to CELL Module)

(1) The RCV module shall have the interface to provide the following signals to middle plane interface.

A)	Signal Form	three-wire electrical communication link (CMOS)
B)	Logic Level	[ ]a,c
C)	Data Output Cycle	[ ]a,c
D)	Clock Frequency	[ ]a,c
E)	Transmission Waveform	Figure 6-10
F)	Transmission Format	Figure 6-1
G)	Bit Configuration	Figure 6-2

(2) The CELL module shall have the interface to receive the above signals from middle plane interface.

[ ]a,c

Figure 6-10 Transmission Waveform of LPRM Input Data

6.3.2. APRM Unit Data (From RCV Module to CELL Module)

(1) The RCV module shall have the interface to provide the following signals to middle plane interface.

A)	Signal Form	three-wire electrical communication link (CMOS)
B)	Logic Level	[ ]a,c
C)	Data Output Cycle	[ ]a,c
D)	Clock Frequency	[ ]a,c
E)	Transmission Waveform	Figure 6-11
F)	Transmission Format	Figure 6-3
G)	Bit Configuration	Figure 6-4

(2) The CELL module shall have the interface to receive the above signals from middle plane interface.

[ ]a,c

Figure 6-11 Transmission Waveform of APRM Input Data

6.3.3. OPRM Cell Data (From CELL Module to AGRD, PBD and DAT/ST Modules)

(1) The CELL module shall have the interface to provide following signals to middle plane interface.

A) Signal Form three-wire electrical communication link (CMOS)
B) Logic Level [ ]a,c
C) [Deleted]
D) Transmission Cycle [ ]a,c
E) Clock Frequency [ ]a,c
F) Transmission Waveform Figure 6-12
G) Transmission Format Figure 6-13
H) Bit Configuration Figure 6-14

(2) The AGRD, PBD and DAT/ST module shall have the interface to receive above signals from middle plane interface.

[ ]a,c

Figure 6-12 Transmission Waveform of OPRM Cell Data

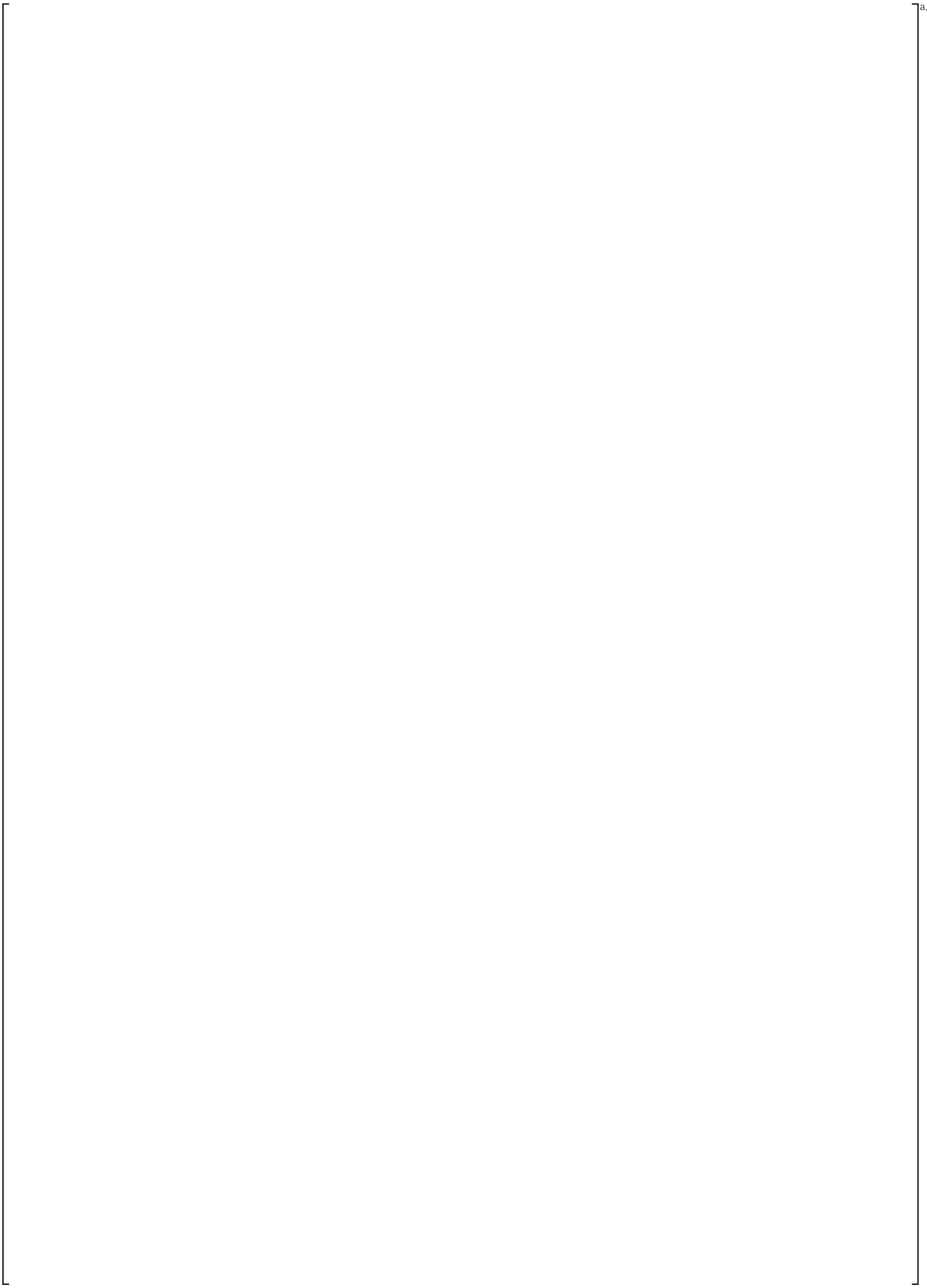


Figure 6-13 Transmission Format of OPRM Cell Data

Figure 6-14 Bit Configuration of OPRM Cell Data

6.3.4. OPRM Calculation Data (From CELL Module to DAT/ST Module)

(1) The CELL module shall have the interface to provide the following signals to middle plane interface.

A)	Signal Form	three-wire electrical communication link (CMOS)
B)	Logic Level	[ ]a,c
C)	Number of Output	[ ]a,c
D)	Transmission Cycle	[ ]a,c
E)	Clock Frequency	[ ]a,c
F)	Transmission Waveform	Figure 6-15
G)	Transmission Format	Figure 6-16
H)	Bit Configuration	Figure 6-17

(2) The DAT/ST module shall have the interface to receive the above signals from middle plane interface.

Figure 6-15 Transmission Waveform of OPRM Calculation Data

a,c

a,c

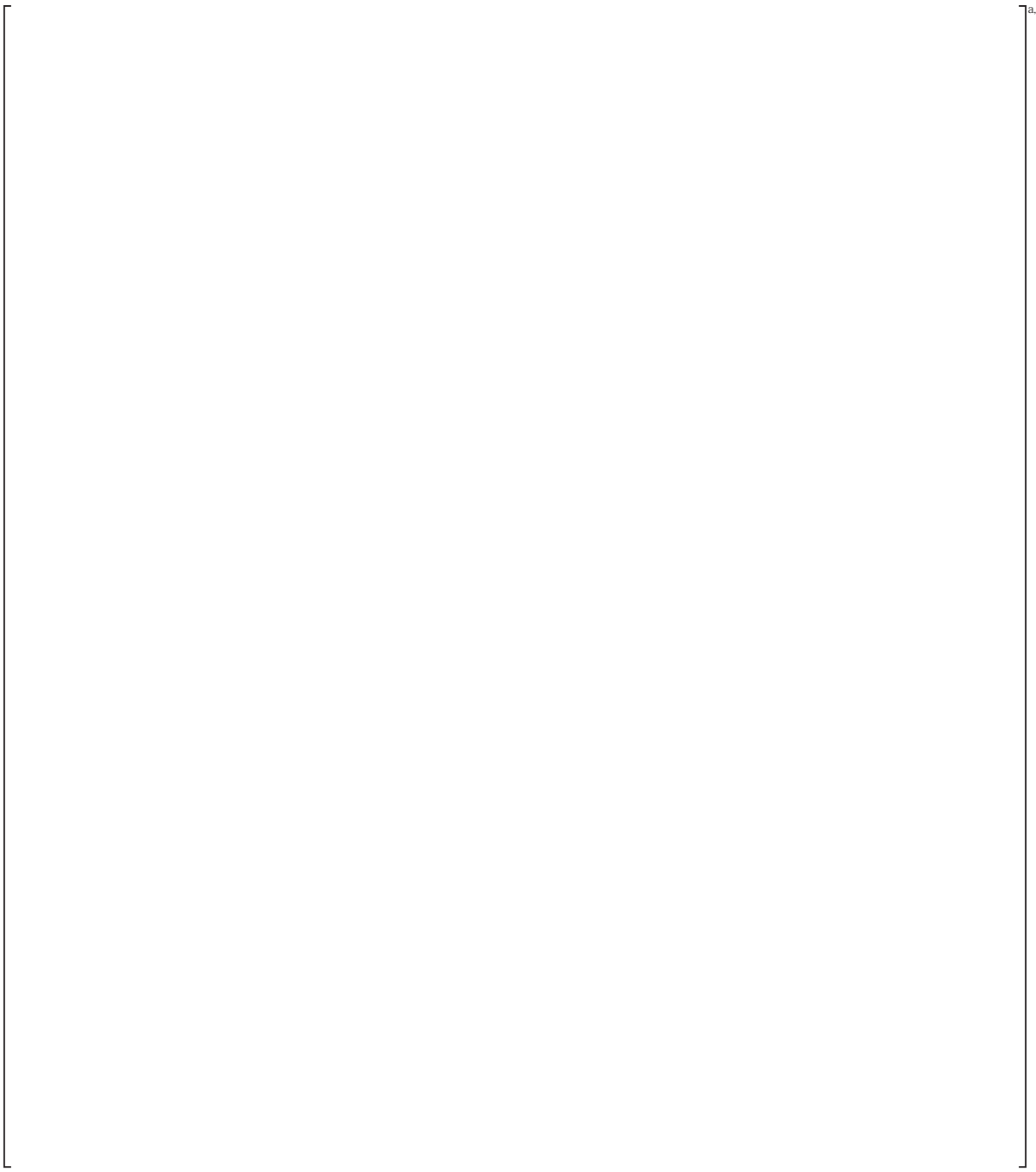


Figure 6-16(2/4) Transmission Format of OPRM Calculation Data

[a,c]

Figure 6-16(3/4) Transmission Format of OPRM Calculation Data

a,c

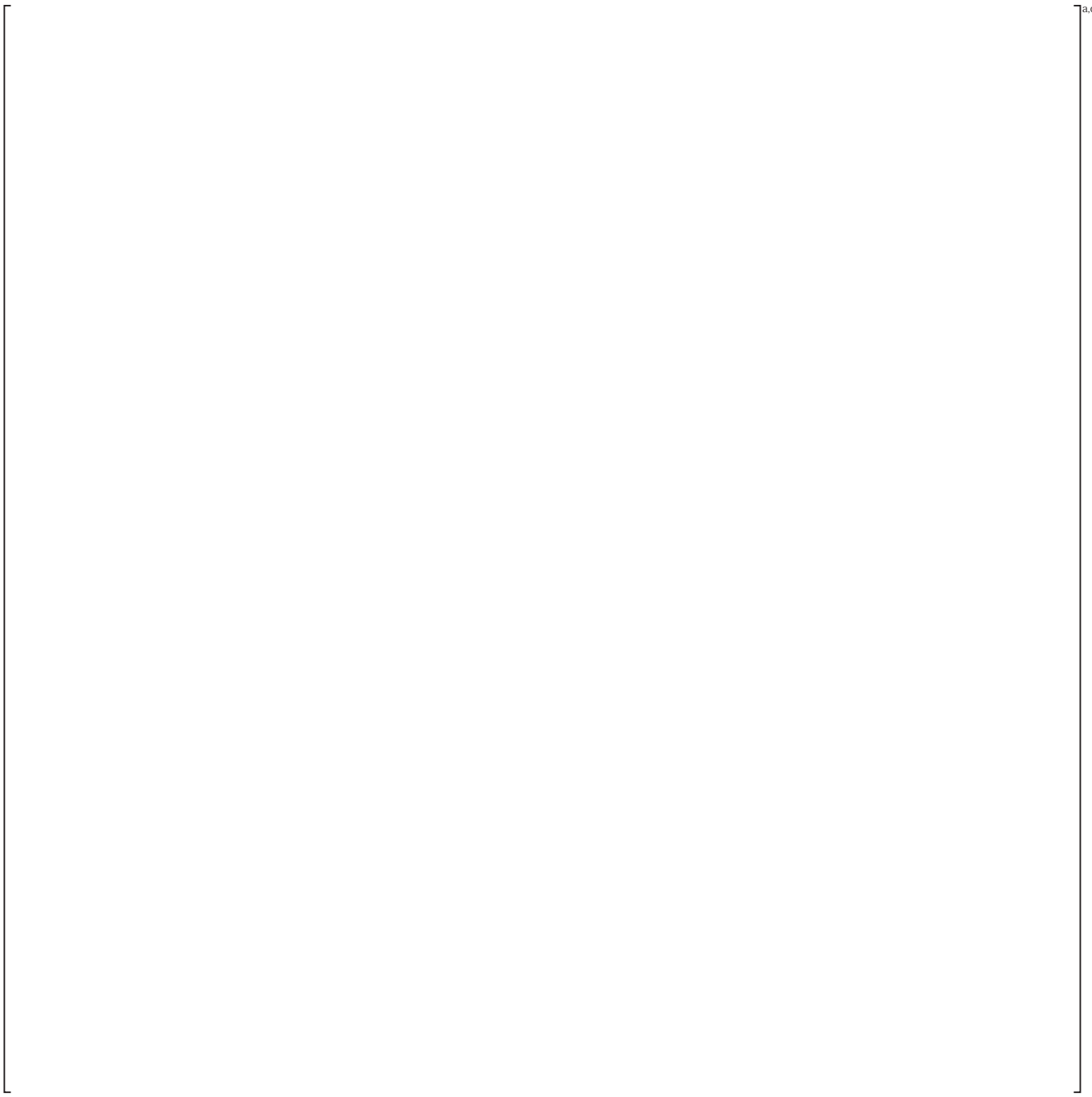


Figure 6-16 (4/4) Transmission Format of OPRM Calculation Data

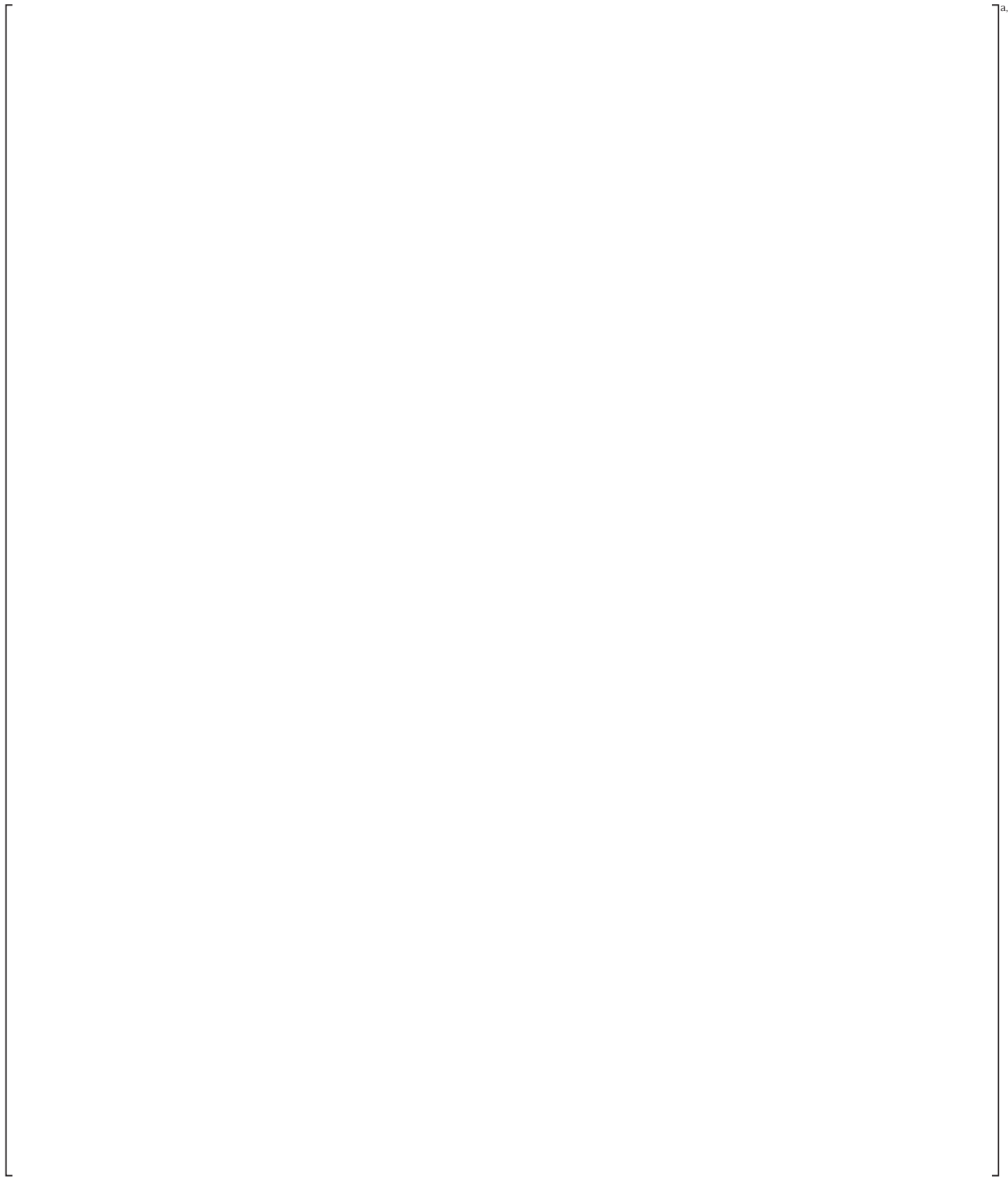


Figure 6-17 (1/3) Bit Configuration of OPRM Calculation Data

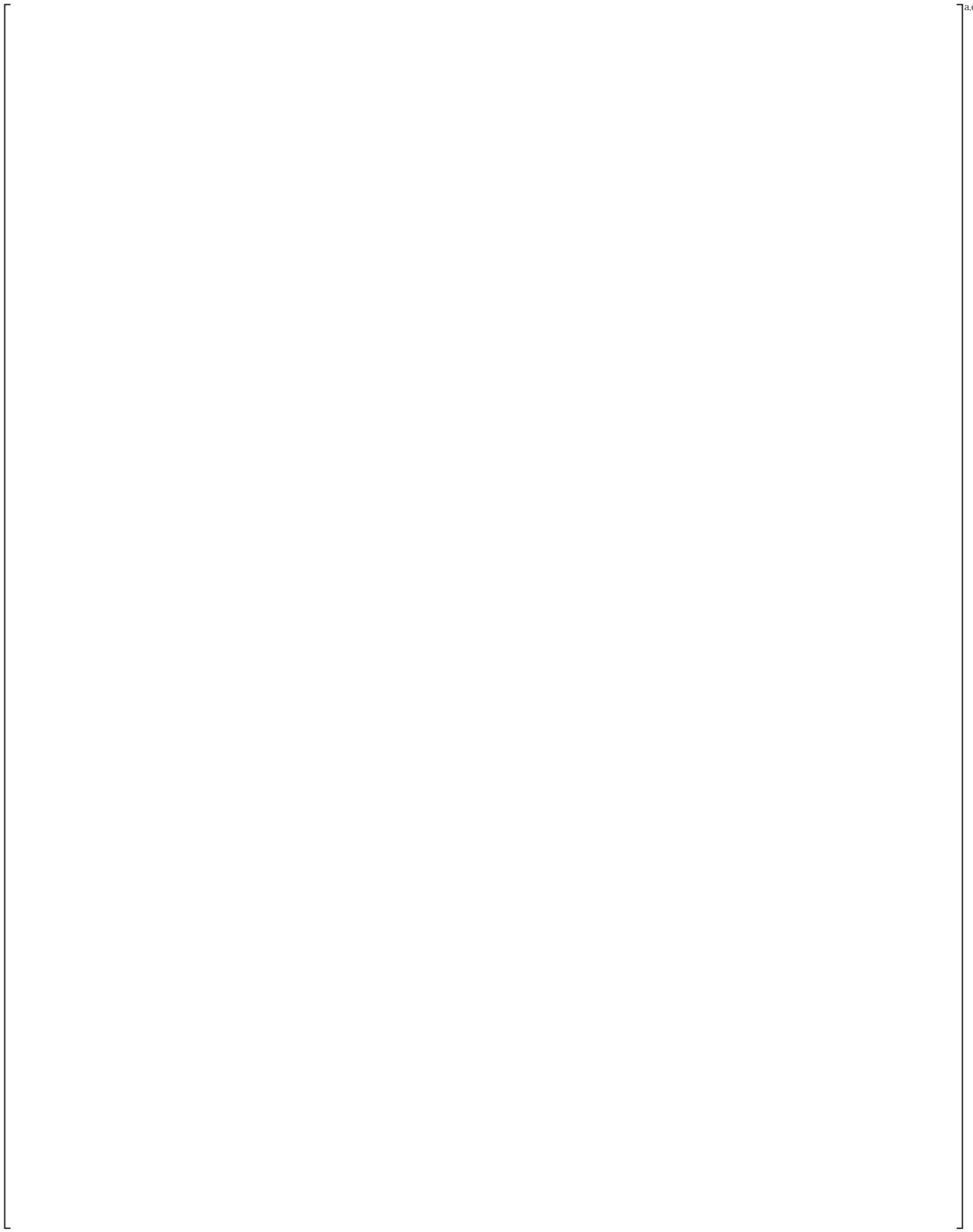


Figure 6-17 (2/3) Bit Configuration of OPRM Calculation Data

a,c

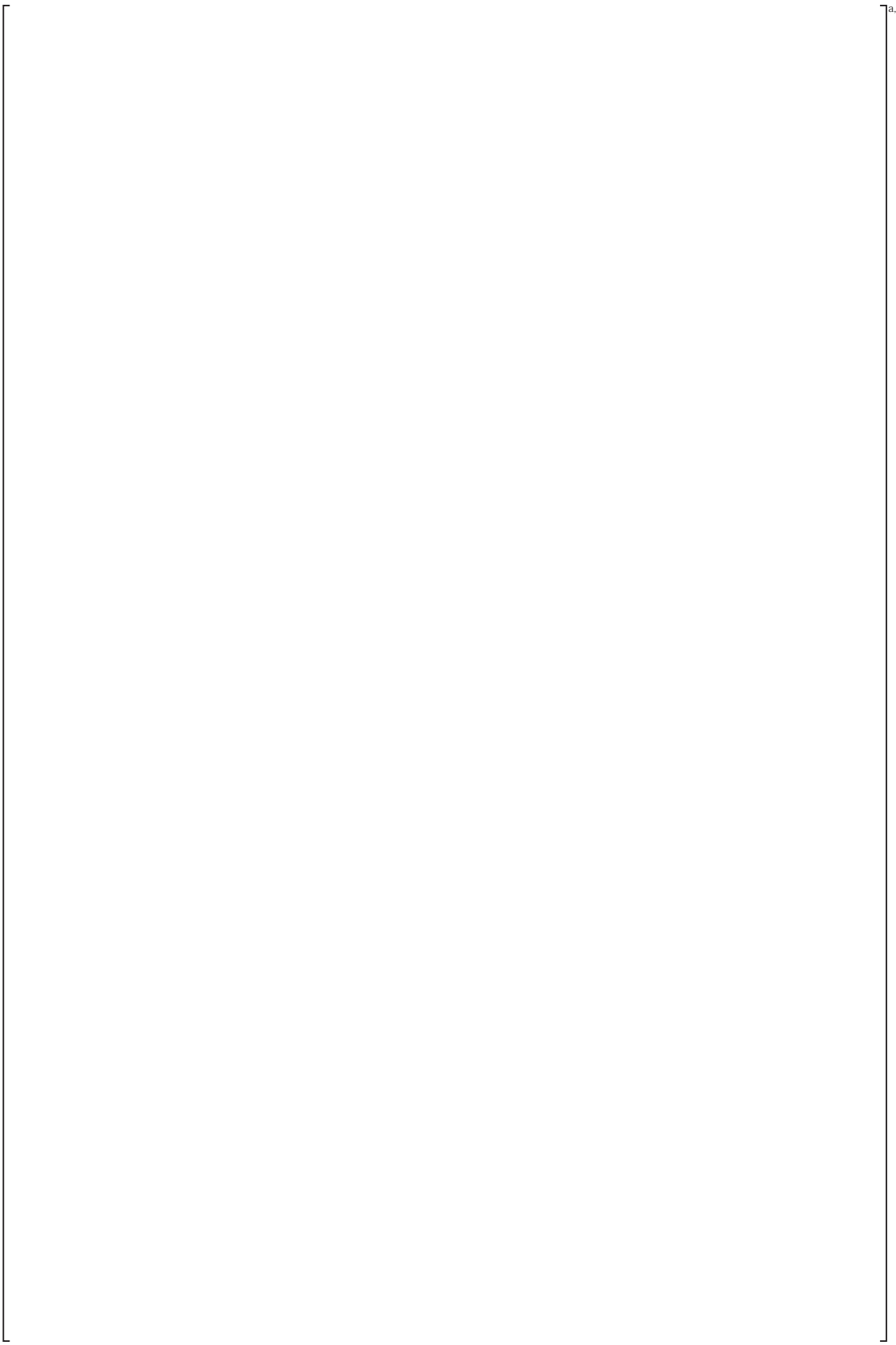


Figure 6-17 (3/3) Bit Configuration of OPRM Calculation Data

6.3.5. AGRD Calculation Data (From AGRD Module to DAT/ST Module)

(1) The AGRD module shall have the interface to provide the following signals to middle plane interface.

A)	Signal Form	three-wire electrical communication link (CMOS)
B)	Logic Level	[redacted]
C)	Transmission Cycle	[redacted]
D)	Clock Frequency	[redacted]
E)	Transmission Waveform	Figure 6-18
F)	Transmission Format	Figure 6-19
G)	Bit Configuration	Figure 6-20

(2) The DAT/ST module shall have the interface to receive the above signals from middle plane interface.

[redacted]

Figure 6-18 Transmission Waveform of AGRD Calculation Data

a,c

Figure 6-19(1/2) Transmission Format of AGRD Calculation Data

a,c

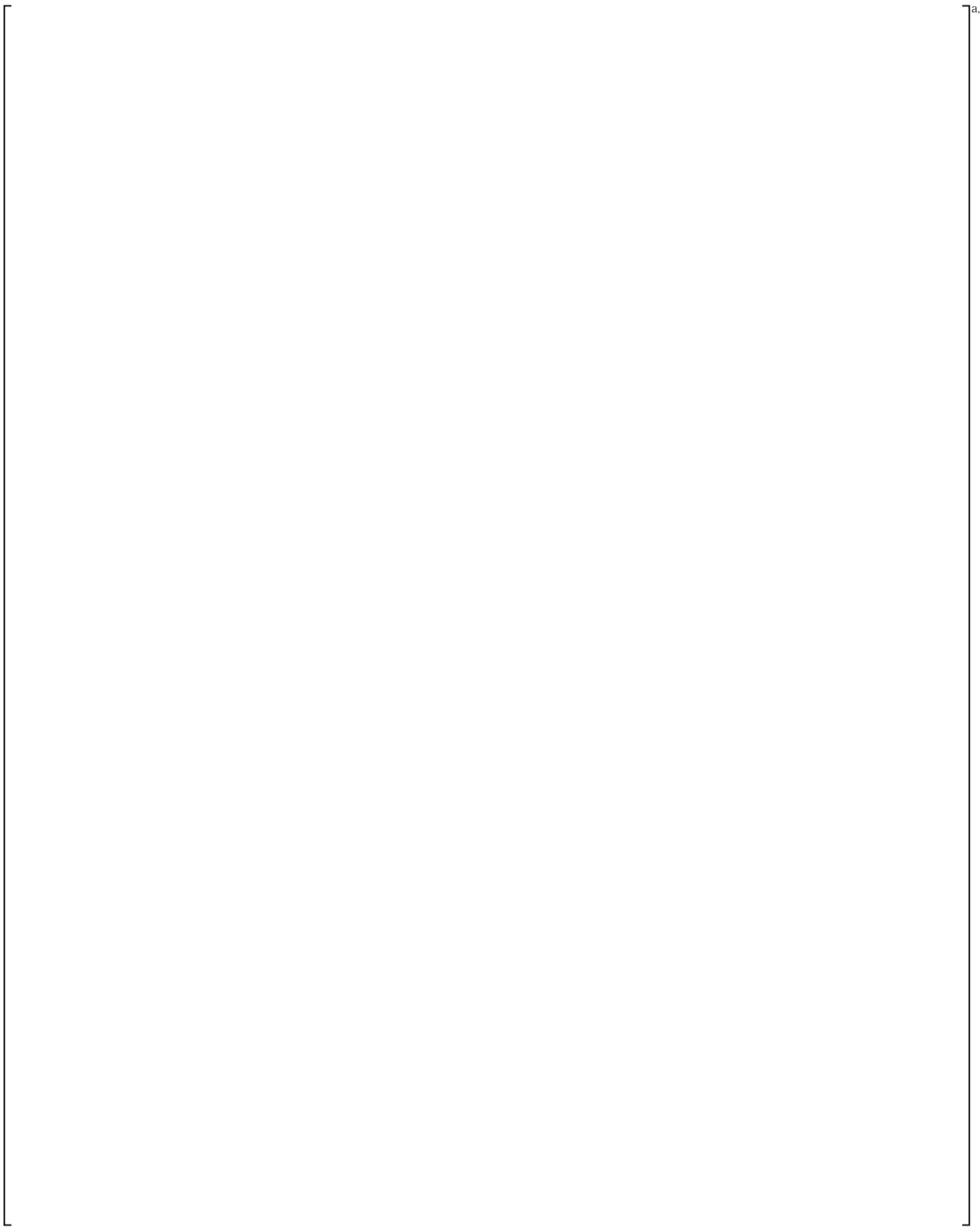


Figure 6-19(2/2) Transmission Format of AGRD Calculation Data

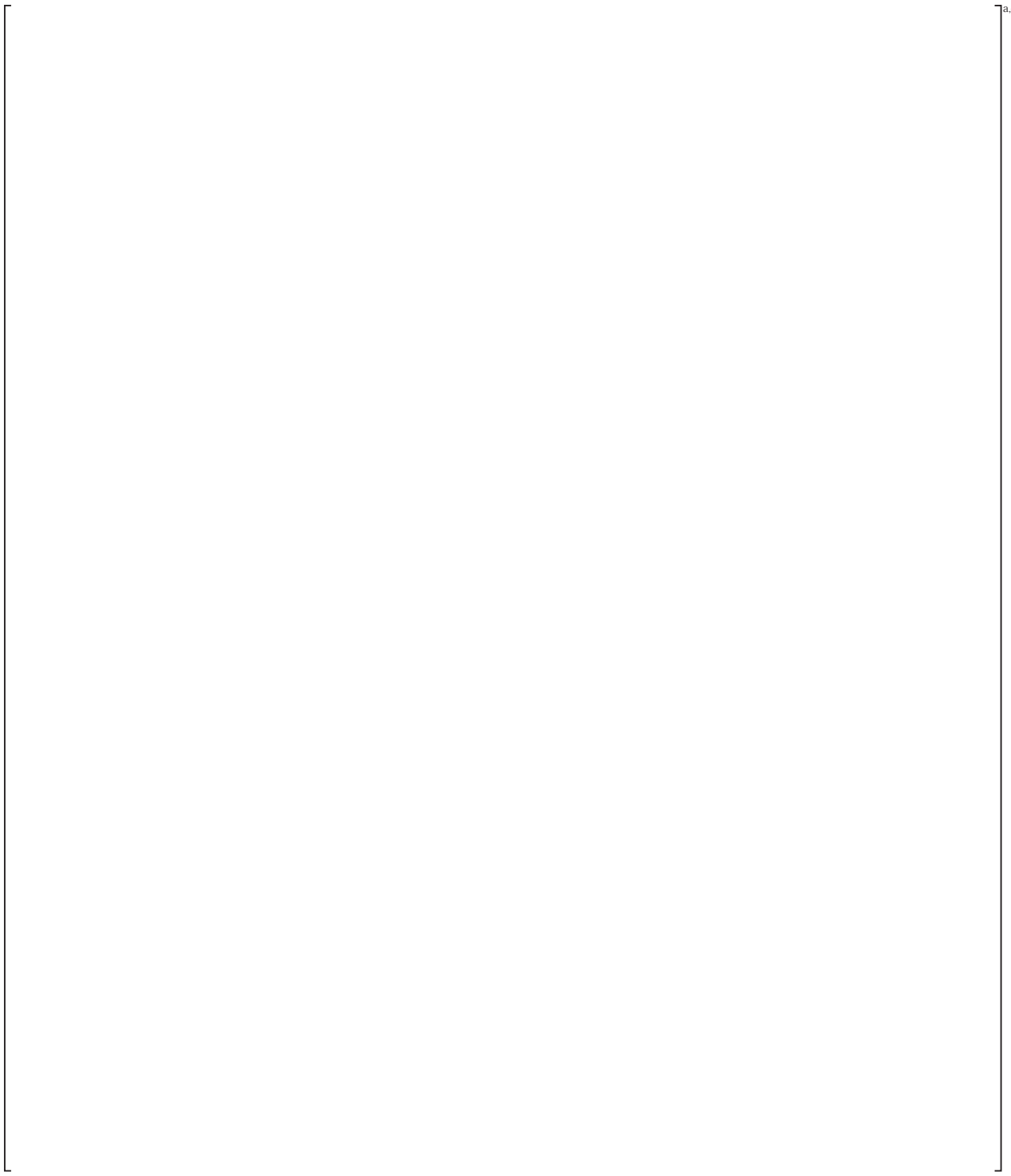


Figure 6-20(1/3) Bit Configuration of AGRD Calculation Data

a,c

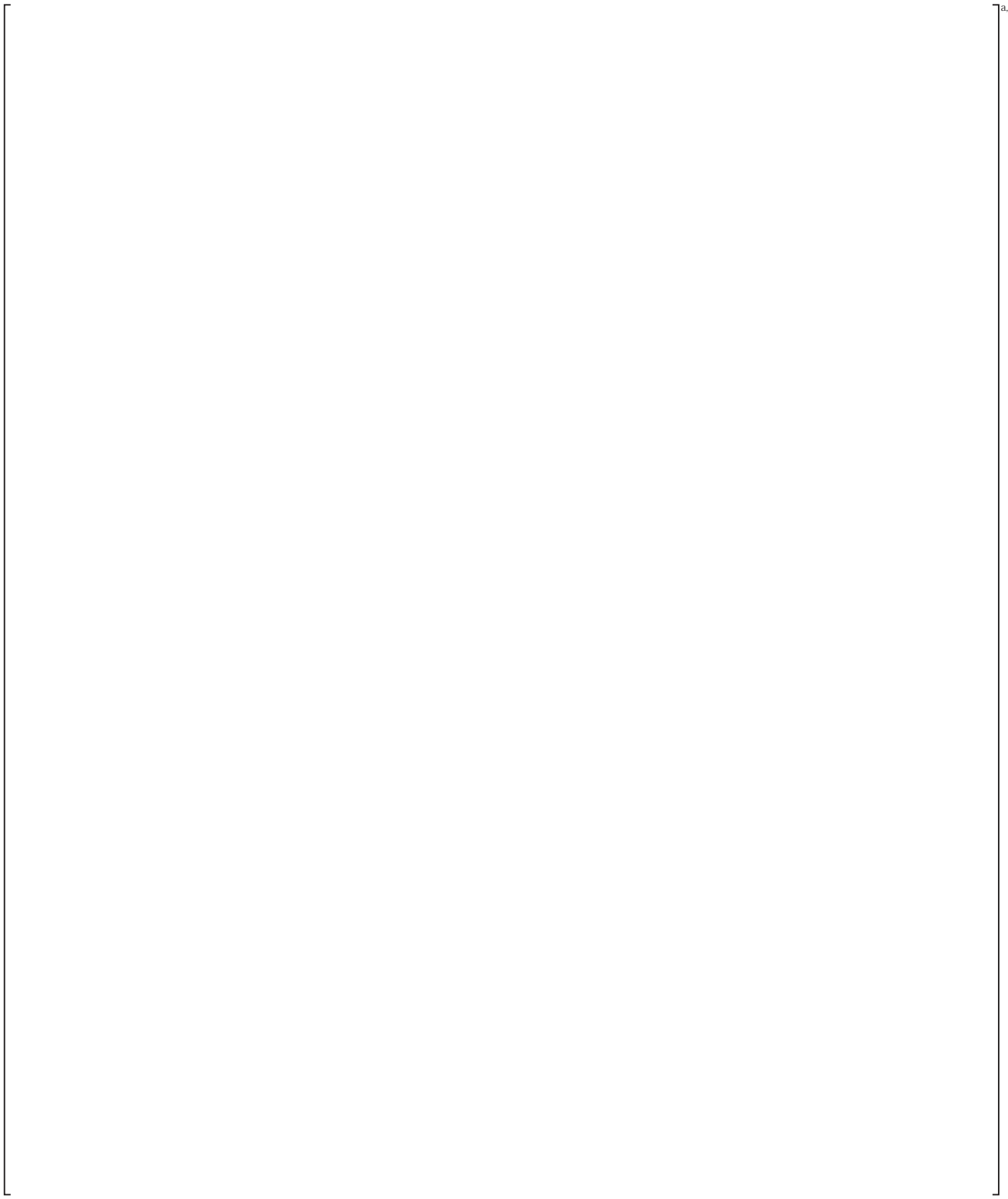


Figure 6-20(2/3) Bit Configuration of AGRD Calculation Data

[a,c]

Figure 6-20(3/3) Bit Configuration of AGRD Calculation Data

6.3.6. PBD Calculation Data (From PBD Module to DAT/ST Module)

(1) The PBD module shall have the interface to provide the following signals to middle plane interface.

A)	Signal Form	three-wire electrical communication link (CMOS)
B)	Logic Level	[ ]a,c
C)	Transmission Cycle	[ ]a,c
D)	Clock Frequency	[ ]a,c
E)	Transmission Waveform	Figure 6-21
F)	Transmission Format	Figure 6-22
G)	Bit Configuration	Figure 6-23

(2) The DAT/ST module shall have the interface to receive the above signals from middle plane interface.

[ ]a,c

Figure 6-21 Transmission Waveform of PBD Calculation Data

a,c

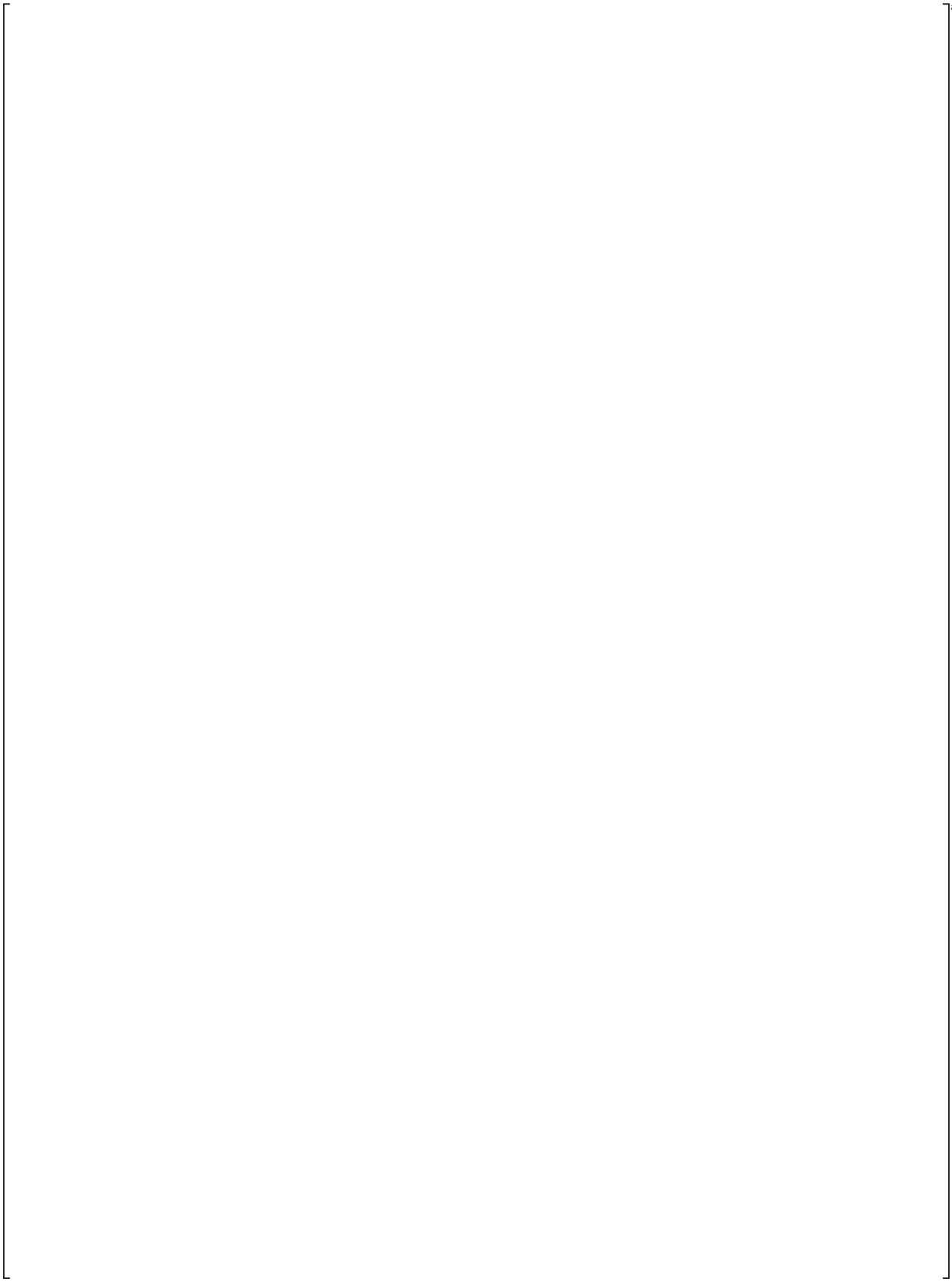


Figure 6-22 Transmission Format of PBD Calculation Data

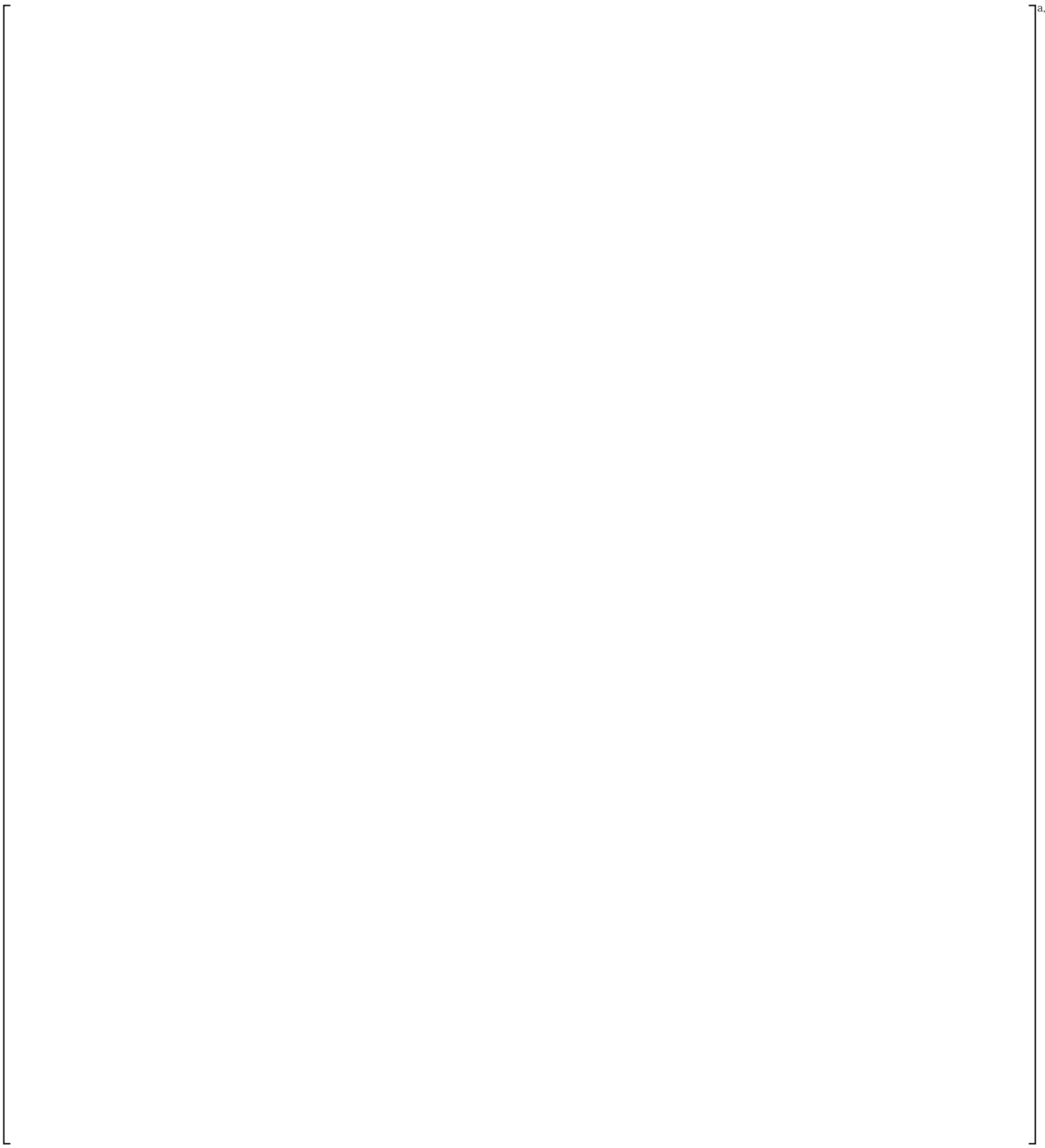


Figure 6-23(1/2) Bit Configuration of PBD Calculation Data

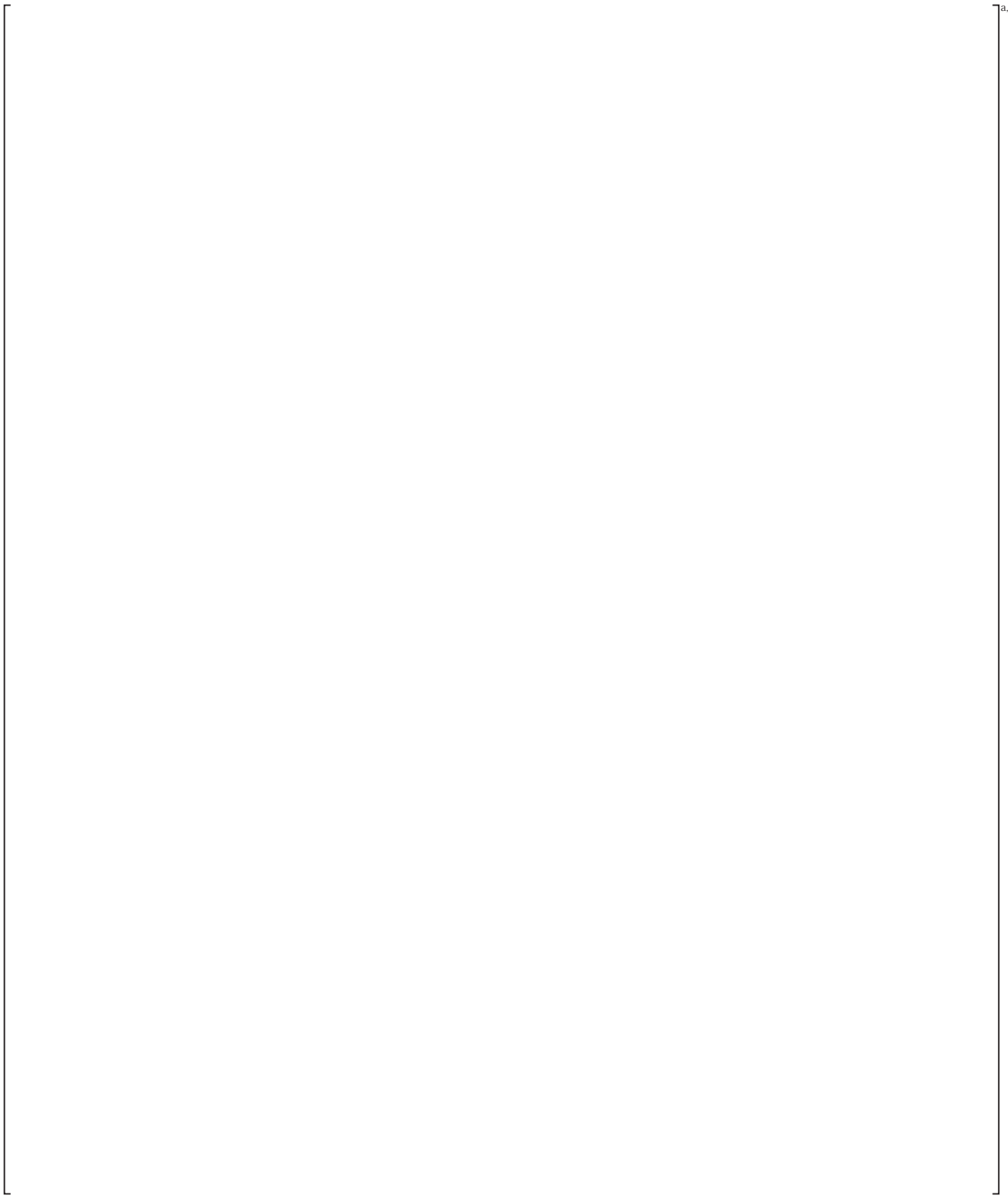


Figure 6-23(2/2) Bit Configuration of PBD Calculation Data

6.3.7. OPRM Multiplexed Data (From DAT/ST module to TRN module)

(1) The DAT/ST module shall have the interface to provide the following signals to middle plane interface.

A)	Signal Form	three-wire electrical communication link (CMOS)
B)	Logic Level	[ ]a,c
C)	Transmission Cycle	[ ]a,c
D)	Clock Frequency	[ ]a,c
E)	Transmission Waveform	Figure 6-24
F)	Transmission Format	Figure 6-6
G)	Bit Configuration	Figure 6-7

(2) The TRN module shall have the interface to receive the above signals from middle plane interface.

[ ]a,c

Figure 6-24 Transmission Waveform of OPRM Multiplexed Data

6.3.8. OPRM Record Data (From DAT/ST module to TRN module)

(1) The DAT/ST module shall have the interface to provide the following signals to middle plane interface.

A)	Signal Form	three-wire electrical communication link (CMOS)
B)	Logic Level	[ ]a,c
C)	Transmission Cycle	[ ]a,c
D)	Clock Frequency	[ ]a,c
E)	Transmission Waveform	Figure 6-25
F)	Transmission Format	Figure 6-8
G)	Bit Configuration	Figure 6-9

(2) The TRN module shall have the interface to receive the above signals from middle plane interface.

[ ]a,c

Fig 6-25 Transmission Waveform of OPRM Record Data

6.3.9. LPRM Unit Data Input Error Signal (From RCV Module to CELL Module)

(1) The RCV module shall have the interface to send the following signals to middle plane interface.

A) Signal Name [a,c]

B) Number of Output

C) Output Method

D) Logic Level

(2) The CELL module shall have the interface to receive the above signals from middle plane interface.

6.3.10. APRM Unit Data Input Error Signal (From RCV Module to CELL Module)

(1) The RCV module shall have the interface to send the following signals to middle plane interface.

A) Signal Name [a,c]

B) Number of Output

C) Output Method

D) Logic Level

(2) The CELL module shall have the interface to receive the above signals from middle plane interface.

6.3.11. APRM Bypass Signal (From DIO module to CELL module)

(1) The DIO module shall have the interface to send the following signals to middle plane interface.

A) Signal Name [a,c]

B) Number of Output

C) Output Method

D) Logic Level

(2) The CELL module shall have the interface to receive the above signals from middle plane interface.

6.3.12. OPRM Inoperative Signal (From [ ]a,c of AGRD, PBD and CELL Modules to DAT/ST and DIO Modules)

(1) The CELL, AGRD and PBD modules shall have the interface to send the following signals to middle plane interface.

A) Signal Name
B) Number of Output
C) Output Method
D) Logic Level

[ ]a,c

(2) The middle plane shall connect three "OPRM Inoperative signals" from the CELL module, AGRD module and PBD module by the [ ]a,c described in Figure 6-26.

(3) The CELL, DAT/ST and DIO module shall have the interface to receive the following signals from middle plane interface.

A) Signal Name
B) Number of Input
C) Input Method
D) Logic Level

[ ]a,c

[ ]a,c

Figure 6-26 I/F Circuit for Logical Sum of Inoperative Signals

6.3.13. OPRM Minor Failure Signal (From [ ]a,c of AGRD, PBD, CELL and DAT/ST Modules to DAT/ST and DIO Modules)

(1) The CELL, AGRD, PBD and DAT/ST module shall have the interface to send the following signals to middle plane interface.

A) Signal Name
B) Number of Output
C) Output Method
D) Logic Level

[ ]a,c

(2) The middle plane shall connect four OPRM Minor Failure signals from the CELL, AGRD, PBD module and DAT/ST module by the [ ]a,c described in Figure 6-27.

(3) The DIO module shall have the interface to receive the following signals from middle plane interface.

A) Signal Name
B) Number of Input
C) Input Method
D) Logic Level

[ ]a,c

[ ]a,c

Figure 6-27 I/F Circuit for Logical Sum of Minor Failure Signals

6.3.14. CELL Module Input Data Error Signal (From CELL Module to DAT/ST Module)

(1) The CELL module shall have the interface to send the following signals to middle plane interface.

A) Signal Name [a,c]

B) Number of Output
C) Output Method
D) Logic Level

(2) The DAT/ST module shall have the interface to receive the above signals from middle plane interface.

6.3.15. OPRM Automatic Bypass Signal (From CELL module to DIO module)

(1) The CELL module shall have the interface to send the following signals to middle plane interface.

A) Signal Name [a,c]
B) Number of Output
C) Output Method
D) Logic Level

(2) The DIO module shall have the interface to receive the above signals from middle plane interface.

6.3.16. APRM Unit Data Select Signal (From CELL module to DAT/ST module)

(1) The CELL module shall have the interface to send the following signals to middle plane interface.

A) Signal Name [a,c]
B) Number of Output
C) Output Method
D) Logic Level

(2) The DAT/ST module shall have the interface to receive the above signals from middle plane interface.

(3) The CELL module shall generate APRM Unit Data1 Select signal at the following conditions.

- APRM Unit Data1 and APRM Unit Data2 are normal.
- APRM Unit Data1 and APRM Unit Data2 are abnormal.
- APRM Unit Data2 is abnormal.

The CELL module shall generate APRM Unit Data2 Select signal at the following conditions.

- APRM Unit Data1 is abnormal.

6.3.17. OPRM Trip Signal (From [ ]a,c of AGRD and PBD Modules to DAT/ST Module)

(1) The AGRD and PBD module shall have the interface to send the following signals to middle plane interface.
- A) Signal Name
- B) Number of Output
- C) Output Method
- D) Logic Level

[ ]a,c

(2) The middle plane shall connect two Trip signals from the AGRD and PBD module by [ ]a,c described in Figure 6-28.

(3) The DAT/ST and DIO module shall have the interface to receive the following signals from middle plane interface.
- A) Signal Name
- B) Number of Input
- C) Input Method
- D) Logic Level

[ ]a,c

(4) The CELL module shall have the interface to the [ ]a,c on the middle plane. The CELL module printed circuit board pattern shall make a short circuit.

[ ]a,c

Figure 6-28 I/F Circuit for Logical Sum of Trip Signal

6.3.18. ABA Trip Signal (From AGRD Module to DIO Module)

(1) The AGRD module shall have the interface to send the following signals to middle plane interface.
- A) Signal Name
- B) Number of Output
- C) Output Method
- D) Logic Level

[ ]a,c

(2) The DIO module shall have the interface to receive the above signals from middle plane interface.

6.3.19. GRA Trip Signal (From AGRD Module to DIO Module)

(1) The AGRD module shall have the interface to send the following signals to middle plane interface.

A) Signal Name
B) Number of Output
C) Output Method
D) Logic Level

[ ]a,c

(2) The DIO module shall have the interface to receive the above signals from middle plane interface.

6.3.20. PBDA Trip Signal (From PBD Module to DIO Module)

(1) The PBD module shall have the interface to send the following signals to middle plane interface.

A) Signal Name
B) Number of Output
C) Output Method
D) Logic Level

[ ]a,c

(2) The DIO module shall have the interface to receive the above signals from middle plane interface.

6.3.21. Trip Judgment Status(ABA) Signal (From AGRD Module to DIO Module)

(1) The AGRD module shall have the interface to send the following signals to middle plane interface.

A) Signal Name
B) Number of Output
C) Output Method
D) Logic Level

[ ]a,c

(2) The DIO module shall have the interface to receive the above signals from middle plane interface.

6.3.22. Trip Judgment Status(GRA) Signal (From AGRD Module to DIO Module)

(1) The AGRD module shall have the interface to send the following signals to middle plane interface.

A) Signal Name
B) Number of Output
C) Output Method
D) Logic Level

[ ]a,c

(2) The DIO module shall have the interface to receive the above signals from middle plane interface.

6.3.23. Trip Judgment Status(PBDA) Signal (From PBD Module to DIO Module)

(1) The PBD module shall have the interface to send the following signals to middle plane interface.

A) Signal Name
B) Number of Output
C) Output Method
D) Logic Level

[ ]a,c

(2) The DIO module shall have the interface to receive the above signals from middle plane interface.

6.3.24. Power Supply Error Monitoring Signal (From LVPS Module to DAT/ST Module)

(1) Each LVPS modules shall have the interface to send the following signals to middle plane interface.

A) Signal Name
B) Number of Output
C) Output Method
D) Logic Level

[ ]a,c

(2) The DAT/ST module shall have the interface to receive the above signals from middle plane interface.

6.4. Middle Plane Interface

(1) The middle plane pin assignment of the CELL module shall be designed as follows.

Table 6-1 Middle Plane Connector Pin Assignment of CELL Module

Pin	c-row Signal Name	b-row Signal Name	a-row Signal Name
1	[redacted]	[redacted]	[redacted] a,c
2			
3			
4			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			

(2) The middle plane pin assignment of the AGRD module shall be designed as follows.

Table 6-2 Middle Plane Connector Pin Assignment of AGRD Module

Pin	c-row Signal Name	b-row Signal Name	a-row Signal Name
1	[redacted]	[redacted]	[redacted] a,c
2			
3			
4			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			

(3) The middle plane pin assignment of the PBD module shall be designed as follows.

Table 6-3 Middle Plane Connector Pin Assignment of PBD Module

Pin	c-row Signal Name	b-row Signal Name	a-row Signal Name
1	[		] a,c
2			
3			
4			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32	]		

(4) The middle plane pin assignment of the DAT/ST module shall be designed as follows.

Table 6-4 Middle Plane Connector Pin Assignment of DAT/ST Module

Pin	c-row Signal Name	b-row Signal Name	a-row Signal Name
1	[redacted]	[redacted]	[redacted] a,c
2			
3			
4			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			

(5) The middle plane pin assignment of the DIO module shall be designed as follows.

Table 6-5 Middle Plane Connector Pin Assignment of DIO Module

Pin	c-row Signal Name	b-row Signal Name	a-row Signal Name
1	[redacted]	[redacted]	[redacted] a,c
2			
3			
4			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			

(6) The middle plane pin assignment of the TRN module shall be designed as follows.

Table 6-6-1 Middle Plane Connector Pin Assignment of TRN Module (1)

Pin	c-row Signal Name	b-row Signal Name	a-row Signal Name
1	[redacted]	[redacted]	[redacted] a,c
2			
3			
4			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			

Table 6-6-2 Middle Plane Connector Pin Assignment of TRN Module (2)

Pin	c-row Signal Name	b-row Signal Name	a-row Signal Name
1	[redacted]	[redacted]	[redacted] a,c
2			
3			
4			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			

(7) The middle plane pin assignment of the RCV module shall be designed as follows.

Table 6-7-1 Middle Plane Connector Pin Assignment of RCV Module (1)

Pin	c-row Signal Name	b-row Signal Name	a-row Signal Name
1	[redacted]		
2			
3			
4			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			

a,c

Table 6-7-2 Middle Plane Connector Pin Assignment of RCV Module (2)

Pin	c-row Signal Name	b-row Signal Name	a-row Signal Name
1	[redacted]		
2			
3			
4			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17			
18			
19			
20			
21			
22			
23			
24			
25			
26			
27			
28			
29			
30			
31			
32			

a,c

(8) The middle plane pin assignment of the LVPS module shall be designed as follows.

Table 6-8-1 DC Input Connector Pin Assignment of LVPS Module

Pin	Name	Remarks
A	[	a,c
B		
C		
D	]	

Table 6-8-2 Middle Plane Connector Pin Assignment of LVPS Module

Pin	Name	Remarks
z4	[	a,c
d6		
z8		
d10		
z12		
d14		
z16		
d18		
z20		
d22		
z24		
d26		
z28		
d30		
z32	]	

7. Performance

7.1. Response Time

The OPRM trip response time of the OPRM unit from when the core oscillation initiation detected by LPRM detector is input to the OPRM unit to when the OPRM trip function initiation from the OPRM unit shall not exceed [ ]a,c ms based on the condition specified in Section 5.1.4-6 B) of EDS (Reference 2.2 (1)).

In EDS, it is recommended that a processing cycle be less than or equal to [ ]a,c ms. Thus OPRM-specific signal processing is conducted and signals processing cycles for the CELL, AGRD, PBD and DAT/ST modules are determined to be [ ]a,c ms.

7.2. Input and Output Characteristics

Not required.

7.3. Power Supply Fluctuation Effect Requirements

(1) Power voltage-resistant fluctuation

The OPRM unit shall satisfy the following performances when AC input power voltage to PFC is fluctuated under the following condition.

Power voltage range: 90 to 150VAC

Power frequency: 60Hz

A) Trip output

Trip signal shall be normal output.

False trips shall not occur.

B) Display and key operation

Display and key operation shall work normally.

C) DC power voltage measurement

Output voltage from LVPS module shall be within following ranges.

Secondary voltage +5 V: +4.75 V to +5.25 V

+15 V: +14.25 V to +15.75 V

-15 V: -14.25 V to -15.75 V

(2) Frequency-resistant fluctuation

The OPRM unit shall satisfy the following performances when AC input power frequency to PFC is fluctuated under the following condition.

Power voltage range: 120VAC

Power frequency: 57 to 63Hz

A) Trip output

Trip signal shall be normal output.

False trips shall not occur.

(3) Instantaneous Power Failure

OPRM unit shall withstand instantaneous power failure for more than [ ]a,c msec. During Hold up time for AC supplied power sources ([ ]a,c msec), digital I/Os shall not change and the change of analog I/Os shall be within 5% of full scale in accordance with EPRI TR-107330 Section 4.6.1 (Reference 2.1(8)).

The value, however, is a value obtained when a parallel operation of two identical power sources is performed at rated load.

(4) Recovery from Power Failure

The OPRM unit shall start up normally after its power is turned on and off for [ ]a,c seconds continuously.

(5) Operation with one power supply module

Failure of one of the redundant power supplies shall not cause the discrete I/O to change state for more than [ ]a,c milliseconds.

Application logic shall continue to operate even during the failure of redundant power supply.

Redundant power supply shall be protected so that undervoltage and overvoltage, shorts to ground.

And other faults in one power supply do not prevent operation of the alternate supply.

7.4. Availability and Reliability Requirements

The availability of the OPRM unit shall be more than 99%. This availability has been calculated on the assumption that the failed module can be replaced with a permanently-installed spare part.

(1) "Mean Time To Repair (MTTR)" shall be within [ ]a,c.
(2) "Mean Time Between Failures (MTBF)" shall be calculated and evaluated for each module design.
(3) "Failure Mode Effect Analysis (FMEA)" shall be performed for each module design.

7.5. Design Life

The design life of OPRM unit is [ ]a,c years based on sound engineering practices and manufacturer's recommendations using known significant aging mechanisms and reliability data.
As for the design life of modules in OPRM unit that are less than [ ]a,c years, appropriate maintenance and replacement shall be provided in accordance with instruction manual.

7.6. Data Retention Capability Requirements

Field modifiable constants shall be stored in EEPROM which shall be capable of at least 100,000 write cycles. EEPROM is electrically erasable PROM.

8. Initializing Processes

(1) Modules that include the FPGAs (CELL, AGRD, PBD, DAT/ST, TRN and RCV module) shall have the power on reset function to initialize the signal processing when the DC power is supplied.
(2) Modules that include the FPGAs (CELL, AGRD, PBD, DAT/ST, TRN and RCV module) shall have the power on reset function to initialize the signal processing when the module +5VDC power supply recovers after the module detect the low voltage of +5VDC power supply.
(3) OPRM unit shall generate all trip and alarm signals when initializing.
(4) Initializing of signal processing is described in Section 5.2. Initializing of normalized oscillation signal calculation function is described in Section 5.2.1. Initializing of Amplitude Based Detection Algorithm and Growth Rate-Based Detection Algorithm are described in Section 5.2.2. Initializing of Period Based Detection Algorithm is described in Section 5.2.3.
(5) When the power to OPRM unit is turned off, the OPRM unit stops operation and all trip and alarm signals of discrete output turn on.

9. Self-Diagnosis Function

The OPRM unit shall have following self-diagnosis functions to detect failure.

(1) Unit Power Supply Voltage Monitor

The OPRM unit monitors the output voltage of the LVPS module. When the OPRM unit detects the error, the OPRM unit displays an error on the alarm display of the DAT/ST module and generates the trip alarm. This function is described in Sections 5.2.4 and 5.2.8.

OPRM unit generates OPRM inoperative signal when both power supply is halt.

(2) Power Supply Voltage Monitor of Each Module

This function is included in Section 8 (2).

(3) FPGA Operation Monitor using Watchdog Timer

A) The modules which include the FPGAs (CELL, AGRD, PBD, DAT/ST, TRN, and RCV modules) shall monitor the FPGA operations for [ ]a,c using the watchdog timer function.

B) The CELL module, AGRD module and PBD modules shall generate the OPRM Inoperative signal when the watchdog timer function detects [ ]a,c.

C) The DAT/ST module shall generate the OPRM Minor Failure signal when the watchdog timer function detects [ ]a,c.

D) The CELL, AGRD and PBD modules generate OPRM Minor Failure signal when the watchdog timer function detects [ ]a,c.

E) The RCV module shall generate [ ]a,c or [ ]a,c when the watchdog timer function detects the halts of [ ]a,c.

F) The TRN module shall indicate the occurrence of [ ]a,c on the LED indicator when the watchdog timer function detects [ ]a,c.

G) The watchdog timer of each module shall monitor [ ]a,c.

H) The watchdog timer of each module shall not be included in [ ]a,c.

I) The watchdog timer of each module shall be independent from the clock signal used [ ]a,c.

J) The watchdog timer shall monitor [ ]a,c.

(4) Data Transmission Monitors

A) OPRM unit shall generate the alarm signal at following condition, when "timeout error" or "[ ]a,c" occur continuously [ ]a,c.

B) The RCV module shall monitor the input timeout for cyclically transmitted data from the LPRM unit and the APRM unit.

C) The RCV module shall monitor [ ]a,c inside the data from the APRM unit and LPRM unit.

D) The CELL module shall generate the OPRM Minor Failure signal when the input timeout error or [ ]a,c is detected in RCV module.

E) The CELL, AGRD, PBD and DAT/ST modules shall monitor the input time-out for cyclically transmitted data from other modules.

F) The CELL, AGRD, PBD and DAT/ST modules shall monitor [ ]a,c inside the data from other modules.

G) The AGRD and PBD module shall generate the OPRM Inoperative signal when the input timeout error or [ ]a,c is detected. CELL module shall generate the OPRM Inoperative signal when the input time out error or [ ]a,c of both APRM data is detected.

H) The DAT/ST modules shall generate the OPRM Minor Failure signal when the input timeout error or [ ]a,c is detected. CELL module shall generate the OPRM Minor Failure signal when the input time out error or [ ]a,c of LPRM Unit Data or APRM Unit Data.

I) OPRM unit shall generate the alarm signal when [ ]a,c is detected.

J) The OPRM unit shall use the following [ ]a,c.

[ ]a,c

K) OPRM unit should have a [ ]a,c test function which checks the [ ]a,c function at module level testing.

(5) Memory Check

A) The CELL, AGRD and PBD modules shall detect [ ]a,c.

B) The CELL, AGRD and PBD modules shall generate OPRM Minor Failure signal in the case of [

C) The CELL, AGRD and PBD modules shall generate OPRM Inoperative signal in the case of [ ]a,c [ ]a,c

D) If a constant is saved in a field modifiable memory, the constant shall be protected by [ ]a,c

(6) Calculation Monitoring

A) CELL module shall generate [ ]a,c data.

B) CELL module shall generate OPRM Inoperative signal when the result of [ ]a,c data became abnormal.

10. Environmental Requirements

10.1. Temperature and Humidity

The OPRM unit shall meet environmental conditions shown in Table10-1.

Table 10-1 Environmental Conditions Requirements

	Normal Environmental Conditions	Abnormal Environmental Conditions
Temperature Range	Min 16ºC(60ºF), Max 40ºC(104ºF)	Min 4ºC(40ºF), Max 50ºC(120ºF)
Humidity Range	Min 40%, Max 95%*	Min 10%, Max 95%*

*: non condensing

10.2. Radiation

The OPRM unit shall meet radiation exposure level as shown in Table 10-2.

Table 10-2 Radiation Exposure level

	Normal Environmental Conditions	Abnormal Environmental Conditions
Radiation Exposure	10^3RADS	10^3RADS

10.3. Seismic

The OPRM unit shall be designed to be suitable for qualification as a Category 1 Seismic device as described in Section 5.5.2 of Equipment Design Specification (Reference 2.2 (1)).

10.4.Electromagnetic Compatibility

The OPRM unit shall be designed to withstand the requirements of EDS Sections 5.5.3 to 5.5.6. There are no special requirements only for the OPRM unit.

10.5.Isolation Requirements

External interface of the OPRM unit shall be isolated by optical components.

10.6.Fire Resistance

The OPRM unit shall use flame-retardant material in order to minimize the probability of fire and subsequent consequences.

Power supply: Board [ ]a,c
Input Wire [ ]a,c
Output Wire [ ]a,c
Board: [ ]a,c
Cable: See Table 4-1

10.7.Power Supply

The OPRM unit including PFC shall be designed to receive four divisional class 1E 120VAC vital powers and four divisional class 1E 120 VAC instrument and control powers as redundant power supplies.
OPRM unit shall be designed to operate by the vital power described in Section 5.2.8.
The requirements for PFC are shown in Section 5.2.8.

11. Parts List (Including purchases)

The following items are required for unit configuration. (Not including module connectors)
Other items should be used, as applicable.

Table.11-1 Components of OPRM Unit

Item	Type	Number of Pieces	Supplier	Use Application
OPRM Unit	[a,c	1	NICSD	The assembly of modules and chassis.
CELL module		1	Power Platform Development Department (PPDD)	Refer to table 4.2
AGRD module		1	PPDD	Refer to table 4.2
PBD module		1	PPDD	Refer to table 4.2
DAT/ST module		1	PPDD	Refer to table 4.2
LVPS module		2	PPDD	Refer to table 4.2
TRN module		2	PPDD	Refer to table 4.2
RCV module		2	PPDD	Refer to table 4.2
DIO module		1	PPDD	Refer to table 4.2
PFC		2	Bellnix	Input line filter for LVPS
Chassis for OPRM unit	]	1	Schroff	For module storage (Including middle plane)

The CELL module, AGRD module, PBD module, DAT/ST module, TRN module and RCV module shall use either one or both of the following FPGAs.

Table.11-2 FPGA Types

FPGA Type	Supplier	Remarks
[		] a,c