REVISED RESPONSE TO REQUEST FOR ADDITIONAL INFORMATION

APR1400 Design Certification

Korea Electric Power Corporation / Korea Hydro & Nuclear Power Co., LTD

Docket No. 52-046

RAI No.:	**295-8263**
SRP Section:	**16 – Technical Specifications**
Application Section:	**16.3.3**
Date of RAI Issue:	**11/05/2015**

Question No. 16-122

The “Surveillance Requirements” section of the Bases for generic TS Section 3.3 needs the following suggested clarifications to be useable. The applicant is requested to consider incorporating the suggested changes, as indicated; please explain and correct any errors in the suggested changes:

1. In the “Surveillance Requirements” section of the Bases for generic TS 3.3.1, 3.3.4, 3.3.4 and 3.3.6, revise first paragraph so the meaning is clear:

(TS 3.3.1 SR Bases) The OPERABILITY of **the** interface and test processor (ITP) is not ~~limited per~~ **required by** LCO 3.3.1 because **the RPS does not need the** ITP ~~does not~~ **to** perform the safety function of RPS. However, **the** ITP shall **be** maintain**ed** ~~the functional integrity to perform~~ **capable of supporting performance of the** CHANNEL FUNCTIONAL TEST of SRs 3.3.1.7, 3.3.1.10, and 3.3.1.12.

(TS 3.3.4 SR Bases) The OPERABILITY of the ~~ITP~~ **interface and test processor (ITP)** is not ~~limited per~~ **required by** LCO 3.3.4 because **the RPS does not need the** ITP ~~does not~~ **to** perform the safety function of RPS. However, the ITP shall **be** maintain**ed** ~~the functional integrity to perform~~ **capable of supporting performance of the** CHANNEL FUNCTIONAL TEST of SR**s** 3.3.4.1 and 3.3.4.2.

(TS 3.3.5 SR Bases) Since the ~~ITP~~ **interface and test processor (ITP) is not needed to** ~~does not~~ perform **any ESFAS** safety ~~related~~ function ~~for ESFAS~~, **the** OPERABILITY **of the ITP is not required by** ~~per~~ LCO 3.3.5 ~~is not required~~. However, the ITP shall **be** maintain**ed**

~~the functional integrity for~~ **capable of supporting performance of** the CHANNEL FUNCTIONAL TEST ~~in~~ **of** SRs 3.3.5.2, 3.3.5.3, and 3.3.5.5.

(TS 3.3.6 SR bases) Since the ~~ITP~~ **interface and test processor (ITP) is not needed to** ~~does not~~ perform ~~the~~ **any ESFAS** safety ~~related~~ function~~s of ESFAS~~, the OPERABILITY **of the ITP** is not **required** ~~limited~~ by LCO 3.3.6. **However, the** ~~But,~~ ITP ~~must~~ **shall be** maintain**ed** ~~the functional integrity for operation~~ **capable of supporting performance** of **the** CHANNEL FUNCTIONAL TEST **of SR 3.3.6.1**.

In the above paragraphs, which do not exist in the STS, recommend changing the word "shall" to "must" in the second sentence, since using "shall" is not customary in the Bases.

2. Under the heading "SR 3.3.5.2" in the "Surveillance Requirements" section of the Bases for generic TS 3.3.5, are five paragraphs taken from STS Bases for SR 3.3.5.2, with design- difference related changes. The resulting paragraphs need clarification, such as the suggested changes indicated in the following markup (existing text as proposed is colored black; proposed text identical to STS text is colored green; added text is blue; and proposed text being removed is lined out and colored ~~red~~):

(1st paragraph) A CHANNEL FUNCTIONAL TEST on each channel is performed ~~every 31 days~~ to ensure the entire channel will perform its intended function when needed. The OPERABILITY of each ESFAS instrumentation channel is verified on a 31 day interval with applicable extensions. This Frequency is based on operating experience which shows that ESFAS instrument channels usually pass the CHANNEL FUNCTIONAL TEST when performed on a 31 day Frequency. ~~This test is part of an overlapping test sequence similar to that employed in the RPS.~~

(2nd paragraph) This test is part of an overlapping test sequence similar to that employed in the RPS. This sequence consists of SR~~s~~ 3.3.5.2, SR 3.3.6.1, and SR 3.3.6.2 and tests the entire ESFAS from sensor input to the bistable logic processor ~~input to actuational~~ through the automatic ESF actuation logic (actuational) output of each subgroup. These overlapping tests are described in ~~DCD Tier 2~~ FSAR Section 7.3 (Reference 1).

(3rd paragraph) SR~~s~~ 3.3.5.2 and SR 3.3.6.1 are performed together and in conjunction with ESFAS testing. SR 3.3.6.2 verifies that each subgroup can actuate ESF~~AS~~ equipment when actuational output of each subgroup is generated.

(4th paragraph) These tests verify that the ESFAS is capable of performing its intended function, from sensor input to the bistable logic processor ~~input~~ through the actuational output of each subgroup to the actuated ESF components. SR~~s~~ 3.3.6.1 and SR 3.3.6.2 are described in LCO 3.3.6. SR 3.3.5.2 includes bistable logic processor testing.

(5th paragraph) To assure that the actual trip ~~occurrence by~~ setting in the bistable logic processor is ~~within~~ conservative with respect to the Allowable Value ~~of setpoint~~, a test signal is superimposed on the input in one channel at a time to verify that the bistable *processor* trips within the specified *as-found setting* tolerance around the ~~setpoint~~ *previous as-left setting*[HC1] ~~infected in only one channel at a time~~. This is performed ~~in bypassed status of~~ with the corresponding RPS trip channel placed in trip channel bypass. Setpoint adjustment must be performed ~~consistent with the plant specific setpoint analysis~~ as specified in the Setpoint Control Program.

3. Under the heading “SR 3.3.6.1” in the “Surveillance Requirements” section of the Bases for generic TS 3.3.6, are three paragraphs taken from STS Bases for SR 3.3.6.1, with design- difference related changes. The resulting paragraphs need clarification, such as the suggested changes indicated in the following markup (existing text as proposed is colored black; proposed text identical to STS text is colored green; added text is blue; and proposed text being removed is lined out and colored ~~red~~):

(1st paragraph) A CHANNEL FUNCTIONAL TEST is performed ~~every 31 days~~ to ensure the entire channel will perform its intended function when needed. The ~~operability~~ OPERABILITY of ~~the each channel or automatic actuation logic channel~~ each ESFAS Logic channel, ESFAS Manual Trip channel, and Diverse Manual ESF Actuation channel is verified by the operator every 31 days at least to meet ~~the surveillance requirement~~ on a 31 day interval with applicable extensions. This Frequency is based on operating experience which shows that automatic ESF actuation logic channels, ESF manual trip channels, and diverse manual ESF actuation channels usually pass the CHANNEL FUNCTIONAL TEST when performed on a 31 day Frequency.

(2nd paragraph) The CHANNEL FUNCTIONAL TEST is part of an overlapping test sequence similar to that employed in the RPS. This sequence, consisting of SR~~s~~ 3.3.5.2, SR 3.3.6.1, and SR 3.3.6.2 tests the entire ESFAS from sensor input to the bistable logic processor ~~input~~ through the automatic ESF actuation logic (actuational) output of each ~~the actuation of the individual~~ subgroup. These overlapping tests are described in Reference

1. SR~~s~~ 3.3.5.2 and SR 3.3.6.1 are normally performed together and in conjunction with ESFAS testing. When the actuational output signal ~~of each~~ for a subgroup is generated, SR 3.3.6.2 verifies that the ~~actuation ability of~~ ESF components associated ~~actuation signal of the associated~~ with ~~each~~ the subgroup are capable of being actuated by the ESF-CCS.

(3rd paragraph) These tests verify that the ESFAS is capable of performing its intended function, from sensor input to the bistable logic processor ~~input~~ through the actuated components. SR 3.3.5.2 is addressed in LCO 3.3.5. SR 3.3.6.1 includes LCL testing, initiation logic (trip path) testing, and actuation logic testing.

(4th paragraph) Local Coincidence Logic Testing

LCL testing ~~is tested to verify~~ verifies the ~~operability~~ OPERABILITY of the two-out-of-four coincidence logic and trip channel bypass logic.

(5th paragraph) Initiation Logic (Trip Path) Testing

Testing of initiation logic, ~~Initiation logic testing is for Initiation Logic~~ which consists of logical "OR" (selective 2-out-of-4 logic), ~~and~~ is performed after the completion of LCL testing. This testing ~~implements the~~ exercises only one ~~Initiation~~ initiation logic ~~of one~~ channel at a time, which affects only one trip path.

(6th paragraph) Actuation Logic Testing

Actuation logic testing ~~is tested to verify~~ verifies the ~~operability~~ OPERABILITY of the two-out-of-four actuation logic after the completion of initiation logic (trip path) testing. *This test is performed only for one channel and one actuation logic by periodic automatic test.*

a. The applicant is requested to explain and clarify the last sentence of the 6th paragraph.

b. The applicant is requested to explain why the LCL, initiation logic, and actuation logic tests are described in the above Bases discussions as being performed sequentially, without any discussion of overlap.

c. Overall, the Bases descriptions of the ESFAS Actuation Logic are unclear, in large measure to there being no definitive statement of the correspondence to the various parts of an ESFAS Function instrumentation loop, and the various ESFAS instrument and logic functions, and what defines a channel (or division) in an ESFAS instrument

function, and in each type of ESFAS logic function. The applicant is requested to review the following correspondence list and correct errors; also provide a concise description of the correspondences between the items in the list.

Sensor and APC- S.....
LCO
3.3.5

Bistable Logic Processor in the PPS
..... LCO 3.3.5

ESF-CCS Group Controller and local coincidence logic
(LCL)..... LCO 3.3.6

ESF-CCS Local Controller (LC) and initiation logic (selective 2/4) (trip path)....
LCO 3.3.6

ESF-CCS Component control logic and actuation logic, subgroups
..... LCO 3.3.6

Component Interface Module (CIM) ..... LCO on associated component

d. The applicant is requested to list all component groups, subgroups, which ESF-CCS ESFAS Actuation Logic Division is associated with the components in each subgroup, and which subgroups cannot be tested during power operation of the unit, and “must be tested in accordance with the Note to [SR 3.3.6.2].”

e. The applicant is requested to clarify the meaning of the Bases for the Frequency of SR 3.3.6.2, which says

> The 31-day Frequency on a staggered test basis complies with the operating experience and ensures the problems of individual logic signal can be detected within this time frame.

f. Because Table 3.3.6-1 does not list applicable SRs for each ESFAS Logic Function, ESFAS Manual Trip Function, and diverse Manual ESF actuation function, and no Note is provided in the SRs about the applicability of each SR to each Function, it is ambiguous whether SR 3.3.6.1 and SR 3.3.6.2 apply to Function 7. The applicant is requested to clarify this by making appropriate changes to generic TS 3.3.6.

[HC1]This text is from STS Rev 4 page B 3.3.5B-26

Response – (Rev. 1)

1. The first paragraph in the “Surveillance Requirements” section of the Bases for generic TS 3.3.1, 3.3.4, 3.3.4 and 3.3.6 will be revised as follows:

(TS 3.3.1 SR Bases) The OPERABILITY of the interface and test processor (ITP) is not required by LCO 3.3.1 because the RPS does not need the ITP to perform the safety function of RPS. However, the ITP must be maintained capable of supporting performance of the CHANNEL FUNCTIONAL TEST of SRs 3.3.1.7, 3.3.1.10, and 3.3.1.12.

(TS 3.3.4 SR Bases) The OPERABILITY of the interface and test processor (ITP) is not required by LCO 3.3.4 because the RPS does not need the ITP to perform the safety function of RPS. However, the ITP must be maintained capable of supporting performance of the CHANNEL FUNCTIONAL TEST of SRs 3.3.4.1 and 3.3.4.2.

(TS 3.3.5 SR Bases) Since the interface and test processor (ITP) is not needed to perform any ESFAS safety function, the OPERABILITY of the ITP is not required by LCO 3.3.5. However, the ITP must be maintained capable of supporting performance of the CHANNEL FUNCTIONAL TEST of SRs 3.3.5.2, 3.3.5.3, and 3.3.5.5.

(TS 3.3.6 SR bases) Since the interface and test processor (ITP) is not needed to perform any ESFAS safety function, the OPERABILITY of the ITP is not required by LCO 3.3.6. However, the ITP must be maintained capable of supporting performance of the CHANNEL FUNCTIONAL TEST of SR 3.3.6.1.

2. The five paragraphs under the heading “SR 3.3.5.2” in the “Surveillance Requirements” section of the Bases for generic TS 3.3.5 will be revised as follows:

(1st paragraph) A CHANNEL FUNCTIONAL TEST on each channel is performed to ensure the entire channel will perform its intended function when needed. The OPERABILITY of each ESFAS instrumentation channel is verified on a 31 day interval with applicable extensions. This Frequency is based on operating experience which shows that ESFAS instrument channels usually pass the CHANNEL FUNCTIONAL TEST when performed on a 31 day Frequency.

(2nd paragraph) This test is part of an overlapping test sequence similar to that employed in the RPS. This sequence consists of SR 3.3.5.2, SR 3.3.6.1, and SR 3.3.6.2 and tests the entire ESFAS from sensor input to the bistable logic processor through the automatic ESF actuation logic (actuational) output of each subgroup. These overlapping tests are described in FSAR Section 7.3 (Reference 1).

(3rd paragraph) SR 3.3.5.2 and SR 3.3.6.1 are performed together and in conjunction with ESFAS testing. SR 3.3.6.2 verifies that each

subgroup can actuate ESF equipment when actuational output of each subgroup is generated.

(4th paragraph) These tests verify that the ESFAS is capable of performing its intended function, from sensor input to the bistable logic processor through the actuational output of each subgroup to the actuated ESF components. SR 3.3.6.1 and SR 3.3.6.2 are described in LCO 3.3.6. SR 3.3.5.2 includes bistable logic processor testing.

(5th paragraph) To assure that the actual trip setting in the bistable logic processor is conservative with respect to the Allowable Value, a test signal is superimposed on the input in one channel at a time to verify that the bistable *processor* trips within the specified *as-found setting* tolerance around the *previous as-left setting*. This is performed with the corresponding RPS trip channel placed in trip channel bypass. Setpoint adjustment must be performed as specified in the Setpoint Control Program.

3. a Including clarifying the last sentence in the 6th paragraph on Actuation logic testing, the six paragraphs under the heading “SR 3.3.6.21” in the “Surveillance Requirements” section of the Bases for generic TS 3.3.6 will be revised as follows:

(1st paragraph) A CHANNEL FUNCTIONAL TEST is performed to ensure the entire channel will perform its intended function when needed. The OPERABILITY of each ESFAS Logic channel and ESFAS Manual Trip channel is verified on a 31 day interval with applicable extensions. This Frequency is based on operating experience which shows that automatic ESF actuation logic channels and ESF manual trip channels usually pass the CHANNEL FUNCTIONAL TEST when performed on a 31 day Frequency.

(2nd paragraph) The CHANNEL FUNCTIONAL TEST is part of an overlapping test sequence similar to that employed in the RPS. This sequence, consisting of SR 3.3.5.2, SR 3.3.6.1, and SR 3.3.6.2 tests the entire ESFAS from sensor input to the bistable logic processor through the automatic ESF actuation logic (actuational) output of each subgroup. These overlapping tests are described in Reference 1. SR 3.3.5.2 and SR 3.3.6.1 are normally performed together and in conjunction with ESFAS testing. When the actuational output signal for a subgroup is generated, SR 3.3.6.2 verifies that the ESF components associated with the subgroup are capable of being actuated by the ESF-CCS.

(3rd paragraph) These tests verify that the ESFAS is capable of performing its intended function, from sensor input to the bistable logic processor through the actuated components. SR 3.3.5.2 is

addressed in LCO 3.3.5. SR 3.3.6.1 includes LCL testing, initiation logic (trip path) testing, and actuation logic testing.

(4th paragraph) Local Coincidence Logic Testing

LCL testing verifies the OPERABILITY of the two-out-of-four coincidence logic and trip channel bypass logic.

(5th paragraph) Initiation Logic (Trip Path) Testing

Testing of initiation logic, which consists of logical "OR", is performed after the completion of LCL testing. This testing exercises only one initiation logic channel at a time, which affects only one trip path.

(6th paragraph) Actuation Logic Testing

Actuation logic testing verifies the OPERABILITY of the selective two-out-of-four actuation logic after the completion of initiation logic (trip path) testing. This test is performed only for one channel and one actuation logic at a time by periodic automatic test.

3. b The following sentences stated in SR 3.3.6.1 indicate that the CHANNEL FUNTIONAL TEST is performed using overlapping tests.

"The CHANNEL FUNCTIONAL TEST is part of an overlapping test sequence similar to that employed in the RPS. This sequence, consisting of SR 3.3.5.2, SR 3.3.6.1, and SR 3.3.6.2 tests the entire ESFAS from the bistable logic processor through the automatic ESF actuation logic (actuational) output of each subgroup. These overlapping tests are described in Reference 1."

3. c LCO 3.3.5 covers the sensor, the APC-S, and the Bistable logic processor in the PPS. LCO 3.3.6 covers the PPS local coincidence logic (LCL), the PPS initiation logic ("OR" logic), the ESF-CCS Group Controller (GC), the ESF-CCS Loop Controller (LC), and the Component Interface Module (CIM). The initiation logic following the LCL in the PPS is not a selective 2/4 logic, but a logical "OR" and its output signal is transmitted to the ESF-CCS GC.

3. d A list of all components in the ESF-CCS ESFAS Actuation Logic Division Functions for the groups and subgroups is attached.

3. e The subgroup of Actuation Logic channels A and C are tested during the interval of the 31-day Frequency and then the remaining channels B and D are tested during the next interval of 31-day Frequency. Therefore, all channels are tested during the 62-day Frequency interval.

Following description about the note will be inserted to Bases for SR 3.3.6.2.

In accordance with Note 2 to this SR, the pair of Actuation logic subgroup channels A and C are tested during the first interval of the staggered 31 day Frequency and the pair of Actuation Logic subgroup channels B and D are tested during the second interval of staggered 31 day Frequency. Therefore, each pair of Actuation Logic subgroup channels is tested during an interval of 62 days, plus applicable extensions.

The note for SR 3.3.6.2 will be revised as follows.

2. The pair of Actuation Logic subgroup channels A and C and the pair of Actuation Logic subgroup channels B and D.

3. f The CHANNEL FUNCTIONAL TEST for the Function 7 “Diverse Manual ESF Actuation Signal” is separately performed by the SR 3.3.6.3.

The prior revisions of the RAI response were incorporated into Rev. 1 of the DCD and TS; therefore this revision starts with and only contains mark-ups to Revision 1 of the DCD and TS.

Impact on DCD

Same as changes described in the impact on Technical Specifications section.

Impact on PRA

There is no impact on the PRA.

Impact on Technical Specifications

Technical Specification 3.3.6 and Bases TS 3.3.6 will be revised as indicated in the Attachment.

Impact on Technical/Topical/Environmental Reports

There is no impact on any Technical, Topical or Environmental Report.

SURVEILLANCE REQUIREMENTS

	SURVEILLANCE	FREQUENCY
SR 3.3.6.1	NOTE Testing of Actuation Logic shall include the verification of proper operation of each actuation circuit.	
	Perform CHANNEL FUNCTIONAL TEST on each ESFAS logic channel and Manual ESF Actuation channel.	31 days
SR 3.3.6.2	NOTES 1. Components exempt from testing during operation shall be tested once every 18 months (MODE 6) or in MODE 5 if not tested within the previous 62 days. 2. ~~Subgroup of Actuation Logic channel A, C and B, D shall be tested on a staggered basis.~~	The pair of Actuation Logic subgroup channels A and C and the pair of Actuation Logic subgroup channels B and D
	Perform a verification of the OPERABILITY of subgroup for Actuation signal of each Actuation Logic channel	31 days on a STAGGERED TEST BASIS
SR 3.3.6.3	Perform CHANNEL FUNCTIONAL TEST on each Diverse Manual ESF Actuation channel	18 months

BASES

SURVEILLANCE REQUIREMENTS

Since the interface and test processor (ITP) is not needed to perform any ESFAS safety function, the OPERABILITY of the ITP is not required by LCO 3.3.6. However, the ITP must be maintained capable of supporting performance of the CHANNEL FUNCTIONAL TEST of SR 3.3.6.1.

SR 3.3.6.1

The OPERABILITY of each

and

Q16-122.3a

Q16-122.3f

A CHANNEL FUNCTIONAL TEST is performed to ensure the entire channel will perform its intended function when needed. ~~Each~~ ESFAS Logic channel~~,~~ ESFAS Manual Trip channel~~, and Diverse Manual ESF Actuation channel~~ is verified ~~by the operator every 31 days at least to meet~~ on a 31 day interval with applicable extensions. This Frequency is based on operating experience which shows that automatic ESF actuation logic channels~~,~~ ESF manual trip channels~~, and diverse manual ESF actuation channels~~ usually pass the CHANNEL FUNCTIONAL TEST when performed on a 31 day Frequency.

and

The CHANNEL FUNCTIONAL TEST is part of an overlapping test sequence similar to that employed in the RPS. This sequence, consisting of SR 3.3.5.2, SR 3.3.6.1, and SR 3.3.6.2 tests the entire ESFAS from sensor input to the bistable logic processor through the automatic ESF actuation logic (actuational) output of each subgroup. These overlapping tests are described in Reference 1. SR 3.3.5.2 and SR 3.3.6.1 are normally performed together and in conjunction with ESFAS testing. When the actuational output signal for a subgroup is generated, SR 3.3.6.2 verifies that ESF components associated with the subgroup are capable of being actuated by the ESF-CCS.

These tests verify that the ESFAS is capable of performing its intended function, from sensor input to the bistable logic processor through the actuated components. SR 3.3.5.2 is addressed in LCO 3.3.5.
SR 3.3.6.1 includes LCL testing, initiation logic (trip path) testing, and actuation logic testing.

Local Coincidence Logic Testing

LCL testing verifies the OPERABILITY of the 2-out-of-4 coincidence logic and trip channel bypass logic.

Initiation Logic (Trip Path) Testing

Q16-122.3c

Testing of initiation logic, which consists of logical “OR” ~~(selective 2-out-of-4 logic)~~, is performed after the completion of LCL testing. This testing exercises only one initiation logic channel at a time, which affects only one trip path.

BASES

SURVEILLANCE REQUIREMENTS (continued)

selective

Actuation Logic Testing

Q16-122.3a

Actuation logic testing verifies the OPERABILITY of the 2-out-of-4 actuation logic after the completion of initiation logic (trip path) testing. This test is performed only for one channel and one actuation logic at a time by periodic automatic test.

Manual ESF Actuation Testing

Manual ESF actuation testing is tested every 31 days to verify that manual pushbutton can actuate the actuation logic as designed.

The 31 day Surveillance period is determined by operating experience and shows that equipment can meet the Surveillance requirement condition when equipment is tested as this Surveillance period.

SR 3.3.6.2

Individual subgroup must also be tested, one at a time, to verify the individual ESFAS components will actuate when required.

Each ESFAS Function has an associated group of outputs. Each group of outputs is divided into subgroups. Outputs within a subgroup are tested concurrently and are selectively arranged so that concurrent actuation does not adversely affect plant operations.

The ESFAS initiation signals from the PPS are sent to separate ESF-CCS cabinets. Each cabinet contains the actuation logic for only one division. Therefore, a failure in one cabinet cannot affect the circuitry and actuated equipment of the other divisions.

Single failures of the actuation logic will cause, at worst, only a failure of a component, group of components, or one entire redundant train. The actuation of the remaining redundant division is sufficient for the protective action.

A CHANNEL FUNCTION TEST performs to verify a EDG start is actuated by SIAS, CSAS, and AFAS signals.

The 31 day Frequency on a STAGGERED TEST BASIS complies with the operating experience and ensures the problems of individual logic signal can be detected within this time frame.

BASES

SURVEILLANCE REQUIREMENTS (continued)

Some components cannot be tested at power operation since their actuation may lead to plant trip or equipment damage. Actuation logic subgroups not tested at power operation must be tested in accordance with ~~the Notes~~ to this SR.

Q16-122.3e

SR 3.3.6.3 Note 1

A CHANNEL FUNCTIONAL TEST for diverse ESF manual actuation channel performs the diverse manual ESF actuation circuit by manual actuation of each Function. This testing is performed every 18 months to verify that the trip pushbutton can actuate the actuation logic as designed.

REFERENCES 1. FSAR, Section 7.3.

In accordance with Note 2 to this SR, the pair of Actuation Logic subgroup channels A and C are tested during the first interval of the staggered 31 day Frequency, and the pair of Actuation Logic subgroup channels B and D are tested during the second interval of the staggered 31 day Frequency. Therefore, each pair of Actuation Logic subgroup channels is tested during an interval of 62 days, plus applicable extensions.