REVISED RESPONSE TO REQUEST FOR ADDITIONAL INFORMATION

APR1400 Design Certification

Korea Electric Power Corporation / Korea Hydro & Nuclear Power Co., LTD

Docket No. 52-046

RAI No.:	**295-8263**
SRP Section:	**16 – Technical Specifications**
Application Section:	**16.3.3**
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Question No. 16-116

According to DCD Tier 2 Section 7.3.1.4 Component Control Logic, on page 7.3-9, the “LC priority logic performs a prioritization between ESF actuation signals and component-level signal from the ESCM and MI switches. The output of the LC priority logic is then inputted to the priority logic in the CIM.” The applicant is requested to describe how the priority logic, which is implemented in the LC and the CIM, is considered to be within the scope of generic TS 3.3.6, ESFAS Actuation Logic, for generic TS Table 3.3.6-1 Functions 1c, 2c, 3c, 4c, 5c, and 6c.

Response – (Rev. 1)

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The description of ESFAS priority logic will be incorporated to ensure the priority logic performs as designed in the APR1400 Technical Specifications Bases section 3.3.6 as indicated in the attachment associated with this response.

Impact on DCD

There is no impact on the DCD.

Impact on PRA

There is no impact on the PRA.

Impact on Technical Specifications

APR1400 Technical Specifications Bases section 3.3.6 will be revised, as indicated in the attachment associated with this response.

Impact on Technical /Topical/Environmental Reports

There is no impact on any Technical, Topical, or Environmental Report.

BASES

BACKGROUND (continued)

The devices and circuitry that generate the above ESFAS signals are grouped into the following interconnected parts. These parts are:

- Measurement channels,
- Bistable logic processor channels,
- ESFAS logic channels:
  - Coincidence Logic,
  - Initiation Logic (trip paths), and
  - Actuation Logic.

This LCO addresses the ESFAS logic channels. Bistable logic processor channels and measurement channels are addressed in LCO 3.3.5, “Engineered Safety Features Actuation System (ESFAS) Instrumentation”.

The roles of the measurement channels and bistable logic processor channels are described in LCO 3.3.5. The role of the ESFAS logic is described below.

ESFAS Logic

The ESFAS logic, consisting of coincidence, initiation and actuation logic, employs a scheme that provides an ESFAS actuation signal from all four PPS divisions to the component control logic of all trains of the associated ESF Systems when any two of the four bistable logic processor channels sense that the same input parameter has satisfied the ESFAS Function’s trip setpoint on the input parameter. This logic scheme is called a 2-out-of-4 trip logic.

The actuation logic includes the priority logic.

Coincidence Logic

There is one local coincidence logic (LCL) associated with each trip bistable logic of each channel of a given ESFAS instrument Function. Each LCL receives four trip signals, one from the trip bistable logic in the associated channel and one from each trip bistable logic located in the other three channels of the affected ESFAS instrument Function. The LCL also receives the trip channel bypass status signal associated with each of the bistable signals. The function of the LCL is to generate a coincidence logic trip signal whenever two or more like bistables are in a tripped condition. Each LCL automatically changes the state of each of the four coincidence logic channels based on the state of the trip channel bypass Function in each channel. For example, a 2-out-of-4 trip logic goes to 2-out-of-3 if one trip bistable logic channel is bypassed.

BASES

BACKGROUND (continued)

Designating the protection channels as A, B, C, D, with no trip channel bypass signal present, the LCL will produce a coincidence logic trip signal for any of the following trip inputs: AB, AC, BC, BD, CD, ABC, ABD, ACD, BCD, ABCD. These represent all possible 2- or more out-of-4 trip combinations of the four protection channels. Should a trip channel bypass be present, the logic will provide a coincidence logic trip signal when two or more of the three un-bypassed trip bistable logic channels are in a tripped condition.

Initiation Logic

The initiation logic is designed to be fail-safe. Failure of one initiation logic channel will result in a partial trip (1 of 4) in the 1-out-of-2 taken twice ESFAS selective actuation logic. The partial trip will be alarmed the same as a full ESFAS trip and will be indicated by the Qualified Indication and Alarm System – Safety (QIAS-P) and the Information Processing System (IPS); the partial trip cannot be bypassed.

Actuation Logic

The four initiation logic signals from the PPS are used to generate a selective 2-out-of-4 logic actuation signal in each division of the ESF-CCS. In the actuation logic, each signal also sets a latch when the selective two-out-of-four logic actuates to assure that the ESF actuation signal is not automatically reset once it has been generated.

A trip leg is defined as the “logical or” combination of channel states which represent half of a selective 2-out-of-4 logic function. When both trip ~~leg~~ legs of a selective 2-out-of-4 logic function assume a true state, the output of the selective 2-out-of-4 logic function assumes a true state (e.g., in a selective 2-out-of-4 logic [(A “or” C) “and” (B “or” D) = N]; the term (A “or” C) is a trip leg, the term (B “or” D) is a trip leg, and N is the output).

Receipt of two ESFAS initiation logic channel signals will generate the actuation logic division signals. This is done independently in each ESF-CCS cabinet, generating division A and division B signals, and where required for ESF Systems with four trains, division C and division D actuation signals.

Insert following page

Manual Trip

ESFAS Manual Trip capability is provided to permit the operator to manually actuate an ESF System when necessary.

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The actuation logic includes the priority logic in the ESF-CCS loop controller (LC) and the priority logic in the component interface module (CIM). The LC provides the prioritization logic between system-level ESFAS signals and component-level control signals. The system-level ESFAS signals have priority over the component-level control signals.

The manual ESFAS switches generate system-level ESFAS manual actuation signals that have priority over the component-level control signals, using the priority logic in the LC.

The CIM prioritizes the control signals from the (A) ESF-CCS LC, (B) diverse protection system (DPS), and (C) diverse manual actuation (DMA) switches. Of signals A and B, the one that causes the associated component to go to its safety state is the higher priority signal (state based priority). Regardless of signals A and B, signal C has the higher priority. Since the DMA functions initiate system-level actuation of all ESF trains, the DMA switch generated signals have system-level priority.