HF Controls

HFC-6000 Control System

ERD1192 – Control System Qualification Project

Operability Test Procedure Remote 01

TP901-301-05 Rev B

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[XXXXXXXXXXXXX]

Revision History

Date	Revision	Author	Changes
08/26/11	A0	E. Herchenrader	Initial Draft
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03/27/12	B	D. Briner	CR 2012-0140

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1.0 PURPOSE AND SCOPE

A HFC-6000 safety control system (Test Specimen), is configured for generic qualification as a commercially available control system for safety-related applications in nuclear power plants. The following set of Operability tests will be performed following completion of burn-in, system integration, and TSAP validation:

- **Accuracy Test** - This test will verify that analog I/O modules meet the accuracy and linearity requirements. (EPRI TR-107330 references: 4.3.2.1, 4.3.3.1, 5.3.A, 6.2.2.B.2, B.6, and B.8)

- **Response Time Test** – This test will measure the response time for discrete and analog inputs from the leading edge of the input to the leading edge of the resulting output (EPRI TR-107330 references: 4.2.1.A, 5.3.B, 6.2.2.B5).

- **Discrete Input Operability Test** - This test will verify the capability of discrete input channels to respond to simulated input signals. (EPRI TR-107330 references: 5.3.C, 6.2.2.B.6) – Not applicable

- **Discrete Output Operability Test** - This test will verify the capability of discrete output channels to produce output signals having specified voltages and currents. (EPRI TR-107330 references: 5.3.D, 6.2.2.B.8) – Not applicable

- **Communication Operability Test** – This test will verify reliable data transfer over the ICL, C-Link, and serial interfaces with CSMs and M/A stations. (EPRI TR-107330 references: 5.3.E)

- **Coprocessor Operability Test** – Not applicable

- **Timer Test** – This test will verify the accuracy of the timer function accessible to the TSAP. (EPRI TR-107330 references: 5.3.G, 6.2.2.B.3)

- **Failure To Complete Scan Test** – This test will validate the system will still function when an application cannot complete one cycle of execution within HFC-6000 operation context switch time. In the current configuration, the context switch time is 100ms. (EPRI TR-107330 references: 4.2.3.7.A, 5.3.G, 6.2.2.B.3)

- **Failover Operability Test** – This test will demonstrate correct operation of the failover function. (EPRI TR-107330 references: 4.3.4.7, 5.3.I)

- **Loss of Power Test** – This test will demonstrate correct response of all I/O channels to loss of source power followed by reapplication of power to the system. (EPRI TR-107330 references: 5.3.J)

- **Power Interruption Test** – This test will demonstrate the capability of the power modules to sustain system operation during a temporary (transient) power interruption. (EPRI TR-107330 references: 4.6.1.1.F, 5.3.K)

- **Power Quality Tolerance Test** – This test will demonstrate the capability of the Test Specimen to continue normal operation over a range of source power voltages and frequencies. (EPRI TR-107330 References: 4.2.3.7.B, 4.6.1, 6.4.3, 6.4.4.F)

The results of these tests will establish the performance baseline for the system. This performance baseline will then be used as the basis for evaluating system performance during and/or following each of the qualification tests required by the EPRI standard.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

This test procedure constitutes part of the prequalification testing for the HFC-6000 control system. These tests have been developed to document the baseline performance of the control system Test Specimen prior to the start of qualification stress testing.

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996
IEEE 1050	IEEE Guide for Instrumentation and Control Equipment Grounding in Generating Stations,

2.2 RELATED PLANS AND PROCEDURES

TP901-301-02	ERD1192 Integration Test Procedure, Rev. B
VV901-300-02	ERD1192 Master Test Plan, Rev. A
VV901-304-01	ERD1192 Master Configuration List, Rev. A
VV901-304-02	ERD1192 Test Specimen Design Specification, Rev. A

2.3 SUPPORT DOCUMENTATION

500620-01	ERD1192 Remote Loop Layout, Rev. F
500621-01	ERD1192 Power Distribution, Rev. D
500633-01	ERD1192 TSAP Schematic Wiring Diagrams Remote 1, Rev. B
500638-01	ERD1192 HPAT Schematic Wiring Diagrams Remote 2, Rev. B

2.4 HFC INTERNAL STANDARDS AND PROCEDURES

QPP 5.1	Review and Approval of Quality Documents
QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-205	Develop Software/Firmware Test Procedure

2.5 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

CPC	Communication Protocol Controller
CSM	Control Switch Module
HAS	Historical Archiving System

HPAT	HFC Plant Automated Tester
M/A	Manual/Automatic
M&TE	Measuring and Test Equipment
PCC	Peripheral Communication Controller
RH	Relative Humidity
SOE	Sequence of Events
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test Specimen Application Program

3.0 PREREQUISITES

The following paragraphs provide detailed instructions for setup and performance of each Operability test. The Prudency tests may be running concurrently with the Operability tests (Refer to TP901-301-04). To the maximum extent possible, both the Operability and Prudency tests will be configured to run automatically under control of the HPAT tester. Any operability test that cannot be executed under automatic control will not be run concurrently with the qualification tests.

3.1 EQUIPMENT REQUIRED

A detailed listing of hardware and software components of the Test Specimen is provided in the Master Configuration List, VV901-304-01. Detailed requirements for component assembly and interconnection are provided by the engineering drawing package listed in section 2.3 of this document.

The following equipment will be required during performance of this test. Test personnel shall verify that all test and measuring equipment are capable of producing the level of accuracy required by the specific test being performed and that the calibration for the M&TE to be used is current. Use attachment 7.1 to record test equipment used.

- [redacted]

3.2 ENVIRONMENTAL CONDITIONS

This test will be conducted under various conditions of temperature and humidity. During prequalification testing, the test will be conducted under normal operating conditions for the Test Specimen:

Temperature	50 deg to 104 deg F
Relative Humidity	7% to 90% non-condensing

During the qualification tests, required environmental conditions are stipulated within in the procedures governing those tests.

3.3 TEST PERSONNEL

The set of Operability tests will be conducted at the in-house test facility of HFC following completion of the TSAP Validation Test and at vendor facilities during qualification testing. All of the testing and monitoring functions will be conducted by a qualified HFC test engineer both at the HFC facility and at the facility of the vendor during qualification testing.

3.4 PRECAUTIONS

WARNING

Certain I/O circuits are energized with high voltages and may carry potentially hazardous current loads. Exercise caution whenever working around exposed terminals or circuitry.

3.5 RED-LINE POLICY

The HFC policy for entering red-line corrections into a test procedure are presented in paragraph 2.6.2 of VV901-300-02, "ERD1192 Master Test Plan". Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.6 TEST SETUP REQUIREMENTS

3.6.1 Test Specimen Setup

1. Verify that the copy of the Operability Test Procedure test in hand is a controlled copy of the latest revision according to Document Control records.

2. Verify that execution of the ERD1192 Integration Test Plan, TP901-301-02, is complete.

3. Verify that execution of the TSAP Validation Procedure, TP901-301-03, has been successfully completed.

Validation that test setup is complete: _____

Name/Date

3.6.2 SOE Point Configuration

An SOE logger will be used to monitor high speed (up to ± 1 ms resolution) logic transitions of TSAP DO channels during operation of the Operability tests or static states during the qualification tests. Table 1 lists the SOE point assignments for both the operability test and for static point tests. (Remote 2 runs the HPAT application for the Operability and Prudency tests.) The following procedure describes the sequence of steps necessary to configure the SOE logger prior to running the Operability tests for the first time. Individual digital I/O signals are configured for logging by connecting the associated signal line to the SOE channel indicated in Table 1.

1.

2.

Figure 1 – SOE Manual Trigger Control

Validation that SOE setup is complete: _____

Name/Date

Table 1. Points Configured for SOE Logging

Description	Output Point	Input Point	SOE Log Points	Chatter Box Point
Digital Response Time Test				
Analog Response Time Test				
Timer Operability Test				
Failure to Complete Scan Test				
Signals for Digital Static Test Conditions				
HFC-SBC04A Timer & BOE Test				

3.6.3 HAS Configuration

The HFC HAS software utility will be used for logging the value of analog signals as well as digital signals that do not require a time resolution of less than 1 second. Table 2 lists the combination of points selected for HAS logging during the initial qualification tests and for the repetition of selected tests. The following procedure describes the sequence of steps necessary to configure the HAS database before running the logger for the first time.

1.

2.

3.

Figure 2 – PointConfig.xls

Table 2. Points Configured for HAS Logging

Description	Output Point	Input Point	Log Points	Chatter Box Point
Analog Accuracy Test Points				
Digital Response Time Operability Test				
Communication Operability Test				
Burst of Events Test Points				

Description	Output Point	Input Point	Log Points	Chatter Box Point
Miscellaneous Points for Static Tests				
Miscellaneous I/O Points				

Validation that HAS setup is complete: _____

Name/Date

4.0 TEST PROCEDURE

Each of the individual tests within the Operability test provides a separate evaluation for a specific aspect of the Test Specimen performance and operation. No fixed sequence of execution is assumed or implied by the order of specific tests in this document. Before executing the test, mark the test condition for this operability test to be executed in the following:

Test Condition

☐ Pre-Qualification / Baseline

☐ Environment ☐ High Temp/RH ☐ Low Temp/RH ☐ Post Stress

☐ Seismic ☐ During ☐ Post

☐ EMI/RFI

☐ Post ESD

☐ Other _____

The majority of the tests are controlled by the MCRT. Index.gra should be set as the default graphic when starting MCRT for this test. Figure 3 shows a screenshot of a typical Index.gra screen.

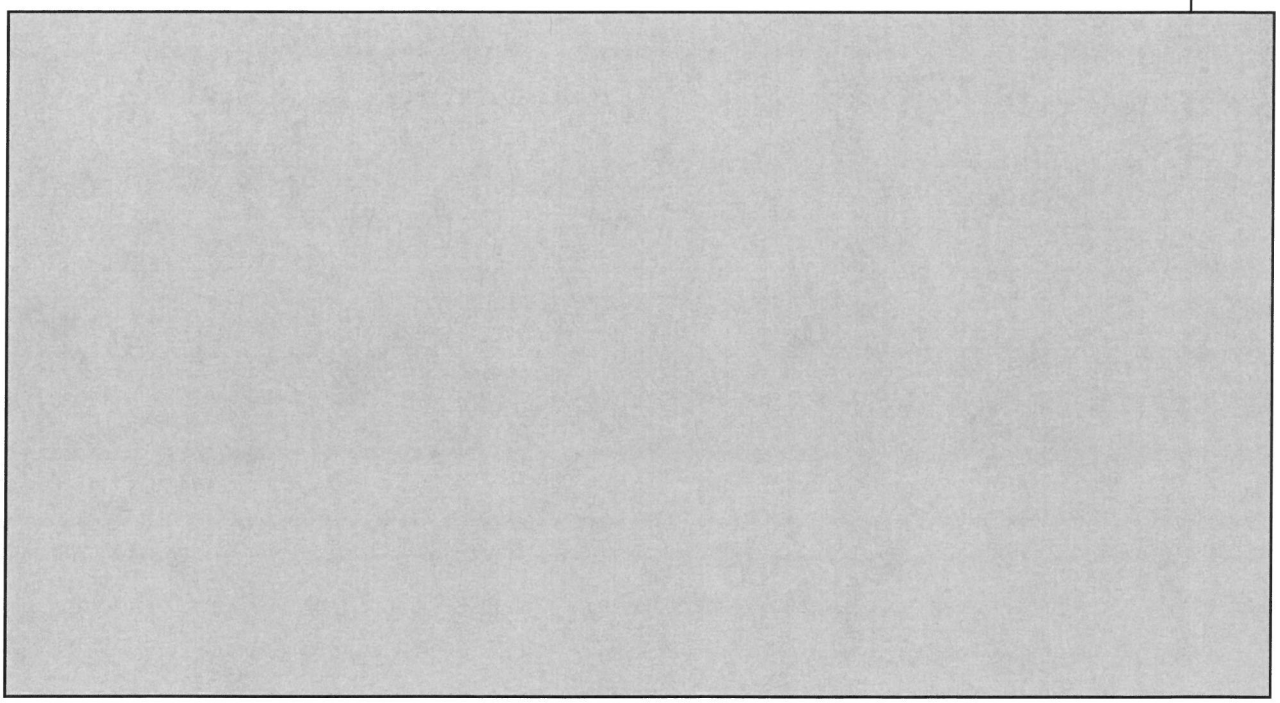


Figure 3 – Index page for ERD1192 Remote 1 controls

4.1 ACCURACY TESTS

The HPAT test algorithm and the Test Specimen TSAP include a stair-step analog algorithm (Figure 4) to support automated testing of 4 to 20mA analog I/O channels. The HPAT produces analog output signals that are routed to Test Specimen AI channels

under test, and the TSAP algorithm drives the AO channels under test. These test algorithms are fully automated and will be conducted under two conditions:

- Under normal operating conditions with no abnormal stress applied
- While specified qualification tests are in progress

In contrast, generation of the test signal for the RTD, TC, and pulse card AI channels cannot be automated. During the qualification tests, each of these channels will have a fixed input value or will be reading the input from an actual TC or RTD. Table 2 lists all I/O channels configured to support accuracy testing, lists the origin of the test signal, and the point to be logged to monitor test results.

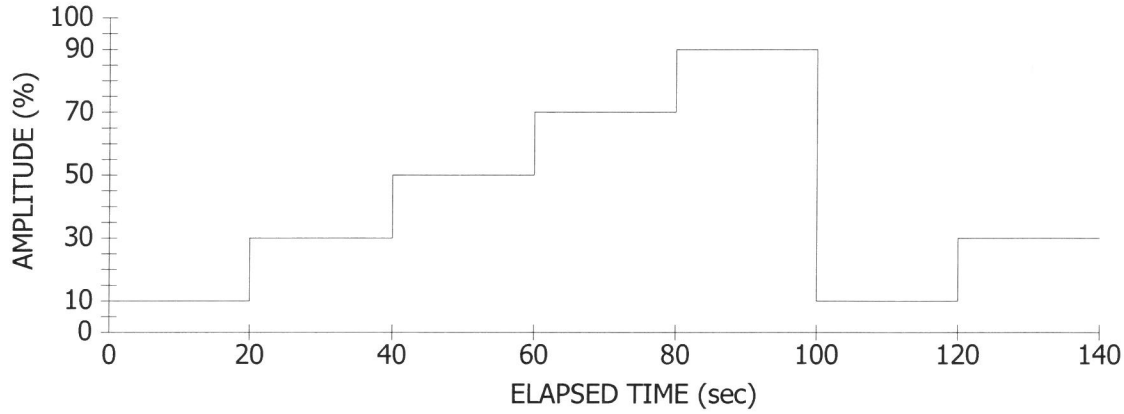


Figure 4 – Algorithm for 4-20 mA Analog Channel Accuracy Test

Automated Test Sequence

1. On the EWS workstation, ensure the HAS Logging program is running _____
2. On the MCRT graphic, actuate the START button for the analog accuracy test _____
3. Allow the test to run for a minimum of three complete cycles of the test waveform (5 minutes) or the duration of the qualification test being run _____
4. On the MCRT graphic, actuate the STOP button for the automated analog accuracy test _____
5. Record the HAS file name created during this test using attachment 7.13. _____

Validation of Automated Test Sequence: _____
Test Engineer/Date

4.2 RESPONSE TIME TEST

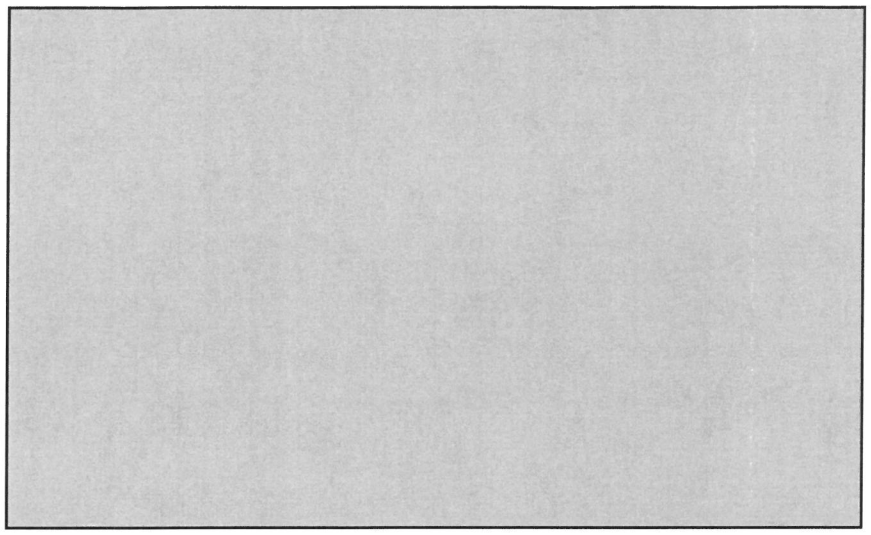
The HPAT and the TSAP include separate algorithms to support direct measurement of Test Specimen response time for analog and digital logic components. Both test algorithms can be started and stopped from the MCRT workstation and are designed to support automatic logging. Use attachment 7.8 to record the test results.

4.2.1 Digital Response Time Measurement

The TSAP provides a round-robin discrete input/output/input/output program pattern composed of seven DI channels and seven DO channels. (Figure 5 illustrates the design of the test algorithm; refer to the TSAP to identify the specific I/O points used to implement the algorithm.) [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX] In addition, the HPAT application provides a free-running square wave that is not synchronized with the operation of the TSAP. The output from this logic controls the input of a simulated trip memory (R/S logic in Figure 5).

This arrangement provides a mechanism for measuring both the stability of the processing cycles and the response time of the digital processing logic. The resulting response time measurement will include the time required for the following processing steps:

- Input filtering and signal conditioning
- Input processing by the I/O card processor
- Transfer over the internal system ICL to the controller
- Two processing cycles of the equation interpreter algorithm having a minimum of 2000 simple logic elements
- Transfer over the internal system ICL to the DO card
- Output processing of the DO processor
- Operation of the output relay



[redacted]

Figure 5 – Remote 01 TSAP Algorithm for Digital Response Test

The average processing cycle time is [XX] of the total period of the free-running square wave produced by the TSAP algorithm. The digital logic response time is measured directly by the transition of 1,DO,668 following the input from 1,DI,616 (refer to Remote 01 Logic drawing, 500633-01). The following parameters will be recorded as system baseline values following the initial execution of the digital response time test.

- The calculated value is an average of equation cycle time and deviation. (This calculated value will be compared with the value produced by the Equation Cycle counter 1,CO,50).

4.2.2 Analog Response Time Measurement

The TSAP provides a test algorithm (Figure 6) composed of two blocks and a simulated trip memory to support system response time measurements for analog components. [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX].

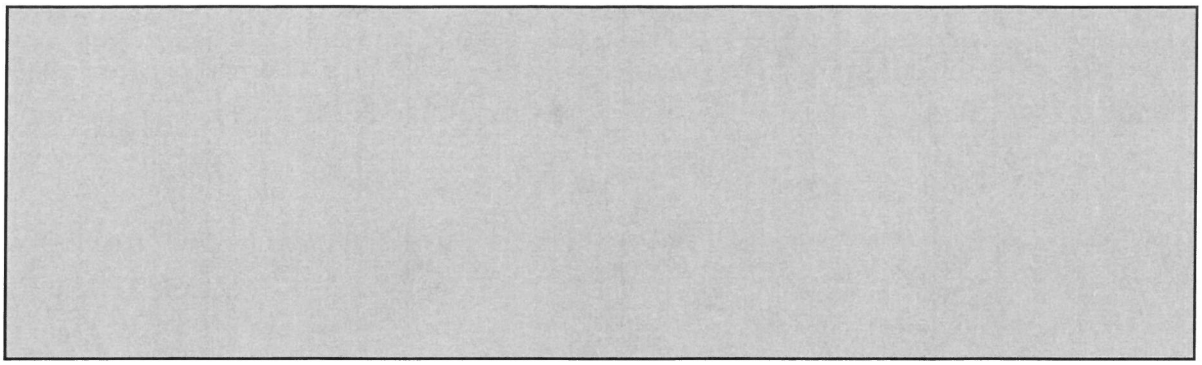


Figure 6 – TSAP Algorithm for Analog Response Testing

The SOE logger is used for measuring the response time. The logger records the off-to-on and on-to-off transitions of the simulated trip signal with an accuracy of ±1 ms. The difference between the trip output signal and the trip trigger signal gives accurate measurements for the response time.

4.2.3 Automated Response Time Test Sequence

The automated response time test will be conducted during the prequalification phase of testing and it will be repeated before, during, and after selected qualification tests. While the test is running, logic transitions will be logged automatically by the SOE and HAS utilities.

1. On the EWS workstation start the HAS Server program or make sure HAS server is running. _____
2. On the MCRT graphic, ensure AUTO SOE Trigger is enabled. _____
3. On the MCRT graphic, actuate the START button for the Response Time test. _____
4. Allow the test to run for a minimum of 3 minutes or the duration of the qualification test being run. _____
5. On the MCRT graphic, actuate the STOP button for the automated Response Time test. _____
6. Record the SOE and HAS files created during this test on attachment 7.13. _____

Validation of Automated Response Time Test Sequence: _____

Test Engineer/Date

4.2.4 Manual Analog Response Time Test Sequence

This manual analog response time test sequence shall be performed during qualification acceptance test. Data collected by this test sequence shall be used for calculating the actual analog response time. The automated analog response tests are mainly for accessing the stress performance during qualification tests.

1. Ensure that AUTO SOE Trigger is enabled. _____

2. The analog step signal is applied to 1,AI,896, and the simulated trip output is 1,DO,389. Connect channel 1 of the oscilloscope to the terminals for 1,AI,896 _____

3. Connect channel 2 of the oscilloscope to the terminals for 2,DI,161 _____

4. On MCRT graphic, actuate the START button for the response time test _____

5. Use the print screen capability of the oscilloscope to record the following measurements on attachment 7.8 _____
   - The transfer delay from the low-to-high input of the AI signal to the low-to high transition of the DO signal as leading edge transfer delay
   - The transfer delay from the high-to-low transition of the AI signal to the high-to-low transition of the DO signal as trailing edge transfer delay

6. Obtain a minimum of 3 measurements in step 5 on attachment 7.8 _____

7. On MCRT graphic, actuate the STOP button for the response time test _____

8. Record the SOE log files using attachment 7.8. The SOE files contain the analog response time in the system which is part of the transfer delay measured in step 5. _____

Validation of Manual Analog Response Time Test Sequence: _____
Test Engineer/Date

4.2.5 Manual Digital Response Time Test Sequence

Perform this manual digital response time during prequalification test. The automated digital response tests should provide the same information. During qualification tests, perform this test sequence only when automated tests cannot be executed.

1. Ensure that AUTO SOE Trigger is enabled _____

2. The specific DI and DO channels selected for running the digital response time are listed in Table 1. Connect channel 1 of the oscilloscope to the terminals for 1,DO,661 (shown as DO,2 in Figure 5). _____

3. Connect channel 2 of the oscilloscope to 1,DI,616 controlling the input to the simulated trip memory (shown as DI,8 in Figure 5). _____

4. Connect channel 3 of the oscilloscope to 1,DO,668 from the simulated trip memory (shown as DO,8 in Figure 5). _____

5. Actuate the START button for the response time test _____

6. Allow the waveform shown on channel 1 of the oscilloscope to stabilize. Configure trace 1 of the oscilloscope to measure the period of the free-running square wave (equation processing cycle time measurement). _____

7. Configure traces 2 and 3 to measure and record the interval from the false-to-true transition of 1,DI,616 to the false-to-true transition of 1,DO,668 as leading edge response time on attachment 7.8. _____

8. Configure traces 2 and 3 to measure and record the interval from the true-to-false transition of 1,DI,616 to the true-to-false transition of 1,DO,668 as trailing edge response time on attachment 7.8. _____

9. Use the print screen capability of the oscilloscope to record the measurements. Also record the true and false period of the signal. _____

10. Repeat steps ***8*** to ***10*** for 2 more measurements _____

11. Actuate the STOP button for the response time test _____

12. Record the SOE log files using attachment 7.8 _____

Validation of Manual Digital Response Time Test Sequence: _____
Test Engineer/Date

4.3 COMMUNICATION OPERABILITY TEST

The HFC-6000 control system includes two internal communication networks. Redundant Intercommunication Links (ICL) enable communication between the controller and all configured I/O modules for a particular controller. Redundant C-Link channels enable communication between a remote controller and attached workstation PCs or with external equipment. (If a control system includes more than one remote controller, each controller is configured as a separate node on the C-Link, and a token-passing protocol enables transfer of link mastership from node to node in a continuous round-robin sequence.) This test will use link error counters to provide a basis for evaluating the quality of communication on these links. The test will be conducted during the pre-qualification phase of testing and then repeated before, during, and after each qualification test. The overall test method will consist of recording the count value of the error counters at the start and end of a test period and interpreting the total accumulated error count as the measure of communication reliability. The test will be configured to run concurrent with other operability tests. Use attachment 7.11 to record test results.

1. Open the Memory Editor program, and read memory location 0415:7AB8 (ICL diagnostic structure) with integer format selected. Table 3 defines the detailed contents of this structure. _____

Table 3. ICL Diagnostic Structures

2. Open the Database Editor to read 1,CO,10 through 1,CO,11. Record the values on attachment 7.11. _____

3. On the MCRT graphic, actuate the START buttons for the analog accuracy, response time test, and Burst of Events test to provide a level of background operation _____

4. Select repeat mode for Memory Editor and take a screen capture of the data returned. (The second word on the first row of the ICL status byte display is the cumulative error counter for each link.) Save the screen capture in a separate file. _____

5. On the MCRT graphic, ensure AUTO SOE Trigger is enabled _____

6. Ensure that the HAS Server is running _____

7. Allow the test to run for a minimum of 5 minutes or the duration of the qualification test being run _____

8. Take a screen capture of the Memory Edit window showing the cumulative error count, and save it in a separate file. (The Memory Edit window provides a display of current time). _____

9. On the MCRT graphic, actuate the STOP button for the automated analog accuracy, burst of events and response time tests _____

10. Record the SOE log files and HAS files using attachment 7.13 _____

Validation of Communication Operability Test: _____
Test Engineer/Date

4.4 TIMER TEST

The timer test will be based on logic completely contained within the TASP. This logic will consist of four pulse timers configured to control two separate free-running square waveforms, as illustrated in Figure 7; the specific DO channels assigned for this test are listed in Table 1. The output from one set of timers will be on for 1 second and off for 1 second; the waveform from the second set will be on for 5 seconds and off for 1 second. The two output signals will drive separate DO channels so that the timer periods can be measured directly with an oscilloscope. During qualification testing, the outputs will be routed to separate SOE input channels of the HPAT to permit automatic recording of the signal transitions. Use attachment 7.11 to record test results.

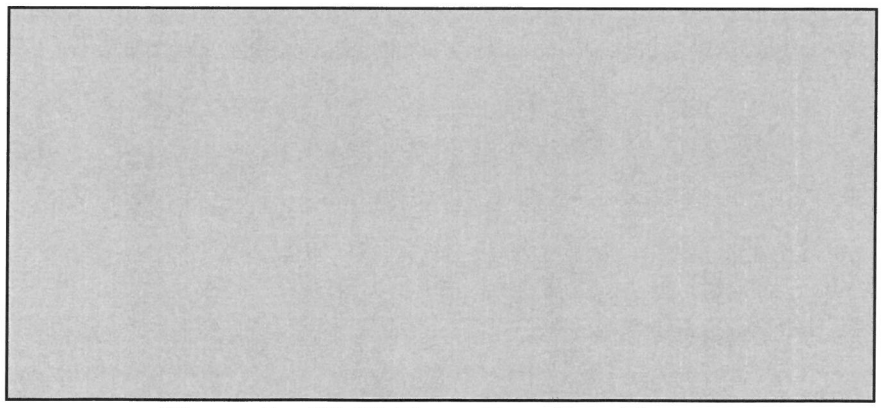


Figure 7 – TSAP Timer Test Algorithm

4.4.1 Manual Test Sequence

The manual test sequence will be executed during the prequalification phase of testing to establish a performance baseline for the Test Specimen. Repetition of the manual test prior to qualification tests will not be required unless system performance characteristics have changed.

1. Connect channel 1 of the oscilloscope to terminals for 1,DO,643 (shown as DO,1 in Figure 7), and connect channel 2 to the terminals for 1,DO,644 (shown as DO,2 in Figure 7) _____

2. On the MCRT graphic display actuate the START button for the timer test _____

3. Configure the trace for channel 1 to display one complete period for the waveform of 1,DO,643 _____

4. Configure the trace for channel 2 to display the complete period for the waveform of 1,DO,644 _____

5. Use the screen capture function of the oscilloscope to record both waveforms using attachment 7.13 _____

6. Obtain a minimum of three measurements for both traces _____

7. On the MCRT graphic, actuate the STOP button for the timer test _____

8. Ensure that 1,DO,643 and 1,DO,644 are reconnected to 2,DI,151 and 2,DI,152, respectively _____

Validation of Manual Timer Test Sequence: _____
Test Engineer/Date

4.4.2 Automated Timer Test

The automated timer test will be performed before, during, and after selected qualification tests in order to detect any deterioration in system performance.

1. The automated timer test does not require any preliminary setup beyond ensuring that 1,DO,643 and 1,DO,644 are connected to 2,DI,151 and 2,DI,152 respectively _____

2. On the MCRT graphic, ensure AUTO SOE Trigger is enabled _____

3. Ensure that the HAS Server is running

4. On the MCRT graphic, actuate the START button for the timer test _____

5. Allow the test to run for a minimum of 1 minute or the duration of the qualification test being run _____

6. On the MCRT graphic, actuate the STOP button for the Timer test _____

7. Record the SOE log files and HAS files using attachment 7.13 _____

Validation of Automated Timer Test Sequence: _____
Test Engineer/Date

4.5 FAILOVER OPERABILITY TEST

The HFC-6000 Remote 01 control system as configured includes redundant controllers and redundant power supplies. The redundant controllers share a Dual-Ported Memory (DPM) assembly that provides the mechanism for transferring system status from the primary to the secondary controller. The power supplies normally are both powered on and provide operating power to separate power traces on the back plane. Diode auctioneering on each card in the chassis provide the mechanism for maintaining isolation between the power supplies. Consequently, only the controllers will be subjected to failover testing. Use attachment 7.11 to record test results.

NOTE

This test requires connection of test probes to the backplane. Consequently, this test cannot be performed while environment, seismic, EMI/RFI tests are being run.

1. Ensure AUTO SOE Trigger and HAS server logging is running _____

2. Enable the automated accuracy, response time, and timer tests to provide a minimum set of dynamic operations. (Refer to Paragraphs 4.1, 4.2.3, and 4.4.2.) _____
3. Measure the cycle period of the controller as follows: _____
   a. Open the Memory Editor, and configure it to read 1,CO,50
   b. Select Integer data format
   c. Select Repeat mode
   d. The counter value appears in the upper left corner of the display
   e. Time the processor for a minimum of 5 minutes, and record the following parameters in the test report record:
      - Counter value at start of interval
      - Counter value at end of interval
      - Total period of measurement

Record the average amount of time required for a single operating cycle of the controller on attachment 7.11.

4. Slot 13 in the backplane contains the DPM card. The P1 connector enables access to the following signals used for failover control. _____

   - P13-A39 SANE_A/
   - P13-C39 SANE_B/
   - P13-B39 PRI_A/
   - P13-B40 PRI_B/

5. Identify the controller that is operating as primary (A or B) _____

6. Connect the probe for channel 1 of the oscilloscope to the SANE signal for the controller operating as primary and connect the probe for channel 2 to the PRI signal for the secondary. _____

7. On the MCRT, initiate the "Failure to Scan" test _____

8. The card disables SANE status, and this transition will initiate transfer of PRIMARY status to the secondary. Use the oscilloscope to record the delay between the low-to-high transition of the SANE/ signal (channel 1) and the high-to-low transition of the PRI/ signal (channel 2) on attachment 7.11. _____

9. Restart the controller _____

10. Monitor the affect of failover on analog control loops as follows: _____
    a. Select the simulated analog loops for control valve FIK-135. Display the single point display for 1,BL,21 (PID controller) on EWS.
    b. Connect the probe for channel 1 of the oscilloscope to 2,AI,31 (the CO channel for the analog loop). (Refer to drawing 500638-01 sheet 2, for the specific terminal assignments.)
    c. Connect the probe for channel 2 of the oscilloscope to 2,AO,43 (the PV channel for this analog loop).
    d. Press the red pushbutton switch on the front edge of the DPM card to initiate failover.
    e. If any disruption in the control loop occurs, use the oscilloscope to record the magnitude and duration of the disruption on attachment 7.11. Take a screen capture of the single point display video trend.
    f. Use the M/A station for this loop to change the set-point value (SV) of the control loop by 20%.
    g. Use a stopwatch to measure how long the loop requires for the PV to

stabilize. Measure the time period from the point that the SV stops changing to the time when the PV is one scale increment from its final value.
Settle time = _____ (record that on attachment 7.11)

h. Return the SV back to its starting value.
i. After the PV stabilizes, repeat steps ***e*** and ***f***. Trigger failover before the PV completely stabilizes.
j. Measure the settling time with a stop watch. Take a screen capture of the single point display video trend to record the magnitude and duration of any disruption that occurs in the settling process.
Settle time = _____ (record that also on attachment 7.11)

11. Record the SOE log files and HAS files using attachment 7.13 _____

Validation of Failover Operability Test: _____
Test Engineer/Date

4.6 LOSS OF POWER TEST

During this test, power is removed from the Test Specimen for a minimum period of 30 seconds, and then the power is restored. The purpose of the test is to demonstrate that all I/O channels transition to default power-off state when power is removed and then hold these states following restoration of power until after system initialization is complete, at which time normal operation resumes. Because this test disrupts the operation of the controller, it will not be executed while any of the qualification tests are in progress. Use attachment 7.12 to record test results.

1. Ensure HAS logging and AUTO SOE trigger are running _____

2. Configure all of the simulated analog control loops as follows: _____

   a. Press the M/A station A switch to select Auto mode
   b. Verify that the SV is at its default value or at mid range
   c. Allow the process variable (PV) and controlled output (CO) values to stabilize

3. Configure all of the simulated digital control loops as follows: _____

   a. Press any CSM switch to clear alarm status.
   b. Use the CSM to change the control loop from its starting default state

4. Enable the automated accuracy, response time, and timer tests to provide a minimum set of dynamic operations. (Refer to Paragraphs 4.1, 4.2.3, and 4.4.2.) _____

5. Remove power from Remote 01 for a minimum period of 30 seconds. Ensure that the HPAT assembly is not powered down. _____

6. While power is out, verify indicated conditions for selected channels: _____
   - AO channels are at 0 mA 1,AO,841 _____ 1,AO,921 _____
   - Power output channels are open 1,DO,321 _____ 1,DO,261 _____
   - DO channels are de-energized. (Verify that all Remote 2 DI channels are off by inspecting the card edge LED's). _____
7. Restore ac power to Remote 01. Verify the following: _____
   - Test Specimen output channels remain disabled while initialization tests are in progress
   - After initialization tests are completed, the automated tests resume automatically without additional operator intervention
   - The simulated control loops remain in their initial default state
8. Record the SOE log files and HAS files using attachment 7.13 _____

Validation of Loss of Power Test: _____
Test Engineer/Date

4.7 POWER INTERRUPT TEST

During this test, power is removed from the Test Specimen for a period of 40 ms to simulate a power transient or transfer to an emergency backup power source. The purpose of the test is to demonstrate that the Test Specimen power supplies can maintain the output voltage at a level necessary to maintain controller operation during such a transfer. Because this test could disrupt any automated test that may be running, the power interruption test will not be executed while any of the qualification tests are in progress. Use attachment 7.12 to record test results.

1. Turn both of the two power sources for the Test Specimen off _____
2. Connect one power source to the Test Specimen through a timer relay. Configure the timer relay to interrupt power flow to the Test Specimen for a fixed interval of 40 ms. _____
3. Set power to the Test Specimen on _____
4. Configure all simulated analog loops as follows: _____
   a. Press the M/A station A switch to select Auto mode
   b. Verify that the SV is at its default value or at mid range
   c. Allow the process variable (PV) and controlled output (CO) values to stabilize

5. Configure all simulated digital loops as follows: _____

   a. Press any CSM switch to clear alarm status
   b. Use the CSM to change the control loop from its starting default state

6. Ensure SOE and HAS logging is running _____

7. Enable the automated accuracy, response time, and timer tests to provide a minimum set of dynamic operations. (Refer to Paragraphs 4.1, 4.2.3, and 4.4.2.) _____

8. Initiate the 40-ms interruption in source power _____

9. Allow the system to continue logging data for a minimum of 30 seconds after the power interruption _____

10. Disable the automated test sequences. (Refer to Paragraphs 4.1, 4.2.3, and 4.4.2.) _____

11. Record the SOE log files and HAS files using attachment 7.13 _____

Validation of Power Interrupt Test: _____
Test Engineer/Date

4.8 POWER QUALITY TOLERANCE TEST

The Test Specimen contains one set of redundant power supply modules for the HFC-6000 chassis. This test will verify the capability of the power supplies to continue providing adequate operating power to the control system under varying conditions of source power quality.

The power quality tolerance test is not a regular part of the operability test. It shall be conducted at the end of the high temperature phase of the environmental stress test and after completion of the SSE seismic test. Execution of this test is not required before, during, or after the other qualification tests. Use attachment 7.12 to record test results.

4.8.1 Pretest Setup

1. Power down the Test Specimen, and connect a variable power source to the redundant power modules. Add the MTE information for the power source to Attachment 7.1. _____

2. Configure all of the simulated analog control loops as follows: _____

   a. Press the M/A station A switch to select Auto mode
   b. Verify that the SV is at its default value or at mid range
   c. Allow the process variable (PV) and controlled output (CO) values to stabilize

3. Configure each of the simulated digital control loops as follows: _____

   a. Press any CSM switch to clear alarm status
   b. Use the CSM to change the control loop from its starting default state

4. Ensure AUTO SOE Trigger is enabled and HAS logging is running. _____

5. Enable the automated accuracy, response time, and timer tests to provide a minimum set of dynamic operations. (Refer to Paragraphs 4.1, 4.2.3, and 4.4.2.) _____

6. Record the SOE log files and HAS files using attachment 7.13 _____

Validation of Power Quality Pretest: _____
Test Engineer/Date

4.8.2 Power Quality Test

Note

The tolerance of the output produced by the variable AC power source used during this test should be [XXXXXXXXXXXX].

1. Set the power source to provide [XXXXXXXXXX], and power up the power supplies _____

2. Use a multimeter to monitor the output voltage level produced by each power supply _____

3. Ensure AUTO SOE Trigger is enabled _____

4. Verify low voltage operation as follows: _____

   a. Reduce the output from the variable power source to [XXXXXXXX]
   b. Record the output voltage levels produced by the power supplies
   c. Record the output voltage levels produced by the each power supply module on the test data record form with attachment 7.12

5. Verify power supply operation with power source at high frequency limit: _____

   a. Increase the variable output source frequency [XXX]
   b. Record the output voltage levels produced by each module on the test data record form with attachment 7.12

6. Verify system response to under voltage trip condition: _____

   a. Reduce the output from the variable power source to [XXXX]
   b. Verify that under voltage protection forces all power supplies off
   c. Verify that Test Specimen LED's are all off

7. Verify power supply recovery: _____

   a. Set the variable power source to [XXXXXX]
   b. Record the output voltage levels produced by all of the power supplies with attachment 7.12

8. Restore the original setup conditions. (Refer to Paragraph 4.9.1.) _____

9. Verify high voltage operation as follows: _____

   a. Increase the output from the variable power source to [XXXXXXXX XX]
   b. Record the output voltage levels produced by each power supply

10. Verify power supply operation with power source at high frequency limit: _____

    a. Increase the variable output source frequency to [XXXX]
    b. Record the output voltage levels produced by the power supplies connected to the high voltage power source

11. Restore the normal operation configuration: _____

    a. Set the variable power source to [XXXXXX]
    b. Record the output voltage levels produced by the power supplies

12. Record the SOE log files and HAS files using attachment 7.13 _____

Validation of Power Quality Test: _____
Test Engineer/Date

4.9 FAILURE TO COMPLETE SCAN TEST

The test is to validate the system handling of application failure to complete one execution within a context switch time.

1. On the EWS workstation, ensure the HAS Logging program is running _____
2. On the MCRT graphic, ensure AUTO SOE Trigger is enabled (see figure 1) _____
3. On the MCRT graphic, actuate the START button for the Failure to Scan Test _____
4. Allow the test to run for a minimum of 5 seconds _____
5. On the MCRT graphic, actuate the STOP button for the Failure to Scan Test _____
6. Record the SOE log files and HAS files using attachment 7.13 _____

Validation of Failure to Complete Scan Test: _____
Test Engineer/Date

5.0 ACCEPTANCE CRITERIA

The acceptance criteria for the operability tests are defined by EPRI TR-107330 and also based on the HFC specifications for the HFC-6000 product line. A preliminary set of results obtained during the prequalification phase of testing will establish baseline performance characteristics for the Test Specimen and TSAP. Subsequent performance of the operability tests during the qualification tests will disclose any deterioration from the baseline performance caused by the environmental stress conditions. The following sections describe the specific acceptance criteria for individual tests.

5.1 ACCURACY TEST ACCEPTANCE CRITERIA

4- to 20-mA AI Channels

HFC Design Specification	15 bit AI image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.35% of span over the entire range

4- to 20-mA AO Channels

HFC Design Specification	12 bit AO image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.32% of span over the entire range

100-ohm RTD Input Channels

HFC Design Specification	15 bit AI image 0 deg to 200 deg C design operating range

	Accuracy within ±0.1% of range over the entire range
During qualification test	Accuracy within ±2 deg C (3.6 deg F) over entire range

Type E Thermocouple Input Channels

HFC Design Specification	15 bit AI image -30 deg to 500 deg C design operating range Accuracy within ±0.1% of range over the entire range
During qualification test	Accuracy within ±3 deg C (5.4 deg F) over entire range

Pulse Input Channels, AI4K

Rate Mode	12-bit count value image within 1 bit accuracy 512 Hz minimum input pulse rate (12-bit image)
Accumulate mode	24-bit count image within 1 bit accuracy
During qualification test	Accuracy within 1 bit

Pulse Input Channels, AI4K2

Pulse Measurement	4-byte count image within ± 1ms (1000 count) accuracy
During qualification test	Accuracy within ± 1ms (1000 count) accuracy

5.2 RESPONSE TIME ACCEPTANCE CRITERIA

a. Response time from activation of the trip condition to output of the trip signal for digital signal shall be less than 100ms and for analog signal shall be less than 300ms

b. The measured response time shall not vary by more than ±10% from measured baseline value

5.3 DISCRETE INPUT/OUTPUT OPERABILITY ACCEPTANCE CRITERIA

Discrete Input Operability

DI set voltage level	Guaranteed DI set level is 12 to 15 v at 25 deg C
DI dropout voltage	Guaranteed DI dropout level is 12 to 15 v at 25 deg C
Maximum input voltage	Maximum input voltage is 53 v at 25 deg C

Discrete Output Operability

Relay DO channels	5 A at 30 v for resistive load

Solid State DO Channels	Correct digital output state
120 vac output channels	90 to 130 vac at 47 to 63 Hz minimum range 2 A minimum in-rush capacity Up to 0.5 A steady state current 2 vac maximum on state voltage drop at 0.5 A Supplies off state leakage current for coil continuity monitoring function without energizing the relay
125 vdc output channels	90 to 140 vdc 2 A minimum in-rush capacity Up to 0.5 A steady state current 2 vdc maximum on state voltage drop at 0.5 A Supplies off state leakage current for coil continuity monitoring function without energizing relay

5.4 COMMUNICATION OPERABILITY ACCEPTANCE CRITERIA

C-Link - Overall system operation continues in the presence of noise interference

ICL - I/O scanning continues in the presence of noise interference

5.5 TIMER TEST ACCEPTANCE CRITERIA

Timer accuracy shall vary by no more than ±1% of preset value or ±3 scan cycles

5.6 FAILOVER TEST ACCEPTANCE CRITERIA

(EPRI TR 107330 4.3.4.7 A & D)

a. Transfer to secondary controller shall trigger an alarm

b. Secondary controller shall continue to run in normal operation mode

c. The transfer shall ensure the following:

   i. Shall occur with 200 ms (2 main processor scan cycle times)

   ii. Shall not cause I/O modules to have more than an 0.5% transient shift in the final output signal

   iii. Shall not cause a change in the I/O signal that persists for more than 5 ms for DC signals or 1 cycle for AC signals

iv. Shall not cause pulse input modules to lose signal

v. Shall not cause digital I/O to change state for more than 2 ms, and analog I/O signals to change by more than 5%

5.7 POWER QUALITY ACCEPTANCE CRITERIA

Loss of Power Test

All output channels return to the de-energized state on loss of power

All output channels remain in a failsafe state defined for the control circuit until the operator initiates operation

Power Interruption Test

None of the processors reset

No static DO channels change state

None of the static AO channels change their output signal by more than 5%

Logged parameters of all automated tests remain within tolerance

Power Quality Tolerance Test

While source power is between 90 to 150 vac and 57 to 63 Hz, the output voltage level produced by the power supply remains within ±1% of its set-point level

No power supply dropout alarm occurs while source power is within the above specified range

Under voltage protection trips the power supply output and the power supply produces a system status alarm

Over voltage protection trips the power supply output and the power supply produces a system status alarm

The power supply recovers from over voltage / under voltage conditions automatically

5.8 FAILURE TO COMPLETE SCAN TEST ACCEPTANCE CRITERIA

a. When an input triggers the logic which indicates execution time is over 100ms, the system fails over from the main controller to the secondary controller and the system continues to operate properly on the new primary
b. The failover event is logged

c. A power reset of the 'failed' controller will bring the system back to redundant configuration

d. SOE log indicates the failure to complete scan detected within 200 ± 100ms

6.0 QA RECORDS

All data generated by execution of the tests covered by this procedure will become QA records. Test data generated during manual execution of the Operability tests will be recorded on the appended Test Data Record sheets. Results for the automated portions of the Operability tests will be recorded in a set of SOE and HAS report files. All test data records during the qualification phase of testing will be filed in accordance with the QPP 17.1, "Quality Records".

7.0 ATTACHEMENTS

Attachment 7.1 – Test Equipment Log
Attachment 7.8 – Response Time Test Record
Attachment 7.11 – Communication, Timer, Failover Test Record
Attachment 7.12 – Power Quality Test Record
Attachment 7.13 – SOE and HAS Test Records

Attachment 7.1 – Test Equipment Log

Test Equipment	Instrument ID	Calibration Due Date

Test Reviewer/Date

Attachment 7.2 – Response Time Test Record

Analog Response Time	**Measurement**		
	1	**2**	**3**
Leading edge transfer delay	_____	_____	_____
Trailing edge transfer delay	_____	_____	_____
SOE Report Files	_____	_____	_____
	4	**5**	**6**
Leading edge transfer delay	_____	_____	_____
Trailing edge transfer delay	_____	_____	_____
SOE Report Files	_____	_____	_____

Digital Response Time	**Measurement**		
	1	**2**	**3**
TRUE period of 1,DO,668	_____	_____	_____
FALSE period of 1,DO,668	_____	_____	_____
Leading edge response time	_____	_____	_____
Trailing edge response time	_____	_____	_____
SOE Report Files	_____	_____	_____

Test Engineer _____ **Date** _____

Attachment 7.3 – Communication, Timer, Failover Test Record

Communication Operability Test

(Append Memory Editor screen captures)

ICL Errors	
Error count at start	
Final error count	
Duration of test	

(Append Database Editor screen captures)

C-Link Errors			
Channel 0 (1,CO,10)		Channel 1 (1,CO,11)	
Error count at start		Error count at start	
Final error count		Final error count	
Duration of test		Duration of test	

Timer Operability Test

Timer	Average Over 10 Periods Minimum	
	Period	Jitter
1 Sec		
5 Sec		

Failover Operability Test

Processor Cycle Time Measurement

1,CO,50 value at start of interval _____

1,CO,50 value at end of interval _____

Total period of measurement _____

Average processor cycle time _____

Failover Transfer Time Measurement

Delay from trailing edge of SANE_A/ to leading edge of PRI_B/ _____

Analog Loop Disruption

Magnitude of disruption for stable analog values _____

PV Settling time for 20% increase in SP value without failover _____

PV Settling time for 20% increase in SP value with failover _____

Magnitude of disruption for analog values in transition _____

Digital Loop Disruption

Duration of disruption for stable DI and DO channels _____

Duration of disruption for DI and DO channels in transition _____

Test Engineer _____ **Date** _____

Attachment 7.4 – Power Quality Test Record

Power Loss Test

On loss of power:

All AO channels are open (0 mA output signal.) _____

All power (120 vac and 125 vdc) output channels are open. _____

All solid state relay DO channels are open (no continuity) _____

All mechanical relay DO channels are deenergized (NO contacts open, NC contacts closed) _____

On restoration of power:

All output channels remain disabled while powerup initialization remains in progress. _____

Automated test functions controlled from the HPAT resume without user intervention. _____

Simulated control loops remain in default states. _____

Power Interruption Test (Append HAS and SOE reports for logged points.)

Neither primary nor secondary controller reset due to the power interruption. _____

None of the I/O card processors reset due to the power interruption. _____

None of the static DO channels change state during the power interruption. _____

None of the static AO channels change by more than 5% during the power interruption. _____

Measured parameters of the automated tests remain within tolerance during and following the power interruption. _____

Test Engineer _____ **Date** _____

Attachment 7.12 Power Quality Test Record (Continued)

Power Quality Tolerance Test (Append HAS and SOE reports for logged points.)

Test Setup:

All automated Operability tests configured for dynamic operation. _____

All simulated analog loops set to Auto mode with the SP at mid range. _____

All simulated digital loops have alarm status cleared and are set to simulate operating status (run/open status). _____

SOE and HAS loggers configured to record dynamic operating status. _____

All automated Operability tests enabled. _____

Record Power supply Output Voltage Levels

Power Feed	Power Module A		Power Module B	
	24-vdc (slot 1)	24 vdc (slot 4)	24 vdc (slot 5)	24 vdc (slot 8)
[XXXXXXX]				
[XXXXXXX]				
[XXXXXXX]				
[XXXXXXX]				
[XXXXXXX]				
[XXXXXXX]				
[XXXXXXX]				
[XXXXXXX]				

Test Engineer _____ **Date** _____

Attachment 7.5 – SOE and HAS Test Records

Record the file name, date and time for each test run.

Test Conducted	File Name	Date and Time Created
4- to 20-mA AI Accuracy		
4- to 20-mA AO Accuracy		
TC AI Accuracy		
RTD AI Accuracy		
Digital Response Time		
Analog Response Time		
Timer Test		
Communication Test		

Test Engineer _____ **Date** _____

Attachment 7.13 – SOE and HAS Test Records (Continued)

Test Conducted	File Name	Date and Time Created
Failover Operability Test		
Loss of Power Test		
Power Interrupt Test		
Power Quality Tolerance Test		
Failure to Complete Scan Test		

Test Engineer _____ **Date** _____