Summary of MELTAC Platform V&V

Non-Proprietary

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Revision	Date	Page (section)	Description
0	January 2015	All	Initial issue
1	June 2015	General (P1, 6, 11, 36) P7-10 P33,34 P35	Modified the typo. Added the section “Summary of V&V Result”. Added the document number and revision. Updated the revision.
2	May 2016	1 (2.0) 11 - 51 (APPENDIX A)	- Modified the description related to the contents of Appendix A. - Deleted the MRP related description. - Updated the information regarding the MELTAC Platform V&V documents in accordance with “Mapping of MELTAC Platform Licensing Documents to the DI&C-ISG-06 Guidance” (JEXU-1041-1012-P, R0).

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1.0 INTRODUCTION

This summary describes the Verification and Validation (V&V) and testing activities associated with the Mitsubishi Electric Corporation (MELCO) Energy Systems Center (ESC) Mitsubishi Electric Total Advanced Controller (MELTAC) platform. The MELCO ESC V&V documents encompass the V&V for the MELTAC platform basic software, which includes the firmware and Field Programmable Gate Arrays (FPGAs) on all MELTAC platform modules.

This document supports the “Safety System Digital Platform - MELTAC - Topical Report” (JEXU-1041-1008) and the “MELTAC Platform Software Program Manual” (JEXU-1041-1016) and satisfies the commitments made under Table 1 sections 1.9, 2.2, 2.4, 2.5, 2.6, 2.7, 3.1, 3.2, 3.3, 3.4, 3.5 and 3.6 of “Mapping of MELTAC Platform Licensing Documents to the DI&C-ISG-06 Guidance” (JEXU-1041-1012).

2.0 DOCUMENTATION TREE AND CATEGORIZATION

Figure 1 shows the MELTAC Platform Documentation Tree. These documents are internal documents, which are categorized into three groups according to the following phases: Design Phase, Qualification Phase, and V&V Phase. The scope of this summary is the V&V documents prepared in the V&V Phase.

The Qualification Phase documents are described in “Summary of MELTAC Platform Equipment Qualification” (JEXU-1041-1023), and the Design Phase documents are described in “Summary of MELTAC Platform Design” (JEXU-1041-1022).

The MELTAC platform V&V documents corresponding to the information required by ISG-06 Enclosure B (Tier 3) are listed in Section 3. Specific document numbers are identified in Appendix A.

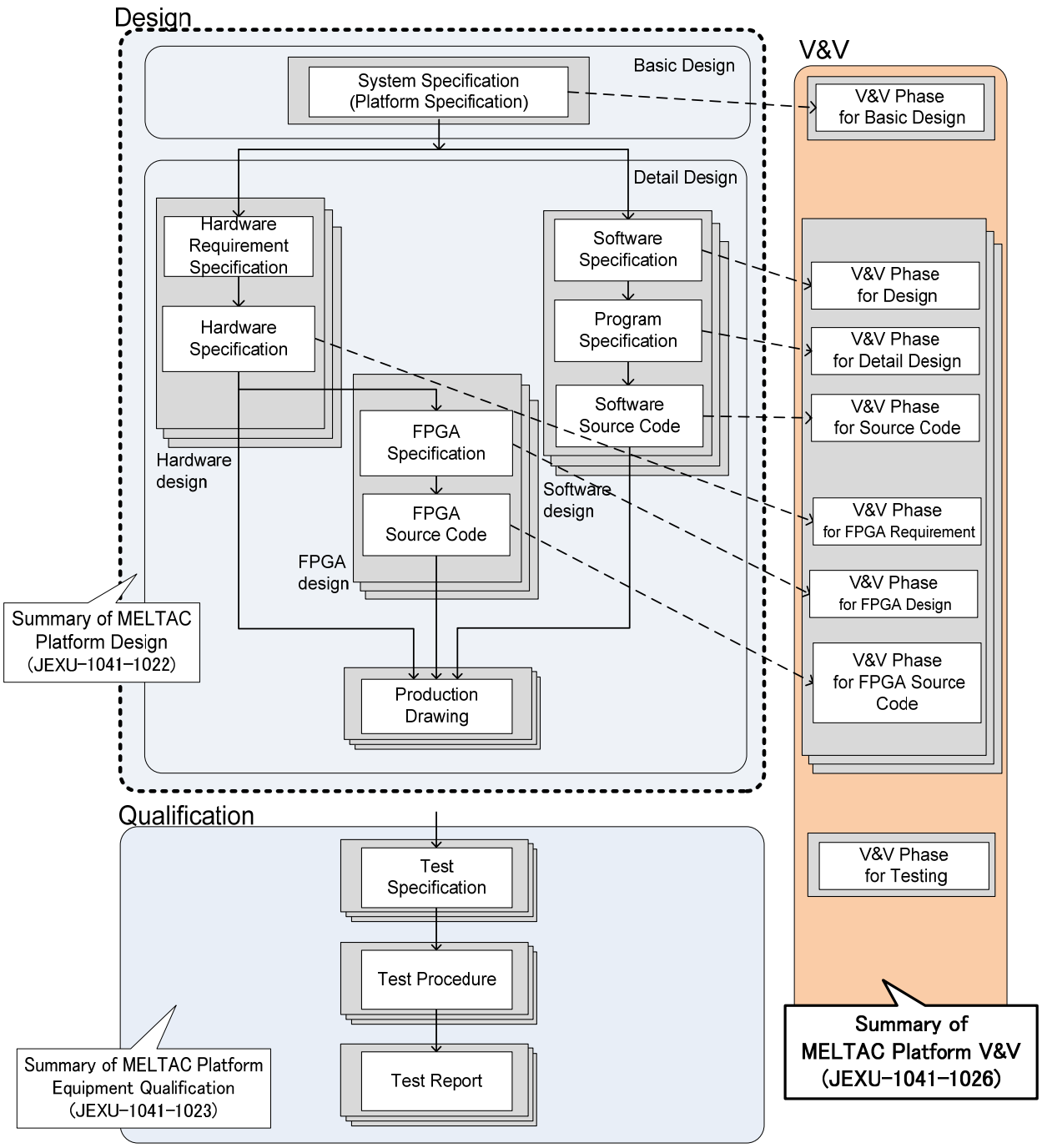

Figure 1 MELTAC Platform Documentation Tree

3.0 MELTAC V&V DOCUMENTS CORRESPONDING TO THE DOCUMENTS IN ISG-06 ENCLOSURE B TIER 3

The MELTAC V&V documents corresponding to the documents required by ISG-06 Tier 3 are listed in Table 1.

Table 1 MELTAC V&V Documents Corresponding to Documents in ISG-06 Enclosure B Tier 3 (1 / 3)

ISG-06 Enclosure B Tier 3 Document		Applicable ISG-06 Section	MELTAC V&V Documents		
			No.	Document Title in SPM	Document Title at MELCO ESC
1.9	Software V&V Plan (SVVP)	D.4.4.1.10	1	V&V Task Manual (Note1)	Software V&V Plan
2.2	V&V Reports	D.4.4.2.2	2	V&V Summary Report	V&V Task Report
			3	Task-specific documents and reports	V&V Report
			4	Final V&V Report	V&V Final Report
			5	Regression Analysis Report	Regression Analysis Report
2.4	Test Design Specification	D.4.4.2.4	6	Unit V&V Test Description	Unit Test Specification
			7	Unit V&V Test Specification	

Table 1 MELTAC V&V Documents Corresponding to Documents in ISG-06 Enclosure B Tier 3 (2 / 3)

ISG-06 Enclosure B Tier 3 Document		Applicable ISG-06 Section	MELTAC V&V Documents		
			No.	Document Title in SPM	Document Title at MELCO ESC
2.4	Test Design Specification	D.4.4.2.4	8	Integration V&V Test Description	Integration Test Specification
			9	Integration V&V Test Specification	
2.5	Summary Test Reports	D.4.4.2.4	10	Test Phase V&V Summary Report	Integration V&V Task Report
2.6	Summary of Test Results	D.4.4.2.4	11	Test Phase V&V Summary Report	Integration V&V Task Report
2.7	Requirement Traceability Matrix	D.9.4.2	12	Requirement Traceability Matrix (RTM)	Requirement Traceability Matrix (RTM)
3.1	Software Integration Report	D.4.4.1.4 D.4.4.2.2	13	Integration V&V Test Report	Integration Test Report
3.2	Individual V&V Problem Reports up to FAT	D.4.4.2.2	14	V&V Anomaly Report	V&V Anomaly Report
3.3	Configuration Management Reports	D.4.4.2.3	15	Configuration Management Sheet	Configuration Management Sheet (V&V)
3.4	Test Procedure Specification	D.4.4.2.4	16	Unit V&V Test Specification	Unit Test Specification

Table 1 MELTAC V&V Documents Corresponding to Documents in ISG-06 Enclosure B Tier 3 (3 / 3)

ISG-06 Enclosure B Tier 3 Document		Applicable ISG-06 Section	MELTAC V&V Documents		
			No.	Document Title in SPM	Document Title at MELCO ESC
3.4	Test Procedure Specification	D.4.4.2.4	17	Integration V&V Test Specification	Integration Test Specification
3.5	Completed Test Procedures and Reports	D.4.4.2.4 D.5.2	18	Unit V&V Test Report	Unit Test Report
			19	Integration V&V Test Report	Integration Test Report
3.6	Test Incident Reports	D.4.4.2.4	20	V&V Anomaly Report	V&V Anomaly Report

(Note1) “V&V Task Manual” is the document that specifies project-specific items, such as schedule, organization, and cost, when performing a specific project. MELCO ESC refers to this document as Project-specific SVVP.

4.0 MELTAC PLATFORM V&V / TESTING ACTIVITIES AND DOCUMENTS

The details of MELTAC platform V&V activities and the corresponding documents are described in sections 3.10 “Software Verification and Validation Plan” and 3.12 “Software Test Plan” of the “MELTAC Platform Software Program Manual” (JEXU-1041-1016).

The details of MELTAC platform configuration management activities and the corresponding documents are described in section 3.11 “Software Configuration Management Plan” of the “MELTAC Platform Software Program Manual” (JEXU-1041-1016).

The details of MELTAC platform testing activities (not related to software) and the corresponding documents are described in MELCO ESC procedures as follows.

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5.0 SUMMARY OF V&V RESULT

This section shows the summary of V&V activities, their results and associated lifecycle phase.

Table 2 V&V Activity and Result

No.	V&V Activity and Result	Lifecycle Phase
1	Basic Design The V&V Team verified the System Specification from the following viewpoints using the System Specification V&V Checklist specified in ESC Procedure N. **[** **]** As a result, the V&V Team found no problem that requires a V&V Anomaly Report and issued a V&V Task Report*.	Requirements
2	Software Design The V&V Team verified the Software Specification from the following viewpoints using the Software Specification V&V Checklist specified in ESC Procedure N. **[** **]** As a result, the V&V Team found no problem that requires a V&V Anomaly Report and issued a V&V Task Report.	Design
3	Software Design The V&V Team verified the Hardware Specification from the following viewpoints using the Hardware Specification V&V Checklist specified in ESC Procedure N. **[** **]** As a result, the V&V Team found no problem that requires a V&V Anomaly Report and issued a V&V Task Report.	Design

No.	V&V Activity and Result	Lifecycle Phase
4	Program Design The V&V Team verified the Program Specification from the following viewpoints using the Program Specification V&V Checklist specified in ESC Procedure N. **[** **]** As a result, the V&V Team issued V&V Anomaly Reports to the design team. After receiving the response from the design section, the V&V Team performed additional checks and confirmed that the anomalies were resolved. Since there were no outstanding anomalies, the V&V Team issued a V&V Task Report.	Design
5	Program Design The V&V Team verified the FPGA Specification from the following viewpoints using the FPGA Specification V&V Checklist specified in ESC Procedure N. **[** **]** As a result, the V&V Team found no problem that requires a V&V Anomaly Report and issued a V&V Task Report.	Design

No.	V&V Activity and Result	Lifecycle Phase
6	<u>Coding</u> The V&V Team verified the source code from the following viewpoints using the Source Code V&V Checklist specified in ESC Procedure N. **[** **]** As a result, the V&V Team found no problem that requires a V&V Anomaly Report and issued a V&V Task Report.	Implementation
7	<u>Coding</u> The V&V Team verified the FPGA source code from the following viewpoints using the Source Code V&V Checklist specified in ESC Procedure N. **[** **]** As a result, the V&V Team found no problem that requires a V&V Anomaly Report and issued a V&V Task Report.	Implementation
8	<u>Software Unit Test</u> **[** **]** After receiving the response from the design section, the V&V Team performed additional checks and confirmed that the anomalies were resolved. Since there were no outstanding anomalies in the test results, the V&V Team issued Unit Test Reports and a V&V Task Report.	Implementation

No.	V&V Activity and Result	Lifecycle Phase
9	Software Unit Test **[** **]** After receiving the response from the design section, the V&V Team performed additional checks and confirmed that the anomalies were resolved. Since there were no outstanding anomalies in the test results, the V&V Team issued FPGA Unit Test Reports and a V&V Task Report.	Implementation
10	Integration Test The V&V Team performed integration test as specified in the Integration Test Specification, based on the System Specification, and issued V&V Anomaly Reports to the design team during the integration test. After receiving the response from the design section, the V&V Team performed additional checks and confirmed that the anomalies were resolved. Since there were no outstanding anomalies in the test results, the V&V Team issued an Integration Test Report and a V&V Task Report.	Test

* Corresponding to “V&V Activity Summary Report” in IEEE 1012 (see Table B-1 in Appendix B of this document).

APPENDIX A

MELTAC Platform V&V documents are listed.

(1) Software V&V Plan (Document type : No.1 of Table 1)

(2) V&V Report (System Specification) (Document type : No.3 of Table 1)

(3) V&V Task Report (System Specification) (Document type : No.2 of Table 1)

(4) V&V Report (Hardware Specification) (Document type : No.3 of Table 1)

(5) V&V Task Report (Hardware Specification) (Document type : No.2 of Table 1)

(6) V&V Report (Software Specification) (Document type : No.3 of Table 1)

(7) V&V Task Report (Software Specification) (Document type : No.2 of Table 1)

(8) V&V Report (FPGA Specification) (Document type : No.3 of Table 1)

(9) V&V Task Report (FPGA Specification) (Document type : No.2 of Table 1)

(10) V&V Report (Program Specification) (Document type : No.3 of Table 1)

(11) V&V Task Report (Program Specification) (Document type : No.2 of Table 1)

(12) V&V Report (FPGA Source code) (Document type : No.3 of Table 1)

(13) V&V Task Report (FPGA Source code) (Document type : No.2 of Table 1)

(14) V&V Report (Source code) (Document type : No.3 of Table 1)

(15) V&V Task Report (Source code) (Document type : No.2 of Table 1)

(16) Unit Test Specification(FPGA Software) (Document type : No.6 and 7 of Table 1)

(17) Unit Test Specification(Software) (Document type : No.6 and 7 of Table 1)

(18) Unit Test Report(FPGA Software) (Document type : No.18 of Table 1)

(19) Unit Test Report(Software) (Document type : No.18 of Table 1)

(20) V&V Task Report (FPGA Software Unit Test) (Document type : No.2 of Table 1)

(21) V&V Task Report (Software Unit Test) (Document type : No.2 of Table 1)

(22) Integration Test Specification (Document type : No.8 and 9 of Table 1)

(23) Integration Test Report (Document type : No.13 of Table 1)

(24) V&V Task Report (Integration Test) (Document type : No.10 of Table 1)

(25) V&V Anomaly Report (Document type : No.14 of Table 1)

(26) V&V Final Report (Document type : No.3 of Table 1)

APPENDIX B

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Table B-1 Correspondence of Document Titles Between IEEE1012 and MELTAC SPM/MELCO QAP

Table B-2 Title of V&V Output Document of Each Phase (on ESC Procedure N) (1 / 7)

Table B-2 Title of V&V Output Document of Each Phase (on ESC Procedure N) (2 / 7)

Table B-2 Title of V&V Output Document of Each Phase (on ESC Procedure N) (3 / 7)

Table B-2 Title of V&V Output Document of Each Phase (on ESC Procedure N) (4 / 7)

Table B-2 Title of V&V Output Document of Each Phase (on ESC Procedure N) (5 / 7)

Table B-2 Title of V&V Output Document of Each Phase (on ESC Procedure N) (6 / 7)

Table B-2 Title of V&V Output Document of Each Phase (on ESC Procedure N) (7 / 7)