NRW-FPGA-Based PRM System Qualification Project

Document Title
Verification and Validation Plan

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**Independent Reviewer**

(Sign & Date)

Toshiba

April 23, 2007
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1 Purpose

This Verification and Validation (V&V) plan is prepared by Toshiba Nuclear Energy Systems & Services Division (NED) for the NRW-FPGA (Non-Rewritable Field Programmable Gate Array) -Based Power Range Monitor (PRM). This plan has the following purposes:

(1) This V&V plan (VVP) specifies V&V activities performed by NED and Toshiba Nuclear Instrumentation & Control Systems Dep. (NICSD).

(2) This VVP defines the envelope of the NICSD VVP.

For the V&V of NRW-FPGA-Based PRM System, NICSD shall prepare its own VVP describing their V&V activities in detail.


TOSHIBA CORPORATION
Nuclear Energy Systems & Services Division
2 Reference Documents

2.1 Code of Federal Regulations

This VVP does not refer to the Code of Federal Regulations (CDR) directly, but does indirectly through the TOSHIBA internal standards in section 2.4.

2.2 Regulatory Guides and NRC Documents


Other regulatory guides and NRC documents are referenced through the TOSHIBA internal standards in section 2.4.

2.3 Industry Standards and EPRI Reports

2.3.1 IEEE Std 1012-1998, "IEEE Standard for Software Verification and Validation"

2.3.2 IEEE Std 829-1983, "IEEE Standard for Software Test Documentation"

2.3.3 IEEE Std 7.4.3.2-1993, "IEEE Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations"

2.4 Toshiba Internal Documents

2.4.1 AS-200A002, "Design Verification Procedure"

2.4.2 AS-200A005, "Design Review Meeting Convening Standard"
2.4.3 AS-200A010, “Control Procedure of vendor generated documents”
2.4.4 AS-200A015, "Design Change Control Procedure"
2.4.5 AS-200A128, “Digital System Life Cycle Procedure”
2.4.6 AS-200A129, “Digital System Development Procedure”
2.4.7 AS-200A130, “Digital System Verification & Validation Procedure”
2.4.8 AS-200A131, “Digital System Configuration Management Procedure”
2.4.9 AS-200A132, “Digital System Safety and Hazards Analysis Procedure”
2.4.10 AS-300A006, “Nonconformance Control Procedure for Procured Items and Services”
2.4.11 AS-300A008, “Nonconformance Control and Corrective Action Procedure”
2.4.12 AS-300A103, “Test Control Procedure”
2.4.13 P-101, “NICSD Manufacture of FPGA-Based Equipment”
2.4.14 FPG-PLN-A70-0001, Project Quality Assurance Plan
2.4.15 FPG-PLN-C51-0002, Software Quality Assurance Plan
2.4.16 FPG-RQS-C51-0001, Equipment Requirement Specification
2.4.17 FPG-PRD-A11-0002, Master Engineering Schedule
2.4.18 FPG-DRT-C51-0002, Preliminary Hazard Analysis Report
2.4.19 NICSD D-68016, “NICSD Procedural Standard for FPGA Products Development”
2.4.20 NICSD D-68017, “NICSD Procedural Standard for FPGA Device Development”
2.4.21 NICSD D-68018, “NICSD Procedural Standard for Functional Element Development”
2.4.22 NICSD D-68019, “NICSD Procedural Standard for FPGA Configuration Management”
2.4.23 NICSD D-68020, “NICSD Procedural Standard for Control of Software Tools Used with FPGA Based Systems”
2.4.24 NICSD D-67003, "NICSD Procedural Standard for Software Media Registration and Change"

Notice: Upon application of above NED, NICSD and other Toshiba internal standards, the latest version shall be used.
3 Definitions and Abbreviations

3.1 Definitions

**Functional Element (FE):** A Functional Element is a component of digital logic that shall be completely verified and validated through full pattern tests. i.e. tests that are performed for every possible input combination. An FE is written in Very High Speed Integrated Circuit Hardware Definition Language (VHDL). All VHDL source for the NRW-FPGA-Based PRM System shall solely consist of FEs and interconnects between FEs.

**hazard:** A source of potential harm or a situation with a potential for harm in terms of human injury, damage to health, property, or the environment, or some combination of these (Reference 2.3.1).

**module:** A part of a unit. Modules have the specific functions, for example, circuit board(s), AC-DC converter, connector assembly etc. See unit.

**Netlist:** Description of logics created by the logic synthesis tool. A design engineer describes FPGA logic in the form of VHDL source codes. The logic synthesis tool converts the VHDL source code into forms of digital circuits and outputs the resulting circuit in the form of a Netlist. The layout tool transforms the Netlist into physical placement of interconnects on the FPGA, which are represented as an FPGA fuse-map.

**unit:** NRW-FPGA-Based PRM System consists of the LPRM units, the LPRM/APRM units, and the FLOW units. Each unit is a drawer type chassis which houses the individual plug-in modules.

**validation:** Confirmation by examination and provisions of objective evidence that the particular requirements for a specific intended use are fulfilled. The process of evaluating a system or component during or at the end of the development process to determine whether it satisfies specified requirements.

**verification:** Confirmation by examination and provision of objective evidence that specified requirements have been fulfilled. The process of evaluating a system or component to determine whether the products of a given development phase satisfy the conditions imposed at the start of that phase.

3.2 Abbreviations

**APRM:** Average Power Range Monitor
DRS: Document Review Sheet
DVR: Design Verification Report
EDIF: Electronic Design Interchange Format
ERS: Equipment Requirement Specification
FPGA: Field Programmable Gate Array (a programmable logic device)
ICDD: Control & Electrical Systems Design & Engineering Department
IPSNE: Toshiba Corporation, Industrial and Power Systems & Services
Company, Nuclear Energy
IR: Independent Reviewer
LPRM: Local Power Range Monitor
MCL: Master Configuration List
NED: Nuclear Energy Systems and Services Division
NICSD: Nuclear Instrumentation & Control Systems Department
NRW-FPGA: Non-Rewritable Field Programmable Gate Array
PHA: Preliminary Hazard Analysis
PRM: Power Range Monitor
PRS: Problem Reporting Sheet
QA: Quality Assurance
RTM: Requirements Traceability Matrix
SCSI: Small Computer System Interface
SDD: Software Design Description
SER: Safety Evaluation Report
SIL: Software Integrity Level
SOAP: Software Quality Assurance Plan
SRS: Software Requirements Specification
VHDL: Very High Speed Integrated Circuit Hardware Definition Language (A hardware description language that defines the FPGA circuit)
V&V: Verification and Validation
VVP: Verification and Validation Plan
VVR: Verification and Validation Report
4 Verification and Validation Overview

4.1 Organization

The NRW-FPGA-Based PRM System Software Quality Assurance Plan (SQAP) (Reference 2.4.15) describes the V&V Team organization. Figure 4-1 is excerpted from the SQAP and depicts the NED V&V Team organization.

Both design and V&V activities shall be performed by Control & Electrical Systems Design & Engineering Dept. (ICDD). However, as shown in the figure above, the Monitoring System Engineering Group (which consists of the Design Engineers lead by the Group Manager) shall perform design activities, and the V&V team (that is independent from the Design Engineers) shall perform V&V activities which require independence.

NICSD shall describe its V&V organization in the NICSD VVP.

* The V&V team consists of persons who belong to the Control & Electrical Systems Design & Engineering Department, and who are independent from the Monitoring System Engineering Group with separate cost, schedule and resources.

Figure 4-1 NED Organization associated with this Plan
4.2 Master Schedule

Activities described in this VVP shall be performed according to the Master Engineering Schedule (Reference 2.4.17) that was established by NED at the beginning of the NRW-FPGA-Based PRM System Qualification Project (FPGA/SER Project).

For the V&V activities performed by NICSD, NICSD shall establish its master schedule based on NED’s Master Engineering Schedule. NICSD shall provide its schedule to NED with the NICSD VVP (See section 5.2).

4.3 Software Integrity Level Scheme

The software integrity level (SIL) scheme shall be determined based on Table A-1 of AS-200A129 Digital System Development Procedure (Reference 2.4.6), which is considered to be equivalent to the Appendix B of IEEE Std 1012 (Reference 2.3.1).

The SIL shall be 4 for the PRM safety software and 3 for the PRM non-safety software as documented in the Appendix A of the SQAP. Note that all the V&V activities defined in section 5 shall be applied for both SIL-3 and SIL-4 PRM software.

4.4 Resource Summary

The Senior Manager of ICDD of NED shall assign appropriate persons for the V&V team to perform the NED V&V activities. The V&V team members shall meet the following restrictions:

- Be independent of the design activities in schedule, cost, and resource.
- Be technically qualified for the work performed.

NICSD shall assign appropriate persons for the NICSD V&V team to perform the NICSD V&V activities. NICSD shall state more detail about the resources for activities in the NICSD VVP. The NICSD V&V team members shall meet the following restrictions:

- Be independent of the design activities in schedule, cost, and resource.
- Be technically qualified for the work performed.

The NICSD Senior Manager or a Group Manager who is independent of the design activities shall be responsible for the assignment of the NICSD V&V team members.

This VVP includes some special procedural requirements to NICSD. NICSD shall prepare necessary resources including facilities and tools in order to meet the requirements.
4.5 Responsibilities

For the NED part of the V&V activities, the responsibilities of the V&V activities are defined in AS-200A130 Digital System V&V Procedure (Reference 2.4.7) as follows:

The Preparer(s) of documentation of V&V activities must:
- Be in the V&V team which is independent of the Engineering/Design Group that has responsibility for the software development activities, with separate cost, schedule and resources.
- Not have contributed to the design.
- Be technically qualified for the work performed.

The Independent Reviewer of documentation of V&V activities must:
- Be in the V&V team which is independent of the Engineering/Design Group that has responsibility for the software development activities, with separate cost, schedule and resources.
- Not have contributed to the design.
- Be independent of the Preparer of the V&V Activity Output Document (that is, the Independent Reviewer must not have collaborated on the preparation of the document).
- Be technically qualified for the work being reviewed.

The independent review of documentation of V&V activities, as well as design documentation, shall be performed by V&V personnel. As shown in Figure 4-1 the V&V personnel are independent of the Monitoring System Engineering Group.

All safety related development documents must also be approved in writing prior to use. The Approver is usually the Group Manager.

For the Preparer, the Independent Reviewer, and the Approver for specific documents, Table 3 of ICDD P-101 (Reference 2.4.13) shall be applied.

For the NICSD part of the V&V, NICSD shall assign NICSD V&V team for the NICSD V&V activities. The responsibilities of the Preparer, the Independent Reviewer, and the Approver of NICSD must be equivalent to those of NED stated above.

The NICSD V&V team shall be responsible for the following activities:
- Establishing the NICSD VVP
- Independent review of design documents
- Reviewing the Requirements Traceability Matrix (RTM) that is prepared based on the concept phase RTM, which is to be received from NED.
- Issuing the NICSD V&V report (VVR) at the end of each V&V phase.

The NICSD V&V team shall submit the NICSD VVP and NICSD VVRs to the NED V&V team without delay. The NED V&V team reviews those documents to determine whether they are acceptable for NED. If those documents are not acceptable, the NED V&V team...
shall prepare Nonconformance Notice Report (NNR) in accordance with the SQAP (Reference 2.4.15).

NED V&V personnel may also perform witness activities on the works of NED and NICSD design engineers to verify that they are working in compliance with applicable internal standards. For NICSD design engineers, they are required to work in accordance with the special provisions from NED, especially provisions to avoid security risks. Results of these reviews if necessary, shall be documented in NED’s VVR for each phase..

4.6 Tools, Techniques, and Methodologies

For tools, techniques, and methodologies, refer to Section 9 of the SQAP. The following is additional information about the tools that NICSD uses for its V&V activities:

1. Synplify Tool
   The Synplify tool synthesizes logic from VHDL source codes and produces Netlists. As by-products of logic synthesizing, Synplify performs syntactic check of the VHDL source codes and adequacy check of the synthesized logic.

2. Netlist Viewer tool
   The Netlist Viewer tool depicts the logic block diagrams according to the Netlists. The Netlist Viewer tool is used to inspect the Netlist to ensure the correct conversion of the logic, i.e. ensure that functional elements (FEs) are correctly connected in the Netlists. The Netlist Viewer tool is integrated as a function in the Actel Libero tool, which is an FPGA development package. (See 5.5.2)

3. Designer tool
   The Designer tool is a layout tool. It converts gate-level Netlists into a Fuse Map file. To generate the Fuse Map file, the Designer tool determines which cells in an FPGA chip are to be used, and makes connections to obtain the desired circuit defined by the Netlist. The Designer tool is used to generate the gate-level delay information.

4. ModelSim tool
   ModelSim tool is used for simulation of an FPGA using the gate-level Netlists and gate-level delay information generated by Designer tool, for generation of test signals for the PinPort device to test FPGAs, and for measurement of the toggle coverage rate for given test vectors.

5. Silicon Sculptor tool
   Silicon Sculptor tool embeds Fuse Maps generated by the Designer tool on the FPGA chips.

6. PinPort device
   The PinPort device has a small computer system interface (SCSI), which is connected by an SCSI cable to a personal computer containing the ModelSim tool.
For each test, the ModelSim tool generates inputs to, and monitors outputs from, the FPGA chip. For this testing, the FPGA chip is mounted in a socket in the PinPort device.

NICSD shall use these tools in accordance with NICSD procedure D-68020 (Reference 2.4.23). In addition, NICSD shall prepare an appropriate procedure meeting the requirements in section 3.2.3 of SQAP, in particular personnel training to use the tools. The procedure can be prepared as a part of the NICSD VVP.

NICSD may use test equipment for the validation testing of Units/Modules. This equipment includes a signal generator and a data recorder. The signal generator generates inputs to the Units/Modules, while the data recorder records outputs from the Units/Modules. To control the signal generator and the data recorder, test equipment software may be used.

To develop new test equipment software, or use legacy software, NICSD shall follow the SQAP including the requirements for configuration management, and D-68020. NICSD shall explain the V&V activities associated with the use of their tools in the NICSD VVP.

NED shall assess the controls of the tools and test equipment software as a V&V activity. See section 5.5.6, 5.6.4, and 5.7.4.

For system validation testing, NED may use test equipment software similar to that used for Unit/Module testing. To develop new equipment software, or use legacy software, NED shall follow the SQAP including the requirements for configuration management. Specifically:

- For newly developed test equipment software, NED shall follow the life cycle approach in accordance with AS-200A128 through AS-200A132. The SIL shall be 2 for the software, and the scope and rigor of V&V for the software are determined in accordance with SIL 2. The developed software shall be controlled under the configuration management requirements of section 10 of the SQAP.

- For legacy test equipment software, NED shall perform the following activities for the software:
  - Define the Test Equipment software functions required in the project.
  - Establish the equipment software acceptance criteria.
  - Establish the procedure to use the equipment software. This procedure includes the methods to record errors in accordance with the configuration management process.
  - Perform hazard analysis to ensure that the software causes no harm to the product.
  - Train the personnel to use the test equipment software.

Section 5.5 of SQAP defines the metrics that should be maintained for each NRW-FPGA-Based PRM system.
5 Verification and Validation Activities for This Project

(1) Management of V&V

IEEE Std 1012 (Reference 2.3.1) defines tasks for the management of V&V. Table 5-1 shows the corresponding activities in the project.

<table>
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<th>Task defined in IEEE Std 1012</th>
<th>Activity in this VVP</th>
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<tr>
<td>1) Software Verification and Validation Plan (SVVP) Generation</td>
<td>Establishment of this VVP</td>
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<tr>
<td>2) Baseline Change Assessment</td>
<td>The configuration management activities in section 5.10 covers the requirements of the Baseline Change Assessment</td>
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<tr>
<td>3) Management Review of V&amp;V</td>
<td>V&amp;V personnel shall review the V&amp;V efforts at the end of each V&amp;V phase, and summarize the results in the VVR.</td>
</tr>
<tr>
<td>4) Management and Technical Review Support</td>
<td>V&amp;V personnel shall attend the design review meetings, which is prescribed in AS-200A005 (Reference 7), for management and technical support, if necessary.</td>
</tr>
<tr>
<td>5) Interface With Organizational and Supporting Processes</td>
<td>V&amp;V personnel shall attend the project meeting to coordinate V&amp;V effort with organizational and supporting processes.</td>
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(2) V&V Phases

Required V&V activities for the NWR-FPGA-Based development are defined in AS-200A130 “Digital System Verification & Validation Procedure” (Reference 2.4.7).

ICDD P-101 (Reference 2.4.13) describes how the requirements of the AS-200A128 (Reference 8) through AS-200A132 (Reference 2.4.9) are to be implemented in the development and procurement of FPGA-based systems from NICSD.

P-101 decomposes the V&V phases in AS-200A130 to the following, as shown in Figure 5-1:

(1) Project Planning and Concept Definition phase
(2) Requirements Definition phase
(3) Design phase
(4) Implementation and Integration phase
(5) Unit/Module Validation Testing phase
(6) System Validation Testing phase
(7) Operation and Maintenance (O&M) phase.
In addition, P-101 prescribes which parts NED shall perform and which parts NICSD shall perform. Further information for V&V activities for each phase is described in the following sections. In this project, the O&M phase is considered to correspond to the qualification testing phase. Note that the scope of this VVP does not include the O&M phase.

The following sections, V&V inputs and outputs are defined for each V&V phase. The source and format of the inputs and outputs are defined in relevant NED and NICSD standards.

### 5.1 Project Planning and Concept Definition Phase

NED V&V personnel shall perform all Project Planning and Concept Definition Phase (Concept Phase) V&V activities.

**V&V Inputs:**

1. ERS (Review Document) (Reference 2.4.16)
2. SQAP (Review Document) (Reference 2.4.15)

**V&V Outputs:**

1. VVP (This document)
2. Document Review Reports
3. Project Planning and Concept Definition Phase RTM
4. Project Planning and Concept Definition Phase VVR
5.1.1 Preparation of VVP
NED V&V personnel shall prepare NED VVP in accordance with AS-200A130 and the SQAP.

5.1.2 Document Reviews
NED V&V personnel shall perform an independent review of the following documents for completeness, correctness, consistency, and accuracy:
- SQAP, including the Project Specific Configuration Management Plan.
- Equipment Requirement Specification (ERS)
- Preliminary Hazard Analysis Report (PHA)
- VVP (This document)
- Concept Phase RTM
- Concept Phase VVR

Note that the section 6 of the SQAP states the reviews for the ERS and VVP, and Appendix A of the SQAP defines the SIL applied to the PRM Systems.

All documents listed above will be independently reviewed. The results of the document review shall be documented in accordance with AS-200A002 (Reference 2.4.1) if the document includes design, otherwise they may be documented using the DRS that is the exhibit of P-101.

For the review of the RTM, the Independent Reviewer shall review to ensure all entries made contain sufficient detail, complete and unambiguous.

5.1.3 Project Planning and Concept Definition Phase RTM effort
(1) Preparation of the RTM
NED design engineer shall prepare the Project Planning and Concept Definition Phase RTM, to track implementation of requirements.

The requirements shall be taken from the input documents of the Project Planning and Concept Definition, which are listed as “input” at the beginning of this section.

All the requirements entered in the RTM shall be collected and compiled by the RTM Preparers. The entries in the RTM should be limited to requirements which are verifiable (testable or measurable) but must completely cover all the functionality of the product under development.

The Preparer shall summarize any open items revealed by the RTM effort. The Design/Engineering Group must resolve these items to the satisfaction of the RTM Preparer and the Reviewer.

(2) Compilation of the Project Planning and Concept Definition Phase RTM report
NED design engineer shall prepare and release the Project Planning and Concept Definition Phase RTM report for internal use, with a summary of open items revealed by the RTM effort.
5.1.4 Concept Phase VVR
NED V&V personnel shall produce this VVR including:
   (1) References to the reviewed documents.
   (2) References to the DVRs.
   (3) Reference to the Concept Phase RTM.
   (4) Any findings, recommendations, or suggestions to reduce any risks identified in
       the V&V activities.

5.2 Establishment of NICSD V&V Plan
The NICSD V&V team shall establish its own VVP conforming to the NED VVP (this
document) and submit the NICSD VVP to the NED V&V team in accordance with
AS-200A010 (Reference 2.4.3). The NED V&V personnel shall review the NICSD VVP
to assure that the Plan meets the requirements of the NED VVP. The review shall be
performed in accordance with section 6.4 of the SQAP. The NED V&V Team shall notify
NICSD in writing about the results of this review and whether the NICSD VVP is
acceptable. The Group Manager of the Monitoring System Engineering Group shall approve
the NICSD VVP based on the review.

The NICSD VVP may be written in Japanese.

5.3 Requirements Definition Phase
NICSD shall perform the Requirements Definition Phase (Requirements Phase) V&V
activities in accordance with the NICSD VVP. In addition, NED V&V personnel will
perform the independent review of the updated PHA, and prepare an NED Requirement
Phase VVR. This section states the minimum requirements for the NICSD VVP, which
shall specify the details of the NICSD V&V activities.

V&V Inputs:
   (1) ERS (Base Document)
   (2) Project Planning and Concept Definition Phase RTM (Base Document)
   (3) Unit/Module Design Specifications (Review Document)
   (4) NICSD Requirements Phase VVR (Review Document)
   (5) PHA Report (Review Document)

V&V Outputs:
   (1) Document Review Reports (by NICSD and NED)
   (2) Requirements Definition Phase RTM (by NICSD)
   (3) Requirements Phase VVR (by NED)

5.3.1 Document Reviews
The NICSD V&V team shall perform the following independent reviews:
Review of the Software Requirements Specification (SRS) included in the Unit Design
Specifications and Module Design Specifications, for completeness, correctness, consistency,
and accuracy. The review includes a check that the requirements are unambiguous, testable
or observable, and that the requirements provide acceptance criteria or acceptable ranges of values. The functional requirements, interface requirements and functional allocation written in the SRS shall be reviewed.

The reviewers shall document results of the review in accordance with NICSD D-68016 (Reference 2.4.19).

The NED V&V personnel shall independently review the Requirements Definition Phase PHA; and document the results of the review in accordance with AS-200A002.

5.3.2 Requirements Definition Phase RTM effort

(1) Preparation of Requirements Phase RTM

NICSD design engineer shall generate the Requirement Definition Phase RTM to trace the requirements collected during the Concept Phase RTM effort to the requirements in the Unit/Module Design Specifications.

The NICSD V&V team shall independently review this RTM, and verify the following:

- The requirements are traceable “forwards” from the base requirements (from the Concept Phase RTM) to the SRS; that is, that all the requirements from the Concept Phase appropriately correspond to the functions described in the Unit/Module Design Specifications. In addition, the SIL requirements from the Concept Phase are addressed in the SRS.

It should be noted that since NED prepares the ERS based on the vendor package, the requirements in the Concept Phase RTM should be consistent with those in the SRS.

- The requirements are traceable “backwards” from the SRS to the Concept Phase. That is, all the requirements listed in the SRS are covered by the Concept Phase requirements, and no new requirements have been created in the Unit/Module Design Specification.

The NICSD Design Group and V&V team shall report any open items or nonconformance items revealed by the Requirements Definition Phase RTM effort. The report shall be issued to NED in accordance with AS-300A006 (Reference 2.4.10)

The NICSD VVP shall specify the method to track the completion of open items.

(2) Compilation of the Requirements Definition Phase RTM report

NICSD shall compile the Requirements Definition Phase RTM report. The RTM report must include the RTM, how each requirement is addressed in the Unit/Module Design Specifications, the open items, and any resolutions to the open items.

5.3.3 Issuance of the Requirements Definition Phase V&V Report

The NICSD V&V team shall issue the NICSD Requirements Definition Phase VVR. The report includes:

(1) Copies of or references to Document Reviews.
(2) Reference to the Requirements Definition Phase RTM
(3) Any findings, recommendations, or suggestions to reduce risks identified in the V&V activities.

NED V&V personnel shall establish the Requirements Definition Phase VVR based on the NICSD VVR. The report includes any findings, recommendations, or suggestions to mitigate any V&V risks in this phase. The NICSD VVR shall be attached to the NED VVR.

5.4 Design Phase

In the design phase, NICSD produces the FPGA Design Specifications including the Software Design Description (SDD) for each FPGA. Because FPGAs are independent from each other, most of the activities in this phase and the implementation phase can be performed independently.

NICSD shall perform the Design Phase V&V in accordance with the NICSD VVP. In addition, NED V&V personnel will perform the independent review of the updated PHA, and prepare an NED Design Phase VVR. This section states the minimum requirements for the NICSD VVP, which shall specify the details of the NICSD V&V activities.

It should be noted that the logic design is made using FEs and interconnects between FEs. All the FEs used in design are registered in the FE library through the life-cycle activities defined in the NICSD procedure D-68018 (Reference 2.4.21).

V&V Inputs:
(1) Unit/Module Design Specifications (Base Document)
(2) Requirements Definition Phase RTM (Base Document)
(3) FPGA Design Specification (Review Document)
(4) PHA Report (Review Document) (Reference 2.4.18)

V&V Outputs:
(1) Document Review Reports (by NICSD and NED)
(2) Design Phase RTM (by NICSD)
(3) NICSD Design Phase VVR (by NICSD)
(4) Design Phase VVR (by NED)

Note: NICSD V&V activities for FEs are described separately in Section 5.8.

5.4.1 Document Reviews

The NICSD V&V team shall perform an independent review of the SDD included in the FPGA Design Specifications for completeness, correctness, consistency, and accuracy. The FPGA design shall comply with the design rules of FPGA logic in Appendix A of NICSD procedure D-68017 (Reference 2.4.20). The special instruction to be applied in the review is that the logic of FPGA shall be constructed of previously tested FEs, and the interface to each FE shall be consistent with that specified in FE specifications.

The review includes the check of FE documents. (See section 5.8.)
The reviewers shall document results of the review in accordance with NICSD D-68016.

The NED V&V personnel shall independently review the Design Phase PHA, and document the results of the review in accordance with AS-200A002.

5.4.2 Design Phase RTM effort

(1) Preparation of Design Phase RTM

NICSD shall perform the Design Phase RTM effort to trace the design as documented in the FPGA Design Specifications to the Requirements Phase RTM effort.

The NICSD V&V team shall independently review this RTM, and verify the following:
- The requirements are traceable “forwards” from the base requirements in the Requirements Phase to the FPGA Design Specifications; that is, each FPGA in the FPGA Design Specifications addresses the functions and interfaces of the FPGA requirements described in the Module Design Specifications. In addition, the SIL requirements from the Requirements Phase are addressed in the FPGA Design Specifications.
- The requirements are traceable “backwards” from the FPGA Design Specifications to the Requirements Phase.

The NICSD Design Group and V&V team shall report any open items revealed by the Design Phase RTM effort. The report shall be issued in accordance with the official document procedure of NICSD. The Design Group must resolve these items to the satisfaction of the RTM Preparer and the Reviewer. Any open items not resolved during this phase must be carried to the next phase.

The NICSD VVP shall specify the method to track the completion of open items.

(2) Compilation of the Design Phase RTM report

NICSD shall compile the Design Phase RTM report. The Design Phase RTM report must include the RTM, how each requirement is addressed in the FPGA Design Specifications, the open items, and any resolutions to the open items.

5.4.3 Issuance of Design Phase V&V Activities Report

NICSD shall issue the NICSD Design Phase VVR. The report includes:
(1) Copies of or references to Document Reviews.
(2) Copies of or references to the results of the checks of the FE document, the FE library control, and the software tool control. (See 5.8)
(3) Reference to the Design Phase RTM.
(4) Any findings, recommendations, or suggestions to reduce any risks identified in the V&V activities.

NED V&V personnel shall establish the NED Design Phase VVIR based on the NICSD VVR. The report includes any findings, recommendations, or suggestions to mitigate any V&V risks in this phase. The NICSD VVR shall be attached to the NED VVR.
5.5 Implementation and Integration Phase

NICSD shall perform the Implementation and Integration Phase (Implementation Phase) V&V in accordance with the NICSD VVP. In addition, NED V&V personnel will perform the independent review of the updated PHA, and prepare an NED Implementation Phase VVR. This section includes the minimum requirements for the NICSD V&V, which will specify the details of the NICSD V&V activities.

The development activities in the implementation and integration phase are divided into the following steps as illustrated in P-101.

- Step (1): VHDL Source Coding
- Step (2): FPGA Implementation
- Step (3): FPGA Validation

In step (1), NICSD design engineers generate VHDL source codes implementing the functional requirements from the SDD using editor tools. In the coding, verified functional elements (FEs) are used to implement specific logic steps. Although editor tools are software, errors in the editor tools are likely to be obvious to the NICSD design engineers.

In step (2), the VHDL source codes are compiled into gate-level Netlists by the Synplify tool. To verify that the gate-level Netlists are correctly converted, the Netlists are drawn in logic diagrams, and visually compared with the VHDL source codes. The gate-level Netlists are converted to Fuse Maps by the Actel Designer tool, then the NICSD design engineers embed the Fuse Maps into FPGA chips by the Silicon Sculptor tool. Test vectors used in step (3) and FPGA Validation test procedures are prepared in this step. The test vectors shall be prepared so that every operative connection between FEs is tested. More detailed explanation is described in section 5.5.2.

Note that “FPGA Validation test procedure” is equivalent to “FPGA Test Procedure” in NICSD procedure D-68017. Similarly, “FPGA Validation test report” is equivalent to “FPGA Test Report” in NICSD procedure D-68017.

In step (3), the NICSD design engineers test the FPGA chips with embedded Fuse Maps using the PinPort device and ModelSim tool. The ModelSim tool generates inputs to the FPGAs according to the test vectors, which are generated prior to the FPGA validation testing.

For steps (2) and (3), software tools are used where the results of software tool errors may not be obvious to the NICSD design engineers. So, the verification and testing are carefully considered.

The V&V in this phase includes activities (discussed below) to mitigate software tool errors, such as incorrect compilation of VHDL source codes, incorrect gate assignment, or faulty connections between FEs.

V&V Inputs:
(1) FPGA Design Specifications (Base Document)
5.5.1 VHDL Source Codes
The NICSD V&V team shall review the VHDL source codes for FPGA logics with the depth and intensity commensurate with the SIL of the source codes.
The review includes:
- Tracing the source code to the FPGA design specifications to verify correctness, consistency, completeness, and accuracy.
- Reviewing the source code for compliance with the design rules of FPGA logic in Appendix A of NICSD procedure D-68017.
In particular, the logic for the safety system FPGA must consist of combinations of the FEs. The review shall check to ensure that the interfaces between FEs are correct.

5.5.2 Logic Synthesis and Layout Verification
The NICSD design engineers use the Synplify tool to compile a VHDL source code to gate-level Netlists. A Netlist is stored in an EDIF (Electronic Design Interchange Format) file.
The Netlist Viewer tool integrated in the Actel Libero tool depicts logic diagrams according to the Netlist. The NICSD design engineers compare the original VHDL files with the logic diagrams to verify the correctness of the compilation. In the comparison, checks shall be made for the block connections and the FE interfaces. Note that FEs are seen as elementary logic blocks on the logic diagrams.
Since VHDL source codes implement logics using FEs, the Netlist includes “calls” for the FEs. The Designer tool integrates the Netlist file and the FE Netlists withdrawn from the FE library into a single Fuse Map.
The NICSD V&V team shall perform the verification, which includes:
1. Checking the message files produced by Synplify tool and Designer tool, to confirm that the logic synthesis and layout are performed normally. The software tool options and tool warning messages shall be checked.
2. Review the results of comparison between the logic block diagrams and VHDL files.
The NICSD VVP shall state the method to be used in performing the verification.

5.5.3 FPGA validation testing
FPGA validation testing shall be performed in accordance with NICSD procedure D-68017, using test purpose FPGAs that are prepared in the same manner as those FPGAs to be implemented in the modules.

The design engineers who perform FPGA testing shall prepare Problem Reporting Sheets (PRS) in accordance with NICSD procedure D-68017, to document any test failures, any product or configuration nonconformance, or any errors in the test procedure itself. The PRS shall be resolved by modifying design documentation, logic, or testing plans and procedures as necessary, revising all previous materials and performing reviews as necessary to incorporate the changes. NICSD shall document the amount of retest required for these changes, and shall perform retests as needed to resolve all PRSs.

5.5.4 Document Reviews
The NICSD V&V team shall perform an independent review of the following items:

(1) FPGA validation test procedures
Review the FPGA validation test procedures prepared by the NICSD Design Group for completeness, correctness, consistency, and accuracy. The FPGA Validation tests shall achieve 100% toggle coverage of the active FE connections using the toggle coverage scheme provided by the ModelSim tool.

The FPGA Validation tests shall be performed to assure that every operative connection between FEs is toggled. Note that not all connections in a FPGA can be toggled, because some connections are connected to ground level or power level directly.

NICSD shall evaluate the test coverage ratio, i.e. the number of toggled connections in the test to the number of operative connections, and confirm that the ratio achieves 100%.

In addition, experience has shown that 100% toggle testing may not fully test all connections between FEs. For example, in testing an OR gate that inputs signal A and B, and outputs signal X, toggling the signal A while the signal B is set to “1” has no meaning, since the signal X keeps “1” regardless of the signal A value. NICSD design engineers shall review the circuit performance using the Netlist Viewer tool to determine if additional tests are needed to check all connections. When needed, these additional tests are added to the test vector. The final test vector is fully verified to assure the completeness of the logic of the FPGA circuit design.

(2) FPGA validation test reports
After NICSD design engineers (who are independent of the design engineers of the FPGA product being tested as required by D-68016) will perform these tests, the NICSD V&V Team shall reviews the FPGA validation test reports to verify:
- The tests have been appropriately performed according to the test procedures.
• There are sufficient tests records, including the findings during the validation testing
• The tests results are acceptable.
• If above issues are not satisfied, the test shall be performed again.

(3) Software Baseline
The NICSD design engineers shall establish the Software Baseline after FPGA Validation Testing is finished. The NICSD V&V Team shall review the Software Baseline to confirm that the items required by the NICSD procedure D-68019 (Reference 2.4.22) have been appropriately established.

(4) Implementation Phase PHA
The NED V&V personnel shall independently review the Implementation Phase PHA, and document the results of the review in accordance with AS-200A002.

5.5.5 Implementation Phase RTM effort
(1) Preparation of Implementation Phase RTM
NICSD shall perform the Implementation Phase RTM effort to trace the FPGA validation test procedures to the preceding phases of the RTM effort.

The NICSD V&V team shall independently review this RTM, and verify the following:
• The requirements are traceable "forwards" from the base requirements to the FPGA; that is, that all the requirements in the Design Phase are correctly addressed in the FPGA validation test cases and the test results are acceptable.
• The requirements are traceable "backwards" from the FPGA validation procedures to the Design Phase.

(2) Compilation of the Implementation Phase RTM Report
• The Implementation Phase RTM report must include the RTM, how each requirement is addressed in the FPGA validation test procedures, the open items, and any resolutions to the open items.

5.5.6 Assessment of Software tools
NED V&V personnel shall assess the NICSD control of the software tools used in the design and V&V activities.

NED V&V personnel shall review NICSD's records for software tool control to ensure:
• FPGAs used for the project are manufactured using the correct tool versions.
• NICSD is controlling the software tools in accordance with procedures that NED has reviewed and approved.

NED may also perform in-process audits and witness activities to verify that NICSD is working in compliance with these controls and procedures. Results of these reviews, and audits if necessary, shall be documented in NED's VVR for this phase.
5.5.7. Issuance of Implementation Phase V&V Report

NICSD shall issue the NICSD Implementation Phase VVR. The report includes:

1. Copies of or references to Document Reviews.
2. Copies of or references to the source code reviews.
3. Copies of or references to the software tools message file checks.
4. Copies of or references to the logic block diagram checks.
5. Reference to the Implementation Phase RTM.
6. Any findings, recommendations, or suggestions to reduce risks identified in the V&V activities.

NED V&V personnel shall establish the Implementation Phase VVR based on the NICSD VVR. The report includes any findings, recommendations, or suggestions to mitigate any V&V risks in this phase. The NICSD VVR shall be attached to the NED VVR.

5.6 Unit/Module Validation Testing Phase

After the FPGA testing has finished, the validated FPGA logics are embedded into new FPGAs, which are soldered on the printed circuit boards. Finally, the printed circuit boards are assembled as the modules. NICSD shall perform Unit/Module Validation Testing Phase V&V in accordance with the NICSD VVP. In addition, NED V&V personnel will perform the independent review of the updated PHA, and prepare an NED Unit/Module Validation Testing Phase VVR. This section states the minimum requirements for the NICSD VVP, which will specify the details of the NICSD V&V activities.

V&V Inputs:
1. Module validation test procedures (Review Document, Base Document)
2. Unit validation test procedures (Review Document, Base Document)
3. Module validation test reports (Review Document)
4. Unit validation test reports (Review Document)
5. User Documentation for Unit and Module (Review Document)
6. Requirements Phase RTM (Base Document)
7. PHA Report (Review Document)

V&V Outputs:
1. Document Review Reports (by NICSD and NED)
2. Unit/Module Validation RTM (by NICSD)
3. NICSD Unit/Module Validation Testing Phase VVR (by NICSD)
4. Unit/Module Validation Testing Phase VVR (by NED)

5.6.1 Unit and Module validation testing

1. NICSD shall perform the Module validation testing and Unit validation testing by personnel who are independent of the Design Group. The tests shall be performed following the Module validation test procedures and Unit validation test procedures respectively. NICSD shall establish these test procedures prior to the testing.
2. NICSD shall prepare Problem Reporting Sheets (PRS) in accordance with NICSD procedure D-68016 (Reference 2.4.19), to document any test failures, any product or...
configuration nonconformance, or any errors in the validation test procedure itself. The NICSD Test Group shall forward the PRS to the NICSD Design Group for resolution. The PRS shall be resolved by modifying design documentation, logic, or testing plans and procedures as necessary, revising all previous materials and performing reviews as necessary to incorporate the changes. NICSD shall document the amount of retest required for these changes, and shall perform retests as needed to resolve all PRSs.

5.6.2 Document Reviews
(1) Module validation test procedures
The NICSD V&V team shall review the Module validation test procedures prepared by the NICSD design engineers for completeness, correctness, consistency, and accuracy.

(2) Unit validation test procedures
The NICSD V&V team shall review the Unit validation test procedures prepared by the NICSD design engineers for completeness, correctness, consistency, and accuracy.

(3) Module validation test reports
The NICSD design engineers shall prepare the Module validation test reports including the signed validation test procedures, and any PRSs written as results of the testing. The NICSD V&V personnel shall perform an independent review of the Module validation test reports. The validation test reports shall be prepared and reviewed in accordance with NICSD procedure D-68016. In this review, the Module validation test procedures are considered to be base documents.

(4) Unit validation test reports
The NICSD design engineers shall prepare the Unit validation test reports including the signed validation test procedures, and any PRSs written as results of the testing. The NICSD V&V personnel shall perform an independent review of the Module validation test reports and the Unit validation test reports. The validation test reports shall be prepared and reviewed in accordance with NICSD procedure D-68016. In this review, the Unit validation test procedures are considered to be base documents.

(5) User Documentation for Unit and Module
The NICSD design engineers shall prepare the Unit and Module user documentation, which includes the contents stated in Section 4.1.6 of SQAP at minimum. The NICSD V&V personnel shall perform an independent review of the user documentation.

(6) Unit/Module Validation Testing Phase PHA
The NED V&V personnel shall independently review the Unit/Module Validation Testing Phase PHA, and document the results of the review in accordance with AS-200A002.

5.6.3 Unit/Module Validation Phase RTM effort
(1) Preparation of Unit/Module Validation Phase RTM
NICSD shall perform Unit/Module Validation Phase RTM effort to trace the requirements from Requirements Phase RTM, and report any open items revealed by this RTM effort.
The NICSD Design Group must resolve these items to the satisfaction of the RTM Preparer and the Reviewer. NICSD must resolve all open items before the end of Unit/Module Validation Testing Phase. NICSD and NED shall confirm that the validation tests comprehensively validate all the entries in the RTM from the Requirements Phase.

(2) Compilation of the Unit/Module Validation Phase RTM report
The NICSD V&V team shall compile the Unit/Module Validation Phase RTM report

5.6.4 Assessment of Test Equipment Software
NED V&V personnel shall assess the NICSD control of the test equipment software, if used in the Unit/Module Validation Testing.

NED V&V personnel shall review NICSD's records for test equipment software control to ensure:

- Test equipment software used for the project tests is prepared in accordance with procedures that NED V&V personnel have reviewed and approved.
- NICSD is controlling the software tools in accordance with NICSD procedure D-67003 (Reference 2.4.24).

NED may also perform in-process audits and witness activities to verify that NICSD is working in compliance with these controls and procedures. Results of these reviews, and audits if necessary, shall be documented in NED's VVR for this phase.

5.6.5 Issuance of the Unit/Module VVR
The NICSD V&V team shall establish the NICSD Unit/Module VVR. The report includes:

(1) A description of how the V&V activities were completed.
(2) A description of how adherence to each software life cycle requirements and system requirements were demonstrated,
(3) Copies of or reference to the NICSD VVRs issued for requirements phase through implementation phase.
(4) References to the independent reviews of the unit and module hardware review.
   (See 5.9)
(5) Copies of or references to Unit/Module Validation Test Reports, including the configuration of the test specimen.
(6) Reference to the Unit/Module Validation Phase RTM.

Approval of this phase VVR confirms that all required reviews and testing were performed completely and that no unresolved anomalies (PRSs) or issues remain.
NED V&V personnel shall establish the Unit/Module Verification and Validation Final report based on the NICSD VVR, when the NICSD VVR is acceptable to NED. The report includes any findings, recommendations, or suggestions on using the NICSD Unit/Module VVR. NICSD and NED shall confirm that the validation tests comprehensively validate all the entries in the RTM from Requirements Phase.

5.7 System Validation Testing Phase

NED V&V personnel shall perform the System Validation Testing Phase V&V activities.

V&V Inputs:
1. ERS (Base Document)
2. System Validation test procedure (Review Document)
3. System Validation test report (Review Document)
4. System Validation Testing Phase RTM (Review Document)
5. Concept Phase RTM (Base Document)

V&V Outputs:
1. Document Review Reports (by NED)
2. System Validation Testing Phase RTM (by NED)
3. System Verification and Validation Final report (by NED)

5.7.1 System Validation Testing

(1) NED PQA (see Figure 4-1) shall perform the system validation testing.

(2) NED PQA shall prepare nonconformance notice reports (NNRs) to document any test failures, any product or configuration nonconformance, or any errors in the validation test procedure itself. NED PQA shall forward the NNRs to the Design Group for resolution, and perform retests as needed to resolve all NNRs.

See sections 5.7.2 through 5.7.5 for NED V&V activities.

5.7.2 Document Reviews

NED V&V personnel shall review the system validation testing procedures (which are prepared by NED design engineers) and the System Validation Test Reports (which are prepared by NED design engineers), and any NNRs written as a result of the testing.

The NED V&V personnel shall independently review the final hazard analysis report, and document the results of the review in accordance with AS-200A002.

5.7.3 System Validation Testing Phase RTM effort

(1) Preparation of System Validation Testing Phase RTM

NED V&V personnel shall perform the System Validation Testing Phase RTM effort to trace the requirements from Concept Phase RTM for the System. NED shall confirm that the validation tests comprehensively validate all the entries in the Concept Phase RTM.

(2) Compilation of the Final RTM report

The NED design engineers prepare the Final RTM report. The Final RTM report must include the RTM, how each requirement is addressed in the test results, and resolutions to all
open items. The Final RTM shall be reviewed by NED V&V personnel, and approved by the Group Manager of the Monitoring System Engineering Group.

5.7.4 Assessment of Test Equipment Software
NED may use Test Equipment Software for the System Validation Testing. In that case, NED test personnel shall use the software in accordance with the requirements for test equipment software in section 4.6.

NED V&V personnel shall review the records for test equipment software control to ensure:

- Test Equipment Software used for the tests is prepared in accordance with the SQAP and section 4.6.
- The test equipment software is controlled using Master Configuration List (MCL) in accordance with AS-200A131.

If NED PQA uses the test equipment software that NICSD developed for Unit/Module testing for system testing, the test equipment software shall be considered as legacy software discussed in section 4.6.

5.7.5 Issuance of the final VVR
The NED V&V Team shall prepare, review and approve the Verification and Validation Final report. The report includes:

- A description of how the V&V activities were completed,
- A description of how adherence to each software and system requirement was demonstrated,
- System configuration tested,
- Version data for all test equipment software used in the testing.

Approval of the final VVR confirms that all required reviews and testing are performed completely and that no unresolved anomalies or issues remain.

5.8 Functional Element V&V
NICSD design engineer controls a library of general purpose FEs. For the FEs used in the FPGAs for the PRM system, V&V effort from the requirements phase through the implementation phase shall be applied. The depth and intensity of the V&V effort shall be in accordance with the SIL of the target FPGAs.

NICSD shall follow NICSD procedure D-68018 (Reference 2.4.21) for NICSD activities related to the design, V&V, testing or modification of FEs.

The following is the outline of the procedure prescribed in D-68018:

(1) FE Requirements Definition
The FE Requirements Specification is established to address at a minimum:

- FE functional requirements,
- Input/Output Signals,
• Interface/Interaction with other FE

(2) FE Design
The FE Specification (also referred to as a Software Design Document or SDD) is established. The FE Specification specifically states how all of the requirements specified in the FE Requirements Specification for this FE will be implemented. The FE Specification should contain sufficient criteria to support verification testing of the FE when performing FE testing.

The RTM is prepared to trace the design features in the FE Specification to the requirements shown in the FE Requirements Specification.

The FE test procedure that documents the following process is prepared:
- Make a VHDL source code which only indicates the connection to I/O pins and call the FE EDIF File.
- Convert the VHDL source code into an EDIF File with the synthesis tool and convert the EDIF File into a Fuse map with the layout tool.
- Implement the Fuse-map into the FPGA chip with the implementation tool.
- Mount the implemented FPGA chip on the signal test tool.
- Test the FE embedded in the FPGA chip for all possible input patterns to determine the correctness on the signal test tool.

The RTM is prepared to trace the tests in the FE test procedure to the requirements shown in the FE Requirements Specification.

(3) FE Coding
The coding of FEs is performed in VHDL. FEs are designed in accordance with the design rules shown in D-68017 Appendix A.

VHDL source code is translated into FE EDIF File with the logic synthesis tool.

(4) FE Testing
The tests are performed in accordance with the FE Test Procedure, and the Test Report is produced.

(5) Final FE Acceptance/Release
The FE is registered into the FE library after the confirmation of the issuance of the Test Report.

(6) Maintenance Phase
FE logic modifications are approved, documented, verified and validated, and controlled.

Above activities corresponds to the FE life cycle phases in SQAP (Reference 2.4.15) as shown in Table 5-1.
Table 5-2 The Relation between FE Life Cycle Phase and Activities for FE per D-68018

<table>
<thead>
<tr>
<th>Expected FE Life Cycle Phase in SQAP</th>
<th>Activities for FE per D-68018</th>
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<tbody>
<tr>
<td>Requirements Definition Phase</td>
<td>FE Requirements Definition</td>
</tr>
<tr>
<td>Design and Implementation Phase</td>
<td>FE Design, FE Coding</td>
</tr>
<tr>
<td>Testing Phase</td>
<td>FE Testing, Final FE Acceptance/Release</td>
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<tr>
<td>N/A</td>
<td>Maintenance Phase</td>
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</tbody>
</table>

NICSD shall perform the following V&V activities in the FPGA/SER project.

5.8.1 Document Check
The NICSD V&V team shall check the following documents to ensure that NICSD procedure D-68018 is appropriately applied for FEs placed in the FE library and used in the PRM project:

- FE Requirements Specification
- FE Specification
- RTM between the FE Specification and the FE Requirements Specification
- FE test procedure
- RTM between the FE Specification and the FE test procedure
- FE test report

In the check, the NICSD V&V team shall ensure that the full pattern tests have been appropriately performed for each FE.

The NICSD VVP shall document the procedure for the check. The NED V&V Team shall review this procedure as part of the review of NICSD's VVP.

The results of the check shall be documented and included in the Design phase VVR, and shall be reviewed by NED V&V personnel. See section 5.4.

5.8.2 Check of the FE library control and the software tool control
The NICSD V&V team shall check that appropriate control activities have been performed as follows:

- The FE library is being controlled in accordance with NICSD procedure D-68019.
- The software tools are being controlled in accordance with NICSD procedure D-68020 (Reference 2.4.23)

The results of the check shall be documented and included in the NICSD Design phase VVR, and shall be reviewed by NED V&V personnel. (See section 5.4)
5.9 Hardware V&V

The NICSD V&V team shall perform the independent review of the unit and module hardware design in accordance with NICSD procedure D-68016. The results of the review shall be documented and reported as a part of Unit/Module Validation Testing Phase VVR.

5.10 Configuration Management

SQAP Section 10 describes the Configuration Management Plan to be used by NED and NICSD in this project. Required V&V activities throughout the project are as follows:

- The NED V&V Team shall perform V&V activities on the NED MCL throughout the project life cycle in accordance with the requirements of Procedure AS-200A130. Specifically, this includes performing an independent review of the software baseline (when applicable) throughout the project. The NED V&V Team shall document the results of these activities in the NED VVR for each phase.
- The NICSD V&V Team shall perform V&V activities on the NICSD MCL throughout the NICSD effort in accordance with NICSD VVP. The NICSD V&V team shall document the results of NICSD V&V activities in the NICSD VVR for each phase. The specific activities to be performed by NICSD V&V personnel will be described in NICSD's VVP.
- The NED V&V Team shall review the NICSD V&V Team VVR to ensure that NICSD is performing the appropriate V&V activities for the NICSD MCL. NED shall document the results of this review in the NED VVR for each life cycle phase.

Note that the Project Specific Configuration Management Plan is contained in the SQAP; accordingly, independent review of the SQAP adequately completes the AS-200A130 and AS-200A131 procedure requirement for independent review of the Project Specific Configuration Management Plan.
6 Software Verification and Validation Reporting

The NICSD VVP shall state that the reports to be issued by NICSD include the followings:

- **Problem Reporting Sheet (PRS)**
  Problem Reporting Sheet shall be prepared to document any test failures, any product or configuration nonconformance, or any errors in the test procedure itself during FPGA and Unit/Module validation testing. See D-68016 (Reference 2.4.19) and D-68017 (Reference 2.4.20).

- **NNR**
  An NNR shall be issued if NICSD finds any problems in documents, equipment, or activities, for which an NICSD VVR has been already issued. See AS-300A006 (Reference 2.4.10).

- **RTM Reports for Phases in NICSD’s Scope**
  RTM Reports shall be prepared to trace the requirements in the previous phase to the current phase documents.

- **VVR for each phase**
  A VVR shall be prepared at the end of each V&V phase. The report shall include the results of documents reviews, copies of or references to PRS or NNR, and RTM Reports.

These NICSD reports shall be written in Japanese.

The reports issued by NED include:

- **NNR**
  An NNR shall be issued if NED finds any problems in documents, equipment, or activities, for which a VVR has been already issued. In addition, an NNR shall be issued to document any test failures, any product or configuration nonconformance, or any errors in the test procedure itself during system validation testing. See AS-300A008 (Reference 2.4.11)

- **RTM Reports in NED’s Scope**
  RTM Reports shall compare the results of the System Validation Testing Phase with the requirements in the Project Planning and Concept Definition Phase.

- **Hazard Analysis Report**
  The Hazard Analysis Report shall be prepared and updated to determine if the design and associated activities throughout the life cycle are established in a manner that minimize risk and design errors. The PHA Report shall be first prepared at the Concept Phase, and be updated from the Requirements Definition Phase through System Validation Testing Phase.

- **VVR for each phase**
  A VVR shall be prepared at the end of each V&V phase. The report includes the results of documents reviews, copies of or references to PRS or NNR, NICSD VVRs, and references to the PHA Report and RTM Report.

- **V&V Final Report**
  The V&V Final Report shall be established at the end of V&V activities. The Report includes copies or references to all VVRs from the life cycle phases.
These NED reports shall be written in English and available in NED offices for audit. For preparation of Hazard Analysis Reports, see section 4.2.4 of SQAP.
7 V&V Administrative Requirements

7.1 Problem Reporting and Corrective Action

If NED or NICSD find any problem in documentation, equipment, or design and V&V activities, the problems shall be reported, and corrective action shall be taken in accordance with section 8 of SQAP (Reference 2.4.15).

7.2 Task Iteration Policy

Affected V&V tasks or activities shall be repeated if design documents are changed in accordance with AS-200A015 (Reference 2.4.4) or if this VVP is updated.

If design documents are changed, the independent review shall be performed for the affected documents. Further, the design engineer shall update the RTM and the PHA to reflect the design change. This requires another independent review of the RTM. As a result, the VVR of the phase for the updated documents shall be updated.

For RTMs, design engineers shall revise the RTM even if there is nothing affected by the design change. V&V personnel shall verify that the decision of the design engineers as to the need for documentation change is correct.

Note that the change of the RTM may affect the next phase RTM. The design engineers shall follow the propagation of the effects of change through RTMs. All changes of RTMs shall be reviewed by V&V personnel.

The above policy applies to both the NED and the NICSD V&V activities.

For the case of this VVP update, see the next section.

7.3 Deviation Policy

If the NED V&V personnel determine that this VVP must be changed, the change shall be made in the same manner in which this plan has been established, i.e. the update shall be reviewed independently, and approved by the Project Manager.

For the approval of the VVP change, the Project Manager may need to know the impact on the quality of the project, the schedule, and the resources. The V&V personnel must explain this information to the Project Manager along with the reason of the change.

When the VVP is updated, the NED V&V personnel shall perform the following actions:
The NED V&V personnel shall assess the effect of the change to determine if there are any V&V activities to be repeated.
- The NED V&V personnel shall repeat the needed V&V activities.
- The NED V&V personnel shall notify the NICSD V&V team about the change to the NED VVP.

When the VVP is updated, the NICSD V&V team shall perform the following actions:
- The NICSD V&V team shall update the NICSD VVP so that it conforms to the updated NED VVP. The changes to be made to the NICSD VVP shall be approved by the NED V&V personnel.
- The NICSD V&V personnel shall assess the effect of the change to determine if there are any V&V activities to be iterated.
- The NICSD V&V personnel shall repeat the needed V&V activities.

If the NICSD V&V team change the NICSD VVP, the change shall be made in the same manner in which the initial NICSD VVP has been established, i.e. NICSD shall submit the updated VVP to the NED for approval. The NED V&V personnel shall review the updated NICSD VVP for its conformance to the NED VVP, and the Group Manager of the Monitoring System Engineering Group shall approve the updated NICSD VVP based on the review.

The NICSD V&V team may change the NICSD VVP of their necessity, as long as the change is submitted to and approved by the NED.

The V&V activities affected by the change shall be updated in accordance with the updated VVP.

### 7.4 Control Procedures

The documents that resulted from the V&V effort shall be controlled in accordance with the Project Quality Assurance Plan (Reference 2.4.14) and section 10 of the SQAP.

### 7.5 Standards, Practices and Conventions

For Standards, Practices, and Conventions, Refer to section 5 of SQAP.
8 V&V Documentation Requirements

This section defines the purpose, format, and content of the test documents, the Hazard Analysis Documents, and the RTMs.

8.1 Test Documents

NED shall establish the following test documents.

(1) System Validation test procedure
The System Validation test procedure shall be established so that it includes the contents of the Test Plan, the Test-Design Specification, the Test-Case Specification, and the Test-Procedure defined in IEEE Std 829-1983 (Reference 2.3.2).

The System Validation test procedure shall be accordance with AS-300A103 (Reference 2.4.12).

(2) System Validation test report
The System Validation test report shall be established so that it includes the contents of Test Log, Test Incident Report, and Test Summary Report defined in IEEE Std 829-1983.

The System Validation test report shall be prepared in accordance with AS-300A103.

Note that IEEE Std 829-1983 requires the Test-Item Transmittal Report. However, since the transmittal of the test items or the test specimen is performed in accordance with another procedure of this project, the Test-Item Transmittal Report is not included in this plan.

NICSD shall establish the following test documents in accordance with IEEE Std 829-1983:

(1) Unit/Module Validation test procedures
(2) Unit/Module Validation test reports
(3) FPGA Validation test procedures
(4) FPGA Validation test reports

The NICSD VVP shall prescribe the purpose, format, and content of the test documents.

8.2 Hazard Analysis Documents

For Hazard Analysis, the initial PHA Report shall be prepared at the Concept Phase, and be updated from the Requirements Definition Phase through System Validation Testing Phase. SQAP (Reference 2.4.15) section 4.2.4 describes the reporting in detail.
8.3 RTM

As described in Section 5 of this plan, NED will create the Concept phase RTM, and then NICSD will maintain and update the RTM for the work in NICSD’s scope.

NED shall develop the Concept phase RTM in accordance with procedure AS-200A130 (Reference 2.4.7). The content of the RTM shall consist of the requirements from the ERS and other applicable documents, presented in a matrix format.

NED and NICSD shall use the same general format in Exhibit for the RTM. If the RTM becomes too large to be filled in the format, the RTM may be divided into sub matrices, as long as the traceability between two subsequent phases must be clearly shown.
Exhibit RTM format

<table>
<thead>
<tr>
<th>No.</th>
<th>Findings and Open Items</th>
<th>Project Planning and Concept Definition Phase</th>
<th>Requirements Definition Phase</th>
<th>Design Phase</th>
<th>Implementation and Integration Phase</th>
<th>Unit/Module Validation Testing Phase</th>
<th>System Validation Testing Phase</th>
</tr>
</thead>
</table>

Note: The row width and the column height, and the size of the format are not restricted.
## Appendix A Compliance with IEEE Std 1012-1998

<table>
<thead>
<tr>
<th>Section</th>
<th>IEEE Std 1012-1998</th>
<th>NED V&amp;V Plan</th>
<th>Compliance</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Overview</td>
<td>-</td>
<td>-</td>
<td>No specific requirement</td>
</tr>
<tr>
<td>2</td>
<td>Normative reference</td>
<td>-</td>
<td>-</td>
<td>No specific requirement</td>
</tr>
<tr>
<td>3</td>
<td>Definitions, abbreviations</td>
<td>-</td>
<td>-</td>
<td>No specific requirement</td>
</tr>
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<td>4</td>
<td>V&amp;V software integrity levels</td>
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<td>-</td>
<td>Section title</td>
</tr>
<tr>
<td>4.1</td>
<td>Software integrity levels</td>
<td>-</td>
<td>4.3</td>
<td>Comply</td>
</tr>
<tr>
<td></td>
<td>The V&amp;V effort shall specify a software integrity scheme.</td>
<td>4.3</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td></td>
<td>The mapping of the software integrity level scheme and the associated minimum V&amp;V tasks shall be documented in the SVVP.</td>
<td>4.3</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td></td>
<td>The basis for assigning software integrity levels to software components shall be documented in a V&amp;V Task Report and V&amp;V Final Report.</td>
<td>4.3</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td></td>
<td>The integrity level assigned to reusable software shall be in accordance with the integrity level scheme adopted for the project, and the reusable software shall be evaluated for use in the context of its application.</td>
<td>4.6</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>V&amp;V processes</td>
<td>-</td>
<td>5</td>
<td>Comply</td>
</tr>
<tr>
<td></td>
<td>The V&amp;V effort shall comply with the task descriptions, inputs, and outputs as described in Table 1.</td>
<td>5</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td></td>
<td>The V&amp;V effort shall perform the minimum V&amp;V tasks as specified in Table 2 for the assigned software integrity level.</td>
<td>5</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td></td>
<td>If the user of this standard has selected a different software integrity level scheme, then the mapping of that integrity level scheme to Table 2 shall define the minimum V&amp;V tasks for each of the user's software integrity levels.</td>
<td>4.3</td>
<td>Comply</td>
<td></td>
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<td></td>
<td>Some V&amp;V activities and tasks include analysis, evaluations, and tests that may be performed by multiple organizations (e.g., software development, project management, quality assurance, V&amp;V). The degree to which these analyses efforts are coordinated with other organizations shall be documented in the organizational responsibility section of the SVVP.</td>
<td>N/A for VVP</td>
<td>SQAP covers the requirement by describing the Hazard Analyses that performed by the Design engineers.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>The user of this standard shall document the V&amp;V processes in the SVVP and shall define the information and facilities necessary to manage and perform these processes, activities, and tasks, and to coordinate those V&amp;V processes with other related aspects of the project. The results of V&amp;V activities and tasks shall be documented in task reports, activity summary reports, anomaly reports, V&amp;V test documents, and the V&amp;V Final Report.</td>
<td>5, 6</td>
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<td>Process: Management</td>
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<td>5.1.1</td>
<td>The V&amp;V effort shall perform, as appropriate for the selected software integrity level, the minimum V&amp;V tasks for Management of V&amp;V from the following list:</td>
<td>-</td>
<td>-</td>
<td>Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.</td>
</tr>
<tr>
<td></td>
<td>1) Task: Software Verification and Validation Plan (SVVP) Generation</td>
<td>Table 5-1</td>
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<td>Section</td>
<td>IEEE Std 1012-1998</td>
<td>NED V&amp;V Plan</td>
<td>Compliance</td>
<td>Comments</td>
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<td>5.2</td>
<td>Process: Acquisition</td>
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<tr>
<td>5.3</td>
<td>Process: Supply</td>
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<td>Activity: Planning V&amp;V</td>
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<td>Section title</td>
</tr>
<tr>
<td>5.4</td>
<td>Process: Development</td>
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<td>Section title</td>
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<td>5.4.1</td>
<td>Activity: Concept V&amp;V</td>
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<td>-</td>
<td>Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.</td>
</tr>
<tr>
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<td>The V&amp;V effort shall perform, as appropriate for the selected software integrity level, the minimum V&amp;V tasks for Concept V&amp;V from the following list:</td>
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<td>1) Task: Concept Documentation Evaluation</td>
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<td>2) Task: Criticality Analysis</td>
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<td></td>
<td>3) Task: Hardware/Software/User Requirements Allocation Analysis</td>
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<td>4) Task: Traceability Analysis</td>
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<td>5) Task: Hazard Analysis</td>
<td>5.1.2</td>
<td>Comply</td>
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<tr>
<td></td>
<td>6) Task: Risk Analysis</td>
<td>5.1.4</td>
<td>Comply</td>
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<tr>
<td></td>
<td>7) Task: Operation Procedure Evaluation</td>
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<td>5.4.2</td>
<td>Activity: Requirements V&amp;V</td>
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<td>-</td>
<td>Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.</td>
</tr>
<tr>
<td></td>
<td>The V&amp;V effort shall perform, as appropriate for the selected software integrity level, the minimum V&amp;V tasks for Requirements V&amp;V from the following list:</td>
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<tr>
<td></td>
<td>1) Task: Traceability Analysis</td>
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<td>Comply</td>
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<td>2) Task: Software Requirements Evaluation</td>
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<td>3) Task: Interface Analysis</td>
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<td>4) Task: Criticality Analysis</td>
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<td>5) Task: System V&amp;V Test Plan Generation and Verification</td>
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<td>6) Task: Acceptance V&amp;V Test Plan Generation and Verification</td>
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<td>7) Task: Configuration Management Assessment</td>
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<td>8) Task: Hazard Analysis</td>
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<tr>
<td></td>
<td>9) Task: Risk Analysis</td>
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<tr>
<td>5.4.3</td>
<td>Activity: Design V&amp;V</td>
<td>5.4</td>
<td>-</td>
<td>VVR describe the project risk.</td>
</tr>
<tr>
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<td>The V&amp;V effort shall perform, as appropriate for the selected software integrity level, the minimum V&amp;V tasks for Design V&amp;V from the following list:</td>
<td></td>
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<tr>
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<td>1) Task: Traceability Analysis</td>
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<td></td>
<td>2) Task: Software Design Evaluation</td>
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<td>Comply</td>
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<tr>
<td></td>
<td>3) Task: Interface Analysis</td>
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<td>4) Task: Criticality Analysis</td>
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<td>Comply</td>
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<td></td>
<td>5) Task: Component V&amp;V Test Plan Generation and Verification</td>
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<td></td>
<td>6) Task: Integration V&amp;V Test Plan Generation and Verification</td>
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<td>Comply</td>
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<tr>
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<td>7) Task: V&amp;V Test Design Generation and Verification</td>
<td>5.5.4</td>
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<td></td>
<td>8) Task: Hazard Analysis</td>
<td>5.4.1</td>
<td>Comply</td>
<td></td>
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<tr>
<td></td>
<td>9) Task: Risk Analysis</td>
<td>5.4.3</td>
<td>Comply</td>
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</tr>
<tr>
<td>5.4.4</td>
<td>Activity: Implementation V&amp;V</td>
<td>-</td>
<td>-</td>
<td>Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.</td>
</tr>
<tr>
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<td>The V&amp;V effort shall perform, as appropriate for the selected software integrity level, the minimum V&amp;V tasks for Implementation V&amp;V from the following list:</td>
<td></td>
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<tr>
<td></td>
<td>1) Task: Traceability Analysis</td>
<td>5.5.5, 5.5.1</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2) Task: Source Code and Source Code Documentation Evaluation</td>
<td>5.5.1</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>Section</td>
<td>IEEE Std 1012-1998</td>
<td>NED V&amp;V Plan</td>
<td>Compliance</td>
<td>Comments</td>
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</tr>
<tr>
<td>3) Task: Interface Analysis</td>
<td></td>
<td>5.5.4</td>
<td>Comply</td>
<td>The interface in IEEE standard is considered to correspond to internal and external wiring connections in FPGA systems.</td>
</tr>
<tr>
<td>4) Task: Criticality Analysis</td>
<td></td>
<td>5.5.1, 5.5.4</td>
<td>Comply</td>
<td>The V&amp;V activities of the Implementation phase are planned so that they are commensurate with SIL 4 software.</td>
</tr>
<tr>
<td>5) Task: V&amp;V Test Case Generation and Verification</td>
<td></td>
<td>5.5.4</td>
<td>Comply</td>
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<td>6) Task: V&amp;V Test Procedure Generation and Verification</td>
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<tr>
<td>7) Task: Component V&amp;V Test Execution and Verification</td>
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<td>5.5.4</td>
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<td></td>
</tr>
<tr>
<td>9) Task: Risk Analysis</td>
<td></td>
<td>5.5.7</td>
<td>Comply</td>
<td></td>
</tr>
</tbody>
</table>

5.4.5 **Activity: Test V&V**

For software integrity levels 3 and 4, the V&V effort shall generate its own V&V software and system test products (e.g., plans, designs, cases, procedures), execute and record its own tests, and verify those plans, designs, cases, procedures, and test results against software requirements.

For software integrity levels 1 and 2, the V&V effort shall verify the development process test activities and products (e.g., test plans, designs, cases, procedures, and test execution results).

The V&V effort shall perform, as appropriate for the selected software integrity level, the minimum V&V tasks for Test V&V from the following list:

1) Task: Traceability Analysis | 5.6.3, 5.7.3 | Comply | |
2) Task: Acceptance V&V Test Procedure Generation and Verification | N/A | Out of the project scope | |
3) Task: Integration V&V Test Execution and Verification | 5.6.1 | Comply | |
4) Task: System V&V Test Execution and Verification | 5.7.1 | Comply | |
5) Task: Acceptance V&V Test Execution and Verification | N/A | Out of the project scope | |
6) Task: Hazard Analysis | 5.6.5, 5.7.2 | Comply | |
7) Task: Risk Analysis | 5.6.6 | Comply | |

5.4.6 **Activity: Installation and Checkout V&V**

1) Anomaly Resolution and Reporting | 7.1 | Comply | |

**Software V&V reporting, administrative, and documentation requirements**

- **Section title**

6.1 V&V reporting requirements

V&V reporting occurs throughout the software life cycle. The SVVP shall specify the content, format, and timing of all V&V reports. The V&V reports shall constitute the Software Verification and Validation Report (SVVR). The V&V reports shall consist of required V&V reports (i.e., V&V Task Reports, V&V Activity Summary Reports, V&V Anomaly Reports, and V&V Final Report). The V&V reports may also include optional reports. Reporting requirements are described in 7.6 of this standard.

6.2 V&V administrative requirements

The SVVP describes the V&V administrative requirements that support the V&V effort. These V&V administrative requirements shall consist of the following:

1) Anomaly Resolution and Reporting | 7.1 | Comply | Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.
<table>
<thead>
<tr>
<th>Section</th>
<th>IEEE Std 1012-1998</th>
<th>NED V&amp;V Plan</th>
<th>Compliance</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>2)</td>
<td>Task Iteration Policy</td>
<td>7.2</td>
<td>Comply</td>
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<tr>
<td>3)</td>
<td>Deviation Policy</td>
<td>7.3</td>
<td>Comply</td>
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<td>4)</td>
<td>Control Procedures</td>
<td>7.4</td>
<td>Comply</td>
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<tr>
<td>5)</td>
<td>Standards, Practices, and Conventions</td>
<td>7.5</td>
<td>Comply</td>
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</tr>
<tr>
<td>V&amp;V documentation requirements</td>
<td>8</td>
<td>Comply</td>
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</tr>
<tr>
<td>7.</td>
<td>SVVP outline</td>
<td>VVP section 1 through 8</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>7.1</td>
<td>(SVVP Section 1) Purpose</td>
<td>1</td>
<td>Comply</td>
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<tr>
<td></td>
<td>The SVVP shall contain the content as described in 7.1 through 7.8 of this standard.</td>
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<tr>
<td>7.2</td>
<td>(SVVP Section 2) Referenced documents</td>
<td>2</td>
<td>Comply</td>
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<tr>
<td></td>
<td>The SVVP shall identify the compliance documents, documents referenced by the SVVP, and any supporting documents supplementing or implementing the SVVP.</td>
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<tr>
<td>7.3</td>
<td>(SVVP Section 3) Definitions</td>
<td>3</td>
<td>Comply</td>
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<td></td>
<td>The SVVP shall define or reference all terms used in the SVVP, including the criteria for classifying an anomaly as a critical anomaly. All abbreviations and notations used in the SVVP shall be described.</td>
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<tr>
<td>7.4</td>
<td>(SVVP Section 4) V&amp;V overview</td>
<td>4</td>
<td>Comply</td>
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<tr>
<td></td>
<td>The SVVP shall describe the organization, schedule, software integrity level scheme, resources, responsibilities, tools, techniques, and methods necessary to perform the software V&amp;V.</td>
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<tr>
<td>7.4.1</td>
<td>(SVVP Section 4.1) Organization</td>
<td>4.1</td>
<td>Comply</td>
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<tr>
<td></td>
<td>The SVVP shall describe the organization of the V&amp;V effort, including the degree of independence required. The SVVP shall describe the relationship of the V&amp;V processes to other processes such as development, project management, quality assurance, and configuration management. The SVVP shall describe the lines of communication within the V&amp;V effort, the authority for resolving issues raised by V&amp;V tasks, and the authority for approving V&amp;V products.</td>
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<tr>
<td>7.4.2</td>
<td>(SVVP Section 4.2) Master Schedule</td>
<td>4.2</td>
<td>Comply</td>
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<td></td>
<td>The SVVP shall describe the project life cycle and milestones. It shall summarize the schedule of V&amp;V tasks and task results as feedback to the development, organizational, and supporting processes. V&amp;V tasks shall be scheduled to be re-performed according to the task iteration policy.</td>
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<tr>
<td>Section</td>
<td>IEEE Std 1012-1998</td>
<td>NED V&amp;V Plan</td>
<td>Compliance</td>
<td>Comments</td>
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<tr>
<td>7.4.3</td>
<td>(SVVP Section 4.3) Software integrity level scheme</td>
<td>4.3</td>
<td>Comply</td>
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<td></td>
<td>The SVVP shall describe the agreed upon software integrity level scheme established for the system and the mapping of the selected scheme to the model used in this standard. The SVVP shall document the assignment of software integrity levels to individual components (e.g., requirements, detailed functions, software modules, subsystems, or other software partitions), where there are differing software integrity levels assigned within the program. For each SVVP update, the assignment of software integrity levels shall be reassessed to reflect changes that may occur in the integrity levels as a result of architecture selection, detailed design choices, code construction usage, or other development activities.</td>
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<tr>
<td>7.4.4</td>
<td>(SVVP Section 4.4) Resources summary</td>
<td>4.4</td>
<td>Comply</td>
<td></td>
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<tr>
<td></td>
<td>The SVVP shall summarize the V&amp;V resources, including staffing, facilities, tools, finances, and special procedural requirements (e.g., security, access rights, and documentation control).</td>
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<tr>
<td>7.4.5</td>
<td>(SVVP Section 4.5) Responsibilities</td>
<td>4.5</td>
<td>Comply</td>
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<tr>
<td></td>
<td>The SVVP shall identify an overview of the organizational element(s) and responsibilities for V&amp;V tasks.</td>
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<tr>
<td>7.4.6</td>
<td>(SVVP Section 4.6) Tools, techniques, and methods</td>
<td>4.6</td>
<td>Comply</td>
<td></td>
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<tr>
<td></td>
<td>The SVVP shall describe documents, hardware and software V&amp;V tools, techniques, methods, and operating and test environment to be used in the V&amp;V process. Acquisition, training, support, and qualification information for each tool, technology, and method shall be included.</td>
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<td></td>
<td>Tools that insert code into the software shall be verified and validated to the same rigor as the highest software integrity level of the software. Tools that do not insert code shall be verified and validated to assure that they meet their operational requirements. If partitioning of tool functions can be demonstrated, only those functions that are used in the V&amp;V process shall be verified to demonstrate that they perform correctly for their intended use.</td>
<td>-</td>
<td>Not Comply</td>
<td>In Regulatory Guide 1.168, the NRC staff states that this requirement is one of the exceptions in endorsing IEEE std 1012-1998. See Appendix B.</td>
</tr>
<tr>
<td></td>
<td>The SVVP shall document the metrics to be used by V&amp;V (see Annex E), and shall describe how these metrics support the V&amp;V objectives.</td>
<td>4.6</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>7.5</td>
<td>(SVVP Section 5) V&amp;V processes</td>
<td>5</td>
<td>Comply</td>
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<td></td>
<td>The SVVP shall identify V&amp;V activities and tasks to be performed for each of the V&amp;V processes described in Clause 5 of this standard, and shall document those V&amp;V activities and tasks. The SVVP shall contain an overview of the V&amp;V activities and tasks for all software life cycle processes.</td>
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<tr>
<td>7.5.1</td>
<td>(SVVP Sections 5.1 through 5.6) &quot;Software life cycle&quot;</td>
<td>-</td>
<td>-</td>
<td>Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.</td>
</tr>
<tr>
<td></td>
<td>The SVVP shall include sections 5.1 through 5.6 for V&amp;V activities and tasks as shown in SVVP Outline (boxed text).</td>
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<tr>
<td></td>
<td>The SVVP shall address the following eight topics for each V&amp;V activity:</td>
<td></td>
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</tr>
<tr>
<td>Section</td>
<td>IEEE Std 1012-1998</td>
<td>NED V&amp;V Plan</td>
<td>Compliance</td>
<td>Comments</td>
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<td>----------</td>
</tr>
<tr>
<td>1) V&amp;V Tasks. The SVVP shall identify the V&amp;V tasks to be performed.</td>
<td></td>
<td>5</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>2) Methods and Procedures. The SVVP shall describe the methods and procedures for each task, including on-line access, and conditions for observation/evaluation of development processes. The SVVP shall define the criteria for evaluating the task results.</td>
<td></td>
<td>5.1 - 5.10</td>
<td>Comply</td>
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</tr>
<tr>
<td>3) Inputs. The SVVP shall identify the required inputs for each V&amp;V task. The SVVP shall specify the source and format of each input.</td>
<td></td>
<td>5, 5.1, 5.3 - 5.8</td>
<td>Comply</td>
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<tr>
<td>4) Outputs. The SVVP shall identify the required outputs from each V&amp;V task. The SVVP shall specify the purpose, format, and recipients of each output.</td>
<td></td>
<td>5, 5.1, 5.3 - 5.8</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>The outputs of the Management of V&amp;V and of the V&amp;V tasks shall become inputs to subsequent processes and activities, as appropriate.</td>
<td></td>
<td>5, 5.1, 5.3 - 5.8</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>5) Schedule. The SVVP shall describe the schedule for the V&amp;V tasks. The SVVP shall establish specific milestones for initiating and completing each task, for the receipt and criteria of each input, and for the delivery of each output.</td>
<td></td>
<td>4.2</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>6) Resources. The SVVP shall identify the resources for the performance of the V&amp;V tasks. The SVVP shall specify resources by category (e.g., staffing, equipment, facilities, travel, and training).</td>
<td></td>
<td>4.4</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>7) Risks and Assumptions. The SVVP shall identify the risks (e.g., schedule, resources, or technical approach) and assumptions associated with the V&amp;V tasks. The SVVP shall provide recommendations to eliminate, reduce, or mitigate risks.</td>
<td></td>
<td>5.1, 5.3 - 5.8</td>
<td>Comply</td>
<td>The risks and assumptions will be included in the VVR, and reported to the project management.</td>
</tr>
<tr>
<td>8) Roles and Responsibilities. The SVVP shall identify the organizational elements or individuals responsible for performing the V&amp;V tasks.</td>
<td></td>
<td>5.1, 5.3 - 5.8</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>7.6 (SVVP Section 6) V&amp;V reporting requirements</td>
<td></td>
<td>6</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>V&amp;V reporting shall consist of Task Reports, V&amp;V Activity Summary Reports, Anomaly Reports, and the V&amp;V Final Report.</td>
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<tr>
<td>7.7 (SVVP Section 7) V&amp;V administrative requirements</td>
<td></td>
<td>7</td>
<td>-</td>
<td>Section title</td>
</tr>
<tr>
<td>7.7.1 (SVVP Section 7.1) Anomaly resolution and tracking</td>
<td></td>
<td>7.1</td>
<td>Comply</td>
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</tr>
<tr>
<td>The SVVP shall describe the method of reporting and resolving anomalies, including the criteria for reporting an anomaly, the anomaly report distribution list, and the authority and time lines for resolving anomalies. The section shall define the anomaly criticality levels.</td>
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<tr>
<td>7.7.2 (SVVP Section 7.2) Task iteration policy</td>
<td></td>
<td>7.2</td>
<td>Comply</td>
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</tr>
<tr>
<td>The SVVP shall describe the criteria used to determine the extent to which a V&amp;V task shall be repeated when its input is changed or task procedure is changed.</td>
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<tr>
<td>Section</td>
<td>IEEE Std 1012-1998</td>
<td>NED V&amp;V Plan</td>
<td>Compliance</td>
<td>Comments</td>
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<tr>
<td>7.7.3</td>
<td>(SVVP Section 7.3) Deviation policy</td>
<td>7.3</td>
<td>Comply</td>
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<tr>
<td></td>
<td>The SVVP shall describe the procedures and criteria used to deviate from the Plan. The information required for deviations shall include task identification, rationale, and effect on software quality. The SVVP shall identify the authorities responsible for approving deviations.</td>
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<tr>
<td>7.7.4</td>
<td>(SVVP Section 7.4) Control procedures</td>
<td>7.4</td>
<td>Comply</td>
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<tr>
<td></td>
<td>The SVVP shall identify control procedures applied to the V&amp;V effort. These procedures shall describe how software products and V&amp;V results shall be configured, protected, and stored.</td>
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<td></td>
<td>The SVVP shall describe how the V&amp;V effort shall comply with existing security provisions and how the validity of V&amp;V results shall be protected from unauthorized alterations.</td>
<td>4.5</td>
<td>Comply</td>
<td></td>
</tr>
<tr>
<td>7.7.5</td>
<td>(SVVP Section 7.5) Standards, practices, and conventions</td>
<td>7.5</td>
<td>Comply</td>
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<td></td>
<td>The SVVP shall identify the standards, practices, and conventions that govern the performance of V&amp;V tasks including internal organizational standards, practices, and policies.</td>
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<tr>
<td>7.8</td>
<td>(SVVP Section 8) V&amp;V documentation requirements</td>
<td>8</td>
<td>Comply</td>
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<tr>
<td></td>
<td>The SVVP shall define the purpose, format, and content of the test documents.</td>
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</tbody>
</table>
# Appendix B  Compliance with Regulatory Guide 1.168

Regulatory Guide 1.168 Rev.1 (Reference 2.2.1) endorses IEEE Std 1012-1998 with some exceptions. The following table describes the compliance of the VVP with the exceptions.

<table>
<thead>
<tr>
<th>Reg. Guide 1.168 Regulatory Position</th>
<th>NED V&amp;V Plan</th>
<th>Compliance</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. CRITICAL SOFTWARE</td>
<td>4.3</td>
<td>Comply</td>
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<tr>
<td>Software used in nuclear power plant safety systems should be assigned integrity level 4 or equivalent, as demonstrated by a mapping between the applicant or licensee approach and integrity level 4 as defined in IEEE Std 1012-1998.</td>
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<tr>
<td>2. SOFTWARE RELIABILITY</td>
<td>5</td>
<td>Comply</td>
<td>The NED VVP describes the V&amp;V activities that shall be performed. The criterion for the reliability goal is whether the activities are appropriately accomplished or not.</td>
</tr>
<tr>
<td>Consistent with the staff's position on reliability measures for digital safety systems contained in other regulatory guides, the NRC staff's acceptance of quantitative reliability goals for computer-based safety systems is predicated on deterministic criteria for the computer system in its entirety (i.e., hardware, system software, firmware, application, and interconnections).</td>
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<tr>
<td>3. INDEPENDENCE OF SOFTWARE</td>
<td>4.1</td>
<td>Comply</td>
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<tr>
<td>VERIFICATION AND VALIDATION</td>
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<tr>
<td>A method of performing independent software V&amp;V is described in Revision 1 of Regulatory Guide 1.152.</td>
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<tr>
<td>4. CONFORMANCE OF MATERIALS</td>
<td>-</td>
<td>N/A</td>
<td>No legacy software shall be used in the FRM system.</td>
</tr>
<tr>
<td>IEEE Std 1012-1998 provides guidance for retrospective V&amp;V of software that was not verified under the standard. The use of this guidance for the acceptance of pre-existing safety system software not verified during development to the provisions of this regulatory guide or its equivalent is not endorsed.</td>
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<tr>
<td>Revision 1 of Regulatory Guide 1.152 provides information on the acceptance of pre-existing software. Additional detailed information on acceptance processes is available in EPRI TR-106439, “Guideline on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications” (October 1996).</td>
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</tr>
<tr>
<td>5. QUALITY ASSURANCE</td>
<td>-</td>
<td>N/A for VVP</td>
<td>TOSHIBA NED QA program based on Appendix B shall be applied.</td>
</tr>
<tr>
<td>In addition to the provisions of IEEE Std 1012-1998 (in Clause 7.7.4) regarding control procedures, any V&amp;V materials necessary for the verification of the effectiveness of the V&amp;V programs or necessary to furnish evidence of activities affecting quality should be maintained as quality assurance records. The records necessary for the verification of changes must be maintained in accordance with Criterion XVII.</td>
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<tr>
<td>6. TOOLS FOR SOFTWARE DEVELOPMENT</td>
<td>5.5.2, 5.5.4, 5.8</td>
<td>Comply</td>
<td>Section 5.5.2, 5.5.4, and 5.8 of VVP address how to possible tool errors.</td>
</tr>
<tr>
<td>Tools used in the development of safety system software should be handled according to IEEE Std 7-4.3.2-1993,1 as endorsed by Revision 1 of Regulatory Guide 1.152. IEEE Std 7-4.3.2-1993 states that “V&amp;V tasks of witnessing, reviewing, and testing are not required for software tools, provided the software that is produced using the tools is subject to V&amp;V activities that will detect flaws introduced by the tools.” If this cannot be demonstrated, the provisions of this regulatory guide are applicable.</td>
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<tr>
<td>7. VERIFICATION AND VALIDATION TASKS</td>
<td>-</td>
<td>-</td>
<td>Section title</td>
</tr>
<tr>
<td>Exception is taken to the “optional” status of some tasks on this list; they are considered by the NRC staff to be necessary components of acceptable methods for meeting the requirements of Appendices A and B to 10 CFR Part 50 as applied to software, regardless of whether they are performed by the V&amp;V organization.</td>
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<tr>
<td>Section</td>
<td>Description</td>
<td>Compliance</td>
<td>Notes</td>
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<tr>
<td>7.1</td>
<td>Audits&lt;br&gt;Safety system software V&amp;V organizations may employ audits, including functional audits, in-process audits, and physical audits of software. Although these audits are commonly considered to be the responsibility of the software quality assurance organization and the configuration management organization, they may be performed and relied upon by the V&amp;V organization.</td>
<td>N/A for VVP</td>
<td>Because Audit shall be performed by PJ QA, this V&amp;V does not refer to audit.</td>
</tr>
<tr>
<td>7.2</td>
<td>Regression Analysis and Testing&lt;br&gt;Criterion III, &quot;Design Control,&quot; requires that design changes be subject to design control measures commensurate with those applied to the original design. Regression analysis and testing following the implementation of software modifications is an element of the V&amp;V of software changes. It is considered by the NRC staff to be part of the minimum set of software V&amp;V activities for safety system software.</td>
<td>Comply</td>
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<tr>
<td>7.3</td>
<td>Security Assessment&lt;br&gt;A security breach of a digital system containing safety system software has the potential to prevent that software from fulfilling its safety function. Appendix A imposes functional and reliability requirements with respect to safety systems. According to 10 CFR 73.46, vital equipment (which includes safety system software) must be protected by physical barriers and access control. The NRC staff considers security assessment of safety system software to be part of the minimum set of software V&amp;V activities for such software.</td>
<td>Comply</td>
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<tr>
<td>7.4</td>
<td>Test Evaluation&lt;br&gt;Test evaluation includes confirming the technical adequacy of test materials such as plans, designs, and results. These materials are evaluated for consistency with Criterion II, &quot;Quality Assurance Program,&quot; in its requirement for controlled conditions, and with Criterion XI, &quot;Test Control,&quot; in its requirement for the evaluation of test results.</td>
<td>5.5.4, 5.6.2, 5.7.2, 5.7.4</td>
<td>Comply</td>
</tr>
<tr>
<td>7.5</td>
<td>Evaluation of User Documentation&lt;br&gt;User documentation is important to the safe operation and proper maintenance of safety system software. The requirements of Criterion III, &quot;Design Control,&quot; for correctly translating the design basis of safety system software into specifications, procedures, drawings, and instructions, apply to software documentation, including user documentation.</td>
<td>5.6.2</td>
<td>Comply</td>
</tr>
<tr>
<td>8.</td>
<td>OTHER CODES AND STANDARDS&lt;br&gt;Various sections of IEEE Std 1012-1998 and IEEE Std 1028-1997 reference other industry codes and standards. These references to other standards should be treated individually. If a referenced standard has been incorporated separately into the NRC's regulations, licensees and applicants must comply with that standard as set forth in the regulation. If the referenced standard has been endorsed in a regulatory guide, the standard constitutes a method acceptable to the NRC staff for meeting a regulatory requirement as described in the regulatory guide. If a referenced standard has been neither incorporated into the NRC's regulations nor endorsed in a regulatory guide, licensees and applicants may consider and use the information in the referenced standard, if appropriately justified, consistent with current regulatory practice.</td>
<td>N/A</td>
<td></td>
</tr>
</tbody>
</table>