

**US Safety Related**

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 TOSHIBA CORPORATION  
 NUCLEAR ENERGY SYSTEMS & SERVICES DIV.

**NRW-FPGA-Based PRM System Qualification Project**

Document Title

Acceptance Plan for Test Specimen Units, Interconnecting Cables

CUSTOMER NAME	None
PROJECT NAME	NRW-FPGA-Based PRM System Qualification Project
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**TOSHIBA CORPORATION** Nuclear Energy Systems & Services Division



# Acceptance Plan for Commercial Grade Dedication

商用品採用受領計画書

Sheet ( 1 / 7 )

Document No. FPG-PLN-C51-0008

Rev.1

Plan Date: April/24/2006

The purpose of this form is to document critical characteristics for acceptance of commercial grade items and services. This form should indicate the acceptance criteria and how each CCA will be verified (i.e., acceptance method), and include references to additional documents or procedures as needed. (本書式使用の目的は商用品及び役務の受領に対する決定的特性(CCA)を図書化するためである。本書式はCCAの合格基準及びその検証方法(受領方法)を示し、また、必要な追加図書または要領も含まなければならない。)

Acceptance Method 受領方法	Required Procedure 要求要領	Additional Documentation 追加図書	
Method 1 - Special tests and inspections 方法 1-特別試験及び検査	AS-200A111 or AS-200A112	Test/Inspection Plan; Test/Inspection Procedure, Test/Inspection Record 試験/検査計画, 試験/検査要領, 試験/検査記録	
Method 2 - Commercial grade survey 方法 2-商用サーベイ	AS-300A002	Source verification Report 立会検査報告書	
Method 3 - Source verification 方法 3-立会検査	AS-200A111 or AS-200A112	Surveillance Plan, Source verification Report サーベイ計画, 立会検査報告書	
Method 4 - Supplier/item performance record 方法 4-供給者実績/製品性能記録	AS-200A111	Supplier/Item Performance Record 供給者実績/製品性能記録	
Critical characteristic for acceptance (CCA) 受領に対する CCA	Acceptance criteria including tolerances 許容誤差を含む受領基準	Acceptance method(s) (Note1) 受領方法(注1)	Additional documentation prepared by Toshiba (NED) to support the acceptance method (note 2) (原子力)作成受領方法サポート追加図書(注2)
<b>Unit Model Numbers</b>			
Model Number of LPRM Unit -- Unit Model Number -- Revision Number -- Serial Number	Model No.: HNU100; 12 LPRM Type (6E8H7301 LPRM Unit Users Manual)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Model Number of LPRM/APRM Unit -- Unit Model Number -- Revision Number -- Serial Number	Model No.: HNU200 (6E8H7302 APRM Unit Users Manual)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Model Number of FLOW Unit -- Unit Model Number -- Revision Number -- Serial Number	Model No.: HNU300 (6E8H7306 FLOW Unit Users Manual)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
<b>Configuration Identifications of Units</b>			
Configuration Identification of LPRM Unit -- Module Model Numbers -- Revision Number -- Serial Number	Model No.: HNU100 Including Module: LPRM Module (HNS011) X12 Status Module (HNS092) X1 BLANK Module (HNS490) X1 LVPS Module (HNS500) X2 AO1 Module (HNS514) X1 AO2 Module (HNS511) X1 DIO Module (HNS520) X1 TRN Module (HNS530) X1 (6E8H7301 LPRM Unit Users Manual)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>

(Note 1): Acceptance method shall include one or more of the above "Acceptance Method" and shall be described the first column of each method (受領方法には上記から選択し、空欄に記入すること。)

(Note 2): Required additional documentations are noted the above "Additional Documentation" for each method chosen. (要求された追加図書は選択された方法毎に追加図書を記入すること。)

Acceptance Plan for Commercial Grade Dedication 商用品採用受領計画書		Sheet ( 2 / 7 )	
		Document No. FPG-PLN-C51-0008	Rev.1
		Plan Date: April/24/2006	
Critical characteristic for acceptance (CCA) 受領に対する CCA	Acceptance criteria including tolerances 許容誤差を含む受領基準	Acceptance method(s) (Note1) 受領方法(注1)	Additional documentation prepared by Toshiba (NED) to support the acceptance method (note 2) (原子力)作成受領方法サポート追加図書(注2)
Configuration Identification of LPRM/APRM Unit -- Module Model Numbers -- Revision Number -- Serial Number	Model No.: HNU200 Including Module: LPRM Module (HNS011) X10 APRM Module (HNS020) X1 Status Module (HNS091) X1 LVPS Module (HNS500) X2 AO1 Module (HNS514) X1 AO2 Module (HNS511) X1 AO3 Module (HNS512) X1 DIO Module (HNS520) X1 RCV Module (HNS540) X1 TRN Module (HNS530) X1 (6E8H7302 APRM Unit Users Manual)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Configuration Identification of FLOW Unit -- Module Model Numbers -- Revision Number -- Serial Number	Model No.: HNU300 Including Module: SQ-ROOT Module (HNS030) X2 FLOW Module (HNS040) X1 Status Module (HNS093) X1 LVPS Module (HNS500) X2 AO1 Module (HNS514) X1 AO2 Module (HNS512) X1 AO3 Module (HNS513) X1 DIO Module (HNS520) X1 TRN Module (HNS530) X2  (6E8H7306 FLOW Unit Users Manual)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Spare Modules			
Identification of Spare Modules -- Module Model Numbers -- Revision Number -- Serial Number	LPRM Module (HNS011) X5 APRM Module (HNS020) X1 SQ-ROOT Module (HNS030) X1 FLOW Module (HNS040) X1 STS Module (HNS091) X1 STS Module (HNS093) X1 BLANK Module (HNS490) X1 LVPS Module (HNS500) X1 AO Module (HNS511) X5 AO Module (HNS512) X5 AO Module (HNS513) X3 AO Module (HNS514) X7 DIO Module (HNS520) X1 TRN Module (HNS530) X1 RCV Module (HNS540) X1	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Interconnecting Cables			
Cable Type	Vendor: [ ] Type No. [ ] (光ケーブルの参照)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>

Acceptance Plan for Commercial Grade Dedication 商用品採用受領計画書		Sheet ( 3 / 7 )	
		Document No. FPG-PLN-C51-0008	Rev.1
		Plan Date: April/24/2006	
Length	3.0 m (FPG-DRT-C51-0001 Preliminary Technical Evaluation Report)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Connector Type	FC type connector (6E8H7301 LPRM Unit Users Manual 6E8H7302 APRM Unit Users Manual 6E8H7306 FLOW Unit Users Manual)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
<b>Setpoint of Each Unit</b>			
LPRM Unit Trip Setpoint	LPRM Unit Trip Setpoint can be changed. (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
LPRM/APRM Unit Trip Setpoint	LPRM/APRM Unit Trip Setpoint can be changed. (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Gain Setpoints for All Modules	Gain setpoints can be changed. (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
<b>Performing correct action upon reaching setpoint</b>			
Accuracy of APRM Upscale (High-High) Trip/Reset	Within $\pm 2.0\%$ FS (Trip Reset Point shall be $-1.25\% \pm 0.2\%$ FS). (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Accuracy of Simulated Thermal Power Upscale Trip/Reset	Within $\pm 2.0\%$ FS (Trip Reset Point shall be $-1.25\% \pm 0.2\%$ FS). (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
APRM Inoperable Trip	Trip occurs in the following conditions: (1) When the Mode of the APRM unit is other than "OP". (2) When the Number of bypassed LPRM signals exceeds the permitted number. (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
<b>Change of state of signal when mode is changed</b>			
LPRM Module Mode Switch Operation	Change of state of signal when mode is changed (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>

Acceptance Plan for Commercial Grade Dedication 商用品採用受領計画書		Sheet ( 4 / 7 )	
		Document No. FPG-PLN-C51-0008	Rev.1
		Plan Date: April/24/2006	
APRM Module Mode Switch Operation	Change of state of signal when mode is changed (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
FLOW Module Mode Switch Operation	Change of state of signal when mode is changed (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
<b>Fault condition signal generated during faults</b>			
Self Test Functions and Surveillance Testing Capability for Modules	Compliance with design requirements specified in ERS section 5.1.6. (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
<b>Accuracy</b>			
Input-and-Output Linearity for Units (analog signal)	Within $\pm 2.0\%$ (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Input-Output Linearity for Units (Display)	Within $\pm 2.0\%$ (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Accuracy of Trip/Reset of Modules	Within $\pm 2.0\%$ (Trip Reset Point shall be $-1.25\% \pm 0.2\%FS$ ) (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
<b>Chassis</b>			
Chassis structure for all units	<ul style="list-style-type: none"> <li>Outer surface of the chassis is anodic oxide coating.</li> <li>Inner surface of the chassis is alodine coating.</li> </ul> (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Chassis type, dimensions and mounting for all units	Confirm following points:  D: 440.8 $\pm 4$ (mm) W: 482.6 $\pm 4$ (mm) H: 177 $\pm 2.5$ (mm) Weight 19kg or less Material: Aluminium (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
<b>Module Design</b>			
LVPS Power output	LVPS can supply all the +5, +15, and -15 volt DC power (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>

Acceptance Plan for Commercial Grade Dedication 商用品採用受領計画書		Sheet ( 5 / 7 )	
		Document No. FPG-PLN-C51-0008	Rev.1
		Plan Date: April/24/2006	
Connector Type of all modules	LPRM Unit - Type of connector: SHV connector APRM Unit - Type of connector: SHV connector FLOW Unit - Type of connector: D-SUB connector DIO module - Type of connector: 38 pins ELCO Connector AO module - Type of connector: 38 pins ELCO Connector TRN module, RCV module - Type of connector: FC type connector LVPS module - Type of connector: MS connector (6E8H7301 LPRM Unit Users Manual 6E8H7302 APRM Unit Users Manual 6E8H7306 FLOW Unit Users Manual)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
FPGA type	[ ] FPGAs, models [ ] <sup>a,c</sup> (FPG-DRT-C51-0005 Critical Digital Review Report of NICSD)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
ROM type	EEPROM: equivalent to [ ] <sup>a,c</sup> [ ] <sup>a,c</sup>  - Any memory used for field modifiable constants shall be capable of at least 100,000 write cycles. (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Provision of Grounding/Shielding Points	-Providing a ground connection point on each chassis. -Providing shielding connection points for the I/O module field terminations. (FPG-RQS-C51-0001 Equipment Requirement Specification of FPGA based Units)	Method 3 Source Verification	<ul style="list-style-type: none"> <li>Source Verification Check Sheet and Record</li> <li>Source Verification Report</li> </ul>
Power Supply Line			

Acceptance Plan for Commercial Grade Dedication 商用品採用受領計画書		Sheet ( 6 / 7 )	
		Document No. FPG-PLN-C51-0008	Rev.1
		Plan Date: April/24/2006	
Varistor and Noise Filter type	<ul style="list-style-type: none"> <li>- Varistor (between line for AC connection and ground): [ ]<sup>a,c</sup> for the equivalent one.</li> <li>- Varistor (between neutral for AC connection and ground): [ ]<sup>a,c</sup> for the equivalent one.</li> <li>- Varistor (between line and neutral for AC connection): [ ]<sup>a,c</sup> for the equivalent one.</li> <li>- Noise Filter (between line and neutral for AC connection)[ ]<sup>a,c</sup>, [ ]<sup>a,c</sup> for the equivalent one.</li> </ul>	Method 3 Source Verification	<ul style="list-style-type: none"> <li>· Source Verification Check Sheet and Record</li> <li>· Source Verification Report</li> </ul>
<b>Dependability</b>			
<b>Quality of Design</b> - QA staff and organization definition - QA procedures - Specific Software QA procedures Evidence that QA program was applied in the production	The specific quality assurance activities identified through a valid commercial grade survey implemented effectively.	Method 2 Commercial Grade Survey	<ul style="list-style-type: none"> <li>· Survey Plan</li> <li>· Survey Report</li> </ul>
<b>Quality of Manufacture</b> - QA staff and organization definition - QA procedures - Specific Software QA procedures - Evidence that QA program was applied in the production Module/Unit Testing Procedures	The specific quality assurance activities identified through a valid commercial grade survey implemented effectively.	Method 2 Commercial Grade Survey	<ul style="list-style-type: none"> <li>· Survey Plan</li> <li>· Survey Report</li> </ul>



**Acceptance Plan for Commercial Grade Dedication**

商用品採用受領計画書

Sheet ( 7 / 7 )

Document No. FPG-PLN-C51-0008

Rev.1

Plan Date: April/24/2006

<p>Documentation</p>	<p>Following documents shall be submitted:</p> <ul style="list-style-type: none"> <li>- Engineering Schedule</li> <li>- Submittal Document List</li> <li>- Unit/Module Design Specifications</li> <li>- FPGA Design Specifications</li> <li>- FPGA Control Sheets</li> <li>- Module Parts Lists</li> <li>- Module Circuit Diagrams</li> <li>- Unit Assembly Drawings</li> <li>- Users Manuals</li> <li>- Unit/Module Test Procedures</li> <li>- Unit/Module Test Reports</li> <li>- FPGA Test Procedures</li> <li>- FPGA Test Reports</li> <li>- FE Test Procedures</li> <li>- FE Test Reports</li> <li>- Reliability and Availability Analysis</li> <li>- FMEA Reports</li> <li>- RTM Reports</li> <li>- Master Configuration List</li> <li>- V&amp;V documents (plan and reports)</li> <li>- Unit Electrical Cable Wiring Diagram (ECWD)</li> <li>- Applicable Design/Fabrication/identification and markings procedures.</li> </ul>	<p>Method 3 Source Verification</p>	<ul style="list-style-type: none"> <li>• Source Verification Check Sheet and Record</li> <li>• Source Verification Report</li> </ul>
<p>Documentation that work is performed in accordance with a program that has:</p> <ul style="list-style-type: none"> <li>- Lifecycle V&amp;V requirements</li> <li>- Traceability Requirements (of the boards, etc.)</li> <li>- Document and Coding Control Requirements</li> <li>- Configuration Control requirements</li> <li>- Change Control Requirements</li> <li>- Design Language and Tool Control Requirements</li> </ul> <p>Labeling requirements for logic revision number on chips</p>	<p>Activities are performed in accordance with ERS section 5.3.</p>	<p>Method 2 Commercial Grade Survey</p>	<ul style="list-style-type: none"> <li>• Survey Plan</li> <li>• Survey Report</li> </ul>