HF Controls

HFC-6000 Control System

SLC – Control System Qualification Project

Operability Test Procedure

TP901-203-04 Rev C

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Revision History

Date	Revision	Author	Changes
5/11/10	A	J Taylor	Initial Revision
7/07/10	B	J. Taylor	Revisions per CR2010-0106 and 2010-0161
1/04/11	C	I. Chow	Revisions per CR2010-0306

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1.0 PURPOSE AND SCOPE

Selected components of the HFC-6000 product line will be configured as a single-loop controller (SLC). This controller consists of two PCB assemblies contained in an 8-inch rack. The single-loop controller assembly includes both onboard processor capability and digital I/O. The second PCB provides four each AI and AO channels. This assembly will be mounted in an equipment cabinet with other controller modules that will be tested concurrently to qualify them for use in safety-related applications. The following set of Operability tests are based on test requirements defined by EPRI TR-107330.

- **Accuracy Test** - This test verifies that analog I/O modules in the test specimen meet the accuracy and linearity requirements. (EPRI TR-107330 references: 4.3.2.1, 4.3.3.1, 5.3.A, 6.2.2.B.2, B.6, and B.8)

- **Response Time Test** – This test will measure the response time for discrete and analog inputs from the leading edge of the input to the leading edge of the resulting output (EPRI TR-107330 references: 4.2.1.A, 5.3.B, 6.2.2.B5).

- **Discrete Input Operability Test** - This test will verify the capability of discrete input channels to respond to simulated input signals. (EPRI TR-107330 references: 5.3.C, 6.2.2.B.6)

- **Discrete Output Operability Test** - This test will verify the capability of discrete output channels to produce output signals having specified voltages and currents. (EPRI TR-107330 references: 5.3.D, 6.2.2.B.8)

- **Communication Operability Test** – This test will verify reliable data transfer over all serial communication links associated by the Test Specimen. (EPRI TR-107330 references: 5.3.E)

- **Timer Test** – This test will verify the accuracy of the timer function accessible to the TSAP. (EPRI TR-107330 references: 5.3.G, 6.2.2.B.3)

- **Failure To Complete Scan Detection** – This test will verify the capability of the system software to detect failure to complete at least one execution of the application program during each context switch interval. (EPRI TR-107330 references: 4.2.3.7.A, 4.4.6.3.C, 5.3.H)

- **Loss of Power Test** – This test will demonstrate correct response of all I/O channels to loss of source power followed by reapplication of power to the system. (EPRI TR-107330 references: 5.3.J)

- **Power Interruption Test** – This test will demonstrate the capability of the power modules to sustain system operation during a temporary (transient) power interruption. (EPRI TR-107330 references: 4.6.1.1.F, 5.3.K)

- **Power Quality Tolerance Test** – This test will demonstrate the capability of the Test Specimen to continue normal operation over a range of source power voltages and frequencies. (EPRI TR-107330 References: 4.2.3.7.B, 4.6.1, 6.4.3, 6.4.4.F)

These tests are designed to exercise control system functions to provide a basis for evaluating its performance. The complete set of tests will be run prior to the actual qualification tests to establish a performance baseline for the system. This performance baseline will then be used as the basis for evaluating system performance during and/or following each of the qualification tests to be accomplished.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants (December 1996)

2.2 RELATED PLANS AND PROCEDURES

RS901-200-01	Master Test Plan Rev A
TP901-203-02	Integration Test Plan
VV901-303-02	SLC Master Configuration List

2.3 SUPPORT DOCUMENTATION

UG004-000-01	EWS User's Guide Rev E
UG004-000-16	MCRT User's Guide Rev B
UG004-000-03	HAS User's Guide Rev E

2.4 HFC INTERNAL STANDARDS AND PROCEDURES

Implementation of HFC test programs is based on the current version of the following internal procedures:

QPP 5.1	Review and Approval of Quality Documents, Rev G
QPP 5.2	Preparation of Procedures, Rev M
QPP 11.1	Test Control, Rev H
WI-ENG-003	Configuration Management, Ref E
WI-ENG-205	Develop Software/Firmware Test Procedure, Rev B

2.5 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

C-Link	Communication Link
BOE	Burst of Events
HAS	Historical Archiving System

HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
M&TE	Measuring and Test Equipment
RH	Relative Humidity
SLC	Single Loop Controller
SOE	Sequence of Events
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test System Application Program

3.0 PREREQUISITES

The following paragraphs provide detailed instructions for setup and performance of each Operability test. Operability tests may be run individually or concurrently with other tests. To the maximum extent possible, the individual Operability tests will be automated so that a test engineer can start/stop the selected tests while a qualification test is in progress. However, certain of the operability tests will either disrupt operation of the Test Specimen as a whole or will require direct access to the Test Specimen hardware. Such tests will not be automated or run concurrently with any qualification test.

3.1 EQUIPMENT REQUIRED

A detailed listing of hardware and software components of the Test Specimen are provided in VV901-303-02, Master Configuration List. Detailed requirements for component assembly and interconnection are provided by the engineering drawing package. Detailed requirements for arranging Test Specimen components are provided by section 3.3.2 of this document.

The following equipment and facilities will be required during performance of this test. Test personnel shall verify that all test and measuring equipment are capable of producing the level of accuracy required by the specific test being performed and that the calibration for the M&TE to be used is current.

- PC workstation with EWS and MCRT software installed
- Fluke 187 Multimeter or equivalent
- HP 8116A Function Generator or equivalent
- Relay/timer or equivalent
- Variable ac power source capable of producing an output signal having the following range: 60 to 300 vac, 40 to 65 Hz.
- Stopwatch
- Tektronix TDS3034 Oscilloscope or equivalent (two input channels minimum)

Record all test equipment used during execution of this test in attachment 7.1, Test Equipment Log.

3.2 ENVIRONMENTAL CONDITIONS

This test will be conducted under various environmental conditions. During prequalification testing, the test will be conducted in the HFC test facility under normal ambient environmental condition. The normal range of environmental conditions in the HFC test facility are indicated below. During the qualification tests, required environmental conditions are stipulated within in the procedures governing those tests.

Temperature	50° to 104° F
Relative Humidity	7% to 90% noncondensing

3.3 TEST PERSONNEL

The set of Operability tests will be conducted at the in-house test facility of HFC following completion of the TSAP Validation Test and at vendor facilities during qualification testing. All of the testing and monitoring functions will be conducted by one or more qualified HFC test engineers/technicians both at the HFC facility and at vendor facilities during qualification testing.

3.4 PRECAUTIONS

WARNING

Certain I/O circuits are energized with high voltages and may carry potentially hazardous current loads. Exercise caution whenever working around exposed terminals or circuitry.

3.5 RED-LINE POLICY

The HFC policy for entering red-line corrections into a test procedure are presented in WI-ENG-815, “Red Line” Procedure. Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.6 TEST SETUP REQUIREMENTS

3.6.1 Test Specimen Setup

1. Verify that the copy of the Operability Test Procedure test in hand is a controlled copy of the latest revision according to Document Control records.

2. Verify that all integration testing has been completed successfully.

3. Verify that the TP901-203-02, Integration Test Plan, has been completed successfully and signed off.

Validation that test setup is complete: _____
Name/Date

3.6.2 SOE Point Configuration

An SOE logger will be configured as part of the HPAT (Remote 2). The SOE will be used to monitor high speed (up to ± 1 ms resolution) logic transitions of selected DO and AO channels during operation of the Operability tests. Table 1 lists SOE point assignments for both Operability and Prudency test points. The following procedure describes the sequence of steps necessary to configure the SOE logger prior to running the Operability tests for the first time or following reassembly of the Test Specimen in a vendor's test facility.

1. Configure the SOE to operate without a trigger point or alarm point.

2. Configure the SOE logger with a pre-time cutoff of 90 seconds and a post-time cutoff of 30 seconds.

3. Use the default logger directory.

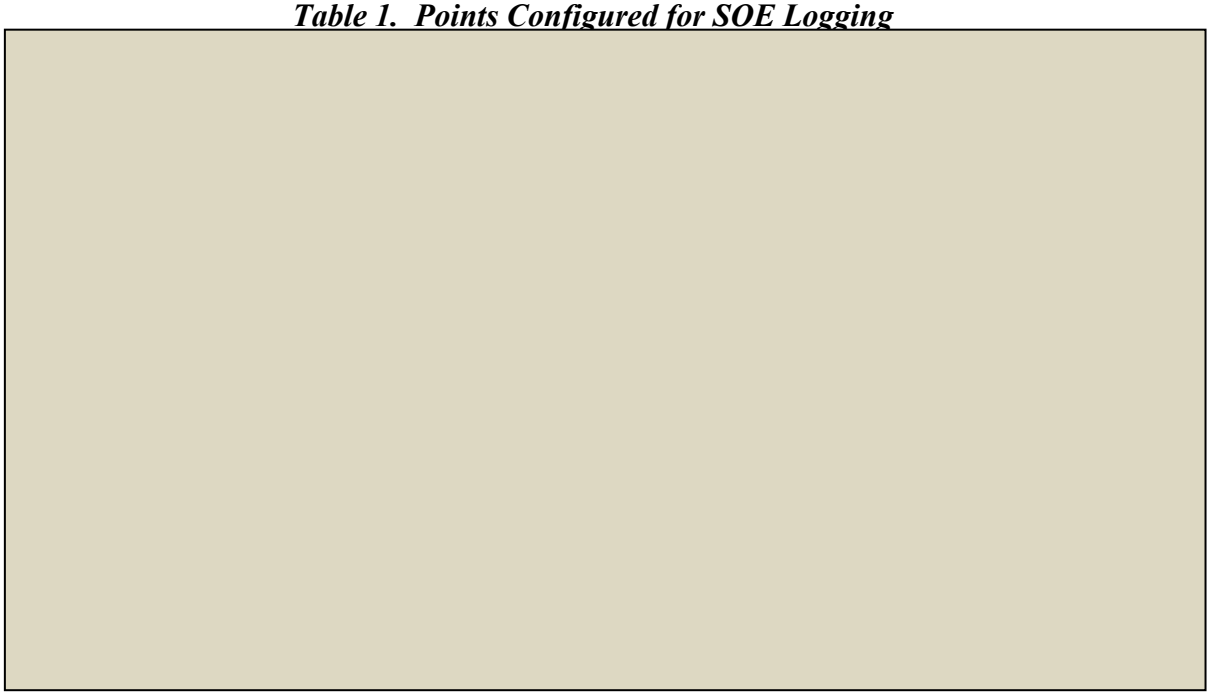
4. Select the Build option to verify that the SOE remote detects all of the SOE cards installed in the SOE remote I/O chassis.

5. Select the Manual Start option.

6. Verify that the SOE subsystem runs an SOE scan to all configured SOE cards.

Validation that SOE setup is complete: _____
Name/Date

Table 1. Points Configured for SOE Logging



3.6.3 HAS Configuration

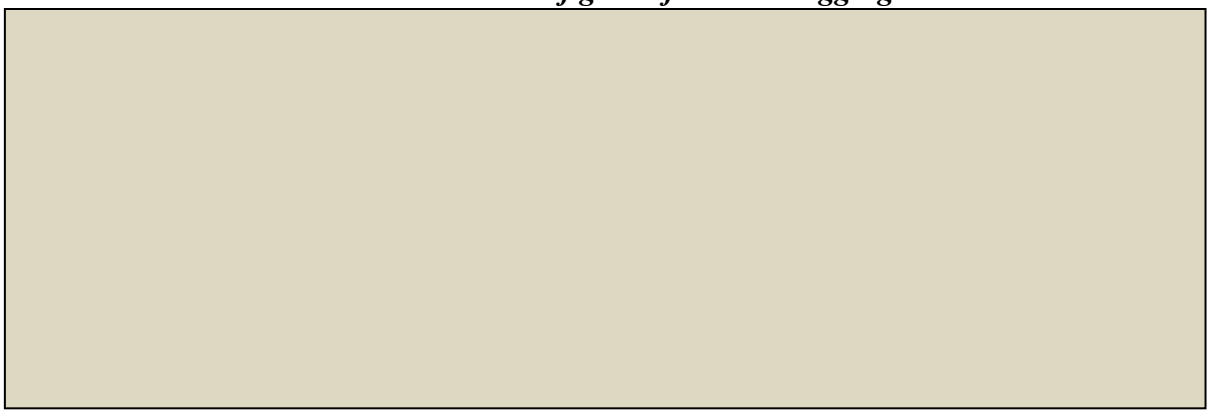
The HFC HAS software utility will be used for logging the value of analog signals as well as digital signals that do not require a time resolution of less than 1 second. Table 2 lists the combination of points selected for HAS logging. (Table 2 includes log points for both Operability and Prudency BOE tests.) The HAS log points shall be configured and verified during the first execution of the Operability and Prudency tests.

1. Enter the HAS log points specified in Table 2. (Refer to the ***HAS User's Guide*** for detailed instructions.)

2. For analog points, set the deadband parameter to 0.0 to ensure that the point will be logged during every update cycle.

3. Save the spreadsheet file and exit.

Table 2. Points Configured for HAS Logging



HAS setup is complete: _____
Name/Date

4.0 OPERABILITY TEST PROCEDURE

Each of the Operability tests provides a separate evaluation for a specific aspect of the Test Specimen performance and operation. No fixed sequence of execution is assumed or implied by the order of specific tests in this document.

4.1 ACCURACY TESTS

The TSAP contains a stair-step analog algorithm (Figure 1) to support automated testing of analog I/O channels. This wave form drives one AO point, and the resulting analog output signal is fed back to an AI point. (The AO channels are rated for 4- to 20 mA, but the AI channels are rated for 0- to 5-v. Hardware modules inside the test cabinet provide the necessary signal conversion.) The test algorithm is fully automated and will be run under two conditions:

- Under ambient operating conditions with no abnormal stress applied
- While specified qualification tests are in progress

This procedure includes both manual and automated test sequences. The complete accuracy test will be conducted during both pre-test and post-test phases. Only the automated test sequences will be executed during the qualification tests. Table 2 lists all

Figure 1. Algorithm for 4- to 20 mA Analog Channel Accuracy Test

4.1.1 Manual Analog Accuracy Test

The waveform shown in Figure 1 is generated by a test algorithm running in the TSAP. As a minimum, manual execution of this test will be conducted during the prequalification and post qualification phases. The purpose of the manual execution of the test is to record the signal level produced by the AO channel at each step level. The purpose of the post test execution is to determine if equipment performance levels remain within acceptable limits.

1. Disconnect the I/O signal lines to the terminal points for AI,23 (BL,19), and connect them to an multimeter. _____
2. Use the MCRT to start the analog accuracy test. _____
3. Use the multimeter to measure the signal level for each step of the analog accuracy test waveform. _____
4. Record the magnitude of the output current from AO,23 for each step level in attachment 7.2.1. Make a minimum of three measurements for each step level. _____
5. On MCRT, display the counter values for the SLC Analog points. _____
6. Record the counter value and the count value for each step level in attachment 7.2.1. _____
7. Use the MCRT to stop the analog accuracy test. _____
8. Reconnect the I/O wires to the terminals to AI,23. _____
9. Use the MCRT to start the analog accuracy test. _____
10. Open the TSAP equation file on the Equation Editor. _____
11. Locate the AIC block processing AI,23 (BL,19), and display the block edit window. _____
12. Record the AI image count value and the block value for each step level in attachment 7.2.1. Record a minimum of three measurements for each step level to establish repeatability. _____
13. Use the MCRT to stop the analog accuracy test. _____

4.1.2 Automated Analog Accuracy Test

The test waveform for the HFC-AC36FD analog I/O channels is generated by an algorithm running in the TSAP on command from the MCRT. No special configuration is required prior to running the automated test. The automated test sequence will be executed after initial execution of the manual test sequences during prequalification testing, and then it will be repeated at specified points throughout qualification testing.

1. Ensure that the HAS.Server program is running. _____

2. Use the MCRT to start the analog accuracy test. _____

3. Allow the test to run for a minimum of three complete cycles of the test waveform (5 minutes) or the duration of the qualification test being run. _____

4. Use the MCRT to stop the analog accuracy test. _____

5. Record the data and time that the test was run in attachment 7.2.2. _____

4.2 RESPONSE TIME TEST

The SLC provides separate test algorithms for supporting direct measurement of analog and digital response time. The test algorithms can be started and stopped from the MCRT workstation, and test points are configured in the SOE logger to support automatic recording of test data.

Repetition of the manual response time tests prior to execution of the qualification tests is not necessary unless one of the I/O modules involved in the test has had to be replaced.

4.2.1 Digital Response Time Measurement

The algorithm for measuring digital response time of the SLC will consist of a free-running square wave generator that produces a trigger pulse (DI,1 in Figure 2) that controls the image of DO,1. This arrangement provides a mechanism for direct measurement of the digital response time from input to output. The resulting response time measurement will include the time required for the following processing steps:

- Input filtering
- Input processing by the I/O hardware
- Transfer over the internal system ICL to the controller
- Transfer over the internal system ICL to the DO interface

The following parameters will be recorded as system baseline values following the initial execution of the digital response time test.

- The calculated average equation cycle time based on the value of CO,50 (equation cycle counter) over a fixed interval.

- The trigger pulse will be generated by the equation interpreter, but the transitions at the DI channel will not be synchronized with I/O scan cycles. As a result, a range of response times will be observed. This range corresponds to the difference between the best case synchronization and the worst case synchronization of the processing cycles involved.

Figure 2. TSAP Algorithm for SLC Digital Response Test

4.2.2 Analog Response Time Measurement

The TSAP provides a test algorithm composed of two blocks and a simulated trip memory to support system response time measurements for analog components. One block receives an input from an AI channel, and the output of that block provides the input to a DHA (digital high alarm) block. (The DHA block is configured with an alarm setpoint of 50% and a deadband of 0.01.) The HPAT application provides an algorithm consisting of a free-running square wave that switches on and off with a period of 16 seconds (8 seconds high, 8 seconds low). This signal drives a DO channel, which is connected to a level conversion circuit. The level conversion circuit performs two functions:

- It converts the 24-vdc DO signal into an analog signal that switches between 0 and 5v (0 to 100%). This signal provides the input to 1,AI,2.
- The TSAP controls AO,2, which is driven directly from the image of AI,2. The conversion circuit uses the AO,2 to control a relay, and the relay output provides a signal that can be detected by the SOE logger.

As a result, the transitions of AI,2, AO,2, and DO,2 are all available for logging. When the response time test is started, the Response Time Trigger logic HPAT starts producing the digital output pulses that produce the test trigger, and the TSAP produces both an AO signal and the simulated trip DO signal. Figure 2 illustrates the TSAP logic and the test waveform used for this test.

Figure 3. TSAP Algorithm for Analog Response Testing

During prequalification testing, an oscilloscope will be used to measure and record the rize time delay from 0 to 50% of span at the input of AI,2 so that the transfer delay from the input of the SLC to the output response can be calculated. During qualification testing, all data will be obtained from the SOE log, and the rize time delay will be used as a correction factor.

4.2.3 Manual Test Sequence

1. Connect channel 1 of the oscilloscope between TB-1-10 (switched +5 vdc) and the negative lead of TB-1-11 (AO input). (The SOE point for the AO of the signal adapter board for TMR) _____
2. Connect channel 2 of the oscilloscope to the terminal points for the AI,2 SOE log point (TB-1-4 and TB-1-8 SOE input signal). _____
3. Use the MCRT to start the Analog Response Time test algorithm. _____
4. Measure the delay between the AO signal and the SOE input signal. Record a minimum of three measurements for both leading and trialing edges in attachment 7.3.2. _____
5. Use the MCRT to stop the Analog Response Time test. _____

4.2.4 Automated Response Time Test Sequence

The automated response time test will be conducted during the prequalification phase of testing after completion of the manual tests, and it will be repeated at specified points during the qualification tests. While the test is running, logic transitions will be recorded automatically by the SOE logger.

1. On the MCRT start the Response Time tests. _____

2. While the response time algorithms are both running, SOE input channels indicate activity. _____

3. Allow the test to run for a minimum of 5 minutes. _____

4. On the MCRT stop the response time test. _____

5. SOE subsystem generates the report file automatically. _____

6. Verify that the SOE report file contains data for the test just run. _____

7. Record the SOE report file name in attachment 7.3. _____

4.3 DISCRETE INPUT OPERABILITY TEST

The purpose of the discrete input operability test is to demonstrate the capability of each type of discrete input channel to detect a transition in the signal being monitored. In order to accomplish this, the channel under test will be subjected to an input signal whose voltage level is controlled by a manual rheostat. The peak value of the input will be at the rated value for the channel, and the minimum value will be 0 volts. During the test, the set voltage level and the reset voltage level for the DI channel under test will be measured. The test will be conducted during the prequalification phase of testing to establish a performance baseline. It will then be repeated at the end of the high temperature phase of the environmental stress tests and during post qualification testing to detect any deterioration in performance.

1. The SLC has only one type of DI channel. DI,2 has been selected for test. _____

2. Connect DI,2 to a rheostat to control the magnitude of the input voltage level. _____

3. Select Repeat mode operation of the Memory Editor. Display the status of the DI images beginning with DI,1. (The normal "OFF" state image is 0100_H; the normal "ON" state image is 8100_H.) _____

4. Slowly increase the input voltage level from 0 v up to the point where the image for DI,2 switches from "OFF" to "ON." Record this voltage level in attachment 7.4. _____

5. Each DI channel in HFC-SBC04A product line is rated for a nominal excitation voltage of 48 v, but the terminal boards in the cabinet are rated for a maximum of 24 VDC. Slowly increase the input signal from turn-on threshold up to a maximum of 24 v. Verify that the DI image remains stable throughout this range. _____

6. Slowly reduce the input voltage level until the DI image switches from "ON" to "OFF." Record this voltage level in attachment 7.4. _____

7. Decrease the input from the reset voltage level to 0. Verify that the DI channel remains "OFF." _____

8. Cycle the input voltage a total of three times. Record the "ON" and "OFF" voltage levels for each cycle. Verify that no other DI channel is affected by the input signal being manipulated. _____

4.4 DISCRETE OUTPUT OPERABILITY TEST

The purpose of the discrete output operability test is to demonstrate the capability of each type of discrete output channel to operate within its specified range of loading conditions. In order to accomplish this, the channel under test will be energized while connected to a simulated field load that will impose maximum loading on the channel. The test will demonstrate the capability for individual channels to sustain such maximum loading conditions without failure and without affecting operation of adjacent channels. The test will be conducted during the prequalification phase of testing to establish a performance baseline. During subsequent testing, this test will be conducted at specified points during the environmental test and during the post test period.

1. The SLC has only one type of DO channel. DO,2 has been reserved for this test. _____

2. Use the MCRT to set this DO channel image to TRUE. _____

3. Verify that the status LED for this channel becomes lit. _____

4.5 COMMUNICATION OPERABILITY TEST

The SLC includes two serial communication links. A redundant Intercommunication Link (ICL) enables the SLC to communicate with Rem 4, and a non redundant ICL enables it to communicate with its configured I/O modules. Because the communication links and the message structures are not accessible during system operation, this test will use link error counters to provide the basis for evaluating the quality of communication on these links. The test will be conducted during the pre-qualification phase of testing and then repeated at specified points during the qualification tests. The overall test method will consist of recording the value of the error counters at the start and end of a test period and interpreting the total accumulated error count as the measure of

communication quality. This test typically will run concurrently with other Operability and Prudency tests.

1. Open one copy of the Memory Editor program. Select Rem 4, memory address 0547:6888, and PCN00. The SLC is configured for slot 2 on the ICL of Rem 4. _____

2. Open a second copy of the Memory Editor program. Select Loop 0291, address 0489:4f4, and PCN00. The SLC has one I/O module configured on its ICL as well as its local digital I/O channels. _____

3. Use the memory editor to read the memory for both controllers. Table 3 defines the content of the ICL diagnostic structure associated with each station in remote 4 configured on the ICL.

   The second data word in the structure contains the cumulative value of the ICL error counter. _____

4. Read the memory in both the remote and the loop controller. Print a copy of the screen capture and append it to attachment 7.6. _____

5. Allow the test to run for a minimum of 5 minutes or the duration of the qualification test being run. _____
6. Take additional screen captures at the end of the test interval to record the cumulative error count. Append printed copies of the screen capture to attachment 7.6.

   _____

7. Record the start and end time of the test in attachment 7.6.

   _____

Table 3. ICL Diagnostic Structures

4.6 TIMER TEST

The timer test will be based on logic completely contained within the TSAP of the SLC. This logic will consist of four pulse timers configured to control two separate free-running square waveforms. The output from one set of timers will be "ON" for 1 second and "OFF" for 1 second; the waveform from the second set will be "ON" for 5 seconds and "OFF" for 1 second. The two waveforms will drive separate DO channels so that the timer periods can be measured directly with an oscilloscope. During qualification testing, the outputs will be routed to separate SOE input channels (Table 1) to permit automatic recording of the signal transitions.

1. The automated timer test does not require any preliminary setup beyond ensuring that signal wires from DO,3 and DO,2 are connected to the correct terminals of the SOE logger. _____

2. Use the MCRT to start the timer test function. Additional tests may run concurrently. _____

3. Allow the test to run for a minimum of 1 minute or the duration of the qualification test being run. _____

4. Use the MCRT to stop the timer test function. _____

5. The SOE subsystem generates the report file automatically. _____

6. Open the SOE report file and verify that the expected data is present. Record the name of the SOE report file in attachment 7.7. _____

4.7 POWER SUPPLY TESTS

A series of three tests will be conducted to establish operability characteristics of the power supplies being used with the test specimen. A single set of power supplies is being used by the TMR, DMR and SLC, and the detailed procedure for executing these tests is contained in TP901-202-04. Pretest setup for the SLC consists of starting the automated accuracy and response time tests to provide a level of background activity.

5.0 ACCEPTANCE CRITERIA

Acceptable results for the operability tests are defined by EPRI TR-107330, which has been used for guidance in developing the qualification test program. The following list presents the design standards for each parameter as published in the HFC specifications for the HFC-6000 product line as well as deviation limits for performance during the qualification tests. A preliminary set of results obtained during the prequalification phase of testing will establish baseline performance characteristics for the SLC Test Specimen, and these results will be used to update the acceptance criteria. Subsequent performance

of the operability tests during the qualification tests will disclose any deterioration from the baseline performance caused by the stress conditions being imposed.

Accuracy Tests Acceptance Criteria

4- to 20-v AI Channels

HFC Design Specification	15 bit AI image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.35% of span over the entire rang

4- to 20-mA AO Channels

HFC Design Specification	12 bit AO image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.35% of span over the entire range

Response Time

Digital Circuit	Average response time shall be 100 ms from activation of the trip condition to output of the trip DO signal
Analog Circuit	Average response time shall be 300 ms from activation of the trip condition to output of the trip DO signal
During Qualification Test	The maximum response time shall not increase by more than 10% from measured baseline value.

Discrete Input Operability

DI set voltage level	Guaranteed DI “ON” level is 20 v at 25° C
DI dropout voltage	Guaranteed DI “OFF” level is 12 to 15 v at 25° C
Maximum input voltage	Maximum input voltage for TMR is 24 v at 25° C

Discrete Output Operability

Solid State DO channels	24 vdc at 300 mA for resistive load

Communication Operability

ICL to Control Remote	Reliable communication continues in the presence of noise/operational stress conditions.
ICL to I/O Modules	Reliable communication continues in the presence of noise/operational stress conditions.

Timer Test	Timer accuracy shall vary by no more than ±1% when averaged over 10 cycles.
Power Supply Tests	Refer to TP901-202-04.

6.0 QA RECORDS

All data generated by execution of the tests covered by this procedure will become QA records. Test data generated during manual execution of the Operability tests will be recorded on the appended Test Data Record sheets. Results for the automated portions of the Operability tests will be recorded in a set of SOE and HAS report files. These files shall be transferred to CDs to provide a permanent, unchangeable record of test results for subsequent analysis.

7.0 ATTACHEMENTS

Test Data Record forms are attached to this document. These forms shall be filled out by the test engineer while the tests are being executed.

Attachment	Description
7.1	Test Equipment Log
7.2	Analog Channel Accuracy Test Records
7.2.1	HFC-AC36FD AO to AI Test Record
7.2.2	HFC-AC36FD AO to AI Automated Test Record
7.3	Response Time Test
7.4	Discrete Input Test
7.5	Discrete Output Test
7.6	Communication Test
7.7	Timer Test
7.8	Power Supply Operability Tests

7.1 Test Equipment Log

Test Equipment	Instrument ID	Cal Due Date

Test Engineer _____ Date _____

7.2 Analog Channel Accuracy Test Records

7.2.1 HFC-AC36FD AO to AI Manual Test Record

Test Step	AO,1		AI,1	
	AO Image (Count Value)	Measured Value (mA)	AI Image (Count Value)	AIC Block Value (%)
10%				
30%				
50%				
70%				
90%				

7.2.2 HFC-AC36FD AO-AI Automated Test Record

All data for the automated AO-AI accuracy test is logged by the HAS. Record time and date for each execution of the automated accuracy test.

Start Time	Stop time

Test Engineer _____ Date _____

7.3 Response Time Test

Digital trigger signal to AI,2 SOE input

Leading edge transfer delay: _____ _____ _____

Trailing edge transfer delay: _____ _____ _____

SOE Report File Name(s):

7.4 Discrete Input Test

Card Type Under Test	HFC-SBC04A		
Input Channel Rating	_____		
ON Voltage Threshold (3 cycles minimum)	_____	_____	_____
Maximum Input Voltage (3 cycles minimum)	_____	_____	_____
OFF Voltage (3 cycles minimum)	_____	_____	_____

7.5 Discrete Output Test

Card Type Under Test	HFC-SBC04A
DO Stratus "ON" verified	_____
DO Status "OFF" verified	_____

Test Engineer _____ Date _____

7.6 Communication Test

	Loop 0291 ICL Status	Rem 4 ICL Status
Time at Start of Test		
Time at end of Test		
Duration		

Append Screen Captures

7.7 Timer Test

Record SOE Report file name(s) for automated test execution.

7.8 Power Supply Operability Tests

Refer to the test data record for TMR Operability Test Results.

Test Engineer _____ Date _____