Entergy

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GNRO-2015/00012

March 3, 2015

U.S. Nuclear Regulatory Commission
Attn: Document Control Desk
Washington, DC 20555-0001

SUBJECT: Response to License Amendment Request for Revision of Five Technical Specification Allowable Value Setpoints Request for Additional Information
Grand Gulf Nuclear Station, Unit 1
Docket No. 50-416
License No. NPF-29

REFERENCES:
1. Electronic Request for Additional Information Regarding "License Amendment Request for Revision of Five Technical Specification Allowable Value Setpoints."
2. Entergy Letter, "License Amendment Request for Revision of Five Technical Specification Allowable Value Setpoints," GNRO-2014/00014, dated August 1, 2014 (ADAMS Accession No. ML14216A383).

Dear Sir or Madam:

Entergy Operations, Inc. is providing in Attachment 1 a response to the Reference 1 Request for Additional Information (RAI). The RAI is in response to the Reference 2 License Amendment Request (LAR). Attachments 2-6 provide supporting vendor information.

This letter contains no new commitments. If you have any questions concerning this submittal, please contact Mr. James Nadeau at (601) 437-2103.

I declare under penalty of perjury that the foregoing is true and correct; executed on March 3, 2015.

Sincerely,

KJM/tmc

Attachments: 1. Response to Request for Additional Information

Attachments (continued):

2. TR Model Relay Vendor Information
3. ETR Model Relay Information
4. LSS Vendor Manual
5. LSS Vendor Information
6. LSS Reset Information

cc:

U.S. Nuclear Regulatory Commission
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U.S. Nuclear Regulatory Commission
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NRC Senior Resident Inspector
Grand Gulf Nuclear Station
Port Gibson, MS 39150

Dr. Mary Currier, M.D., M.P.H
State Health Officer
Mississippi Department of Health
P.O. Box 1700
Jackson, MS 39215-1700

Attachment 1
to GNRO-2015/00012

Response to Request for Additional Information

1) The license amendment request (LAR) requests correction of five non-conservative technical specification allowable values. However, the LAR does not explain how the licensee determined the current allowable values to be non-conservative, and thus the changes requested in the amendment. Please explain how the current allowable values in the technical specification (TS) were not conservative and therefore resulted in the need for correcting these values.

   Response:

   The current Tech spec AV's were determined to be non-conservative based on new revisions to the associated setpoint calculations that were provided to the NRC in the August 1, 2014, LAR.

   When the allowable values for the Containment Spray Actuation Time Delay and ADS System Initiation Time Delay were originally derived by GE they assumed a 2% repeatability / accuracy (reference 22A3856AA and 22A3139AK). PERR 93/D8630 rev 1 authorized the replacement of obsolete 164C5257 (FTR) relays that have a 2% repeatability / accuracy (normal environment) with 169C9488 (ETR) relays that have a 5% repeatability / accuracy (normal environment) without addressing the accuracy difference and the impact on associated setpoint calculations JC-Q1B21-K114 or JC-Q1E12-K093. MNCR 0652-83 earlier approved the replacement of the FTR relay with the ETR relay. It incorrectly assumed that the extreme environment 10% accuracy / repeatability specification (which applies to both the FTR and ETR) was utilized. The revised calculations conservatively assume a 5% repeatability / accuracy for the ETR relays. Based on the revised calculation JC-Q1B21-K114, a conservative AV of 115 seconds is being proposed for the ADS initiation timer. Based on the revised calculation JC-Q1E12-K093, a conservative lower AV of 10.6 minutes is being proposed for the Containment spray timers.

   Per calculation JC-Q1R21-90024-1, no allowance for loop uncertainty exists between the 3744 V lower analytic limit and the lower allowable value currently specified in tech spec table 3.3.8.1-1 for the 4160 VAC Div 1 & 2 degraded voltage setpoint. Based on the revised calculation JC-Q1R21-90024-1, a conservative AV of 3764.25 VAC is being proposed for the Div 1 and 2 Degraded 4.16 KV Bus Voltage.

   Per calculation JC-Q1P81-90024, the 3558.8 VAC lower allowable value currently Specified for the Div 3 degraded voltage setpoint is slightly non-conservative. Based on the revised calculation JC-Q1P81-90024, a conservative lower AV of 3605 VAC is being proposed for the Div 3 Degraded 4.16 KV Bus Voltage.

   Per calculation JC-Q1P81-90024, the 3.6 second lower allowable value currently Specified for the Div 3 degraded voltage setpoint time delay is slightly non-conservative. Based on the revised calculation JC-Q1P81-90024, a conservative lower AV of 3.68 seconds is being proposed for the Div 3 Degraded 4.16 KV Bus Voltage time delay.

2) Section 2.1 in the LAR lists the proposed changes for the five TS allowable values, in addition to information regarding the current Allowable Value (AV) identified in the Technical Specifications. The staff noted the Current AV for Sys A & B Containment Spray Timers is listed in this section as ≥ 10.25 min. However, the Technical Specifications in Attachments 2 and 3 (TS pages) list the Current AV as ≥ 10.26 min. Please explain the inconsistency with the value reported for Sys A & B Containment Spray Timers.

   Response:

   The Tech Spec currently specified lower AV for the containment spray timers is 10.26 minutes. The 10.25 second value in the LAR is a typo.

3) In Attachment 4 of the LAR, the licensee provided its calculation JC-Q1B21-K114, Instrument Uncertainty and Setpoint Determination for the System IB21-ADS, Initiation Timer Setpoint Validation. The staff has the following questions regarding this calculation:

   a. Section 2.0, "Design Requirements," (Sheet 7 of 62) identifies the current Technical Specification AV as ≤ 117 seconds. If the LAR is approved and the changes to the TS are implemented, this value in the Design Requirements section of the calculation will no longer be consistent. What is the plan to revise the Design Requirements to reflect the correct TS allowable value?

      Response:

      The calculation will be revised after the LAR is approved.

   b. Section 4.4, "1B21CK005A,B, ADS Timer Vendor Data," (Sheet 11 of 62) provides detailed information taken from the vendor data sheets, including accuracy, repeatability, and environmental capabilities. However, this calculation does not provide the vendor data sheets for the automatic depressurization system (ADS) Timers impacted by this calculation included with the LAR. Please identify the specific model of ADS Timer that is being used and provide a copy of the vendor data sheets for this model so staff can verify the specifications used in the calculation are accurate.

      Response:

      Vendor data for the TR and ETR model relays is attached.

4) In Attachment 5 of the LAR, the licensee provided its calculation JC-Q1E12-K093, Instrument Uncertainty and Setpoint Determination for System E12 Containment Spray Actuation Timer. The staff has the following questions regarding this calculation:

   a. Section 2.0, "Design Requirements" (Sheet 6 of 47), identifies the current Technical Specification AV as ≥ 10.26 min and ≤ 11.44 min, which are the

current AVs before this LAR is approved. If the LAR is approved and the changes to the TS are implemented, these values in the Design Requirements section of the calculation will no longer be consistent. What is the plan to revise the Design Requirements to reflect the correct TS allowable value?

Response:

The calculation will be revised after the LAR is approved.

b. Sections 7.12, licensee event report (LER) Avoidance System A Loop, and Section 7.13, LER Avoidance System B Loop, (Sheet 20 of 47) calculate the Z value for the LER avoidance for the System A Loop and System B Loop, respectively. The General Electric setpoint methodology identifies a minimum acceptable value for the Z value. However, this section shows the values for System A and System B are below the minimum acceptable Z value for 90% LER avoidance. Please explain the reason for accepting the Z value values for System A and System B.

Response:

The as-found and as-left data for the relays over a 6.7 year period was collected for the relays and is included in the calculation. During this time period the as-found setting was never below the proposed 10.6 minute (636 second) allowable value.

c. Section 4.3, 1E12K093A, B Vendor Data, and Section 4.4, 1E12AK116 Vendor Data, (Sheet 9 and 10 of 47) provides detailed information taken from the vendor data sheets including accuracy, repeatability, and environmental capabilities. There are no copies of the vendor data sheets for the ETR model timers that are impacted by this calculation included with the LAR. Please provide a copy of the vendor data sheets for this model so that staff can verify the information from the vendor data sheets that is used within the calculation is accurate.

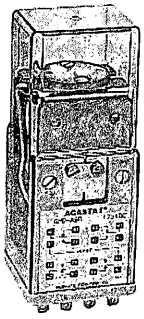
Response:

Vendor data for the ETR model relays is attached.

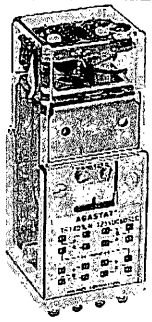
In Attachment 6 in the LAR, the licensee submitted its calculation JC-Q1R21-90024-1, Division 1 & 2 Degraded 4.16 KV Bus Voltage Setpoint Validation. Section 3.2.4, Uncertainty Effects – Time Delay Relay, (Sheet 9 of 23) provides detail information taken from the vendor data sheets including accuracy and environmental capabilities. However, this calculation does not provide the vendor data sheets for the bistable logic cards and time delay one shot cards that are impacted by this calculation. Please provide a copy of the vendor data sheets for the bistable and time delay cards so that staff can verify the information from the vendor data sheets that is used within the calculation is accurate. A copy of the vendor manual and vendor correspondence is attached.

Attachment 2
to GNRO-2015/00012

TR Model Relay Vendor Information



SERIES GP



SERIES TR

GP/ML/TR series

10 Amp Control Relay
Non-latching, Latching & Timing Versions

File E15631 File LR29186

Users should thoroughly review the technical data before selecting a product part number. It is recommended that users also seek out the pertinent approvals files of the agencies/laboratories and review them to ensure the product meets the requirements for a given application.

GP/ML/TR Design Features

Among the advances AGASTAT control relays offer over existing designs is a unique contact operating mechanism. An articulated arm assembly amplifies the movement of the solenoid core, allowing the use of a short stroke coil to produce an extremely wide contact gap. The long support arms used in conventional relays are eliminated. Both current capacity and shock/vibration tolerance are greatly increased, as well as life expectancy.

Design/Construction

AGASTAT control relays are operated by a moving core electromagnet whose main gap is at the center of the coil. A shoe is fitted to the core which overlaps the yoke and further increases the magnetic attraction.

The coil itself is in the form of an elongated cylinder, which provides a low mean turn length and also assists heat dissipation. Since the maximum travel of the electromagnet does not provide optimum contacts movement, an ingenious amplifying device has been designed.

This consists of a W-shaped mechanism, shown in figure 1. When the center of the W is moved vertically the lower extremities move closer to each other as can be seen in the illustration. The center of the W mechanism is connected to the moving core of the electromagnet and the two lower points are connected to the moving contacts.

Two of these mechanisms are placed side-by-side to actuate the four contacts sets of the relay. The outer arms of the W mechanisms are leaf springs, manufactured from a flat piece of non-ferrous metal. These outer arms act as return springs for their corresponding contacts. This provides each contact with its own separate return spring, making the contacts independent.

The mechanical amplification of the motion of the electromagnet permits a greater distance between the contacts, while the high efficiency of the electromagnet provides a nominal contact force in excess of 100 grams on the normally open contacts.

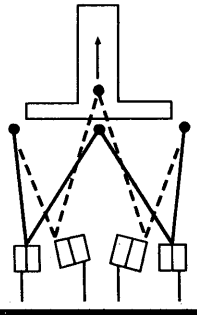
All the contacts are positioned well away from the cover and are well ventilated and separated from each other by insulating walls.

The absence of metal-to-metal friction, the symmetrical design of the contact arrangement and the lack of heavy impacts provides a mechanical life of 100,000,000 operations.

For use in AC circuits, the relay is supplied with a built-in rectification circuit, thus retaining the high DC efficiency of the electromagnet. The current peak on energizing is also eliminated and consequently the relay can operate with a resistance in series (e.g. for high voltages or for drop-out by shorting the coil). The use of the rectification circuit offers still other advantages. The same model can operated at frequencies ranging from 40 to 400 cycles. Operation of the relay is crisp; even with a low AC voltage, there is a complete absence of hum and vibration.

The plastic dust cover has two windows through which the iron yoke protrudes to facilitate cooling and also to allow direct mounting arrangement of the relay irrespective of the terminals.

Figure 1 – Illustration of Amplification



This diagram illustrates amplification obtained by the articulated operating mechanism.

NOTE: Seismic & radiation tested EGP, EML and ETR models are available. Consult factory for detailed information.

Features

- Occupies very small panel space
- May be mounted singly, in continuous rows or in groups.
- Available with screw terminal molded socket.
- 4 SPDT contacts.
- Magnetic blowout device option increases DC current carrying ability approximately ten times for both N.O. and N.C. contacts. In both AC and DC operation, the addition of the device will normally double the contact life, due to reduced arcing.

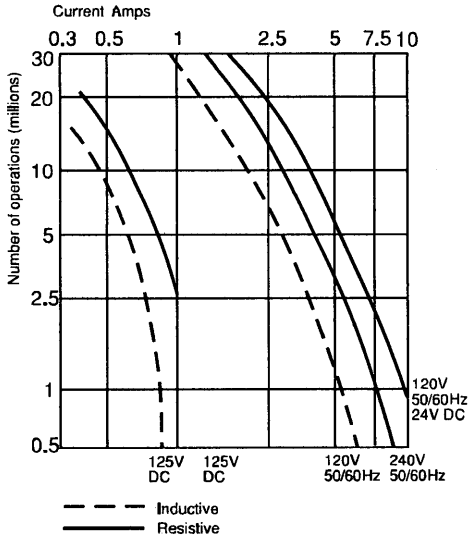
GP/ML Contact Data @ 25°C

Arrangements: 4 Form C (4PDT)
Material: Siver plated.
Ratings: See chart.
Expected Life: **Mechanical:** 100 million operations.
Electrical: See chart and graph.

Contact Ratings and Expected Life

Voltage	Current (Amps)	Power Factor or Time Constant	Number of Electrical Operations	Remarks
540 VAC	3	COS Ø = 0.5	15,000	2 contacts in series
380 VAC	15	Resistive	10,000	2 contacts in parallel
380 VAC	10	Resistive	200,000	
380 VAC	3 x 3.3	COS Ø = 0.8	200,000	3hp motor
220 VAC	20	Resistive	20,000	2 contacts in parallel
220 VAC	15	COS Ø = 0.5	20,000	2 contacts in parallel
220 VAC	10	Resistive	400,000	
220 VAC	3 x 6	COS Ø = 0.8	200,000	3hp motor
220 VAC	5		1,500,000	Filament lamps
220 VAC	5	Resistive	3,000,000	
220 VAC	2.5	COS Ø = 0.25	2,000,000	
220 VAC	2	Resistive	15,000,000	
220 VAC	1.25	Resistive	30,000,000	
120 VDC	1.5	Resistive	20,000,000	with blow-out device
48 VDC	10	Resistive	1,000,000	

Load Life Curve



Initial Dielectric Strength

Between non-connected terminals: 2,000V rms, 60 Hz.
Between non-connected terminals & relay yoke: 2,000V rms, 60 Hz.

Initial Insulation Resistance

Between non-connected terminals: 10^9 ohms at 500VDC.
Between non-connected terminals & relay yoke: 10^9 ohms at 500VDC.

Coil Data

Voltage: 24, 120 & 220VAC, 60 Hz. Add series resistor for 380-440VDC; 12, 24, 48, 125 & 250VDC.

Duty Cycle: Continuous.
Nominal Coil Power: 6VA for AC coils; 6W for DC coils.
There is no surge current during operation.

Coil Operating Voltage

	DC					AC, 50/60Hz		
Nominal Coil Voltage	12	24	48	125	250	24	120	220
Minimum Pick-up Voltage at 20°C	9	18	36	94	187	19	92	175
Minimum Pick-up Voltage at 40°C	9.5	19	38	100	200	20	102	188
Maximum voltage for continuous use	13.5	27	53	143	275	27	137	245

For 380VAC – Use 6800 ohms 4 watt resistor in series with 220VAC relay.
For 440VAC – Use 8200 ohms 6 watt resistor in series with 220VAC relay.

Drop-out voltage is between 10% and 40% of the nomninal voltages for both DC and AC (For example: in a 120 VAC unit, drop-out will occur between 12 and 48 volts.) DC relays will function with unfiltered DC from a full-wave bridge rectifier.

Operate Data @ 20°C

Operate Time at Rated Voltage: Between energizing and opening of normally closed contacts, less than 18 milliseconds on AC and less than 15 milliseconds on DC.
Release Time: Between energizing and closing of normally open contacts, less than 35 milliseconds on AC and less than 30 milliseconds on DC. Between de-energizing and opening of normally open contacts, less than 70 milliseconds on AC and less than 8 milliseconds on DC. Between de-energizing and closing of normally closed contacts, less than 85 milliseconds on AC and less than 25 milliseconds on DC.

Environmenal Data

Operating Temperature Range: 0°C to +60°C.
Vibration: Single axis fragility curve data are available on request at frequencies from 5 Hz. to 33 Hz.
Shock: The relay, when kept energized by means of one of its own contact sets, will withstand 40g shock load when operating on DC, and 150g shock load on AC.

Mechanical Data

Mounting Terminals: 16 flat base pins. Screw terminal sockets are available.
Wire Connection: The 16 flat pins are arranged in four symmetrical rows of four pins; the pitch in both directions being .394". Connection may be made to the relay by soldering. Sockets are available with screw terminals.
The internal wiring of the relay is also symmetrical as shown in the adjacent figure, allowing the relay to be inserted into the socket in either of two positions. Terminals B2 and B3 are provided as extra connections for special applications.
Weight: 10.9 oz. (308g) approximately.

Ordering Information

Typical Part No. ➤ GP | I | N

1. Basic Series:
GP = Non-latching Control Relay
ML = Magnetic Latching Control Relay

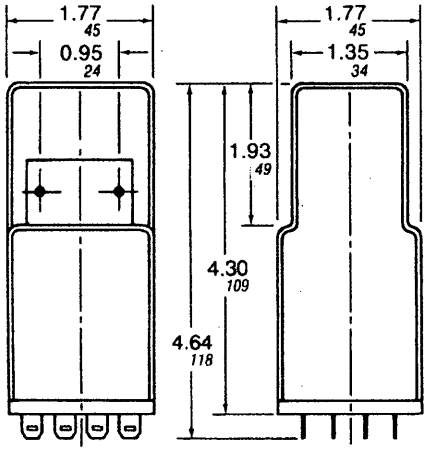
2. Coil Voltage:
A = 12VDC
B = 24VDC
C = 48VDC
D = 125VDC
F = 250VDC
G = 24VAC, 60 Hz.
I = 120VAC, 60 Hz.
J = 220VAC, 60 Hz.

3. Options:
N = Magnetic Blow-out Device
Q = Light to indicate coil energization (GP only. 120VAC, 125VDC, 220VAC and 250VDC voltages only.)
R = Internal diode to suppress coil de-energization transient. (GP only. When used on DC unit, relay release time increases to same value as AC unit).

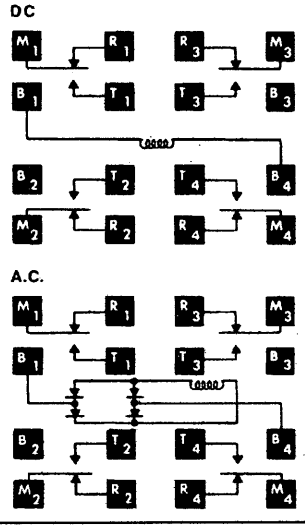
Our authorized distributors are more likely to maintain the following items in stock for immediate delivery..

GPD
GPDN

Outline Dimensions



Wiring Diagrams (Bottom Views)



Dimensions are shown for reference purposes only.
Dimensions are in inches over (millimeters) unless otherwise specified.
Specifications and availability subject to change.
www.tycoelectronics.com
Technical support:
Refer to inside back cover.

TR series

10 Amp Control Relay – Timing Version

TR Features

- 8 timing ranges.
- 4 SPDT contacts.
- Magnetic blowout device option increases DC current carrying ability approximately ten times for both N.O. and N.C. contacts. In both AC and DC operation, the addition of the device will normally double the contact life, due to reduced arcing.

TR Design/Construction

Couples an advanced electromechanical design with a field-proven solid-state timing network, an adaptation of the circuit used in the AGASTAT premium grade SSC Timer.

This unique circuit also eliminates the need for supplementary temperature-compensation components, affording unusual stability over a realistically broad operating temperature range. It also provides transient protection and protection against premature switching of the output contacts due to power interruption during timing.

Timing Specifications

Operating Mode: On-Delay (Delay on energization).
Timing Adjustment: Internal fixed or internal potentiometer.
Timing Ranges:

.15 to 3 sec.	4 to 120 sec.
.55 to 15 sec.	10 to 300 sec.
1 to 30 sec.	1 to 30 min.
2 to 60 sec.	2 to 60 min.

Accuracy:
Repeat: ±2% as fixed temerature and voltage.
Overall: ±5% over combined rated extremes of temerature and voltage.
Reset Time: 75ms.

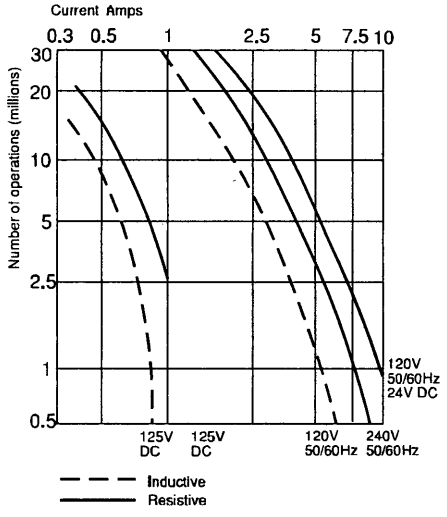
Contact Data @ 25°C

Arrangements: 4 Form C (4PDT)
Nominal Rating: 10A @ 120VAC.
Contact Pressure:
Between movable and normally closed contacts: 30 g, typical.
Between movable and normally open contacts: 100 g, typical.
Expected Life: **Mechanical:** 100 million operations.
Electrical: See load/life graph.

Initial Dielectric Strength

Between terminals and case and between mutually-isolated contacts: 2,000VAC.

Load Life Curve



Initial Insulation Resistance

Between non-connected terminals: 10^9 ohms at 500VDC.
Between non-connected terminals & relay yoke: 10^9 ohms at 500VDC.

Coil Data

Voltage: 120VAC, 50-60 Hz.; 24 & 125VDC.

Transient Protection

1,500 volt transient of less than 100 microseconds, or 1,000 volts or less.

Environmenal Data

Operating Temperature Range: 0°C to +50°C.

Mechanical Data

Mounting Terminals: 16 flat base pins. Screw terminal sockets are available.
Weight: 11 oz. (311g) approximately.

Ordering Information

Typical Part No. ➤	TR	1	4	B	1	A	N

1. Basic Series:
TR = Timing control relay

2. Operation:
1 = On-delay

3. Output:
4 = 4PDT (4 form C)

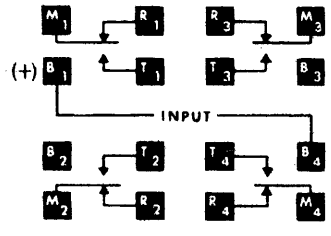
4. Operating Voltage:
B = 24VDC D = 215VDC I = 120VAC, 50/60 Hz.

5. Timing Adjustment:
1 = Internal fixed. 3 = Internal potentiometer.

6. Timing Range:
A = .15 to 3 sec. C = 1 to 30 sec. E = 4 to 120 sec. I = 2 to 60 min.
B = .55 to 15 sec. D = 2 to 60 sec. G = 10 to 300 sec. N = 1 to 30 min.

7. Options:
N = Magnetic blow-out device.

Wiring Diagram (Bottom View)



Outline Dimensions

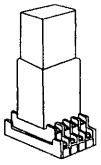
Same as GP/MR. See previous page.

Our authorized distributors are more likely to maintain the following items in stock for immediate delivery..

None at present.

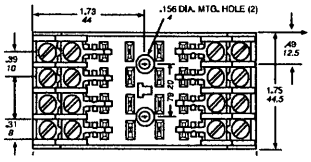
Accessories for GP/ML/TR series control relays

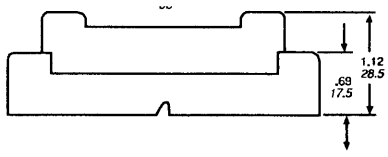
Front connected sockets

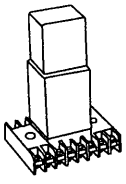


Cat. No. CR0001
With captive clamp terminals

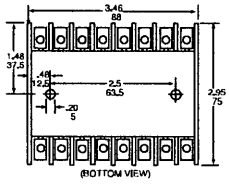
Cat. No. CR0002
With (#6) binding head screws

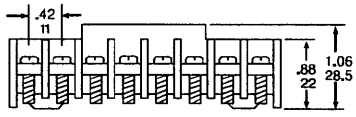




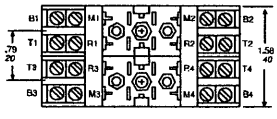


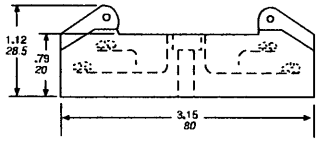
Cat. No. CR0095
With (#6) screw terminals



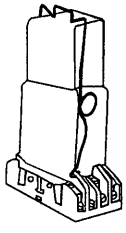


Cat. No. CR0067
With (#6) screw terminals

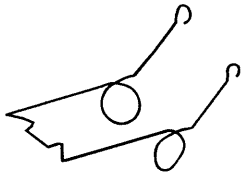


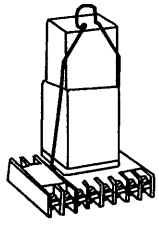


Hold down (locking) springs

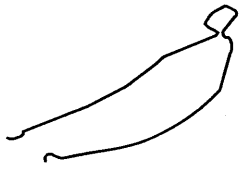


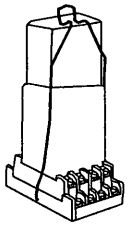
Cat. No. CR0069
For socket: CR0067





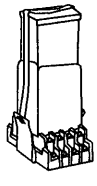
Cat. No. CR0070
For socket: CR0095



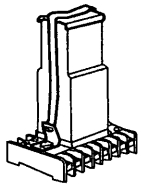


Cat. No. CR0111
For sockets: CR0001& CR0002

Heavy-duty hold down (locking) straps



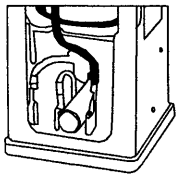
***Cat. No. CR0133**
For socket: CR0001 & CR0002



***Cat. No. CR0155**
For socket: CR0095

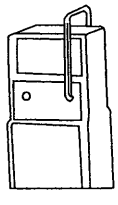
* Catalog number includes strap, strap plate and necessary brackets.

Magnetic blowout device



Cat. No. CR0190
Reduces arcing on the relay contacts when they make or break contact, either upon energizing or de-energizing, resulting in less contact degradation. Extends the life of the contact.

Extracting handle



Cat. No. CR0179
Used to remove GP, ML and TR units from mounting bases.

Attachment 3
to GNRO-2015/00012

ETR Model Relay Information

AGASTAT nuclear qualified control relays

seismic & radiation tested

In order to satisfy the growing need for electrical control components suitable for class 1E service in nuclear power generating stations, Thomas & Betts offers a series of AGASTAT® control relays which have been tested for these applications. Series EGP, EML and ETR have demonstrated compliance with the requirements of IEEE Standards 323-1974 (Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations) and IEEE Standard 344-1975 (Seismic Qualification for Nuclear Power Generating Stations). Testing was also referenced to ANSI/IEEE C37.98 (formerly IEEE Standard 501-1978, Standard for Seismic Testing of Relays).

The design of Series EGP, EML and ETR control relays has evolved over 20 years of continual use in a wide range of industrial applications. Power Relay, Magnetic Latch and Timing Relay versions are available for use with a choice of coil voltages, as well as an internal fixed or adjustable potentiometer in the Series ETR time delay version.

Thomas&Betts

test procedure

TEST PROCEDURE

AGASTAT® control relay Series EGP, EML and ETR were tested in accordance with the requirements of IEEE STD. 323-1974 (Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations), IEEE STD. 344-1975 (Seismic Qualification for Nuclear Power Generating Stations) and referenced to ANSI/IEEE C37.98 (formerly IEEE Standard 501-1978, Standard for Seismic Testing of Relays). The relays were tested according to parameters which, in practice, should encompass the majority of applications. Documented data apply to relays which were mounted on rigid test fixtures. The following descriptions of the tests performed are presented in their actual sequence.

RADIATION AGING

Relays were subjected to a radiation dosage of 2.0 X 10^6 Rads, which is considered to exceed adverse plant operating requirements for such areas as auxiliary and control buildings.

CYCLING WITH LOAD AGING

The radiated units were then subjected to 27,500 operations at accelerated rate, with one set of contacts loaded to 120VAC, 60Hz at 10 amps; or 125VDC at 1 amp, and the number of mechanical operations exceeding those experienced in actual service.

TEMPERATURE AGING

This test subjected the relays to a temperature of 100°C for 42 days, with performance measured before and after thermal stress.

SEISMIC AGING

Sufficient interactions were performed at levels less than the fragility levels of the devices in order to satisfy the seismic aging requirements of IEEE STD 323-1974 and IEEE STD 344-1975.

SEISMIC QUALIFICATION

Artificially aged relays were subjected to simulated seismic vibration, which verified the ability of the individual device to perform its required function before, during and/or following design basis earthquakes. Relays were tested in the non-operating, operating and transitional modes.

HOSTILE ENVIRONMENT

Since the relays are intended for use in auxiliary and control buildings, and not in the reactor containment areas, a hostile environment test was performed in place of the Loss of Coolant Accident (LOCA) test. Relays were subjected to combination extreme temperature/humidity plus under/over voltage testing to prove their ability to function under adverse conditions even after having undergone all the previous aging simulation and seismic testing. The devices were operated at minimum and maximum voltage extremes: 85 and 120 percent of rated voltage for AC units, and 80 and 120 percent of rated voltage for DC units, with temperatures ranging from 40°F to 172°F at 95 percent relative humidity.

BASELINE PERFORMANCE

In addition to aging tests, a series of baseline tests were conducted before, and immediately after each aging sequence, in the following areas:

- Pull-in Voltage
- Drop-out Voltage
- Dielectric Strength at 1650V 60Hz
- Insulation Resistance
- Operate Time (milliseconds)
- Recycle Time (milliseconds)
- Time Delay (seconds) } Series ETR only
- Repeatability (percent) }
- Contact Bounce (milliseconds at 28VDC, 1 amp.)
- Contact Resistance (milliohms at 28VDC, 1 amp.)

Data were measured and recorded and used for comparison throughout the qualification test program in order to detect any degradation of performance.

The SRS shape (at 5 percent damping), is defined by four points:
point A = 1.0 Hz and an acceleration equal to 25 percent of the Zero Period Acceleration
point D = 4.0 Hz and 250 percent of the ZPA
point E = 16.0 Hz and 250 percent of the ZPA
point G = 33.0 Hz and a level equal to the ZPA

SPECIMEN 13, 15 & 16 (EGP SERIES)
RELAY STATE: NON-OPERATE MODE (DE-ENER.)
TEST RUN NO. 318, 319, (205-206), (198-199)
AXIS (H+V):
COMPOSITE OF FB/V-, SB/V, SB/V+, FB/V+ X .707
DUE TO 45° INCLINATION OF TEST MACHINE.

FULL SCALE SHOCK SPECTRUM (g Peak) MODELS TESTED:
1.0 ☐ 10 ☐ 100 ☒ 1000 ☐ EGPD001 EGPD001
DAMPING 5%

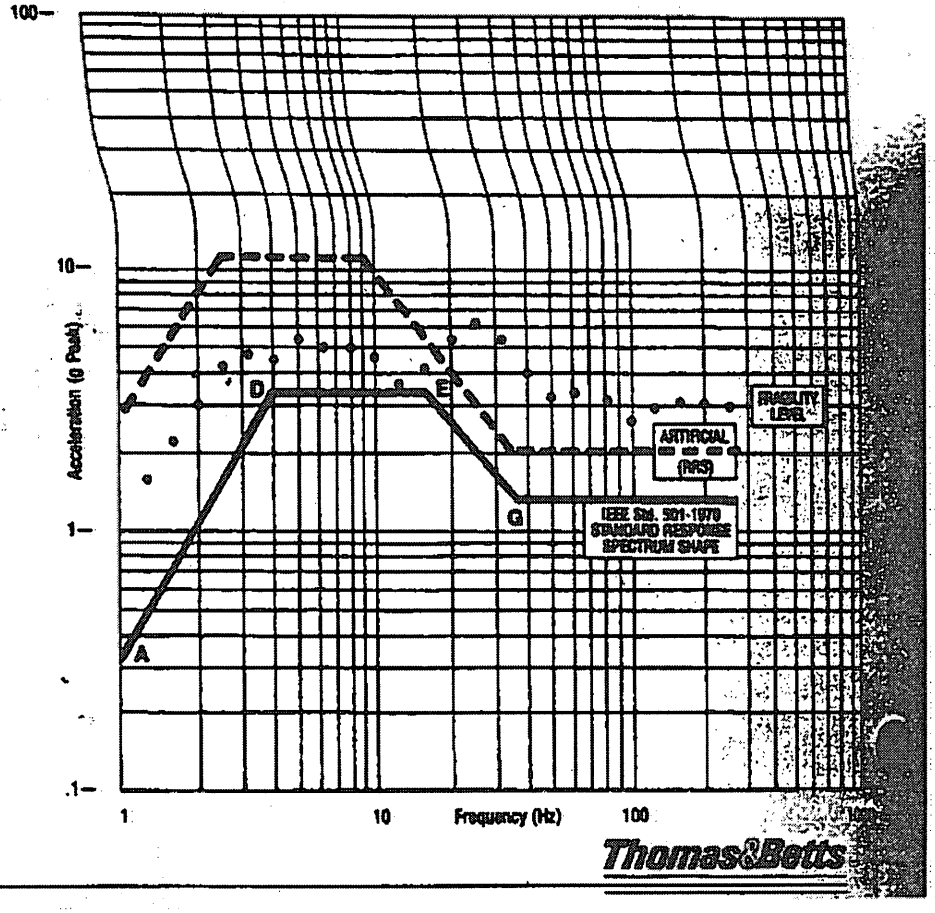


Figure 1. Model EGP, Response Spectrum, Non-Operate Mode

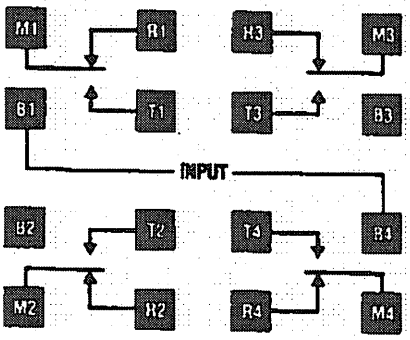
RELAY STATE: *NON-OPERATE MODE* (DE-ENER.)
TEST RUN NO. 318, 319, (205-206), (198-199)

Additional Seismic Response Curves are available on request from the Sales Application Engineering Department of Industrial Electrical Products, Livingston, New Jersey.

operation

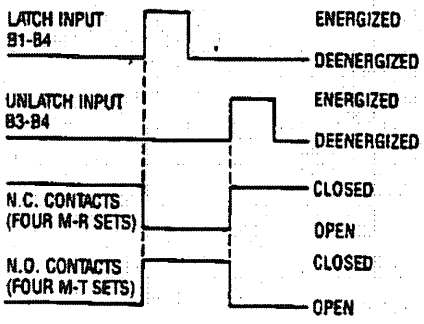
SERIES EGP
Power Relay

Applying a continuous voltage to the coil (B1-B4) energizes the coil and instantaneously transfers the switch, breaking the normally closed contacts (M1-R1, M2-R2, M3-R3, M4-R4) and making the normally open contacts (M1-T1, M2-T2, M3-T3, M4-T4). The contacts remain in this transferred position until the coil is deenergized, at which time the switch instantaneously returns the contacts to their original position.



SERIES EML
Magnetic Latch

Application of a voltage to the latching input (B1-B4) will cause the relay to latch in (Make the N.O. Contacts, break the N.C. Contacts). When this voltage is removed, the relay will remain in this "Latched" condition. Application of a voltage to the un-latching input (B3-B4) will cause the relay to dropout (Break the N.O. Contacts, make the N.C. Contacts). When this voltage is removed the relay will remain in this "Unlatched" condition.

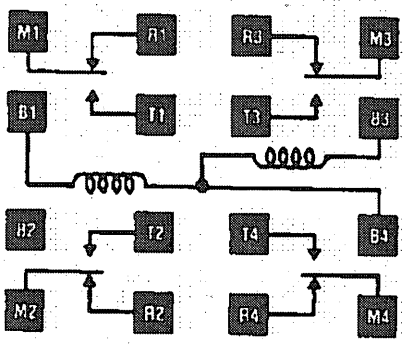


Wiring Diagram (Wiring and Connections)

The ML relay has three terminals for the windings: latching winding between terminals B1 and B4, un-latching winding between terminals B3 and B4.

The ML Relay is not symmetrical due to its three coil connections.

The relays are normally delivered polarized so that terminal B4 carries the negative voltage. To reverse the polarity, a deenenergize/energize cycle should be carried out using a voltage 50% greater than the normal rating.



Continuous Duty Wiring

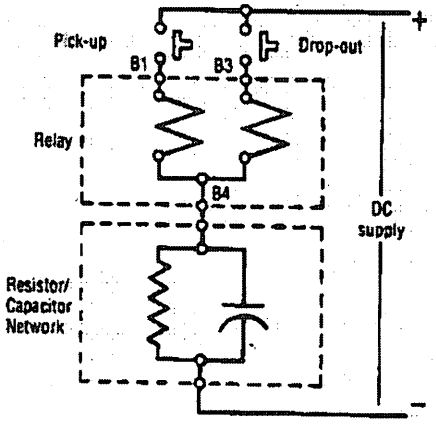
Since the double wound coil does not have a continuous duty rating, voltage pulses to the coils should not exceed a ratio of 40% on, to 60% off, with maximum power-on periods not to exceed 10 minutes.

If continuous energizing only is available, a resistor/capacitor network should be connected as shown below. In this case the shortest time between two operations must not be less than 5 seconds.

The relay will always assume the energized position in the event of both windings being energized simultaneously.

It is advisable not to put another load in parallel with the windings of the ML relay.

ML Series Relay for DC operation with a resistor/capacitor network

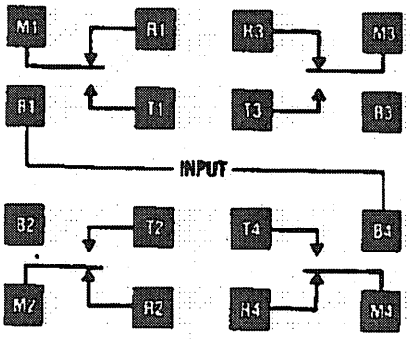


R-C Values

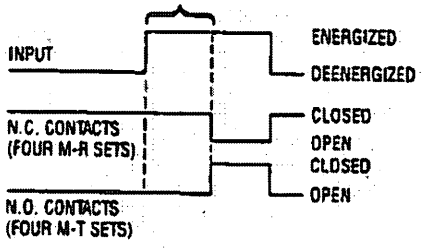
NOMINAL VOLTAGE VDC	R OHMS ±5%	R WATTS	C UF	C VDC
12	62	2	5000	15
24	240	2	2000	50
48	1000	2	500	100
125	6200	2	150	150

SERIES ETR
Time Delay Relay
(Delay on Energization)

Applying a continuous voltage to the input terminals (B1-B4) starts a time delay lasting for the preset time period. During this period the normally closed contacts (Four M-R sets) remain closed. At the end of the delay period, the normally closed contacts break and the normally open contacts (Four M-T sets) make. The contacts remain in this position until the relay is deenergized, at which time the contacts instantaneously return to their normal position. Deenergizing the relay, either during or after the delay period will recycle the unit within .075 second. It will then provide a full delay period upon reenergization, regardless of how often the voltage is interrupted before the unit has been permitted to "time-out" to its full delay setting.



PRESET TIME DELAY



operation

OPERATING CHARACTERISTICS

Environmental Conditions (Qualified Life) — Series EGP/EML/ETR

PARAMETER	MIN.	NORMAL	MAX.
Temperature (°F)	40	70-104	156
Humidity (R.H. %)	10	40-60	95
Pressure	—	Atmospheric	—
Radiation (rads)	—	—	2.0×10^4 (Gamma)

Operating Conditions, Normal Environment — Series EGP/EML/ETR

NORMAL OPERATING SPECIFICATIONS	WITH DC COILS			WITH AC COILS	
	EGP	EML	ETR	EGP	ETR
Coil Operating Voltage, Nominal (rated)*	As Spec.	As Spec.	As Spec.	As Spec.	As Spec.
Pull-in (% of rated value)	80% Min.	85% Min.	80% Min.	85% Min.	85% Min.
Drop-out (% of rated value)	5-45%	85% Min.	5-45%	5-45%	5-50%
Continuous (% of rated value)	110% Max.	NA	110% Max.	110% Max.	110% Max.
Power (Watts at rated value)					
Pull-in	6 Apprx.	15 Apprx.	6 Apprx.	6 Apprx.	6 Apprx.
Drop-out	NA	13 Apprx.	NA	NA	NA
Relay Operate Time	30 ms Max.	25 ms Max. With min. latch pulse of 35 ms.	NA	35 ms Max.	NA
Relay Release (Recycle) Time	25 ms Max.	20 ms Max. With min. latch pulse of 30 ms.	75 ms Max.	85 ms Max.	75 ms Max.
Contact Ratings, Continuous					
Resistive at 125 vdc	1.0 amp.	1.0 amp.	1.0 amp.	1.0 amp.	1.0 amp.
Resistive at 120 vac, 60 Hz	10.0 amp.	10.0 amp.	10.0 amp.	10.0 amp.	10.0 amp.
Insulation Resistance (in megohms at 500 vdc)	500 Min.	500 Min.	500 Min.	500 Min.	500 Min.
Dielectric (vrms, 60 Hz)					
Between Terminals and Ground	1,500	1,500	1,500	1,500	1,500
Between Non-connected Terminals	1,500	1,500	1,500	1,500	1,500
Repeat Accuracy	NA	NA	±5%	NA	±5%

Operating Conditions, Abnormal Environment — Series EGP/EML

ADVERSE OPERATING SPECIFICATIONS	NORMAL	DB "A"	DB "B"	DB "C"	DB "D"
Temperature (°F)	70-104	40	120	145	156
Humidity (R.H. %)	40-60	10-95	10-95	10-95	10-95
Coil Operating Voltage (% of rated)*					
AC (Series EGP only)	85-110	85-110	85-110	85-110	85-110
DC (Series EGP only)	80-110	80-110	80-110	80-110	80-110
DC (Series EML only)	85-110	85-110	85-110	85-110	85-110
Relay Operate Time (ms)					
AC (Series EGP only)	35 Max.	35 Max.	35 Max.	35 Max.	35 Max.
DC (Series EGP, Series EML)	30 Max.	25 Max.	37 Max.	40 Max.	40 Max.

Operating Conditions, Abnormal Environment — Series ETR

ADVERSE OPERATING SPECIFICATIONS	WITH DC COILS	WITH AC COILS
Coil Operating Voltage (rated)*	As Spec.	As Spec.
Pull-in (% of rated value)	80% Min.	85% Min.
Continuous (% of rated value)	110% Max.	110% Max.
Drop-out (% of rated value)	5-45%	5-50%
Power (Watts at rated value)	6 Apprx.	6 Apprx.
Relay Release (Recycle) Time	75 ms Max.	75 ms Max.
Contact Ratings, Continuous		
Resistive at 125 vdc	1.0 amp.	1.0 amp.
Resistive at 120 vac, 60 Hz	10.0 amp.	10.0 amp.
Repeat Accuracy	±10%	±10%

*All coils may be operated on intermittent duty cycles at voltages 10% above listed maximums (Intermittent Duty = Maximum 50% duty cycle and 30 minutes "ON" time.)

specifications

CONTACT RATINGS — Series EGP/EML/ETR

Contact Capacity in Amperes (Resistive)

Contact Voltage	Min. 1,000,000 Operations
24 vdc	10.0 amps
125 vdc	1.0 amp
120 vac, 60 Hz	10.0 amps
240 vac, 60 Hz	7.5 amps

CONTACT RATINGS, UL — Series EGP/EML Only

Contact ratings as listed under the Underwriters Laboratory Component Recognition Program. (Two poles per load):
- 1/3 Horsepower, 120 vac
- 10 amps, General Purpose, 240 vac
- 120 vdc, 1.0 amp

MECHANICAL LIFE — Series EGP/EML/ETR

1,000,000 mechanical operations

APPROXIMATE WEIGHT — Series EGP/EML/ETR

1 lb.

TRANSIENT PROTECTION — Series ETR Only

A 1500 volt transient of less than 100 microseconds, or 1000 volts of less than 1 millisecond will not affect timing accuracy.

TIMING ADJUSTMENT — Series ETR Only

Internal Fixed
Internal Potentiometer

TIME RANGES — Series ETR Only

.15 to 3 Sec.	4 to 120 Sec.
.55 to 15 Sec.	10 to 300 Sec.
1 to 30 Sec.	2 to 60 Min.
2 to 60 Sec.	1 to 30 Min.

REPEAT ACCURACY — Series ETR Only

The repeat accuracy deviation (A_R) of a time-delay relay is a measure of the maximum deviation in the time-delay that will be experienced in five successive operations at any particular time setting of the relay and over the operating voltage and temperature range specified. Repeat accuracy is obtained from the following formula:

$$A_R = \pm 100 \frac{(T_1 - T_2)}{(T_1 + T_2)}$$

Where —
T_1 = Maximum Time Delay
T_2 = Minimum Time Delay

REPLACEMENT SCHEDULE — Series EGP/EML/ETR

The qualified life of these relays is 25,000 electrical operations or 10 years from the date of manufacture, whichever occurs first.

The date of manufacture can be found in the first four (4) digits of the serial number on the nameplate:

XX XX

First two digits indicate the year.

Second two digits indicate the week.

EXAMPLE
In the date code "7814" below:
"78" indicates the year 1978;
"14" indicates the 14th week (or April 3 through April 7).

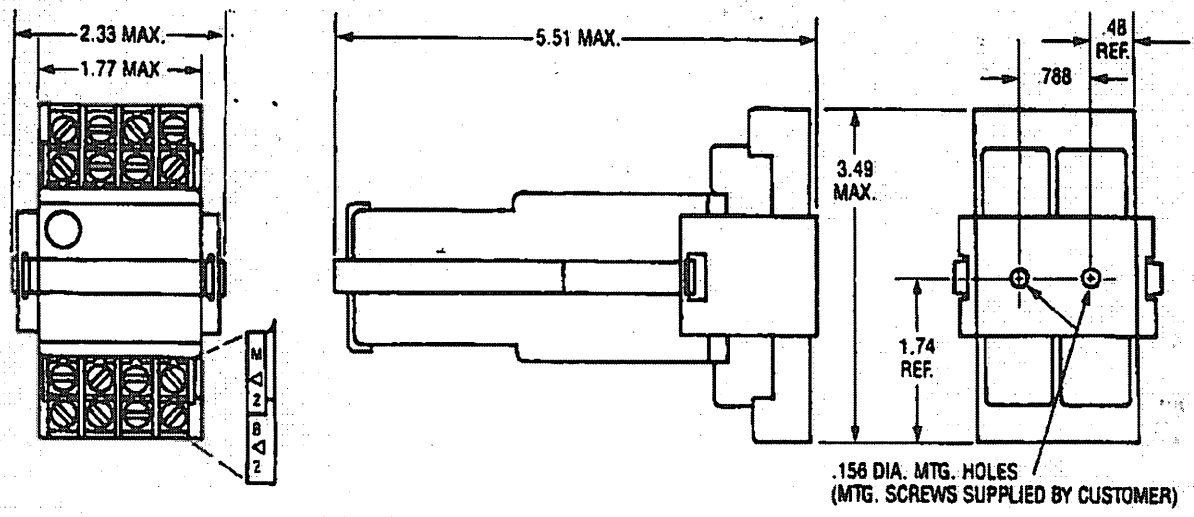
MODEL	
COIL	125 VDC
SERIAL	78140028
Thomas & Betts Corporation Memphis, TN 38119	

NOTE
Amerace Corporation does not recommend the use of its products in the containment areas of Nuclear Power Generating Stations.

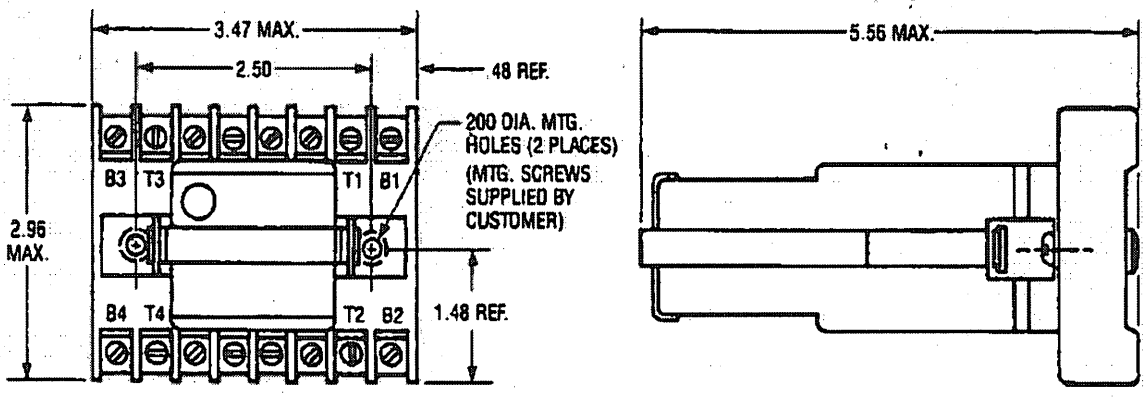
dimensions & mounting

SERIES EGP, EML and ETR

All dimensions in inches



Qualification tested in the horizontal position, mounted in socket ECR0001-001 (captive clamp terminals) or in socket ECR0002-001 (screw terminals) with locking straps ECR0133.



Qualification tested in the horizontal position, mounted in socket ECR0095-001 (screw terminals) with locking strap ECR0155.

Series EGP, EML and ETR AGASTAT® control *relays must be mounted in the horizontal position;* performance specifications of these units are valid only when they are mounted as indicated in either of the above drawings.

ordering information

CATALOG NUMBER CODE — Series EGP and EML

E	GP	A	004
NUCLEAR SAFETY RELATED	AGASTAT® CONTROL RELAY MODEL	COIL VOLTAGE	CONFIGURATION CODE*

CODE
E

CODE
GP — Power Relay
ML — Magnetic Latch

CODE
DC: A — 12 VDC; B — 24 VDC; C — 48 VDC; D — 125 VDC; E — 110 VDC; F — 250 VDC (Series EGP Only)
AC: G — 24 VAC 60Hz (Series EGP Only); H — 48 VAC 60 Hz (Series EGP Only); I — 120 VAC 60 Hz (Series EGP Only); J — 220 VAC 60 Hz (Series EGP Only)

CODE
003

*CONFIGURATION CODE
The Configuration Code is a suffix to the Catalog Number Code which provides a means of identification. When a significant product change is introduced, the Configuration Code and specification sheets will be revised from 003 to 004, etc.

CATALOG NUMBER CODE — Series ETR

E	TR14	B	1	A	004
NUCLEAR SAFETY RELATED	AGASTAT® CONTROL RELAY MODEL	OPERATING VOLTAGE	TIMING ADJUSTMENT	TIME RANGE	CONFIGURATION CODE*

CODE
E

CODE
TR14 — Time Delay Relay (Delay on Pull-in)

CODE
DC: B — 24 VDC; D — 125 VDC
AC: I — 120 VAC 60Hz

CODE
1 — Internal Fixed
3 — Internal Potentiometer

CODE
A — .15 to 3 sec.
B — .55 to 15 sec.
C — 1 to 30 sec.
D — 2 to 60 sec.
E — 4 to 120 sec.
G — 10 to 300 sec.
I — 2 to 60 min.
N — 1 to 30 min.

CODE
003

*CONFIGURATION CODE
The Configuration Code is a suffix to the Catalog Number Code which provides a means of identification. When a significant product change is introduced, the Configuration Code and specification sheets will be revised from 003 to 004, etc.

Relay Classifications
Control Code Summary

Product	Configuration Control			
	Code - 001	Code - 002	Code-- 003	Code - 004
E7000	Contains all materials present in original qualification testing.	Sept. 1981 - Elastomer gasket material change to improve thermal aging properties. Material changed for Buna N or Neoprene to Neoprene only.	March 1989 - Paint change to timing head portion of relay. New paint: Sherwin Williams E61YC37 primer and PPG W48392 silver polyester top coat.	Dec. 1991 - Paint change to timing head portion of relay. New paint: Prime coatings No. 28032 Enamel. No primer is used with this finish.
EGP	Contains all materials present in original qualification testing.	Nov. 1981 - Material change to coil wrapping tape and lead wire insulation to improve thermal life.	Dec. 1987 - Material change on leaf spring from nickel copper to beryllium copper.	Dec. 1995 - Material change on bobbin from Nylon Zytel 101 to Rynite FR530. Material change on base from Melamine Phenolic to Grilon PMV-5HV0.
EML	Contains all materials present in original qualification testing.	Nov. 1981 - Material change to coil wrapping tape and lead wire insulation to improve thermal life.	Dec. 1987 - Material change on leaf spring from nickel copper to beryllium copper.	Dec. 1995 - Material change on bobbin from Nylon Zytel 101 to Rynite FR530. Material change on base from Melamine Phenolic to Grilon PMV-5HV0.
ETR	Contains all materials present in original qualification testing.	Nov. 1981 - Material change to coil wrapping tape and lead wire insulation to improve thermal life.	Dec. 1987 - Material change on leaf spring from nickel copper to beryllium copper.	Dec. 1995 - Material change on bobbin from Nylon Zytel 101 to Rynite FR530. Material change on base from Melamine Phenolic to Grilon PMV-5HV0.
ECR0001	Contains all materials present in original qualification testing.	June 1989 - material change from Noryl N-225 std. black to Noryl SE-I-701AA black.		
ECR0002	Contains all materials present in original qualification testing.	June 1989 - material change from Noryl N-225 std. black to Noryl SE-I-701AA black.		
ECR0095	Contains all materials present in original qualification testing.			
ECR0133	Contains all materials present in original qualification testing.			
ECR0155	Contains all materials present in original qualification testing.			

Attachment 4
to GNRO-2015/00012

LSS Vendor Manual

SHEET 1 OF 1
MNCR 733-83

REVISION STATUS		
LTR	DATE	APPROVED
A	2/82	[illegible]
B	8/83	[illegible]

MANUAL REVIEWED BY [signature] 3-7-84
SIGNATURE DATE

TITLE: MAINT. ENGINEER

INSTRUCTION MANUAL
FOR
LOAD SHEDDING AND SEQUENCING PANEL

Grand Gulf Nuclear Station
Units 1 and 2

SEP 20 1983

Prepared for.

Mississippi Power and Light Company

MPL No. 9645-E-092.0-Q1H22-P331-4.0-1-I

Under

Purchase Order No. 9645-E-092.0

Prepared by:

AUTOMATION INDUSTRIES, INC.
VITRO LABORATORIES DIVISION
4700 GEORGIA AVE
SILVER SPRING MARYLAND 20910

March 1978

Approved by:

J. C. Schuessler
Project Leader

RECORD OF REVISION

REV	DATE	DESCRIPTION	RESPONSIBLE ENGINEER INITIALS
N/A	*6/15/04*	*VMA 04/0055 (PE EVAL 8572; replace pg 44 – Table 6 Spare Parts List)*	*VSW*
N/A	*1-23-03*	*VMA 03/0016 (ER 2003-0029-000-0; replace pg 44 – Table 6 Spare Parts List, add VMA pg. 3 through 6 behind Table 6*	*DGO*
N/A	*4-23-02*	*VMA 02/0045 (ER-GG-2001-0091-000 Rev. 2; replace pgs. 43 & 44, add VMA pg. 4 through 8 to back of manual, add Technical Data Sheet –VMA pg. 9 through 44 behind installation instructions)*	*GLA*
N/A	*8-6-91*	*VMA 91-0037*	*AM*
N/A	*8-5-83*	*MNCR 83/0733*	*PR*

VENDOR MANUAL NUMBER:***460000245***

DIRECTIVE REFERENCE SHEET

The directives listed below reference this manual for use in accomplishing an operational or maintenance activity. Any revision to this manual requires that each directive be reviewed for conflict.

DIRECTIVE NUMBER	DIRECTIVE NUMBER	DIRECTIVE NUMBER	DIRECTIVE NUMBER
06-EL-1R21-M-0001	**06-OP-1R21-M-0002**	**07-S-13-R21-1**	

VENDOR MANUAL NO. 460000245

APPLICABLE MPL NUMBER SHEET

DOCUMENT LOCATION NUMBER: *460000245*

TITLE **INSTRUCTION MANUAL FOR LOAD SHEDDING & SEQUENCING PANEL**

MPL NUMBERS	MPL NUMBERS	MPL NUMBERS	MPL NUMBERS	MPL NUMBERS
Q1H22P331				
Q1H22P332				

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Section 1
SYSTEM DESCRIPTION

The Load Shedding and Sequencing Panel is a solid-state digital system which monitors bus voltages, offsite power sources and accident conditions, and through appropriate coincident logic, initiates operation of the diesel generators, selects alternate power sources, and provides logic for the sequential loading of the vital buses.

Each LSS Panel contains separate and independent breaker control circuits and safeguard sequencers with both Manual and Automatic Test capability. Solid-state circuits are utilized for all system logic and timing functions while keeping equipment compatible with existing equipment by using input and output buffering relays.

Section 2
THEORY OF OPERATION

Each LSS Panel monitors four potential transformer voltages via bistables and combines them to detect valid bus undervoltage (BUV) conditions, and monitors LOCA inputs to detect an accident condition. Upon either BUV or LOCA condition, loads from the vital plant bus are shed, incoming power source breakers are tripped if a BUV exists, and selection of and connection to a preferred or alternate power source (offsite or diesel generator) is made. Upon restoration of vital bus voltage, one of three independent loading sequences, depending on preceding inputs, is selected to sequentially load the vital ESF bus with appropriate safety equipment. The three sequences are for a BUV condition only, a loss of offsite power (LOP), and a LOCA condition, respectively.

A BUV sequence is initiated after a BUV condition has been detected, loads shed, incoming breakers tripped, and bus voltage restored via connection of the offsite power source to the vital bus.

A LOP sequence is initiated after a BUV condition has been detected, loads shed, incoming breakers tripped, and bus voltage restored via connection of the ESF diesel generator to the vital bus after determination that no preferred offsite power source is available.

A LOCA sequence is initiated after a LOCA condition has been detected, loads shed, and vital bus voltage made available via connection to the preferred offsite power source or diesel generator if a BUV condition simultaneously existed.

LSS Panel operation is functionally depicted on Vitro drawing 2699-1001, Function Logic Diagram, LSS Panel.

Section 3
SERVICE CONDITIONS

Each LSS Panel is designed to operate continuously at an ambient temperature of 80 ±40°F without forced ventilation and a relative humidity not to exceed 90 percent. The equipment is designed to operate from two Power Station sources, 125 V dc ESF (IE) and 125 V dc BOP (non-IE). The panel requirements on these sources are as follows:

REQUIREMENTS	ESF	BOP
Voltage:	105-140 V dc	105-140 V dc
Grounding:	Ungrounded	Ungrounded
Current drain @ 125 V dc,		
Typical (standby condition)	1A	100 MA
Maximum (activated condition)	3A	500 MA
LSS Panel Fusing:	7A (slow blow)	none provided

Section 4
CIRCUIT DESCRIPTION

As shown in figure 1, LSS Panel - Block diagram, each LSS Panel includes input and output relays and digital isolators, system logic, and control, bistable, and power supply panels.

4.1 INPUT RELAYS

External equipment supplies inputs to the LSS panel and form A contact closures to complete a 125 V dc circuit that actuates an input interface relay. Input relay contracts, in turn, are connected directly into logic circuits, thus providing a protective interface between external equipment and LSS panel system logic. Selected input relay contacts are wired to provide simple logical OR-ing or AND-ing of inputs, such as the LOCA inputs, and the OFFSITE POWER AVAILABLE inputs. Input relays are General Electric Type 35AA relays rated at a coil resistance of 10,000 ohms ±15 percent at 77°F, which will result in a maximum coil current of 17 MA at 140 V dc.

4.2 BISTABLE PANEL

The Bistable Panel provides the interface required for monitoring the four potential transformer inputs. Each potential transformer input is first fused and then applied to the primaries of step-down transformers. The secondaries are in turn connected directly into the bistable circuits of the system logic. The loading of the Bistable Panel on the potential transformer input is monitored by a panel meter on the front of the Bistable Panel, each with a scale reading of 0-150 V ac, ±3%. In addition, a test jack, calibration switch, and potentiometer is provided for each input to be utilized for bistable trip point adjustment and Manual Test operation to simulate input bus undervoltage conditions.

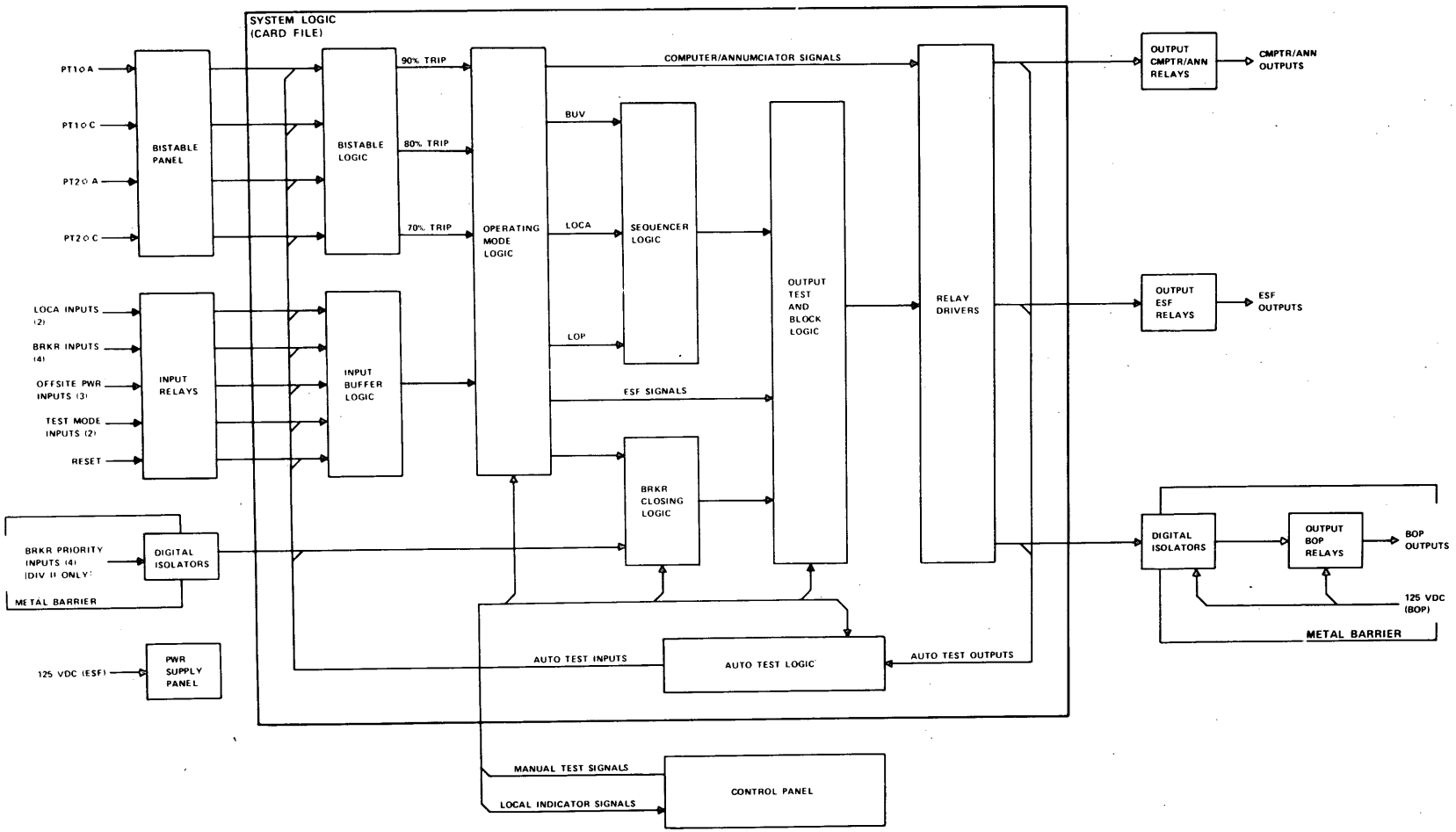

Figure 1. LSS Panel - Block Diagram

4.3 SYSTEM LOGIC

The LSS Panel system logic is realized utilizing solid state high threshold type logic, (HTL and CMOS), which provides superior noise immunity.

4.3.1 INPUT BUFFER LOGIC. The input buffer logic accepts contact inputs from the input relays, provides contact debouncing, distinguishes between real inputs and Auto Test inputs, and provides conditioned logic level signals to the balance of the system logic.

4.3.2 BISTABLE LOGIC. The bistable logic accepts three AC signals from each potential transformer via the Bistable Panel, for a total of twelve signals. These signals are applied to twelve Bistable Cards with trip point settings of nominally 70%, 80%, and 90% of 120 V ac for each of the four potential transformer groups. Each of the bistable card trip outputs are logically combined with the other like trip outputs in a two-out-of-four taken twice fashion and then applied to field programmable time delays before being applied to the balance of the system logic. Any one of twelve bistable trips results in a control signal which inhibits the Auto Test function.

The trip point of any bistable card may be adjusted from 65% to 95% of 120 V ac by means of a multi-turn potentiometer on each card and will maintain a long term accuracy of ±1% of initial setting. Each bistable card has a nominal time response of 20 milliseconds and a hysteresis band not to exceed 1% of 120 V ac to minimize false trips and/or resets. To facilitate trip point adjustments, an LED is located on each bistable card and indicates a trip of that signal channel.

4.3.3 OPERATING MODE LOGIC. The operating mode logic provides the system mode decision logic. It accepts buffered system inputs, bistable trip signals, and Manual Test inputs, and provides appropriate computer or annunciator logic signals, ESF logic signals, and control signals for the balance of the system logic. Among the decisions made by this logic are the proper sequencer mode, initiation and termination of selection of an alternate ESF bus power source, determination of a permissive for Manual and/or Automatic testing modes and appropriate system resets upon any system mode change. The operating mode

logic locks out Manual and Automatic test functions upon the recognition of selected system inputs which constitute an emergency condition and resets the system from any test state so that the system may respond properly to the real input.

4.3.4 SEQUENCER LOGIC. The sequencer logic provides three independent loading sequences depending on the operating mode command. The BUV and LOP loading sequencers provide for six output loading steps while the LOCA loading sequencer provides for five output loading steps. The step time for each sequencer step is field programmable and may be adjusted from 0 to 99 seconds in one second increments. Each step output provides for two types of output loading signals, a maintained and a momentary. Maintained loading signals are all initially operated upon the occurrence of a BUV or LOCA condition. Upon the initiation of a loading sequence the signals are then reset at their appropriate step time. Momentary loading signals are initially operated at their respective step time and remain operated for a field programmable time duration. This momentary time may be adjusted from 0 to 0.9 seconds in 0.1 second increments. Thus, at the conclusion of a loading sequence, all output steps shall be released (except step number 6, maintained outputs upon a LOCA sequence).

4.3.5 BREAKER CLOSING LOGIC. The breaker closing logic functions to select an alternate power source for the vital bus in the event of a bus-undervoltage condition. Four alternate sources are polled sequentially on a priority basis. They are, in order, three offsite power sources and the diesel generator. If an offsite power source is available, a 0.5 second momentary output signal is generated to operate the respective breaker. If bus voltage is not re-established within one second, the next in priority power source is selected and a similar momentary signal generated to operate its respective breaker. This search technique continues until all three offsite sources have been polled without success, at which time a signal is generated to close the diesel generator breaker. If any offsite power source is not available, it will be skipped over during the search.

Division II panels only provide for the interchanging of priority between the first and second offsite power sources. Four system inputs to Division II

panels determine the proper priority. The presence of a Normal Priority input or the presence of an Auto Priority input coincident with both Service and ESF Transformer Breakers Closed inputs will result in a normal priority of power source search. Otherwise, priority will be interchanged between the first and second offsite power sources.

4.3.6 OUTPUT TEST AND BLOCK LOGIC. The output test and block logic electronically blocks output ESF signals when in a Manual Test mode. In addition, outputs may be selectively operated in a Manual Test mode to verify relay operation and wiring continuity. Upon any emergency condition, the output test and block logic is disabled.

4.3.7 RELAY DRIVERS. Solid state relay drivers are utilized to provide the increased drive required by output relays. The relay drivers provide open collector outputs with voltage suppression diodes to reliably drive the inductive load presented by a relay coil.

4.3.8 AUTO TEST LOGIC. The Auto Test logic provides the capability to test the LSS panel continuously while in a standby condition, thereby maintaining a high degree of reliability. For a detailed description of this function, refer to paragraph 8.2.

4.4 OUTPUT RELAYS

Each LSS panel provides output relays to interface with safety equipment. Relay contacts provide isolated electrical outputs used for starting, tripping, and blocking ESF and BOP safety equipment as well as for remote computer and annunciator signals. All output relay contacts are form C, and wired to the output terminal blocks. Three types of output relays are utilized. They are for computer/annunciator outputs, ESF outputs, and BOP outputs.

The computer/annunciator outputs utilize GE type 3SAA relays operated off the 24 V dc internally produced supply voltage. The output contacts are capable of making and carrying 10A at 125 V dc and will break 0.5 A resistive at 125 V dc.

The ESF output relays are Agastat type GPB operated off the panel 24 V dc supply with nominal contact rating of 10A at 120 V ac.

The BOP output relays are Agastat type GPD operated off the external 125 V dc BOP power source and with similar contact rating as the GPB relay above.

4.5 DIGITAL ISOLATORS

Inputs and outputs requiring BOP to ESF isolation utilize digital isolators. A digital isolator consists of a light source and light dependent resistor enclosed in a metal case and mounted in a metal barrier within the panel, which also encloses the BOP relays and terminal blocks for connection to external BOP devices.

For BOP inputs (Division II only) an input contact closure completes a circuit containing the digital isolator light source and a dropping resistor across the 125 V dc BOP power source. The light dependent resistor supplies an isolated signal directly to the system logic.

For BOP outputs, system logic signals control the digital isolator light source. The associated light dependent resistors are wired in series with BOP output relays across the 125 V dc BOP power source, causing relay operation when in a low resistance state.

In addition to BOP inputs and outputs, one digital isolator circuit is utilized in a configuration similar to the BOP inputs less the input contact, and supplies a signal to the power supply panel to indicate presence of the 125 V dc BOP power source.

4.6 CONTROL PANEL

The control panel contains local indicators for observing panel status and test switches for manual and automatic test functions. A description of the control panel functions may be found in paragraph 7.1.

4.7 POWER SUPPLY PANEL

A description of the power supply panel may be found in paragraph 5.2.

Section 5
CABINET DESCRIPTION

Each LSS panel is housed in a separate independent, free-standing, two-bay cabinet (see figures 2 and 3), weighing approximately 1800 pounds. The cabinets are 90 inches high, 58 inches wide, and 36 inches deep.

Each cabinet has two hinged front doors with keylocks. The doors are louvered to provide natural ventilation. The left door is constructed with a safety glass insert permitting continuous status observation of the control panel and bistable panel. An engraved lamicoid nameplate is located on the front of the cabinet.

All ESF electronic portions of the LSS panel are located in the cabinet electronics bay. Relays are mounted within this bay and panel assemblies are mounted in a swing-out panel in the bay. All terminal blocks for Power Station interconnection are located in the cabinet terminal bay. In addition, the metal barrier enclosing all BOP devices is mounted toward the rear of the terminal bay. Each LSS panel is provided with two removable plates at the top of the terminal bay for top entry of Power Station ESF and BOP cables.

5.1 CABINET ASSEMBLY

An LSS panel assembly (see figures 2 and 3) contains the following:

a. Control Panel Assembly
b. Bistable Panel Assembly
c. Card File Assembly
d. Power Supply Assembly
e. Relays
f. Digital Isolator Assembly
g. Isolation Barrier
h. Terminal Blocks.

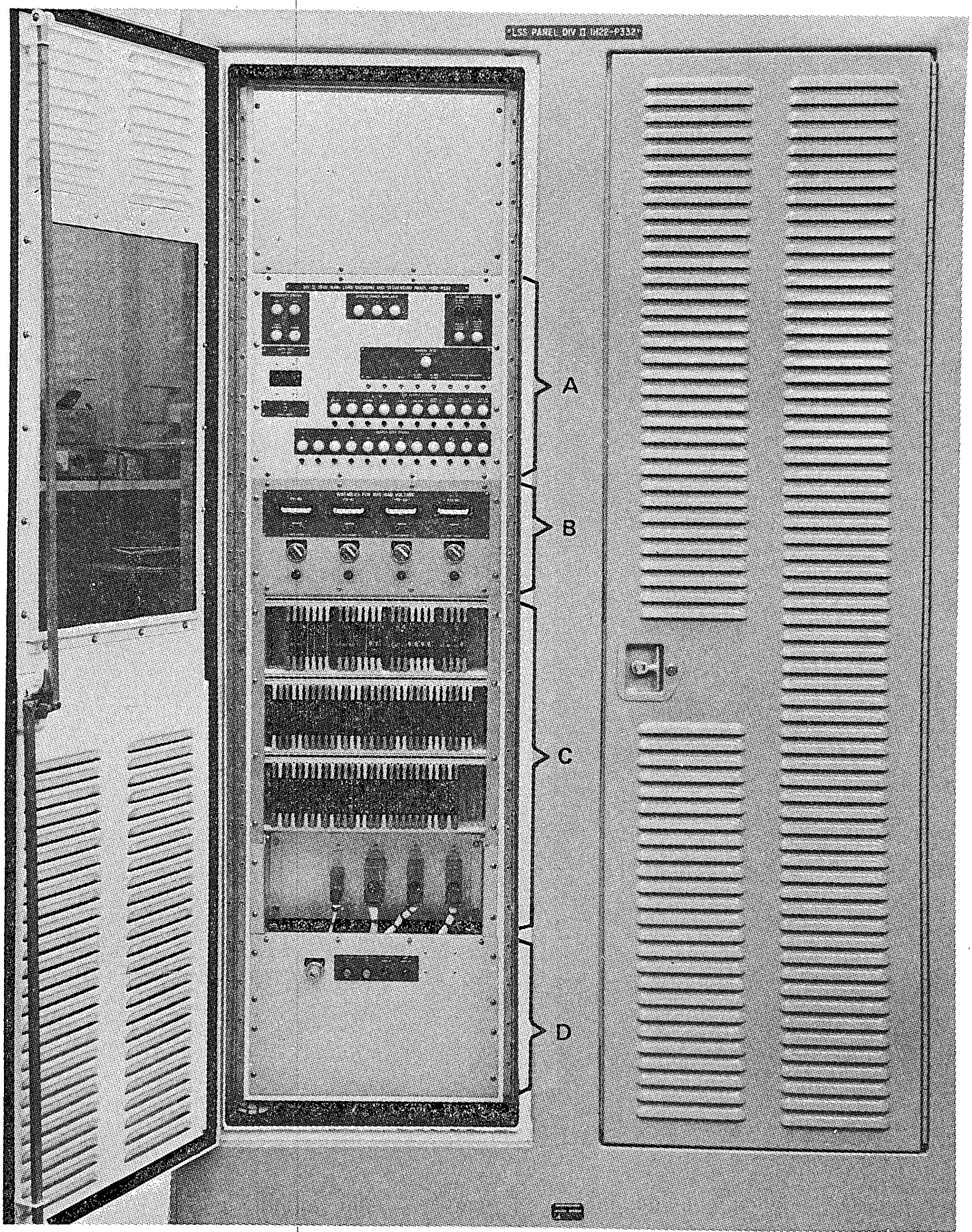

Figure 2. LSS Panel - External View

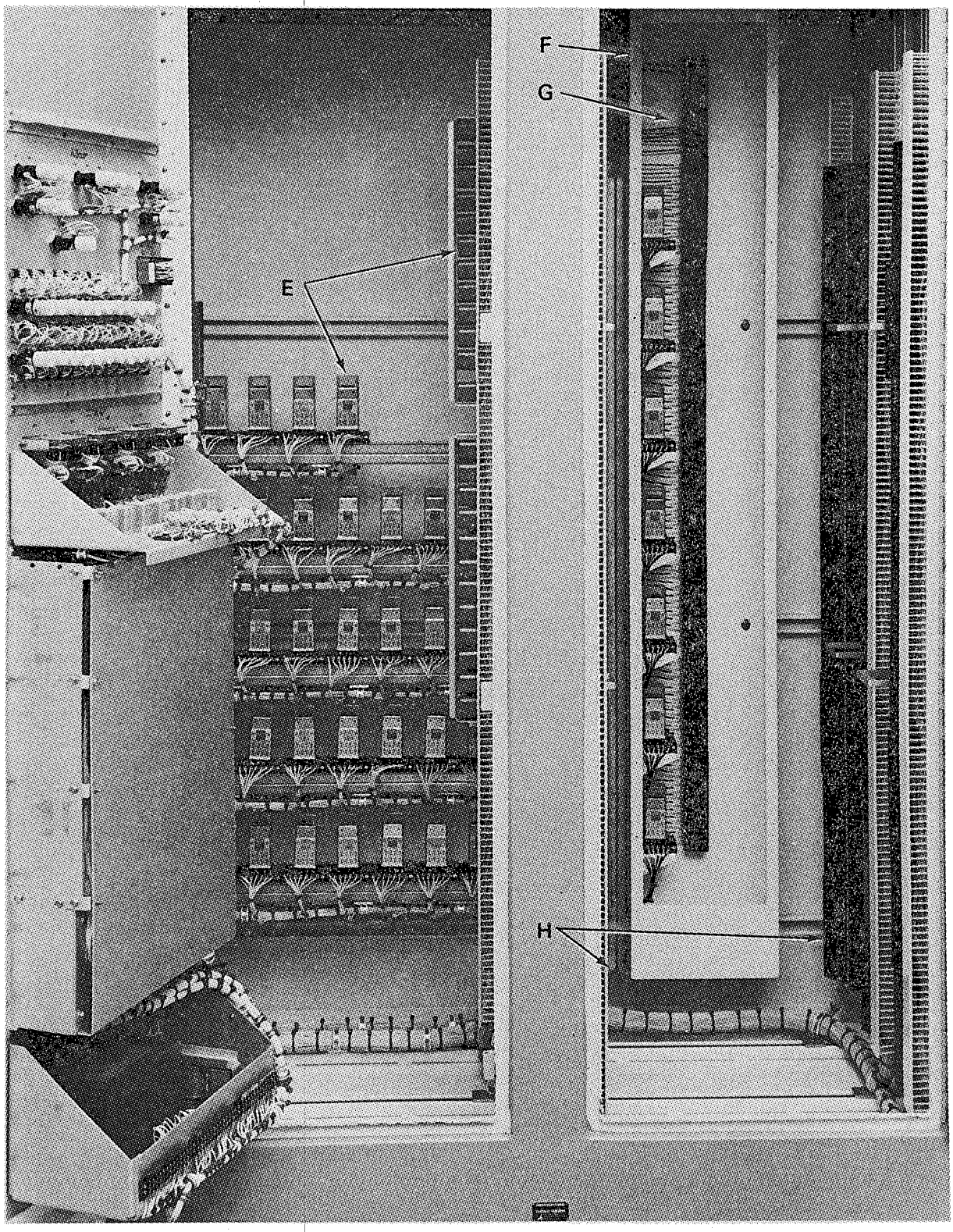

Figure 3. LSS Panel - Internal View

5.2 CABINET ASSEMBLY DETAILS

For cabinet assembly details, see callouts in figures 2 and 3. The control panel (A), as shown in more detail in figure 4, contains switches which provide control and test capability and indicators which display system status.

The bistable panel (B), as shown in more detail in figure 5, contains panel meters for monitoring potential transformer input voltages, and test jacks, calibration switches, and potentiometers which provide the capability for calibrating each bistable channel and manually testing the bistable circuits. In addition, step down transformers are provided and utilized to isolate the input potential transformer voltages from the balance of the system. The potential transformer inputs are fused for protection.

The card file assembly (C), as shown in more detail in figure 6, contains a three-tiered printed circuit card file which houses all PC cards and a lower connector panel containing jacks which mate with connectorized cables from the balance of the cabinet. Each jack and plug is uniquely keyed to ensure correct mating. The card file has card guides and positive locking ejectors for installing and securing PC cards into the card file slots, and PC card edge connectors. All card file wiring is by wire wrapping of PC card edge connector pins and connector jack pins. The PC cards contain the solid-state electronic components for the LSS panel system. The card file assembly contains 85 PC cards representing 18 different PC card types. Each PC card type is uniquely keyed with the card edge connectors for that type, thus preventing incorrect placement of PC cards. For part numbers, quantities, and locations of all printed circuit cards refer to Vitro drawing 2699-1015, Card File Assembly.

The power supply assembly (D), contains a 24 V dc power supply and a 15 V dc power supply. An ON/OFF cylinder lock switch is provided to control the panel 125 V dc ESF power source. Two red neon pilot lights are provided to monitor the input 125 V dc ESF and BOP power sources. Due to isolation requirements, the BOP pilot light is powered from the ESF power source, and therefore, will only give indication of BOP power source status when the ESF power source is available. In addition, electrical protection is provided by indicating fuses installed in each leg of the 125 V dc ESF power source and by transient protectors installed across the ESF power source. The 24 V dc power supply is used to power all control panel indicators, ESF output relays, and

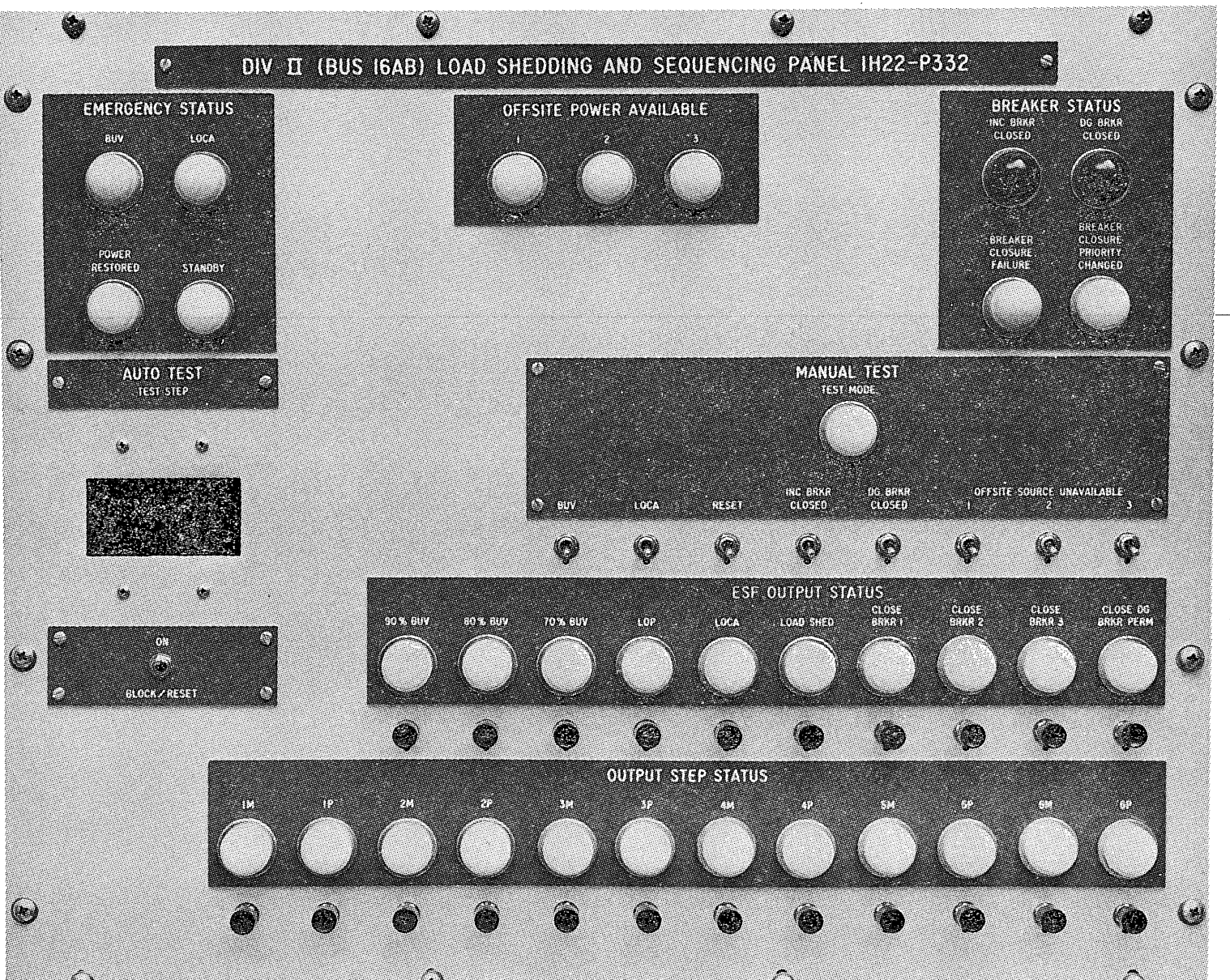

Figure 4. Control Panel

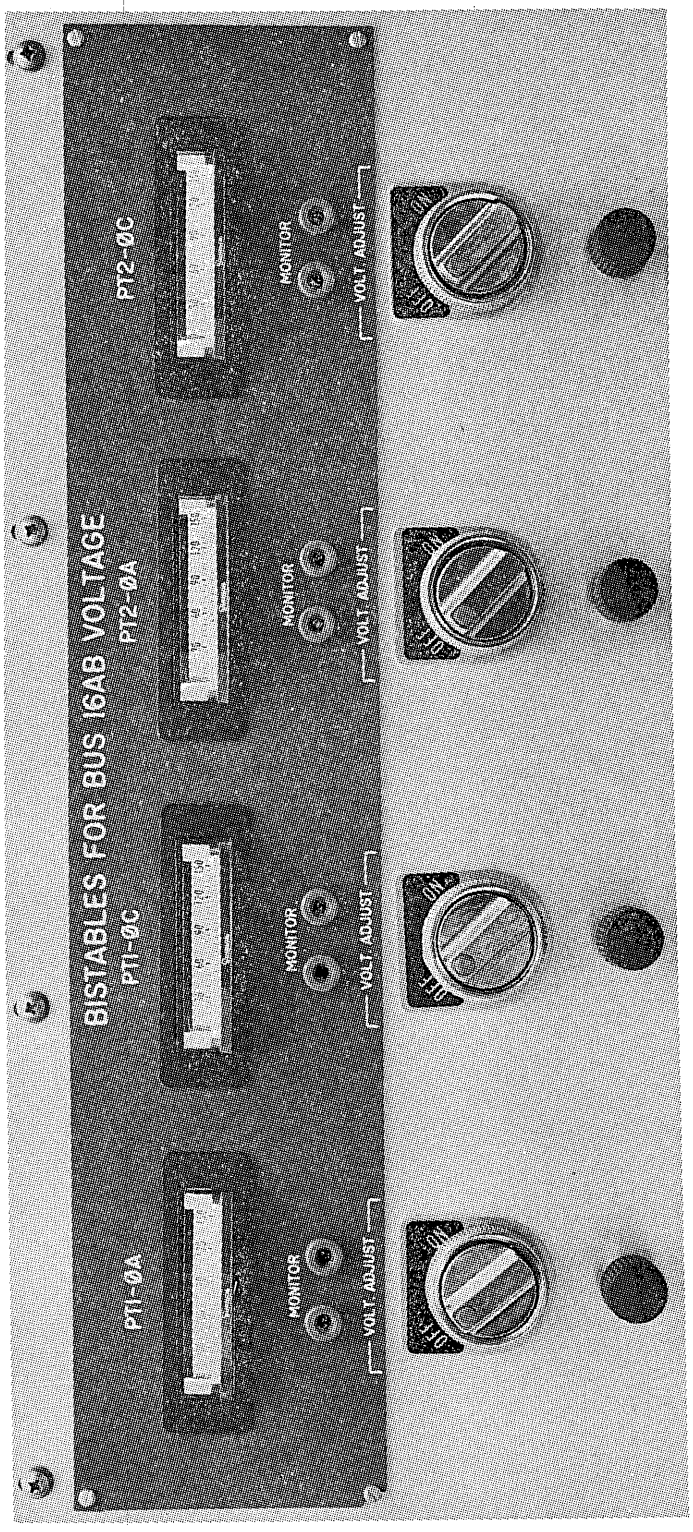

Figure 5. Bistable Panel

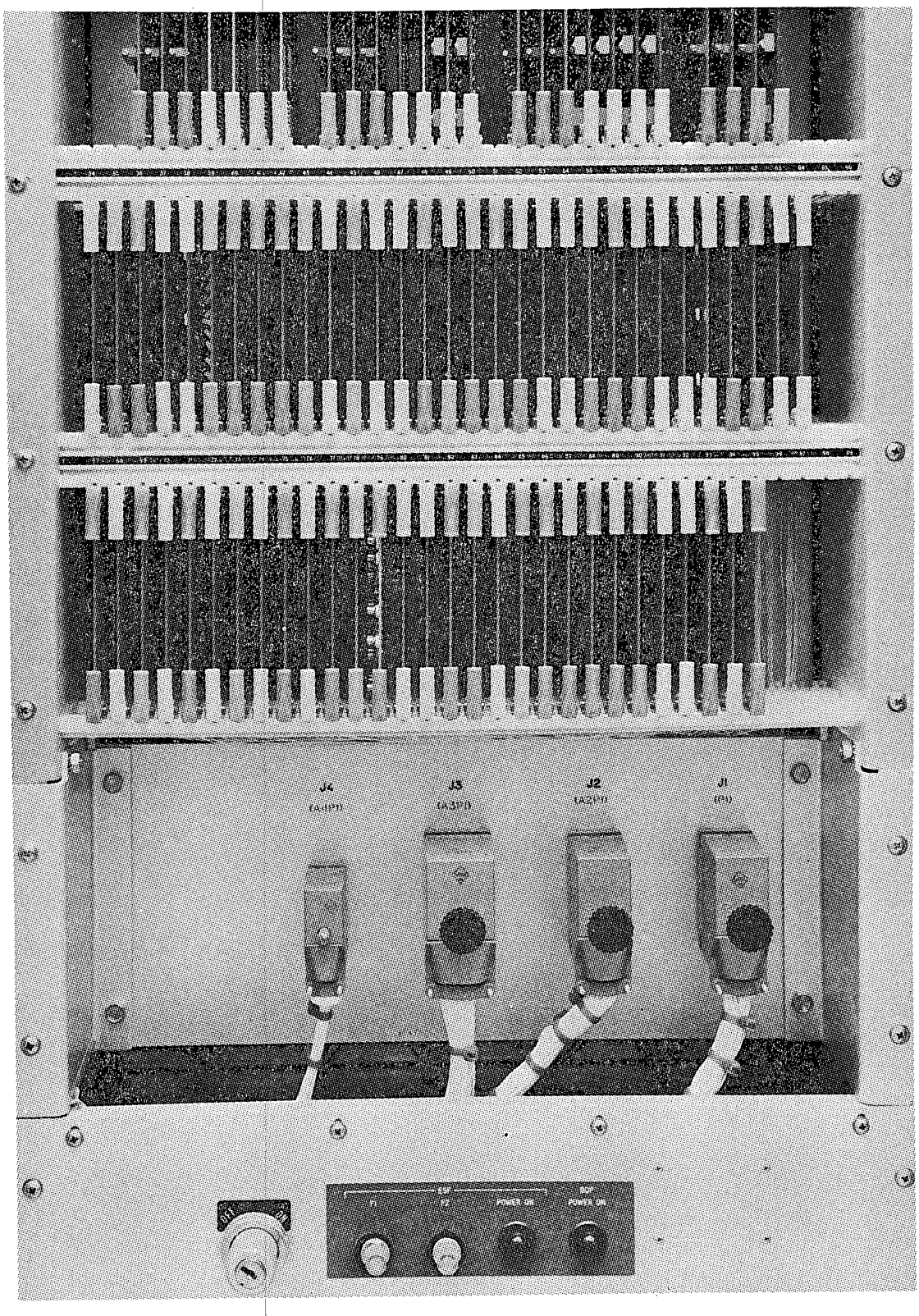

Figure 6. PC Card File

computer/annunicator output relays; the 15 V dc power supply is used to power the solid state electronics. The fused 125 V dc ESF power source is used to power all input ESF relays. The power supply assembly also contains control relays which provide sequential application and removal of all supply voltages during powering up and down of the LSS panel.

Four different varieties of relays (E) are utilized in the LSS panel. ESF input and computer/annunciator relays are located in a single vertical row on the inner side frame of the electronics bay section of the cabinet. ESF output relays are located in five horizontal tiers across the rear of the electronics bay. BOP output relays are located in a tiered vertical row along the left inner side of the isolation barrier in the cabinet terminal bay.

The digital isolator assembly (F), contains all digital isolators, associated dropping resistors, and terminal blocks for wiring connections. It is located in a cutout on the left inner side of the isolation barrier toward the top of the cabinet.

The isolation barrier (G) is located in the rear of the cabinet terminal bay and encloses all BOP relays and terminal blocks.

Terminal blocks (H) facilitate connecting each LSS panel to external equipment. ESF terminal blocks are arranged in six vertical rows. Three rows are located on each side of the cabinet terminal bay section. BOP terminal blocks are arranged in one vertical row within the isolation barrier located in the rear of the terminal bay.

Section 6
INSTALLATION

Each LSS panel shall be installed in accordance with Vitro drawing 2699-1000, Outline Dimensions and Foundation Requirements. All LSS panel input and output signals and primary power wiring connections shall be in accordance with Vitro drawing 2699-1004, External Wiring Connections.

Section 7
LSS PANEL OPERATING INSTRUCTIONS

Once an LSS panel is energized and the Auto Test switch positioned to ON, LSS panel operation is completely automatic and requires no operator intervention. An LSS panel does, however, contain controls, indicators, and adjustments to permit test, maintenance, status monitoring, and trip points and system timing adjustments. The above features are available in the following forms: control panel switches and indicators, bistable adjustments, time adjustment switches, and dc power control.

7.1 CONTROL PANEL SWITCHES AND INDICATORS

The control panel (see figure 4) provides a centralized location for test and monitor functions. Control panel switches and indicators are listed and described in table 1.

Table 1. Control Panel Switches and Indicators

INDICATOR/SWITCH	FUNCTION
EMERGENCY STATUS	
BUV indicator	Lights when a real emergency only 70% bus undervoltage is detected.
LOCA indicator	Lights when a real emergency only LOCA condition is detected.
POWER RESTORED indicator	Lights when bus voltage is re-established after a bus undervoltage condition. This function is indicated under real emergency or manual test conditions.
STANDBY indicator	Lighted continuously under all non-emergency conditions; indicates a permissive for manual or automatic test functions.

Table 1. Control Panel Switches and Indicators (Continued)

INDICATOR/SWITCH	FUNCTION
OFFSITE POWER AVAILABLE	
1, 2, 3 indicators (3)	Lights when associated offsite power source is available for use; indicates a permissive for associated breaker closure signal upon a BUV condition and an alternate power source search function.
BREAKER STATUS	
INC BRKR CLOSED indicators	Lights when one of three incoming breakers is closed connecting an offsite power source to the vital ESF bus.
DG BRKR CLOSED indicator	Lights when the diesel generator is connected to the ESF bus via the closed DG breaker.
BREAKER CLOSURE FAILURE indicator	Lights when a bus undervoltage has existed for a predetermined time between 10 and 19.0 seconds indicating that an alternate power source has not been connected to the ESF bus.
BREAKER CLOSURE PRIORITY CHANGED indicator (DIV II only)	Lights to indicate priority change between first and second offsite power sources for purpose of alternate power source search.
MANUAL TEST	
TEST MODE indicator	Lights to indicate a test mode command input has been detected. This in conjunction with a STANDBY indication constitutes a permissive for manual testing.
BUV, LOCA, RESET, INC BRKR CLOSED, DG BRKR CLOSED, OFFSITE SOURCE UNAVAILABLE 1,2,3 Switches (8)	These eight switches are utilized for manual testing by simulating the indicated input function to the panel.

Table 1. Control Panel Switches and Indicators (Continued)

INDICATOR/SWITCH	FUNCTION
AUTO TEST	
TEST STEP display	Displays the automatic test step in which a malfunction has been detected.
ON, BLOCK/RESET switch	Provides functional control over the automatic test circuits as indicated.
ESF OUTPUT STATUS	
indicator and switch pairs (10 pairs listed below)	Indicators light indicating that the respective output logic signal is detected. Operation of the switches causes the respective output relays to be operated if in an output manual test mode.
90% BUV	A maintained output indicates a 90% bus undervoltage condition has been detected before a 70% bus undervoltage condition may have been detected. A momentary output for less than 1 second indicates a 70% bus undervoltage condition detected first.
80% BUV	Indicates an 80% bus undervoltage condition has been detected under the presence of a LOCA condition without a 90% bus undervoltage condition detected.
70% BUV	Indicates a 70% bus undervoltage condition has been detected.
LOP	Indicates no offsite power sources are available for use.
LOCA	Indicates a LOCA condition detected.
LOAD SHED	Indicates momentary output upon detection of a BUV or LOCA condition.
CLOSE BRKR 1,2,3	Indicates momentary outputs to close respective breakers upon a search function for an alternate power source.

Table 1. Control Panel Switches and Indicators (Continued)

INDICATOR/SWITCH	FUNCTION
CLOSE DG BRKR PERMISSIVE	Indicates that a LOP condition exists, an alternate offsite power source search has failed, or a 90% BUV output exists all under a BUV condition.
OUTPUT STEP STATUS	
indicator and switch pairs (10)	Indicator and switch pairs associated with loading sequencer step outputs functionally equivalent to the ESF OUTPUT STATUS pairs.

7.2 BISTABLE ADJUSTMENTS

The proper operation of the bistable functions in the LSS panel and, therefore, in the Power Station safety system requires accurate settings of all bistable trip points. The input calibration adjustments may be utilized to facilitate making accurate trip point settings.

7.2.1 INPUT CALIBRATION. Input calibration of potential transformer inputs may be accomplished at the bistable panel. Input levels may be monitored locally by the panel meters provided on the front of the panels. However, these meters have an accuracy of only ± 3 percent and, therefore, are not recommended for trip point adjustments. Monitor jacks are provided on the panel for monitoring input levels with a more accurate voltmeter when making trip point settings. A test cable is provided as an accessory for this purpose. To calibrate an input level, the following procedure is recommended:

a. Connect a voltmeter to the desired potential transformer monitor jack with the test cable provided. If a vacuum tube voltmeter (VTVM) is used, which is recommended, allow at least 15 minutes for voltmeter to warm up and stabilize.

b. Place proper calibration switch to ON. This will insert the potentiometer located below the calibration switch in series with the associated potential transformer voltage signal.

c. With the calibration potentiometer fully clockwise, approximately 100% of the input signal is passed through. With potentiometer fully counter-clockwise, approximately 55% of the input signal is passed through. Adjust potentiometer to the desired trip voltage for the bistable to be adjusted.

d. Set trip point on desired bistable as described in paragraph 7.2.2.

e. Readjust calibration voltage for next bistable and continue in this way to set all three bistable trip points off that respective potential transformer signal.

f. Place calibration switch OFF and repeat procedure on next potential transformer signal. Continue until all bistable trip points are set insuring that no two calibration switches are in the ON position at the same time.

7.2.2 BISTABLE TRIP POINTS. Bistable Trip Points may be adjusted utilizing the following procedure.

a. Locate proper bistable PC card in the first tier of the card file. Each bistable card is listed by function in table 2, Bistable Card Trip Point Adjustments.

b. Set up desired trip point level using the calibration procedure of paragraph 7.2.1.

c. Observe LED on bistable card. If it is lighted turn screw adjustment on potentiometer located directly below LED counter-clockwise until LED turns off. A screwdriver tool is provided for this purpose. If LED is blinking, ensure Auto Test switch is placed to BLOCK/RESET.

d. Slowly turn screw adjustment clockwise to precisely the point that the LED turns on. The trip point for that bistable card is now set for the calibration voltage level set up.

NOTE

Due to short term changes in the potential transformer voltages, care should be taken to ensure that the correct calibration voltage is set up at the time of making the trip point setting.

Once a trip point has been set, it is valid only for the slot the bistable card is in. If bistable cards are interchanged, trip points should be reset. All bistable cards must be inserted in card file before trip points are set.

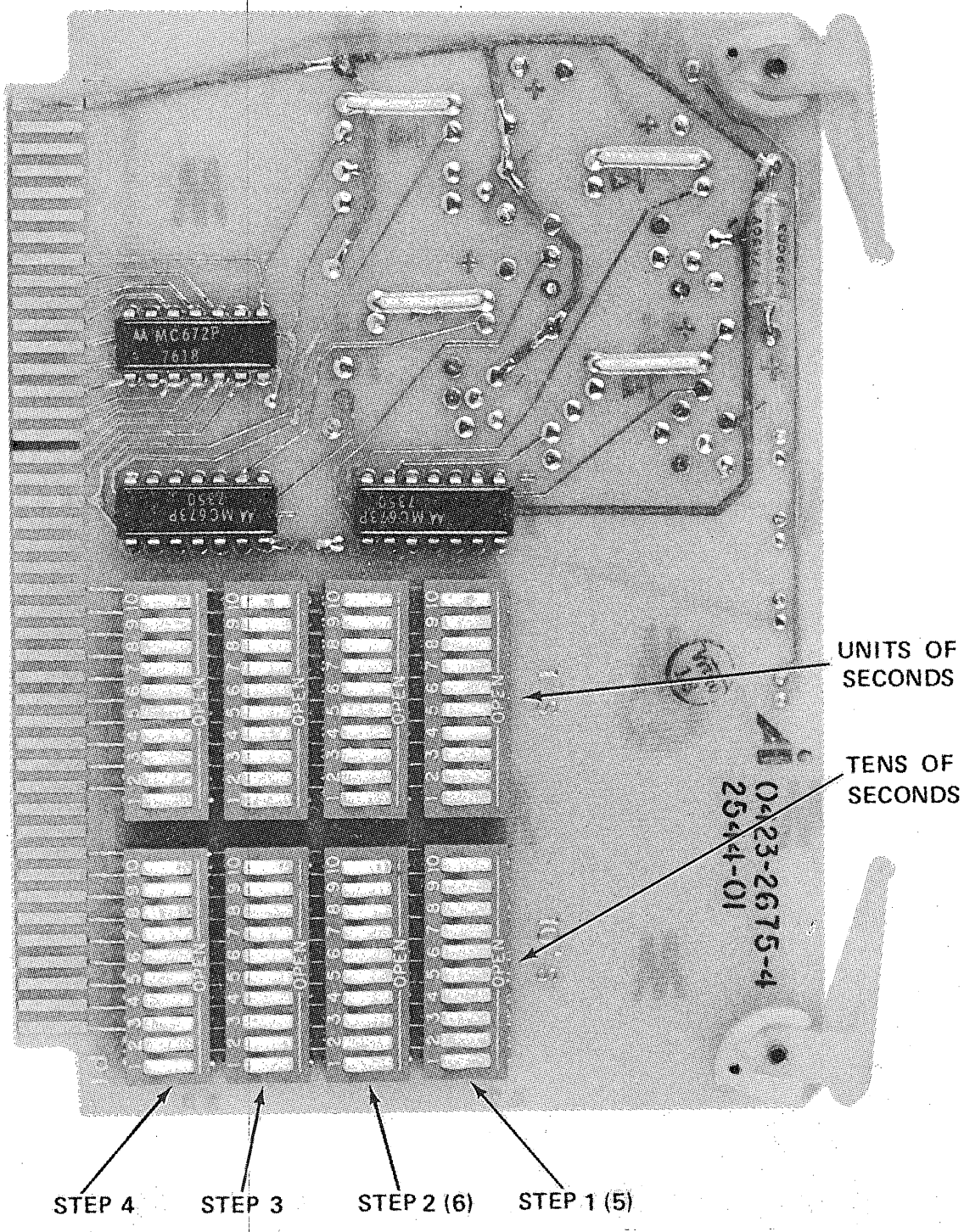

Figure 7. Step Card

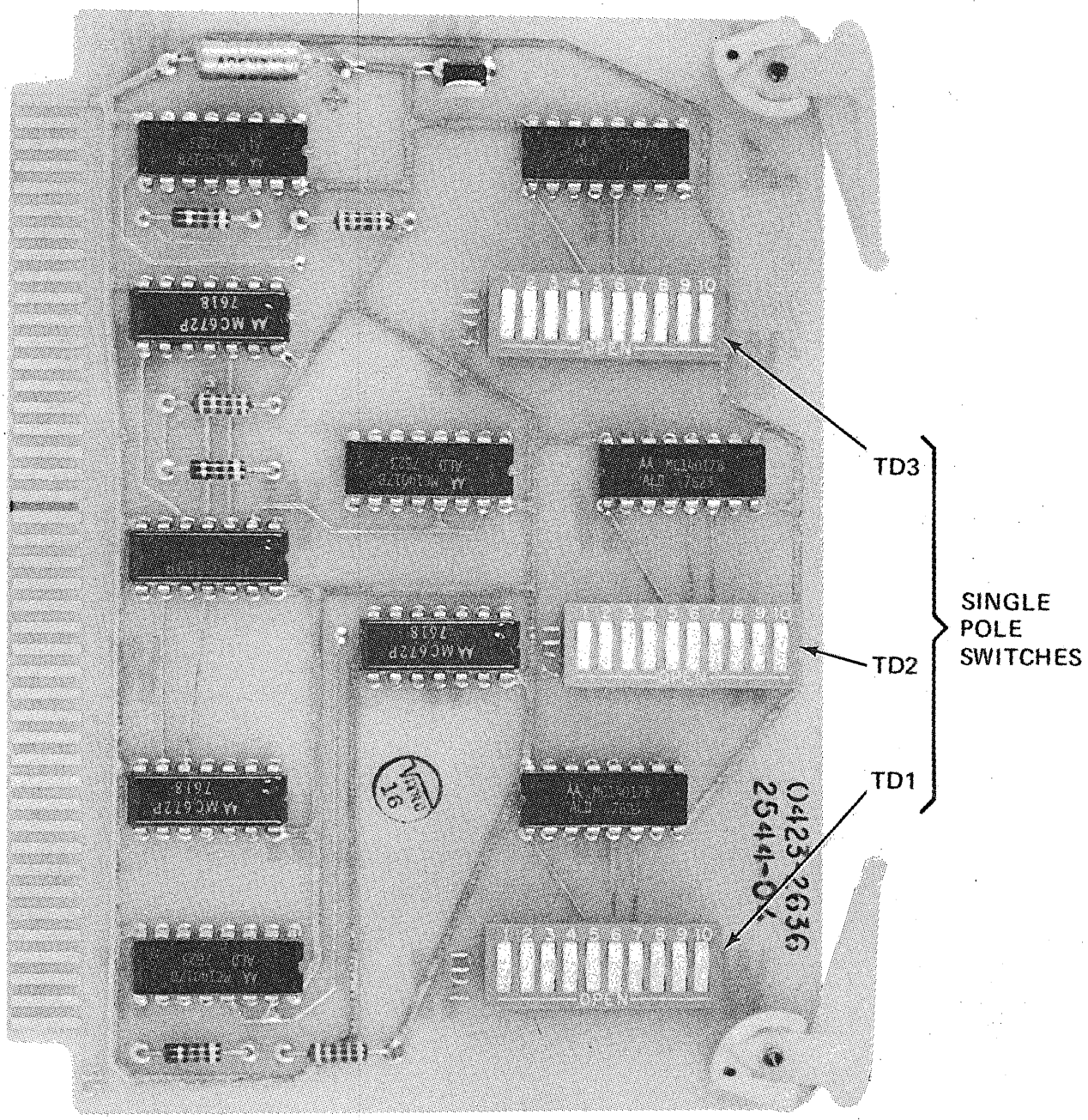

Figure 8. Time Delay/One Shot Card

Table 2. Bistable Card Trip Point Adjustments

CARD FILE SLOT	POTENTIAL TRANSFORMER	NOMINAL TRIP POINT
3	PT1-ØA	70%
4	PT1-ØA	80%
5	PT1-ØA	90%
11	PT1-ØC	70%
12	PT1-ØC	80%
13	PT1-ØC	90%
19	PT2-ØA	70%
20	PT2-ØA	80%
21	PT2-ØA	90%
27	PT2-ØC	70%
28	PT2-ØC	80%
29	PT2-ØC	90%

NOTE

70% corresponds to 84.0 V ac

80% corresponds to 96.0 V ac

90% corresponds to 108.0 V ac

7.3 TIMING ADJUSTMENTS

All sequencer step times and various other panel timing functions are field programmable by closing the applicable PC card rocker switches. There are two types of timing PC cards:

a. Step Card No. 3 (figure 7)

b. Time Delay/One Shot Card (figure 8)

Table 3 lists all programmable timing functions, the type of PC card utilized for that function, the slot location of the PC card, the setting location on the PC card for the timing function, and the step size corresponding to the incremental adjustment for the function.

7.3.1 SEQUENCER STEPS. All time delay adjustments for the maintained sequencer steps are located on a Step Card No. 3 PC card. Figure 7 shows the location of all adjustments on this card. To make the desired time delay adjustments, follow the procedures below:

a. Ensure all rocker switches are in the OPEN position.

b. Locate the proper pair of switch packages for the step desired. This pair includes a tens of seconds package and a units of second package.

c. Close the appropriate switch on the tens of seconds package corresponding to the desired number of tens of seconds, and close the appropriate switch on the units of seconds package corresponding to the desired number of units of seconds. Note that the number '10' corresponds to a zero setting and the remaining numbers coincide with the numerical value of the setting.

Table 3. Timing Adjustments

FUNCTION	CARD	SLOT	SETTING	STEP SIZE
BUV Step 1	Step Card No. 3	6	See fig. 7	1 sec
BUV Step 2	Step Card No. 3	6	See fig. 7	1 sec
BUV Step 3	Step Card No. 3	6	See fig. 7	1 sec
BUV Step 4	Step Card No. 3	6	See fig. 7	1 sec
BUV Step 5	Step Card No. 3	7	See fig. 7	1 sec
BUV Step 6	Step Card No. 3	7	See fig. 7	1 sec
LOP Step 1	Step Card No. 3	8	See fig. 7	1 sec
LOP Step 2	Step Card No. 3	8	See fig. 7	1 sec
LOP Step 3	Step Card No. 3	8	See fig. 7	1 sec
LOP Step 4	Step Card No. 3	8	See fig. 7	1 sec
LOP Step 5	Step Card No. 3	9	See fig. 7	1 sec
LOP Step 6	Step Card No. 3	9	See fig. 7	1 sec
LOCA Step 1	Step Card No. 3	14	See fig. 7	1 sec
LOCA Step 2	Step Card No. 3	14	See fig. 7	1 sec

Table 3. Timing Adjustments (Continued)

FUNCTION	CARD	SLOT	SETTING	STEP SIZE
LOCA Step 3	Step Card No. 3	14	See fig. 7	1 sec
LOCA Step 4	Step Card No. 3	14	See fig. 7	1 sec
LOCA Step 5	Step Card No. 3	15	See fig. 7	1 sec
Step 1 Pulse	TD/OS Card	16	TD1	.1 sec
Step 2 Pulse	TD/OS Card	16	TD2	.1 sec
Step 3 Pulse	TD/OS Card	16	TD3	.1 sec
Step 4 Pulse	TD/OS Card	17	TD1	.1 sec
Step 5 Pulse	TD/OS Card	17	TD2	.1 sec
Step 6 Pulse	TD/OS Card	17	TD3	.1 sec
PT1-70% Trip Delay	TD/OS Card	22	TD1	.1 sec
PT2-70% Trip Delay	TD/OS Card	22	TD2	.1 sec
70% BUV Pulse	TD/OS Card	22	TD3	.1 sec
PT1-90% Trip Delay	TD/OS Card	23	TD1	1 sec
PT2-90% Trip Delay	TD/OS Card	23	TD2	1 sec
70% BUV Delay	TD/OS Card	23	TD3	.5 sec
Real LOCA Input Delay	TD/OS Card	24	TD1	.1 sec
LOCA Delay	TD/OS Card	24	TD2	.5 sec
LOCA Pulse	TD/OS Card	24	TD3	.1 sec
Close DG BRKR PERM. Delay	TD/OS Card	25	TD1	.1 sec
LSS FAILURE DELAY	TD/OS Card	25	TD2	1 sec
PT1-80% Trip Delay #1	TD/OS Card	25	TD3	1 sec
PT2-80% Trip Delay #1	TD/OS Card	30	TD1	1 sec
PT2-80% Trip Delay #2	TD/OS Card	30	TD2	.1 sec
PT1-80% Trip Delay #2	TD/OS Card	30	TD3	.1 sec

7.3.2 TIME DELAYS AND ONE SHOTS. Sequence step pulsed outputs and the remaining timing functions are located on Time Delay/One Shot cards. Each TD/OS card contains three switch packages designated as TD1, TD2, and TD3, as shown in figure 8. The procedure for making these adjustments is similar to that for Step Card No. 3. However, the switch number on the appropriate package

should be considered not to represent absolute time but rather the number of incremental steps where the step size is as indicated in the last column of table 3, Timing Adjustments. The switch labeled '10' again corresponds to zero steps. For example, if it is desired to set the 70% BUV delay to three seconds, the TD3 switch package of the TD/OS card in card file slot 23 should be set so that all rocker switches are open except the one labeled 6 (.5 SEC X 6 = 3 SEC).

7.4 DC INPUT POWER

The ON/OFF power switch on the power supply panel provides on-off control of primary ESF power only. No provision exists at the LSS panel to disconnect BOP primary power. The BOP POWER ON indicator on the power supply is powered from the ESF power source, and therefore will always be off when ESF power is off even though BOP primary power is within the LSS panel.

7.5 INITIAL START-UP

Operating an LSS panel requires no specific start-up procedure. The following procedure, however, is recommended for initial system start-up for each LSS panel:

a. Position Auto Test switch to BLOCK/RESET.

b. Position power supply switch to OFF.

c. Position all bistable panel switches to OFF and control panel manual test switches downward to standby condition.

d. Ensure inputs and outputs are wired in accordance with all appropriate drawings.

e. Make all system timing settings as detailed in paragraph 7.3.

f. Ensure all PC cards, connectors, and relays are installed and properly locked in place.

g. Position power supply switch to ON.

h. Set all bistable trip points as detailed in paragraph 7.2.

i. Position Auto Test switch to ON.

The LSS Panel is now fully operational.

Section 8
TEST FEATURES

Each LSS panel is designed to combine Manual Test with an overlapping Automatic Test to verify LSS panel operation.

8.1 MANUAL TEST

The Manual Test functions provide for simulating actual LSS panel operating conditions by simulating real panel inputs utilizing test switches on the control panel, and verifying system status by observing control panel indicators. An LSS panel is placed in a Manual Test mode by application of one of two possible test mode inputs, PANEL or OUTPUT test mode. Either input allows the panel to be tested by simulating inputs, and both inputs cause all ESF and BOP outputs to be blocked, preventing operation of the output relays. In the OUTPUT test mode, the ESF and BOP output relays may be selectively operated utilizing the output test switches on the control panel.

In addition to the control panel MANUAL TEST functions, the calibration devices of the bistable panel may be utilized for various Manual Test functions. Bistable trip points may be approximately verified by applying a reduced potential transformer voltage via the voltage adjust switch and potentiometer pair to the associated bistable cards and correlating the bistable panel meter voltage with a trip indication by the bistable card LED's. Only one potential transformer channel should be tested at a time due to the two-out-of-four logic necessary for detection of an emergency condition.

The detection of any real input combination that constitutes an emergency condition causes the Manual Test function to be locked out, the panel to be reset from any previous test state, and the panel to then respond to the emergency condition. Manual testing may not be resumed until the emergency condition has ceased, and a remote system reset has been received.

To determine the proper system responses to any Manual Test function, consult Vitro drawing 2699-1001, Functional Logic Diagram, LSS panel.

8.2 AUTOMATIC TEST

The Automatic Test provides continuous LSS panel operation surveillance from the logic input signals through the logic and counter stages, and up to and including the relay driver outputs. The Automatic Test will not interfere with Power Station system requirements nor cause any output relay actuation during normal system operation. The Automatic Test continuously monitors the LSS panel and, upon an improper response, displays the step number of the failed test, causes the Auto Test to be blocked from further operation, and causes the normally operated LSS SYS FAILURE computer/annunciator relay to release for remote annunciation of the failure. The Automatic Test may be conveniently interrupted at any time by positioning the Auto Test switch on the control panel to BLOCK/RESET.

The Automatic Test has two operating modes, an active one and a passive one. In the active operating mode, the Auto Test generates Automatic Test Inputs (ATI's) to simulate panel input signals and other internal test signals. The system is then checked for appropriate Automatic Test Outputs (ATO's) from panel relay drivers and other internal circuits. A high frequency clock signal is substituted for the normal real-time clock signal to allow all system timers to be timed out rapidly. The ATI signals are of sufficient duration to test for proper system operation, but will not actuate output relays. An improper response during the test initiates local and remote fault annunciation. In the passive operating mode, the LSS panel is monitored for valid system inputs. Upon a valid system input occurring, the Automatic Test halts the test sequence, inhibits ATI's, and resets the Automatic Test circuits, allowing the system to respond to the valid system inputs.

8.2.1 AUTOMATIC TEST CIRCUIT DESCRIPTION. The Automatic Test functionally consists of the following:

a. Test Input Generator
b. Input Diode Matrix
c. Fault Logic
d. Buffer Logic.

The Automatic Test may be initiated in two ways. First, it may be initiated by positioning the Auto Test switch on the control panel from BLOCK/RESET to ON. Second, it may be initiated remotely if the Auto Test switch is

already in the ON position by momentary application of a RESET input signal. Either of these actions releases the Automatic Test from a blocked state, and allows the test input generator and the input diode matrix to simulate ATI's necessary for the various tests.

The Automatic Test is designed to produce 60 test steps per cycle, test steps 0 through 59. Test steps 0 through 9 take 100 msec each, and test steps 10 through 59 take 10 msec each, for a total test cycle time of 1.50 seconds. Each test step is divided into the passive and active operating modes. For steps 0 through 9, the first 10 msec is passive and the last 90 msec is active. For steps 10 through 59, the first 9 msec is passive and the last 1 msec is active.

8.2.1.1 Test Input Generator. The test input generator utilizes a 10 KHz clock signal to generate the sixty test step signals as well as associated timing signals necessary for contol functions.

8.2.1.2 Input Diode Matrix. The input diode matrix accepts individual step signals from the test input generator and applies the required ATI's to the system for the desired tests. It inherently provides the diode isolation that maintains the individuality of Automatic Test inputs and system inputs.

8.2.1.3 Buffer Logic. The buffer logic monitors various system output signals and provides signal conditioning functions such as counting, memorizing momentary signals, or inverting. It consists of inverter logic and memory circuits necessary to convert system outputs to signals compatible with the fault logic circuits.

8.2.1.4 Fault Logic. The fault logic monitors relay driver outputs via the buffer logic to verify LSS panel operation. It is segmented to provide individual decodes for each test step. During the active mode of a test step, as Automatic Test inputs are applied, all applicable system output signals are decoded to yield the proper Automatic Test output for the respective step. At the very start of the final 100 usec period of the test step, the Automatic Test output is sampled and stored. If a system fault existed in that step, a fault condition will be initiated. This fault condition is sealed-in,

annunciated remotely by the release of the LSS SYS FAILURE relay which is normally energized, and annunciated locally by display of the test step number in which the fault occurred. In addition to Auto Test failures, the fault logic serves to annunciate a power supply failure, a clock failure in the Clock Card, that the Auto Test switch is in the BLOCK/RESET position, that the Manual Test function has been operated, or that a valid system input signal has been received. In addition, the fault logic provides for local annunciation that the Auto Test circuits are functioning properly in the form of a pair of blinking points in the display which operates at a rate of one blink per second.

8.2.2 OPERATING INSTRUCTIONS. When initiated and functioning properly, the blinking points in the display provide the only local Automatic Test indication. The balance of the display is blanked. When a fault condition occurs, the digital readout is energized and displays the test step number at which the fault occurred.

Upon detecting a fault, the LSS panel indicators and output equipment status should be observed. Since some faults are self-annunciating (e.g., energized input or energized outputs), a simple status check may indicate the fault location.

Generally, the test number displayed indicates the test which the LSS panel failed to pass. It must be recognized, however, that a system clock failure can occur randomly in the Automatic Test sequence. In addition, since the same system outputs are monitored at many different times in the Automatic Test sequence, the test at which an output fails may not necessarily be its first appearance in the Automatic Test sequence. Therefore, after a fault is detected and a test number displayed, resetting and restarting the Auto Test simplifies the fault isolation by displaying the lowest test number involving the failure. An Automatic Test display of "88" in general does not indicate a system fault but rather indicates that the Auto Test is in a blocked state because of one or more of the following conditions:

a. Control panel Auto Test switch positioned to BLOCK/RESET
b. A real input detected

c. Any single bistable trip has occurred

d. System in a Manual Test mode

e. Internal Emergency Condition memory is set.

The Auto Test circuits are locked out as long as any of the above conditions continue to exist. Only after all the above conditions have been cleared may the Auto Test be re-initiated. If the Auto Test had been locked out by any of the conditions b through e above, so that the local Auto Test switch is already in the ON position, the Auto Test may then be restarted remotely by momentary application of the remote RESET input, which will first reset the Emergency Condition memory and return the system to STANDBY, and then restart the Auto Test upon its removal.

8.2.3 AUTOMATIC TEST SEQUENCE. After a fault has been detected, it is necessary to isolate and repair the failed component. As indicated in paragraph 8.2.2, some faults will be self-annunciating, thereby simplifying the isolation procedure. The remaining faults are non-annunciating and require Manual or Automatic Test features for detecting defective parts of the system. Once an Auto Test fault is detected and a test number displayed, the test details for the indicated test number can be obtained from tables 4 and 5.

Table 4. Automatic Test Sequence

STEP NO.	PRIMARY FUNCTIONAL TEST DESCRIPTION	ATI NO.	ATO SCHEM. LOC.
00	Fault logic masking check	None	None
01	Standby state check for no outputs with real-time clock	None	37D6
02	Test bistables PT1-ØA/70%, 80%, 90%	1	37B6
03	Test bistables PT1-ØC/70%, 80%, 90%	2	37A6
04	Test bistables PT2-ØA/70%, 80%, 90%	3	37A6
05	Test bistables PT2-ØC/70%, 80%, 90%	4	37D4
06	Test for presence of 100 Hz real time clock; fast clock substitution	5[1]	37D4
07	Test for presence of 20 Hz real time clock; fast clock substitution	5[1]	37C4
08	Test for presence of 10 Hz real time clock; fast clock substitution	5[1]	37C4
09	Test for no ESF outputs with emergency condition permissive supplied	32	37C4
10	1 out of 4 PT1-ØA bistable trips; emergency condition not detected	6, 7, 36	37B4
11	1 out of 4 PT1-ØC bistable trips; emergency condition not detected	8, 9, 37	37B4
12	1 out of 4 PT2-ØA bistable trips; emergency condition not detected	10, 11, 38	37B4
13	1 out of 4 PT2-ØC bistable trips; emergency condition not detected	12, 13, 39	37B4
14	Test 90% bus undervoltage via PT1ØA and PT2ØA	6, 10	37A4
15	Test 70% bus undervoltage via PT1ØA and PT2ØA	7, 11, 20	37D1
16	Test 90% bus undervoltage via PT1ØC and PT2ØC	8, 12	37C1

[1]ATI 5 is maintained until reset after step 59.

Table 4. Automatic Test Sequence (Continued)

STEP NO.	PRIMARY FUNCTIONAL TEST DESCRIPTION	ATI NO.	ATO SCHEM. LOC.
17	Test 70% bus undervoltage via PT1ØC and PT2ØC	9, 13	37C1
18	Test 70% bus undervoltage followed by 90% bus undervoltage	6, 7, 10, 11	37B1
19	Test 90% bus undervoltage followed by 70% bus undervoltage	6, 7, 10, 11	37B1
20	Test 90% bus undervoltage with DG BRKR CLOSED	6, 10, 16	37A1
21	Test LOCA condition	14, 20	38D6
22	Test for no ESF outputs without EMERG. COND. permissive	22, 23, 25, 26	38C6
23	Test for no sequencer initiation without any breaker closure	15, 23	38B6
24	Test for BUV and LOP sequencers enabled	23, 26	38B6
25	Test for no LOCA sequencer initiation without any breaker closure	15, 23, 25	38C4
26	Test for LOCA sequencer enabled via INC. BRKR closure	23, 25	38C4
27	Test for LOCA sequencer enabled via DG BRKR closure	15, 23, 25, 26	38B4
28	Test for no sequencer initiation via no power restoral	23, 25, 26	
29	Test for sequencer steps pulsed outputs and no maintained outputs	32, 33, 34, 35	38A4
30	Test for no sequencer steps outputs without EMERG. COND. permissive	27, 33, 34, 35	38C2
31	Test for step outputs via LOCA sequencer	27, 32, 33	38C2
32	Test for step outputs via BUV sequencer	27, 32, 34	38B2
33	Test for step outputs via LOP sequencer	27, 32, 35	38B2

Table 4. Automatic Test Sequence (Continued)

STEP NO.	PRIMARY FUNCTIONAL TEST DESCRIPTION	ATI NO.	ATO SCHEM. LOC.
34	Test for RESET input function	7, 11, 14, 20	39D6
35	Test for no ESF CLOSE BRKR outputs without EMERG. COND. permissive	24	39C6
36	Test for LOP output	18, 19, 20, 24	39C6
37	Test for CLOSE BRKR outputs	24, 32	39B6
38	Test for no CLOSE BRKR outputs with DG BRKR CLOSED	24, 26, 32	39A6
39	Test for no CLOSE BRKR outputs with 90% BUV	22, 24, 32	39A6
40	Test for CLOSE BRKR outputs via OFFSITE SOURCE 3	17, 18, 24, 32	39C4
41	Test for CLOSE BRKR outputs via OFFSITE SOURCE 1	18, 19, 24, 32	39B4
42	Test for CLOSE BRKR outputs via OFFSITE SOURCE 2	17, 19, 24, 32	39B4
43	Test for no CLOSE BRKR outputs and LOP outputs with no offsite sources available	17, 18, 19, 24, 32	39B4
44	Test for CLOSE BRKR outputs priority changed	18, 19, 21, 24, 32	39A4
45	Test for CLOSE BRKR outputs priority changed	17, 19, 21, 24, 32	39D2
46	Test for panel test mode permissive	28, 29	39C2
47	Test for panel test mode lockout via EMERG. COND.	16, 28, 29	39B2
48	Test for output test mode permissive	30, 31	39C2
49	Test for output test mode lockout via EMERG. COND.	16, 30, 31	39B2

Table 4. Automatic Test Sequence (Continued)

STEP NO.	PRIMARY FUNCTIONAL TEST DESCRIPTION	ATI NO.	ATO SCHEM. LOC.
50	Test 80% bus undervoltage via PT1ØA and PT2ØA	36, 38	43B5
51	Test 80% bus undervoltage via PT1ØC and PT2ØC	37, 39	43B5
52	Test 80% BUV output with LOCA	25, 36, 38	43A5
53	Test for no 80% BUV output with a 90% BUV trip	22, 25, 36, 38	43A5
54	Test for no 80% BUV output with no EMERG. COND. permissive	25, 40	43A5
55	Test 80% bus undervoltage via EMERG. COND.	25, 32, 40	43A5
56 thru 59	NO TEST FUNCTION	None	43A5

Table 5. Automatic Test Inputs

ATI NO.	SCHEMATIC LOCATION	DESCRIPTION
1	31D6	PT1ØA bistable inputs (3)
2	31D6	PT1ØC bistable inputs (3)
3	31D6	PT2ØA bistable inputs (3)
4	31D6	PT2ØC bistable inputs (3)
5	31C6	Fast clock enable
6	31C6	PT1ØA 90% bistable trip test
7	31B6	PT1ØA 70% bistable trip test
8	31A6	PT1ØC 90% bistable trip test
9	31A6	PT1ØC 70% bistable trip test
10	31D4	PT2ØA 90% bistable trip test
11	31C4	PT2ØA 70% bistable trip test
12	31B4	PT2ØC 90% bistable trip test
13	31B4	PT2ØC 70% bistable trip test
14	31B4	LOCA input
15	31A4	Incoming breaker not closed input
16	31A4	DG breaker closed input
17	31D1	Offsite Source 1 not available input
18	31C1	Offsite Source 2 not available input
19	31B1	Offsite Source 3 not available input
20	31A1	Reset input
21	31A1	Breaker closure priority change input
22	32D7	90% bus undervoltage test signal
23	32D6	70% bus undervoltage test signal
24	32C6	70% BUV test signal to breaker closing circuits
25	32D4	LOCA test signal
26	32C4	DG breaker closed test signal
27	32B4	BUV or LOCA memorized test signal
28	32B4	Manual Test BUV input signal
29	32B4	Panel test mode input

Table 5. Automatic Test Inputs (Continued)

ATI NO.	SCHEMATIC LOCATION	DESCRIPTION
30	32A4	Manual Test LOCA input signal
31	32A4	Output test mode input
32	32D2	Emergency condition test signal
33	32B2	LOCA sequencer enable test signal
34	32B2	BUV sequencer enable test signal
35	32A2	LOP sequencer enable test signal
36	43C4	PT1ØA 80% bistable trip test
37	43C4	PT2ØC 80% bistable trip test
38	43C4	PT2ØC 80% bistable trip test
40	43B4	80% bus undervoltage test signal

Section 9
MAINTENANCE, TROUBLESHOOTING, AND REPAIR

An LSS panel requires no preventative or periodic maintenance. It is recommended, however, that bistable trip point verification be made on a periodic basis. In general, bistable trip point recalibration should be performed on all bistables off a common potential transformer channel any time a bistable card substitution is made or card file slot is changed. System timing functions need no periodic calibration, but may be changed, however, by following the adjustment procedures of section 7.3.

An LSS panel comprises an intricate electronic system. Before a system malfunction can be detected, it is essential that troubleshooting personnel be familiar with proper equipment operating characteristics, basic theory of operation, and electrical schematics. A malfunction can be detected in two possible manners. First, for failures which are self-annunciating, either indicators or actuated outputs annunicate and isolate the problem area. Second, during active testing with Manual Test features, an inoperative function will annunciate and isolate the problem area. After the malfunction has been detected and the general problem area located, Vitro drawing 2699-1021, LSS Panel, Electrical Schematics should be consulted and utilized to isolate the malfunction to a PC card or other part. On Vitro drawing 2699-1021, logic and electronic symbols have an associated reference designation number associated with them. This number refers to the PC card file slot of the PC card containing the particular component or the part identification number utilized in the cabinet. After the malfunction has been isolated, the suspect PC card or other part should be removed and replaced with a spare of the same type. Manual Test features should then be utilized to verify proper system operation.

CAUTION

Inserting or removing PC cards with the ESF portion of the system energized may cause equipment damage. The ESF power switch should be switched off whenever PC cards are removed or inserted. BOP power should be removed external to the LSS panel before troubleshooting within the isolation barrier.

If more than one PC card has been replaced, final determination of a PC card containing a failed device may be accomplished by replacing PC cards one at a time and verifying proper system operation after each insertion. This procedure verifies operational PC cards and eliminates them from further fault isolation activity.

9.1 SPARE PARTS

A list of recommended spare parts for an LSS panel is presented in table 6. Complete parts lists may be found on the following Vitro drawings:

2699 - 1005, LSS Panel Assembly
2699 - 1014, Digital Isolator Panel Assembly (A5)
2699 - 1015, Card File Assembly (A1)
2699 - 1025, Control Panel Assembly (A3)
2699 - 1030, Power Supply Panel Assembly (A2)
2699 - 1035, Bistable Panel Assembly (A4)

Table 6. Spare Parts List

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER	MANUFACTURER
CR1/15,A2CR1/3	Diode assembly	0423-2765-1	Vitro
K1/32	Relay, 24V	GPB	Agastat
K33/41,A2K2	Relay, 24V	3SAA1388A2	General Electric
K42/55,A2K3,K63	Relay, 125V	35AA1425A2	General Electric
K56/62	Relay, 125V	GPD	Agastat

Table 6. Spare Parts List (Continued)

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER	MANUFACTURER
-	TD/OS CARD	0423-2636	Vitro
-	7 Seg. Dis. Drvr.	0423-2640-2	Vitro
-	Step Card No. 3	0423-2675-4	Vitro
-	IC Card A-3	0423-2693-3	Vitro
-	IC Card A-4	0423-2693-4	Vitro
-	IC Card A-7	0423-2693-7	Vitro
-	IC Card A-9	0423-2693-9	Vitro
-	IC Card A-12	0423-2693-12	Vitro
-	IC Card B-1	0423-2695-1	Vitro
-	IC Card B-2	0423-2695-2	Vitro
-	IC Card B-4	0423-2695-4	Vitro
-	IC Card C-1	0423-2696-1	Vitro
-	IC Card D-2	0423-2697-2	Vitro
-	Comp. Card B-1	0423-2699-1	Vitro
-	Comp. Card B-7	0423-2699-7	Vitro
-	AC Bistable Card No. 1	0423-2757	Vitro
-	Driver Card	0423-2758-1	Vitro
-	Clock Card A	0423-2767	Vitro
A2DS1,2	Indicator Lens Lamp	95-0408-09-241 52-0991 B1-A	Dialco Dialco ANSI Spec.
A2F1,2	Fuse Fuseholder	MDA-7 HKL	Bussmann Bussmann
A2K1	Relay, 15V	3SAA1432A2	General Electric
A2PS1	Power Supply, 15V	CEA3B150Y103FLP3	CEA

OR PH300F110-15 LAMBDA

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Table 6. Spare Parts List (Continued)

REFERENCE DESIGNATION	DESCRIPTION	PART NUMBER	MANUFACTURER
A2PS2	Power supply, 24V	~~CEA3A240Y103FLP3~~ PH300F110-24	~~CEA~~ LAMBDA → VMA 02/0045
A2S1	Switch, Lock	OT22KA1 (OR OT2K1)	Westinghouse
	Contact block	OT2M → VMA 03/0016	Westinghouse
A2VR1-3	Suppressor, transient	1.5K62	General Semi.
A3DS1-12, A3DS15-35	Lamp, Indicating (Red)	0116B6708G1-R	General Electric
	Lamp, Indicating (White)	0116B6708G1-W	General Electric
	Lamp, Indicating (Yellow)	0116B6708G1-Y	General Electric
	Lamp, 24V (bulb only)	1819	GE or equal
A3DS13,14	Readout module	710-0301-025	Dialco
	Lamp, 24V (bulb only)	334	GE or equal
A3S1-9	Switch, toggle	8A2011C	Microswitch
A3 S10-S31	Switch, pushbutton	8N2021C	Microswitch
	Cap (black)	8Z0083	Microswitch
A3F1-4	Fuse	MKB 1/8	Bussmann
	Fuse block	3828-4	Bussmann
A4M1-4	Voltmeter, AC	10420	Simpson
A4R1-R4	Resistor, variable	7466R10KL.25	Beckman
A4R5-8	Resistor	RER55F1212M	MIL-R-39009/2
A4S1-4	Switch	OT2S1	Westinghouse
	Contact block	OT2A	Westinghouse
A4T1-8	Transformer	H-915	United Trans. or equal
A5R1-3	Resistor	RER65F3481M	MIL-R-39009/1
A5U1-10	Digital isolator	0423-2645-3	Vitro
	Lamp, 28V (bulb only)	30938-0 (OR 938I-C)	Sylvania
*	Screwdriver	H-90	Bourns
*	Patch cord	1530-60	H.H. Smith

* Special tools and accessories

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Price List
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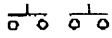
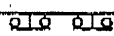
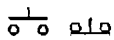
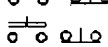
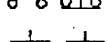
Flush Pushbutton Operators

Operator	Color	Operator Only Without Contact Block or Legend Plate (Cover Mounting Only) Catalog Number
Full Shroud 	All Colors (Black, Red, Green, Yellow, Blue, Gray, Brown)	OT2B4
No Shroud 	Black Red Green Yellow	OT2C1 OT2C2 OT2C3 OT2C4
Mushroom Head 	Black Red Green Yellow	OT2D1 OT2D2 OT2D3 OT2D4
Cylinder Lock  Key Removable in Locked Position Only	Lock Positions Out In In or Out	 OT2E8 OT2F8 OT2G8
Key Removable in All Positions	Out In In or Out	OT2E9 OT2F9 OT2G9

Pushbutton Ratings, Amperes
(For Flush and Extended Operators)

Voltages	Normal Load Break	Inrush and Interr. Capacity	Continuous
110-125 Ac	6.0	60	10
220-250 Ac	3.0	30	10
440-480 Ac	1.5	15	10
550-600 Ac	1.2	12	10
110-125 Dc	1.1	1.1①	
230-250 Dc	.55	.55①	
550-600 Dc	.20	.20①	

Contact Blocks – For Flush Operators②

	Description	Contact Symbol	Catalog Number
Single Circuit 	1 NO		OT2B
	1 NC		OT2D
Double Circuit 	2 NO		OT2M
	2 NC		OT2N
	1 NO, 1 NC		OT2A
	1 NO, 1 NC Make Before Break		OT2V
	2 NO Sequence One Pole Makes Before Other		OT2X
	1 NO, 1 NC Series Wired		OT2AS
	1 NO, 1 NC Parallel Wired		OT2AP
	2 NO, 2 NC Series Wired		OT2MS
	2 NO, 2 NC Parallel Wired		OT2MP

① For applications requiring higher Dc ratings, refer to Westinghouse.
② Torque for mounting screws 7 to 10 inch pounds – 10 inch pounds max.

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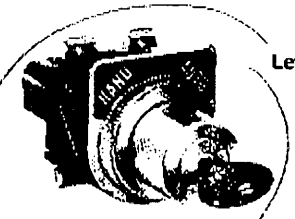
Flush Selector Switches

Standard Handle②④

Lever Handle②④



Cylinder Lock③

Type Operation	Operators Only Legend Plate Not Included③			
	2 Position	3 Position		
	Cam 1 Cat. No.	Cam 2 Catalog Number	Cam 4 Catalog Number	Cam 6 Catalog Number
Standard Handle				
Maintained	OT2S1	OT2S2	OT2S4	OT2S6
Spring Return Right to Left	OT2I1	.....	.....	.....
Spring Return Lft. & Rt. to Ctr.	.....	OT2V2	OT2V4	OT2V6
Spring Return Right to Center	.....	OT2Z2	OT2Z4	OT2Z6
Spring Return Left to Center	.....	OT2W2	OT2W4	OT2W6
Lever Handle				
Maintained	OT2S1W	OT2S2W	OT2S4W	OT2S6W
Spring Return Right to Left	OT2I1W	.....	.....	.....
Spring Return Lft. & Rt. to Ctr.	.....	OT2V2W	OT2V4W	OT2V6W
Spring Return Right to Center	.....	OT2Z2W	OT2Z4W	OT2Z6W
Spring Return Left to Center	.....	OT2W2W	OT2W4W	OT2W6W
Cylinder Lock				
Lock in All Positions	OT2K1	OT2K2	OT2K4	OT2K6
~~Lock in Left Positions~~	~~OT2Y1~~	.....	.....	.....
Lock in Center Positions	.....	OT2Y2	OT2Y4	OT2Y6
Lock in Ctr. & Rt. Positions	.....	OT2O2	OT2O4	OT2O6

Selector Switch Selection Procedure

Westinghouse OT2 selector switch cam and contact selection is based on the fact that there are only two possible 2-position contact sequences, and six possible 3-position sequences.

For two position, only cam 1 is available. Contact sequence is accomplished by selection of NO (OT2B) or NC (OT2D) contact blocks in desired quantities.

Three cams (2, 4, 6) produce all six 3-position sequences. Selection is simplified by using the systematic selection process below.

Procedure	Example
1. Write down contact sequence and sequence numbers from Table I. (X = Closed, O = Open)	XOO = 1B OXX – 1D XXO = 3D OXO = 2D
2. Determine two most common numbers (1, 2, or 3) ignoring letters B and D).	1 and 2
3. Use cam according to Table II and select operator Cat. No.	Cam 4, Cat. No. OT2S4
4. From Table I, determine Cat. No. and circuit position for each contact sequence number in Step 1.	1B = OT2B Left 1D = OT2D Left 3D – OT2AP Both 2D = OT2D Right
5. Order Bill of Material as determined, or fully assembled selector switch.	Standard Operator OT2S4 with following contact blocks: OT2B Left, OT2D Left, OT2AP Both, OT2D Right.

Table I: Cam and Contact Block Selection, Two and Three Position

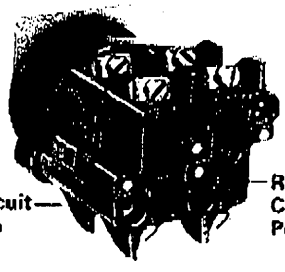
Contact Sequence (Operator Position Viewed From Front)	Seq. No.	Cam and Contact block Combination							
		Cam 1		Cam 2		Cam 4		Cam 6	
		Stand. Oper.① Cat. No. OT2S1		Stand. Oper.① Cat. No. OT2S2		Stand. Oper.① Cat. No. OT2S4		Stand. Oper.① Cat. No. OT2S6	
		Contact Cat. No.	Circuit Posit. ⑦	Contact Cat. No.	Circuit Posit. ⑦	Contact Cat. No.	Circuit Posit. ⑦	Contact Cat. No.	Circuit Posit. ⑦
Two Position									
X O	..	OT2D	Either	....	....	....	....	....	....
O X	..	OT2B	Either	....	....	....	....	....	....
Three Position									
X O O	1B	....	....	OT2AS	Both⑥	OT2B	Left	OT2B	Right
O X X	1D	....	....	OT2AP	Both⑥	OT2D	Left	OT2D	Right
X O X	2B	....	....	OT2B	Right	OT2B	Right	OT2MP	Both⑨
O X O	2D	....	....	OT2D	Right	OT2D	Right	OT2NS	Both⑩
O O X	3B	....	....	OT2B	Left	OT2AS	Both⑥	OT2B	Left
X X O	3D	....	....	OT2D	Left	OT2AP	Both⑥	OT2D	Left

Table II: Sequences to Cam Number – 3 Position

Sequence Number	Cam Number
1	6 or 4
2	2 or 4
3	2 or 6
1 and 2	4
1 and 3	6
2 and 3	2

① Standard and lever handle operators supplied with red color insert.
③ For price of contact block and legend plates, see pages 7 and 8.
④ To position contact block 90° from normal, add suffix "G" to catalog number.
⑤ Two contacts wired in series (NC left and NO right). Can be field assembled from one OT2A or one OT2B and one OT2D contact blocks.
⑥ Two contacts wired in parallel (NC right and NO left). Can be field assembled from one OT2A or one OT2B and one OT2D contact blocks.
⑦ As viewed from rear of assembly.
⑧ For other than standard maintained operator, use operator catalog number from price table.
⑨ Two NO contacts wired in parallel.
⑩ Two NC contacts wired in series.

Circuit Position For Mounting Contact Blocks Determined By Viewing From Rear



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O X

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PAGE 5 OF 6

Westinghouse Electric Company LLC
Repair & Replacement Services
1000 Westinghouse Drive
New Stanton, PA 15672
(724) 722-5927

facsimile transmittal

To:	Daryl (? Spelling)	Fax : 601 437 ~~2175~~ 2379	
From:	Sharon Miller	Date 1/23/03	
Re:	PO MPY30021 W.S.O. 20231	Pages: 1	
CC:		FAX: (724) 722-5462	

☐ Urgent x For Review ☐ Please Comment ☐ Please Reply ☐ Please Recycle

Notes: Daryl

Attached is a cut sheet of the OT22KA1. According to the vendor, the OT22KA1 has been replaced by the OT2K1 and is a 2 position operator. This product was developed back in the 60's and early 70's and there is not much information to provide. Engineering was able to find that the mounting for the OT22KA1 was 1 7/32 and it is the same for the OT2K1 1 7/32. I think this helps to conclude that they are approximate in size.

I hope this helps in your analysis. If you have any questions, please contact me.

Sharon

724 722-5927

BH 2/3/03
VMA 03/~~0116~~ 0016
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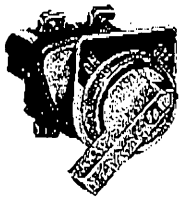
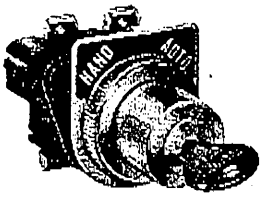
Flush Selector Switches

Standard Handle②④



Lever Handle②④



Cylinder Lock④

Selector Switch Selection Procedure

Westinghouse OT2 selector switch cam and contact selection is based on the fact that there are only two possible 2-position contact sequences, and six possible 3-position sequences.

In two position, only cam 1 is available. Contact sequence is accomplished by selection of NO (OT2B) or NC (OT2D) contact blocks in desired quantities.

Three cams (2, 4, 6) produce all six 3-position sequences. Selection is simplified by using the systematic selection process below.

Procedure	Example
1. Write down contact sequence and sequence numbers from Table I. (X = Closed, O = Open)	XOO = 1B OXX = 1D XXO = 3D OXO = 2D
2. Determine two most common numbers (1, 2, or 3) ignoring letters B and D.	1 and 2
3. Use cam according to Table II and select operator Cat. No.	Cam 4, Cat. No. OT2S4
4. From Table I, determine Cat. No. and circuit position for each contact sequence number in Step 1.	1B = OT2B Left 1D = OT2D Left 3D = OT2AP Both 2D = OT2D Right
5. Order Bill of Material as determined, or fully assembled selector switch.	Standard Operator OT2S4 with following contact blocks: OT2B Left, OT2D Left, OT2AP Both, OT2D Right.

Type Operation	Operators Only Legend Plate Not Included⑪			
	2 Position	3 Position		
	Cam 1 Cat. No.	Cam 2 Catalog Number	Cam 4 Catalog Number	Cam 6 Catalog Number
Standard Handle				
Maintained	OT2S1	OT2S2	OT2S4	OT2S6
Spring Return Right to Left	OT2I1	.....	.....	.....
Spring Return Lft. & Rt. to Ctr.	.....	OT2V2	OT2V4	OT2V6
Spring Return Right to Center	.....	OT2Z2	OT2Z4	OT2Z6
Spring Return Left to Center	.....	OT2W2	OT2W4	OT2W6
Lever Handle				
Maintained	OT2S1W	OT2S2W	OT2S4W	OT2S6W
Spring Return Right to Left	OT2I1W	.....	.....	.....
Spring Return Lft. & Rt. to Ctr.	.....	OT2V2W	OT2V4W	OT2V6W
Spring Return Right to Center	.....	OT2Z2W	OT2Z4W	OT2Z6W
Spring Return Left to Center	.....	OT2W2W	OT2W4W	OT2W6W
Cylinder Lock				
Lock in All Positions	OT22KA1	OT23KA2	OT23KA4	OT23KA6
Lock in Left Position	OT22KE1	.....	.....	.....
Lock in Center Position	.....	OT23KC2	OT23KC4	OT23KC6
Lock in Ctr. & Rt. Position	.....	OT23KE2	OT23KE4	OT23KE6

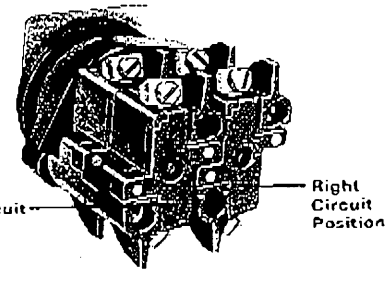
Table I: Cam and Contact Block Selection, Two and Three Position

Contact Sequence (Operator Position Viewed From Front)	Seq. No.	Cam and Contact Block Combination							
		Cam 1		Cam 2		Cam 4		Cam 6	
		Stand. Oper.⑥ Cat. No. OT2S1		Stand. Oper.⑩ Cat. No. OT2S2		Stand. Oper.⑥ Cat. No. OT2S4		Stand. Oper.⑥ Cat. No. OT2S6	
		Contact Cat. No.	Circuit Posit. ⑦	Contact Cat. No.	Circuit Posit. ⑦	Contact Cat. No.	Circuit Posit. ⑦	Contact Cat. No.	Circuit Posit. ⑦
Two Position									
X O	..	OT2D	Either	....	....	....	....	....	....
O X	..	OT2B	Either	....	....	....	....	....	....
Three Position									
X O O	1B	....	....	OT2AS	Both⑤	OT2B	Left	OT2B	Right
O X X	1D	....	....	OT2AP	Both⑥	OT2D	Left	OT2D	Right
X X O	2B	....	....	OT2B	Right	OT2B	Right	OT2MP	Both⑨
O X O	2D	....	....	OT2D	Right	OT2D	Right	OT2NS	Both⑩
O O X	3B	....	....	OT2B	Left	OT2AS	Both⑤	OT2B	Left
X X O	3D	....	....	OT2D	Left	OT2AP	Both⑥	OT2D	Left

Table II: Sequences to Cam Number — 3 Position

Sequence Number	Cam Number
1	6 or 4
2	2 or 4
3	2 or 6
1 and 2	4
1 and 3	6
2 and 3	2

Circuit Position For Mounting Contact Blocks Determined By Viewing From Rear.



⊖ Changed since previous issue.

⑦ Standard and lever handle operators supplied with red color insert. Other colors are available.

⑪ For price of contact block and legend plates, see pages 53, 54.

④ To position contact block 90° from normal, add suffix "G" to catalog number.

⑤ Two contacts wired in series (NC left and NO right). Can be field assembled from one OT2A or one OT2B and one OT2D contact blocks.

⑥ Two contacts wired in parallel (NC right and NO left). Can be field assembled from one OT2A or one OT2B and one OT2D contact blocks.

⑦ As viewed from rear of assembly.

② For other than standard maintained operator, use operator catalog number from price table.

⑨ Two NO contacts wired in parallel.

⑩ Two NC contacts wired in series.

I/C LOGIC FOR CONTROL FUNCTIONS IN HIGH-NOISE INDUSTRIAL ENVIRONMENTS

TABLE OF CONTENTS

I/C LOGIC FOR CONTROL FUNCTIONS IN HIGH-NOISE INDUSTRIAL ENVIRONMENTS

INTRODUCTION AND PHILOSOPHY

Motorola's high threshold logic (MHTL*) family derived its name from the fact that it operates from a nominal 15-volt power supply and exhibits a typical input threshold at 7.5 volts. Because of the high power supply, there is a tendency for greater power dissipation in the circuit. To minimize this dissipation, larger resistor values are employed, which generally result in slower operation. This slower operating speed aids in noise rejection.

With MHTL design, fewer special noise protective methods are necessary; thus, more reliable operation can be achieved in the presence of noise conditions. Higher input threshold voltage combined with a slower response time enables MHTL to excel in both internal and external electrical noise rejection, as compared with other logic families. Better noise immunity is also achieved at the power supply and ground leads, in addition to the signal leads.

Because the system designer has a multiplicity of device types to choose from in the MHTL line, he is able to realize his system objectives with a minimum of parts. Recently introduced translator circuits make possible the usage of MHTL units in areas where high electrical noise exists, and then translating into higher speed, low-level controlling systems. The translator circuits allow MHTL logic levels to be changed to and from the logic levels characteristic of RTL, DTL and TTL circuits, making a combined system extremely attractive for industrial applications.

The high 15-volt power supply voltage of MHTL also makes it easy to interface with discrete components and CMOS—another attractive feature of the devices. MHTL circuits are especially adaptable to numerical control, supervisory control, and computer-peripheral equipment design.

All available data about Motorola's high threshold logic line of integrated circuits for industrial high-noise environment control have been compiled into this convenient single-source "library" for your design use. Included are detailed data specifications for all available MHTL circuits, as well as application design information to assist you in making greater use of these superior high-noise immunity circuits.

In addition, a reply card is included for requesting MHTL applications information and assistance.

Trademark of Motorola Inc.

MHTL

GENERAL INFORMATION

MC660 Series

ISSUE A

INTRODUCTION

MHTL is Motorola's High Threshold Logic family of digital integrated circuits. MHTL is designed for applications in which a high degree of noise immunity is required and high-speed operation is not normally necessary. Exhibiting a large logic swing (13 V typical) and 110 ns typical propagation delays, MHTL has large voltage and energy noise margins.

The basic MHTL logic gate is the NAND function with either active or passive pullup provided. The broad line of basic functions includes expanders, AND-OR-INVERT gates, exclusive OR gates, drivers, gated latches, translators, hex inverters, flip-flops, and multivibrators. The basic logic functions plus complex functions give MHTL good versatility in applications requiring high noise immunity.

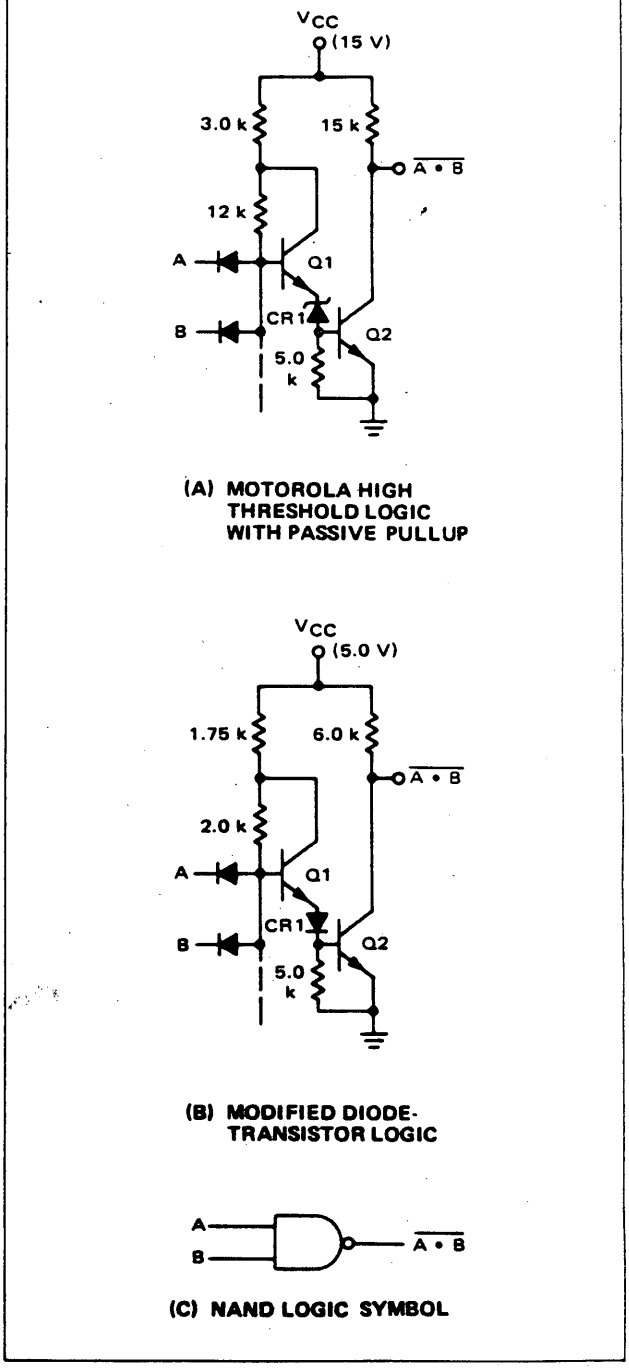
TYPICAL CHARACTERISTICS

Rating	Value	Unit
Supply Voltage	15 ± 1.0	Vdc
Threshold Voltage	7.5	Vdc
Logic "0" Output Voltage @ I_{OL} = 5 ma		
(Active Pullup Output)	1.0	Vdc
(Passive Pullup)	0.4	Vdc
Logic "1" Output Voltage @ V_{CC} = 15 V		
(Active Pullup Output)	14.4	Vdc
(Passive Pullup)	14.9	Vdc
Noise Margin	6.0	Vdc
Propagation Delay	110	ns
Temperature Range	−30 to +75	°C

THE BASIC MHTL LOGIC GATE

The basic MHTL gate is shown in Figure 1(A). It may be noted that this gate is very similar in configuration and operation to the Motorola Diode-Transistor Logic (MDTL) gate shown in Figure 1(B). The basic difference is in diode CR1, resistor values, and the collector supply voltage (V_{CC}). In MDTL, CR1 is a base-emitter diode operated in its forward direction and having a drop of approximately 0.75 volt. The input threshold level of MDTL is a net of two forward diode drops (the input diode offsets a diode drop in the other direction) or about 1.5 volts. In MHTL, CR1 is a base-emitter junction that is operated in its reverse direction; this is commonly called zener operation. Conduction occurs, in this case, when the junction has approximately 6.7 volts across it. The thres-

FIGURE 1 – GATE COMPARISONS



(A) MOTOROLA HIGH THRESHOLD LOGIC WITH PASSIVE PULLUP

(B) MODIFIED DIODE-TRANSISTOR LOGIC

(C) NAND LOGIC SYMBOL

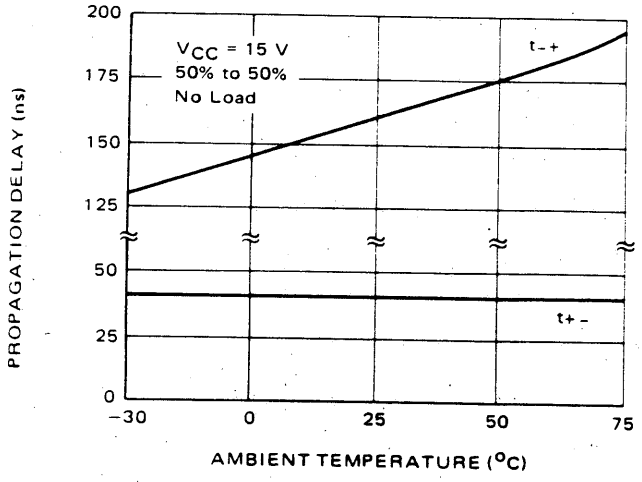
hold voltage for MHTL is one forward diode drop plus one zener diode drop or about 7.5 volts. The normal supply voltage for this family is 15 volts ±1.0 volt. To keep the power dissipation down, the gates have higher resistance values than comparable resistors in MDTL devices.

The MHTL gate provides the same positive-logic NAND function as the MDTL gate. If either the A or B input is below the threshold level, possible base current to the transistor Q1 is routed to the low input. If both inputs are above the threshold level, Q1, CR1 and output transistor Q2 all turn on and the output goes low. Thus the output is true or high if A or B is not true, i.e., $F = \overline{A} + \overline{B} \equiv \overline{A \bullet B}$ (See Figure 1-c).

PROPAGATION DELAY TIMES

The MHTL family of devices exhibits a slower propagation time than normally provided by other integrated circuit logic families. This is an additional aid in rejecting electrical noise because of the inability of the circuits to respond to narrow spikes of noise. Maximum propagation delays for each device are given on the appropriate data sheets. For these measurements, loading composed of a discrete RC network simulates full fan-out for the device. Typical values of propagation delays for the NAND gate with active pullup output are shown as a function of temperature in Figure 2.

FIGURE 2 – TYPICAL "NAND" GATE PROPAGATION DELAY TIMES



CHARACTERISTICS OF NOISE IMMUNITY

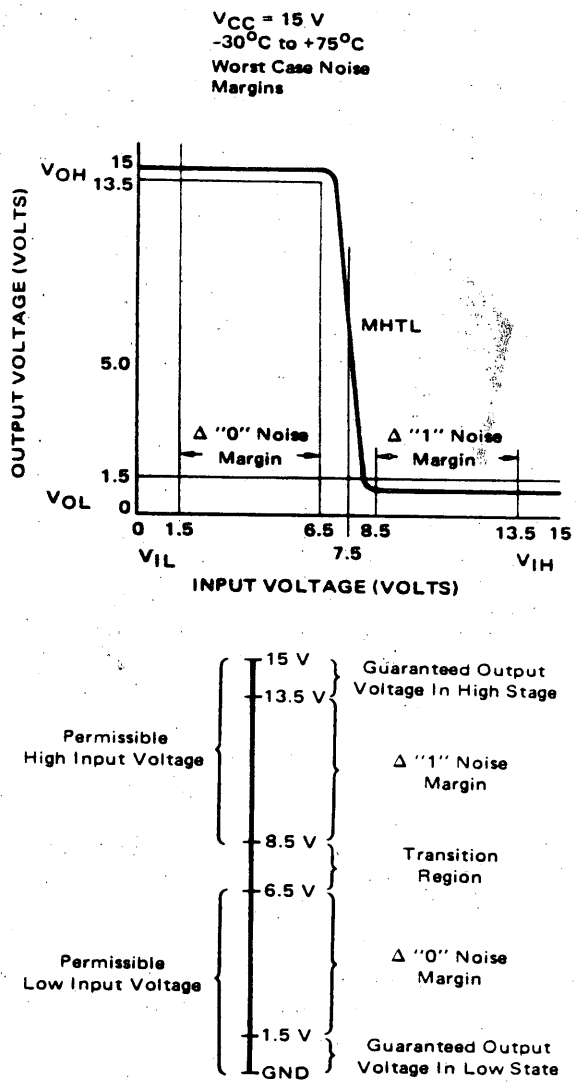
Noise immunity is a measure of the ability of a logic family to reject erroneous signals which cause false conditions in a system. When discussing the effects of noise, certain characteristics of noise must be defined.

DC Noise Margin

To define dc noise margin, the transfer characteristics of an MHTL gate must be considered. The transfer curve for the basic gate operating with a 15-volt supply is shown in Figure 3. For any input signal up to 6.5 volts, the output will remain in the high state or above 13.5 volts. A 2.0-volt margin, from 6.5 to 8.5 volts, is used for the transition region and guards against variations in manufacturing lots and temperature effects from -30°C to +75°C. With 8.5 volts on the input, the output is in the low state or less than 1.5 volts and remains there for any further increase in input voltage.

The specified voltages in the MHTL transfer curve are placed in the dc noise margin chart. The dc noise margin is defined as the difference between the output voltage levels guaranteed for the driving gate and the input voltages required for the driven gate to recognize a "0" or a "1" logic level. Then, the guaranteed noise margin in the high state is calculated by subtracting 8.5 volts from 13.5 volts, and the guaranteed noise margin in the low state is calculated by subtracting 1.5 volts from 6.5 volts. The guaranteed

FIGURE 3 – TRANSFER CURVE AND DC NOISE MARGIN CHART



noise margin is 5.0 volts in either the high or low state. In operation, noise margin is typically 6.0 volts. As a comparison, the 5.0-volt logic families have a threshold voltage of 1.5 volts with typical noise margins of 1.2 volts. Thus, the dc noise margin is 5 times greater for MHTL.

The dc noise margin describes the ability of the circuits to operate correctly when dc offsets and power supply variations exist between boards in a multiboard system. The MHTL circuits have an inherent advantage with respect to dc noise margins.

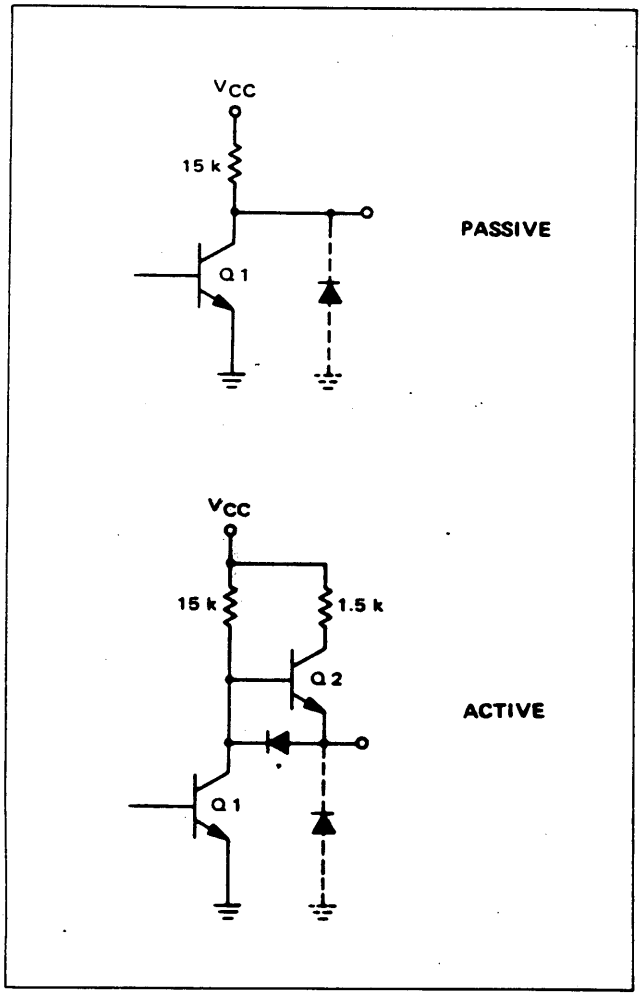
AC Noise Immunity

The ac noise immunity may be defined as the ability of a digital circuit to reject unwanted ac noise on the signal line, V_{CC} power supply line, and the ground line. The ac noise immunity is dependent on the magnitude and duration of voltage change required to cause a system disturbance. The voltage change is dependent upon the nature of the noise, the coupling impedance, and the internal impedance of the digital circuit.

AC Noise Immunity of Active versus Passive Pullup

The relatively slow speed and large voltage swing of MHTL give the logic family superior dc noise margins and ac noise immunity.

FIGURE 4 – MHTL GATE WITH PASSIVE AND ACTIVE PULLUP



To maximize its high noise immunity, MHTL provides active pullup gates in addition to passive pullup devices. Although passive pullup has advantages in certain applications, the active pullup shows superior noise immunity.

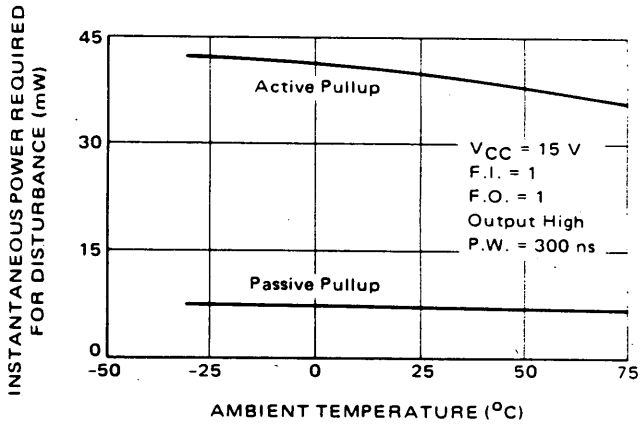
The active pullup is compared to the passive configuration in Figure 4. The passive pullup has a 15 kilohm resistor to the power supply whereas the active pullup has a transistor and 1.5 kilohm resistor to the power supply. When the outputs are in the low state, both pullups exhibit a low impedance to ground through a saturated transistor. The advantage of active pullup appears when the outputs are in the high state.

The outputs are in the high state when transistor Q1 is turned off. The passive pullup exhibits a 15 kilohm impedance to V_{CC}. The active pullup has a lower impedance to V_{CC} as transistor Q2 turns on and has a low impedance in series with the 1.5 kilohm resistor.

If the input of another gate is driven by an output, the lower output impedance of the active pullup requires more current than the passive pullup to cause a low state on the input of the second gate. Because more current is necessary, more energy must be used to change the state of the input.

When an output is in the high state, positive-going noise will not cause a false condition on the output. However, negative-going noise will drive the output low and cause inputs of following gates to propagate a false condition. The lower impedance of the active pullup requires more energy to drive the output down through the threshold voltage. Therefore, the active pullup has a superior noise immunity when compared to the passive pullup. Figure 5 shows a comparison of active and passive pullups over temperature.

FIGURE 5 – SIGNAL LINE NOISE IMMUNITY versus AMBIENT TEMPERATURE



An additional consideration of negative-going noise may be seen by returning to Figure 4. Both configurations show a reverse biased diode to ground. The illustrated diode is the reverse biased junction that isolates Q1 from the rest of the monolithic circuit. If an output is driven below ground sufficiently, the diode becomes forward biased and conducts, showing a low impedance path to ground. Under this condition the output is clamped to −0.7 Vdc.

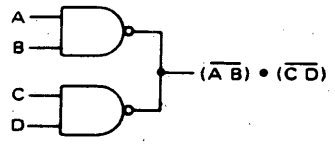
GENERAL DESIGN CONSIDERATIONS

Wired-Collector AND

The outputs of passive pullup gates may be tied together to perform the wired-collector AND function. For each additional output tied to the original output, a factor of 1.2 must be subtracted from the output loading factor.

Active outputs may not be tied together. If two active pullups are wired together and one output goes low, too much current will be pulled through the output configuration causing loss of noise immunity or possibly causing a catastrophic failure of one of the outputs.

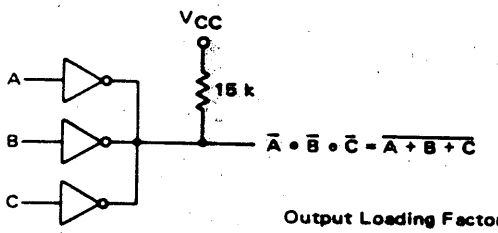
FIGURE 6 – MC668 PASSIVE PULLUP GATES WITH OUTPUTS AS WIRED-COLLECTOR "AND"



Output Loading Factor:
10 -1.2 = 8.8

Some gates are provided with open collector outputs. These outputs may also be tied together; however, an external pullup resistor should be provided for best noise immunity. The minimum resistor size is determined by the I_{OL} that one output is tested to sink at V_{OL}. The I_{OL} will be the sum of the current from the external pullup resistor and the current from the inputs driven from the wired collector AND. In terms of loading factor, a 15-kilohm resistor corresponds to a loading factor of 1.

FIGURE 7 – MC681 USED IN WIRED-COLLECTOR "AND" CONFIGURATION

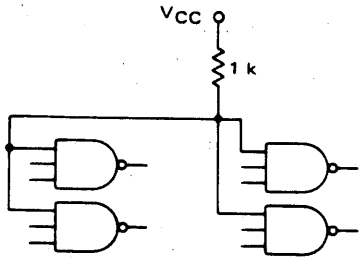


Output Loading Factor:
10 -1 = 9

Unused Inputs

For best noise immunity unused inputs should be tied to the power supply. If the power supply is subject to large voltage transients, the unused inputs should use a limiting resistor to protect the inputs from catastrophic breakdown. Any number of inputs may be tied to one resistor.

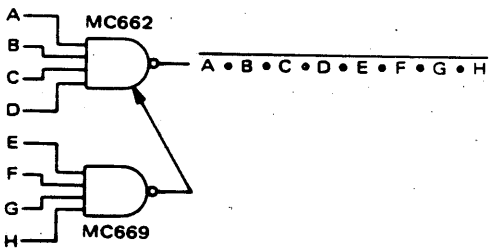
FIGURE 8 – UNUSED INPUTS WITH LIMITING RESISTOR



Fan-In

Fan-in may be increased through the use of the MC669 dual 4-input expander. Fan-in may be increased to a maximum of 20 using the MC669.

FIGURE 9 – MC662 EXPANDED TO 8 INPUTS



Rise and Fall Times

Slow rise and fall times on signal lines may allow oscillation to appear as the signal goes through the threshold level. Oscillation may be caused by noise or feed-back in the system, and if oscillation occurs through the threshold region false clocking of flip-flops may occur.

If slow rise and fall times are a problem, a Schmitt trigger as shown in Figure 10 is useful. The feed-back in the circuit causes a hysteresis action and sharpens rise and fall times.

Power Supply Variations

MHTL devices are tested to ensure proper operation with full fan-out capability over the -30°C to +75°C temperature range and with supply voltages between 14 and 16 volts. Normally the devices will provide proper operation if the voltage varies from the specified range, but they are not tested for this operation. When the 16-volt limit is exceeded, devices may exhibit a higher leakage current on the off transistors, although typical units will endure 20 volts collector supply before this becomes evident.

A disadvantage to using higher power supply values is the increased power dissipation of the circuits. To keep junction temperatures within acceptable limits on some devices, the ambient temperature limits must be reduced. Therefore, it is not advisable to exceed the 16-volt supply rating unless internal power dissipation is within safe limits (see maximum ratings).

FIGURE 10 – ACTIVE PULLUP INVERTERS (MC680) IN SCHMITT TRIGGER CONNECTION

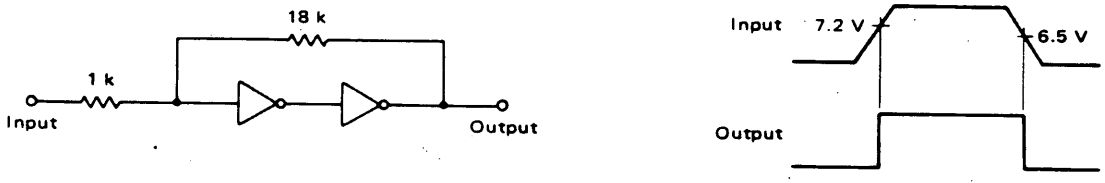


FIGURE 11 – TYPICAL VARIATION IN V_{OL} WITH TEMPERATURE

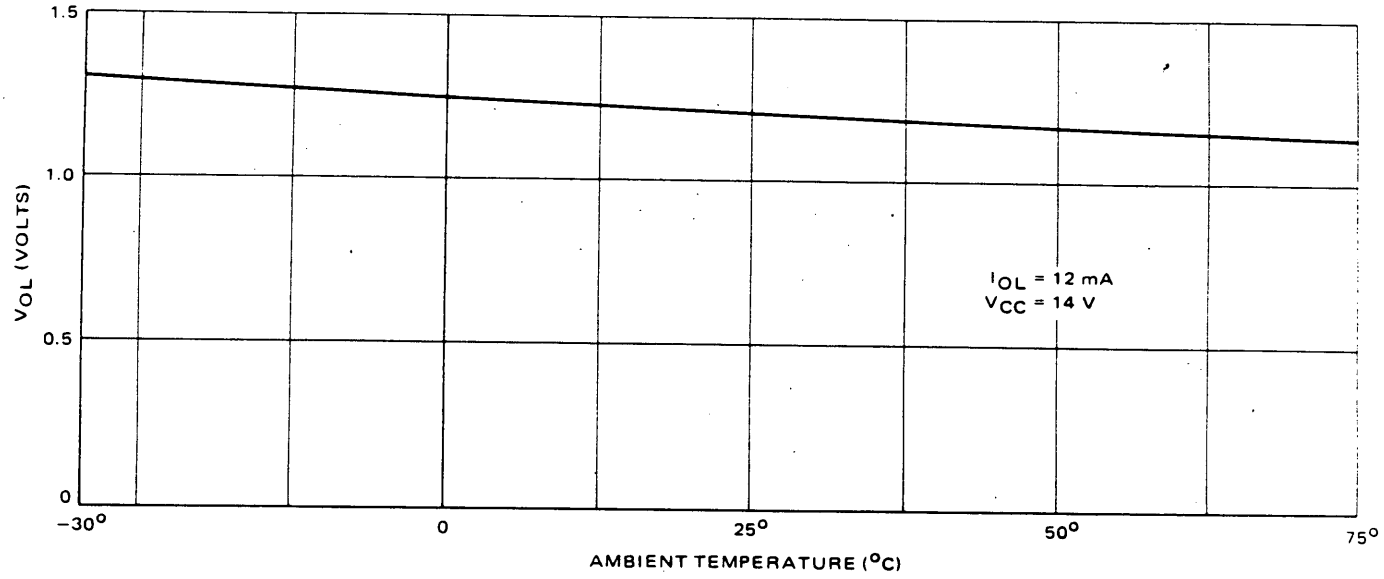
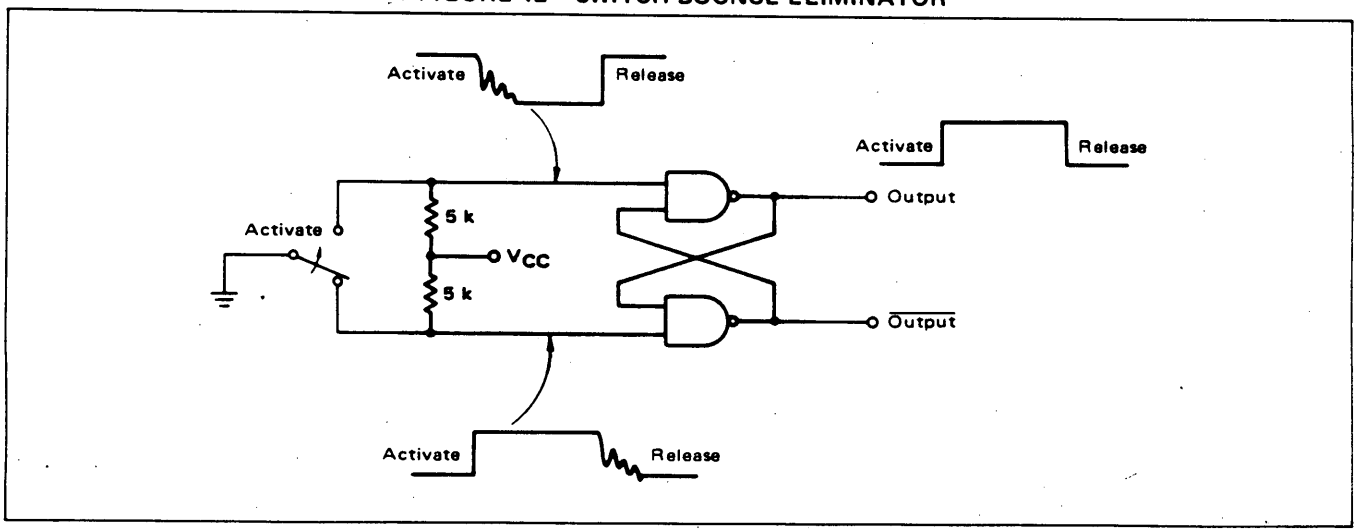


FIGURE 12 – SWITCH BOUNCE ELIMINATOR



When a V_{CC} below 14 volts is used, the base drive to the output transistor is reduced and is not capable of handling the rated fan-out. Figure 11 illustrates the V_{OL} values of typical units as a function of temperature with a V_{CC} of 14 volts and an I_{OL} of 12 mA. The devices are not tested to operate below 14 volts, so operation of the devices at these levels cannot be guaranteed. A second disadvantage of operating the units at a lower V_{CC} voltage is the reduction of the noise margin in the high state. Figure 3 shows that V_{OH} decreases while the device threshold remains constant.

Contact Bounce

In high noise environments, MHTL is extensively interfaced with relay contacts and switches. Contact bounce becomes a major consideration because of its duration and ability to cause oscillation. A contact bounce elimination circuit as in Figure 12 is useful in solving the problem. The circuit eliminates the effects of contact bounce and gives sharp rise and fall times.

FIGURE 13 – PASSIVE PULLUP OUTPUT DRIVING A DISCRETE DEVICE

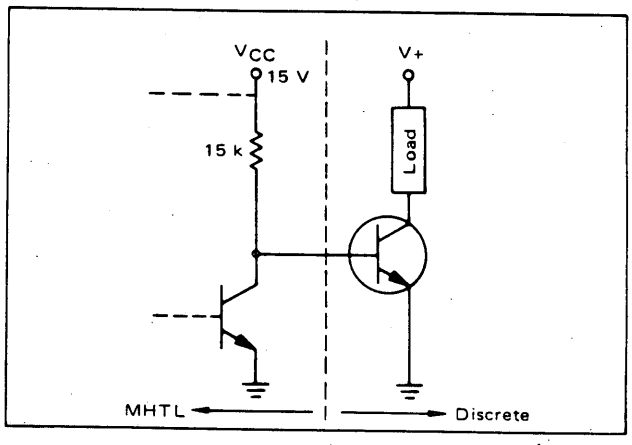
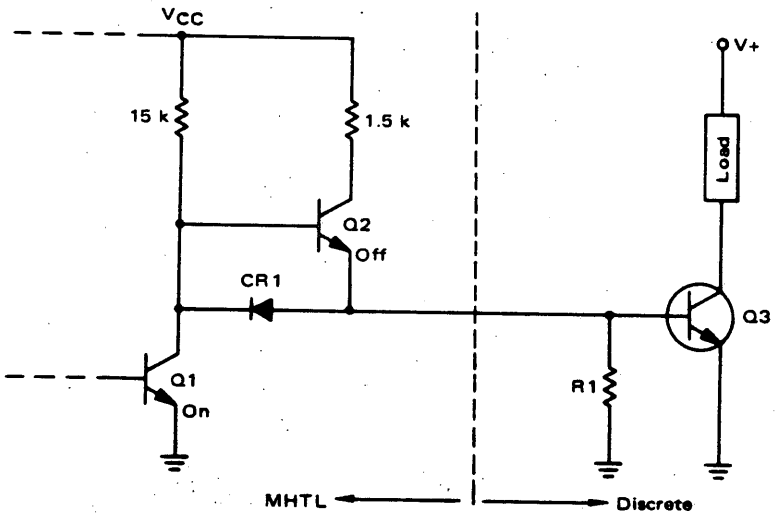


FIGURE 14 – ACTIVE PULLUP OUTPUT DRIVING A DISCRETE DEVICE



Driving Discrete Devices

With a large output voltage swing and good drive capability, MHTL is easily interfaced with discrete devices. Discrete transistor can be driven by MHTL with passive pullup output (Figure 13) or active pullup output (Figure 14).

Resistor R1 in Figure 14 is necessary to reduce leakage currents of Q3 when the MHTL output is low. Select R1 so that $^{1}C_{B}R1 < 0.5$ Vdc.

Note that the active pullup output of Figure 14 is not capable of driving a discrete transistor and a MHTL input simultaneously. The MHTL input would source current to the base of Q3, preventing Q3 from turning off. This would also clamp the MHTL input at 0.7 Vdc.

Temperature Variation

MHTL devices are rated for use from -30°C to +75°C. Normally devices will function properly beyond these limits although not necessarily meeting the specifications set for the rated temperature range. If devices are operated at increased temperature, the significant changes are increased saturation voltages, increased transistor beta, and greater leakage current. Therefore, noise margins are decreased and rise times are increased.

Operation at lower temperatures causes lower transistor beta and higher saturation voltages. The significant change then is higher V_{OL} levels.

MHTL

GENERAL INFORMATION

MC660 Series

MAXIMUM RATINGS
$T_A = 25^oC$

Rating	Symbol	Value	Unit
Power Supply Voltage Continuous Pulsed, 1.0 s	V_{CC}	 18 20	Vdc
Input Voltage MC666 DTL RTL All Others	V_{in}	 −1.0 to +6.0 −4.0 to +4.0 −1.0 to +18	Vdc
Output Current (into outputs) MC662 MC663 MC664 MC669 All Others	–	 60 28 26 – 30	mAdc
Input Reverse Current @ 18 V	I_R	0.5	mAdc
Forward Current (individual) MC669	I_F	30	mAdc
Power Dissipation and Thermal Characteristics Dual-In-Line Ceramic Package Maximum Junction Temperature Maximum Internal Dissipation @ $T_A = 25^oC$ *Thermal Resistance, Junction to Air *Thermal Resistance, Junction to Case Dual-In-Line Plastic Package Maximum Junction Temperature Maximum Internal Dissipation @ $T_A = 25^oC$ *Thermal Resistance, Junction to Air *Thermal Resistance, Junction to Case	 T_J P_D θ_{JA} θ_{JC} T_J P_D θ_{JA} θ_{JC}	 175 1000 0.15 0.09 150 625 0.20 0.15	 °C mW °C/mW °C/mW °C mW mW/°C mW/°C
Operating Temperature Range	T_A	−30 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

*Note: Thermal Resistance values are specified with the device mounted in a socket in still air.

TEST LIMITS TOLERANCE

$T_A = \pm 3^oC$ $V_R = \pm 1\%$ $V_{CC} = \pm 1\%$ $V_{IL} = \pm 1\%$ $V_{IH} = \pm 1\%$ $V_F = \pm 1\%$ $I_{OL} = \pm 1\%$ $I_{OH} = \pm 1\%$

DEFINITIONS

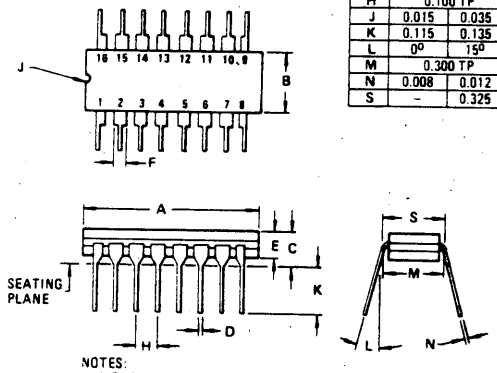
CP	Clock Pulse
I_{CEX}	Collector-to-emitter leakage of the output transistor
I_{CCH}	V_{CC} current drain when all inputs are high
I_{CCL}	V_{CC} current drain when all inputs are low
I_F	Forward current of input diodes for unit input load
2_{IF}	Forward current of input diodes which are equal to twice unit load
I_{OH}	Test current flowing into the output pin when output is high. (Negative)
I_{OL}	Test current flowing into output pin when output is low
I_R	Reverse current of input diodes with V_R applied
2_{IR}	Reverse current of two input diodes with V_R applied
I_{SC}	Short-circuit current obtained from device output when output is high
t_{pd+}	Propagation delay time for a positive-going output pulse
t_{pd-}	Propagation delay time for a negative-going output pulse
V_{CC}	Device power supply voltage
V_{CCH}	High power supply voltage
V_{CCL}	Low power supply voltage
V_{CEX}	Collector-to-emitter voltage of the output transistor
V_F	Input voltage when measuring I_F
V_{IH}	Threshold voltage for high input voltage state
V_{IL}	Threshold voltage for low input voltage state
V_{OH}	Output high voltage state with I_{OH} flowing out of pin
V_{OL}	Output low voltage state with I_{OL} flowing into pin
V_R	Reverse voltage for input diode leakage test
V_X	Threshold voltage for low input voltage state on expander unit

PACKAGING

All MHTL integrated circuits are available in a dual in-line ceramic package (add suffix L to type number when ordering) and in a dual in-line plastic package (suffix P).

L SUFFIX
CERAMIC PACKAGE
CASE 620

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.740	0.780	18.790	19.810
B	0.240	0.275	6.100	6.990
C	0.170	0.200	4.320	5.080
D	0.015	0.020	0.381	0.508
E	0.135	0.165	3.430	4.190
F	0.055	0.065	1.400	1.650
H	0.100 TP		2.54 TP	
J	0.015	0.035	0.381	0.889
K	0.115	0.135	2.930	3.430
L	0°	15°	0°	15°
M	0.300 TP		7.620 TP	
N	0.008	0.012	0.203	0.305
S	–	0.325	–	8.260



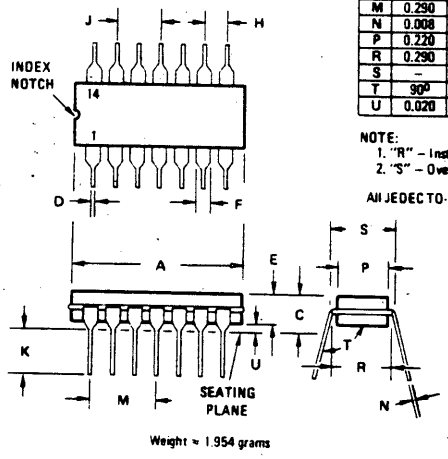
NOTES:
1. DIM. "M" IS MEASURED AT CENTER OF LEADS WHEN FORMED PARALLEL.
2. "J" INDEX:
NOTCH IN LEAD, INK DOT, OR NOTCH IN CERAMIC.

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.660	0.780	17.400	19.900
C	–	0.200	–	5.080
D	0.015	0.023	0.381	0.584
F	0.030	0.070	0.770	1.770
H	0.090	0.110	2.290	2.790
J	0.190	0.210	4.830	5.330
K	0.100	–	2.540	–
M	0.290	0.310	7.370	7.870
N	0.008	0.015	0.203	0.381
P	0.220	0.280	5.580	7.110
R	0.290	0.310	7.370	7.870
S	–	0.325	–	8.260
T	90°	105°		
U	0.020	0.030	0.508	0.762

NOTE:
1. "R" – Installed Position of Lead Centers.
2. "S" – Overall Installed Width.

All JEDEC TO-116 dimensions and notes apply.

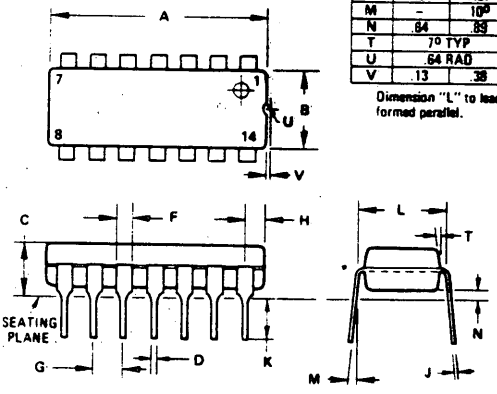


Weight ≈ 1.954 grams

P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.03	18.79	.710	.740
B	6.09	6.60	.240	.260
C	4.06	4.57	.160	.180
D	.38	.51	.015	.020
F	1.02	1.65	.040	.065
G	2.54 BSC		.100 BSC	
H	1.32	1.83	.052	.072
J	.23	.38	.009	.014
K	2.92	3.43	.115	.135
L	7.37	7.87	.290	.310
M	–	10°	–	10°
N	.64	.89	.025	.035
T	7° TYP		7° TYP	
U	.64 RAD		.025 RAD	
V	.13	.38	.005	.015

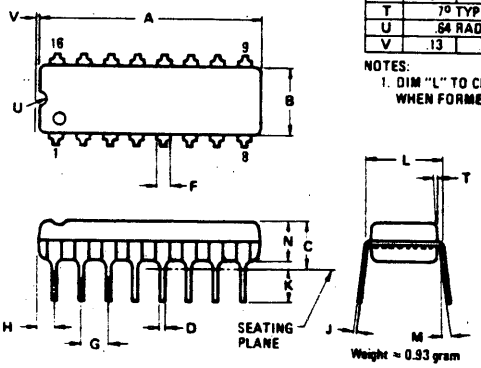
Dimension "L" to lead centerline when formed parallel.



P SUFFIX
PLASTIC PACKAGE
CASE 648

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.21	.815	.835
B	6.09	6.60	.240	.260
C	4.07	4.57	.160	.180
D	.38	.51	.015	.020
F	1.14	1.40	.045	.055
G	2.54 BSC		.100 BSC	
H	1.32	1.83	.052	.072
J	.20	.30	.008	.012
K	2.92	3.43	.115	.135
L	7.37	7.87	.290	.310
M	–	10°	–	10°
N	.64	.89	.025	.035
T	7° TYP		7° TYP	
U	.64 RAD		.025 RAD	
V	.13	.38	.005	.015

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

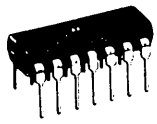


Weight ≈ 0.93 gram

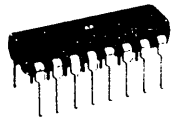
MHTL INTEGRATED CIRCUITS FROM MOTOROLA MHTL

*MC660 Series (-30 to +75°C)

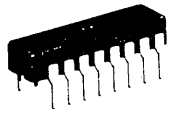
ISSUE B



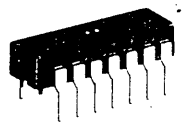
P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

Motorola's MHTL integrated circuits are especially designed to meet the requirements of industrial applications because of the outstanding noise immunity. MHTL circuits provide error-free operation in high noise environments far beyond the tolerance of other integrated circuit families. Multifunction packages and broad operating temperature range further tailor this device family to the industrial designer's requirements.

*MHTL cermaic dual in-line devices are available with specification over the -55°C to +125°C temperature range and/or with hi-rel processing on special order. See your Motorola representative for pricing.

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 15 V ± 1.0 Vdc, T_A = 25°C)

Function	Type ① -30 to +75°C	Loading Factor Each Output	Propagation Delay ns typ	Power Dissipation mW typ/pkg	Case
Expandable Dual 4-Input Gate (active pullup)	MC660	10	110	88/26 ②	632, 646
Expandable Dual 4-Input Gate (passive pullup)	MC661	10	125	88/26 ②	632, 646
Expandable Dual 4-Input Line Driver	MC662	30	140	180/26 ②	632, 646
Dual J-K Flip-Flop	MC663	9	3.0 MHz ③	200	632, 646
Master-Slave R-S Flip-Flop	MC664	6	3.0 MHz ③	160	632, 646
Triple Level Translator	MC665	MDTL = 8 MTTL III = 5.5 MRTL = 5	40	83 (MDTL) 104 (MRTL)	632, 646
Triple Level Translator	MC666	10	75	105	632, 646
Dual Monostable Multivibrator	MC667	10	140	240	632, 646
Quad 2-Input Gate (passive pullup)	MC668	10	128	176/52 ②	632, 646
Dual 4-Input Expander	MC669	–	–	–	632, 646
Triple 3-Input Gate (passive pullup)	MC670	10	125	132/39 ②	632, 646
Triple 3-Input Gate (active pullup)	MC671	10	110	132/39 ②	632, 646
Quad 2-Input Gate (active pullup)	MC672	10	110	176/52 ②	632, 646
Dual 2-Input AND-OR-INVERT Gate	MC673	10	110	160/50 ②	632, 646
Dual 2-Input AND-OR-INVERT Gate	MC674	10	125	160/50 ②	632, 646
Dual Pulse Stretcher	MC675	10	150 (pins 1,6) 110 (pins 5,6)	180	632, 646
BCD-To-Decimal Decoder-Driver	MC676	–	–	380	620, 648
Hex Inverter With Strobe (active pullup)	MC677	10	110	246/96 ②	620, 648
Hex Inverter With Strobe (without output resistors)	MC678	10	125	192/96 ②	620, 648
Dual Lamp Driver	MC679,8	125	0.5 μs typ	250/30 ②	632, 646
Hex Inverter	MC680	10	110	246/96 ②	632, 646
Hex Inverter (open collector)	MC681	10	125	192/96 ②	632, 646
Quad Latch	MC682	10	250	375	620, 648
Quad 2-Input Exclusive OR	MC683	10	–	380	632, 646
• Decade Counter	MC684	10	0.5 MHz ③	480	620,648
• Binary Counter	MC685	10	0.5 MHz ③	480	620,648
• 4-Bit Shift Register	MC686	10	0.5 MHz ③	480	620,648
• Dual J-K Flip-Flop	MC688	10	2.5 MHz ③	375	620,648
• Hex Inverter (high voltage)	MC689	10	150	173/55 ②	632,646
• Hex Inverter (active pullup)	MC690	10	150	173/55 ②	632,646

① L suffix denotes Dual In-Line Ceramic Package, P denotes Dual In-Line Plastic Package (i.e., MC660L = Dual In-Line Ceramic, MC660P = Dual In-Line Plastic Package).

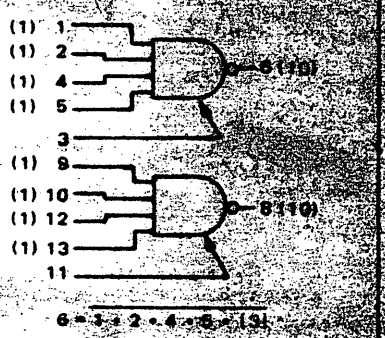
② Inputs High/Input Low ③ f_{Tog}

• New Devices

MOTOROLA Semiconductor Products Inc.

GATES

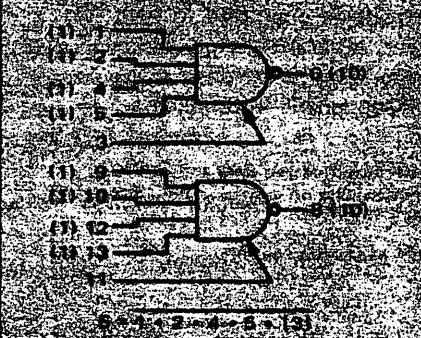
MC669
Expandable
Dual 4-Input NAND Gate
(active output pullup)



$6 = \overline{3 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

t_{pd} = 110 ns typ
P_D = 88 mW typ/pkg (Inputs High)
26 mW typ/pkg (Input Low)

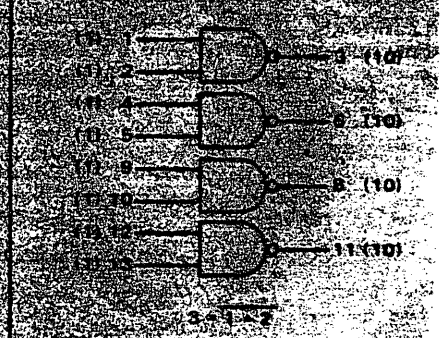
MC667
Expandable
Dual 4-Input NAND Gate
(passive output pullup)



$6 = \overline{3 \cdot 2 \cdot 4 \cdot 5 \cdot (3)}$

t_{pd} = 125 ns typ
P_D = 88 mW typ/pkg (Inputs High)
26 mW typ/pkg (Input Low)

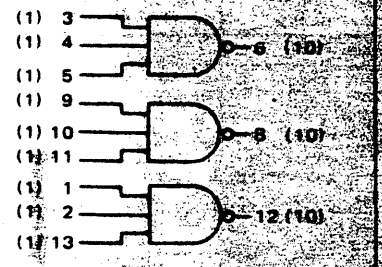
MC668
Dual 2-Input NAND Gate
(passive output pullup)



$3 = \overline{1 \cdot 2}$

t_{pd} = 125 ns typ
P_D = 176 mW typ/pkg (Inputs High)
52 mW typ/pkg (Input Low)

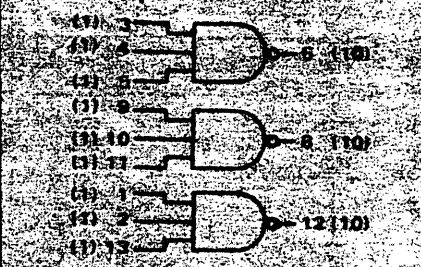
MC670
Triple 3-Input NAND Gate
(passive output pullup)



$6 = \overline{3 \cdot 4 \cdot 5}$

t_{pd} = 125 ns typ
P_D = 132 mW typ/pkg (Inputs High)
39 mW typ/pkg (Input Low)

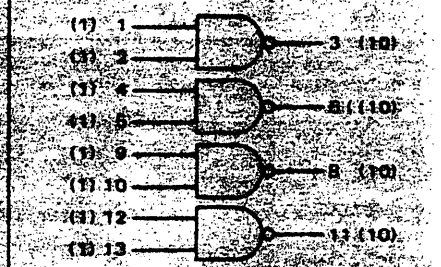
MC671
Triple 3-Input NAND Gate
(active output pullup)



$6 = \overline{3 \cdot 4 \cdot 5}$

t_{pd} = 110 ns typ
P_D = 132 mW typ/pkg (Inputs High)
39 mW typ/pkg (Input Low)

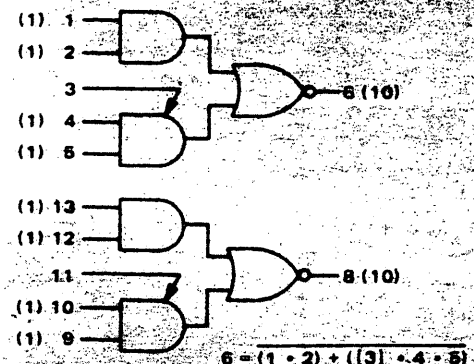
MC672
Quad 2-Input NAND Gate
(active output pullup)



$3 = \overline{1 \cdot 2}$

t_{pd} = 110 ns typ
P_D = 176 mW typ/pkg (Inputs High)
52 mW typ/pkg (Input Low)

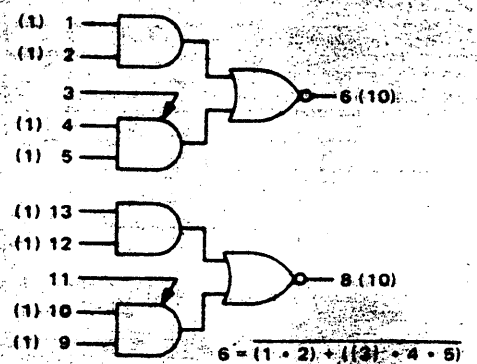
MC673
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate
(active output pullup)



$6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$

t_{pd} = 110 ns typ
P_D = 160 mW typ/pkg (Inputs High)
50 mW typ/pkg (Input Low)

MC674
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate
(passive output pullup)



$6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$

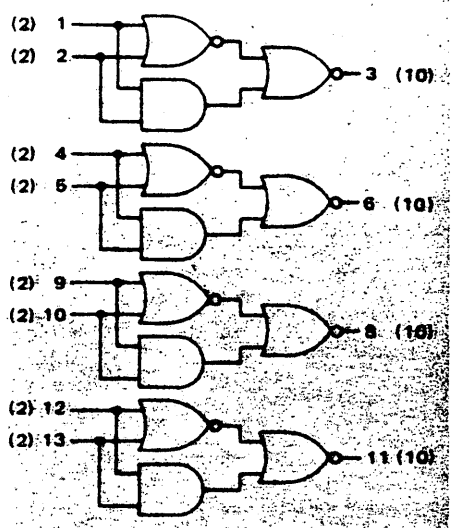
t_{pd} = 125 ns typ
P_D = 160 mW typ/pkg (Inputs High)
50 mW typ/pkg (Input Low)

(continued)

Numbers at ends of terminals represent pin numbers.
Numbers in parenthesis indicate loading.
(V_{CC} = Pin 14, Gnd = Pin 7 for Case 646 and 632; V_{CC} = Pin 16, Gnd = Pin 8 for Case 648 and 620.)

GATES (continued)

MC683
Quad 2-Input Exclusive OR

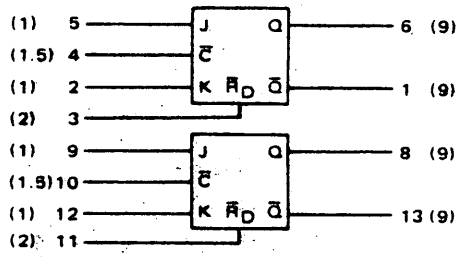


$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

P_D = 380 mW typ/pkg

FLIP-FLOPS

MC863
Dual J-K Flip-Flop



f_{Tog} = 3.0 MHz typ
P_D = 200 mW typ/pkg

TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\overline{Q}$
0	0	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\overline{Q}_n$	Q_n

Direct input ($\overline{R}_D$) must be high.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

NOTE: A low state "0" at the direct reset $\overline{R}_D$ causes a low state "0" at the Q output and the complement at the $\overline{Q}$ output.

MC864
Master-Slave R-S Flip-Flop

f_{Tog} = 3.0 MHz typ
P_D = 180 mW typ/pkg

DIRECT INPUT OPERATION

$\overline{R}_D$	$\overline{S}_D$	Q	$\overline{Q}$
0	0	NC	NC
0	1	1	0
1	0	0	1
1	1	NA	NA

Clock inputs must be low.
0 = low state
1 = high state
NC = No change
NA = Not allowed
X = state of input does not affect state of the circuit
U = Indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

CLOCKED OPERATION

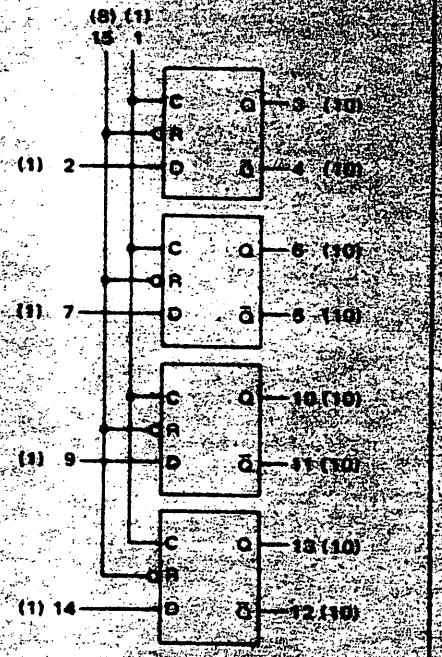
t_n				t_{n+1}
S_n	S_n	R_n	R_n	Q
0	X	0	X	Q_n
0	1	X	0	Q_n
X	0	0	X	Q_n
X	0	1	0	0
0	1	1	1	0
X	0	1	1	0
1	X	0	X	1
1	1	1	0	1
1	1	1	1	U

Direct inputs ($\overline{R}_D$, $\overline{S}_D$) must be high.

(continued)

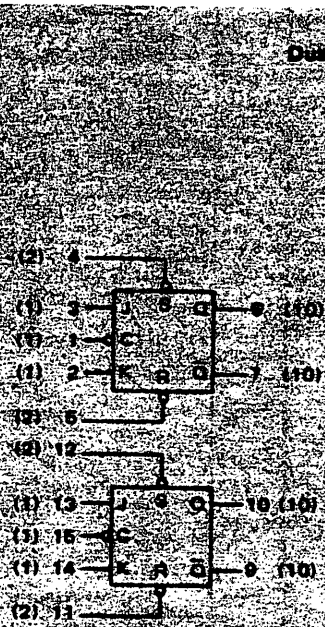
FLIP-FLOPS (continued)

MC882
Quad Latch



t_{pd} = 250 ns typ
P_D = 375 mW typ/pkg

MC888
Dual J-K Flip-Flop



f_{tog} = 2.5 MHz typ
P_D = 375 mW typ/pkg

TRUTH TABLE

t_n				t_{n+1}	
R	S	J	K	Q	Q
0	1	×	×	0	1
1	0	×	×	1	0
1	1	0	0	Q_n	$\overline{Q}_n$
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	$\overline{Q}_n$	Q_n

0 = Low state
1 = High state
× = Don't care
t_n = Time period prior to negative transition of clock pulse.
t_{n+1} = Time period subsequent to negative transition of clock pulse.
Q_n = State of Q output in time period t_n.
* = Clock pulse must be in low state

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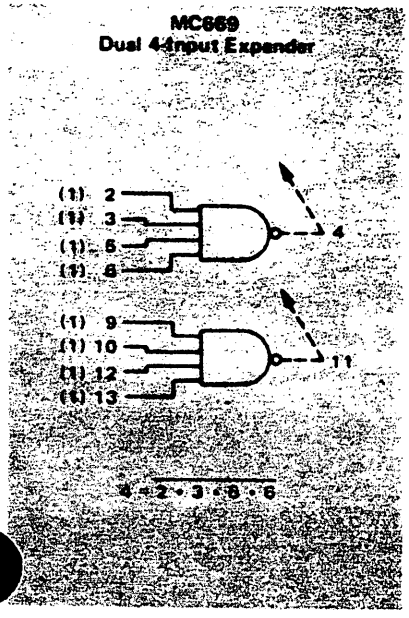
EXPANDER

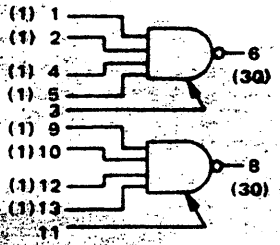
MC869
Dual 4-Input Expander



$6 = \overline{2 \cdot 3 \cdot 8 \cdot 6}$

DRIVERS

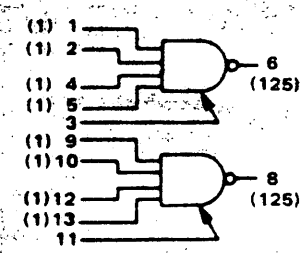
MC662
Expandable
Dual 4-Input Line Driver
(active output pullup)



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

t_{pd} = 140 ns typ
P_D = 180 mW typ/pkg (Inputs High)
20 mW typ/pkg (Input Low)

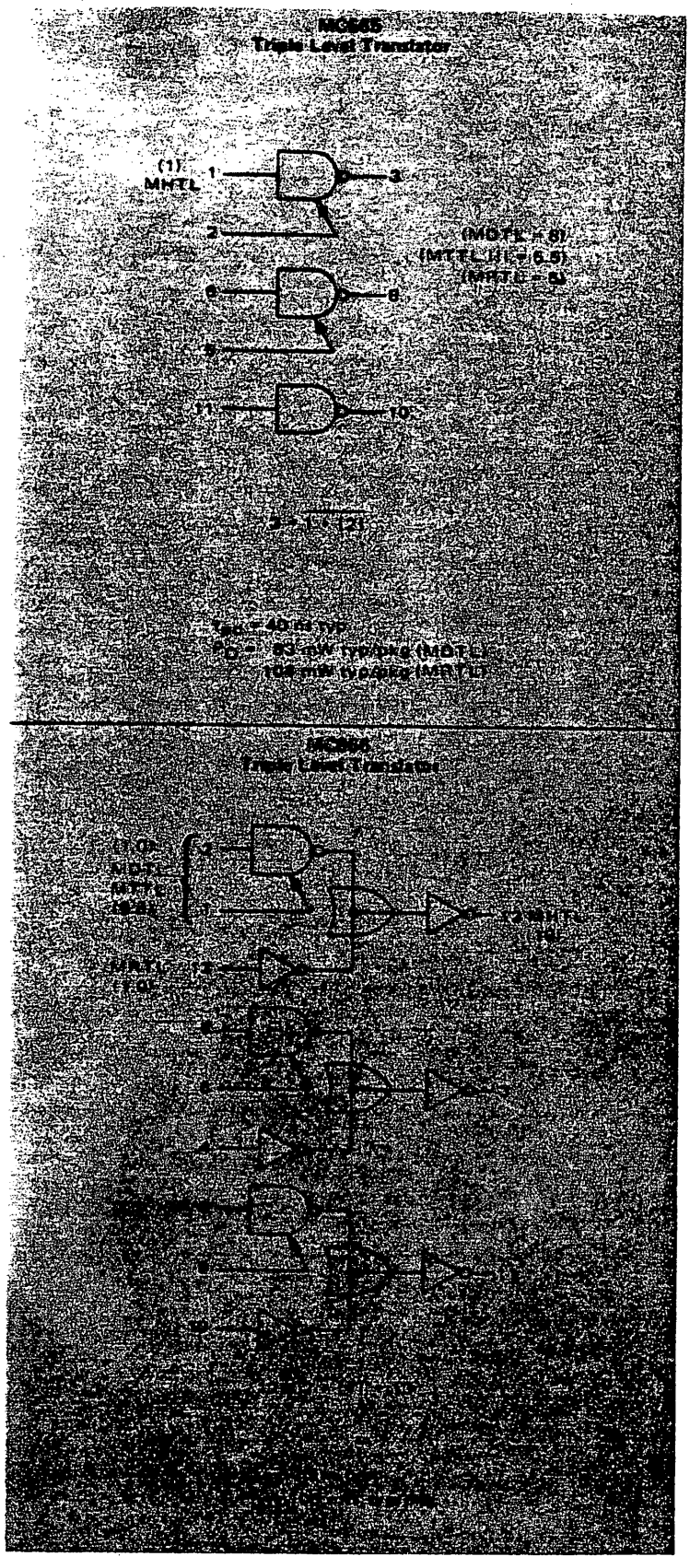
MC679, MC679B
Dual Lamp Driver



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

t_{pd} = 0.6 µs typ
P_D = 250 mW (Inputs High)
20 mW (Input Low)

TRANSLATORS



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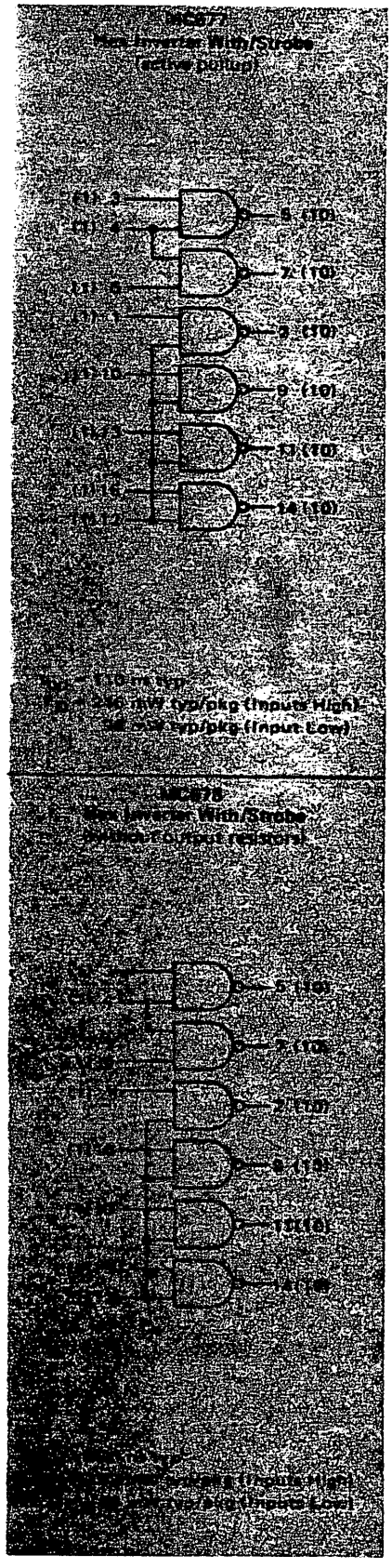
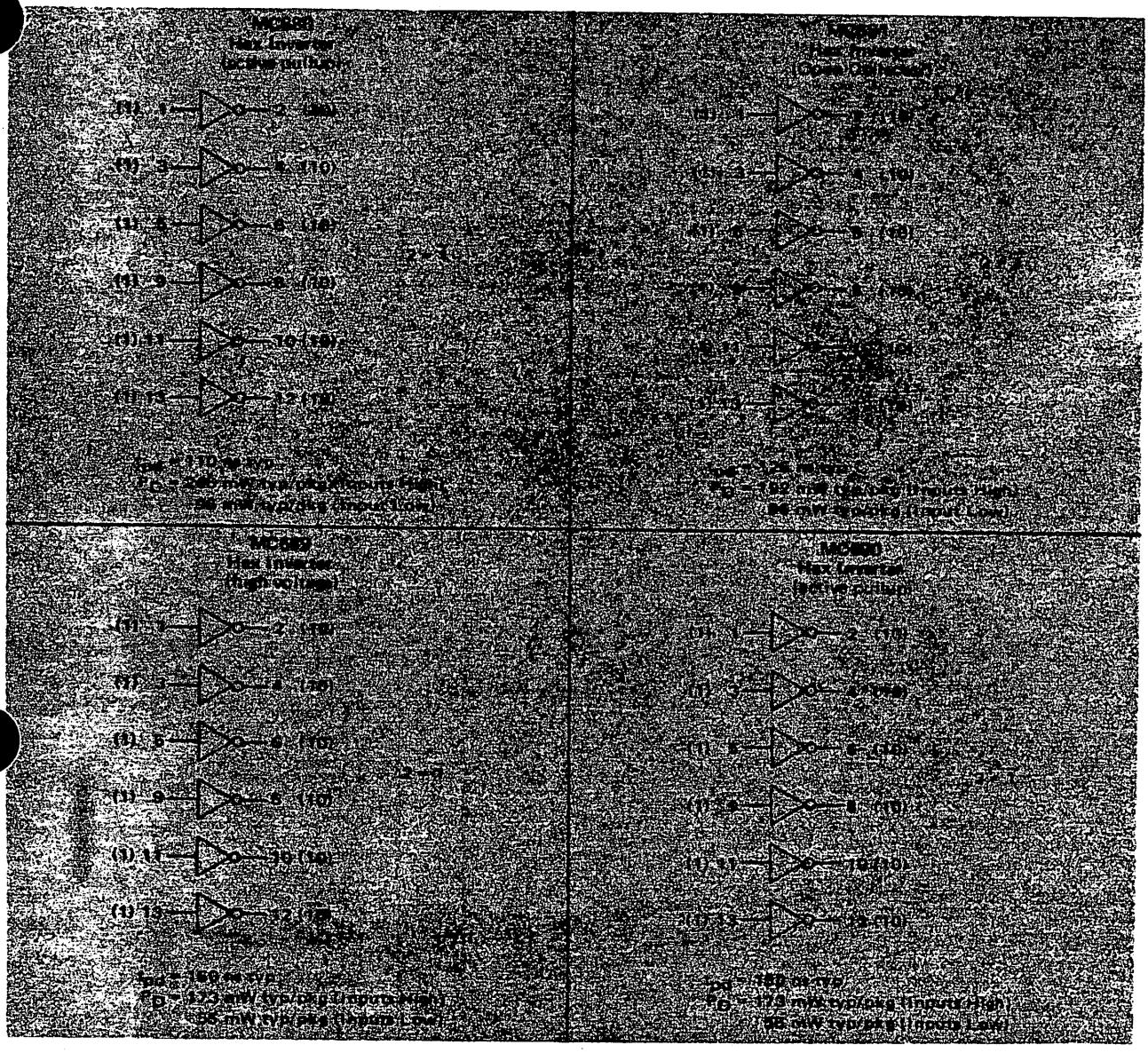
INVERTERS



(continued)

MHTL LOGIC DIAGRAMS

INVERTERS (continued)



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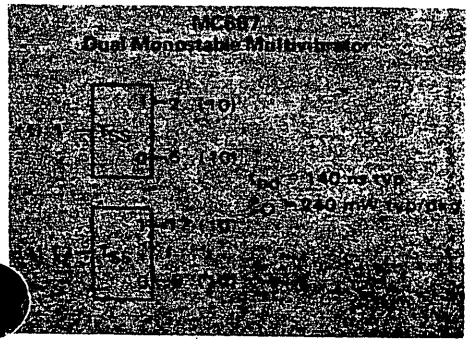
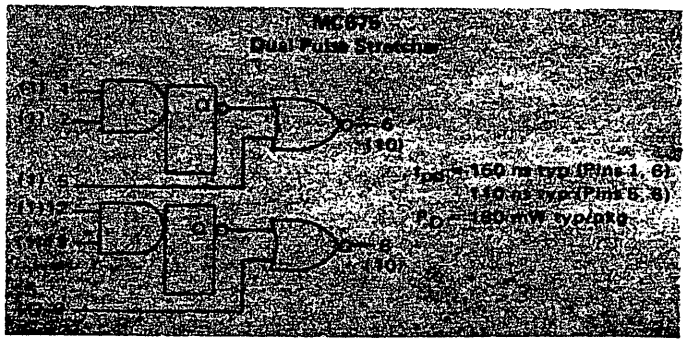
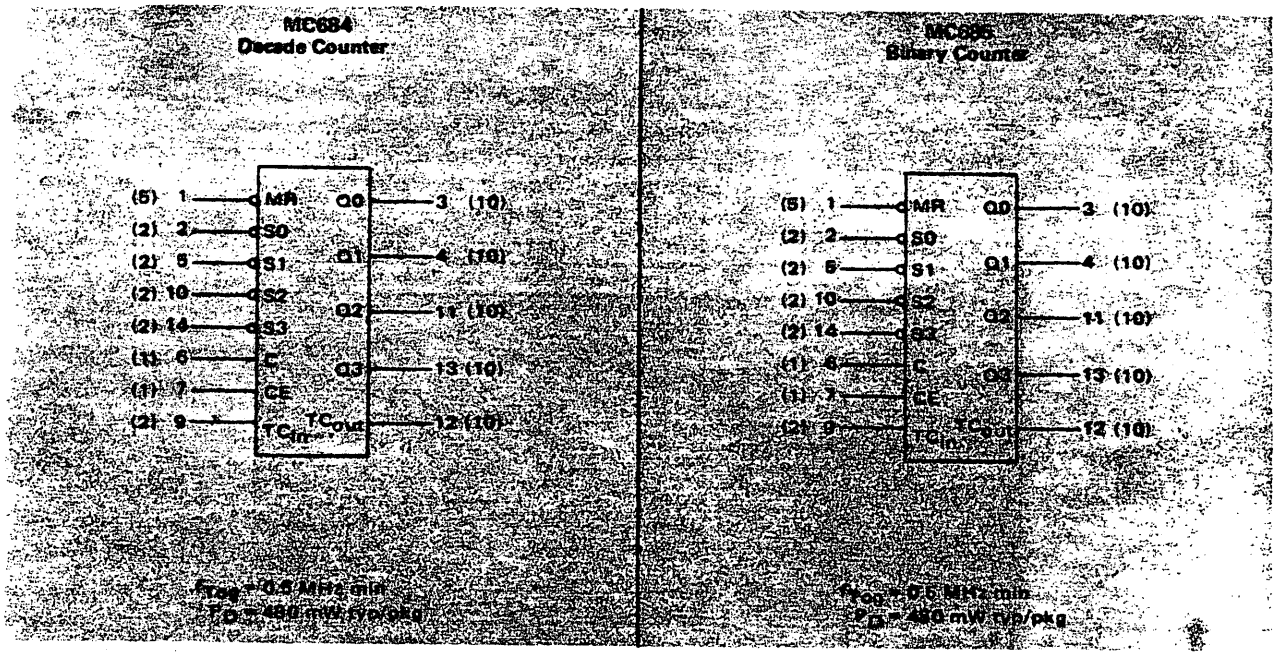
MULTIVIBRATOR



PULSE STRETCHER



COUNTERS



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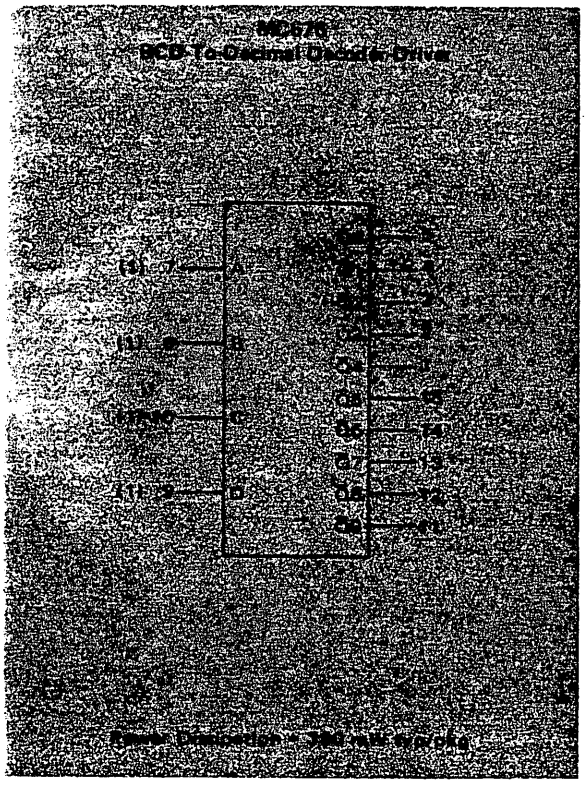
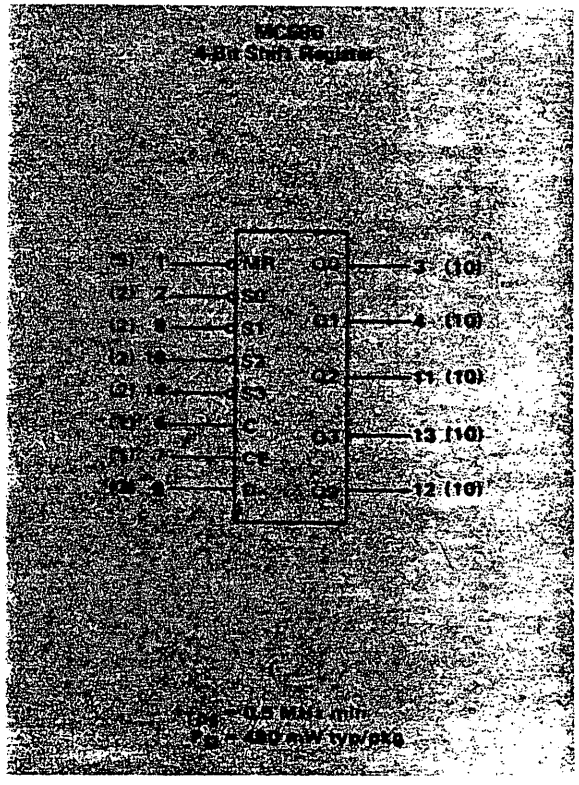
DECODER



SHIFT REGISTER



MHTL LOGIC DIAGRAMS

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage Continuous Pulsed, 1.0 s	V_{CC}	+18 20	Vdc
Input Voltage MC655, MDTL MRTL All Others	V_{in}	-1.0 to +6.0 -4.0 to +6.0 -1.0 to +18	Vdc
Output Current (Into Ground) MC662 MC663 MC664 MC665 All Others		60 75 25 30	mAdc
Input Reverse Current @ 18 V	I_R	0.5	mAdc
Forward Current (Individual) MC665P	I_F	50	mAdc
Operating Temperature Range	T_A	-30 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

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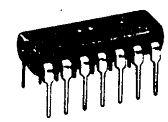
MHTL

INTEGRATED CIRCUITS FROM MOTOROLA

MHTL

*MC660 Series (-30 to +75°C)

ISSUE C



P SUFFIX
PLASTIC PACKAGE
CASE 646

Motorola's MHTL integrated circuits are especially designed to meet the requirements of industrial applications because of the outstanding noise immunity. MHTL circuits provide error-free operation in high noise environments far beyond the tolerance of other integrated circuit families. Multifunction packages and broad operating temperature range further tailor this device family to the industrial designer's requirements.

*MHTL cermaic dual in-line devices are available with specification over the -55°C to +125°C temperature range and/or with hi-rel processing on special order. See your Motorola representative for pricing.

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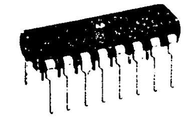
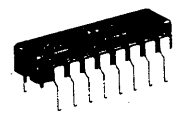
P SUFFIX
PLASTIC PACKAGE
CASE 648





L SUFFIX
CERAMIC PACKAGE
CASE 620

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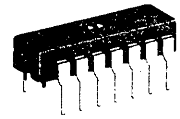
L SUFFIX
CERAMIC PACKAGE
CASE 632



FUNCTIONS AND CHARACTERISTICS (V_{CC} = 15 V ± 1.0 Vdc, T_A = 25°C)

Function	Type ① -30 to +75°C	Loading Factor Each Output	Propagation Delay ns typ	Power Dissipation mW typ/pkg	Case
Expandable Dual 4-Input Gate (active pullup)	[illegible]	[illegible]	[illegible]	55/26 ②	632,646
Expandable Dual 4-Input Gate (passive pullup)	[illegible]	[illegible]	[illegible]	55/26 ②	632,646
Expandable Dual 4-Input Line Driver	[illegible]	[illegible]	[illegible]	100/26 ②	632,646
Dual J-K Flip-Flop	[illegible]	[illegible]	[illegible]	200	632,646
Master Slave R-S Flip-Flop	[illegible]	[illegible]	[illegible]	100	632,646
[illegible] Level Translator	[illegible]	[illegible]	[illegible]	82 (MDTL) 104 (MRTL)	632,646
[illegible] Level Translator	[illegible]	[illegible]	[illegible]	105	632,646
Dual Monostable Multivibrator	[illegible]	[illegible]	[illegible]	240	632,646
Quad 2-Input Gate (passive pullup)	[illegible]	[illegible]	[illegible]	[illegible] ②	[illegible]
Dual 4-Input Expander	[illegible]	[illegible]	[illegible]	[illegible]	632,646
Triple 3-Input Gate (passive pullup)	[illegible]	[illegible]	[illegible]	[illegible] ②	632,646
Triple 3-Input Gate [illegible]	[illegible]	[illegible]	[illegible]	[illegible] ②	632,646
Quad 2-Input Gate [illegible]	[illegible]	[illegible]	[illegible]	[illegible] ②	632,646
Dual 2-Input AND-OR-INVERT [illegible]	[illegible]	[illegible]	[illegible]	[illegible] ②	632,646
Dual 2-Input AND-OR-INVERT [illegible]	[illegible]	[illegible]	[illegible]	[illegible] ②	632,646
Dual Pulse Stretcher	[illegible]	[illegible]	[illegible]	[illegible]	632,646
BCD To Decimal Decoder [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	620,648
Hex Inverter With [illegible]	[illegible]	[illegible]	[illegible]	240/[illegible] ②	620,648
Hex Inverter With [illegible]	[illegible]	[illegible]	[illegible]	[illegible] ②	620,648
Dual Lamp Driver	[illegible]	[illegible]	[illegible]	150/30 ②	632,646
Hex Inverter [illegible]	[illegible]	[illegible]	[illegible]	[illegible] ②	632,646
Hex Inverter [illegible]	[illegible]	[illegible]	[illegible]	[illegible] ②	[illegible]
Quad Latch	[illegible]	[illegible]	[illegible]	[illegible]	620,648
Quad 2-Input Exclusive OR [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	632,646
Decade Counter	[illegible]	[illegible]	[illegible]	450	620,648
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	620,648
[illegible]	[illegible]	[illegible]	[illegible]	270	620,648
[illegible]	[illegible]	[illegible]	[illegible]	[illegible] ②	632,646
[illegible]	[illegible]	[illegible]	[illegible]	[illegible] ②	632,646
• [illegible] Interface Element, Line Driver/[illegible]	[illegible]	[illegible]	[illegible]	225/60 ②	620,648

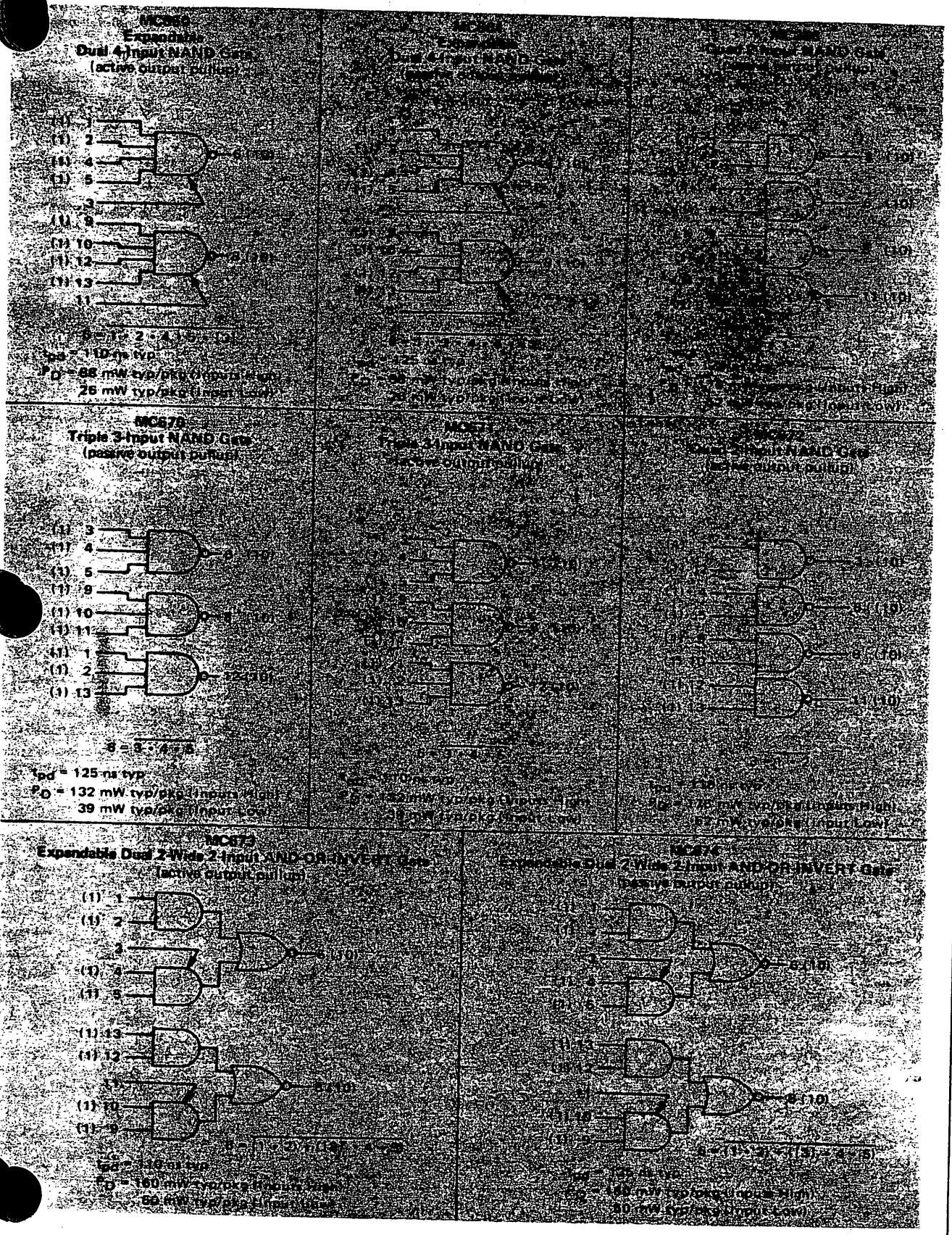
① L suffix denotes Dual In-Line Ceramic Package, P denotes Dual In-Line Plastic Package (i.e., MC660L = Dual In-Line Ceramic, MC660P = Dual In-Line Plastic Package)

② Inputs High/Input Low ③ f_{Tog}

• New Devices

MOTOROLA Semiconductor Products Inc.

GATES



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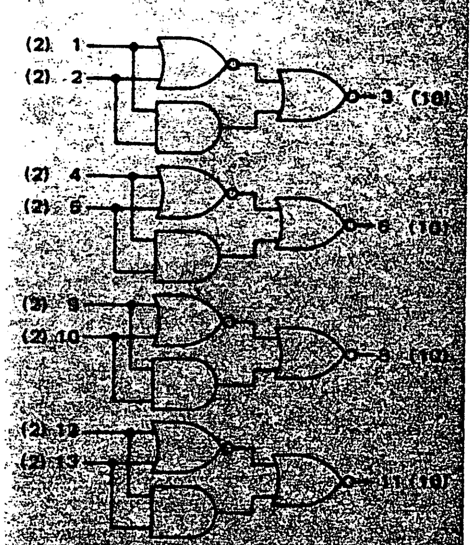
(continued)

Numbers at ends of terminals represent pin numbers.
Numbers in parenthesis indicate loading.
(V_{CC} = Pin 14, Gnd = Pin 7 for Case 646 and 632; V_{CC} = Pin 16, Gnd = Pin 8 for Case 648 and 620.)

GATES (continued)

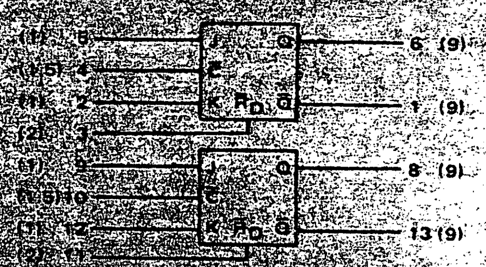
MC683
Quad 2-Input Exclusive OR



P_D = 390 mW typ/pkg

FLIP-FLOPS

MC663
Dual J-K Flip-Flop



f_{tog} = 3.0 MHz typ
P_D = 200 mW typ/pkg

TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\bar{Q}_n$	Q_n

[illegible]
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n
NOTE: A low state "0" at the direct reset R_D causes a low state "0" at the Q output and the complement at the $\bar{Q}$ output.

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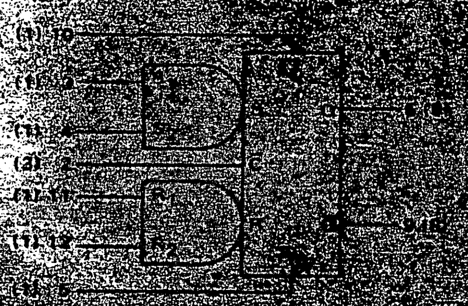
[illegible]
[illegible] R-S Flip-Flop



DIRECT INPUT OPERATION

[illegible]	[illegible]	[illegible]	[illegible]

CLOCKED OPERATION

[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

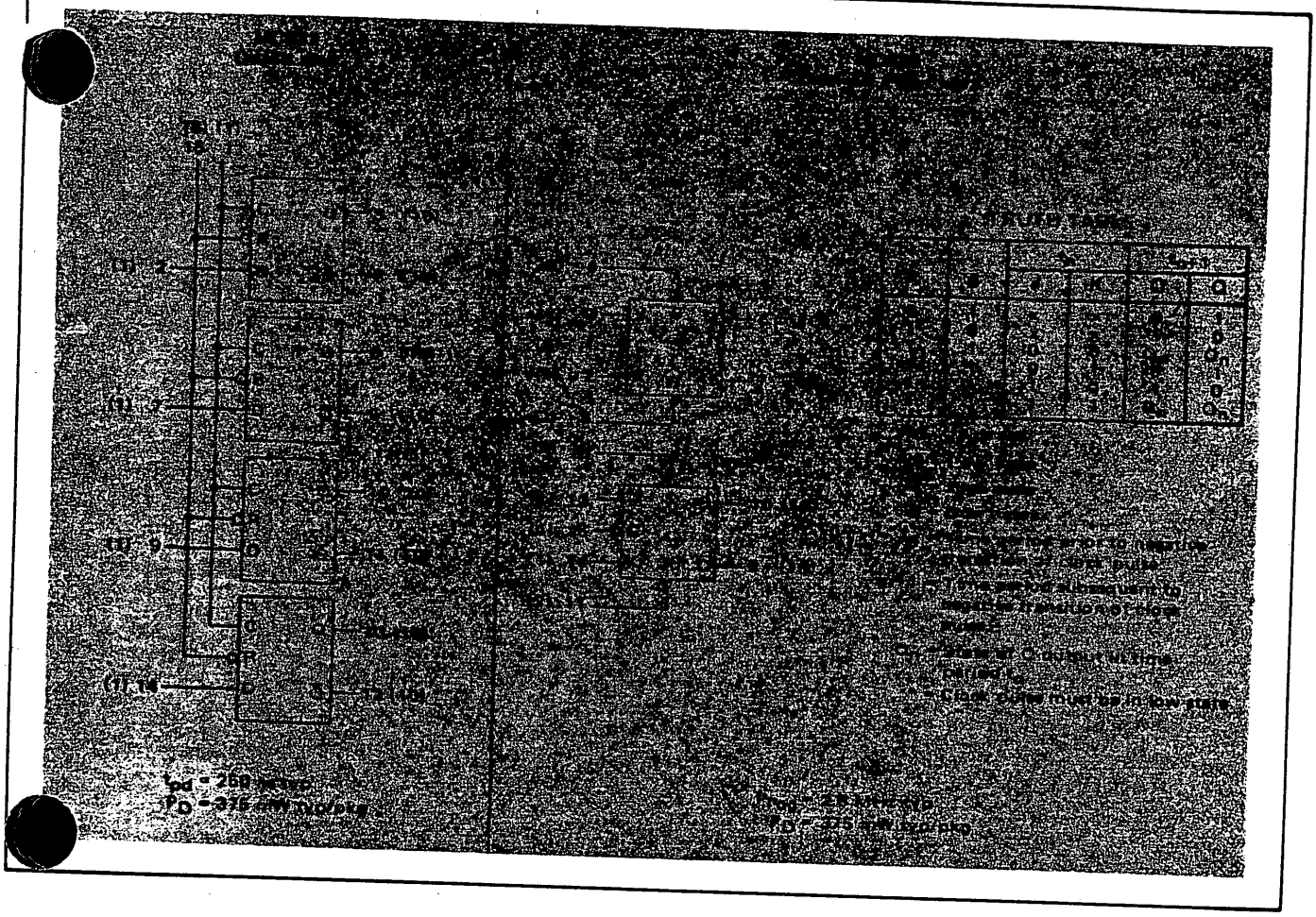
Direct Inputs (R_D, S_D) must be high.

[illegible]
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
[illegible]

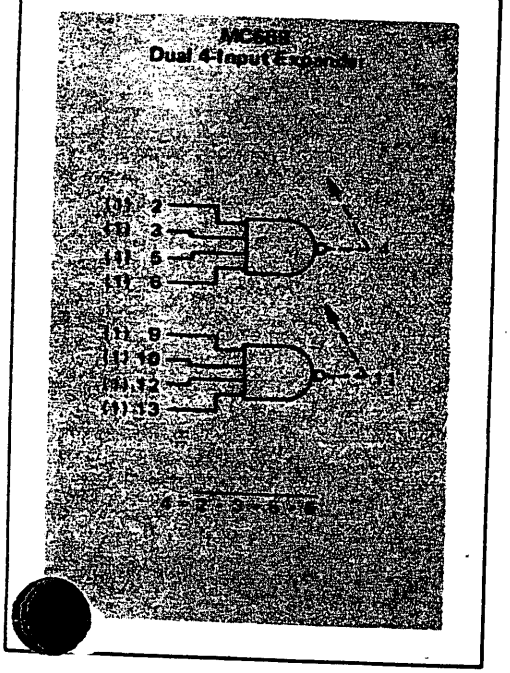
(continued)

MHTL LOGIC DIAGRAMS

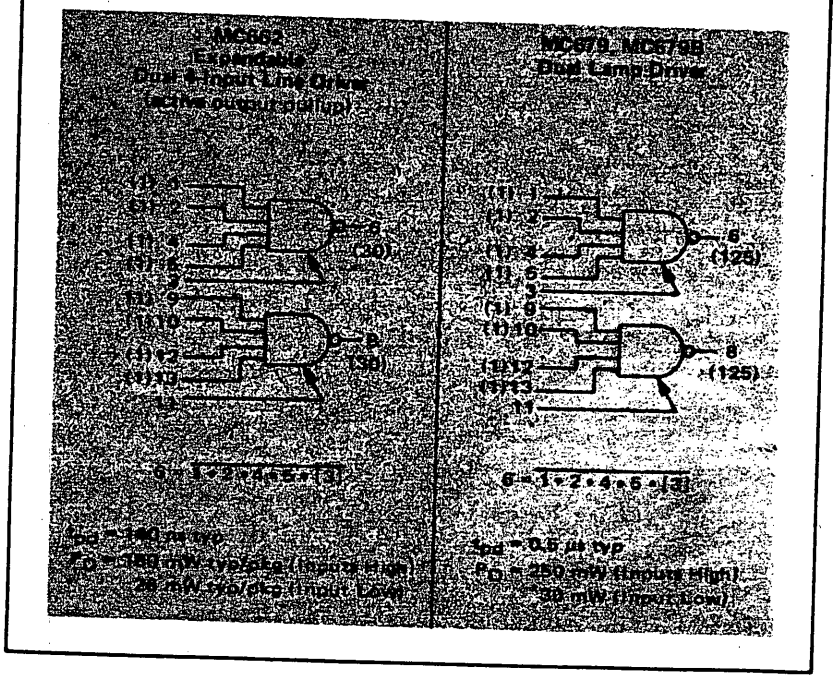
FLIP-FLOPS (continued)



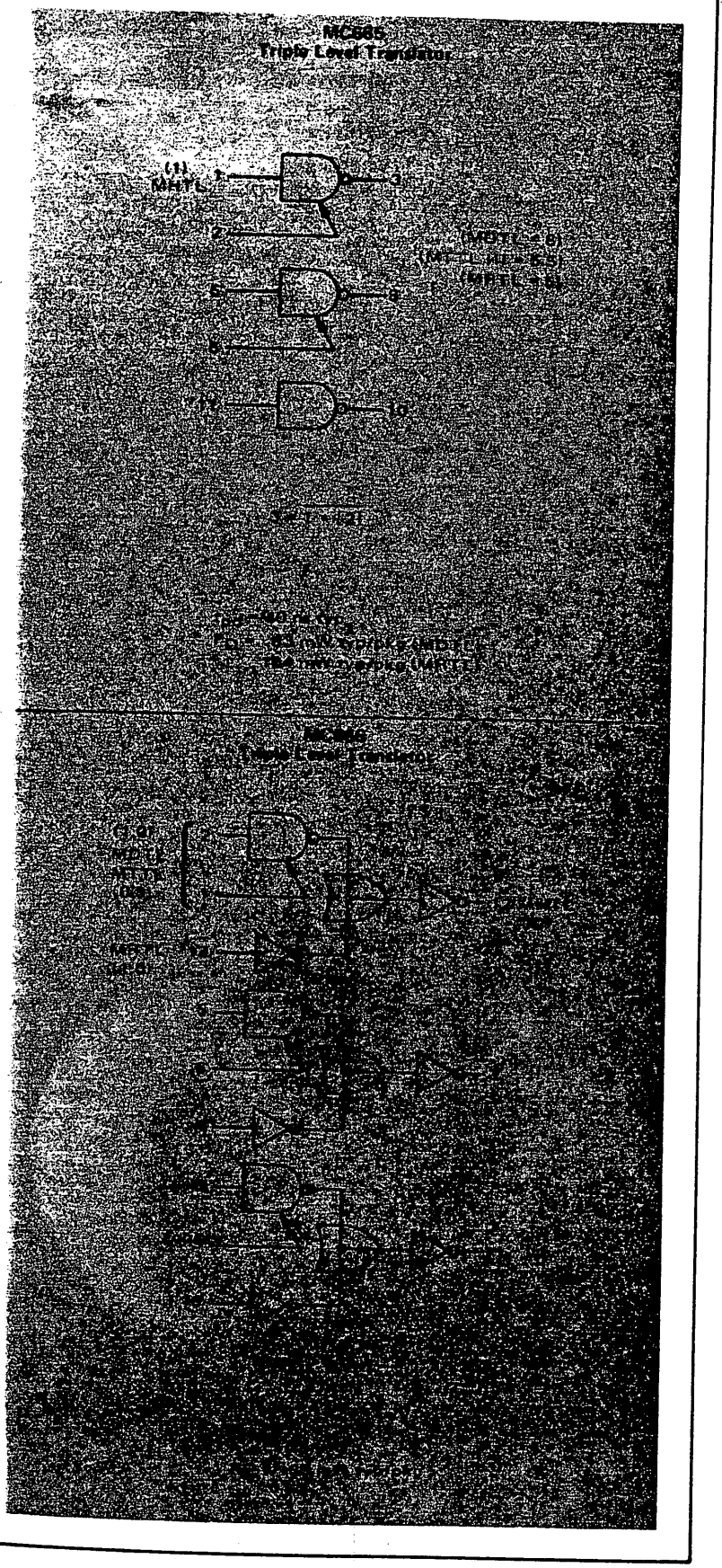
EXPANDER



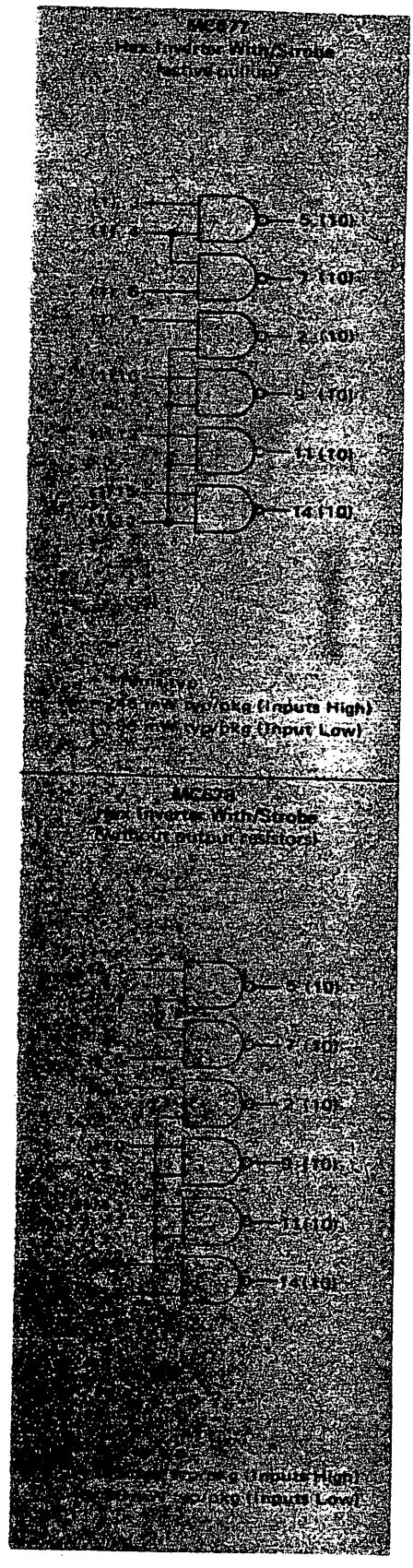
DRIVERS



TRANSLATORS



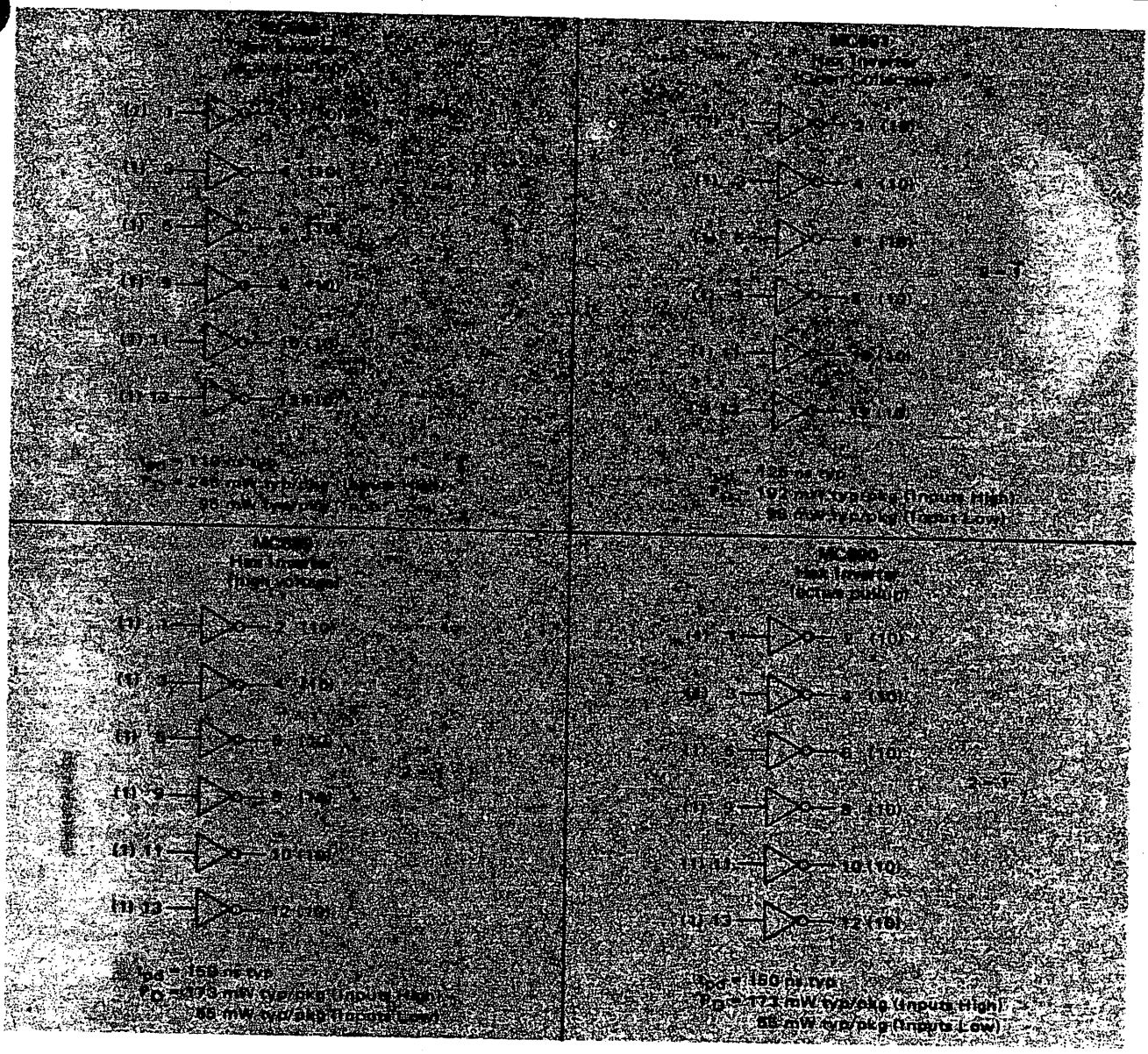
INVERTERS



(continued)

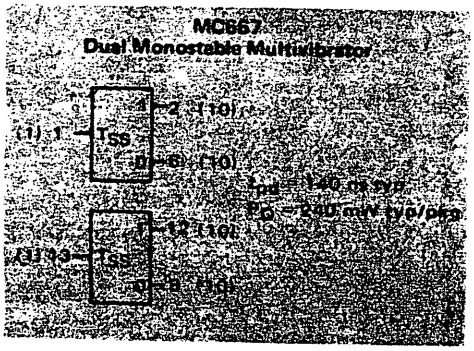
MHTL LOGIC DIAGRAMS

INVERTERS (continued)

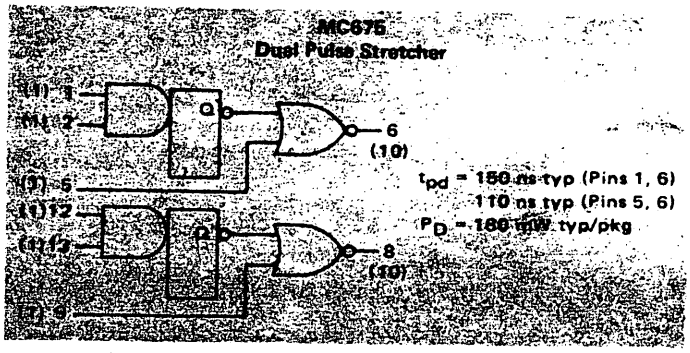


BEST COPY

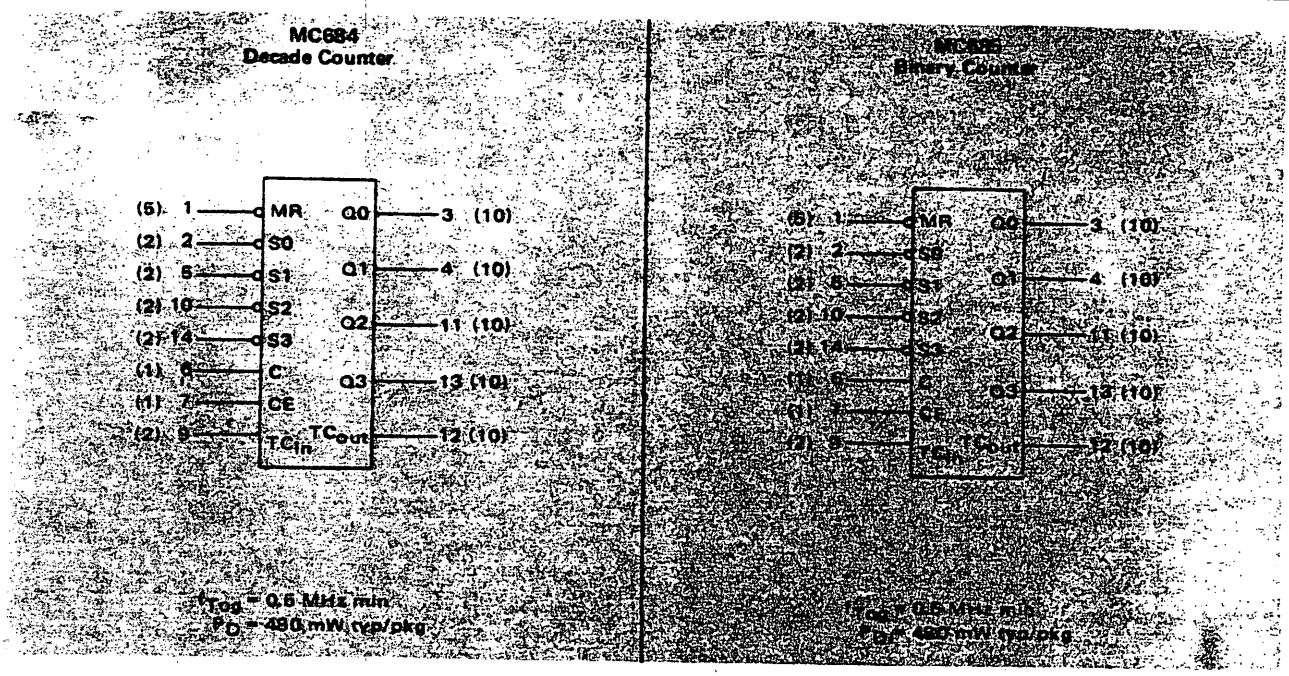
MULTIVIBRATOR



PULSE STRETCHER

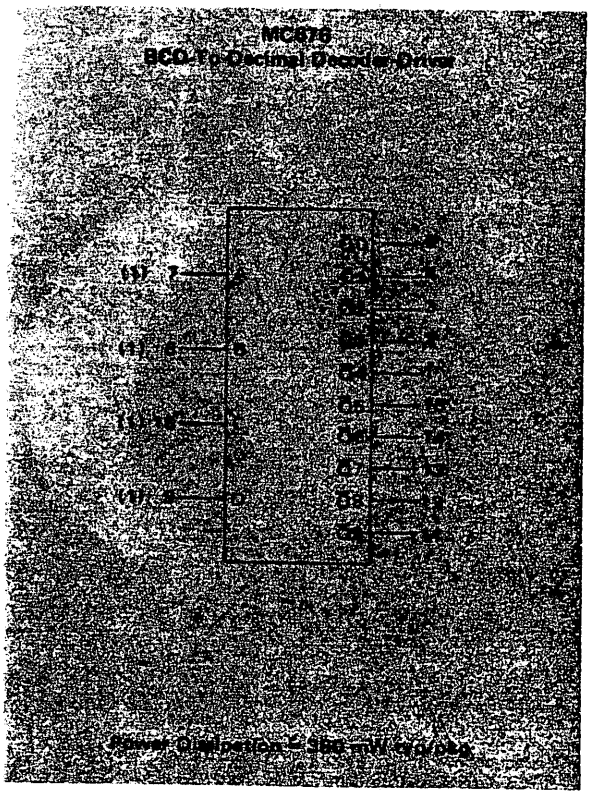


COUNTERS

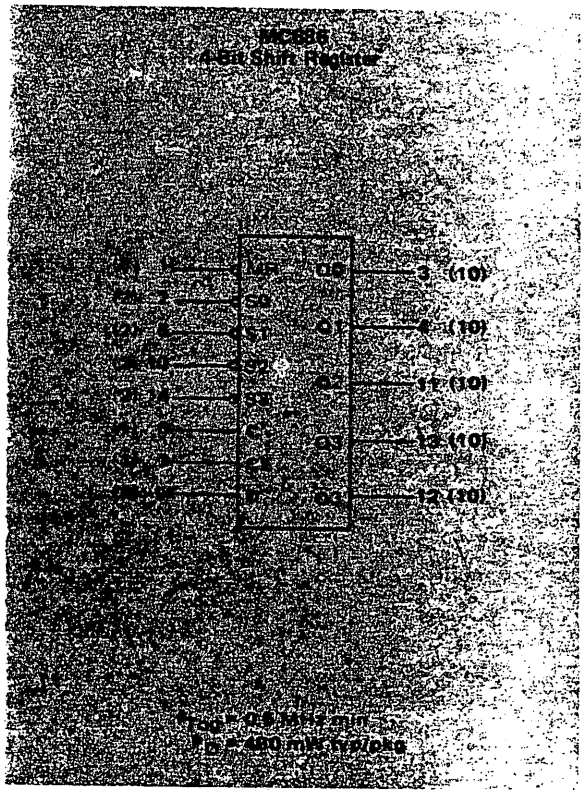


BEST COPY

DECODER

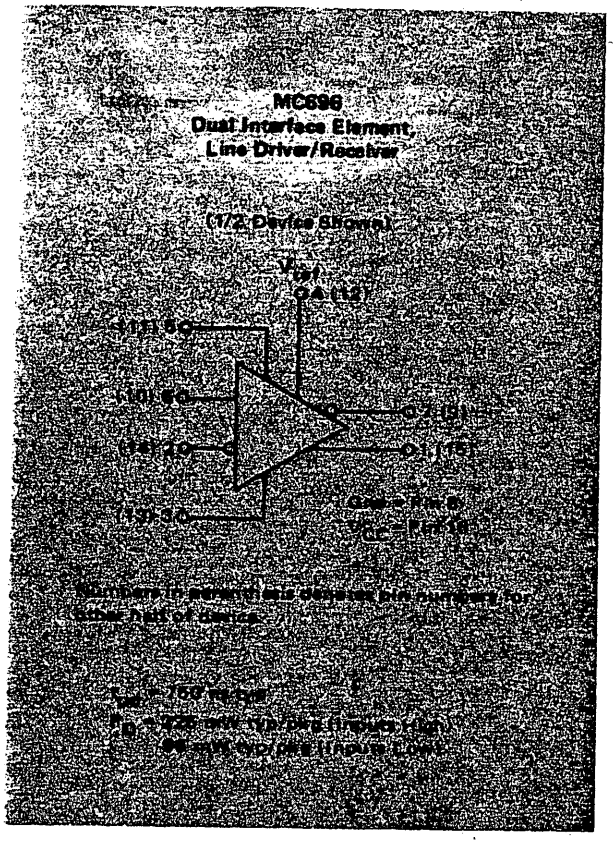


SHIFT REGISTER



MHTL LOGIC DIAGRAMS

LINE DRIVER/RECEIVER



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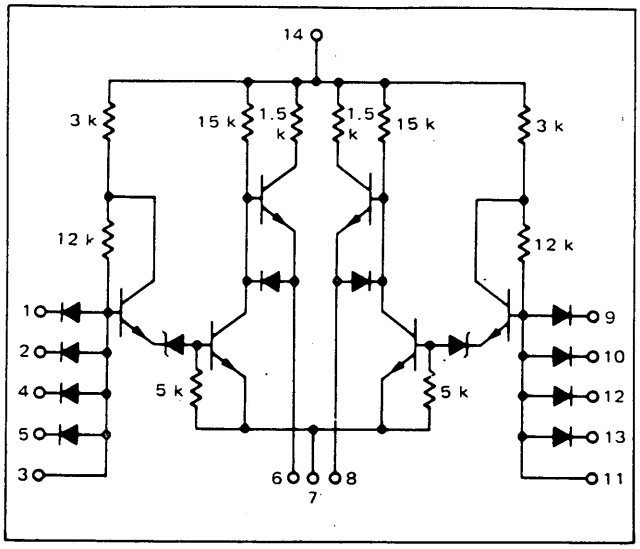
MAXIMUM RATINGS (T_A = 25°C)

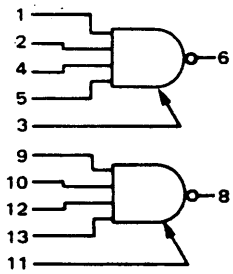
Rating	Symbol	Value	Unit

MOTOROLA Semiconductor Products Inc.
BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

MC660



This device consists of two expandable 4-input NAND gates with active output pullup.



Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High = 88 mW typ/pkg
Input Low = 26 mW typ/pkg

ELECTRICAL CHARACTERISTICS

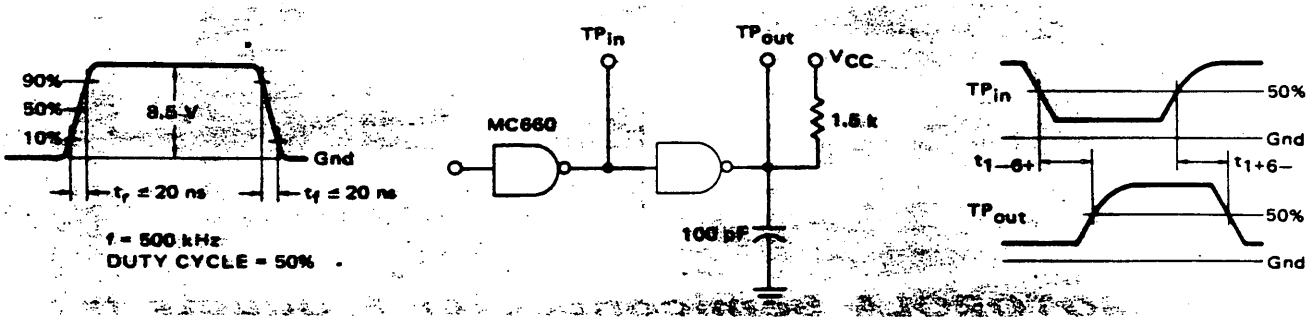
Test procedures are shown for one gate only. The other gate is tested in the same manner.

TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
mA		Volts								
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}
12.0	-0.03	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0

Characteristic	Symbol	Pin Under Test	MC660 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2, 4, 5	14	-	
			-	-		-		-		-		2	-	-	-	-	-	1, 4, 5		-	
			-	-		-		-		-		4	-	-	-	-	-	1, 2, 5		-	
			-	-		-		-		-		5	-	-	-	-	-	1, 2, 4		-	
		▼	-	-	▼	-	▼	-	▼	-	▼	-	-	-	-	3	-	-	▼	-	▼
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
		2	-	-	-		-			-	-	-	-	-	2	-	-	-		-	1, 3, 4, 5, 7
		4	-	-	-		-			-	-	-	-	-	4	-	-	-		-	1, 2, 3, 5, 7
		5	-	-	-	▼	-	▼	▼	-	-	-	-	-	5	-	-	-	▼	-	1, 2, 3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
		2	-	-	-		-			-	-	-	-	2	1, 4, 5	-	-	-	-		
		4	-	-	-		-			-	-	-	-	4	1, 2, 5	-	-	-	-		
		5	-	-	-	▼	-	▼	▼	-	-	-	-	5	1, 2, 4	-	-	-	-	▼	▼
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	3.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
	t_{1-6-}	6	-	-	-	200	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t_{1-6-}	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

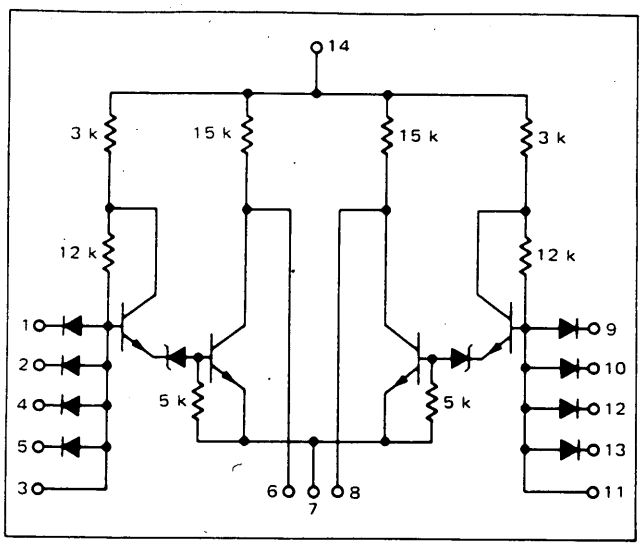


See General Information section for packaging.

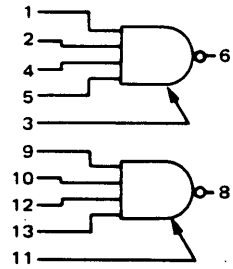
EXPANDABLE
DUAL 4-INPUT "NAND" GATE
(Passive Pullup)

MC661

ISSUE A



This device consists of two expandable 4-input NAND gates with passive output pullup.



Positive Logic $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High = 88 mW typ/pkg
Input Low = 26 mW typ/pkg

ELECTRICAL CHARACTERISTICS

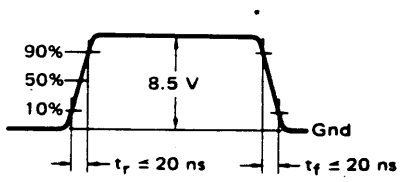
Test procedures are shown for one gate only. The other gate is tested in the same manner

TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
mA		Volts								
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}
12.0	-0.03	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0

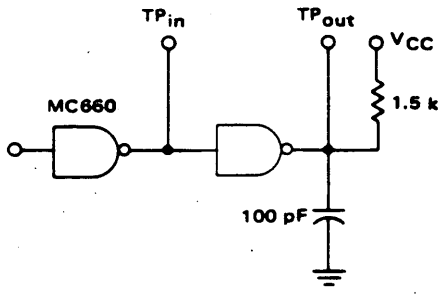
Characteristic	Symbol	Pin Under Test	MC661 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1,2,4,5	-	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2,4,5	14	-	
			-	-		-		-		-		2	-	-	-	-	-	1,4,5		-	
			-	-		-		-		-		4	-	-	-	-	-	1,2,5		-	
			-	-		-		-		-		5	-	-	-	-	-	1,2,4		-	
		▼	-	-	▼	-	▼	-	▼	-	▼	-	-	-	-	3	-	-	▼	-	▼
Short-Circuit Current	I_{SC}	6	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,2,7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2,3,4,5,7
		2	-	-	-		-			-	-	-	-	-	2	-	-	-		-	1,3,4,5,7
		4	-	-	-		-			-	-	-	-	-	4	-	-	-		-	1,2,3,5,7
		5	-	-	-	▼	-	▼	▼	-	-	-	-	-	5	-	-	-	▼	-	1,2,3,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6,14	-	-	-	1,7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2,4,5	-	-	-	-	14	7
		2	-	-	-		-			-	-	-	-	2	1,4,5	-	-	-	-		
		4	-	-	-		-			-	-	-	-	4	1,2,5	-	-	-	-		
		5	-	-	-	▼	-	▼	▼	-	-	-	-	5	1,2,4	-	-	-	-	▼	▼
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	3.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,2,4,5,7
	I_{CCH}	14	-	-	-	10	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7,10,12,13
Switching Times										Pulse In	Pulse Out										
	t_{1-6-}	6	-	-	-	250	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t_{1-6-}	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

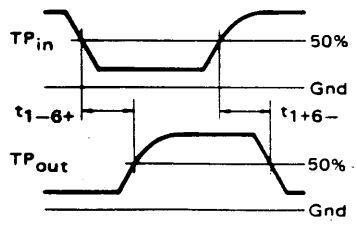
Pins not listed are left open.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



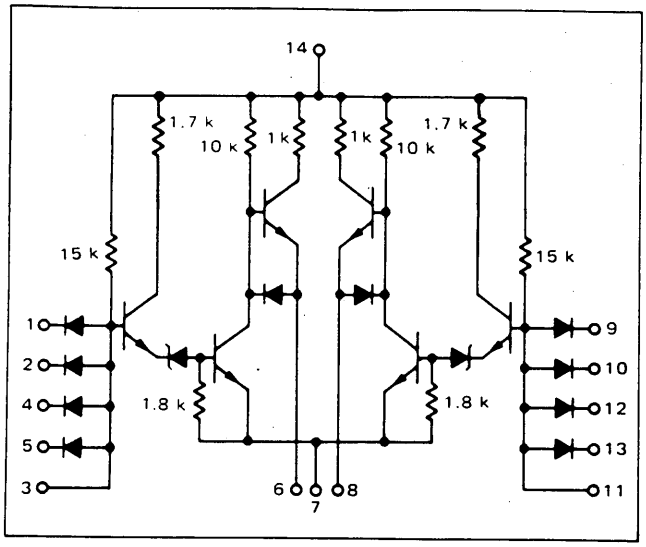
f = 500 kHz
DUTY CYCLE = 50%



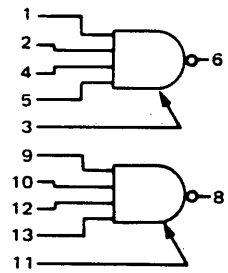


See General Information section for packaging.

MC662



This device consists of two expandable 4-input NAND line drivers with active output pullup. This device allows fan-out to 30 MHTL gates and drives large capacitive loads.



Positive Logic $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

Input Loading Factor = 1
Output Loading Factor = 30

Propagation Delay Time = 140 ns typ
Typical Total Power Dissipation
Inputs High = 180 mW typ/pkg
Input Low = 26 mW typ/pkg

ELECTRICAL CHARACTERISTICS

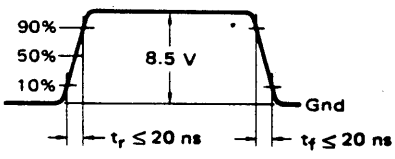
Test procedures are shown for one driver only. The other driver is tested in the same manner.

TEST CURRENT / VOLTAGE VALUES (All Temperatures)										
mA		Volts								
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}
36.0	-0.09	6.50	8.50	1.5	16.0	7.20	16.0	15.0	14.0	16.0

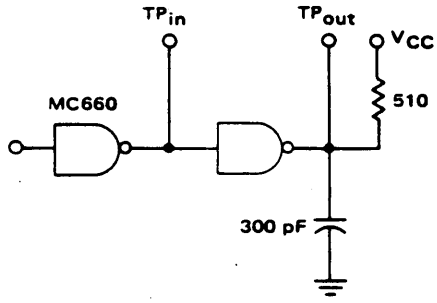
Characteristic	Symbol	Pin Under Test	MC662 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1, 2, 4, 5	-	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	1	-	-	-	-	-	2, 4, 5	14	-	
			-	-		-		-		-		2	-	-	-	-	-	1, 4, 5		-	
			-	-		-		-		-		4	-	-	-	-	-	1, 2, 5		-	
			-	-		-		-		-		5	-	-	-	-	-	1, 2, 4		-	
			-	-		-		-		-		-	-	-	-	3	-	-		-	
Short-Circuit Current	I_{SC}	6	-	-	-10.0	-25.0	-10.0	-25.0	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 6, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2, 3, 4, 5, 7
		2	-	-	-		-			-	-	-	-	-	2	-	-	-		-	1, 3, 4, 5, 7
		4	-	-	-		-			-	-	-	-	-	4	-	-	-		-	1, 2, 4, 5, 7
		5	-	-	-		-			-	-	-	-	-	5	-	-	-		-	1, 2, 3, 4, 7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	-	6, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2, 4, 5	-	-	-	-	14	7
		2	-	-	-		-			-	-	-	-	2	1, 4, 5	-	-	-	-		
		4	-	-	-		-			-	-	-	-	4	1, 2, 5	-	-	-	-		
		5	-	-	-		-			-	-	-	-	5	1, 2, 4	-	-	-	-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	4.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	17	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out										
	t_{1-6-}	6	-	-	-	250	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7
	t_{1-6-}	6	-	-	-	100	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

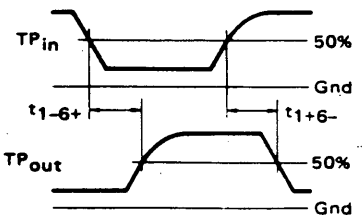
Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



f = 500 kHz
DUTY CYCLE = 50%





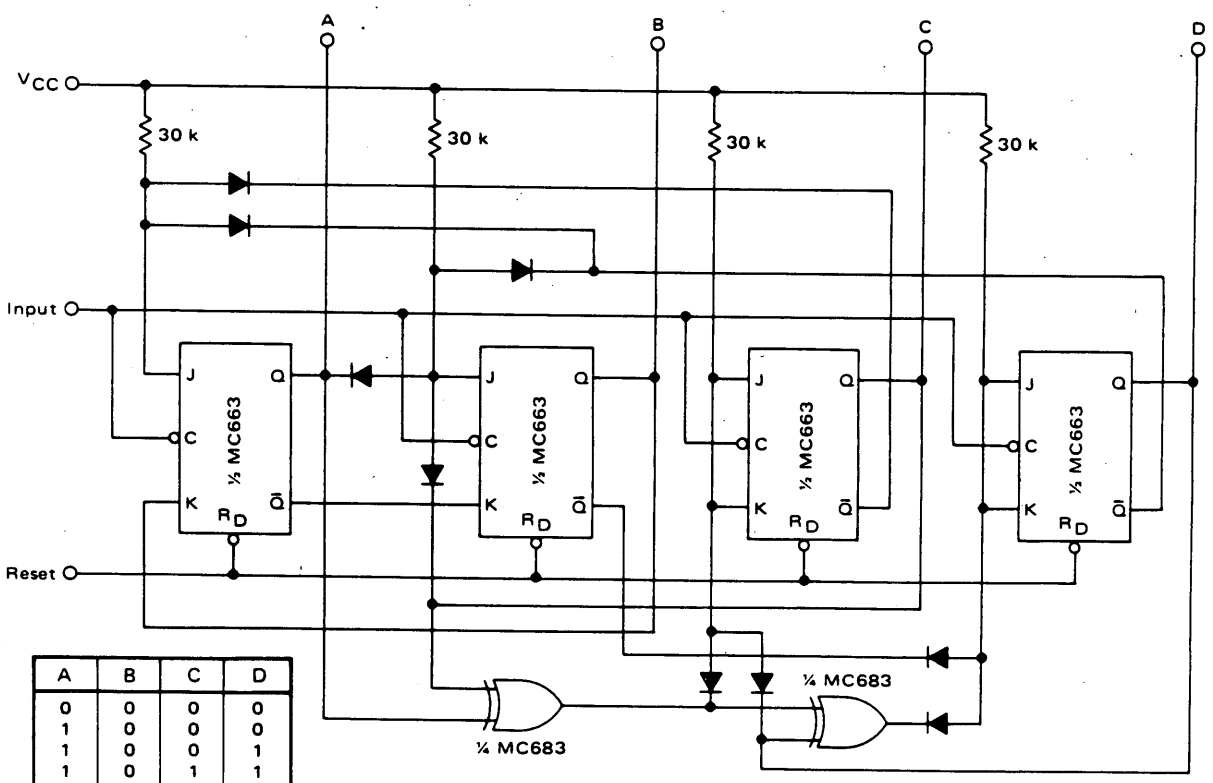
See General Information section for packaging.

APPLICATIONS INFORMATION

The fact that the MC663 may be used as either a synchronous (clocked) flip-flop or in the dynamic J-K mode lends a great deal of versatility to the device. Typical applications – as well as a description of operating principles – may be found in Application Note AN-414.

The high degree of noise immunity inherent in MHTL allows the use of diode "AND" gating if desired with very little loss in performance. A discrete 30 kΩ pull-up resistor is recommended to charge the capacitance associated with the input and insure "one" state noise immunity. (The resistor adds 0.4 loads to the input loading factor.) The Gray-Code counter circuit below illustrates this technique. The discrete components in this counter may be replaced by three 2-input NAND gates, one 3-input NAND gate, and four inverters if desired.

DECIMAL GRAY CODE COUNTER



A	B	C	D
0	0	0	0
1	0	0	0
1	0	0	1
1	0	1	1
1	0	1	0
1	1	1	0
0	1	1	0
0	0	1	0
0	0	1	1
0	0	0	1
0	0	0	0

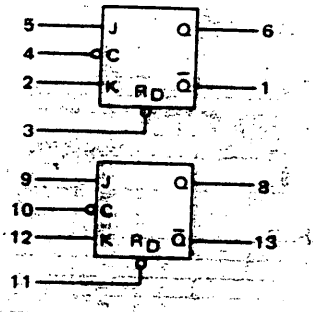
Each Diode = ½ MSD6150 Or Equivalent

DUAL J-K FLIP-FLOP

MC663

NOVEMBER 1971

Two J-K flip-flops in a single package. Each flip-flop has a direct reset input in addition to the clocked inputs.



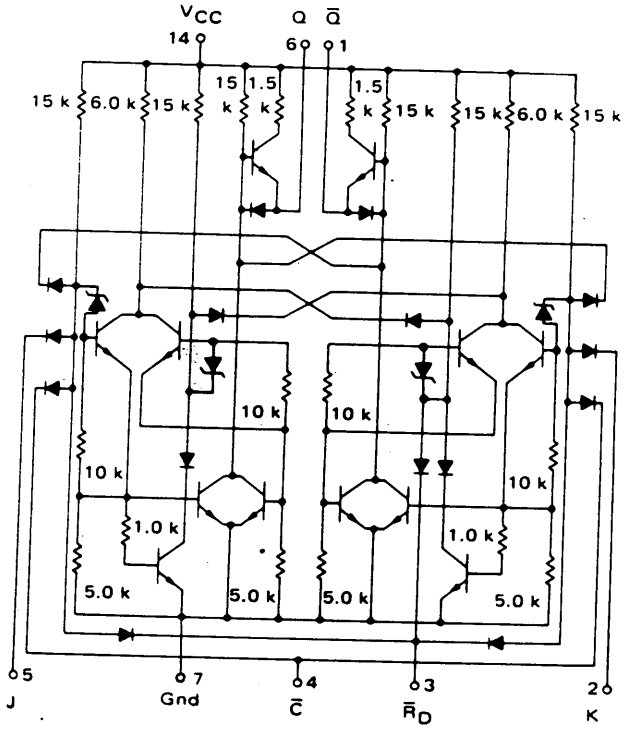
Input Loading Factor:
$\bar{R}_D$ Input = 2
$\bar{C}$ Input = 1.5
Other Inputs = 1

Output Loading Factor = 9

f_{Tog} = 3.0 MHz typ

Total Power Dissipation = 200 mW typ

CIRCUIT SCHEMATIC
(1/2 OF CIRCUIT SHOWN)



See General Information section for packaging.

TRUTH TABLE

	t_n				t_{n+1}				
	J_n	K_n	$\bar{C}_n$	$\bar{R}_D$	J_{n+1}	K_{n+1}	$\overline{C_{n+1}}$	$\bar{R}_D$	Q_{n+1}
See Note e	0	0	X	1	X	X	X	1	Q_n
	1	0	1	1	1	0	0	1	1
	0	1	1	1	0	1	0	1	0
	1	1	1	1	1	1	0	1	$\bar{Q}_n$
See Note f	X	X	0	1	X	X	0	1	Q_n
	1	X	1	1	0	K_n	1	1	1
	X	1	1	1	J_n	Q	1	1	0
	1	1	1	1	0	0	1	1	$\bar{Q}_n$
See Note g	X	X	X	1	X	X	X	0	0

a. t_n refers to the time period immediately prior to an input transition. t_{n+1} applies to the time period after the transition.

b. J_n, K_n, etc., denotes the state of the input during the time period t_n; J_{n+1}, K_{n+1}, etc., denotes the state of the input during the time period t_{n+1}.

c. Q_{n+1} denotes the state achieved by the output during the time period t_{n+1}.

d. A "0" at an input terminal denotes low state (-1.0 V to 6.5 V), "1" denotes high state (8.5 V to 18 V). An "X" means that either a "0" or "1" may be applied.

e. This portion of the truth table refers to synchronous (clocked) operation. Note that a "1" to "0" transition of the J or K input should not occur while the clock input ($\bar{C}$) is high.

f. This portion of the truth table refers to dynamic J-K operation. Note that the clock input ($\bar{C}$) must remain high for this mode of operation.

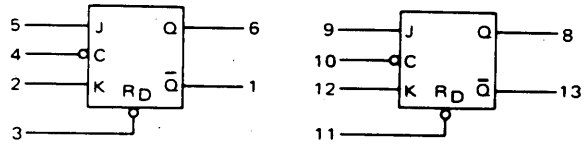
g. This portion of the truth table refers to asynchronous operation. Note that a low level on $\bar{R}_D$ overrides all other inputs.

h. Rise (or fall) time of inputs should be less than 200 nanoseconds measured between 6.5 and 8.5 volts.

j. Inputs which are not used should be returned through a resistor (2 kΩ-20 kΩ) to V_{CC}.

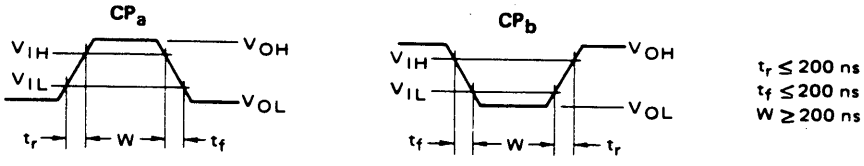
ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.



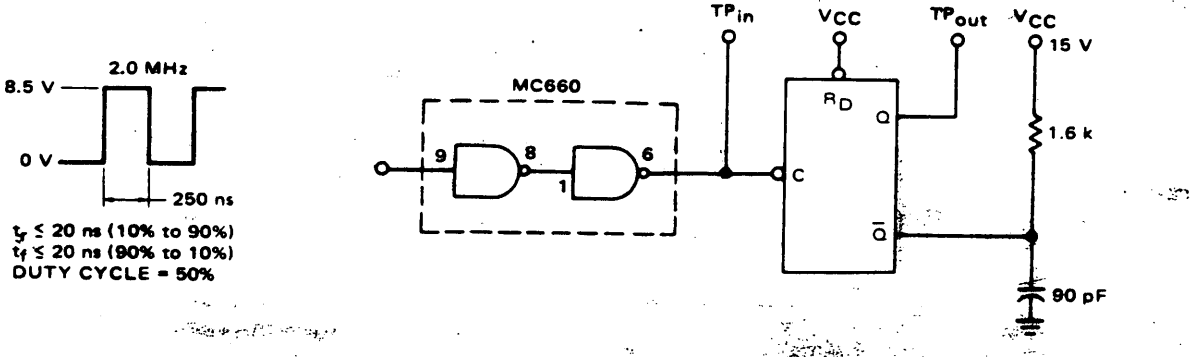
Characteristic	Symbol	Pin Under Test	MC663 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CCL}	Volts V_{CCH}	CP_a	CP_b	Gnd
										10.8	-0.027	6.50	8.50	1.5	16.0	14.0	16.0			
Output Voltage	V_{OL}	1	–	1.5	–	1.5	–	1.5	Vdc	1	–	2	3,5	–	–	14	–	4	–	7
		6	–	1.5	–	1.5	–	1.5	Vdc	6	–	5	2,3	–	–	14	–	4	–	7
	V_{OH}	1	–	–	12.5	–	12.5	–	Vdc	–	1	2,3	5	–	–	14	–	4	–	7
		1	–	–	12.5	–	12.5	–	Vdc	–	1	5	2,3	–	–	14	–	4	–	7
		6	–	–	12.5	–	12.5	–	Vdc	–	6	2	3,5	–	–	14	–	4	–	7
Short Circuit	I_{SC}	1	–	–	-6.5	-15	-6.5	-15	mAdc	–	–	3,4	–	–	–	–	14	–	–	1,7
Reverse Current	I_R	2	–	–	–	2.0	–	2.0	μAdc	–	–	–	–	–	2	14	–	–	–	3,4,5,7
	$3I_R$	3	–	–	–	6.0	–	6.0	μAdc	–	–	–	–	–	3	2,4,5,14	–	–	–	7
	$2I_R$	4	–	–	–	4.0	–	4.0	μAdc	–	–	–	–	–	4	14	–	–	–	2,3,5,7
	I_R	5	–	–	–	2.0	–	2.0	μAdc	–	–	–	–	–	5	14	–	–	–	2,3,4,7
Forward Current	I_F	2	–	–	–	-1.20	–	-1.20	mAdc	–	–	–	–	2	–	–	14	–	4	7
	$2I_F$	3	–	–	–	-2.40	–	-2.40	mAdc	–	–	–	–	3	–	–	14	–	–	2,4,5,7
	$1.5I_F$	4	–	–	–	-1.80	–	-1.80	mAdc	–	–	–	–	4	–	–	2,5,14	–	–	7
	I_F	5	–	–	–	-1.20	–	-1.20	mAdc	–	–	–	–	5	–	–	14	–	4	7
Power Drain Current (Both Flip-Flops)	I_{CCL}	14	–	–	–	16.7	–	–	mAdc	–	–	–	–	–	–	–	14	–	–	2,3,4,5,7,9, 10,11,12
	I_{CCH}	14	–	–	–	16.7	–	–	mAdc	–	–	–	–	–	–	–	14	–	–	7

Pins not listed are left open.



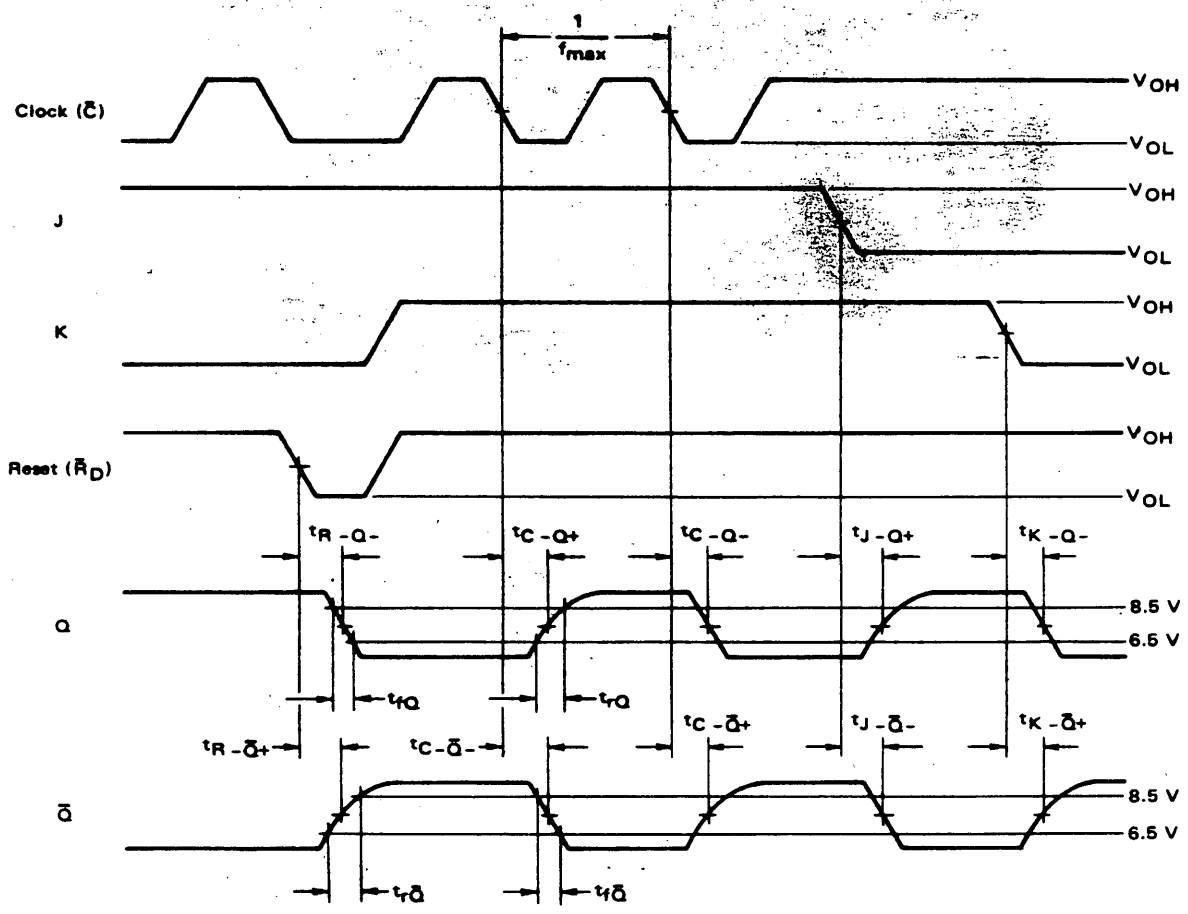
$t_r \leq 200$ ns
$t_f \leq 200$ ns
$W \geq 200$ ns

TOGGLE MODE TEST CIRCUIT



V_{CC} and ground connections to the devices are not shown.
Frequency at TP_{out} must be ½ frequency at TP_{in}.

SWITCHING CHARACTERISTICS



		-30°C	25°C		+75°C	
Characteristic	**Symbol**	**Typ**	**Min**	**Typ**	**Typ**	**Units**
Propagation Delay	t_{R-Q-}	55	–	60	65	ns
	$t_{R-\overline{Q}+}$	150	–	180	210	ns
	t_{C-Q+}, t_{J-Q+}	150	–	180	210	ns
	$t_{C-\overline{Q}-}$, $t_{J-\overline{Q}-}$	55	–	60	65	ns
	t_{C-Q-}, t_{K-Q-}	55	–	60	65	ns
	$t_{C-\overline{Q}+}$, $t_{K-\overline{Q}+}$	150	–	180	210	ns
Rise Time	t_{rQ}, $t_{r\overline{Q}}$	35	–	36	40	ns
Fall Time	t_{fQ}, $t_{f\overline{Q}}$	5.0	–	5.0	4.0	ns
Operating Frequency	f_{max}	4.0	2.0	4.0	3.0	MHz

REDUCED SUPPLY VOLTAGE OPERATION

It is sometimes desirable to operate MHTL at a power supply voltage of 12 volts rather than the specified 15 volts. Most MC663 dual flip-flops will operate with a 12 volt supply if output loading factors are reduced to 5. Noise margins will be reduced considerably, but will remain approximately 5 or 6 times better than 5 volt logic.

The supplementary electrical characteristic table listed below can be used to insure operation of the devices at 12 volt supplies. The table uses built-in guardbands to allow a high degree of probability that the devices will perform over the temperature range of 0°C to 75°C even if tests are only made at 25°C. (If tests are made at the temperature extremes, I_{OL} and I_{OH} should be reduced to 4.0 mAdc and 15 μAdc respectively, and I_R increased to 2 μAdc.)

This table does not represent guaranteed values, but rather a set of recommended tests to which the MC663 may be screened to insure operation at 12 Vdc.

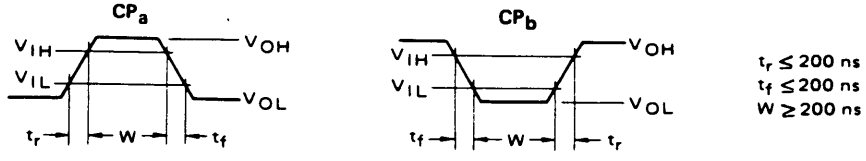
ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.

						TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
						mA		Volts								
						I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}			
						4.0	-0.012	6.50	8.50	1.8	12.25	11.75	12.25			
			Test Limits			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
Characteristic	Symbol	Pin Under Test	All Temperatures① Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}	CP_a	CP_b	Gnd
Output Voltage	V_{OL}	1	–	1.8	Vdc	1	–	2	3,5	–	–	14	–	4	–	7
		6	–	1.8	Vdc	6	–	5	2,3	–	–	14	–	4	–	7
	V_{OH}	1	10.5	–	Vdc	–	1	2,3	5	–	–	14	–	4	–	7
		1	10.5	–	Vdc	–	1	5	2,3	–	–	14	–	4	–	7
		6	10.5	–	Vdc	–	6	2	3,5	–	–	14	–	4	–	7
Short-Circuit Current	I_{SC}	1	-5.0	-10.0	mAdc	–	–	3,4	–	–	–	–	14	–	–	1,7
Reverse Current	I_R	2	–	1.5	μAdc	–	–	–	–	–	2	14	–	–	–	3,4,5,7
	$3I_R$	3	–	4.5	μAdc	–	–	–	–	–	3	2,4,5,14	–	–	–	7
	$2I_R$	4	–	3.0	μAdc	–	–	–	–	–	4	14	–	–	–	2,3,5,7
	I_R	5	–	1.5	μAdc	–	–	–	–	–	5	14	–	–	–	2,3,4,7
Forward Current	I_F	2	-0.55	-0.80	mAdc	–	–	–	–	2	–	–	14	–	4	7
	$2I_F$	3	-1.10	-1.60	mAdc	–	–	–	–	3	–	–	14	–	–	2,4,5,7
	$1.5I_F$	4	-0.80	-1.20	mAdc	–	–	–	–	4	–	–	2,5,14	–	–	7
	I_F	5	-0.55	-0.80	mAdc	–	–	–	–	5	–	–	14	–	4	7
Power Drain Current (Both Flip-Flops)	I_{CCL}	14	–	12.0	mAdc	–	–	–	–	–	–	–	14	–	–	2,3,4,5,7,9,10,11,12
	I_{CCH}	14	–	12.0	mAdc	–	–	–	–	–	–	–	14	–	–	7

Pins not listed are left open

① Best results obtained if T_A limited to 0°C to 75°C.



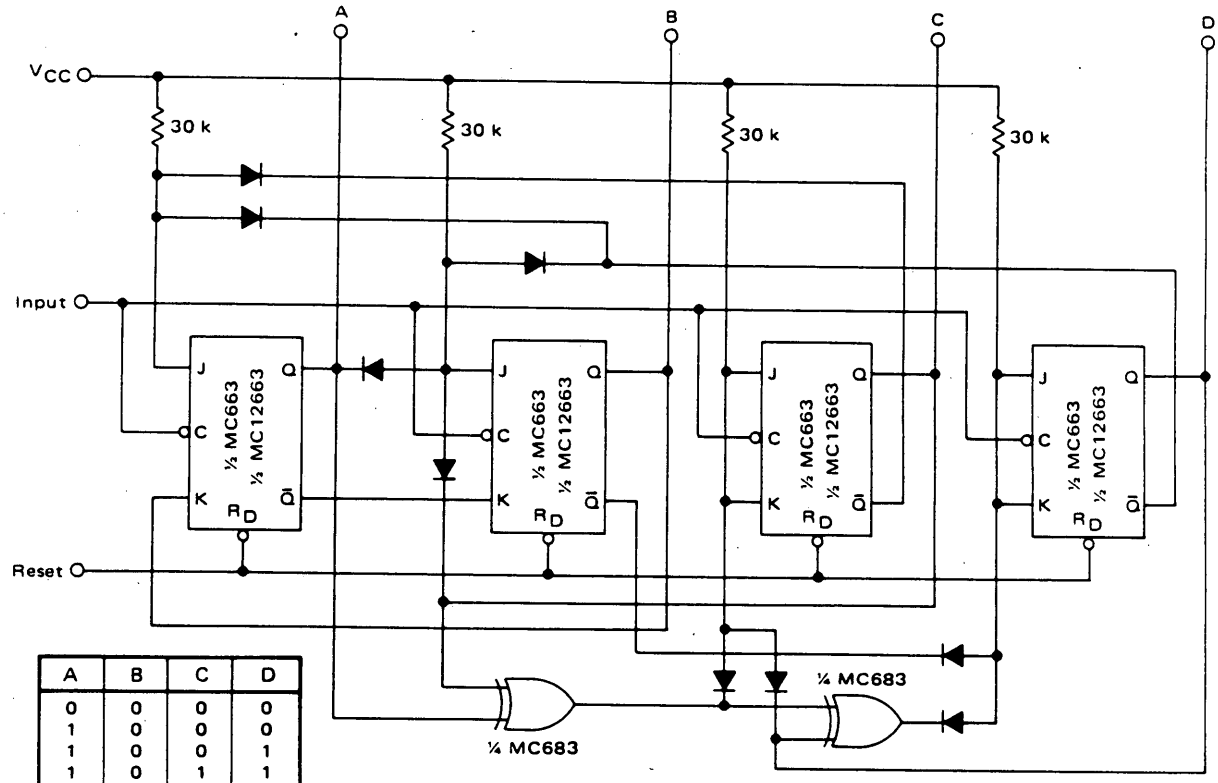
$t_r \leq 200$ ns
$t_f \leq 200$ ns
$W \geq 200$ ns

APPLICATIONS INFORMATION

The fact that the MC663/12663 may be used as either a synchronous (clocked) flip-flop or in the dynamic J-K mode lends a great deal of versatility to the device. Typical applications – as well as a description of operating principles – may be found in Application Note AN-414.

The high degree of noise immunity inherent in MHTL allows the use of diode "AND" gating if desired with very little loss in performance. A discrete 30 kΩ pull-up resistor is recommended to charge the capacitance associated with the input and insure "one" state noise immunity. (The resistor adds 0.4 loads to the input loading factor.) The Gray-Code counter circuit below illustrates this technique. The discrete components in this counter may be replaced by three 2-input NAND gates, one 3-input NAND gate, and four inverters if desired.

DECIMAL GRAY CODE COUNTER

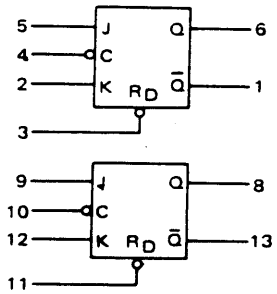


A	B	C	D
0	0	0	0
1	0	0	0
1	0	0	1
1	0	1	1
1	0	1	0
1	1	1	0
0	1	1	0
0	0	1	0
0	0	1	1
0	0	0	1
0	0	0	0

Each Diode = ½ MSD6150 Or Equivalent

MC663
MC12663

ISSUE A



The MC663 and the MC12663 consist of two J-K flip-flops having direct reset inputs in addition to clocked inputs. The 15 volt V_{CC} device (MC663) and the extended 12-15 volt V_{CC} device (MC12663), are schematically indentical. The MC12663 meets the MC663 specifications in addition to the 12 volt specifications. Both are available in the 14 pin dual-in-line plastic package (suffix P) and the 14 pin dual-in-line ceramic package (suffix L). A full temperature version of the MC663 dual-in-line ceramic is also available (suffix tL). This device meets the -30 to +75 standard specifications at -55 to +125 respectively.

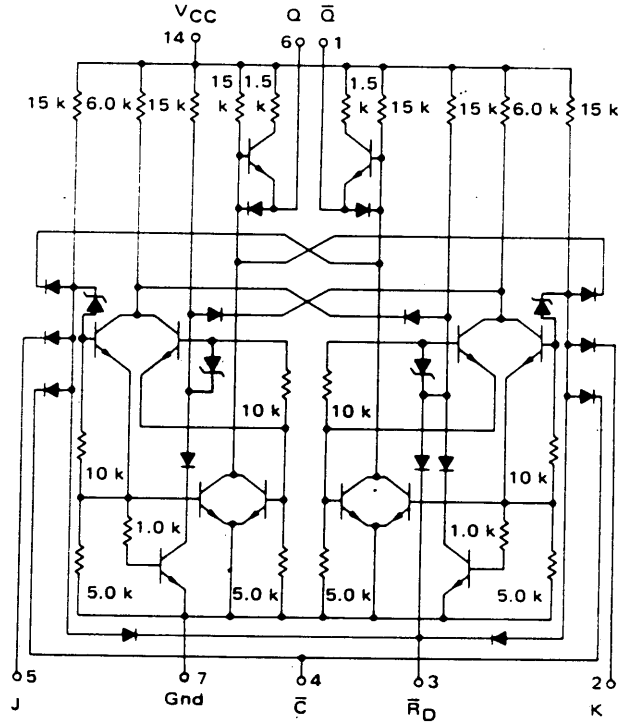
Input Loading Factor:
$\bar{R}_D$ Input = 2
$\bar{C}$ Input = 1.5
Other Inputs = 1

Output Loading Factor = 9

f_{Tog} = 3.0 MHz typ

Total Power Dissipation = 200 mW typ

CIRCUIT SCHEMATIC
(1/2 OF CIRCUIT SHOWN)



See General Information section for packaging.

TRUTH TABLE

	t_n				t_{n+1}				
	J_n	K_n	$\bar{C}_n$	$\bar{R}_D$	J_{n+1}	K_{n+1}	$\overline{C_{n+1}}$	$\bar{R}_D$	Q_{n+1}
See Note e	0	0	X	1	X	X	X	1	Q_n
	1	0	1	1	1	0	0	1	1
	0	1	1	1	0	1	0	1	0
	1	1	1	1	1	1	0	1	$\bar{Q}_n$
See Note f	X	X	0	1	X	X	0	1	Q_n
	1	X	1	1	0	K_n	1	1	1
	X	1	1	1	J_n	0	1	1	0
	1	1	1	1	0	0	1	1	$\bar{Q}_n$
See Note g	X	X	X	1	X	X	X	0	0

a. t_n refers to the time period immediately prior to an input transition. t_{n+1} applies to the time period after the transition.

b. J_n, K_n, etc., denotes the state of the input during the time period t_n; J_{n+1}, K_{n+1}, etc., denotes the state of the input during the time period t_{n+1}.

c. Q_{n+1} denotes the state achieved by the output during the time period t_{n+1}.

d. A "0" at an input terminal denotes low state (-1.0 V to 6.5 V), "1" denotes high state (8.5 V to 18 V). An "X" means that either a "0" or "1" may be applied.

e. This portion of the truth table refers to synchronous (clocked) operation. Note that a "1" to "0" transition of the J or K input should not occur while the clock input ($\bar{C}$) is high.

f. This portion of the truth table refers to dynamic J-K operation. Note that the clock input ($\bar{C}$) must remain high for this mode of operation.

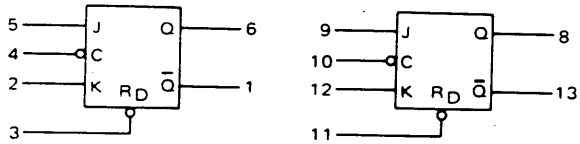
g. This portion of the truth table refers to asynchronous operation. Note that a low level on $\bar{R}_D$ overrides all other inputs.

h. Rise (or fall) time of inputs should be less than 200 nanoseconds measured between 6.5 and 8.5 volts.

j. Inputs which are not used should be returned through a resistor (2 kΩ-20 kΩ) to V_{CC}.

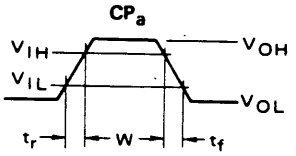
ELECTRICAL CHARACTERISTICS

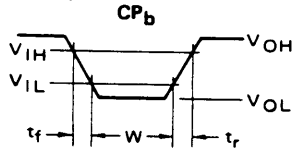
ss otherwise noted, tests are shown for y one flip-flop. The other flip-flop is tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC663 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CCL}	Volts V_{CCH}	CP_a	CP_b	Gnd
										10.8	-0.027	6.50	8.50	1.5	16.0	14.0	16.0			
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
Output Voltage	V_{OL}	1	–	1.5	–	1.5	–	1.5	Vdc	1	–	2	3,5	–	–	14	–	4	–	7
		6	–	1.5	–	1.5	–	1.5	Vdc	6	–	5	2,3	–	–	14	–	4	–	7
	V_{OH}	1	–	–	12.5	–	12.5	–	Vdc	–	1	2,3	5	–	–	14	–	4	–	7
		1	–	–	12.5	–	12.5	–	Vdc	–	1	5	2,3	–	–	14	–	4	–	7
		6	–	–	12.5	–	12.5	–	Vdc	–	6	2	3,5	–	–	14	–	4	–	7
Short Circuit	I_{SC}	1	–	–	-6.5	-15	-6.5	-15	mAdc	–	–	3,4	–	–	–	–	14	–	–	1,7
Reverse Current	I_R	2	–	–	–	2.0	–	2.0	μAdc	–	–	–	–	–	2	14	–	–	–	3,4,5,7
	$3I_R$	3	–	–	–	6.0	–	6.0	μAdc	–	–	–	–	–	3	2,4,5,14	–	–	–	7
	$2I_R$	4	–	–	–	4.0	–	4.0	μAdc	–	–	–	–	–	4	14		–	–	2,3,5,7
	I_R	5	–	–	–	2.0	–	2.0	μAdc	–	–	–	–	–	5	14	–	–	–	2,3,4,7
Forward Current	I_F	2	–	–	–	-1.20	–	-1.20	mAdc	–	–	–	–	2	–	–	14	–	4	7
	$2I_F$	3	–	–	–	-2.40	–	-2.40	mAdc	–	–	–	–	3	–	–	14	–	–	2,4,5
	$1.5I_F$	4	–	–	–	-1.80	–	-1.80	mAdc	–	–	–	–	4	–	–	2,5,14	–	–	7
	I_F	5	–	–	–	-1.20	–	-1.20	mAdc	–	–	–	–	5	–	–	14	–	4	7
Power Drain Current (Both Flip-Flops)	I_{CCL}	14	–	–	–	16.7	–	–	mAdc	–	–	–	–	–	–	–	14	–	–	2,3,4,5,7,9, 10,11,12
	I_{CCH}	14	–	–	–	16.7	–	–	mAdc	–	–	–	–	–	–	–	14	–	–	7

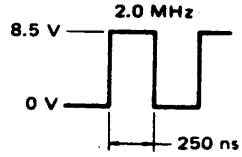
Pins not listed are left open



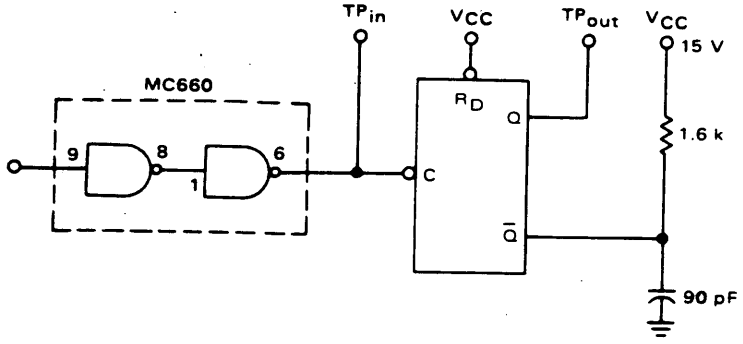


$t_r \leq 200$ ns
$t_f \leq 200$ ns
$W \geq 200$ ns

TOGGLE MODE TEST CIRCUIT

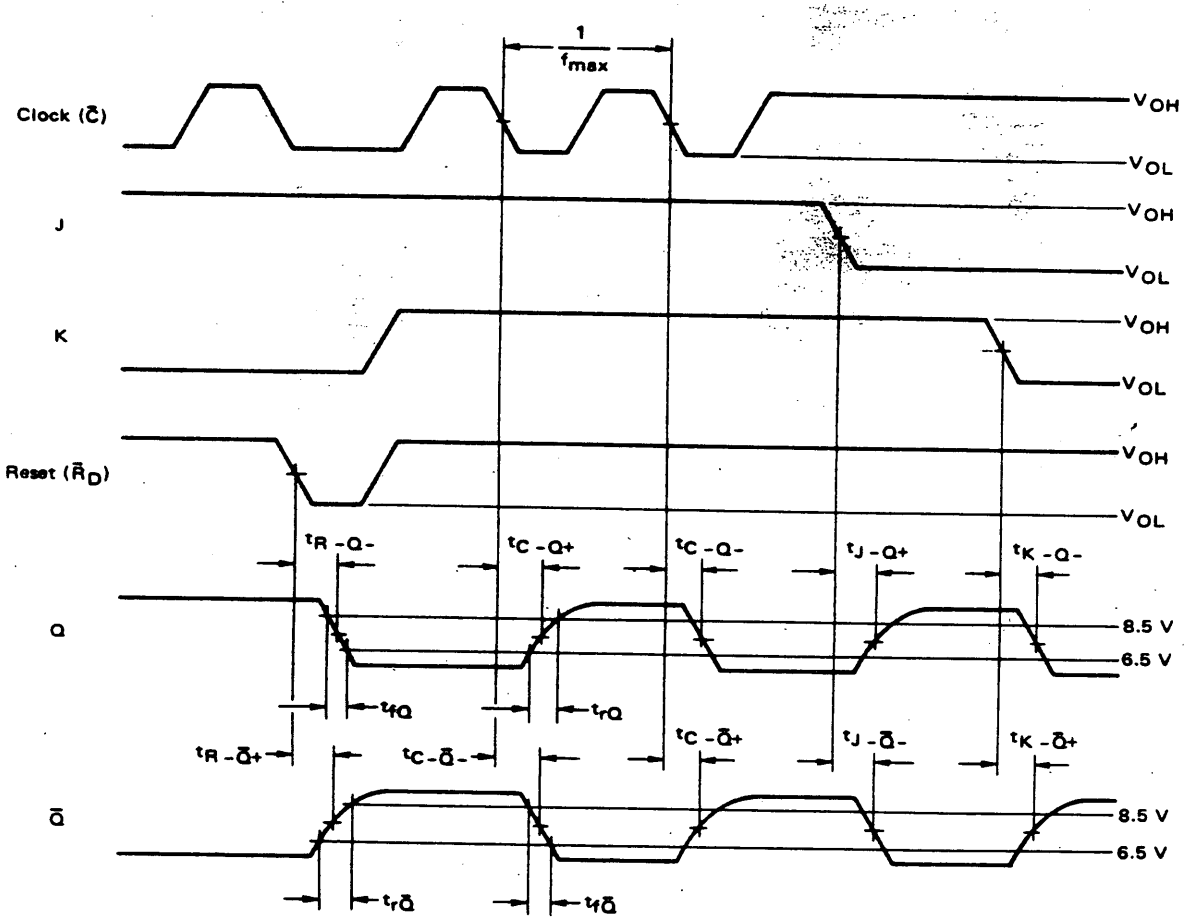


$t_r \leq 20$ ns (10% to 90%)
$t_f \leq 20$ ns (90% to 10%)
DUTY CYCLE = 50%



V_{CC} and ground connections to the devices are not shown.
Frequency at TP_{out} must be ½ frequency at TP_{in}.

SWITCHING CHARACTERISTICS



Characteristic	Symbol	-30°C Typ	25°C Min	25°C Typ	+75°C Typ	Units
Propagation Delay	t_{R-Q-}	55	–	60	65	ns
	$t_{R-\bar{Q}+}$	150	–	180	210	ns
	t_{C-Q+}, t_{J-Q+}	150	–	180	210	ns
	$t_{C-\bar{Q}-}$, $t_{J-\bar{Q}-}$	55	–	60	65	ns
	t_{C-Q-}, t_{K-Q-}	55	–	60	65	ns
	$t_{C-\bar{Q}+}$, $t_{K-\bar{Q}+}$	150	–	180	210	ns
Rise Time	t_{rQ}, $t_{r\bar{Q}}$	35	–	36	40	ns
Fall Time	t_{fQ}, $t_{f\bar{Q}}$	5.0	–	5.0	4.0	ns
Operating Frequency	f_{max}	4.0	2.0	4.0	3.0	MHz

MC12663 – EXTENDED 12-15 VOLT SUPPLY VOLTAGE OPERATION

Most MC663 devices are operable at a V_{CC} as low as 12 volts, there are times when it is necessary to guarantee the 12 volt V_{CC} Operation as well as certain maximum and minimum electrical characteristics. The MC12663 is guaranteed to meet both the standard MC663 electrical specifications and the 12 volt electrical characteristics.

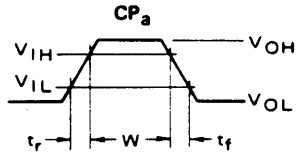
ELECTRICAL CHARACTERISTICS – MC12663

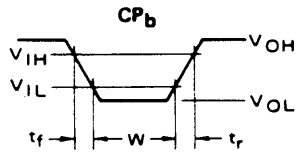
Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.

						TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
						mA			Volts						
						I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}			
						8.0	-0.016	6.50	8.50	1.5	12	12			
			Test Limits			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:									
Characteristic	Symbol	Pin Under Test	$-30 \leq T_A \leq +75^{\circ}C$ (1) Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	CP_a	CP_b	Gnd
Output Voltage	V_{OL}	1	–	1.8	Vdc	1	–	2	3.5	–	–	14	4		7
		6	–	1.8	Vdc	6	–	5	2.3	–	–	14	4		7
	V_{OH}	1	11.0	–	Vdc	–	1	2,3	5	–	–	14	4		7
		1	11.0	–	Vdc	–	1	5	2,3	–	–	14	4		7
		6	11.0	–	Vdc	–	6	2	2,3	–	–	14	4		7
Short Circuit Current	I_{CS}	1	-4.5	-12	mAdc	–	–	3,4	–	–	–	14	–		1,7
Reverse Current	I_R	2	–	2.0	µAdc	–	–	–	–	–	2	14	–		3,4,5,7
	$3I_R$	3	–	6.0	µAdc	–	–	–	–	–	3	2,4,5,14	–		7
	$2I_R$	4	–	4.0	µAdc	–	–	–	–	–	4	14			2,3,5,7
	I_R	5	–	2.0	µAdc	–	–	–	–	–	5	14	–		2,3,4,7
Forward Current	I_F	2	-0.55	-1.0	mAdc	–	–	–	–	2	–	14	–	4	7
	$2I_F$	3	-1.10	-2.0	mAdc	–	–	–	–	3	–	14	–	–	2,4,5
	$1.5I_F$	4	-0.80	-1.5	mAdc	–	–	–	–	4	–	2,5,14	–	–	7
	I_F	5	-0.55	-1.0	mAdc	–	–	–	–	5	–	14	–	4	7
Power Drain Current	I_{CCL}	14	–	12.5	mAdc	–	–	–	–	–	–	14	–		2,3,4,5,7,9,10,11
(Both Flip-Flops)	I_{CCH}	14	–	12.5	mAdc	–	–	–	–	–	–	14	–		7

Pins not listed are left open

(1) Best results obtained if T_A limited to 0°C to 75°C.



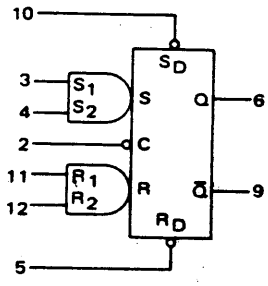


$t_r \leq 200$ ns
$t_f \leq 200$ ns
$W \geq 200$ ns

MC664

ISSUE A

A dc coupled R-S flip-flop operating on the master-slave principle. Information is entered in the master section while the clock pulse is high and is transferred to the slave when the clock goes negative.



DIRECT INPUT OPERATION

$\bar{R}_D$	$\bar{S}_D$	Q	$\bar{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

Clock input (C) must be low.
NC = No change
NA = Not allowed

CLOCKED OPERATION

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

Direct inputs ($\bar{R}_D$, $\bar{S}_D$) must be high.

Input Loading Factor:
$\bar{C}$ Input = 3
Other Inputs = 1

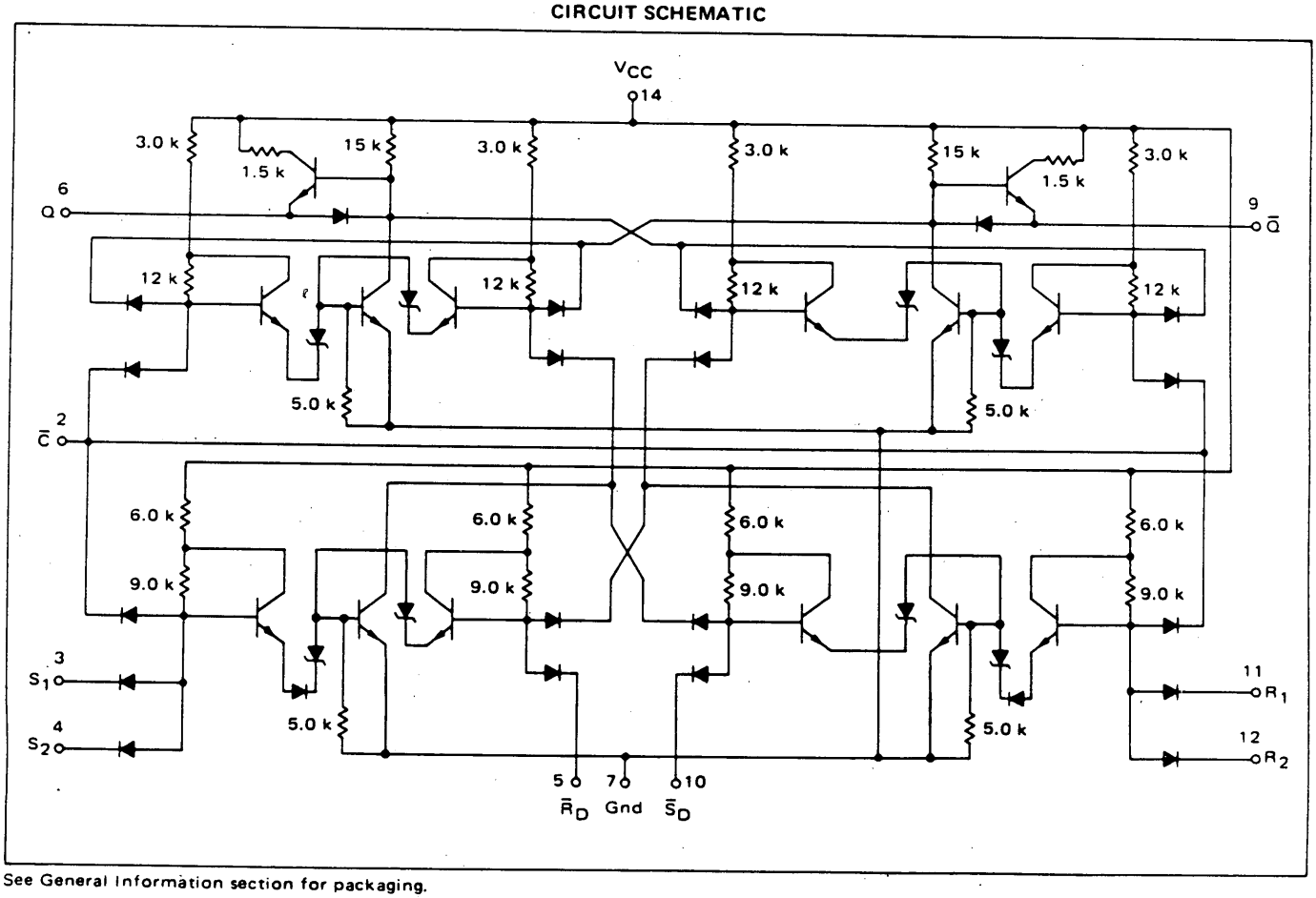
Output Loading Factor = 8

f_{Tog} = 3.0 MHz typ

Total Power Dissipation = 160 mW typ/pkg

0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

CIRCUIT SCHEMATIC



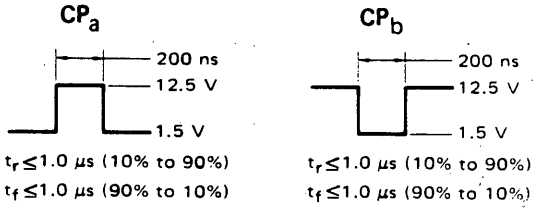
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

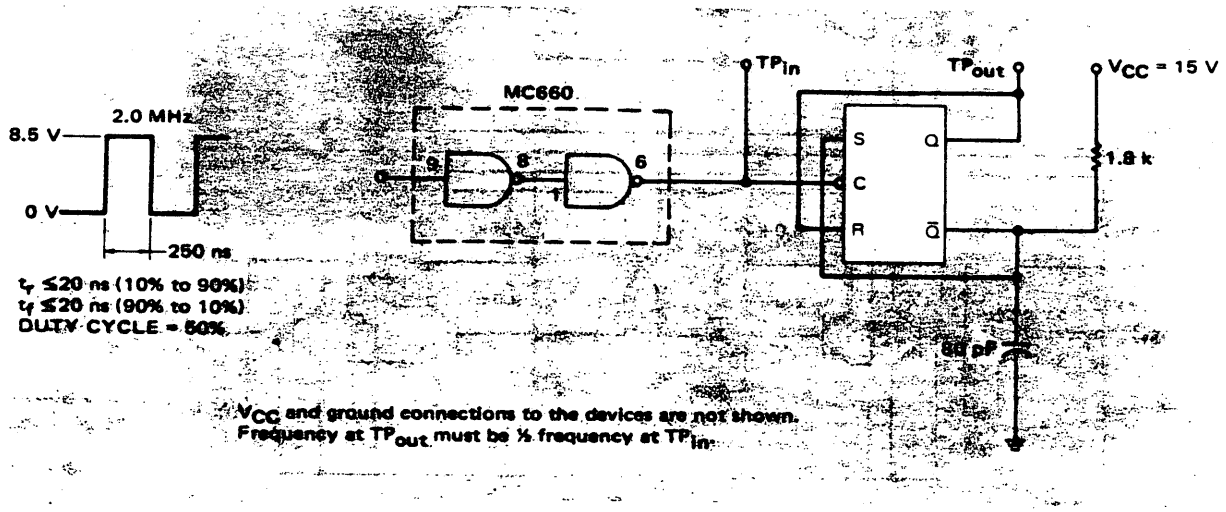
TEST CURRENT / VOLTAGE VALUES (All Temperatures)							
mA		Volts					
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}
9.6	-0.024	6.50	8.50	1.5	16.0	14.0	16.0

Characteristic	Symbol	Pin Under Test	MC664 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}	CP_a	CP_b	Ground
Output Voltage	V_{OL}	6*	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	3, 4, 11, 12	-	-	14	-	-	5	7
		6	-	↓	-	↓	-	↓	↓	6	-	4	3, 5, 11, 12	-	-	↓	-	2	-	7
		6	-		-		-			6	-	3	4, 5, 11, 12	-	-		-	2	-	7
		9‡	-		-		-			9	-	-	3, 4, 11, 12	-	-		-	-	10	7
		9	-		-		-			9	-	11	3, 4, 10, 12	-	-		-	2	-	7
		9	-		-		-			9	-	12	3, 4, 10, 11	-	-		-	2	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	-	5	-	-	14	-	-	-	2, 3, 4, 7, 10, 11, 12
		9	-	-	12.5	-	12.5	-		-	9	-	10	-	-	14	-	-	-	2, 3, 4, 5, 7, 11, 12
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 5	10	-	-	-	14	-	-	6, 7, 9
		9	-	-	-6.5	-15	-6.5	-15	mAdc	-	-	2, 10	5	-	-	-	14	-	-	6, 7, 9
Reverse Current	$4I_R$	2§	-	-	-	8.0	-	8.0	μAdc	-	-	-	5	-	2	14	-	-	-	3, 4, 7, 10, 11, 12
	$4I_R$	2†	-	-	-	8.0	-	8.0		-	-	-	10	-	2	14	-	-	-	3, 4, 5, 7, 11, 12
	I_R	3	-	-	-	2.0	-	2.0		-	-	-	-	-	3	14	-	-	-	2, 4, 7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	-	4	14	-	-	-	2, 3, 7
		5	-	-	-		-			-	-	-	2, 11, 12	-	5	14	-	-	-	7
		10	-	-	-		-			-	-	-	2, 3, 4	-	10	14	-	-	-	7
		11	-	-	-		-			-	-	-	-	-	11	14	-	-	-	2, 7, 12
		12	-	-	-	↓	-	↓	↓	-	-	-	-	-	12	14	-	-	-	2, 7, 11
Forward Current	$3I_F$	2	-	-	-	-3.60	-	-3.60	mAdc	-	-	-	5	2	3, 4, 11, 12	-	14	-	-	7, 10
	$3I_F$	2	-	-	-	-3.60	-	-3.60		-	-	-	10	2	3, 4, 11, 12	-	14	-	-	5, 7
	I_F	3	-	-	-	-1.20	-	-1.20		-	-	-	-	3	2, 4	-	14	-	-	7
		4	-	-	-	↓	-	↓	↓	-	-	-	-	4	2, 3	-	14	-	-	7
		5	-	-	-		-			-	-	-	-	5	-	-	14	-	-	2, 7, 10, 11, 12
		10	-	-	-		-			-	-	-	-	10	-	-	14	-	-	2, 3, 4, 5, 7
		11	-	-	-		-			-	-	-	-	11	2, 12	-	14	-	-	7
		12	-	-	-	↓	-	↓	↓	-	-	-	-	12	2, 11	-	14	-	-	7
Power Drain Current	I_{CCL}	14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	2, 3, 4, 5, 7, 10, 11, 12
	I_{CCH}	14	-	-	-	14.5	-	-	mAdc	-	-	-	-	-	-	-	14	-	-	7

Pins not listed are left open.
*Apply momentary ground to pins 9 and 10 prior to clock pulse
‡Apply momentary ground to pins 5 and 6 prior to clock pulse
§Apply momentary ground to pin 9
†Apply momentary ground to pin 6



TOGGLE MODE TEST CIRCUIT



*VCC and ground connections to the devices are not shown.
Frequency at TP_{out} must be ½ frequency at TP_{in}.

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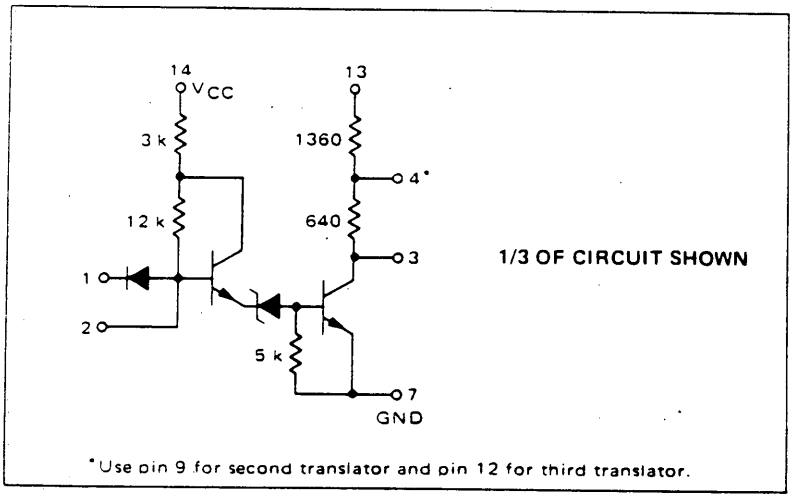
3073-44 PRINTED IN U.S.A. 9-73 IMPERIAL LITHO 837146 10M

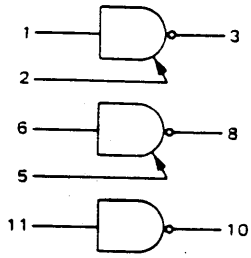
MC665

JANUARY 197

This device is a triple unit capable of translating MHTL logic levels to MRTL, MDTL, or MTTL logic levels. This device is useful when using MHTL devices as peripheral circuitry for a high-speed, low-level logic system. Translation to MDTL and MTTL levels is obtained by applying 5.0 volts to terminal 13 and leaving pins 4, 9, and 12 open, while translation to MRTL is achieved by applying 3.6 volts to pins 4, 9, and 12. Pin 13 may be left open for use with MRTL. Expander nodes are available on two of the units. Utilizing the expander node, the MC665 may be used as a NAND gate with MHTL input levels and MRTL, MDTL, or MTTL output levels. The MC669 dual 4-input expander used with the expander node allows the translator to function as a multiple input NAND gate.



*Use pin 9 for second translator and pin 12 for third translator.



Positive Logic: $3 = \overline{1 \cdot [2]}$

Negative Logic: $3 = \overline{1 + [2]}$

Input Loading Factor = 1

Output Loading Factor:

MDTL MC830 series = 8

MTTL MC3000 series = 5.5

MRTL MC800P series = 5

Power Dissipation = 83 mW typ/pkg (DTL)
104 mW typ/pkg (RTL)

Propagation Delay Time:

t+- = 30 ns typ

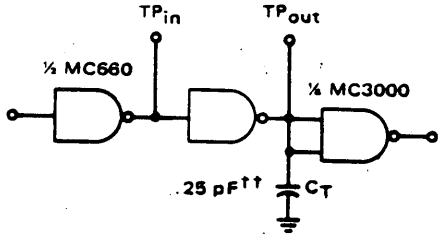
t-+ = 40 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

FIGURE 1

††Total capacitance, including jig, probe, and stray capacitance.

V_{CC} = 15 Vdc on pin 14
V_{CT} = 5 Vdc on pin 13
GND = 7



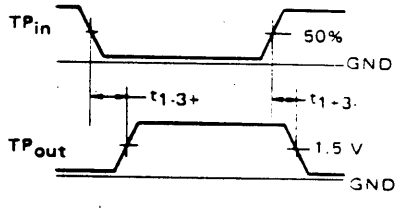
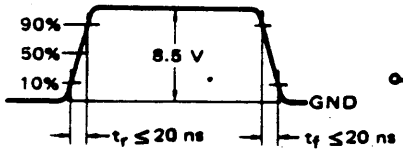
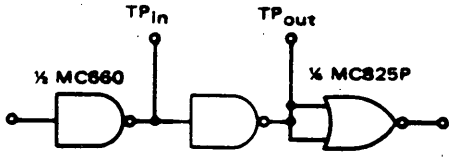


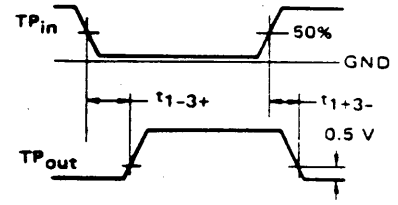
FIGURE 2



f = 500 kHz
DUTY CYLE = 50%



V_{CC} = 15 Vdc on pin 14
V_{CR} = 3.6 Vdc on pin 4
GND = 7

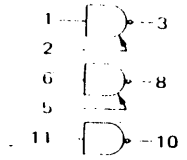


MHTL, MRTL, MDTL, and MTTL are trademarks of Motorola Inc.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one translator.



@ Test Temperature	TEST CURRENT / VOLTAGE VALUES														
	mA		Volts												
	I_{OL}	I_{OH}	V_{IL}	V_{ON}	V_L	V_R	V_X	V_{IH}	V_F	V_{CT}	V_{CR}	V_{CC}	V_{CCL}	V_{CCH}	
−30°C	12.0	-0.5	6.5	1.00	7.0	16.0	7.2	8.5	1.5	5.0	3.6	15.0	14.0	16.0	
+25°C	12.0	-0.5	6.5	0.88	7.0	16.0	7.2	8.5	1.5	5.0	3.6	15.0	14.0	16.0	
+75°C	12.0	-0.5	6.5	0.79	7.0	16.0	7.2	8.5	1.5	5.0	3.6	15.0	14.0	16.0	

Characteristic	Symbol	Pin Under Test	MC665 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{ON}	V_L	V_R	V_X	V_{IH}	V_F	V_{CT}	V_{CR}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	0.4	-	0.4	-	0.5	Vdc	3	-	-	-	-		-	1	-	13			14		7
		3	-	0.29	-	0.26	-	0.34	Vdc	-	-	-	-	-		-	1	-	-	4		14		7
	V_{OH}	3	3.0	-	3.1	-	3.15	-	Vdc	-	3	1		-	-			-	13			14		7
		3	3.0	-	3.1	-	3.15	-	Vdc	-	3	-		-		2		-	13			14		7
	V_{CEX}	3	6.75	-	6.75	-	6.75	-	Vdc	-			-	13		-		-					14	1,7
Short-Circuit Current	I_{SC}	3	-1.75	-3.25	-1.75	-3.25	-1.75	-3.25	mAdc	-	-		-	-	-			-	13				14	1,3,6,7,11
		3	-3.9	-7.3	-3.9	-7.3	-3.9	-7.3	mAdc	-	-		-	-	-			-	-	4,9,12	-		14	1,3,6,7,11
Reverse Current	I_R	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-			13	-	-		14	2,7
Output Current	I_{A5}	3	-3.00	-	-3.00	-	-2.85	-	mAdc	-	-	1	3	-			-	-		4	-	14	-	7
Forward Current	I_F	1	-	-1.2	-	-1.2	-	-1.2	mAdc	-	-	-	-	-	-	-	-	1	13	-		-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	3.9	-	-	mAdc	-	-	-	-	-	-	-	-	-	13	-		-	14	1,6,7,11
	I_{CCH}	14	-	-	-	9.5	-	-		-	-	-	-	-	-	-	-	-	13	-		-	-	7
	I_{CTH}	13	-	-	-	9.4	-	-		-	-	-	-	-	-	-	-	-	13			-	-	
	I_{CRH}	4,9,12	-	-	-	20.7	-	-		-	-	-	-	-	-	-	-	-	-	4,9,12		-	-	
Switching Times	t_{1+3-}*	3	-	-	-	100	-	-	ns	Pulse In: 1	Pulse Out: 3	-	-	-	-	-	-	-	13	-	14	-	-	7
	t_{1-3+}*		-	-	-	150	-	-				-	-	-	-	-	-	-	13			-	-	
	t_{1+3-}†		-	-	-	125	-	-				-	-	-	-	-	-	-	-	4				
	t_{1-3+}†		-	-	-	175	-	-				-	-	-	-	-	-	-	-	4				

*To perform the test, see figure 1.
†To perform the test, see figure 2.
Pins not listed are left open.

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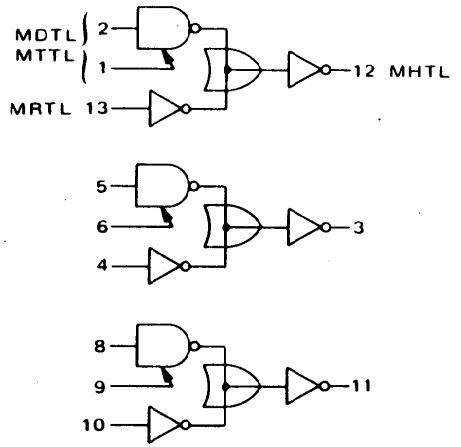
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one translator.



@ Test Temperature	TEST CURRENT/VOLTAGE VALUES											
	mA		Volts									
	I_{OL}	I_{OH}	V_{IL}	V_{ON}	V_{OFF}	V_X	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}
−30°C	12.0	-0.03	1.1	1.20	0.570	-	2.1	0	4.0	-	14.0	16.0
+25°C	12.0	-0.03	1.1	0.880	0.500	1.8	1.9	0	4.0	15.0	14.0	16.0
+75°C	12.0	-0.03	0.9	0.855	0.450	-	1.8	0	4.0	-	14.0	16.0

Characteristic	Symbol	Pin Under Test	MC666 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{ON}	V_{OFF}	V_X	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	12	-	1.5	-	1.5	-	1.5	Vdc	12	-	2	-	13	-	-	-	-	-	14	-	7
		12	-	-	-	1.5	-	-		12	-	-	-	-	1	-	-	-	-		-	7,13
	V_{OH}	12	12.5	-	12.5	-	12.5	-		-	12	-	-	13	-	2	-	-	-		-	7
		12	12.5	-	12.5	-	12.5	-		-	12	2	13	-	-	-	-	-	-		-	7
Short-Circuit Current	I_{SC}	12	-6.5	-15.0	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	2	-	-	-	-	14	7,12,13
Reverse Current	I_R	2	-	5.0	-	5.0	-	10.0	μAdc	-	-	-	-	-	-	-	-	2	-	14	-	7,13
Output Leakage Current	I_{CEX}	12	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	2	-	-	-	-	12,14	7,13
Forward Current	I_F	2	-	-1.5	-	-1.4	-	-1.33	mAdc	-	-	-	-	-	-	-	2	-	-	-	14	7,13
Input Current	I_{in}	13	-	150	-	150	-	150	μAdc	-	-	-	13	-	-	-	-	2	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	12.4	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	-	14	2,4,5,7,8,10,13
	I_{CCH}	14	-	-	-	8.0	-	-	mAdc	-	-	-	4,10,13	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out											
	t_{2+12+}	2,12	-	-	-	200	-	-	ns	2	12	-	-	13	-	-	-	-	14	-	-	7
	t_{2-12-}	2,12	-	-	-	100	-	-		2		-	-	13	-	-	-	-		-	-	
	t_{13+12+}	12,13	-	-	-	200	-	-		13		2	-	-	-	-	-	-		-	-	
	t_{13-12-}	12,13	-	-	-	100	-	-		13		2	-	-	-	-	-	-		-	-	

Pins not listed are left open.

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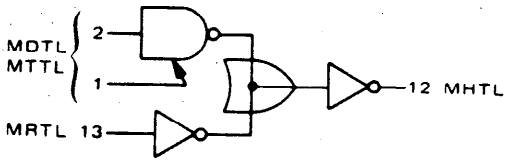
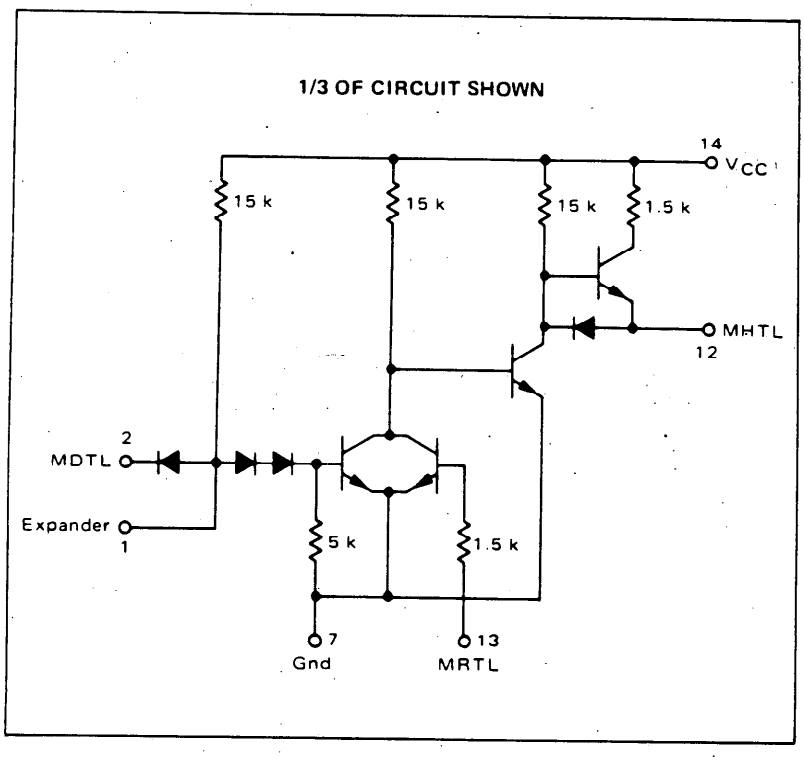
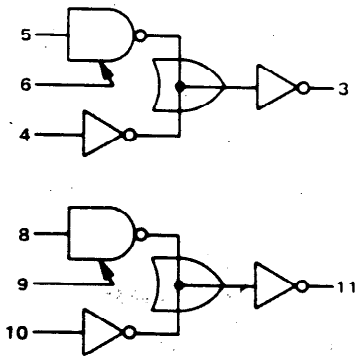
MC666

ISSUE A

This device is a triple unit that translates MRTL, MDTL, and MTTL logic signals to MHTL logic levels. Each unit is divided into two sections, one capable of handling MRTL signals and the other operating from MDTL and MTTL signals. The second section also has an expander node available which, in addition to the normal expander function, allows the usage of high voltage diodes to translate from high voltage circuits. The input associated with the unused section should be grounded for proper operation of the active section.







Positive Logic: $12 = 2 \cdot [1] + 13$

Negative Logic: $12 = (2 + [1]) \cdot 13$

Input Loading Factor:

- **MDTL MC830 series = 1.0**
- **MTTL MC3000 series = 0.8**
- **MRTL MC800P series = 1.0**

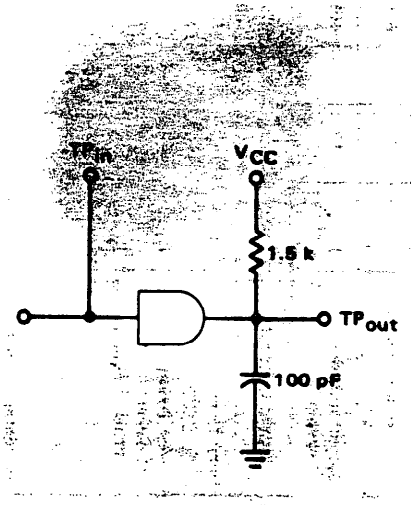
Output Loading Factor = 10

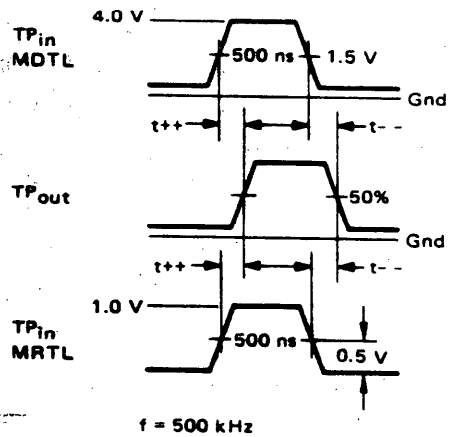
Total Power Dissipation = 105 mW typ/pkg

Propagation Delay Time:

- **t++ = 75 ns typ**
- **t- - = 35 ns typ**

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





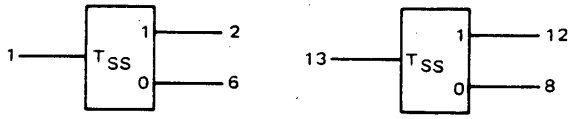
f = 500 kHz

MHTL, MTTL, MRTL, and MDTL are trademarks of Motorola Inc.

See General Information section for packaging.

MC667

NOVEMBER 1970



Input Loading Factor = 1
Output Loading Factor = 10
Total Power Dissipation = 240 mW typ

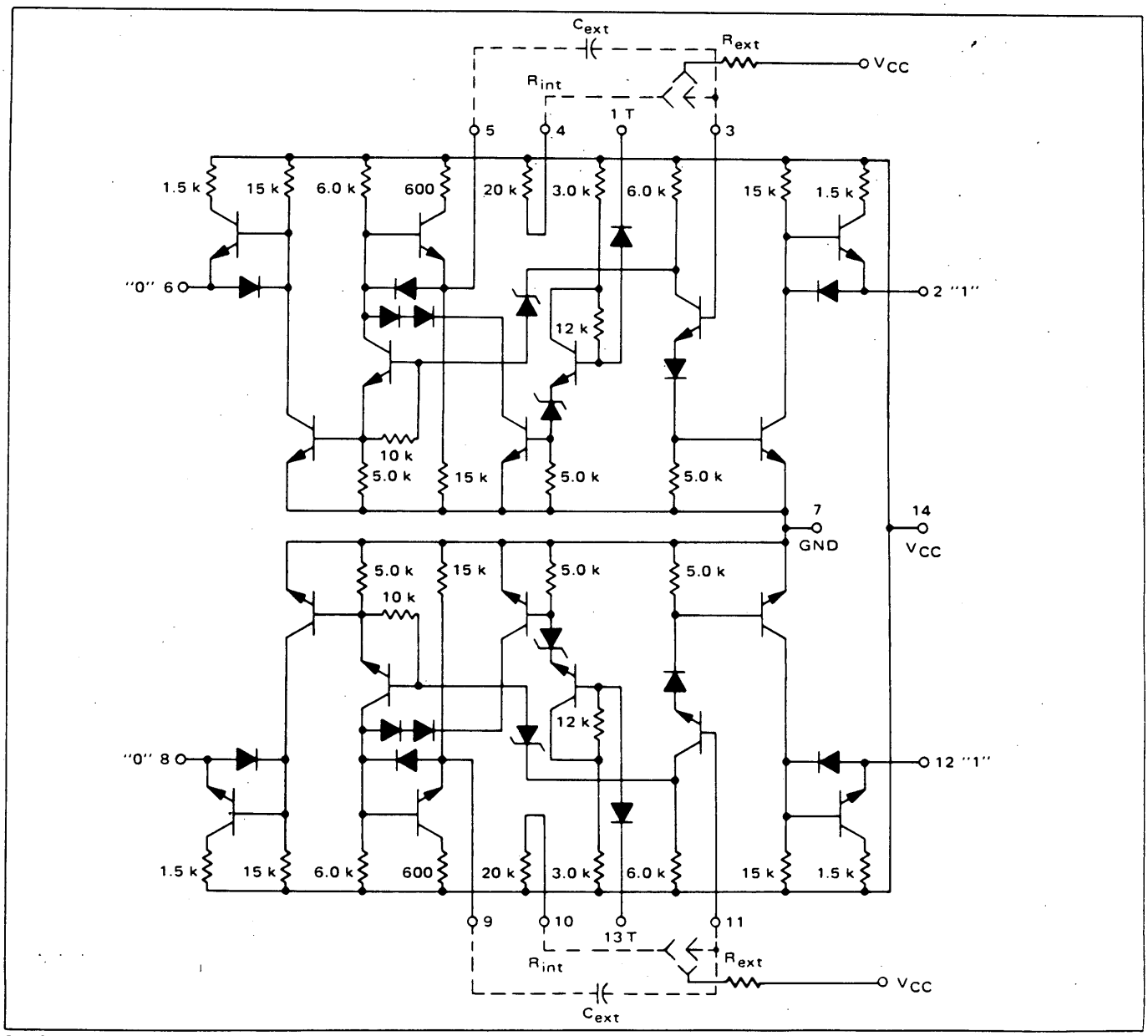
An internal timing resistor is provided at pin 4(10).

An external timing resistor may be connected between V_{CC} and pin 3(11) instead of using pin 4(10).

A timing capacitor is connected between pins 3(11) and 5(9). (See circuit schematic.)

The MC667 is a dual monostable multivibrator whose output pulse width is independent of input pulse width. The device is triggered on the rising edge of a pulse to the toggle input, and the output pulse width is determined by the R-C timing network. Circuit operation is described on Page 7 of Application Note 467.

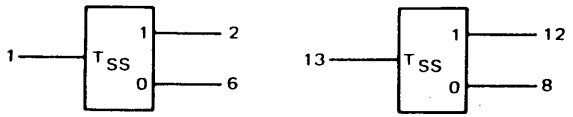
Each multivibrator in the package has both true logic "1" and complement logic "0" outputs available. A positive-going pulse is available at the logic "1" output, and the inverted pulse is available at the logic "0" output. Outputs utilize active pullup circuits to minimize output impedance.



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

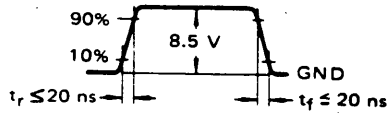
Test procedures are shown for only one monostable multivibrator. The other monostable multivibrator is tested in the same manner.



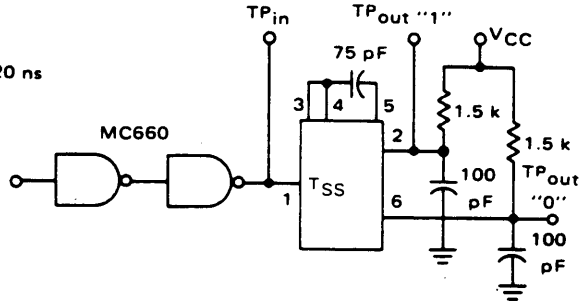
Characteristic	Symbol	Pin Under Test	MC667 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	I_{in}	Volts V_{IL}	V_{IH}	V_F	V_R	V_{RX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
										12.0	-0.03	0.2	6.50	8.50	1.5	16.0	-13	15.0	14.0	16.0	
										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											
Output Voltage	V_{OL}	2	-	1.5	-	1.5	-	1.5	Vdc	2	-	3	-	-	-	-	-	-	14	-	7
		5†	-	2.8	-	2.8	-	2.8		-	-	3	-	1	-	-	-	-		-	7
		5†	-	2.1	-	2.1	-	2.1		-	-	-	-	-	-	-	-	-		-	1,3,7
		6	-	1.5	-	1.5	-	1.5		6	-	-	1	-	-	-	-	-		-	3,7
	V_{OH}	2	12.5	-	12.5	-	12.5	-		-	2	-	-	-	-	-	-	-		-	1,3,7
		5*	12.8	-	12.8	-	12.8	-		-	-	-	1	-	-	-	-	-		-	7
		6	12.5	-	12.5	-	12.5	-		-	6	3	-	-	-	-	-	-		-	1,7
Short-Circuit Current	I_{SC}	2	-6.5	-15	-6.5	-15	-6.5	-15	mAdc	-	-	-	-	-	-	-	-	-	-	14	2,3,7
		4	-0.64	-1.07	-0.64	-1.07	-0.64	-1.07		-	-	-	-	-	-	-	-	-	-		4,7
		5*	-19	-40	-19	-40	-19	-40		-	-	-	-	-	-	-	-	-	-		1,5,7
		6	-6.5	-15	-6.5	-15	-6.5	-15		-	-	3	-	-	-	-	-	-	-		6,7
Reverse Current	I_{R1}	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	-	1	-	-	-	14	7
	I_{R2}	3	-	-2.0	-	-2.0	-	-2.0	μAdc	-	-	-	-	-	-	-	3	-	-	14	7
Output Leakage Current	I_{CEX}	2	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	-	-	-	2,14	3,7
		6*	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	-	-	-	-	6,14	7
Forward Current	I_F	1	-	1.2	-	1.2	-	1.2	mAdc	-	-	-	-	-	1	-	-	-	-	14	7
Power Drain Current (Both Units)	I_{CCL}	14	-	-	-	17.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	14	1,3,7,11,13
	I_{CCH}	14*‡	-	-	-	23	-	-	mAdc	-	-	-	-	-	-	-	-	-	-	1,13,14	7
										Pulse In	Pulse Out										
Switching Times	t_{1+2-}	2	-	-	-	275	-	-	ns	1	2	-	-	-	-	-	-	14	-	-	7
	t_{1+6-}	6	-	-	-	75	-	-	ns	1	6	-	-	-	-	-	-	14	-	-	7

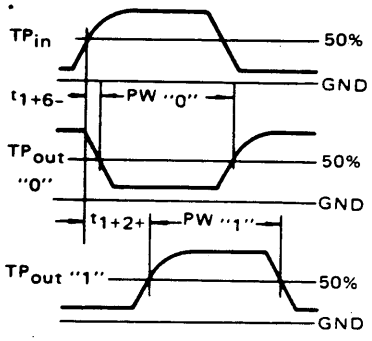
Pins not listed are left open.
*Pin 4 connected to pin 3
†Pin 4 connected to pin 5
‡Pin 11 connected to pin 10

SWITCHING TIME TEST CIRCUIT, WAVEFORMS AND DEFINITIONS



f = 500 kHz
DUTY CYCLE = 50%





Pulse Width: $PW_{"1"} \approx 0.7\ R_T\ C_T - 125 \times 10^{-9}$
$PW_{"0"} \approx 0.7\ R_T\ C_T + 125 \times 10^{-9}$
R_T in ohms, C_T in farads

C_T and R_T are timing resistor and capacitor.

Recovery Time: $t_R = 3\ C_T \times 10^3$ (t_R in seconds, C_T in farads)

Duty Cycle: $DC \approx \frac{PW \times (100)}{PW + t_R} \approx \frac{R_T \times (100)}{R_T + 4.5}$

R_T in ohms

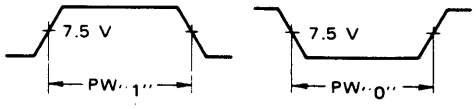
External Timing Resistor: $5.0\ k\Omega \leq R_{ext} \leq 56\ k\Omega$

APPLICATION INFORMATION

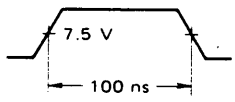
Circuit Operation

1. Any value of external capacitor (C_{ext}) may be used for the timing circuit. If an external resistor is used (20 kΩ internal is provided), $5.0\ k\Omega \leq R_{ext} \leq 56\ k\Omega$.
2. The generated pulse width (PW) is calculated as follows:

$PW_{"1"} \approx 0.7\ R_T\ C_T - 125 \times 10^{-9}$
$PW_{"0"} \approx 0.7\ R_T\ C_T + 125 \times 10^{-9}$
R_T in ohms, C_T in farads



3. Input pulse width may be as narrow as 100 ns.

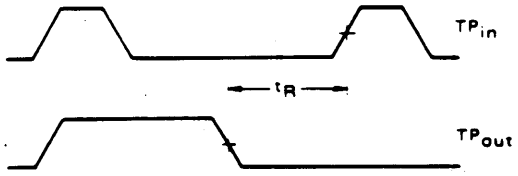


4. Sufficient recovery time must be allowed between input and output pulses. Recovery time is that period of time which the multivibrator requires for the capacitor to reach its quiescent state after triggering. Recovery time begins after the end of the output

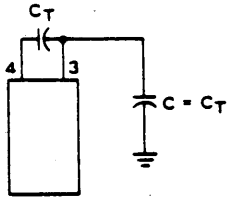
TYPICAL APPLICATIONS (continued)

pulse or the return of the input to the zero state, depending upon which occurs later.

$t_R = 3\,C_T \times 10^3$ t_R in seconds, C_T in farads

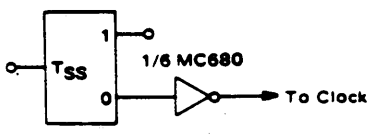


5. Although the toggle input displays the 5.0 volt noise margins of MHTL, the MC667 is susceptible to negative-going noise on the R-C timing network. False triggering may be caused by a negative-going spike of 1.5 volts or greater. V_{CC} should be bypassed at the package by a capacitor if false triggering occurs. Also, a capacitor equal to C_T connected from pin 3 (pin 11 for second multivibrator) to ground will improve noise immunity. The output pulse width will not be significantly affected.

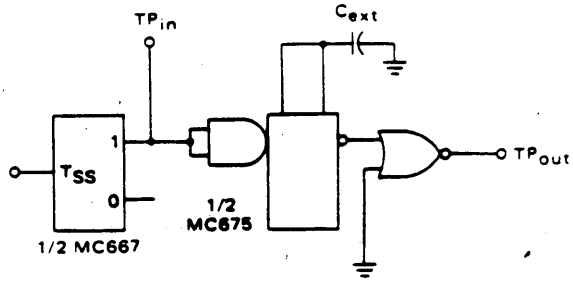


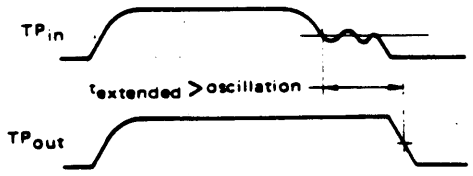
6. If the output pulse width is approximately 0.25 ms or greater, the logic "1" output fall time will be greater than 1.0 μs. If the logic "1" output is used to clock a flip-flop, this long fall time may cause improper toggling due to noise or oscillation on the clock line. Several solutions to this problem are shown.

   A. Use of the logic "0" output inverted. Rise and fall times of the logic "0" output are typically less than 0.5 μs.

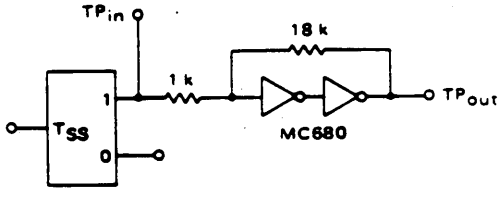


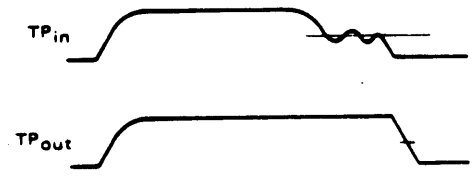
B. Let the output of the MC667 drive 1/2 MC675 pulse stretcher. The pulse stretcher extends the pulse width beyond the oscillation and gives a sharp fall time to the pulse. A typical value of C_{ext} (for the pulse stretcher) is 50 pF.





C. Let the output of the MC667 drive two active pullup inverters (MC680) or gates connected as a Schmitt Trigger. The trigger goes from the high to the low state at a threshold of approximately 6.5 volts. The oscillation then appears at a voltage level above the threshold of the Schmitt Trigger. Also, the hysteresis action of the network helps prevent oscillation from retriggering the Schmitt Trigger and gives sharp rise and fall time at TP_{out}.





TYPICAL APPLICATIONS (continued)

Application Ideas

The configuration shown in Figure 1 is a gated astable multivibrator. Pulse widths may be varied by changing time constants "t_1" and "t_2".

A sequential pulse train may be generated as shown in Figure 2. The timing diagram shows an approximate delay of 250 ns between pulses. Any pulse width in the train must be of sufficient length to allow proper recovery time of the multivibrator following that pulse.

FIGURE 1 – GATED ASTABLE MULTIVIBRATOR

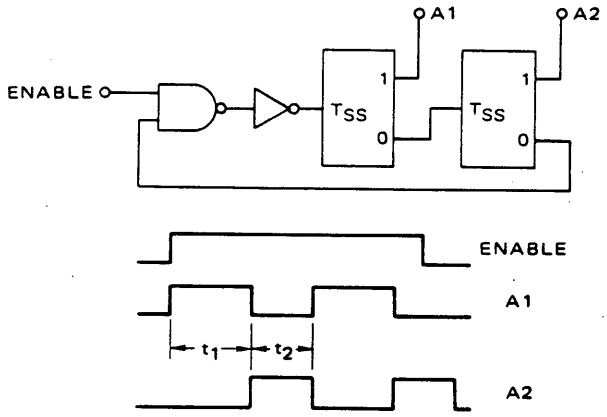
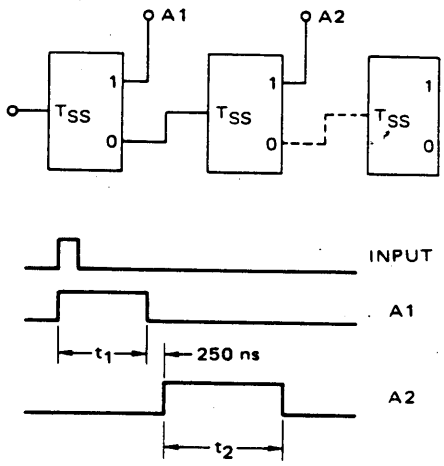


FIGURE 2 – GENERATION OF A SEQUENTIAL PULSE TRAIN



TYPICAL CHARACTERISTICS

FIGURE 3 – OUTPUT PULSE WIDTH versus CAPACITANCE

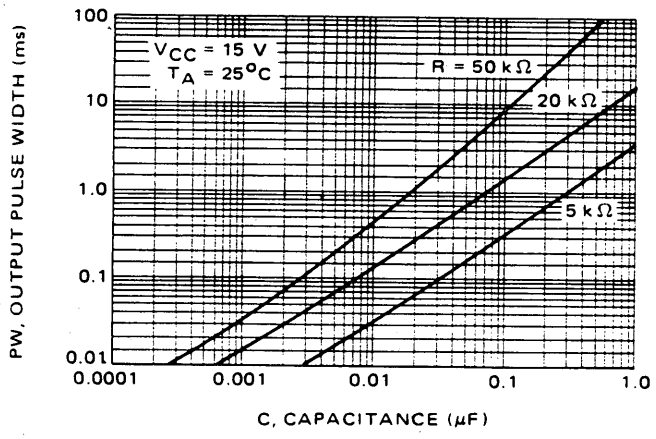
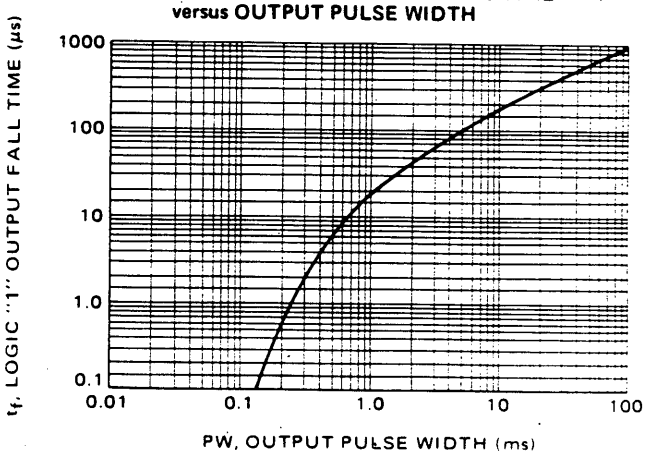


FIGURE 4 – LOGIC "1" OUTPUT FALL TIME versus OUTPUT PULSE WIDTH



TYPICAL CHARACTERISTICS (continued)

FIGURE 5 – RECOVERY TIME versus CAPACITANCE

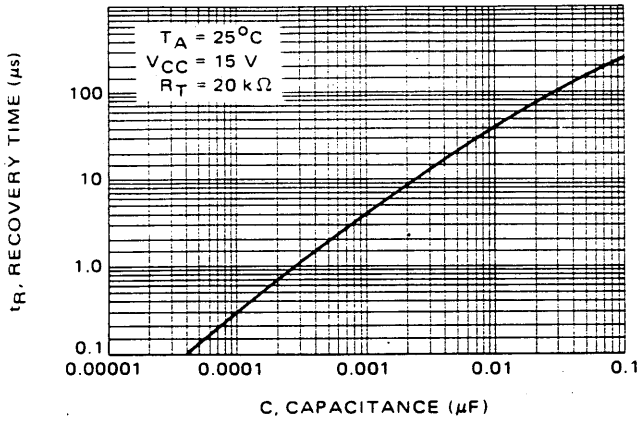


FIGURE 6 – NORMALIZED RECOVERY TIME versus TEMPERATURE

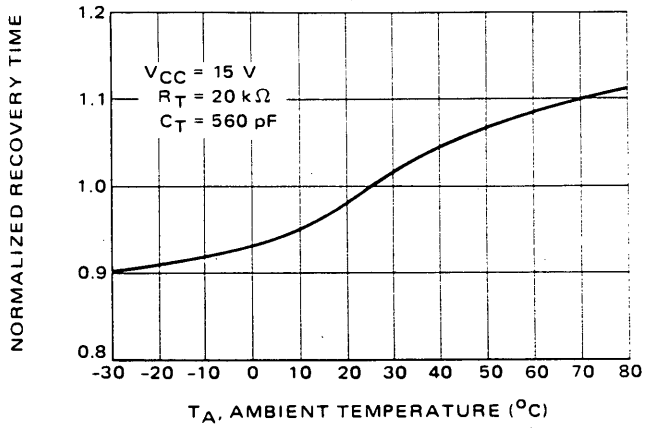


FIGURE 7 – NORMALIZED OUTPUT PULSE versus SUPPLY VOLTAGE

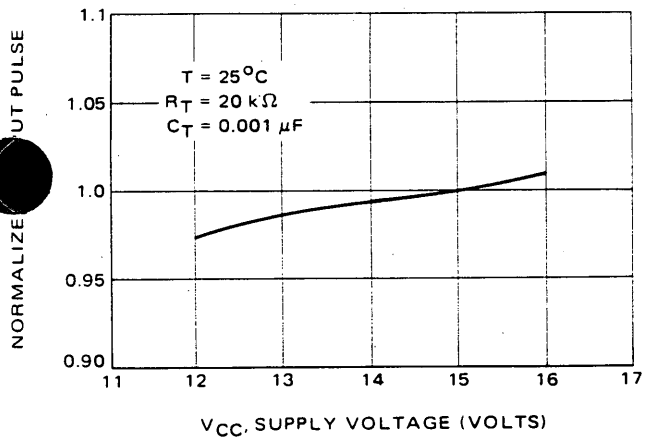
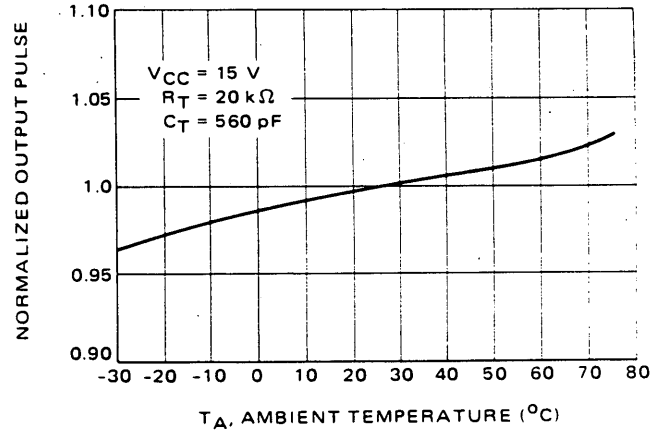
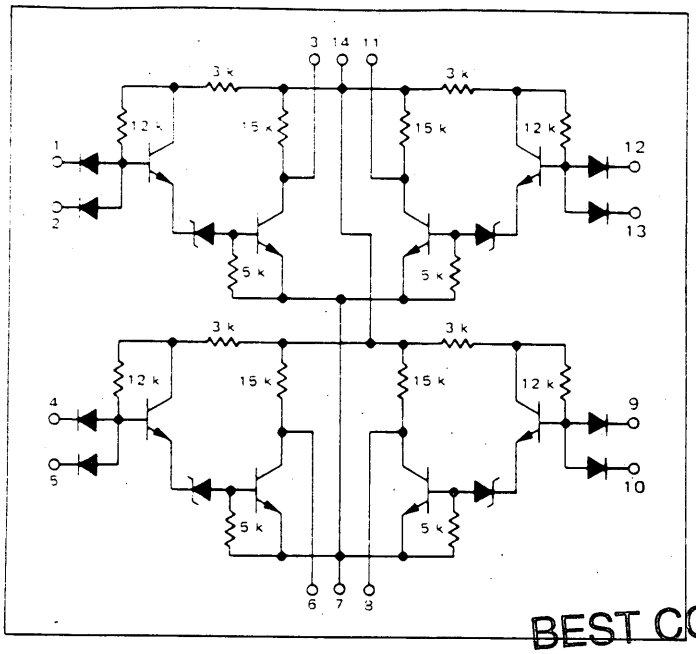


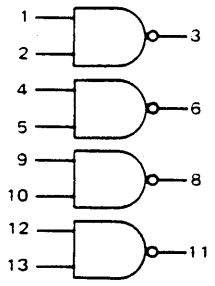
FIGURE 8 – NORMALIZED OUTPUT PULSE versus TEMPERATURE



MC668



This device consists of four 2-input NAND gates with passive output pullup.



Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High = 176 mW typ/pkg
Input Low = 52 mW typ/pkg

ELECTRICAL CHARACTERISTICS

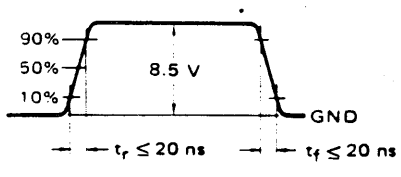
Test procedures are shown for only one gate. The other gates are tested in the same manner.

			TEST CURRENT VOLTAGE VALUES (All Temperatures)										
			mA		Volts								
			I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
			12.0	-0.03	0.50	3.50	1.5	16.0	16.0	15	14	14	

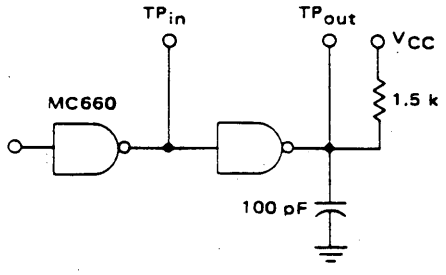
Characteristic	Symbol	Pin Under Test	MC668 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3	-	2	1.2	-	-	-	-	14	-	-
	V_{OH}	3	-	-	12.5	-	12.5	-	V	-	3	1	-	-	-	-	2	14		
		3	-	-	12.5	-	12.5	-		-	3	2	-	-	-	-	1	14		
Short-Circuit Current	I_{SC}	3	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	-
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	-
		2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	-	-	14	-	-
Output Leakage Current	I_{CEX}	3	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	2.14	-	-	-	-
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2	-	-	-	14	-
		2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	1	-	-	-	14	-
Power Drain Current	I_{CCL}	14	-	-	-	6.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-
Power Drain Current	I_{CCH}	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-
Switching Times										Pulse In	Pulse Out									
	t_{1-3-}	3	-	-	-	250	-	-	ns	1	3	-	-	-	-	-	14	-	-	-
	t_{1-3-}	3	-	-	-	100	-	-	ns	1	3	-	-	-	-	-	14	-	-	-

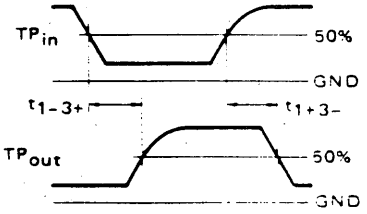
Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



f = 500 kHz
DUTY CYCLE = 50%





See General Information section for packaging.

MOTOROLA Semiconductor Products Inc.

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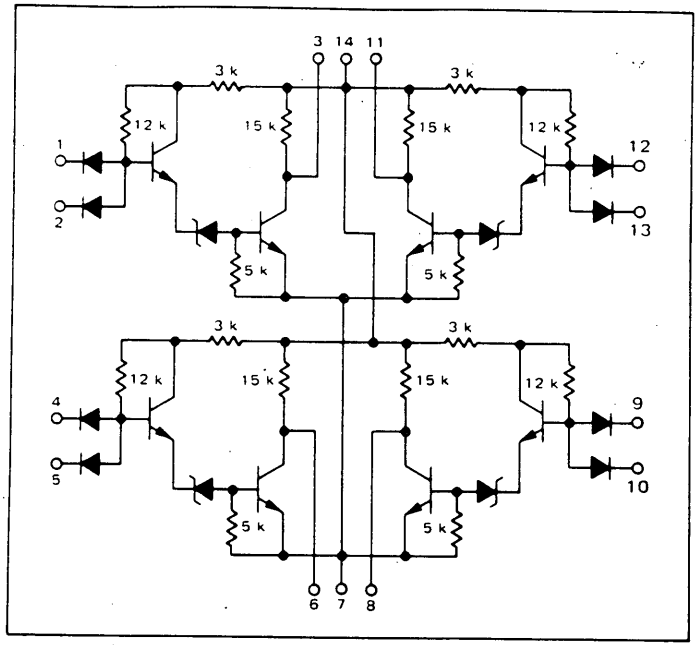
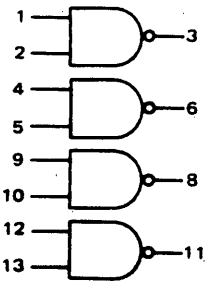
MC668

ISSUE A



This device consists of four 2-input NAND gates with passive output pullup.



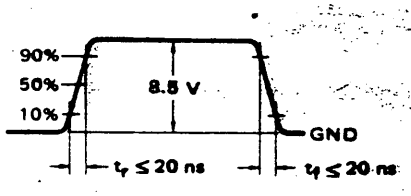
Positive Logic: $3 = \overline{1 \cdot 2}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High = 176 mW typ/pkg
Input Low = 52 mW typ/pkg

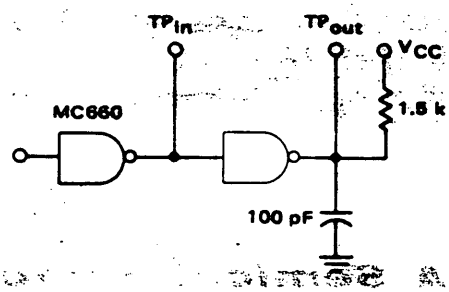
			MC668 Test Limits							TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
			−30°C		+25°C		+75°C			mA		Volts								
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3	-	-	1.2	-	-	-	-	14	-	7
	V_{OH}	3	-	-	12.5	-	12.5	-	↓	-	3	1	-	-	-	-	2	14	-	
		3	-	-	12.5	-	12.5	-		-	3	2	-	-	-	-	1	14	-	↓
Short-Circuit Current	I_{SC}	3	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	1,3,7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	2,7
		2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	-	-	14	-	1,7
Output Leakage Current	I_{CEX}	3	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	3,14	-	-	-	1,7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2	-	-	-	14	7
		2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	1	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	6.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,4,5,7, 9,10,12,13
	I_{CCH}	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{1-3+}	3	-	-	-	250	-	-	ns	1	3	-	-	-	-	-	14	-	-	7
	t_{1-3-}	3	-	-	-	100	-	-	ns	1	3	-	-	-	-	-	14	-	-	7

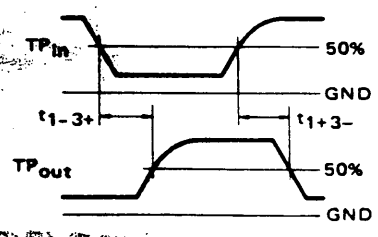
Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



f = 500 kHz
DUTY CYCLE = 50%





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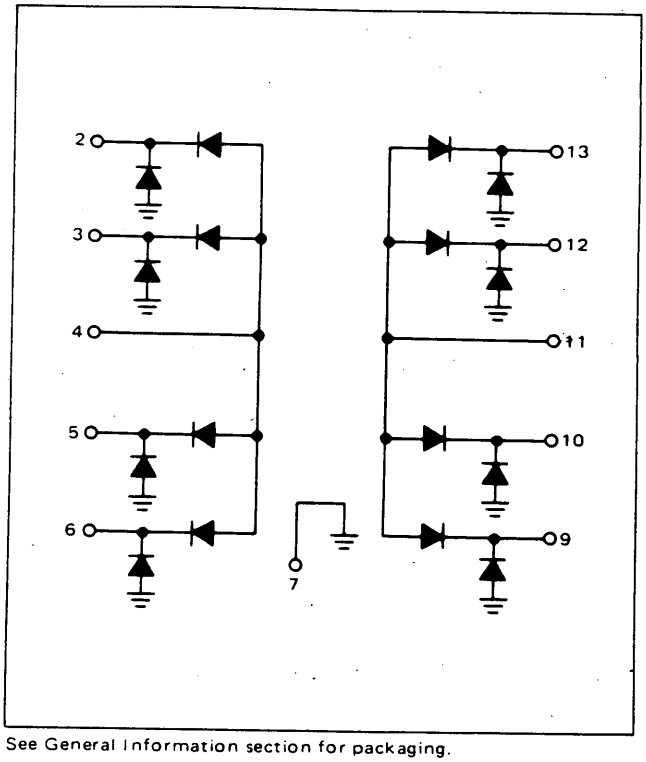
MOTOROLA Semiconductor Products Inc.

BOX 20912 • PHOENIX ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC

3073-44 PRINTED IN U.S.A. 9-73 IMPERIAL LITHO 83746 10M

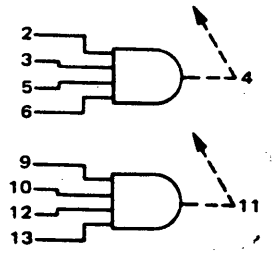
MC669

ISSUE A



See General Information section for packaging.

This device consists of two independent high voltage diode networks with characteristics matched to the input of the gate and buffer elements in the MHTL logic family. Its use increases the fan-in capability of other MHTL devices to a maximum of 20 while having negligible effect on their performance.



Positive Logic: $4 = \overline{2 \cdot 3 \cdot 5 \cdot 6}$

Input Loading Factor = 1

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one expander. The other expander is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC669 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_F	V_R	Gnd
										TEST CURRENT / VOLTAGE VALUES (All Temperatures) mA I_F	Volts V_R	
										1.2	16.0	
Forward Voltage	V_F	4	-	1.1	-	1.0	-	0.9	Vdc	4	-	2,7
			-		-		-				-	3,7
			-		-		-				-	5,7
			-		-		-				-	6,7
Reverse Current	I_R	2	-	2.0	-	2.0	-	2.0	μAdc	-	2	3,5,6,7
		3	-		-		-			-	3	2,5,6,7
		5	-		-		-			-	5	2,3,6,7
		6	-		-		-			-	6	2,3,5,7
	$2\,I_R$	4	-	-	-	4.0	-	-		-	4	7

Pins not listed are left open

MOTOROLA Semiconductor Products Inc.

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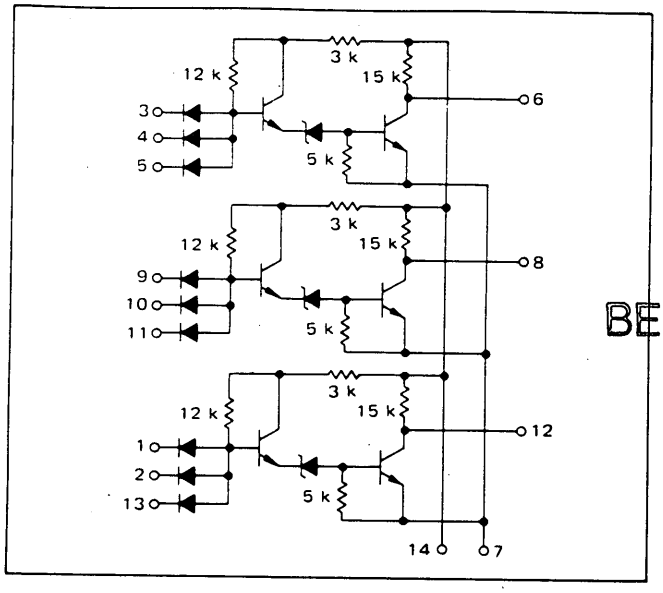
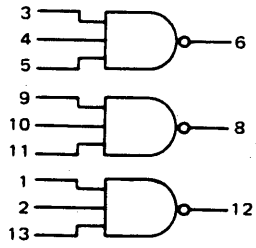
MC670



This device consists of three 3-input NAND gates with passive output pullup.



Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High = 132 mW typ/pkg
Input Low = 39 mW typ/pkg

ELECTRICAL CHARACTERISTICS

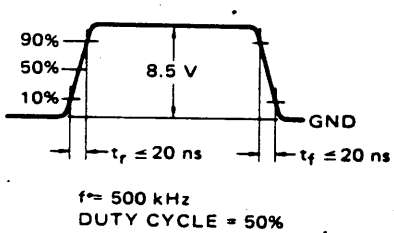
Test procedures are shown for only one gate. The other gates are tested in the same manner.

TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
mA		Volts							
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}
12.0	-0.03	0.50	3.50	1.5	16.0	16.0	15.0	14.0	16.0

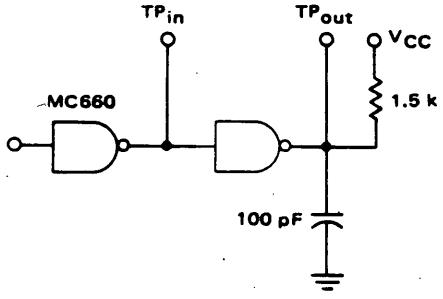
Characteristic	Symbol	Pin Under Test	MC670 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	3,4,5	-	-	-	-	14	-	7
	V_{OH}	6	-	-	12.5	-	12.5	-		-	6	3	-	-	-	-	4.5	14	-	
			-	-		-		-		-		4	-	-	-	-	3.5		-	
		▼	-	-	▼	-	▼	-	▼	-	▼	5	-	-	-	-	3.4	▼	-	▼
Short-Circuit Current	I_{SC}	6	-	-	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	3,6,7
Reverse Current	I_R	3	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	3	-	-	14	-	4,5,7
		4	-	-	-		-			-	-	-	-	-	4	-	-		-	3,5,7
		5	-	-	-	▼	-	▼	▼	-	-	-	-	-	5	-	-	▼	-	3,4,7
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	6,14	-	-	-	3,7
Forward Current	I_F	3	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	3	4.5	-	-	-	14	7
		4	-	-	-		-			-	-	-	-	4	3.5	-	-	-		
		5	-	-	-	▼	-	▼	▼	-	-	-	-	5	3.4	-	-	-	▼	▼
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	4.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,7,9,10,11,13
	I_{CCH}	14	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{3-6+}	6	-	-	-	250	-	-	ns	3	6	-	-	-	-	-	14	-	-	7
	t_{3-6-}	6	-	-	-	100	-	-	ns	3	6	-	-	-	-	-	14	-	-	7

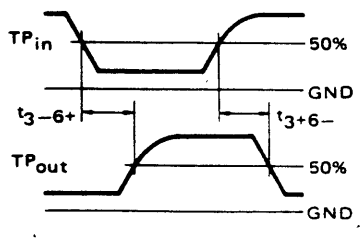
Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



f = 500 kHz
DUTY CYCLE = 50%





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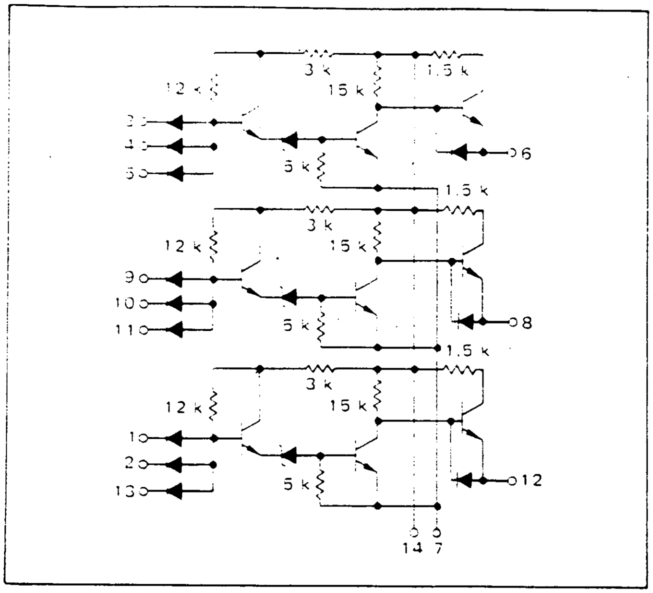
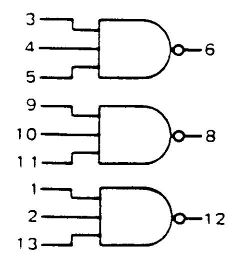
3073-40 PRINTED IN USA 9-72 IMPERIAL LITHO 831778 8M

MC671



This device consists of three 3-input NAND gates with active output pullup.



Positive Logic: $6 = \overline{3 \cdot 4 \cdot 5}$

Input Loading Factor = 1
Output Loading Factor = 10

Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High = 132 mW typ/pkg
Input Low = 39 mW typ/pkg

BEST COPY

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc
	V_{OH}	6	-	-	12.5	-	12.5	-	Vdc
			-	-		-		-	
		▼	-	-	▼	-	▼	-	▼
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdc
Reverse Current	I_R	3	-	-	-	2.0	-	2.0	µAdc
		4	-	-	-		-		
		5	-	-	-	▼	-	▼	▼
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	µAdc
Forward Current	I_F	3	-	-	-	-1.20	-	-1.20	mAdc
		4	-	-	-		-		
		5	-	-	-	▼	-	▼	▼
Power Drain Current Total Device	I_{CCL}	14	-	-	-	4.5	-	-	mAdc
	I_{CCH}	14	-	-	-	15	-	-	mAdc
Switching Times									
	t_{3-6-}	6	-	-	-	200	-	-	ns
	t_{3-6-}	6	-	-	-	100	-	-	ns

TEST CURRENT/VOLTAGE VALUES (All Temperatures)

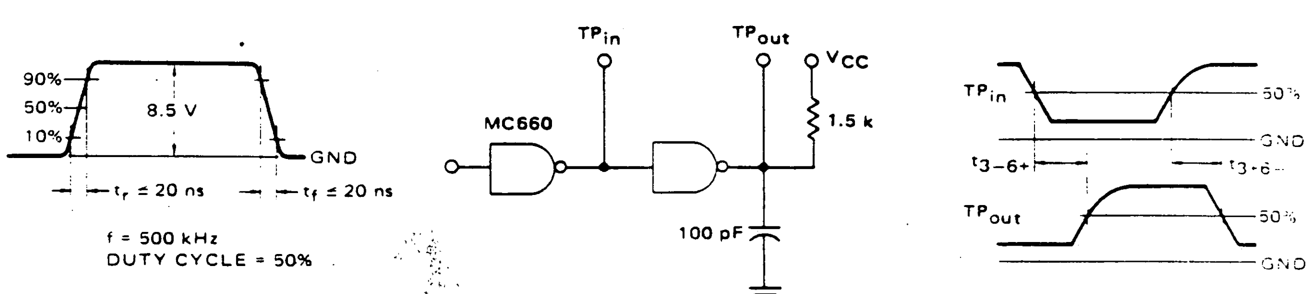
I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}
12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15	14	[illegible]

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:

Symbol	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
V_{OL}	6	-	-	3, 4, 5	-	-	-	-	14	-	-
V_{OH}	-	6	3	-	-	-	-	4, 5, [illegible]	14		
	-		4	-	-	-		[illegible]			
	-	▼	5	-	-	-		[illegible]	▼		▼
I_{SC}	-	-	-	-	-	-		-		14	
I_R	-	-	-	-	-	3	-	-	14		
	-	-	-	-	-	4	-	-			
	-	-	-	-	-	5	-	-	▼		
I_{CEX}	-	-	-	-	-	-	6, 14	-	-		
I_F	-	-	-	-	3	4, 5	-	-	-	14	
	-	-	-	-	4	3, 5	-				
	-	-	-	-	5	3, 4	-	-		▼	▼
I_{CCL}	-	-	-	-	-	-				14	
I_{CCH}	-	-	-	-	-	-	-	-		14	
Switching Times	Pulse In	Pulse Out									
t_{3-6-}	3	6	-	-	-	-	-	14			-
t_{3-6-}	3	6	-	-	-	-	-	14		-	-

Pins not listed are left open.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



See General Information section for packaging.

MOTOROLA Semiconductor Products Inc.

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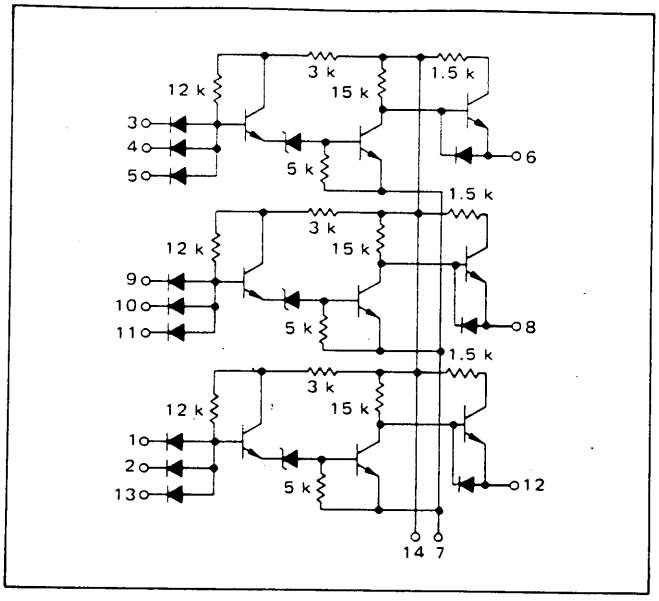
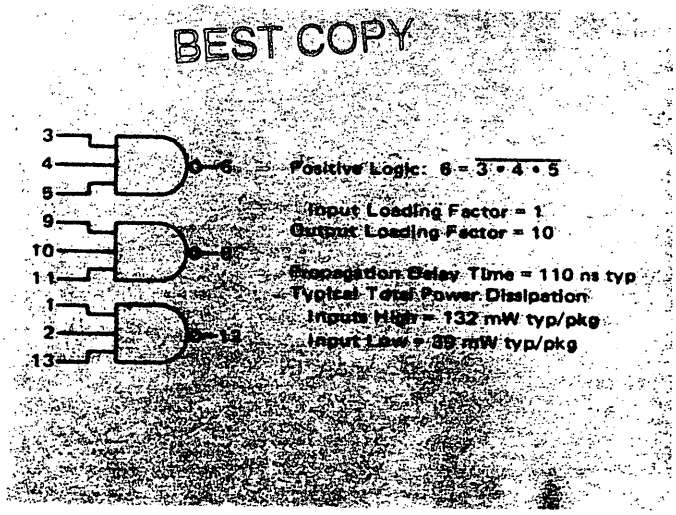
MC671

ISSUE A



This device consists of three 3-input NAND gates with active output pullup.



ELECTRICAL CHARACTERISTICS

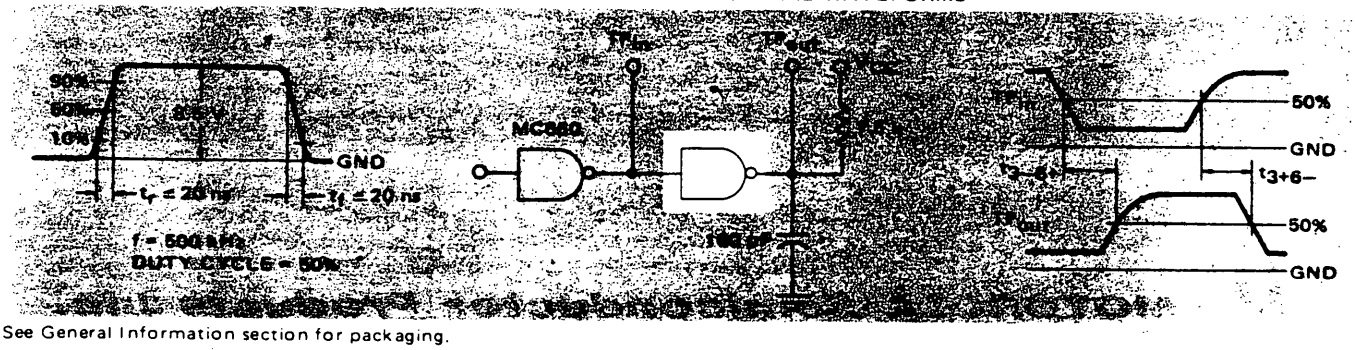
Test procedures are shown for only one gate. The other gates are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC671 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc
	V_{OH}	6	-	-	12.5	-	12.5	-	Vdc
		↓	-	-	↓	-	↓	-	↓
Short-Circuit Current	I_{SC}	6	-	-	-6.5	-15.0	-6.5	-15.0	mAdc
Reverse Current	I_R	3	-	-	-	2.0	-	2.0	μAdc
		4	-	-	-	↓	-	↓	↓
		5	-	-	-		-		
Output Leakage Current	I_{CEX}	6	-	-	-	100	-	100	μAdc
Forward Current	I_F	3	-	-	-	-1.20	-	-1.20	mAdc
		4	-	-	-	↓	-	↓	↓
		5	-	-	-		-		
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	4.5	-	-	mAdc
	I_{CCH}	14	-	-	-	15	-	-	mAdc
Switching Times									
	t_{3-6-}	6	-	-	-	200	-	-	ns
	t_{3-6-}	6	-	-	-	100	-	-	ns

TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
mA		Volts								
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
6	-	-	3,4,5	-	-	-	-	14	-	7
-	6	3	-	-	-	-	4,5	14	-	
-	↓	4	-	-	-	-	3,5		-	
-		5	-	-	-	-	3,4	↓	-	↓
-	-	-	-	-	-	-	-	-	14	3,6,7
-	-	-	-	-	3	-	-	14	-	4,5,7
-	-	-	-	-	4	-	-		-	3,5,7
-	-	-	-	-	5	-	-	↓	-	3,4,7
-	-	-	-	-	-	6,14	-	-	-	3,7
-	-	-	-	3	4,5	-	-	-	14	7
-	-	-	-	4	3,5	-	-	-		
-	-	-	-	5	3,4	-	-	-	↓	↓
-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,7, 9,10,11,13
-	-	-	-	-	-	-	-	-	14	7
Pulse In	Pulse Out									
3	6	-	-	-	-	-	14	-	-	7
3	6	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

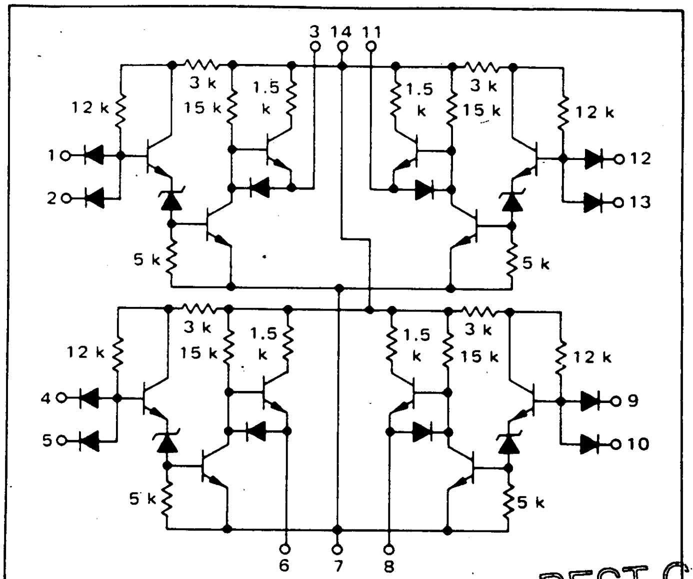
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



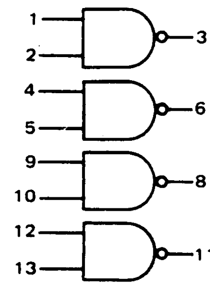
See General Information section for packaging.

MC672

ISSUE A



This device consists of four 2-input NAND gates with active output pullup.



Positive Logic: $3 = \overline{1 \bullet 2}$
Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High = 176 mW typ/pkg
Input Low = 52 mW typ/pkg

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ELECTRICAL CHARACTERISTICS

Test procedures shown are for one gate only. The other gates are tested in the same manner.

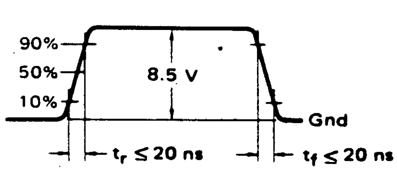
TEST CURRENT/VOLTAGE VALUES (All Temperatures)

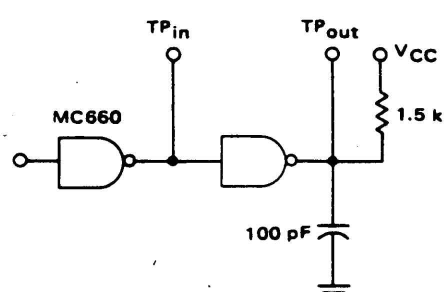
I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{CEX} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)
12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0

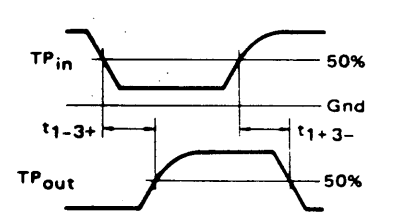
Characteristic	Symbol	Pin Under Test	MC672 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3	-	-	1.2	-	-	-	-	14	-	7
	V_{OH}	3	-	-	12.5	-	12.5	-	Vdc	-	3	1	-	-	-	-	2	14	-	7
		3	-	-	12.5	-	12.5	-	Vdc	-	3	2	-	-	-	-	1	14	-	7
Short-Circuit Current	I_{SC}	3	-	-	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	14	1, 3, 7
Reverse Current	I_R	1	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	2, 7
		2	-	-	-	2.0	-	2.0	μAdc	-	-	-	-	-	2	-	-	14	-	1, 7
Output Leakage Current	I_{CEX}	3	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	3, 14	-	-	-	1, 7
Forward Current	I_F	1	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2	-	-	-	14	7
		2	-	-	-	-1.20	-	-1.20	mAdc	-	-	-	-	2	1	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	6.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1, 2, 4, 5, 7, 9, 10, 12, 13
	I_{CCH}	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{1-3-}	3	-	-	-	200	-	-	ns	1	3	-	-	-	-	-	14	-	-	7
	t_{1-3-}	3	-	-	-	100	-	-	ns	1	3	-	-	-	-	-	14	-	-	7

Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS







f = 500 kHz
DUTY CYCLE = 50%

See General Information section for packaging.

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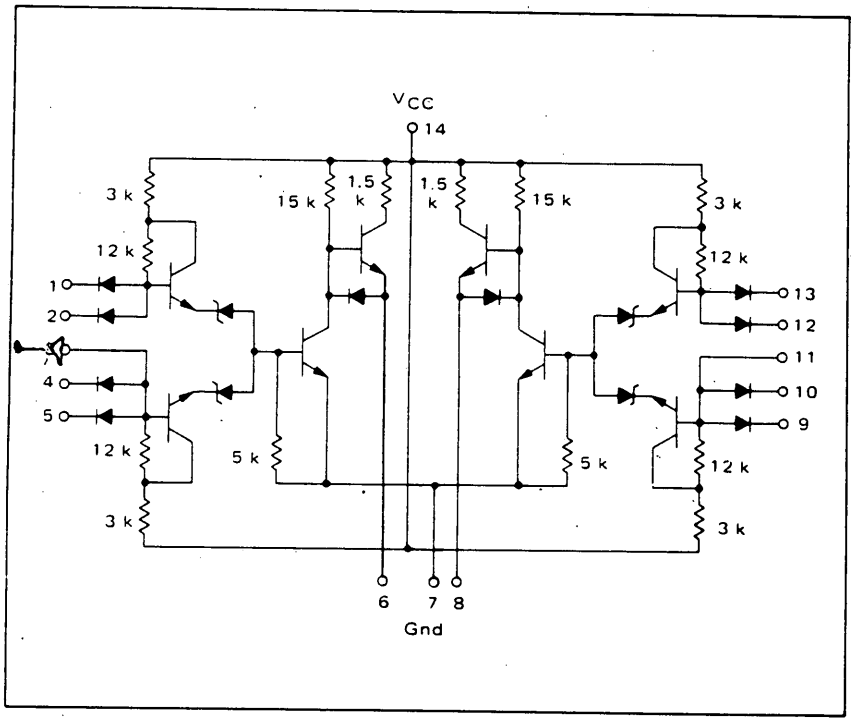
[illegible] PRINTED IN USA [illegible] IMPERIAL LITHO 839295 14M

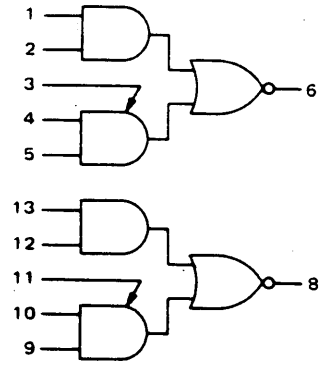
EXPANDABLE
DUAL 2-WIDE 2-INPUT
"AND-OR-INVERT" GATE
(Active Pullup)

MC673

ISSUE A

This device is a dual unit with each unit consisting of two 2-input AND gates (one with an input expander node available) that are internally ORed together into an inverting output configuration. The outputs have an active pullup network, thus the useful wired collector logic function is obtained while maintaining the low output impedance of the active pullup devices.

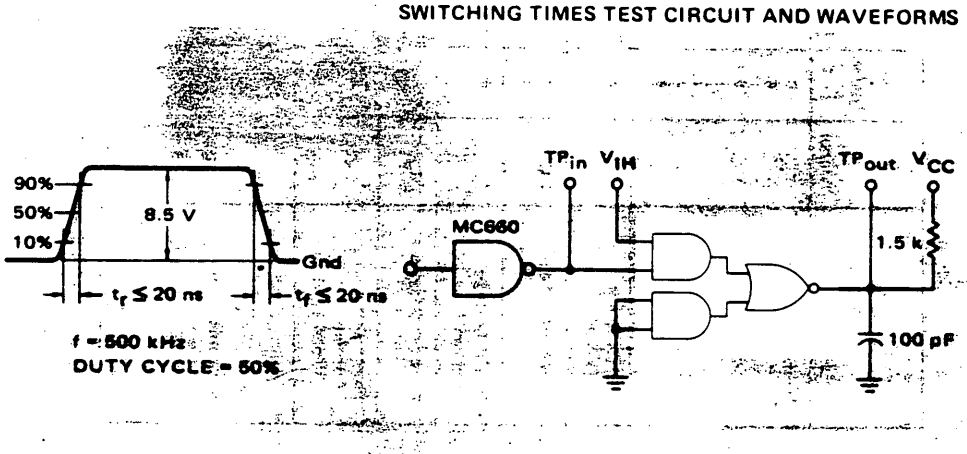


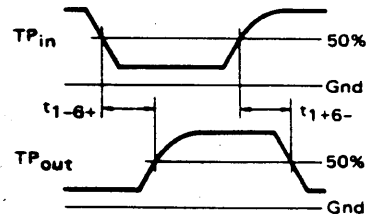


Positive Logic: $6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$
Negative Logic: $6 = \overline{(1 + 2) \cdot ([3] + 4 + 5)}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 110 ns typ
Typical Power Dissipation:
Inputs High = 160 mW typ/pkg
Input Low = 50 mW typ/pkg

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

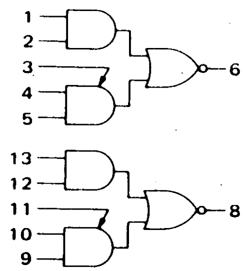




See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only. The other gate is tested in the same manner.



TEST CURRENT / VOLTAGE VALUES (All Temperatures)										
mA		Volts								
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_X
12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	7.2

Characteristic	Symbol	Pin Under Test	MC673 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc
		6	-	1.5	-	1.5	-	1.5	Vdc
	V_{OH}	6	12.5	-	12.5	-	12.5	-	Vdc
		↓	↓	-	↓	-	↓	-	↓
		↓	↓	-	↓	-	↓	-	↓
		↓	↓	-	↓	-	↓	-	↓
		↓	↓	-	↓	-	↓	-	↓
Short-Circuit Current	I_{SC}	6	-6.5	-15.0	-6.5	-15.0	-6.5	-15.0	mAdc
Reverse Current	I_R	1	-	2.0	-	2.0	-	2.0	μAdc
		4	-	2.0	-	2.0	-	2.0	μAdc
Output Leakage Current	I_{CEX}	6	-	100	-	100	-	100	μAdc
Forward Current	I_F	1	-	-1.20	-	-1.20	-	-1.20	mAdc
		4	-	-1.20	-	-1.20	-	-1.20	mAdc
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	5.5	-	-	mAdc
	I_{CCH}	14	-	-	-	15	-	-	mAdc
Switching Times	t_{1-6+}	1,6	-	-	-	200	-	-	ns
	t_{1+6-}	1,6	-	-	-	100	-	-	↓
	t_{4-6+}	4,6	-	-	-	200	-	-	↓
	t_{4+6-}	4,6	-	-	-	100	-	-	↓

Characteristic	Symbol	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_X	Gnd
Output Voltage	V_{OL}	6	-	-	1,2	-	-	-	-	14	-	-	4,5,7
		6	-	-	4,5	-	-	-	-	14	-	-	1,2,7
	V_{OH}	-	6	1	2	-	-	-	-	14	-	-	4,5,7
		-	↓	2	1	-	-	-	-	↓	-	-	4,5,7
		-	↓	4	5	-	-	-	-	↓	-	-	1,2,7
		-	↓	5	4	-	-	-	-	↓	-	-	1,2,7
		-	↓	-	4,5	-	-	-	-	↓	-	3	1,2,7
Short-Circuit Current	I_{SC}	-	-	-	-	-	-	-	-	-	14	-	1,4,6,7
Reverse Current	I_R	-	-	-	-	-	1	-	-	14	-	-	2,7
		-	-	-	-	-	4	-	-	14	-	-	5,7
Output Leakage Current	I_{CEX}	-	-	-	-	-	-	6	-	-	14	-	1,4,7
Forward Current	I_F	-	-	-	-	1	2	-	-	-	14	-	7
		-	-	-	-	4	5	-	-	-	14	-	7
Power Drain Current (Total Device)	I_{CCL}	-	-	-	-	-	-	-	-	-	14	-	1,2,4,5,7,9,10,12,13
	I_{CCH}	-	-	-	-	-	-	-	-	-	14	-	7
		Pulse In	Pulse Out										
Switching Times	t_{1-6+}	1	6	-	2	-	-	-	14	-	-	-	4,5,7
	t_{1+6-}	1	↓	-	2	-	-	-	↓	-	-	-	4,5,7
	t_{4-6+}	4	↓	-	5	-	-	-	↓	-	-	-	1,2,7
	t_{4+6-}	4	↓	-	5	-	-	-	↓	-	-	-	1,2,7

Pins not listed are left open.

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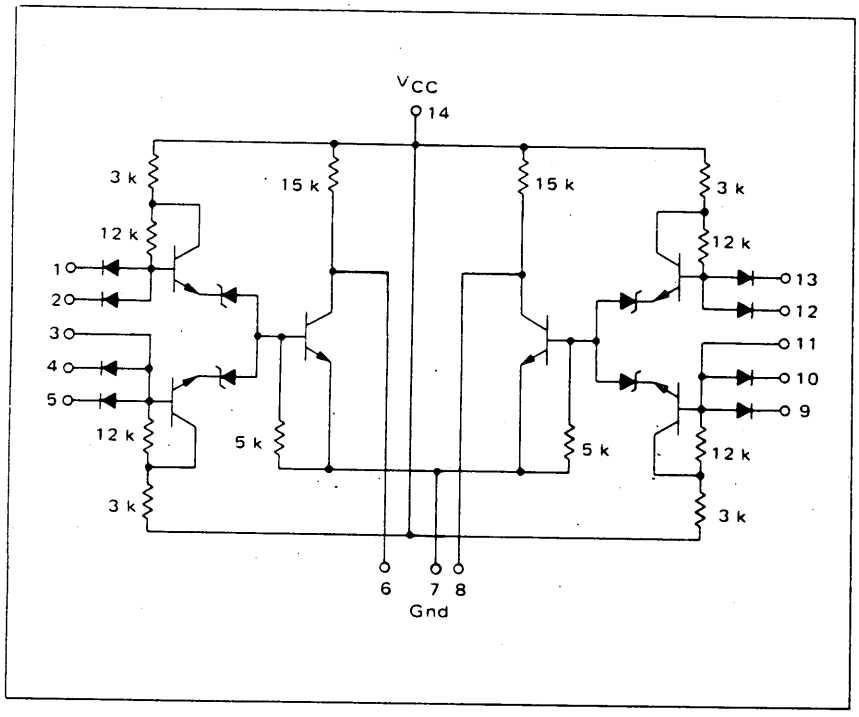
10-73-4a PRINTED IN USA 9-73 IMPERIAL LITHO 83714b 10M

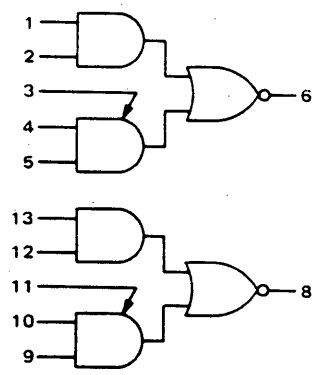
EXPANDABLE
DUAL 2-WIDE 2-INPUT
"AND-OR-INVERT" GATE
(Passive Pullup)

MC674

ISSUE A

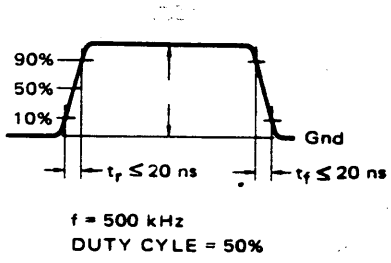
This device is a dual unit with each unit consisting of two 2-input AND gates (one with an input expander node available) that are internally ORed together into an inverting output configuration. This device varies from the MC673 in that a 15 k ohm pullup resistor is used at the outputs providing the capability of an additional wired OR logic function to be obtained from the units.

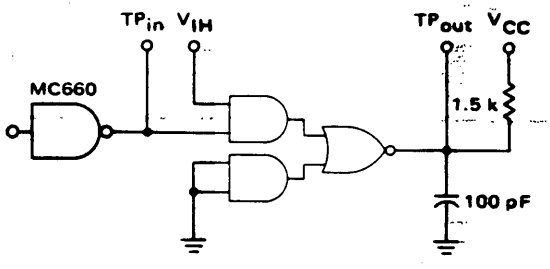


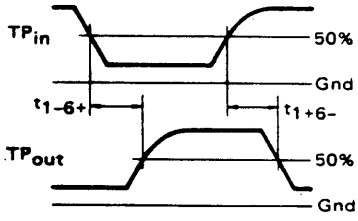


Positive Logic: $6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$
Negative Logic: $6 = (1 + 2) \cdot ([3] + 4 + 5)$
Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Power Dissipation:
Inputs High = 160 mW typ/pkg
Input Low = 50 mW typ/pkg

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



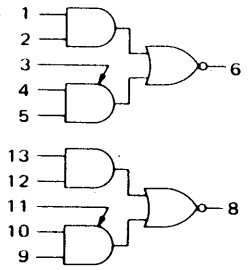




See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only. The other gate is tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC674 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Volts V_X	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	7.2	
										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:											
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	V_X	
Output Voltage	V_{OL}	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1,2	-	-	-	-	14	-	-	4,5,7
		6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	4,5	-	-	-	-	14	-	-	1,2,7
	V_{OH}	6	12.5	-	12.5	-	12.5	-	Vdc	-	6	1	2	-	-	-	-	14	-	-	4,5,7
		↓	↓	-	↓	-	↓	-	↓	-	↓	2	1	-	-	-	-	↓	-	-	4,5,7
				-		-		-		-		4	5	-	-	-	-		-		1,2,7
				-		-		-		-		5	4	-	-	-	-		-	-	1,2,7
		↓	↓	-	↓	-	↓	-	↓	-	↓	-	4,5	-	-	-	-	↓	-	3	1,2,7
Short-Circuit Current	I_{SC}	6	-0.6	-1.5	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,4,6,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	-	14	-	2,7
		4	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	4	-	-	-	14	-	5,7
Output Leakage Current	I_{CEX}	6	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	6	-	-	14	-	1,4,7
Forward Current	I_F	1	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	2	-	-	-	14	-	7
		4	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	-	-	4	5	-	-	-	14	-	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	5.5	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	1,2,4,5,7,9,10,12,13
	I_{CCH}	14	-	-	-	15	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	-	7
										Pulse In	Pulse Out										
Switching Times	t_{1-6+}	1,6	-	-	-	250	-	-	ns	1	6	-	2	-	-	-	14	-	-	-	4,5,7
	t_{1+6-}	1,6	-	-	-	100	-	-	↓	1	↓	-	2	-	-	-	↓	-	-	-	4,5,7
	t_{4-6+}	4,6	-	-	-	250	-	-		4		-	5	-	-	-		-	-	-	1,2,7
	t_{4+6-}	4,6	-	-	-	100	-	-	↓	4	↓	-	5	-	-	-	↓	-	-	-	1,2,7

Pins not listed are left open.

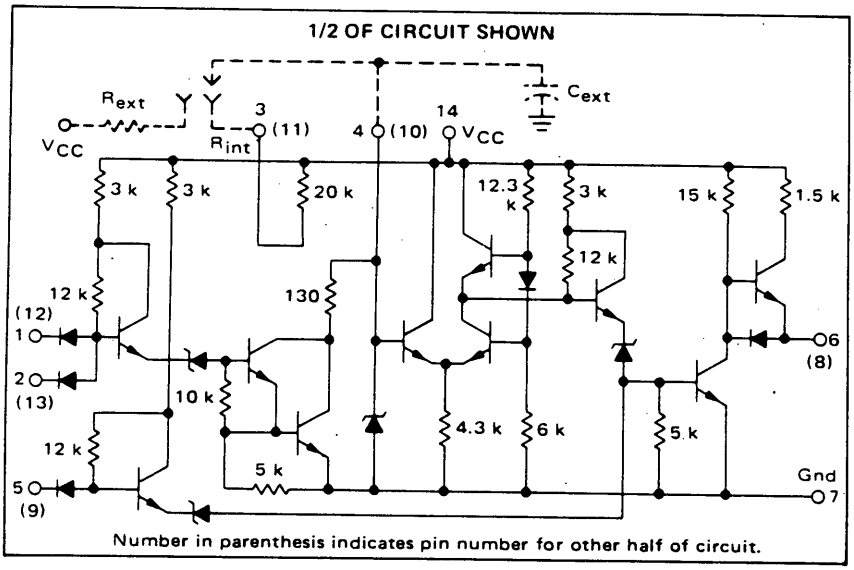
MC675

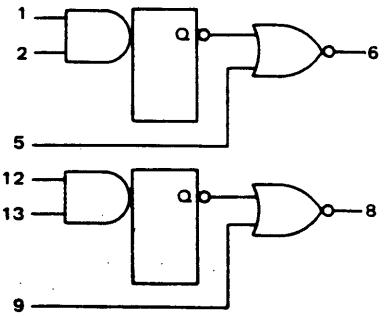
ISSUE A

The MC675 is a dual monolithic pulse-stretcher which gives an output pulse width equal to the sum of the input pulse width and a time interval determined by an external timing capacitor and either an internal or external resistor.

The MC675 operates on threshold levels, making input pulse rise and fall times unimportant. It has the capability of recycling at any time (zero recovery time) including the interval when the output is high, and has the characteristic high noise immunity of MHTL.

Flexibility is provided through the use of a two-input NOR gate at the output. With this input low, the output conforms to the definition of a pulse-stretcher. By applying the input waveform to all three input terminals simultaneously, the output conforms to that of a pulse-shaping monostable. (The output is initiated by the negative transition of the input waveform and has a width which is a function only of the timing elements.)





Input Loading Factor = 1
Output Loading Factor = 10
Power Dissipation = 180 mW per pack/typ
Propagation Delay:
Pins 1, 6 = 150 ns typ
Pins 5, 6 = 110 ns typ

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

FIGURE 1

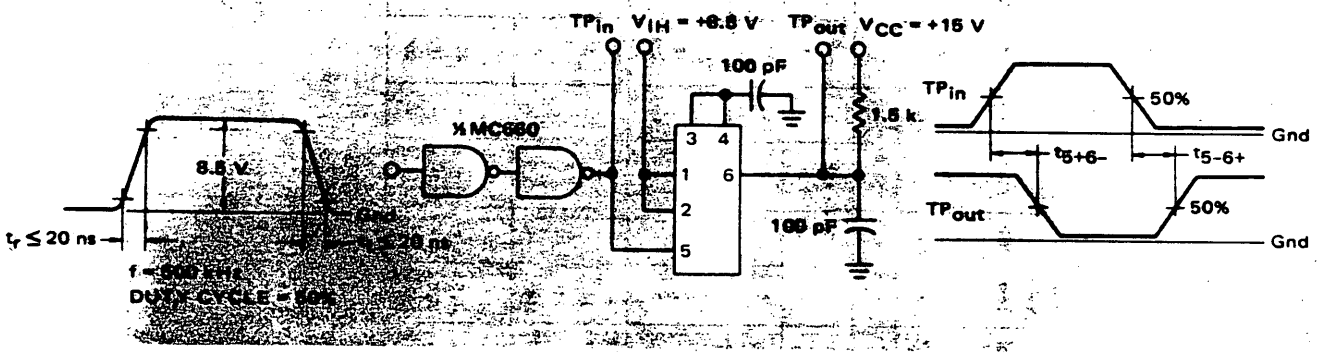
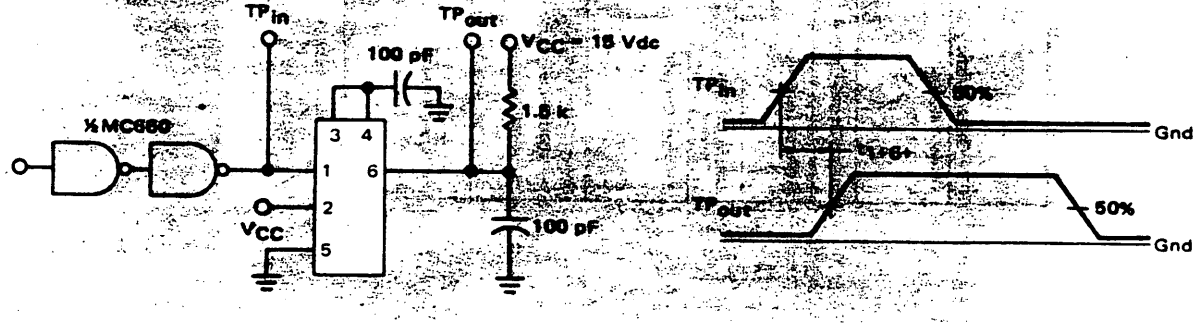


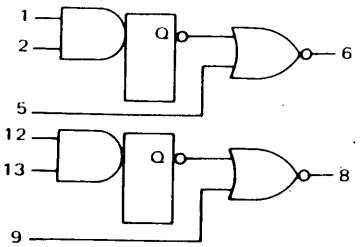
FIGURE 2



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one pulse-stretcher. The other pulse-stretcher is tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC675 Test Limits −30°C Min	−30°C Max	+25° Min	+25° Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
Output Voltage	V_{OL}*	6	-	1.5	-	1.5	-	1.5	Vdc	6	-	-	1,2,5	-	-	-	-	14	-	7
			-	↓	-	↓	-	↓		↓	-	-	2	1,5	-	-	-	↓	-	↓
	V_{OH}*	↓	12.5	-	12.5	-	12.5	-		-	6	5	1,2	2,5	-	-	-		-	
Short-Circuit Current	I_{SC}*	6	-6.5	-15.0	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	1,2	-	-	-	14	5,6,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	2,7
		2	-	↓	-	↓	-	↓		-	-	-	-	-	2	-	-	↓	-	1,7
		5	-		-					-	-	-	-	-	5	-	-		-	7
Output Leakage Current	I_{CEX}*	6	-	100	-	100	-	100	μAdc	-	-	-	-	-	1,2	6	-	-	14	5,7
Forward Current	I_F	1	-	-1.2	-	-1.2	-	-1.2	mAdc	-	-	-	-	1	2	-	-	-	14	7
		2	-	↓	-	↓	-	↓		-	-	-	-	2	1	-	-	-	↓	↓
		5	-		-		-			-	-	-	-	5	-	-	-	-		3,7
	I_3	3	-	-	-0.6	-1.1	-	-	mAdc	-	-	-	-	-	-	-	-	-	↓	
Power Drain Current (Both Units)	I_{CC1}**	14	-	-	-	20	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,5,7,9,12,13
	I_{CC2}**	14	-	-	-	24	-	-		-	-	-	-	-	-	-	5,9	-	↓	1,2,7,12,13
	I_{CC3}**	14	-	-	-	15	-	-		-	-	-		-	-	-	1,2,12,13	-		5,7,9
	I_{CC4}**	14	-	-	-	21	-	-	↓	-	-	-	-	-	-	-	1,2,5,9,12,13	-	↓	7
Switching Times										Pulse In	Pulse Out									
	t_{1+6+}*	1,6	-	-	-	250	-	-	ns	1	6	-	-	-	-	-	2, 14	-	-	5,7
	t_{5+6-}*	5,6	-	-	-	100	-	-		5	↓	-	1, 2	-	-	-	14	-	-	7
	t_{5-6+}*	5,6	-	-	-	200	-	-	↓	5		-	1, 2	-	-	-	14	-	-	7

* Tie pin 3 to pin 4.
** Tie pin 3 to pin 4 and pin 10 to pin 11.
Pins not listed are left open.

APPLICATIONS INFORMATION

When the device is connected in the Pulse Stretcher configuration:

1. Pins 5 and 9 must be grounded.
2. The output pulse, t_{out}, equation is: $t_{out} \approx t_{in} + 0.3\ R_{ext}\ (C_{ext} + 35\ pF)$.*

When the device is connected in the Monostable configuration:

1. Pins 1, 2, and 5 should be connected together and pins 9, 12, and 13 should be connected together.
2. No output pulse will occur for an input noise pulse of $t_{in} < 10\ C_{ext}$.
3. The output pulse, t_{out}, equation is: $t_{out} \approx 0.3\ R_{ext}\ (C_{ext} + 35\ pF)$.*

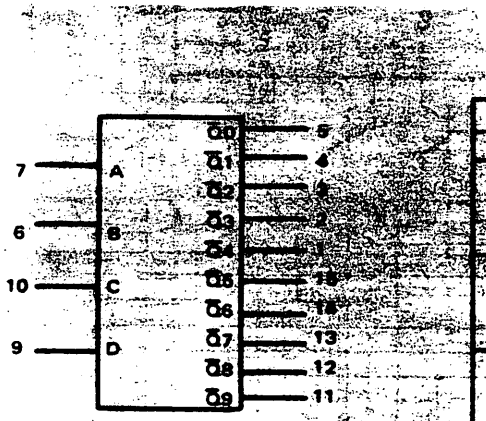
*t_{in} and t_{out} are in seconds, C_{ext} in farads. 3.0 k ohms $\leq R_{ext} \leq$ 100 k ohms.

BCD-TO-DECIMAL
DECODER-DRIVER

MC676

ISSUE A

The MC676 monolithic BCD-to-Decimal Decoder/ Driver is designed for use with gas-filled cold-cathode indicator tubes or other devices requiring high voltage drivers. The high voltage output transistors can withstand 70 volts.

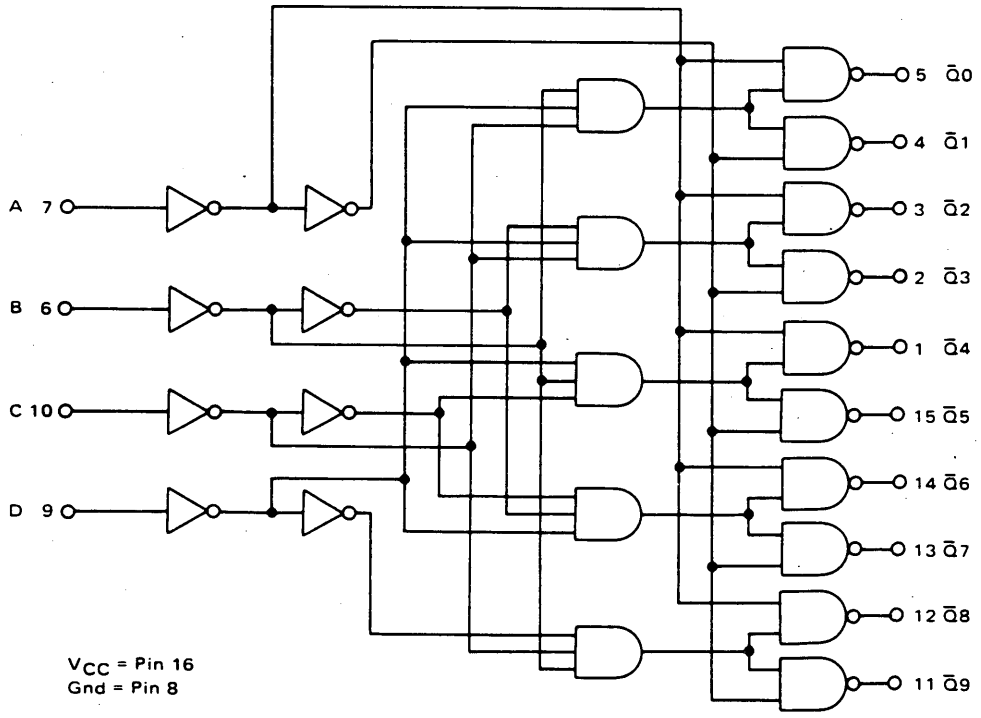


Input Loading Factor = 1
Power Dissipation = 380 mW typ/pkg

TRUTH TABLE

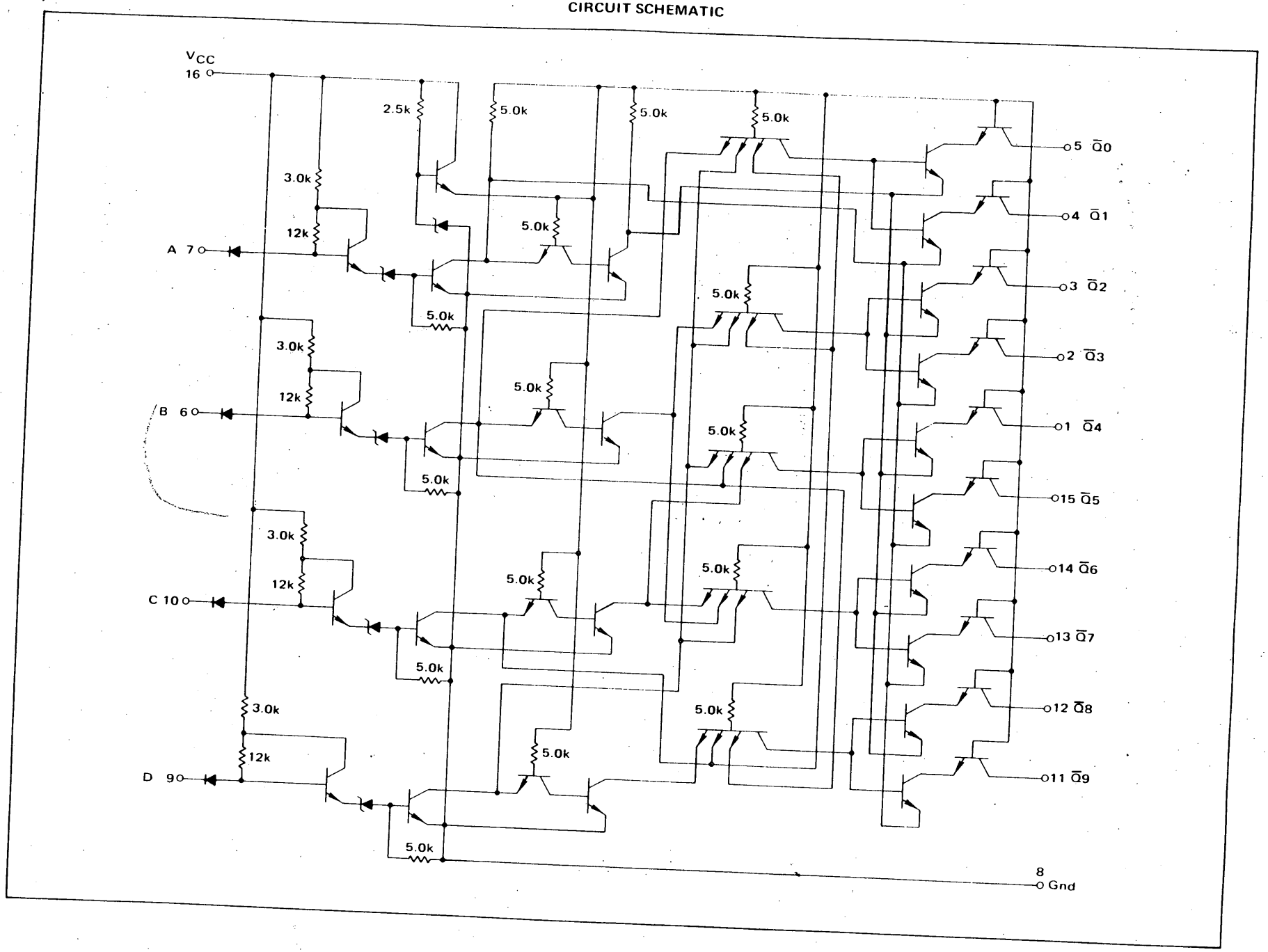
INPUT				OUTPUT									
D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	0	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	1	1	1	1	1	0	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	1	1	1	1	1	0	1	1	1	1	1
0	1	1	0	1	1	1	0	1	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

LOGIC DIAGRAM

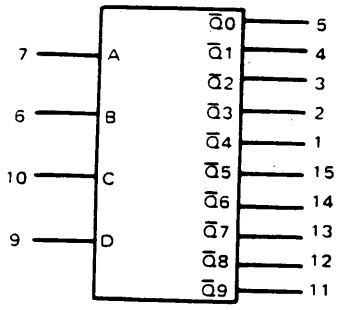


See General Information section for packaging.

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

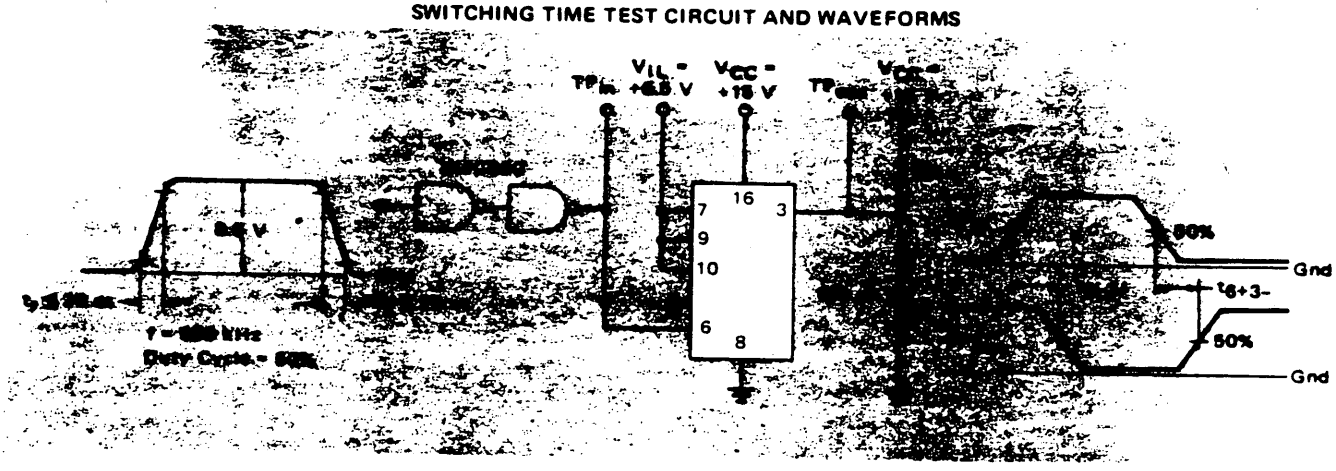


BEST COPY

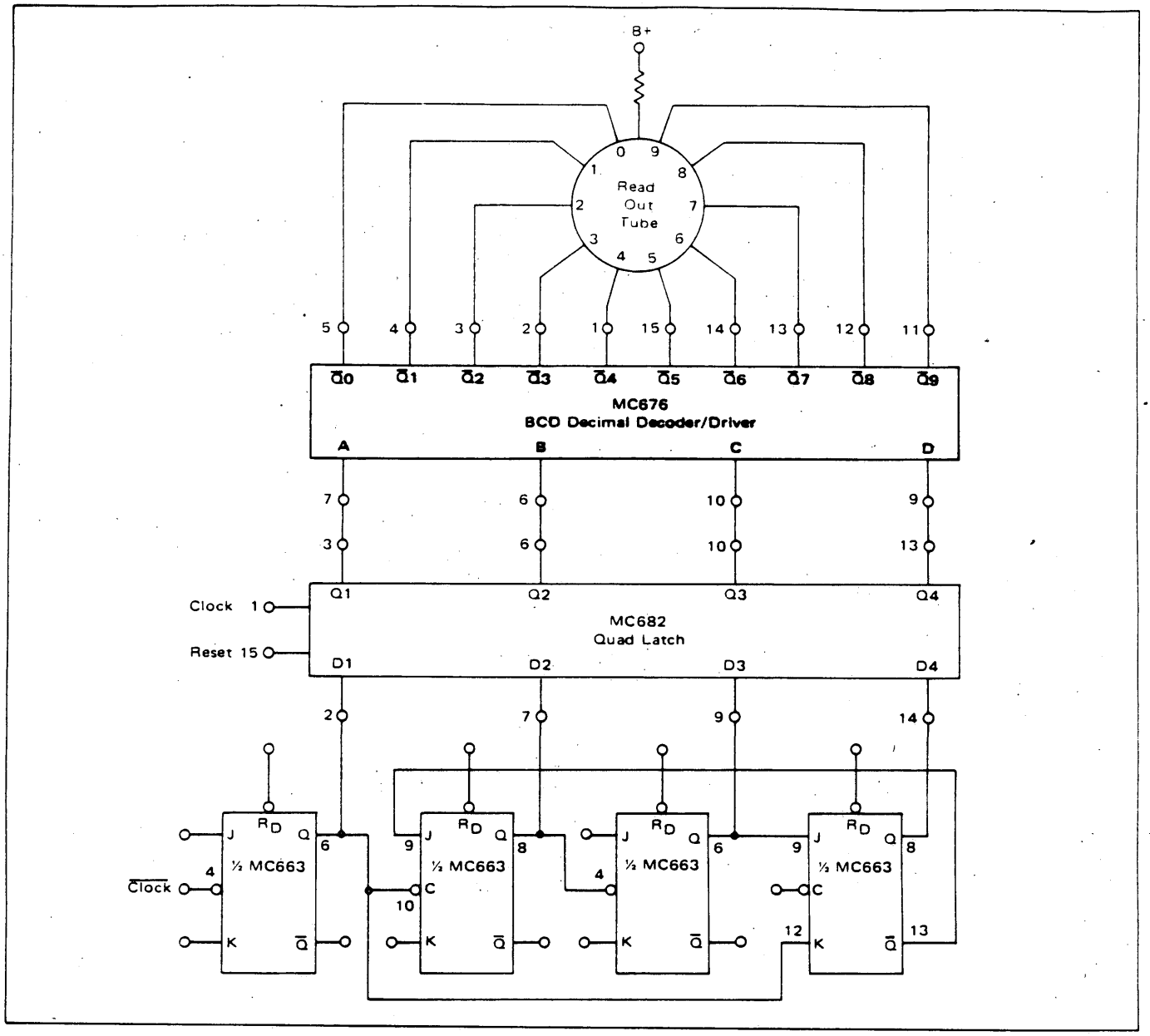
Characteristic	Symbol	Pin Under Test	MC676 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	μA I_{BD}	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
										10.0	100	6.50	8.50	1.5	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:									
Output Voltage	V_{OL}	1	–	1.5	–	1.5	–	1.5	Vdc	1	–	6,7,9	10	–	–	–	16	–	3
		2	–	↓	–	↓	–	↓	↓	2	–	9,10	6,7	–	–	–	↓	–	↓
		3	–		–		–			3	–	7,9,10	6	–	–	–		–	
		4	–		–		–			4	–	6,9,10	7	–	–	–		–	
		5	–		–		–			5	–	6,7,9,10	–	–	–	–		–	
		11	–		–		–			11	–	6,10	7,9	–	–	–		–	
		12	–		–		–			12	–	6,7,10	9	–	–	–		–	
		13	–		–		–			13	–	9	6,7,10	–	–	–		–	
		14	–		–		–			14	–	7,9	6,10	–	–	–		–	
		15	–	↓	–	↓	–	↓	↓	15	–	6,9	7,10	–	–	–	↓	–	↓
Reverse Current	I_R	6	–	2.0	–	2.0	–	2.0	μAdc	–	–	–	–	–	6	–	16	–	3
		7	–	↓	–		–			–	–	–	–	–	7	–		–	
		9	–		–		–			–	–	–	–	–	9	–		–	
		10	–	↓	–		–	↓	↓	–	–	–	–	–	10	–	↓	–	↓
Output Breakdown Voltage	V_{BD}	1	–	–	70	–	70	–	Vdc	–	1	–	6,7,9,10	–	–	–	16	–	8
		2	–	–	↓	–	↓	–	↓	–	2	–	↓	–	–	–	↓	–	↓
		3	–	–		–		–		–	3	–		–	–	–		–	
		4	–	–		–		–		–	4	–		–	–	–		–	
		5	–	–		–		–		–	5	–		–	–	–		–	
		11	–	–		–		–		–	11	–		–	–	–		–	
		12	–	–		–		–		–	12	–		–	–	–		–	
		13	–	–		–		–		–	13	–		–	–	–		–	
		14	–	–		–		–		–	14	–		–	–	–		–	
		15	–	–	↓	–	↓	–	↓	–	15	–	↓	–	–	–	↓	–	↓
Forward Current	I_F	6	–	-1.20	–	-1.20	–	-1.20	mAdc	–	–	–	–	6	–	–	–	16	3
		7	–	↓	–	↓	–	↓	↓	–	–	–	–	7	–	–	–	↓	↓
		9	–		–		–			–	–	–	–	9	–	–	–		
		10	–	↓	–	↓	–	↓	↓	–	–	–	–	10	–	–	–	↓	↓
Power Drain Current (Total Device)	I_{CCL}	16	–	–	–	35.0	–	–	mAdc	–	–	–	–	–	–	–	–	16	6,7,8,9,10
	I_{CCH}	16	–	–	–	35.0	–	–	mAdc	–	–	–	–	–	–	–	–	16	3
										Pulse In	Pulse Out								
Switching Times	t_{6-3+}	3	–	–	–	500	–	–	ns	6	3	7,9,10	–	–	–	16	–	–	3
	t_{6+3-}	3	–	–	–	600	–	–	ns	6	3	7,9,10	–	–	–	16	–	–	8

Pins not listed are left open.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TYPICAL INTERCONNECTION DIAGRAM



MOTOROLA Semiconductor Products Inc.

BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC

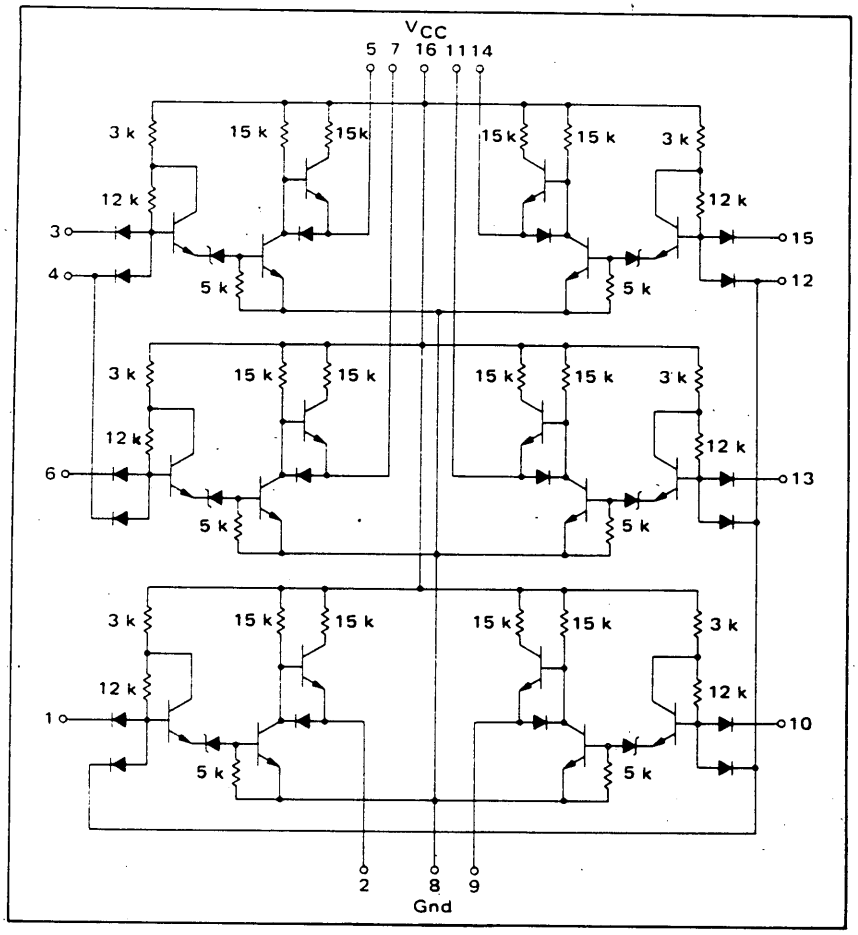
3073-41 PRINTED IN U.S.A. 12-72 IMPERIAL LITHO 833469 12M

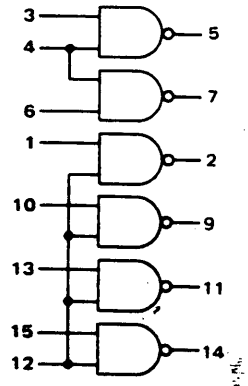
HEX INVERTER
WITH STROBE
(Active Pullup)

MC677

ISSUE A

This hex inverter can replace 1-1/2 quad two-input NAND gate packages in some applications through use of the enable or strobe inputs. The device consists of six two-input NAND gates with one input common to four gates and another common to two gates. Active pull-up elements are utilized to minimize output impedance. This device is in a 16-pin dual-in-line package.

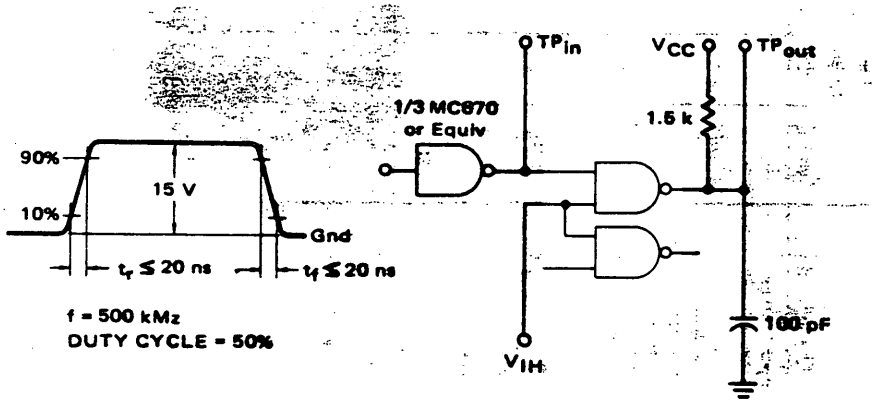


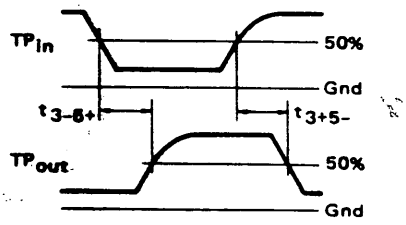


Positive Logic: $5 = \overline{3 \cdot 4}$
$7 = \overline{4 \cdot 6}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation
Inputs High = 246 mW
Input Low = 96 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

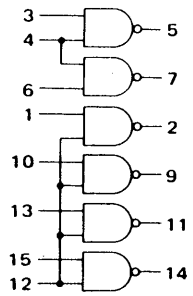




See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC677 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
										TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
Output Voltage	V_{OL}	5	-	1.5	-	1.5	-	1.5	Vdc	5	-	-	3,4	-	-	-	-	16	-	8
	V_{OH}	5	12.5	-	12.5	-	12.5	-	Vdc	-	5	3	4	-	-	-	-	16	-	8
Short-Circuit Current	I_{SC}	5	-6.5	-15.0	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	16	3,4,5,8
Reverse Current#	I_R	3	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	3	-	-	16	-	4,8
	$2I_R$	4	-	4.0	-	4.0	-	4.0	μAdc	-	-	-	-	-	4	-	-	16	-	3,6,8
Output Leakage Current	I_{CEX}	5	-	100	-	100	-	100	μAdc	-	-	-	-	-	-	5.16	-	-	-	4,8
Forward Current*	I_F	3	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	-	-	3	-	-	-	-	16	8
	$2I_F$	4	-	-2.40	-	-2.40	-	-2.40	mAdc	-	-	-	-	4	-	-	-	-	16	8
Power Drain Current (Total Device)	I_{CCL}	16	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	16	1,3,4,6,8,10,12,13,15
	I_{CCH}	16	-	-	-	30	-	-	mAdc	-	-	-	-	-	-	-	-	-	16	8
Switching Times										Pulse In	Pulse Out									
	t_{3-5+}	5	-	-	-	200	-	-	ns	3	5	-	4	-	-	-	16	-	-	8
	t_{3+5-}	5	-	-	-	100	-	-	ns	3	5	-	4	-	-	-	16	-	-	8

Pins not listed are left open.

*When checking pins 2, 9, 11, 14 the test limit for pin 12 is $4I_F$ = -4.8 mAdc.

#When checking pins 2, 9, 11, 14 the test limit for pin 12 is $4I_R$ = 8.0 μAdc.

MOTOROLA Semiconductor Products Inc.
BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC

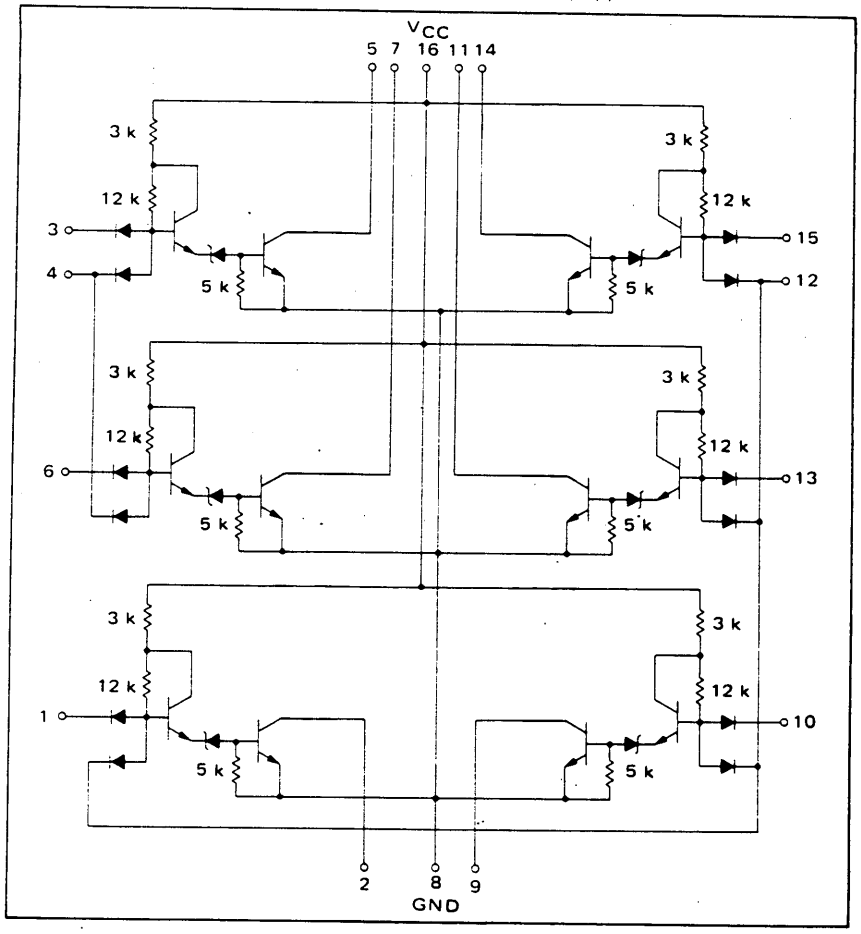
HEX INVERTER
WITH STROBE
(Without Output Resistors)

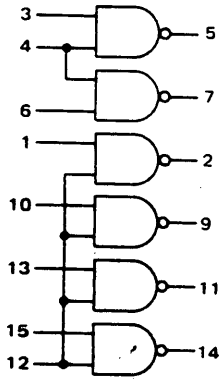
MC678

ISSUE A

This hex inverter is designed to drive low-current lamps, interface with discrete components, and facilitate the implementation of the "Implied AND" (Wired Collector) function with minimum power dissipation and loss of fan-out capability as well as provide a "strobed" inversion function. When used strictly as an inverter, external 15 k-ohm pull-up resistors should be utilized.

The device is in a 16-pin dual in-line package with two pins used to provide enable or strobe inputs. These inputs are common to specific sections of the device and allow the unit to replace 1-1/2 quad two-input gate packages in many applications.

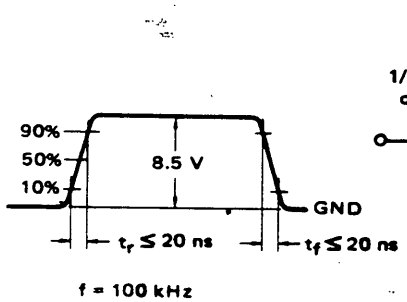


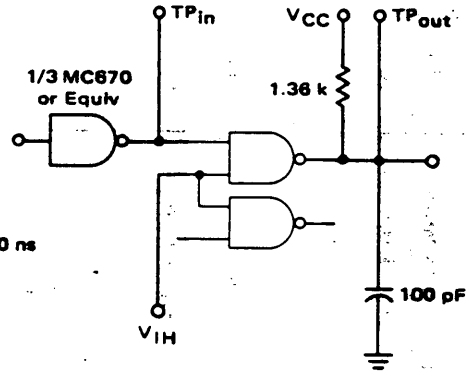


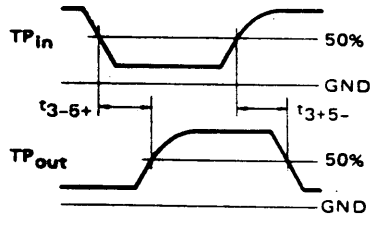
Positive Logic: $5 = \overline{3 \cdot 4}$
$7 = \overline{4 \cdot 6}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High = 192 mW
Input Low = 96 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



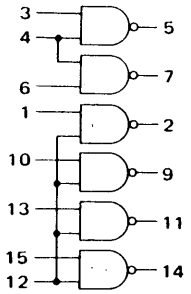




See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC678 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{CEX} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	Gnd
										TEST CURRENT/VOLTAGE VALUES: 12.0 mA	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
Output Voltage	V_{OL}	5	-	1.5	-	1.5	-	1.5	Vdc	5	3,4	-	-	-	-	16	-	8
Reverse Current#	I_R	3	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	3	-	-	16	-	4,8
	$2I_R$	4	-	4.0	-	4.0	-	4.0	μAdc	-	-	-	4	-	-	16	-	3,6,8
Output Leakage Current	I_{CEX}	5	-	-	-	100	-	100	μAdc	-	-	-	-	5,16	-	-	-	4,8
Forward Current*	I_F	3	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	3	-	-	-	-	16	8
	$2I_F$	4	-	-2.40	-	-2.40	-	-2.40	mAdc	-	-	4	-	-	-	-	16	8
Power Drain Current Current (Total Device)	I_{CCL}	16	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	16	1,3,4,6,8,10,12,13,15
	I_{CCH}	16	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	16	8
Switching Times										Pulse In / Pulse Out								
	t_{3-5+}	5	-	-	-	250	-	-	ns	3 / 5	4	-	-	-	16	-	-	8
	t_{3+5-}	5	-	-	-	100	-	-	ns	3 / 5	4	-	-	-	16	-	-	8

Pins not listed are left open.

*When checking pins 2, 9, 11, 14 the test limit for pin 12 is $4I_F = -4.8$ mAdc.
#When checking pins 2, 9, 11, 14 the test limit for pin 12 is $4I_R = 8.0$ μAdc.

MOTOROLA Semiconductor Products Inc.
BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

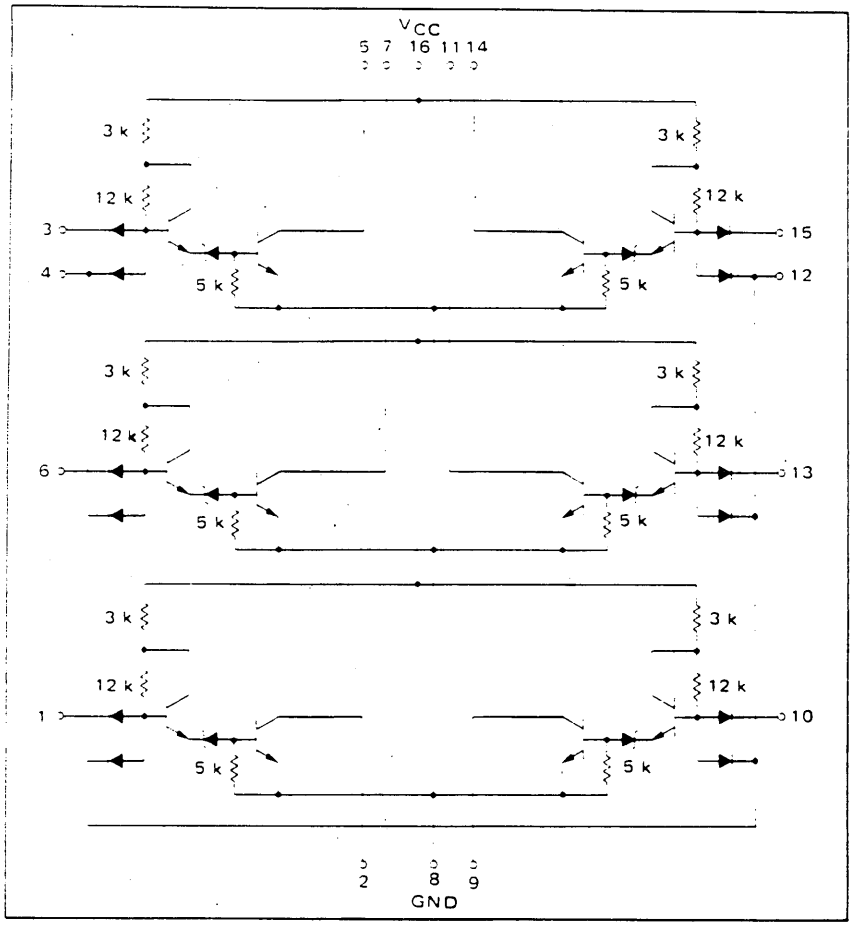
HEX INVERTER
WITH STROBE
(Without Output Resistors)

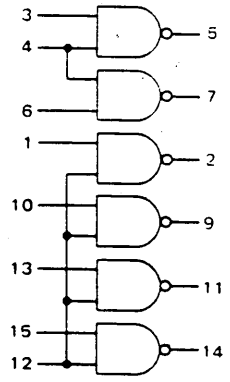
MC678

MARCH 197

This hex inverter is designed to drive low-current lamps, interface with discrete components, and facilitate the implementation of the "Implied AND" (Wired Collector) function with minimum power dissipation and loss of fan-out capability as well as provide a "strobed" inversion function. When used strictly as an inverter, external 15 k-ohm pull-up resistors should be utilized.

The device is in a 16-pin dual in-line package with two pins used to provide enable or strobe inputs. These inputs are common to specific sections of the device and allow the unit to replace 1-1/2 quad two-input gate packages in many applications.

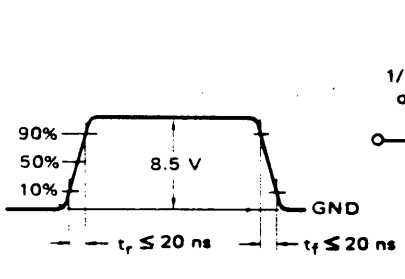


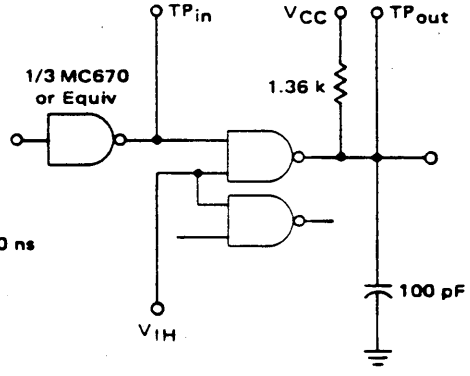


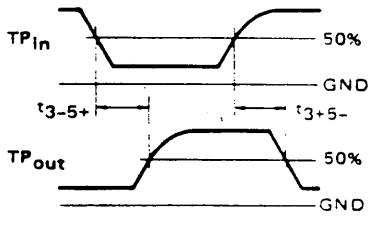
Positive Logic: $5 = \overline{3 \cdot 4}$
$7 = \overline{4 \cdot 6}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation
Inputs High = 192 mW
Input Low = 96 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



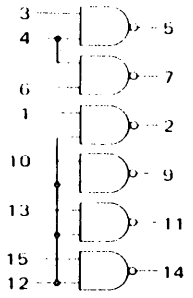




See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC678 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES mA I_{OL}	Volts V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
										12.0	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:								
										I_{OL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	5	-	1.5	-	1.5	-	1.5	Vdc	5	3,4	-	-	-	-	16	-	8
Reverse Current#	I_R	3	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	3	-	-	16	-	4,8
	$2I_R$	4	-	4.0	-	4.0	-	4.0	μAdc	-	-	-	4	-	-	16	-	3,6,8
Output Leakage Current	I_{CEX}	5	-	-	-	100	-	100	μAdc	-	-	-	-	5,16	-	-	-	4,8
Forward Current*	I_F	3	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	3	-	-	-	-	16	8
	$2I_F$	4	-	-2.40	-	-2.40	-	-2.40	mAdc	-	-	4	-	-	-	-	16	8
Power Drain Current Current (Total Device)	I_{CCL}	16	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	16	1,3,4,6,8,10,12,13,15
	I_{CCH}	16	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	16	8
Switching Times										Pulse In / Pulse Out								
	t_{3-5+}	5	-	-	-	250	-	-	ns	3 / 5	4	-	-	-	16	-	-	8
	t_{3+5-}	5	-	-	-	100	-	-	ns	3 / 5	4	-	-	-	16	-	-	8

Pins not listed are left open.

*When checking pins 2, 9, 11, 14 the test limit for pin 12 is $4I_F = -4.8$ mAdc.
#When checking pins 2, 9, 11, 14 the test limit for pin 12 is $4I_R = 8.0$ μAdc.

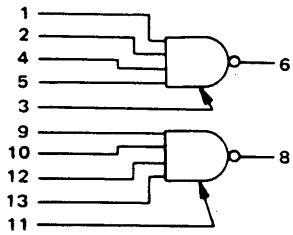
MC679 • MC679B

ISSUE A

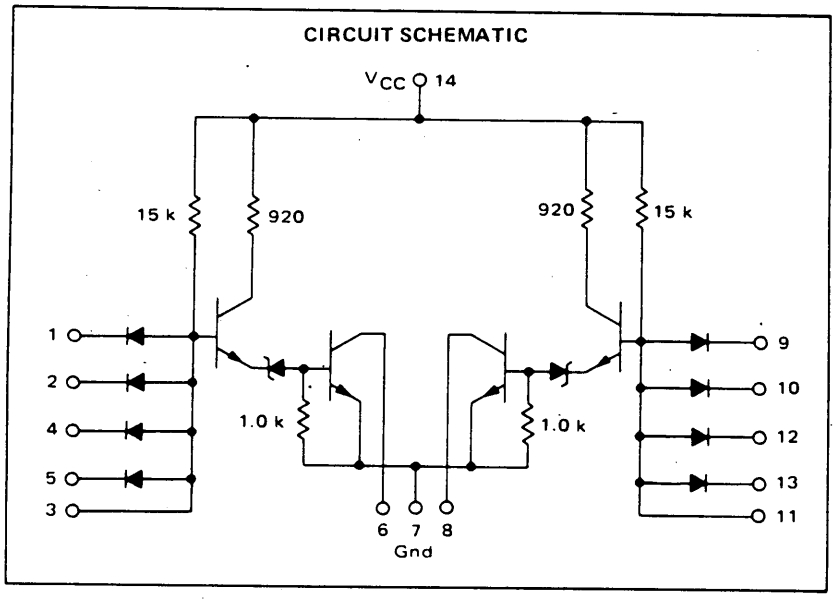
The MC679/679B is a dual lamp/relay driver featuring all-monlithic construction for maximum reliability and economy. Input levels are consistent with other elements in the MHTL series, making the device ideal for use in high noise environments.

The outputs consist of high voltage – high current transistors allowing the device to operate lamps and relays requiring up to 30 volts and/or 150 mA.

The MC679/679B is designed primarily as a lamp/relay driver, but it is also suitable for driving shift register clock lines, high capacitive loads, and interfacing with discrete components.

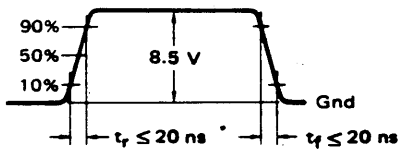


CIRCUIT SCHEMATIC

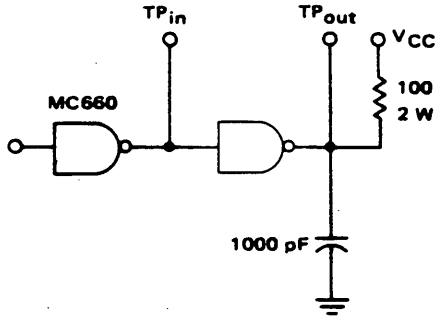


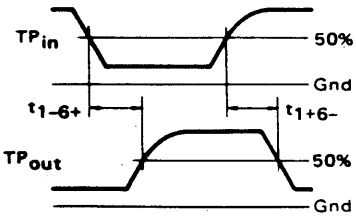
Positive Logic: $6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$
Input Loading Factor = 1
Output Loading Factor = 125
Propagation Delay Time = 0.5 μs typ
Typical Total Power Dissipation:
Inputs High = 250 mW
Input Low = 30 mW

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



f = 100 kHz
DUTY CYCLE = 50%

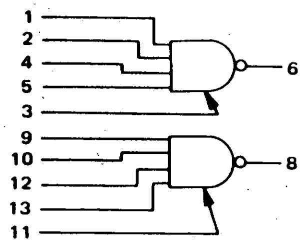




See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one lamp driver only. The other lamp driver is tested in the same manner.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
	mA	µA	Volts							
	I_{OL}	I_{BD}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CC}	V_{CCL}	V_{CCH}
MC679	150	100	6.50	8.50	1.5	16.0	7.20	15.0	14.0	16.0
MC679B	125	100	6.50	9.0	1.5	16.0	7.20	15.0	14.0	16.0

Characteristic	Symbol	Pin Under Test	MC679 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC679B Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Output Voltage	V_{OL}	6	–	1.0	–	1.0	–	1.0	Vdc	–	1.0	–	1.0	–	1.0	Vdc
Reverse Current	I_R	1	–	2.0	–	2.0	–	2.0	µAdc	–	2.0	–	2.0	–	2.0	µAdc
		2	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓
		4	–		–		–			–		–		–		
		5	–		–		–			–		–		–		
Output Breakdown Voltage	V_{BD}	6	–	–	+30	–	+30	–	Vdc	–	–	+24	–	+24	–	Vdc
		↓	–	–	↓	–	↓	–	↓	–	–	↓	–	↓	–	↓
			–	–		–		–		–	–		–		–	
			–	–		–		–		–	–		–		–	
			–	–		–		–		–	–		–		–	
Forward Current	I_F	1	–	-1.20	–	-1.20	–	-1.20	mAdc	–	-1.20	–	-1.20	–	-1.20	mAdc
		2	–	↓	–	↓	–	↓	↓	–	↓	–	↓	–	↓	↓
		4	–		–		–			–		–		–		
		5	–		–		–			–		–		–		
Power Drain Current (Total Device	I_{CCL}	14	–	–	–	3.0	–	–	mAdc	–	–	–	3.0	–	–	mAdc
	I_{CCH}	14	–	–	–	24	–	–	mAdc	–	–	–	30	–	–	mAdc
Switching Times	t_{1-6+}	6	–	–	–	250	–	–	ns	–	–	–	250	–	–	ns
	t_{1+6-}	6	–	–	–	100	–	–	ns	–	–	–	100	–	–	ns

TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:

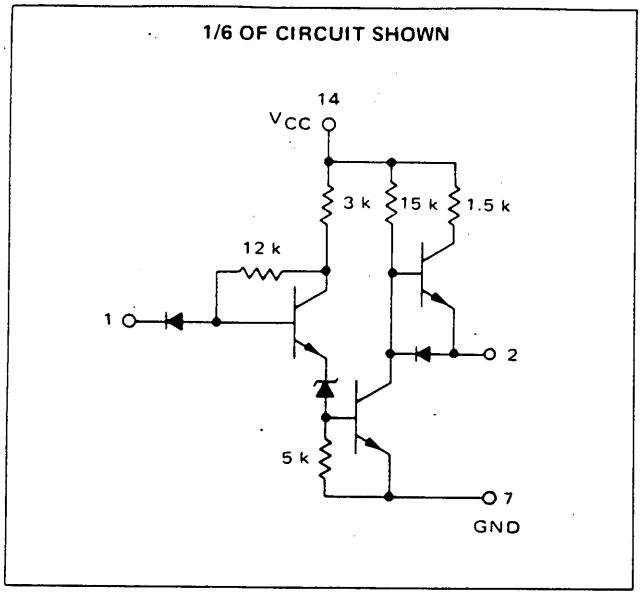
Characteristic	Symbol	I_{OL}	I_{BD}	V_{IL}	V_{IH}	V_F	V_R	V_X	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	6	–	–	1,2,4,5	–	–	–	–	14	–	7
Reverse Current	I_R	–	–	–	–	–	1	–	–	14	–	2,4,5,7
		–	–	–	–	–	2	–	–	↓	–	1,4,5,7
		–	–	–	–	–	4	–	–		–	1,2,5,7
		–	–	–	–	–	5	–	–		–	1,2,4,7
Output Breakdown Voltage	V_{BD}	–	6	–	–	–	–	3	–	–	14	7
		–	↓	1	2,4,5	–	–	–	–	–	↓	↓
		–		2	1,4,5	–	–	–	–	–		
		–		4	1,2,5	–	–	–	–	–		
		–		5	1,2,4	–	–	–	–	–		
Forward Current	I_F	–	–	–	–	1	–	–	–	–	14	7
		–	–	–	–	2	–	–	–	–	↓	↓
		–	–	–	–	4	–	–	–	–		
		–	–	–	–	5	–	–	–	–		
Power Drain Current (Total Device	I_{CCL}	–	–	–	–	–	–	–	–	–	14	1,2,4,5,7,9,10,12,13
	I_{CCH}	–	–	–	–	–	–	–	–	–	14	7
Switching Times		Pulse In	Pulse Out									
	t_{1-6+}	1	6	–	2,4,5	–		–	14	–	–	7
	t_{1+6-}	1	6	–	2,4,5	–	–	–	14	–	–	5

Pins not listed are left open.

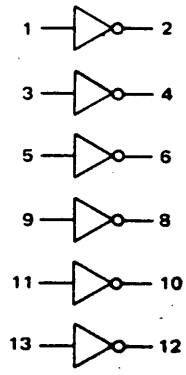
X073-1 PRINTED IN USA 12-72 IMPERIAL LITHO 83469 12M
DS 9091

MC680

ISSUE A



This hex inverter performs the function B = $\overline{A}$ and utilizes an active pull-up to minimize output impedance. This device is available in a 14-pin dual-in-line package with pin configuration identical to the MC836 MDTL hex inverter.



Positive Logic: $2 = \overline{1}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation:
Inputs High = 246 mW
Input Low = 96 mW

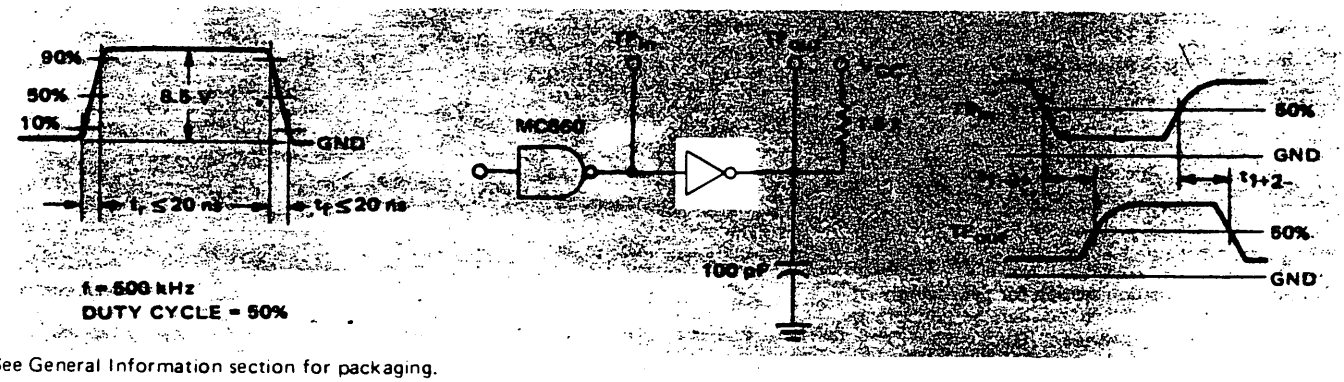
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC680 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{CEX} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
Output Voltage	V_{OL}	2	-	1.5	-	1.5	-	1.5	Vdc	2	-	-	1	-	-	-	-	14	-	7
	V_{OH}	2	12.5	-	12.5	-	12.5	-	Vdc	-	2	1	-	-	-	-	-	14	-	7
Short-Circuit Current	I_{SC}	2	-6.5	-15.0	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	7
Output Leakage Current	I_{CEX}	2	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	2,14	-	-	-	1,7
Forward Current	I_F	1	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	-	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,3,5,7,9,11,13
	I_{CCH}	14	-	-	-	30	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{1-2-}	2	-	-	-	200	-	-	ns	1	2	-	-	-	-	-	14	-	-	7
	t_{1-2-}	2	-	-	-	100	-	-	ns	1	2	-	-	-	-	-	14	-	-	7

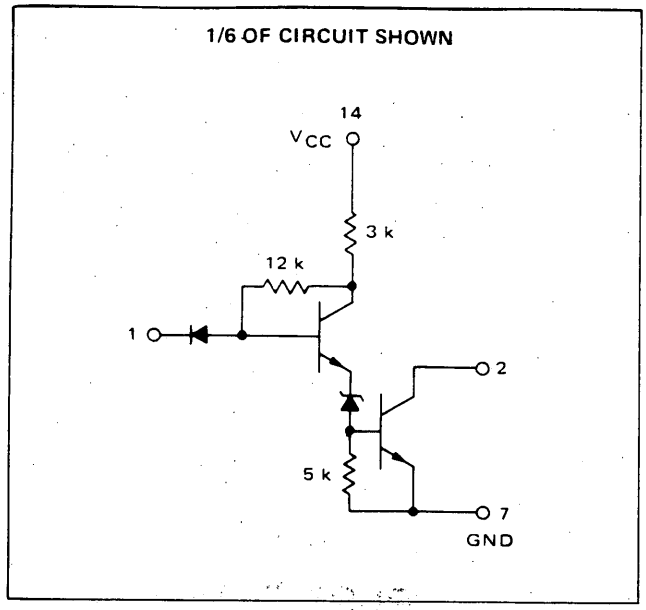
Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



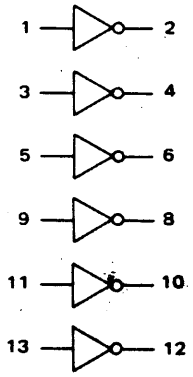
See General Information section for packaging.

MC681



This hex inverter is designed to drive low current lamps, interface with discrete components, and facilitate the implementation of the "Implied AND" (Wired Collector) function with minimum power dissipation and loss of fan-out capability, as well as provide the inversion function. When used strictly as an inverter, external 15 k-ohm pull-up resistors should be utilized.

The device is available in a 14 pin dual-in-line package with the pin configuration identical to the MC836 MDTL hex inverter.



Positive Logic: $2 = \bar{1}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation:
Input High = 192 mW
Input Low = 96 mW

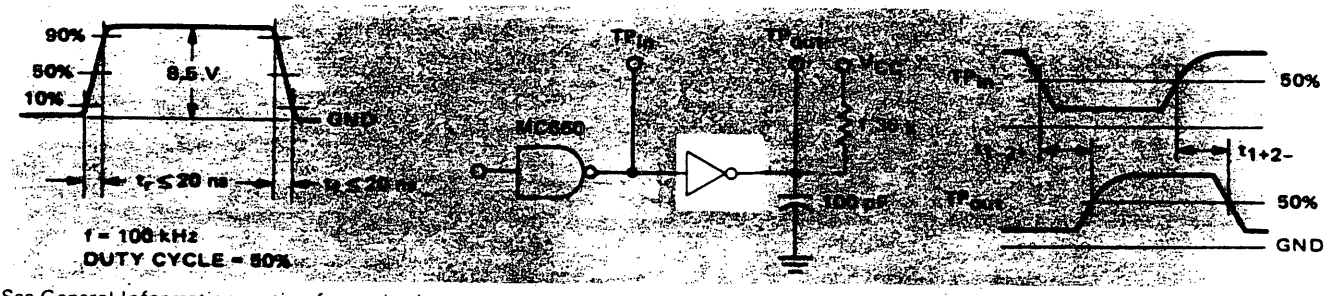
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC681 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
										mA	Volts							
										I_{OL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
Output Voltage	V_{OL}	2	-	1.5	-	1.5	-	1.5	Vdc	2	1	-	-	-	-	14	-	7
Reverse Current	I_R	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	1	-	-	14	-	7
Output Leakage Current	I_{CEX}	2	-	-	-	100	-	100	μAdc	-	-	-	-	2.14	-	-	-	7
Forward Current	I_F	1	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	1	-	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	14	1.3.5.7.9.11.13
	I_{CCH}	14	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out							
	t_{1-2+}	2	-	-	-	250	-	-	ns	1	2	-	-	-	14	-	-	7
	t_{1-2-}	2	-	-	-	100	-	-	ns	1	2	-	-	-	14	-	-	7

Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



See General Information section for packaging.

MOTOROLA Semiconductor Products Inc.
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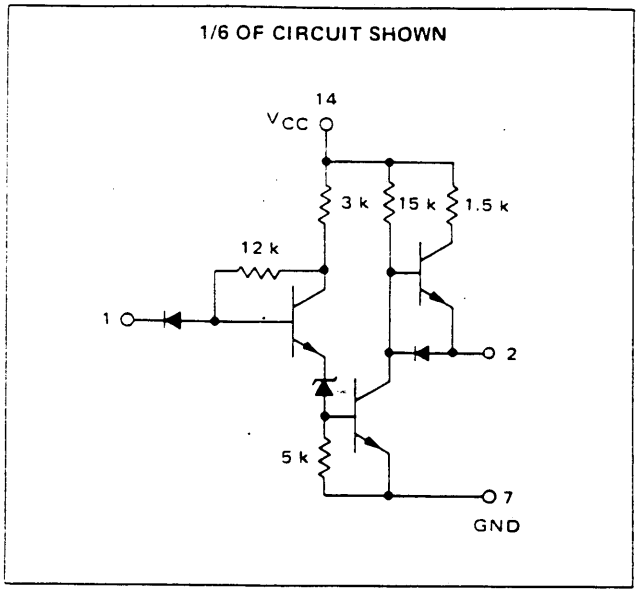
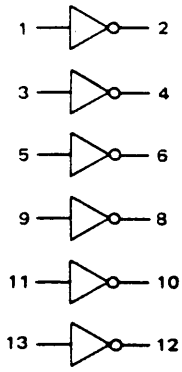
3073-44 PRINTED IN USA 6-73 IMPERIAL LITHO 837146 10M

MC680



This hex inverter performs the function B = $\overline{A}$ and utilizes an active pull-up to minimize output impedance. This device is available in a 14-pin dual-in-line package with pin configuration identical to the MC836 MDTL hex inverter.



Positive Logic: $2 = \overline{1}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 110 ns typ
Typical Total Power Dissipation:
Inputs High = 246 mW
Input Low = 96 mW

ELECTRICAL CHARACTERISTICS

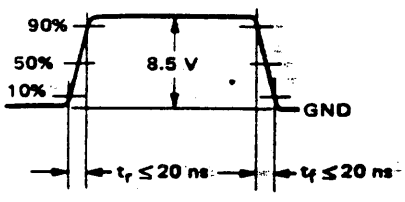
Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

			TEST CURRENT		VOLTAGE VALUES (All Temperatures)							
			mA		Volts							
			I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}
			12.0	-0.03	0.50	2.50	1.5	15.0	15.0	5.0	5.0	5.0

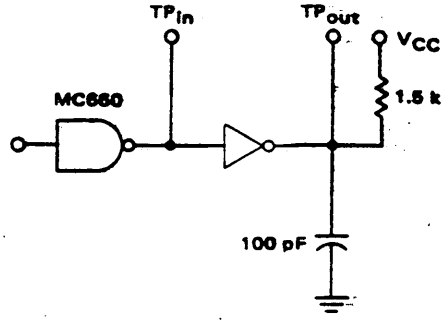
Characteristic	Symbol	Pin Under Test	MC680 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT I_{OL}	I_{OH}	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	2	-	1.5	-	1.5	-	1.5	Vdc	2	-	-	1	-	-	-	-	14	-	7
	V_{OH}	2	12.5	-	12.5	-	12.5	-	Vdc	-	2	1	-	-	-	-	-	14	-	7
Short-Circuit Current	I_{SC}	2	-6.5	-15.0	-6.5	-15.0	-6.5	-15.0	mAdc	-	-	-	-	-	-	-	-	-	14	7
Reverse Current	I_R	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	7
Output Leakage Current	I_{CEX}	2	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	2.14	-	-	-	7
Forward Current	I_F	1	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	-	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,3,4,5,6,8,9,10,11,12,13
	I_{CCH}	14	-	-	-	30	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{1-2-}	2	-	-	-	200	-	-	ns	1	2	-	-	-	-	-	14	-	-	7
	t_{1-2-}	2	-	-	-	100	-	-	ns	1	2	-	-	-	-	-	14	-	-	7

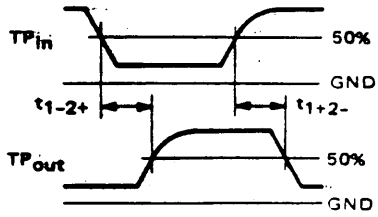
Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



f = 500 kHz
DUTY CYCLE = 50%

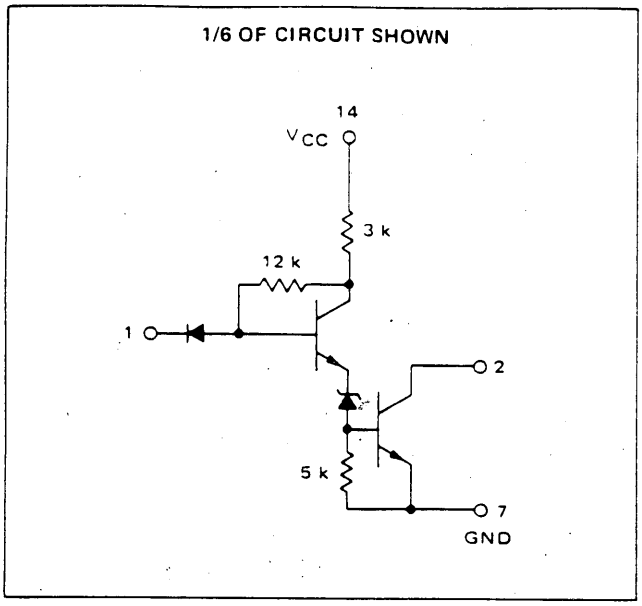




HEX INVERTER
(Open Collector)

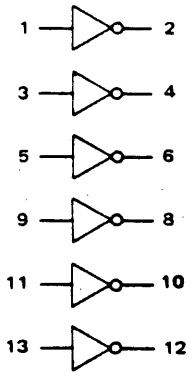
MC681

MAY 1970



This hex inverter is designed to drive low current lamps, interface with discrete components, and facilitate the implementation of the "Implied AND" (Wired Collector) function with minimum power dissipation and loss of fan-out capability, as well as provide the inversion function. When used strictly as an inverter, external 15 k-ohm pull-up resistors should be utilized.

The device is available in a 14 pin dual-in-line package with the pin configuration identical to the MC836 MDTL hex inverter.



Positive Logic: $2 = \bar{1}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation:
Input High = 192 mW
Input Low = 96 mW

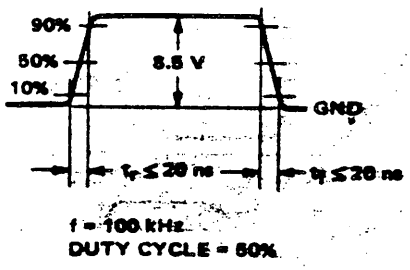
ELECTRICAL CHARACTERISTICS

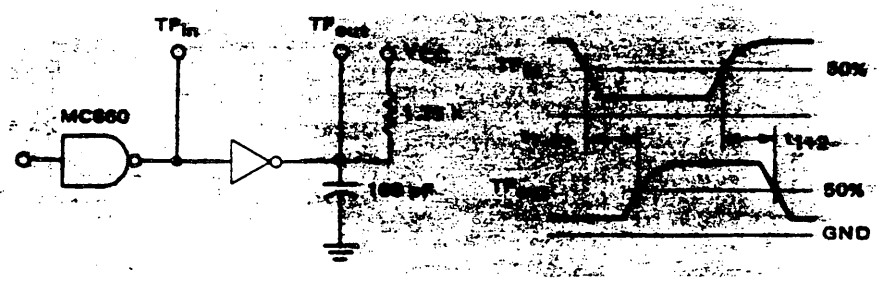
Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

			MC681 Test Limits							TEST CURRENT VOLTAGE VALUES (All Temperatures)								
			−30°C		+25°C		+75°C			mA	Volts							
										I_{OL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	3.50	1.5	16.0	16.0	15.0	14.0	16.0	
										TEST CURRENT VOLTAGE APPLIED TO PINS LISTED BELOW:								
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	2	-	1.5	-	1.5	-	1.5	Vdc	2	1	-	-	-	-	14	-	7
Reverse Current	I_R	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	1	-	-	14	-	7
Output Leakage Current	I_{CEX}	2	-	-	-	100	-	100	μAdc	-	-	-	-	2.14	-	-	-	7
Forward Current	I_F	1	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	1	-	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	14	1,3,5,7,9,11,13
	I_{CCH}	14	-	-	-	24	-	-	mAdc	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out							
	t_{1-2-}	2	-	-	-	250	-	-	ns	1	2	-	-	-	14	-	-	7
	t_{1-2-}	2	-	-	-	100	-	-	ns	1	2	-	-	-	14	-	-	7

Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





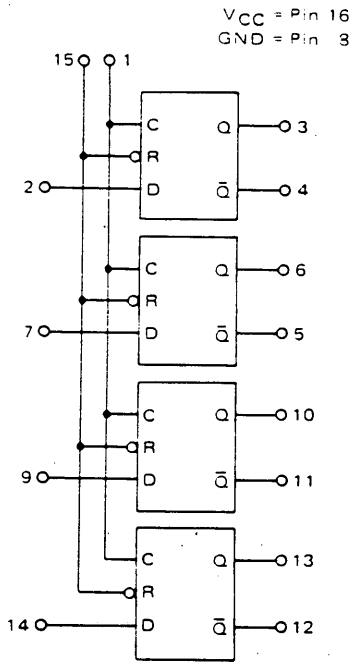
3073-40 PRINTED IN USA 3-72 IMPERIAL LITHO 83179 3M

MC682

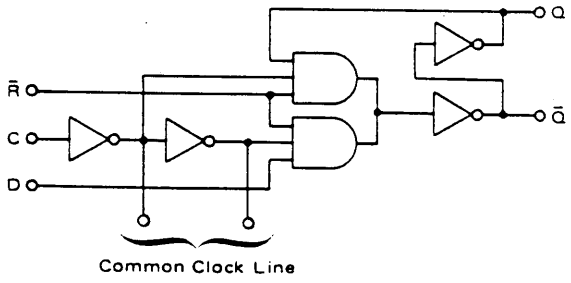
OCTOBER 1970

The MC682 Quad Latch is useful in monitoring or storage applications. A common clock input (C), when in the high state, allows information present at the D input to be transferred to the output of the latch. When C is low, the information present at Q or $\bar{Q}$, will remain at the previous level. A common $\overline{\text{Reset}}$ ($\bar{R}$) input allows resetting of all Q outputs to a logic "0" state independent of C or D.

BLOCK DIAGRAM



LOGIC DIAGRAM
1/4 OF CIRCUIT SHOWN

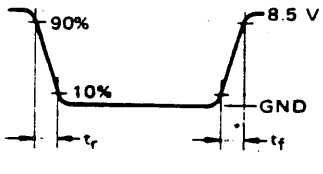


TRUTH TABLE

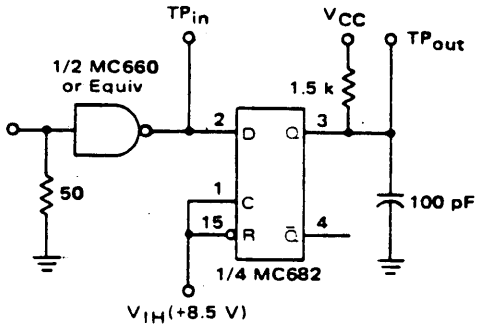
C	D	$\bar{R}$	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	0	1
0	0	1	Q_n	$\bar{Q}_n$
0	1	0	0	1
0	1	1	Q_n	$\bar{Q}_n$
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

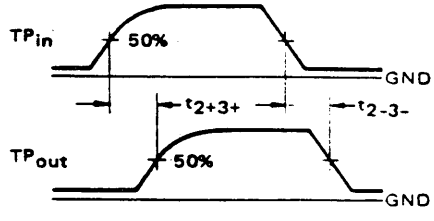
Input Loading Factor:
C, D = 1
$\bar{R}$ = 8
Output Loading Factor = 10
Power Dissipation = 375 mW Typ/pkg

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



$t_r = t_f \leq 20$ ns
f = 100 kHz
Duty Cycle = 50%



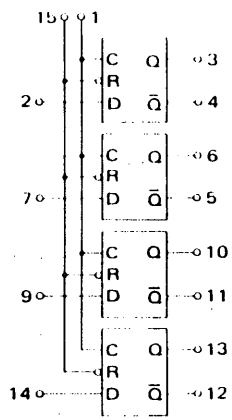


The other outputs are tested in a similar manner.

See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one latch. The other latches are tested in a similar manner.



										TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
										mA		Volts									
										I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	C_P	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
										12.0	-0.03	6.50	8.50	1.5	16.0	•	16.0	15.0	14.0	16.0	
		Pin Under Test	MC682 Test Limits							TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
			-30°C		+25°C		+75°C														
Characteristic	Symbol		Min	Max	Min	Max	Min	Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	C_P	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	1.5	-	1.5		1.5	Vdc	3		2				1			16		8
		4		1.5		1.5		1.5	↓	4			2			1			↓		↓
	V_{OH}	3			12.5		12.5		↓		3		2			1			↓		↓
		4			12.5		12.5		↓		4	2				1			↓		↓
Short-Circuit Current	I_{SC}	3			-6.5	-15.0	-6.5	-15.0	mAdc											1,2,15,16	3,8
		4			-6.5	-15.0	-6.5	-15.0	mAdc											16	4,8,15
Reverse Current	I_R	1	-			2.0		2.0	μAdc						1					16	8
		2	-			2.0		2.0	↓						2					↓	8,15
	$8I_R$	15				16.0		16.0	↓						15					↓	2,7,8,9,14
Output Leakage Current	I_{CEX}	3				100		100	μAdc								3,16			1,2,15	8
		4				100		100	μAdc								4,16				1,2,8,15
Forward Current	I_F	1				-1.20		-1.20	mAdc					1						15,16	8
		2				-1.20		-1.20	↓					2						1,15,16	8
	$8I_F$	15				-9.60		-9.60	↓											2,7,9,14,16	1,8,15
Power Drain Current (Total Device)	I_{CCH}	16				35			mAdc											16	8
	I_{CCL}	16				35			mAdc											16	1,2,7,8,9,14,15
Switching Times										Pulse In	Pulse Out										
	t_{2+3+}	3				300			ns	2	3		1,15					16			8
	t_{2-3-}	3				300			↓	↓	3		↓					↓			↓
	t_{2-4+}	4				250			↓	↓	4		↓					↓			↓
	t_{2+4-}	4				100			↓	↓	4		↓					↓			↓

Pins not listed are left open.

• Pulse 0 V → 12 V before making test

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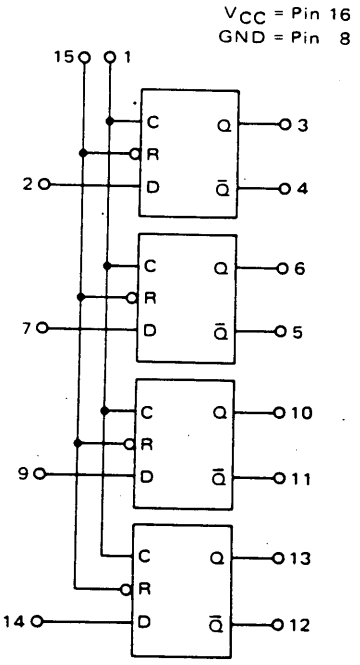
MC682

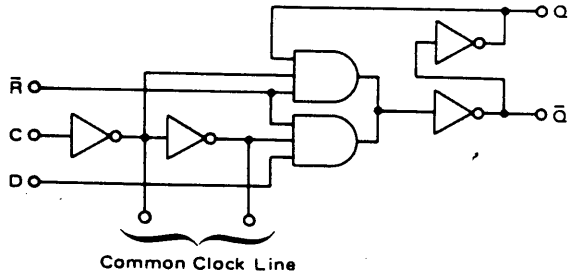
ISSUE A

The MC682 Quad Latch is useful in monitoring or storage applications. A common clock input (C), when in the high state, allows information present at the D input to be transferred to the output of the latch. When C is low, the information present at Q or $\bar{Q}$, will remain at the previous level. A common $\overline{\text{Reset}}$ ($\bar{R}$) input allows resetting of all Q outputs to a logic "0" state independent of C or D.

BLOCK DIAGRAM



LOGIC DIAGRAM
1/4 OF CIRCUIT SHOWN

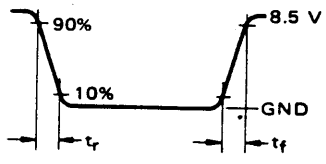


TRUTH TABLE

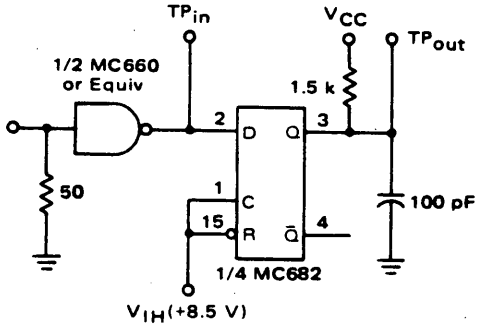
C	D	$\bar{R}$	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	0	1
0	0	1	Q_n	$\bar{Q}_n$
0	1	0	0	1
0	1	1	Q_n	$\bar{Q}_n$
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

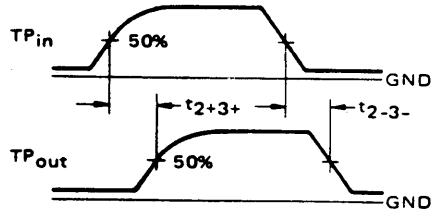
Input Loading Factor:
C, D = 1
$\bar{R}$ = 8
Output Loading Factor = 10
Power Dissipation = 375 mW Typ/pkg

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



$t_r = t_f \leq 20$ ns
f = 100 kHz
Duty Cycle = 50%

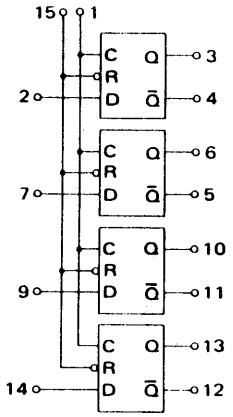




The other outputs are tested in a similar manner.

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one latch. The other latches are tested in a similar manner.



Characteristic	Symbol	Pin Under Test	MC682 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	C_P	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	•	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
Output Voltage	V_{OL}	3	–	1.5	–	1.5	–	1.5	Vdc	3	–	2	–	–	–	1	–	–	16	–	8
		4	–	1.5	–	1.5	–	1.5		4	–	–	2	–	–	1	–	–		–	
	V_{OH}	3	–	–	12.5	–	12.5	–		–	3	–	2	–	–	1	–	–		–	
		4	–	–	12.5	–	12.5	–		–	4	2	–	–	–	1	–	–		–	
Short-Circuit Current	I_{SC}	3	–	–	-6.5	-15.0	-6.5	-15.0	mAdc	–	–	–	–	–	–	–	–	–	–	1,2,15,16	3,8
		4	–	–	-6.5	-15.0	-6.5	-15.0	mAdc	–	–	–	–	–	–	–	–	–	–	16	4,8,15
Reverse Current	I_R	1	–	–	–	2.0	–	2.0	μAdc	–	–	–	–	–	1	–	–	–	–	16	8
		2	–	–	–	2.0	–	2.0		–	–	–	–	–	2	–	–	–	–		8,15
	$8I_R$	15	–	–	–	16.0	–	16.0		–	–	–	–	–	15	–	–	–	–		2,7,8,9,14
Output Leakage Current	I_{CEX}	3	–	–	–	100	–	100	μAdc	–	–	–	–	–	–	–	3,16	–	–	1,2,15	8
		4	–	–	–	100	–	100	μAdc	–	–	–	–	–	–	–	4,16	–	–	–	1,2,8,15
Forward Current	I_F	1	–	–	–	-1.20	–	-1.20	mAdc	–	–	–	–	1	–	–	–	–	–	15,16	8
		2	–	–	–	-1.20	–	-1.20		–	–	–	–	2	–	–	–	–	–	1,15,16	8
	$8I_F$	15	–	–	–	-9.60	–	-9.60		–	–	–	–	–	–	–	–	–	–	2,7,9,14,16	1,8,15
Power Drain Current (Total Device)	I_{CCH}	16	–	–	–	35	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	16	8
	I_{CCL}	16	–	–	–	35	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	16	1,2,7,8,9,14,15
Switching Times										Pulse In	Pulse Out										
	t_{2+3+}	3				300			ns	2	3		1,15					16			8
	t_{2-3-}	3				300					3										
	t_{2-4+}	4				250					4										
	t_{2+4-}	4				100					4										

Pins not listed are left open.

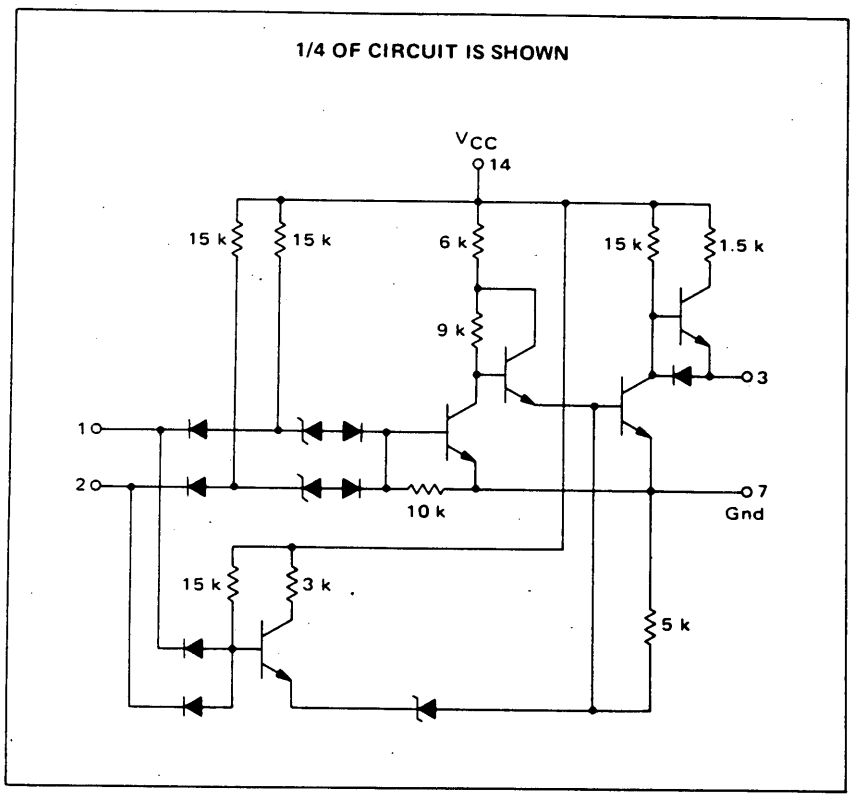
12 V
0 V
before making test

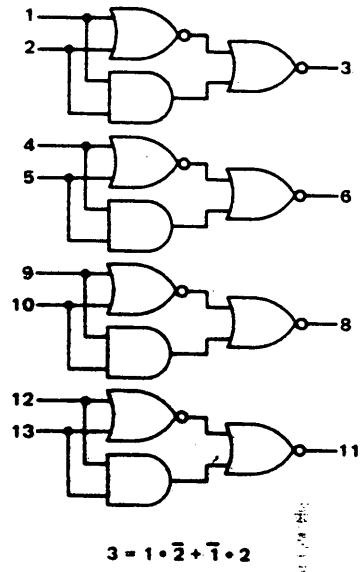
QUAD 2 INPUT
EXCLUSIVE OR GATE

MC683

ISSUE A

Four gate arrays designed to provide four Exclusive OR functions. The output is high only if one input is high and the other input is low.

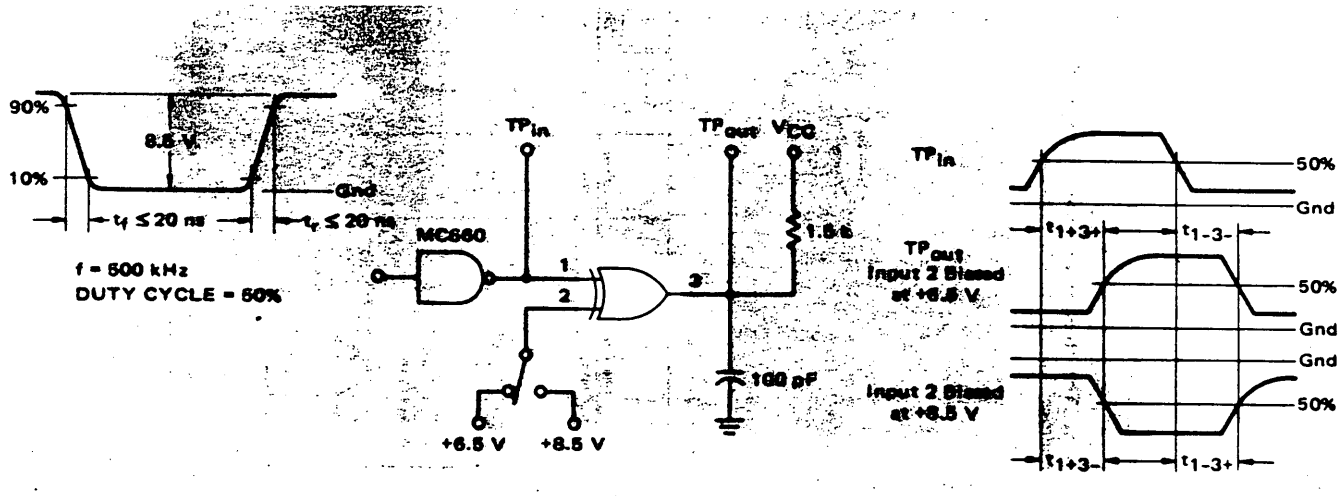




$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

Input Loading Factor = 2
Output Loading Factor = 10
Power Dissipation = 380 mW typ

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



See General Information section for packaging.

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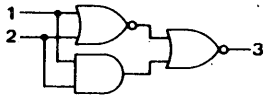
ELECTRICAL CHARACTERISTICS

Test procedures are shown for one gate only. The other gate is tested in the same manner.

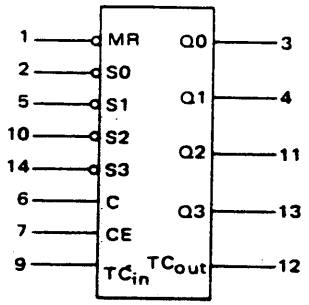


Characteristic	Symbol	Pin Under Test	MC683 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
Output Voltage	V_{OL}	3	–	1.50	–	1.50	–	1.50	Vdc	3	–	–	1,2	–	–	–	–	14	–	7
		3	–	1.50	–	1.50	–	1.50		3	–	1,2	–	–	–	–	–		–	
	V_{OH}	3	–	–	12.5	–	12.5	–		–	3	2	1	–	–	–	–		–	
		3	–	–	12.5	–	12.5	–		–	3	1	2	–	–	–	–		–	
Short-Circuit Current	I_{SC}	3	–	–	-6.50	-15.0	-6.50	-15.0	mAdc	–	–	–	–	–	–	–	2	–	14	1,3,7
Reverse Current	$2I_R$	1	–	–	–	4.0	–	4.0	µAdc	–	–	–	–	–	1	–	–	14	–	7
		2	–	–	–	4.0	–	4.0	µAdc	–	–	–	–	–	2	–	–	14	–	7
Output Leakage Current	I_{CEX}	3	–	–	–	100	–	100	µAdc	–	–	–	–	–	–	3,14	2	–	–	1,7
Forward Current	$2I_F$	1	–	–	–	-2.40	–	-2.40	mAdc	–	–	–	–	1	–	–	–	–	14	7
		2	–	–	–	-2.40	–	-2.40		–	–	–	–	2	–	–	–	–	14	7
Power Drain Current (Total Device)	I_{CCL}	14	–	–	–	35.0	–	–	mAdc	–	–	–	–	–	–	–	–	–	14	1,2,4,5,7,9,10,12,13
	I_{CCH}	14	–	–	–	35.0	–	–	mAdc	–	–	–	–	–	–	–	–	–	14	7
Switching Times										Pulse In	Pulse Out									
Input 2 Biased at +6.5 V	t_{1+3+}	1,3	–	–	–	300	–	–	ns	1	3	2	–	–	–	–	14	–	–	7
	t_{1-3-}		–	–	–	100	–	–				2	–	–	–	–		–	–	
Input 2 Biased at +8.5 V	t_{1+3-}		–	–	–	100	–	–				–	2	–	–	–		–		
	t_{1-3+}		–	–	–	300	–	–				–	2	–	–	–		–	–	

Pins not listed are left open.

MC684

ISSUE C



The MC684 high threshold decade counter consists of four J-K flip-flops plus additional gating to accomplish the counter function. The flip-flops change state on the negative transition of the clock pulse.

An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of the state of the clock. Each flip-flop is provided with an individual set ($\overline{S}$) input which permits any flip-flop or combination of flip-flops to be set by applying a low level to the appropriate set inputs when the clock is low. One may also set the outputs by applying a low level to the set inputs when the master reset ($\overline{MR}$) pin is low, then taking $\overline{MR}$ high before the set pins are taken high.

Inputs CE, TC_{in} and output TC_{out} are useful in cascading counters. TC_{out} provides an output pulse each time the counter reaches its maximum count. All unused inputs should be connected to V_{CC}. The MC684 is self-correcting for BCD states from 10 thru 15.

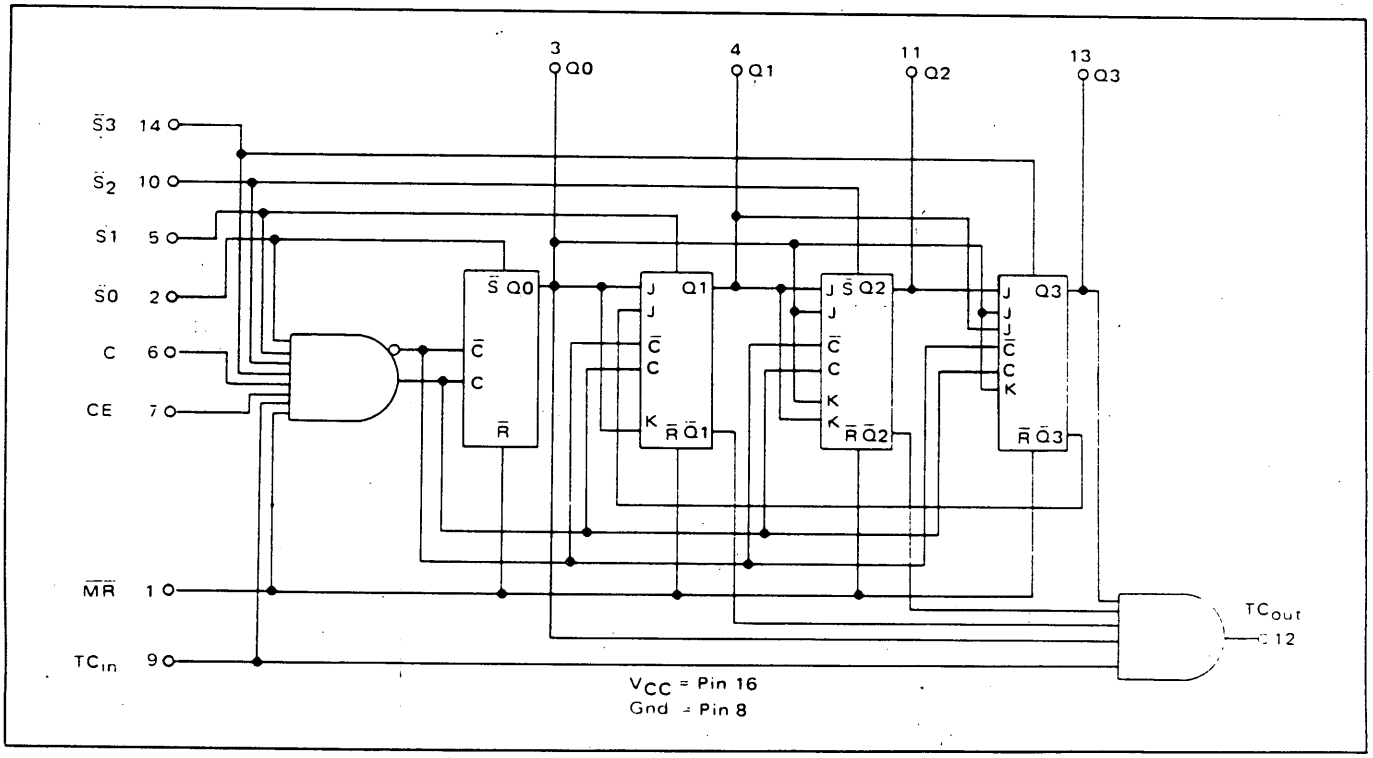
V_{CC} = Pin 16
Gnd = Pin 8

Input Loading Factors:
$\overline{MR}$ = 5
Clock, CE = 1
TC_{in}, S0, S1, S2, S3 = 2
Output Loading Factor = 10
Total Power Dissipation = 480 mW typ/pkg
Toggle Frequency = 0.5 MHz min

COUNT SEQUENCE TRUTH TABLE

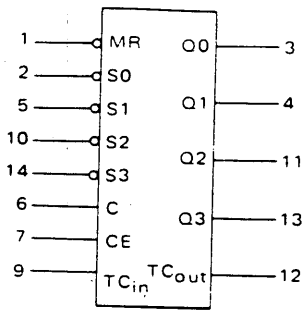
COUNT	OUTPUT				
	T_C	Q3	Q2	Q1	Q0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	1	1	0	0	1

LOGIC DIAGRAM



See General Information section for packaging.

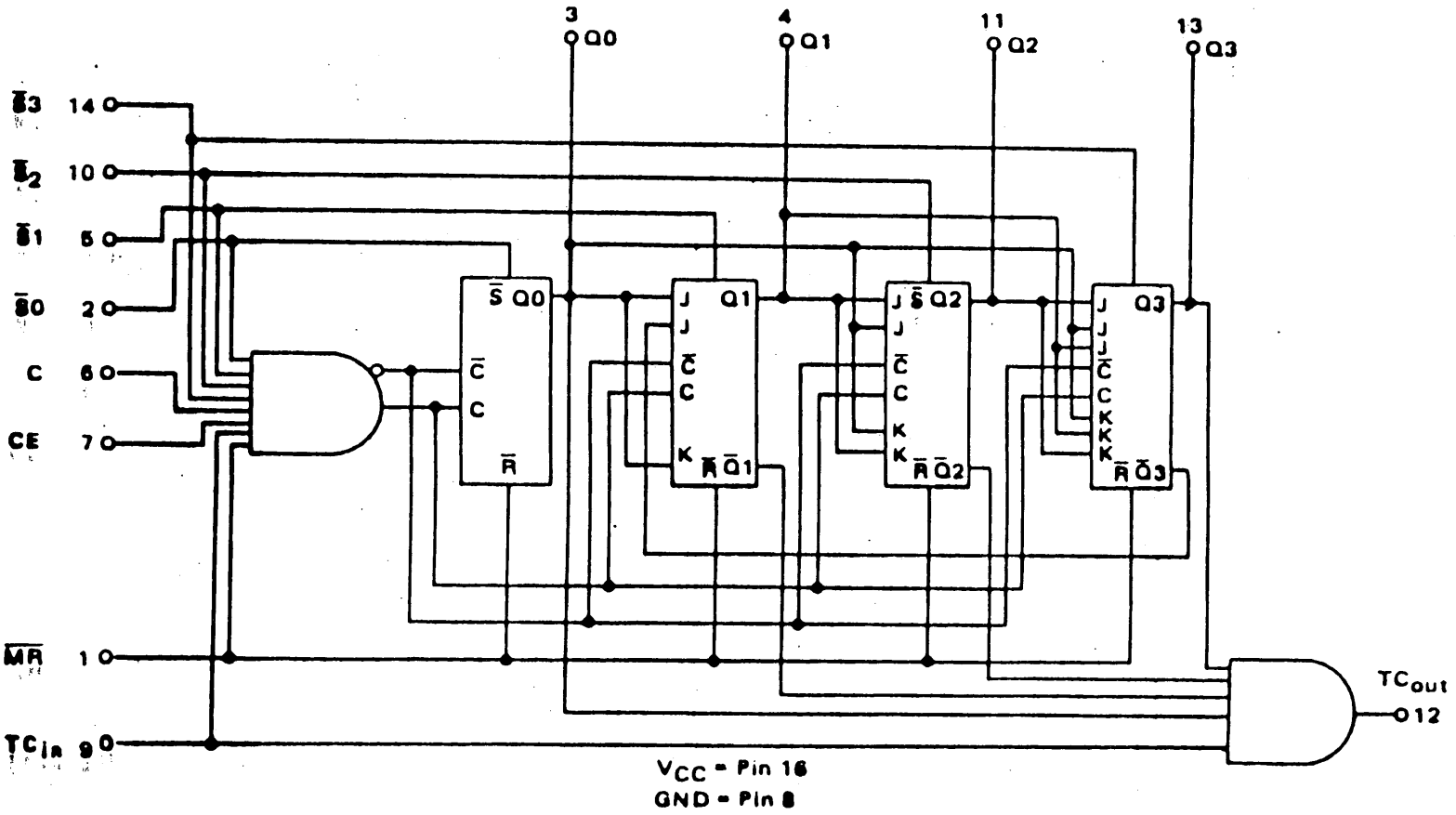
ELECTRICAL CHARACTERISTICS



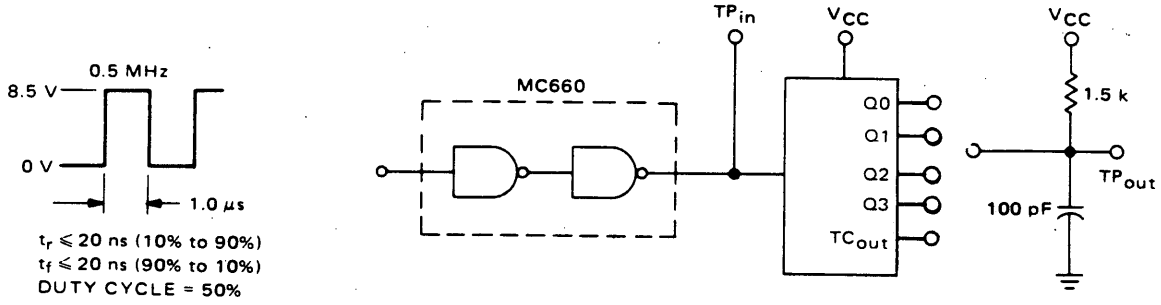
Characteristic	Symbol	Pin Under Test	MC684 Test Limits -30°C Min	-30°C Max	-25°C Min	-25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:										
Output Voltage	V_{OL}	3,4,11,12,13		1.5		1.5		1.5	Vdc			1						16		8
	V_{OH}	3,4,11,12,13	12.5		12.5				Vdc		3,4,11,12,13	2,5,10,2,14,14	5,6,7,9,10					16		8
Short Circuit Current	I_{SC}	3,4,11,12,13	-6.5	-15.0	-6.5	-15.0			mAdc			2,5,10,2,14,14	5,6,7,9,10						16	8
Reverse Current	I_R	6,7		2.0		2.0			μAdc						6,7			16		8
	$2I_R$	2,5,9,10,14		4.0		4.0									2,5,9,10,14					
	$5I_R$	1		10.0		10.0									1					
Output Leakage Current	I_{CEX}	3,4,11,12,13		100		100			μAdc			2,5,10,2,14,14	5,6,7,9,10			3,16,4,16,11,16,12,16,13,16				8
Forward Current	I_F	6,7		-1.20		-1.20			mAdc					6,7					16	8
	$2I_F$	2,5,9,10,14		-2.40		-2.40								2,5,9,10,14						
	$5I_F$	1		-6.0		-6.0								1						
Power Supply Current	I_{CCH}	16		45					mAdc										16	8
Data Sheet	I_{CCL}	16		45					mAdc										16	2,5,6,7,8,9,10,14
Switching Parameters						Typ				Pulse In	Pulse Out									
Clock to Q	t_{CQ}	6,3				170			ns	6	3					16				8
Clock to Q	t_{CQ}	6,3				300					3									
Turn On Delay TC	t_{on}	6,12				220					12									
Turn Off Delay TC	t_{off}	6,12				400					12									

MC 684 DECADE COUNTER

LOGIC DIAGRAM

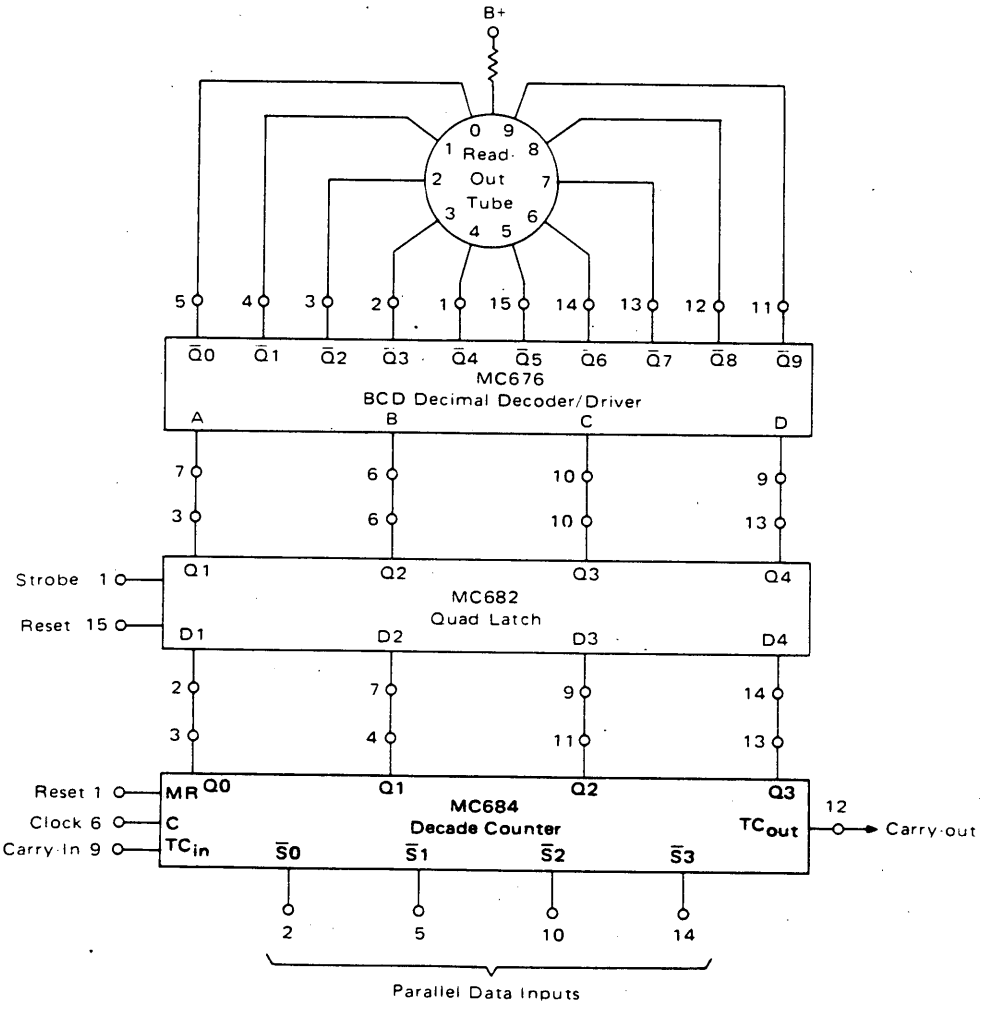


TOGGLE MODE TEST CIRCUIT

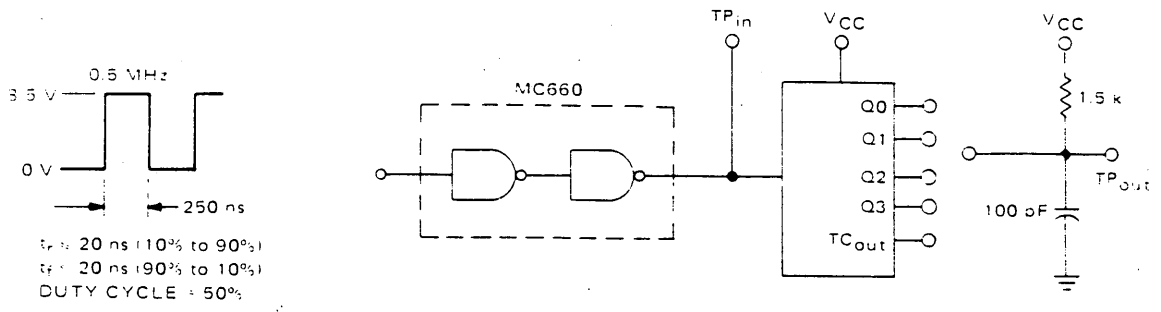


Waveform at TP_{out} must conform to truth table

TYPICAL INTERCONNECTION DIAGRAM

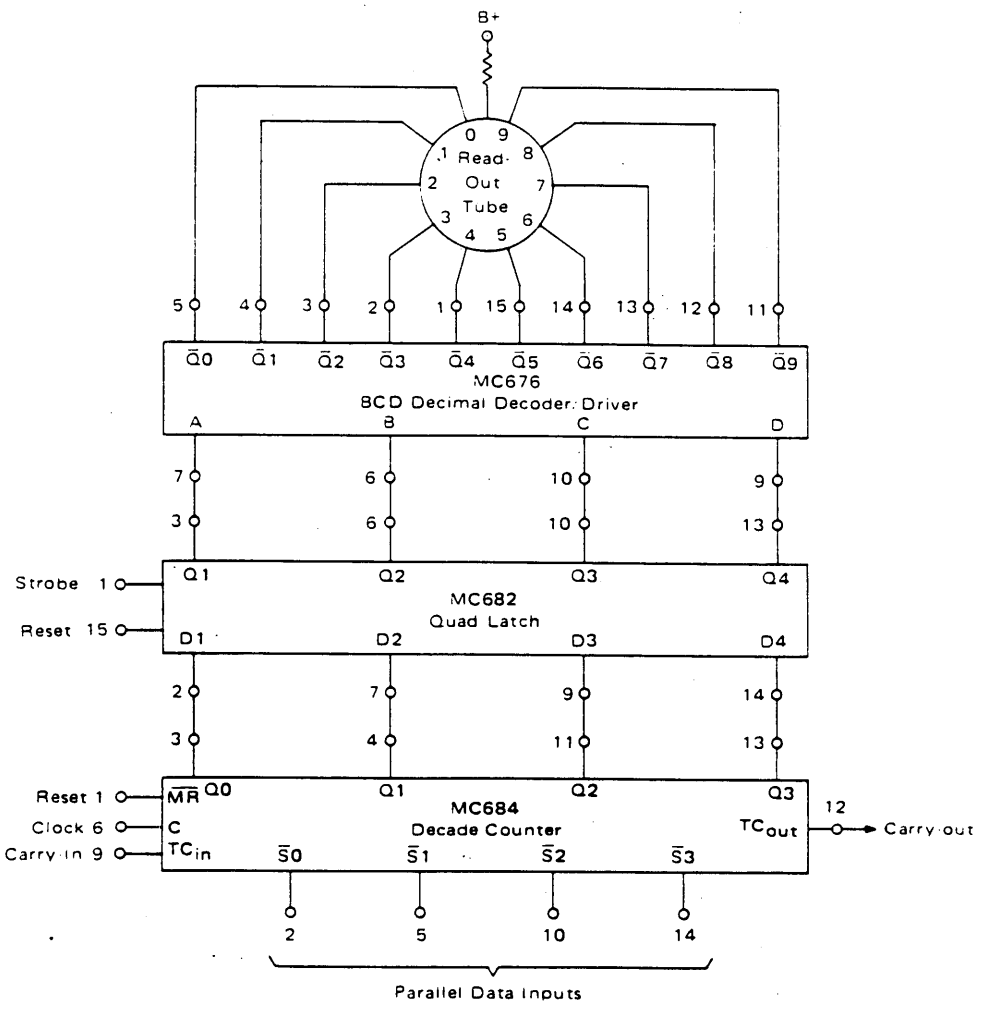


TOGGLE MODE TEST CIRCUIT



Waveform at TP_{out} must conform to truth table

TYPICAL INTERCONNECTION DIAGRAM



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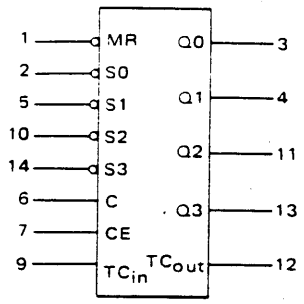
MC685



V_{CC} = Pin 16
Gnd = Pin 8

Input Loading Factors:
$\overline{MR}$ = 5
Clock, CE = 1
TC_{in}, $\overline{S}0$, $\overline{S}1$, $\overline{S}2$, $\overline{S}3$ = 2

Output Loading Factor = 10

Total Power Dissipation = 480 mW typ/pkg

Toggle Frequency = 0.5 MHz min

The MC685 high threshold binary counter consists of four J-K flip-flops plus additional gating to accomplish the counter function. The flip-flops change state on the negative transition of the clock pulse.

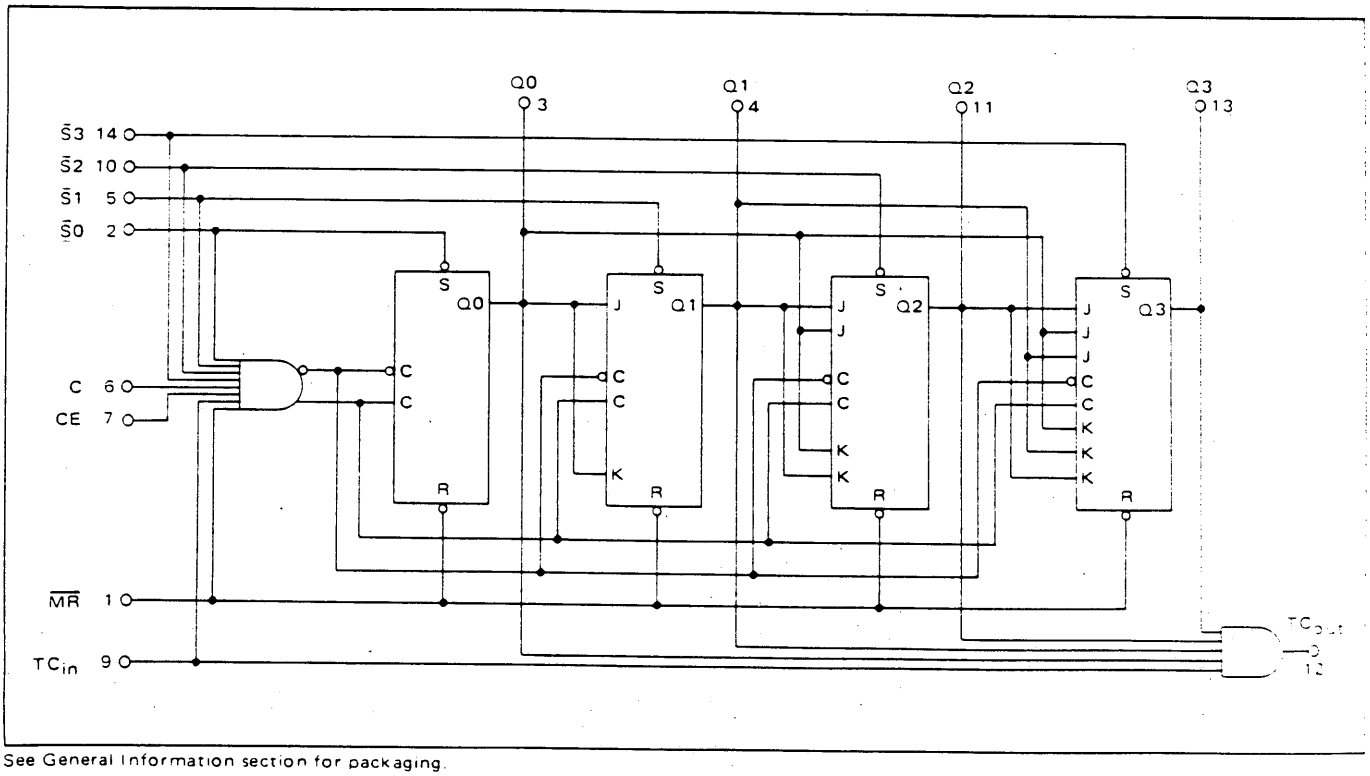
An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of the state of the clock. Each flip-flop is provided with an individual set ($\overline{S}$) input which enables any flip-flop to be set regardless of the state of the clock.

Inputs CE, TC_{in} and output TC_{out} are useful in cascading counters. TC_{out} provides an output pulse each time the counter reaches its maximum count. Negative transitions of CE and TC_{in} should occur when the clock is low to avoid incrementing the counter. All unused inputs should be connected to V_{CC}.

COUNT SEQUENCE TRUTH TABLE

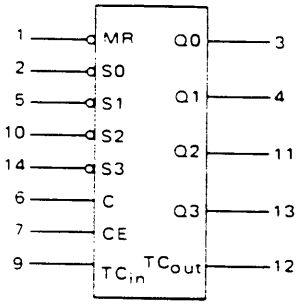
COUNT	OUTPUT				
	TC	Q3	Q2	Q1	Q0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	1	1	1	1	1

LOGIC DIAGRAM



See General Information section for packaging.

ECTRICAL CHARACTERISTICS

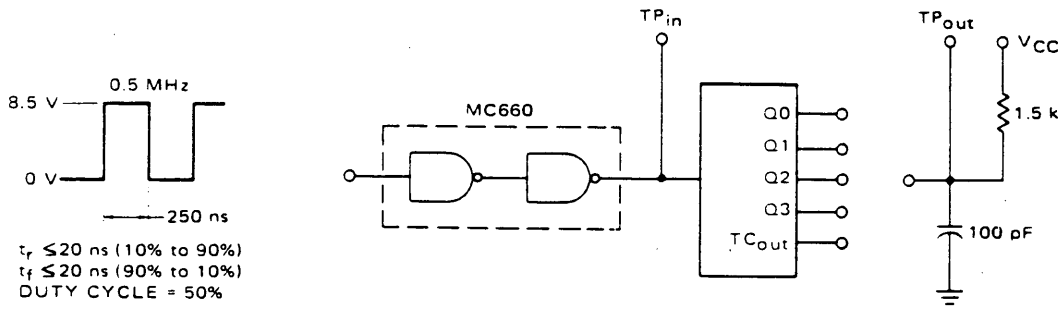


BEST COPY

Characteristic	Symbol	Pin Under Test	MC685 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA IOL	mA IOH	Volts VIL	Volts VIH	Volts VF	Volts VR	Volts VCEX	Volts VCC	Volts VCCL	Volts VCCH	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
Output Voltage	V_{OL}	3	-	1.5	-	1.5		1.5	Vdc	3		1						16		8
		4								4										
		11								11										
		12								12										
		13		▼		▼		▼	▼	13		▼						▼		▼
	V_{OH}	3			12.5		12.5		Vdc		3	2						16		8
		4									4	5								
		11									11	10								
		12									12	2,14	5,6,7, 9,10							
		13		▼		▼		▼	▼		13	14						▼		▼
Short Circuit Current	I_{SC}	3			-6.5	-15.0	-6.5	-15.0	mAdc			2						16		8
		4										5								
		11										10								
		12										2,14	5,6,7, 9,10							
		13		▼		▼		▼	▼			14						▼		▼
Reverse Current	I_R	6			-	2.0		2.0	μAdc						6			16		8
		7				2.0		2.0							7					
	D_R	2				4.0		4.0							2					
		5													5					
		9													9					
		10													10					
		14				▼		▼							14					
	B_R	1				10.0		10.0	▼						1			▼		▼
Output Leakage Current	I_{CEX}	3				100		100	μAdc			2				3,10				8
		4										5				4,13				
		11										10				11,16				
		12										2,14	5,6,7, 9,10			12,16				
		13				▼		▼	▼			14				12,16				▼
Forward Current	I_F	6				-1.20		-1.20	mAdc					6					16	8
		7				-1.20		-1.20						7						
	D_F	2				-2.40		-2.40						2						
		5												5						
		9												9						
		10												10						
		14				▼		▼						14						
	B_F	1				-6.0		-6.0	▼					1					▼	▼
Power Drain Current Total Device	I_{CCH}	16				40			mAdc										16	8
	I_{CCL}	16				40			mAdc										16	8,5,7,9,10,14

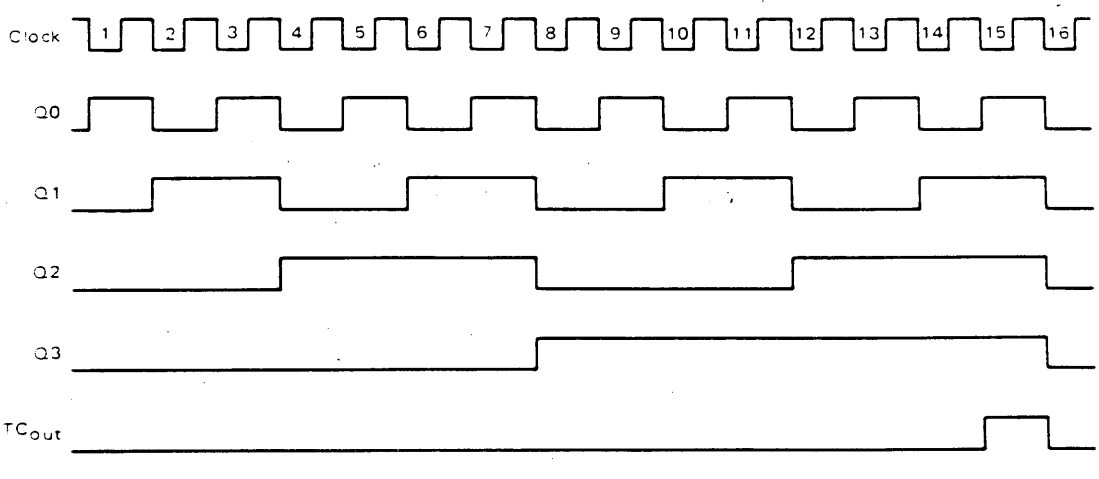
Switching Parameters			Typ		Pulse In	Pulse Out				
Turn-On Delay - Q	t_{pd+}	6,3	170	ns	6	3		16		8
Turn-Off Delay - Q	t_{pd-}	6,3	300			3				
Turn-On Delay - TC	t_{pd+}	9,12	220			12				
Turn-Off Delay - TC	t_{pd-}	9,12	400	▼	▼	12	▼		▼	

TOGGLE MODE TEST CIRCUIT



Waveform at TP_{out} must conform to truth table

TYPICAL COUNTER WAVEFORMS



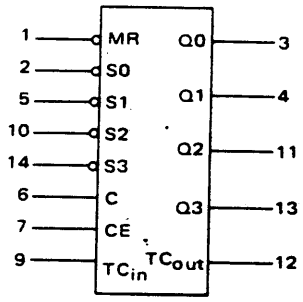
MC685

ISSUE C

The MC685 high threshold binary counter consists of four J-K flip-flops plus additional gating to accomplish the counter function. The flip-flops change state on the negative transition of the clock pulse.

An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of the state of the clock. Each flip-flop is provided with an individual set (S) input which permits any flip-flop or combination of flip-flops to be set by applying a low level to the appropriate set inputs when the clock is low. One may also set the outputs by applying a low level to the set inputs when the master reset ($\overline{MR}$) pin is low, then, taking $\overline{MR}$ high before the set pins are taken high.

Inputs CE, TC_{in} and output TC_{out} are useful in cascading counters. TC_{out} provides an output pulse each time the counter reaches its maximum count. Negative transitions of CE and TC_{in} should occur when the clock is low to avoid incrementing the counter. All unused inputs should be connected to V_{CC}.



V_{CC} = Pin 16
Gnd = Pin 8

Input Loading Factors:
$\overline{MR}$ = 5
Clock, CE = 1
TC_{in}, $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{S3}$ = 2

Output Loading Factor = 10

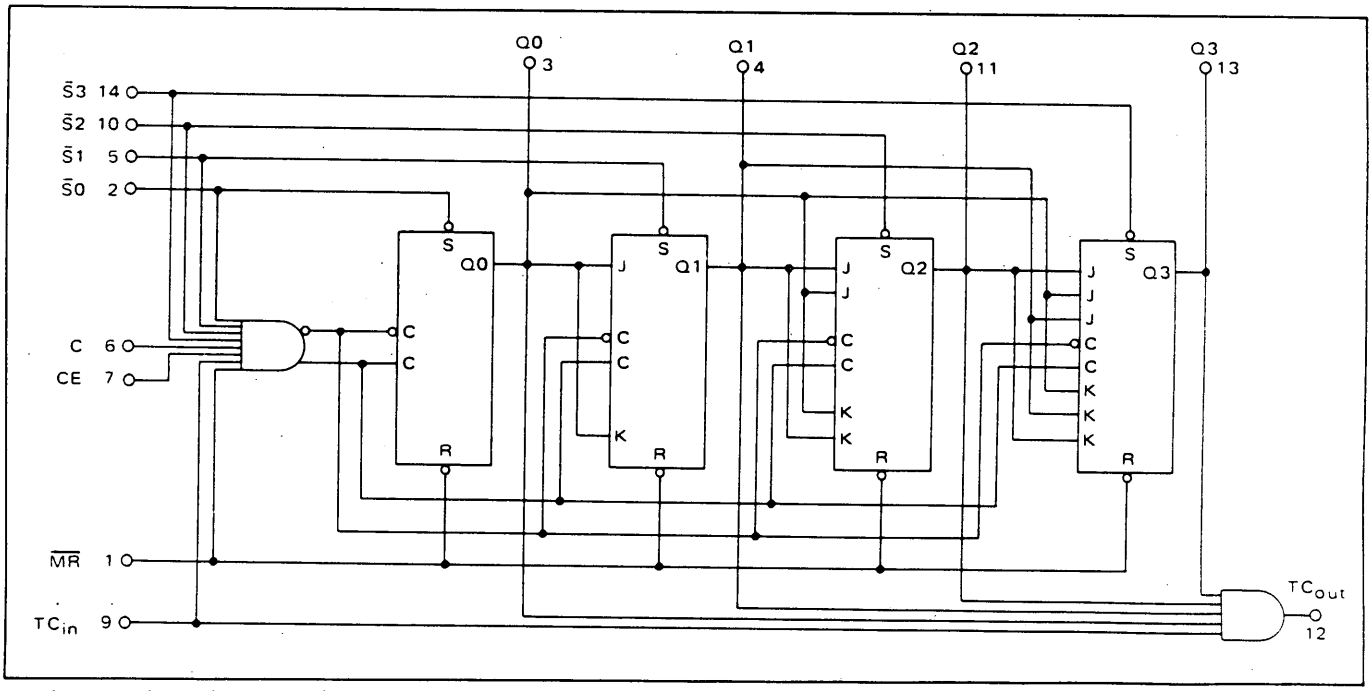
Total Power Dissipation = 480 mW typ/pkg

Toggle Frequency = 0.5 MHz min

COUNT SEQUENCE TRUTH TABLE

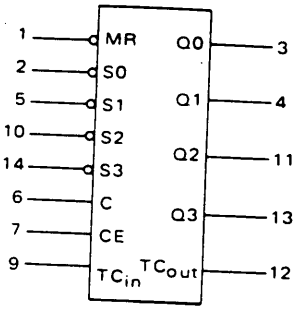
COUNT	OUTPUT				
	TC	Q3	Q2	Q1	Q0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	1	1	1	1	1

LOGIC DIAGRAM



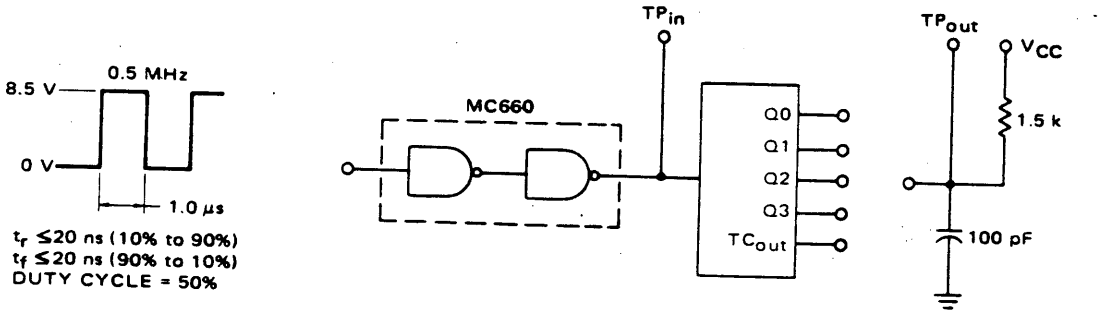
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS



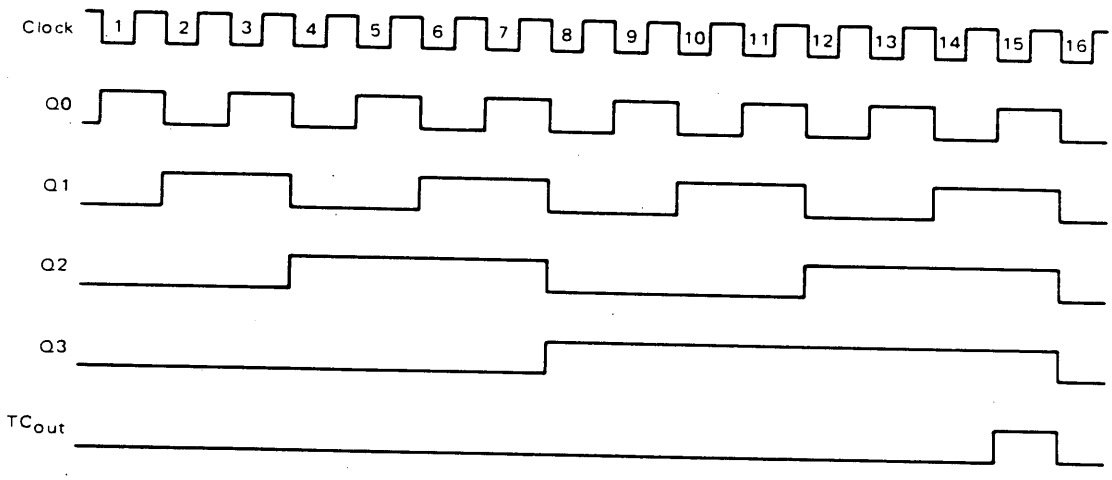
Characteristic	Symbol	Pin Under Test	MC685 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	I_{OH}	Volts V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}
										12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0
Characteristic	Symbol	Pin Under Test								TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3		1								
		4	-	↓	-	↓	-	↓	↓	4		↓						16	-	8
		11	-		-		-			11								↓	↓	↓
		12	-		-		-			12										
		13	-		-		-			13										
	V_{OH}	3	-	-	12.5	-	12.5	-	Vdc	-	3	2								
		4	-	-	↓	-	↓	-	↓		4	5						16	-	8
		11	-	-		-		-			11	10						↓	-	↓
		12	-	-		-		-			12	2,5, 10,14	6,7,9							
		13	-	-		-		-			13	14								
Short Circuit Current	I_{SC}	3	-	-	-6.5	-15.0	-6.5	-15.0	mAdc			2								
		4	-	↓	↓	↓	↓	↓	↓			5						-	16	8
		11	-									10						-	↓	↓
		12	-									2,14	5,6,7, 9,10					-		
		13	-									14						-		
Reverse Current	I_R	6	-			2.0		2.0	μAdc											
		7	-			2.0		2.0	↓					-	6			16	-	3
	$2I_R$	2	-			4.0		4.0							7					↓
		5	-			↓		↓							2					
		9	-												5					
		10	-												9					
		14	-												10					
	$5I_R$	1				10.0		10.0							14					
															1					
Output Leakage Current	I_{CEX}	3				100		100	μAdc			2				3,16				
		4				↓		↓	↓			5				4,16				8
		11										10				11,16				↓
		12										2,14	5,6,7, 9,10			12,16				
		13										14				13,16				
Forward Current	I_F	6				-1.20		-1.20	mAdc											
		7				-1.20		-1.20	↓					6					16	8
	$2I_F$	2				-2.40		-2.40						7						↓
		5				↓		↓						2						
		9												5						
		10												9						
		14												10						
	$5I_F$	1				-6.0		-6.0						14						
														1						
Power Drain Current (Total Device)	I_{CCH}	16				45			mAdc										16	8
	I_{CCL}	16				45			mAdc										16	8
Switching Parameters						Typ				Pulse In	Pulse Out									2,5,6,7,8, 9,10,14
Turn-On Delay Q	t_{pd-}	6,3				170			ns	6	3									
Turn-Off Delay Q	t_{pd+}	6,3				300					3						16			8
Turn-On Delay TC	t_{pd-}	6,12				220					12									
Turn-Off Delay TC	t_{pd+}	6,12				400			↓	↓	12						↓			↓

TOGGLE MODE TEST CIRCUIT



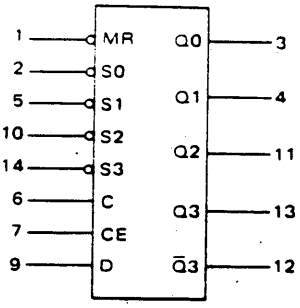
Waveform at TP_{out} must conform to truth table

TYPICAL COUNTER WAVEFORMS



MC686

ISSUE



V_{CC} = Pin 16
Gnd = Pin 8

Input Loading Factors:
$\overline{MR}$ = 5
Clock, CE = 1
D, $\overline{S}0$, $\overline{S}1$, $\overline{S}2$, $\overline{S}3$ = 2

Output Loading Factor = 10

Total Power Dissipation = 480 mW typ/pkg

Toggle Frequency = 0.5 MHz min

The MC686 high-threshold shift register consists of four J-K flip-flops connected in serial fashion. The flip-flops change state on the negative transition of the clock pulse. Q outputs are available from all four stages, and $\overline{Q}$ from the last register stage.

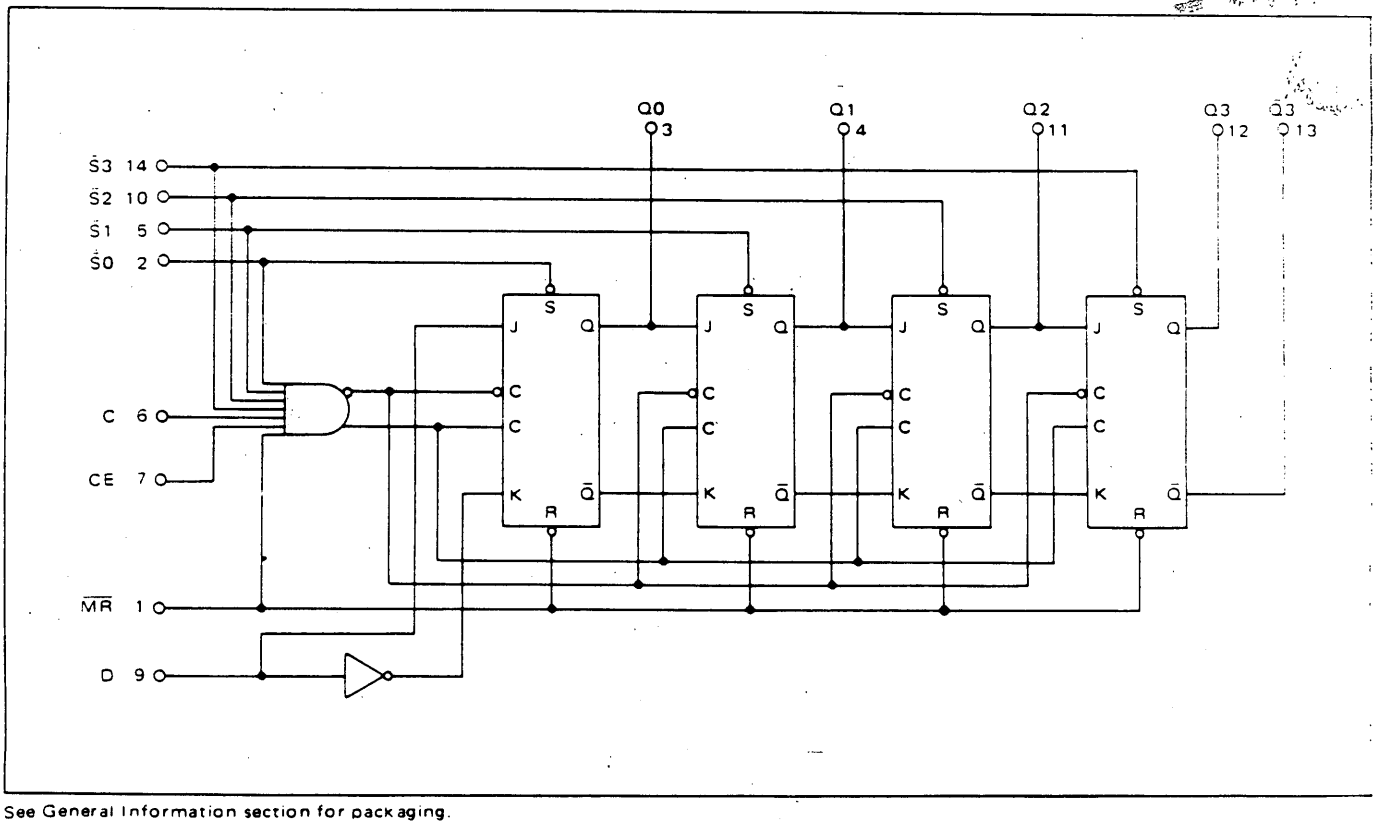
An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of the state of the clock. Each flip-flop is provided with an individual set input ($\overline{S}$) which enables any flip-flop to be set regardless of the state of the clock.

The clock enable (CE) control provides a means of inhibiting the clock input. Negative transitions of CE should occur when the clock is low to avoid shifting the register. All unused inputs should be connected to V_{CC}.

TRUTH TABLE

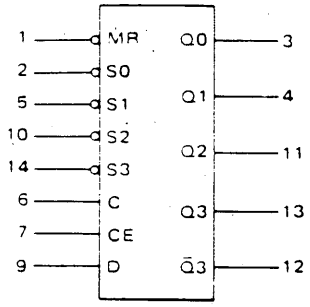
COUNT	D	Q3	Q2	Q1	Q0
0	1	0	0	0	0
1	1	0	0	0	1
2	1	0	0	1	1
3	1	0	1	1	1
4	1	1	1	1	1
0	0	1	1	1	1
1	0	1	1	1	0
2	0	1	1	0	0
3	0	1	0	0	0
4	0	0	0	0	0

LOGIC DIAGRAM



See General Information section for packaging.

ELECTRICAL CHARACTERISTICS



BEST COPY

Characteristic	Symbol	Pin Under Test	MC686 Test Limits -30°C Min	-30°C Max	-25°C Min	-25°C Max	-75°C Min	-75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL} (mA)	I_{OH} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_F (Volts)	V_R (Volts)	V_{CEX} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)	Gnd
										TEST CURRENT/VOLTAGE VALUES (All Temperatures): 12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
Output Voltage	V_{OL}	3	-	1.5	-	1.5	-	1.5	Vdc	3	-	1	-	-	-	-	-	16	-	8
		4	-	↓	-	↓	-	↓	↓	4								↓		↓
		11	-		-		-			11										
		13	-		-		-			13										
		12	-	↓	-	↓	-	↓	↓	12		↓4		-	-	-	-	↓	-	↓
	V_{OH}	3	-	-	12.5	-	-	-		-		-	-	-	-	-	-	16	-	8
		4	-	-	↓	-	-	-		-		-	-	-	-	-	-	↓	-	↓
		11	-	-		-	-	-		-		-	-	-	-	-	-		-	
		12	-	-		-	-	-		-		-	-	-	-	-	-		-	
		13	-	-	↓	-	-	-		-		-	-	-	-	-	-	↓	-	↓
Short Circuit Current	I_{SC}	3	-	-	-6.5	-15.0	-	-		-		-	-	-	-	-	-	16	-	8
		4	-	-	↓	↓	-	-		-		-	-	-	-	-	-	↓	-	↓
		11	-	-			-	-		-		-	-	-	-	-	-		-	
		13	-	-			-	-		-		-	-	-	-	-	-		-	
		12	-	-	↓	↓	-	-		-		-	-	-	-	-	-	↓	-	↓
Reverse Current	I_R	6	-	-		2.0	-	-		-		-	-	-	6	-	-	16	-	8
		7				2.0									7			↓		↓
	$2I_R$	2				4.0									2					
		5				↓									5					
		9													9					
		10													10					
		14													14					
	$5I_R$	1	-	-		↓ 10.0	-	-		-		-	-	-	1	-	-	↓	-	↓
Output Leakage Current	I_{CEX}	3				100						2				3,16				8
		4				↓						5				4,16				↓
		11										10				11,16				
		13										14	-			12,16				
		12				↓		↓	↓			1			-	13,16				↓
Forward Current	I_F	6				-1.20		-1.20	mAdc			-		6	-	-			16	8
		7				-1.20		-1.20				-		7						↓
	$2I_F$	2				-2.40	-	-2.40				-	-	2	-		-			
		5										-	-	5	-		-			
		9	-	-	-		-			-	-	-	-	9	-		-			
		10	-	-	-		-					-	-	10	-		-			
		14			-		-						-	14	-		-			
	$5I_F$	1	-	-	-	-6.0	-	-6.0	↓	-	-	-	-	1	-	-	-		↓	↓
Power Drain Current Total Device:	I_{CCH}	16	-	-	-	40	-	-	mAdc	-	-	-	-	-	-	-	-		16	8
	I_{CCL}	16	-	-	-	40	-	-	mAdc	-	-	-	-	-	-	-	-		16	2,5,6,7,13,9,10,14
Switching Parameters						Typ				Pulse In		Pulse Out								
Turn-On Delay Q	t_{pd-}	6.3	-	-	-	170	-		ns	6		3		-	-	-	16			8
Turn-Off Delay Q	t_{pd-}	6.3	-	-	-	300	-		ns	6		3		-	-	-	16	-	-	8

PUNCH HOLES SO THIS SIDE WILL BE THE LAST PAGE OF THIS DATA SHEET

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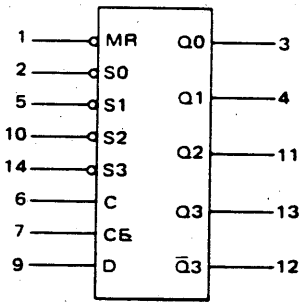
MC686

ISSUE C



V_{CC} = Pin 16
Gnd = Pin 8

The MC686 high-threshold shift register consists of four J-K flip-flops connected in serial fashion. The flip-flops change state on the negative transition of the clock pulse. Q outputs are available from all four stages, and $\overline{Q}$ from the last register stage.

An asynchronous master reset ($\overline{MR}$) clears all flip-flops regardless of the state of the clock. Each flip-flop is provided with an individual set input ($\overline{S}$) which permits any flip-flop or combination of flip-flops to be set by applying a low level to the appropriate set inputs when the clock is low. One may also set the outputs by applying a low level to the set inputs when the master reset ($\overline{MR}$) pin is low, then, taking $\overline{MR}$ high before the set pins are taken high.

The clock enable (CE) control provides a means of inhibiting the clock input. Negative transitions of CE should occur when the clock is low to avoid shifting the register. All unused inputs should be connected to V_{CC}.

Input Loading Factors:
$\overline{MR}$ = 5
Clock, CE = 1
D, $\overline{S}0$, $\overline{S}1$, $\overline{S}2$, $\overline{S}3$ = 2

Output Loading Factor = 10

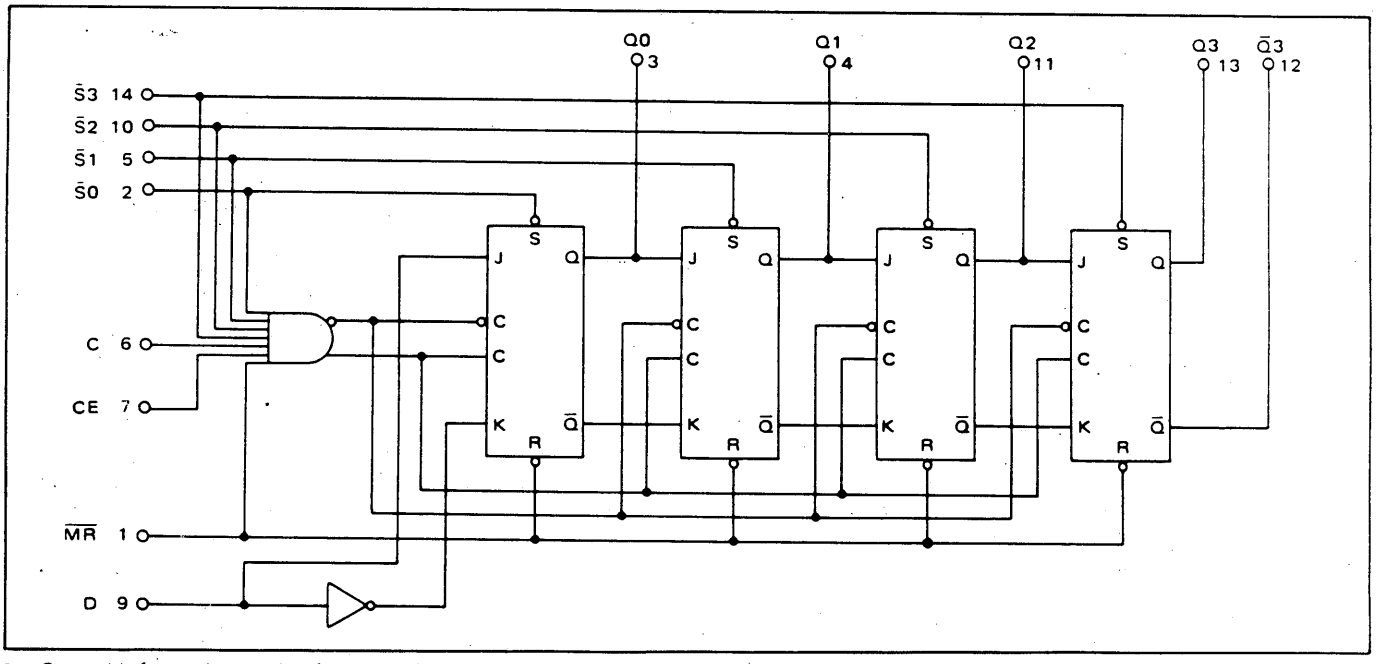
Total Power Dissipation = 480 mW typ/pkg

Toggle Frequency = 0.5 MHz min

TRUTH TABLE

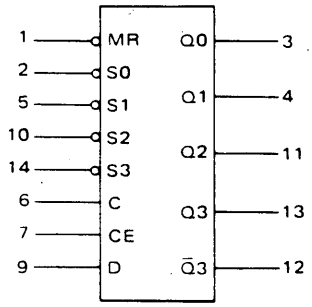
COUNT	D	Q3	Q2	Q1	Q0
0	1	0	0	0	0
1	1	0	0	0	1
2	1	0	0	1	1
3	1	0	1	1	1
4	1	1	1	1	1
0	0	1	1	1	1
1	0	1	1	1	0
2	0	1	1	0	0
3	0	1	0	0	0
4	0	0	0	0	0

LOGIC DIAGRAM



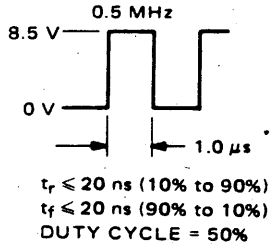
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

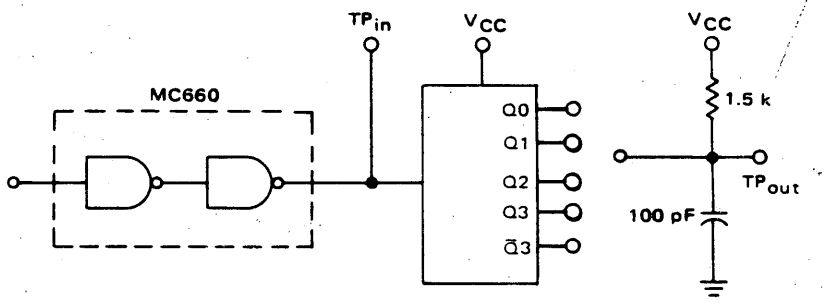


TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
mA		Volts							
I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}
12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0

Characteristic	Symbol	Pin Under Test	MC686 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL}	3		1.5		1.5		1.5	Vdc	3		1						16		8
		4								4										
		11								11										
		13								13										
		12								12		14								
	V_{OH}	3			12.5		12.5		Vdc		3	2						16		8
		4									4	5								
		11									11	10								
		12									12	1								
		13									13	14								
Short Circuit Current	I_{SC}	3			-6.5	-15.0	-6.5	-15.0	mAdc			2							16	8
		4										5								
		11										10								
		13										14								
		12										1								
Reverse Current	I_R	6				2.0		2.0	µAdc						6			16		8
		7				2.0		2.0							7					
	$2I_R$	2				4.0		4.0							2					
		5													5					
		9													9					
		10													10					
		14													14					
	$5I_R$	1				10.0		10.0							1					
Output Leakage Current	I_{CEX}	3				100		100	µAdc			2				3,16				3
		4										5				4,16				
		11										10				11,16				
		13										14				12,16				
		12										1				13,16				
Forward Current	I_F	6				-1.20		-1.20	mAdc					6					16	3
		7				-1.20		-1.20						7						
	$2I_F$	2				-2.40		-2.40						2						
		5												5						
		9												9						
		10												10						
		14												14						
	$5I_F$	1				-6.0		-6.0						1						
Power Drain Current (Total Device)	I_{CCH}	16				45			mAdc										16	8
	I_{CCL}	16				45			mAdc										16	2,5,6,7,8, 9,10,14
Switching Parameters						Typ				Pulse In		Pulse Out								
Turn-On Delay - Q	t_{pd-}	6,3				170			ns	6		3					16			8
Turn-Off Delay - Q	t_{pd+}	6,3				300			ns	6		3					16			8



$t_r \leq 20$ ns (10% to 90%)
$t_f \leq 20$ ns (90% to 10%)
DUTY CYCLE = 50%



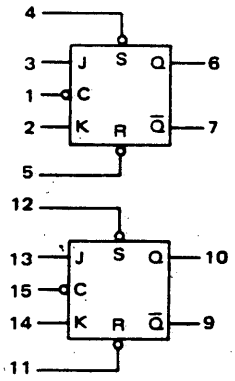
Waveform at TP_{out} must conform to truth table

MC688

ISSUE A

This negative-edge-clocked dual J-K flip-flop operates on the master-slave principle. This device provides both $\overline{SET}$ and $\overline{RESET}$ inputs on both flip-flops in the package. Each flip-flop may be set or reset by applying a low level to that particular input when the clock is low.

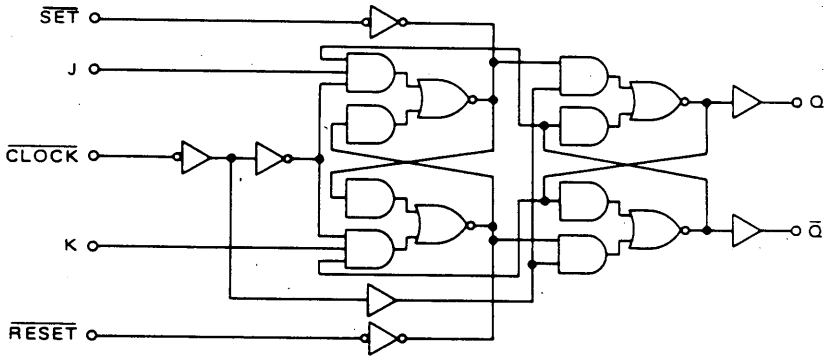
The J and K inputs are inhibited when the clock is low and enabled when the clock is high. The logical state of the J and K inputs MUST NOT be allowed to change when the clock is in the high state.



V_{CC} = Pin 16
Gnd = Pin 8

Input Loading Factor:
$\overline{R}$, $\overline{S}$ Inputs = 2
Other Inputs = 1
Output Loading Factor = 10
f_{Tog} = 2.6 MHz typ
Total Power Dissipation = 375 mW typ

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN



TRUTH TABLE

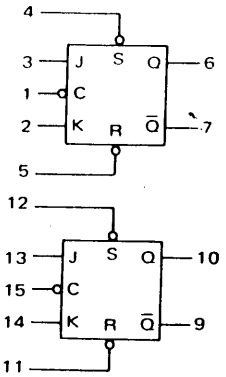
R	S	t_n J	t_n K	t_{n+1} Q	t_{n+1} $\overline{Q}$
0	1	x	x	0	1
1	0	x	x	1	0
1	1	0	0	Q_n	$\overline{Q}_n$
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	$\overline{Q}_n$	Q_n

0 = Low state
1 = High state
x = Don't care
t_n = Time period prior to negative transition of clock pulse.
t_{n+1} = Time period subsequent to negative transition of clock pulse.
Q_n = State of Q output in time period t_n.
• = Clock pulse must be in low state

See General Information section for packaging.

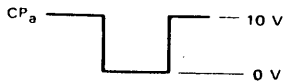
ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.

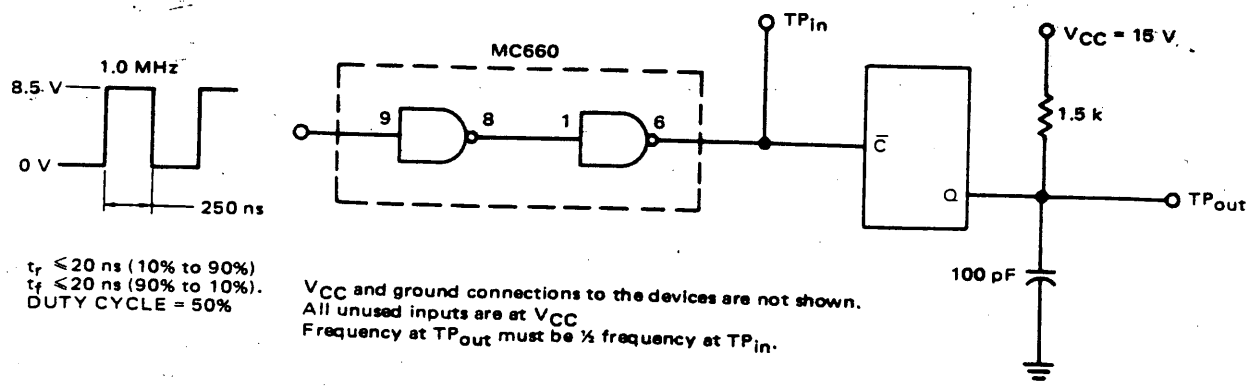


Characteristic	Symbol	Pin Under Test	MC688 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CCL}	V_{CCH}	V_{CC}	V_{CEX}	CP_a	Gnd
										TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA		Volts									
										12.0	-0.03	6.50	8.50	1.5	16.0	14.0	16.0	15.0	16.0		
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
Output Voltage	V_{OL}	6	–	1.5	–	1.5	–	1.5	Vdc	6	–	1,5	2,3,4	–	–	16	–	–	–	–	8
		7	–	↓	–	↓	–	↓	↓	7	–	1,4	2,3,5	–	–	↓	–	–	–	–	↓
		6	–		–		–			6	–	3	2,4,5	–	–		–	–	–	1	
		7	–		–		–			7	–	2	3,4,5	–	–		–	–	–	1	
	V_{OH}	6	12.5	–	12.5	–	12.5	–	Vdc	–	6	1,4	2,3,5	–	–	16	–	–	–	–	8
		7	↓	–	↓	–	↓	–	↓	–	7	1,5	2,3,4	–	–	↓	–	–	–	–	↓
		6		–		–		–		–	6	2	3,4,5	–	–		–	–	–	1	
		7		–		–		–		–	7	3	2,4,5	–	–		–	–	–	1	
Leakage Current	I_{CEX}	6	–	–	–	100	–	100	μAdc	–	–	–	–	–	–	–	–	2,3,5	6,16	–	1,4,8
		7	–	–	–	100	–	100	μAdc	–	–	–	–	–	–	–	–	2,3,5	7,16	–	1,5,8
Short Circuit Current	I_{SC}	6	-6.5	-15	-6.5	-15	-6.5	-15	mAdc	–	–	–	–	–	–	16	–	2,3,5		–	1,4,8,6
		7	-6.5	-15	-6.5	-15	-6.5	-15	mAdc	–	–	–	–	–	–	16	–	2,3,4		–	1,5,7,8
Reverse Current	I_R	1	–	–	–	2.0	–	2.0	μAdc	–	–	–	–	–	1	16	–	–	–	–	8
		2	–	–	–	↓	–	↓	↓	–	–	–	–	–	2	↓	–	–	–	–	1,8
		3	–	–	–		–			–	–	–	–	–	3		–	–	–	–	1,8
		4	–	–	–		–			–	–	–	–	–	4		–	–	–	–	8
		5	–	–	–		–			–	–	–	–	–	5		–	–	–	–	8
Forward Current	I_F	1	–	-1.20	–	-1.20	–	-1.20	mAdc	–	–	–	–	1	–	–	16	–	–	–	8
		2	–	-1.20	–	-1.20	–	-1.20		–	–	–	–	2	–	–	1,16	–	–	–	4,8
		3	–	-1.20	–	-1.20	–	-1.20		–	–	–	–	3	–	–	1,16	–	–	–	5,8
	$2I_F$	4	–	-2.4	–	-2.4	–	-2.4		–	–	–	–	4	–	–	16	–	–	–	1,2,3,5
		5	–	-2.4	–	-2.4	–	-2.4	↓	–	–	–	–	5	–	–	16	–	–	–	1,2,3,4
Power Drain Current (Both Flip-Flops)	I_{CCL}	16	–	–	–	35	–	–	mAdc	–	–	–	–	–	–	–	16	–	–	–	1,2,3,4,5,8,11
	I_{CCH}	16	–	–	–	30	–	–	mAdc	–	–	–	–	–	–	–	16	–	–	–	12,13,14,15

Pins not listed are left open.



TOGGLE MODE TEST CIRCUIT



$t_r \leq 20$ ns (10% to 90%)
$t_f \leq 20$ ns (90% to 10%).
DUTY CYCLE = 50%

V_{CC} and ground connections to the devices are not shown.
All unused inputs are at V_{CC}
Frequency at TP_{out} must be ½ frequency at TP_{in}.

SWITCHING CHARACTERISTICS

Characteristic	Symbol	-30°C	25°C		+75°C	Units
		Typ	Min	Typ	Typ	
Propagation Delay						
Delay from $\overline{S}$ to $\overline{Q}$	t_{pd-}	65	–	80	100	ns
Delay from $\overline{R}$ to $\overline{Q}$	t_{pd-}	65	–	80	100	ns
Delay from $\overline{S}$ to Q	t_{pd+}	250	–	300	400	ns
Delay from $\overline{R}$ to Q	t_{pd+}	250	–	300	400	ns
Delay from C to Q or $\overline{Q}$	t_{pd+}	300	–	350	450	ns
Delay from C to Q or $\overline{Q}$	t_{pd-}	85	–	100	130	ns
J or K Input	t_{setup}	55	–	60	70	ns
J or K Input	t_{hold}	26	–	24	0	ns
f_{Toggle}	f_{Tog}	–	1.0	2.5	–	MHz

OPERATING NOTES

1. If any input of the MC688 is not used, it should be returned through a 2 kΩ resistor to V_{CC}. This is particularly true of $\overline{SET}$ and $\overline{RESET}$ inputs, as these are most susceptible to noise. A single resistor may be used for up to 300 unused inputs.
2. The truth table shown for the MC688 is completely valid only when J & K inputs remain unchanged throughout the entire period when the clock input is high. This is a master-slave device, with the master receiving its instructions while the clock input is high. A study of the logic diagram will reveal that the J & K inputs can cause the master to reverse states once – and only once – while the clock is high. Thus, if – while the clock is high – the logic signals of the J & K inputs are such that the flip-flop should reverse states at the negative clock transition, it will reverse states on the negative clock transition regardless of any subsequent change of J or K.

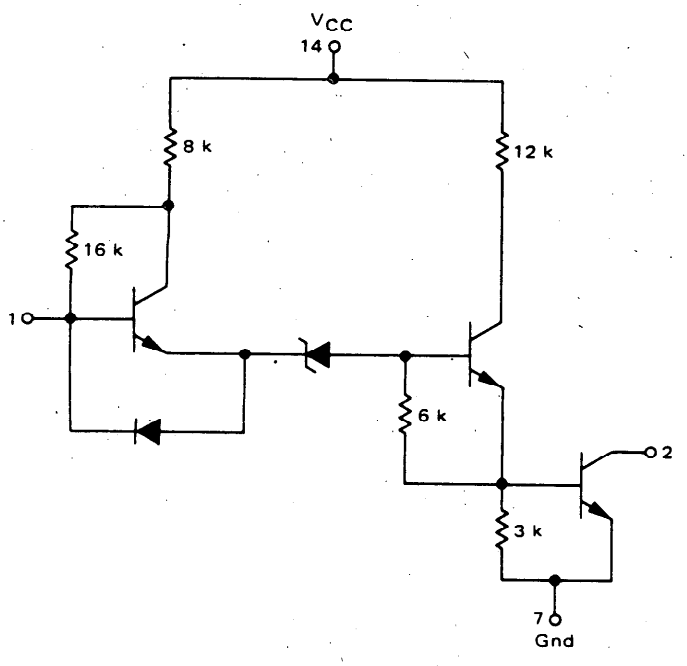
   The master-slave principle as used in this device leads to the aforementioned restriction which may not be desirable in some instances. However, it can be shown that an MHTL system is inherently more susceptible to negative-going noise than positive-going due to the difference in impedance levels. The design of the MC688 is such that negative-going noise appearing on the J or K inputs must last throughout the entire duration of the clock pulse to have any effect. The net result can well be a system with greater than expected noise immunity if care is used in other areas of the system.
3. The $\overline{SET}$ and $\overline{RESET}$ inputs control the output states when activated while the clock is low. A logic zero on these inputs has no immediate effect on the outputs if the clock input is high, but it can change the state of the master section. As an example, consider $\overline{SET}$ & $\overline{RESET}$ high, all other inputs and Q output low. If a clock pulse is received under these conditions, the output will not change. However, if $\overline{SET}$ is momentarily activated with a logic zero while clock is high, the flip-flop will reverse states on the trailing edge of the clock. This provides a means of synchronous data entry into the device without using J & K inputs. This feature is quite useful in certain types of shift registers and counters made with the MC688.
4. As with other saturated logic devices, input rise and fall times should be minimized for best operation. The most critical input in this respect is $\overline{CLOCK}$, which should have a transition time of less than 0.5 μ sec in either direction (measured from 6.5 to 8.5 volts). Failure to observe this restriction may result in triggering on positive clock transition or multiple triggering on negative clock transition.

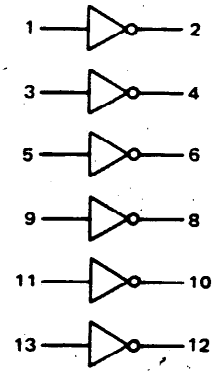
MC689

ISSUE A

The MC689 is a high threshold hex inverter with open collector outputs. It is designed to drive low current lamps, interface with discrete components, and to interface high level logic to any logic level from 4.0 volts to 20 volts. The input diode has been left off the circuit so it may be exapnded to any number of inputs.

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

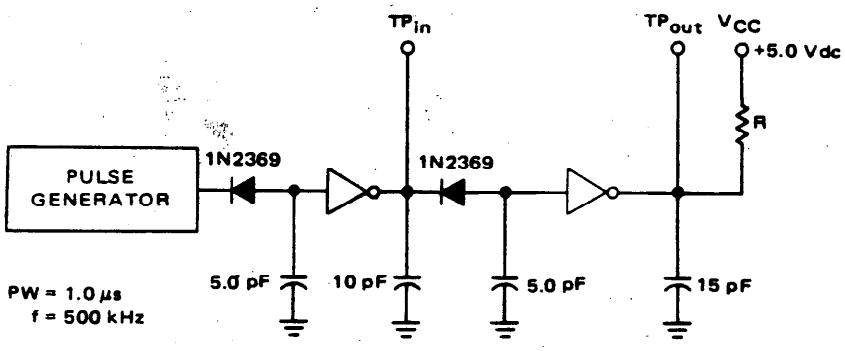


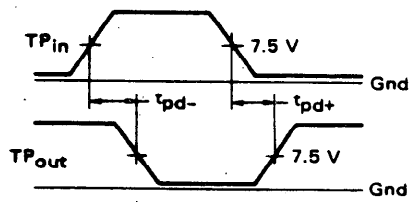


Positive Logic: $2 = \overline{1}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 150 ns typ
Typical Total Power Dissipation with V_{CC} @ 15 V
Inputs High = 173 mW
Inputs Low = 55 mW

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



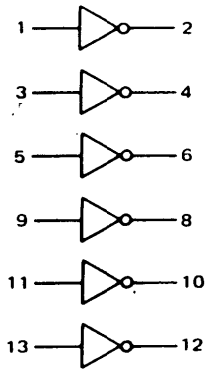


R = 510 ohms for t_{pd-} test.
= 3.6 k ohms for t_{pd+} test.

See General Information section for packaging

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



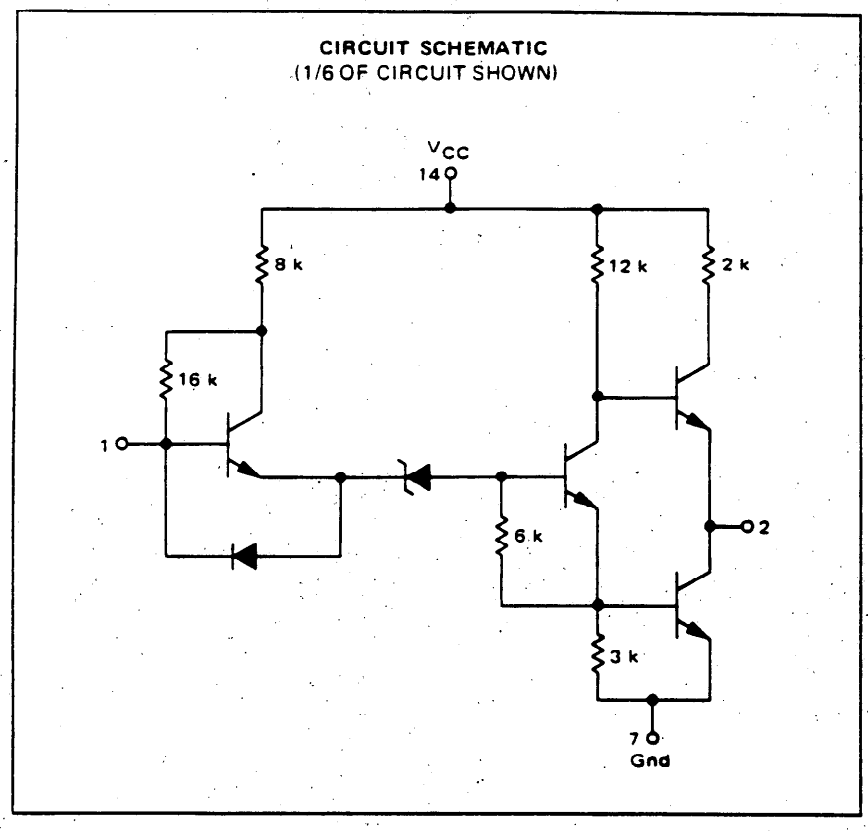
Characteristic	Symbol	Pin Under Test	MC689 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE (All Temperatures) mA I_{OL1}	mA I_{OL2}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_{CEX}	Volts V_{CC}	Volts V_{CCL}	Volts V_{CCH}	Gnd
										10.0	20.0	7.00	8.50	0.5	20.0	20.0	12.0	25.0	
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:									
										I_{OL1}	I_{OL2}	V_{IL}	V_{IH}	V_F	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
Output Voltage	V_{OL1}	2	–	0.5	–	0.5	–	0.5	Vdc	2	–	–	1	–	–	14	–	–	7
	V_{OL2}	2	–	1.0	–	1.0	–	1.0	Vdc	–	2	–	1	–	–	–	14	–	7
Output Leakage Current	I_{CEX}	2	–	75	–	75	–	75	μAdc	–	–	1	–	–	2	14	–	–	7
Forward Current	I_F	1	–	-1.20	–	-1.12	–	-1.12	mAdc	–	–	–	–	1	–	14	–	–	7
Power Drain Current	I_{CCL}	14	–		–	15.0	–	–	mAdc	–	–	–	–	–	–	–	–	14	1,3 5,7,9,11,13
(Total Device)	I_{CCH}	14	–		–	28	–	–	mAdc	–	–	–	–	–	–	14	–	–	7
Switching Times										Pulse In	Pulse Out								
	t_{1-2+}	2	–	–	–	300	–	–	ns	1	2	–	–	–	–	14	–	–	7
	t_{1+2-}	2	–	–	–	200	–	–	ns	1	2	–	–	–	–	14	–	–	7

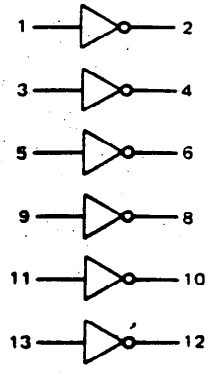
Pins not listed are left open

NOTE: All Tests must be performed with a 1N2369 input diode or equivalent.

MC690

The MC690 is a high threshold hex inverter and utilizes an active pull-up to minimize output impedance. This circuit is useful in high noise environment applications. The input diode has been left off the circuit so it may be expanded to any number of inputs.

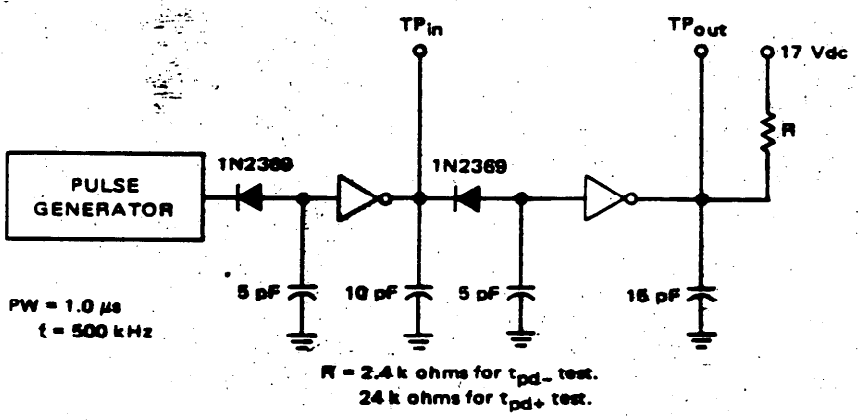


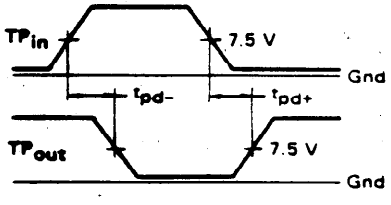


Positive Logic: 2 = $\overline{1}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 150 ns t
Typical Total Power Dissipation with
V_{CC} @ 15 V
Inputs High = 173 mW
Inputs Low = 55 mW

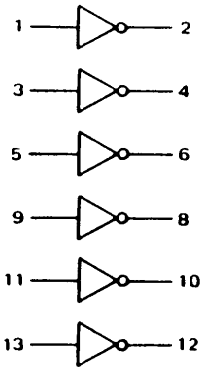
SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





E RICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



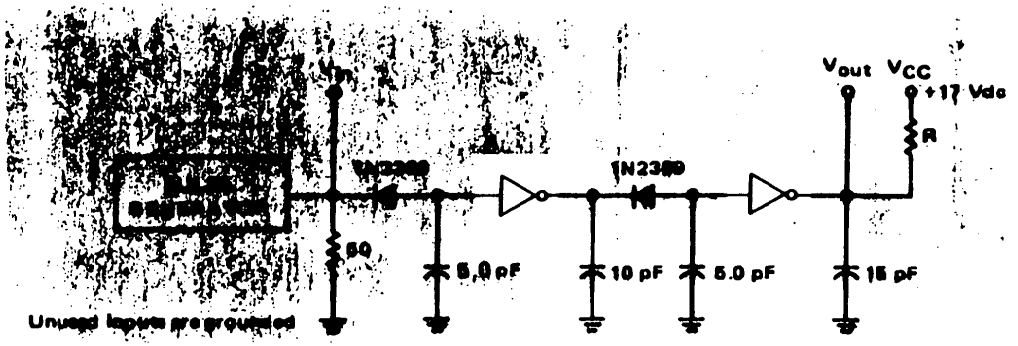
TEST CURRENT/VOLTAGE VALUES (All Temperatures)										
mA			Volts							
$I_{OL\,1}$	$I_{OL\,2}$	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	
10.0	20.0	0.10	7.00	8.50	0.50	16.0	20.0	12.0	25.0	

Characteristic	Symbol	Pin Under Test	MC690 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: $I_{OL\,1}$	$I_{OL\,2}$	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	$V_{OL\,1}$	2	–	0.5	–	0.5	–	0.5	Vdc	2	–	–	–	1	–	–	–	14	–	7
	$V_{OL\,2}$	2	–	1.0	–	1.0	–	1.0	Vdc	–	2	–	–	1	–	–	14	–	–	7
	$V_{OH\,1}$	2	–	–	10	–	–	–	Vdc	–	–	2	–	1	–	–	–	14	–	7
	$V_{OH\,2}$	2	–	–	18	–	–	–	Vdc	–	–	2	–	1	–	–	14	14	–	7
Short-Circuit Current	I_{SC}	2	–	-17.0	–	16.3	–	-15.6	mAdc	–	–	–	–	–	–	–	–	–	14	1,2,7
Forward Current	I_F	1	–	-1.20	–	-1.12	–	-1.12	mAdc	–	–	–	–	–	1	–	14	–	–	7
Power Drain Current	I_{CCL}	14	–	–	–	15.0	–	–	mAdc	–	–	–	–	–	–	–	–	–	14	1,3,5,7,9,11,13
(Total Device)	I_{CCH}	14	–	–	–	28	–	–	mAdc	–	–	–	–	–	–	–	14	–	–	7
Switching Times										Pulse In		Pulse Out								
	t_{1-2+}	2	–	–	–	400	–	–	ns	1		2	–	–	–	–	14	–	–	7
	t_{1+2-}	2	–	–	–	200	–	–	ns	1		2	–	–	–	–	14	–	–	7

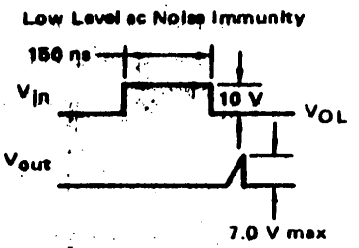
Pins not listed are left open

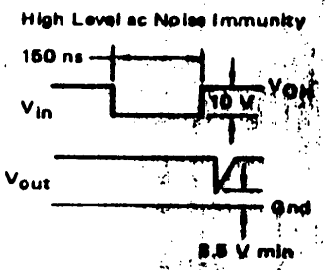
NOTE: All Tests must be performed with a 1N2369 input diode or equivalent.

AC NOISE IMMUNITY TEST CIRCUIT AND WAVEFORMS @ 25°C



R = 24 k ohms for high level test
2.4 k ohms for low level test

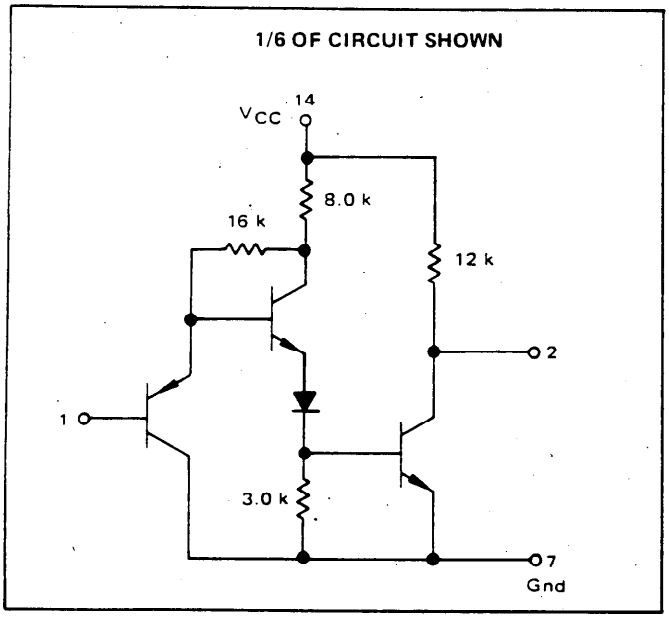


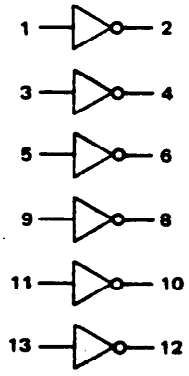


MC691

The MC691 is a monolithic hex inverter/interface element. It consists of six gates for interfacing between nominal 5 volt logic levels (McMOS, MTTL, MDTL) and high logic levels from 12 to 20 volts. The MC691 is ideal for driving MHTL and McMOS high level devices.

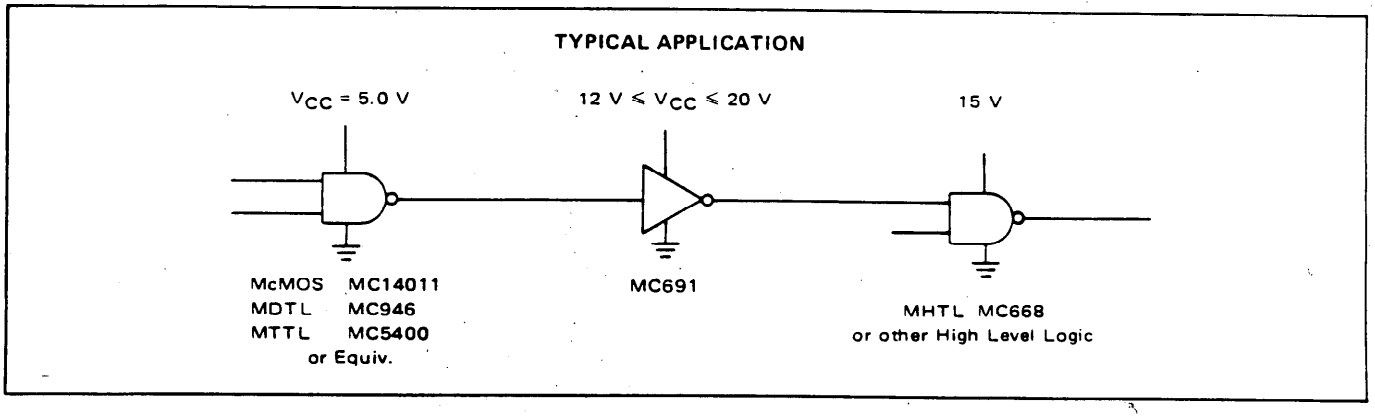
- 5 to 18 Volt CMOS Compatibility
- Wide V_{CC} Range (12 V – 20 V)
- High Fan Out (10 MHTL)
- Wired-OR Capability
- Good ac Noise Immunity
- Available in Dual-in-Line Ceramic or Plastic Package



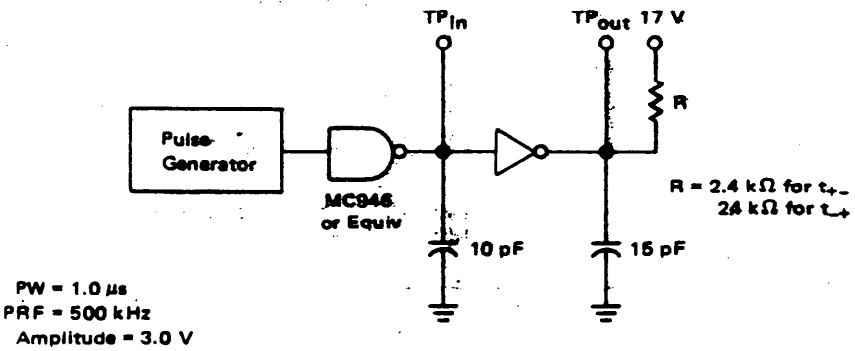


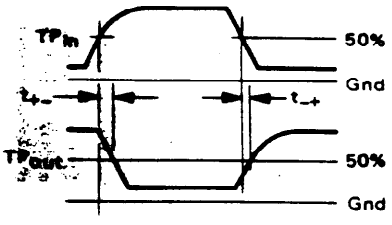
Positive Logic: $2 = \overline{1}$

Input Loading Factor = 0.4
Output Loading Factor = 10
Propagation Delay Time:
t_{+-} = 150 ns typ
t_{-+} = 300 ns typ
Typical Total Power Dissipation:
Inputs High = 500 mW typ/pkg
Input Low = 150 mW typ/pkg



SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



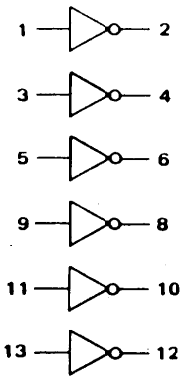


PW = 1.0 µs
PRF = 500 kHz
Amplitude = 3.0 V

See General Information section for packaging

ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.



	TEST CURRENT/VOLTAGE VALUES												
	mA			Volts									
	I_{OL1}	I_{OL2}	I_{OH}	V_{IL}	V_{IH}	V_{R1}	V_{R2}	V_{CEX}	V_F	V_{CC1}	V_{CC2}	V_{CCL}	V_{CCH}
+75°C	10.0	20.0	-0.1	0.8	1.9	4.0	20.0	20.0	0.5	20.0	16.0	12.0	
+25°C	10.0	20.0	-0.1	1.0	2.0	4.0	20.0	20.0	0.5	20.0	16.0	12.0	25.0
-30°C	10.0	20.0	-0.1	1.05	2.1	--	--	20.0	0.5	20.0	16.0	12.0	--

Characteristic	Symbol	Pin Under Test	MC691 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH}	V_{IL}	V_{IH}	V_{R1}	V_{R2}	V_{CEX}	V_F	V_{CC1}	V_{CC2}	V_{CCL}	V_{CCH}	Gnd
Output Voltage	V_{OL1}	2	--	0.5	--	0.5	--	0.5	Vdc	2	--	--	--	1	--	--	--	--	--	--	14	--	7
	V_{OL2}	2	--	1.0	--	1.0	--	1.0	Vdc	--	2	--	--	1	--	--	--	--	14	--	--	--	7
	V_{OH1}	2	10.0	--	10.0	--	10.0	--	Vdc	--	--	2	1	--	--	--	--	--	--	--	14	--	7
	V_{OH2}	2	18.0	--	18.0	--	18.0	--	Vdc	--	--	2	1	--	--	--	--	--	14	--	--	--	7
Short-Circuit Current	I_{SC}	2	--	-2.4	--	-2.3	--	-2.3	mAdc	--	--	--	--	--	--	--	--	--	14	--	--	--	1,2,7
Reverse Current	I_{R1}	1	--	--	--	2.0	--	2.0	µAdc	--	--	--	--	--	1	--	--	--	--	--	14	--	7
	I_{R2}	1	--	--	--	10.0	--	10.0	µAdc	--	--	--	--	--	--	1	--	--	--	--	14	--	7
Output Leakage Current	I_{CEX}	2	--	75	--	75	--	75	µAdc	--	--	--	--	--	--	--	2	--	14	--	--	--	1,7
Forward Current	I_F	1	--	-0.5	--	-0.4	--	-0.4	mAdc	--	--	--	--	--	--	--	--	1	--	14	--	--	7
Power Drain Current (Total Device)	I_{CCL}	14	--	9.5	--	9.0	--	9.0	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	14	1,3,5,7, 9,11,13
	I_{CCH}	14	--	34.0	--	31.0	--	31.0	mAdc	--	--	--	--	--	--	--	--	--	14	--	--	--	7
Switching Parameters										Pulse In		Pulse Out											
Turn-On Delay	t_{1+2-}	2	--	--	--	250	--	--	ns	1		2	--	--	--	--	--	--	14	--	--	--	7
Turn-Off Delay	t_{1-2+}	2	--	--	--	500	--	--	ns	1		2	--	--	--	--	--	--	14	--	--	--	7

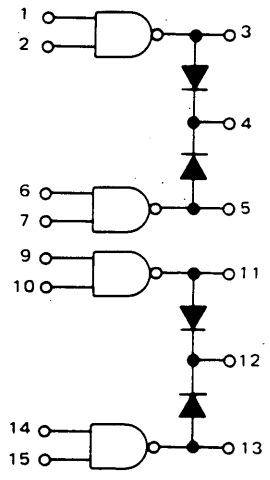
MC693

ISSUE A

The MC693 is a quad, two input NAND gate designed primarily as an output interface/buffer for lamp driving or switching inductive loads. The open collector outputs have built-in clamp diodes for over-voltage suppression.

- Power Supply Voltage 5 Volt $\leq V_{CC} \leq$ 20 Volts
- Input Compatibility with Many Popular Families Including McMOS, MTTL, MDTL and MHTL
- $I_{out\ max}$ = 300 mAdc per Gate
- $V_{OL} \leq$ 1.4 Volts @ I_{OL} = 250 mAdc
- Schmitt Trigger Inputs with the Thresholds Set Internally at V_{IL} = 1/5 V_{CC}, V_{IH} = 3/5 V_{CC}
- Maximum Operating Output Voltage = 30 Volts
- Output Clamp Diodes: $V_F \leq$ 1.5 Volts @ 250 mAdc
- The Plastic Package Has a Built-in Heat Spreader for Greater Maximum Power Dissipation
- Superb Noise Immunity
- Small Variations in Threshold Due to Temperature
- Devices Are Available for Full Temperature (−55° C to +125° C) Operation by Ordering MC693tL

LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

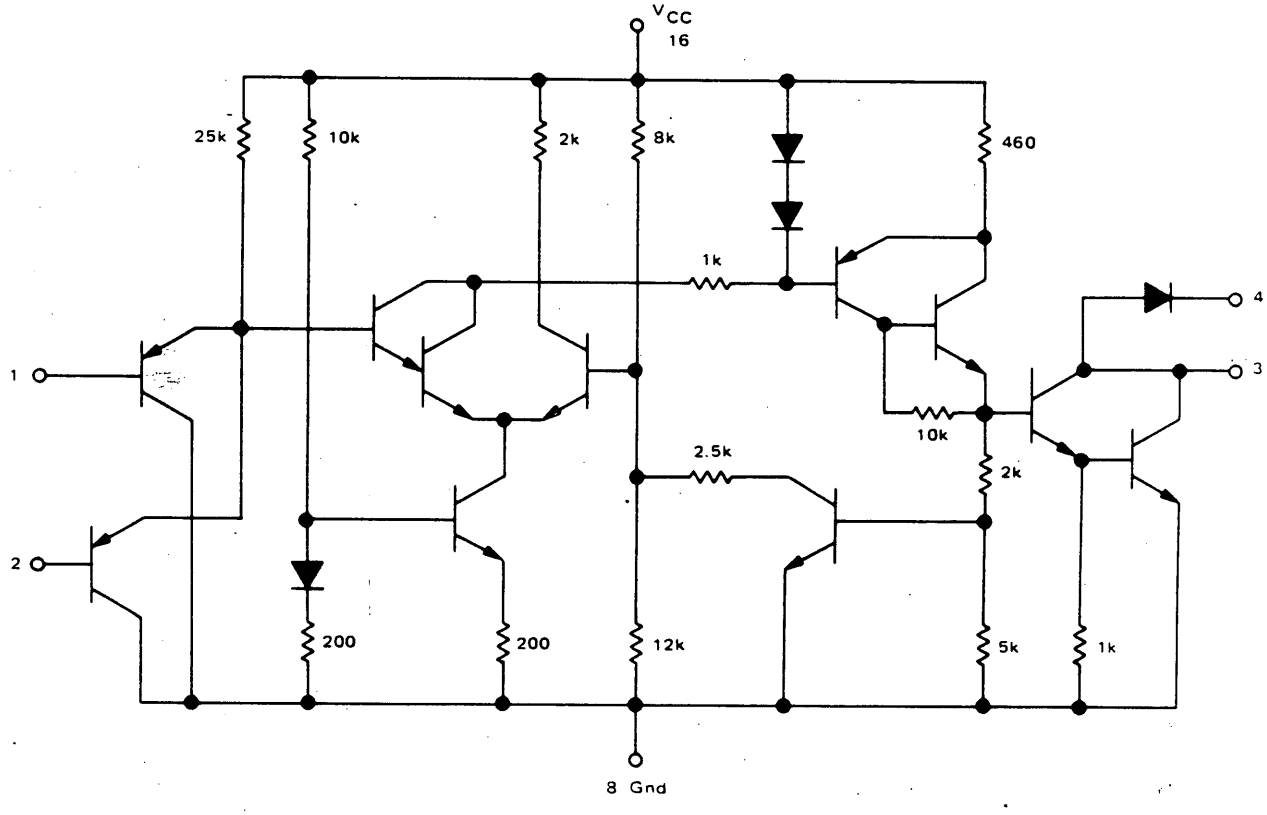
Positive Logic 3 = $\overline{1 \bullet 2}$

Input Loading Factor = 0.415

Propagation Delay Time = 400 ns typ
Typical Total Power Dissipation = 300 mW typ/pkg

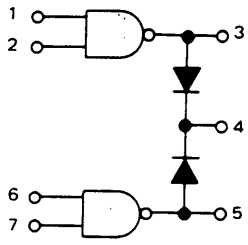
All @ V_{CC} = 15 Volts

CIRCUIT SCHEMATIC
1/4 OF CIRCUIT SHOWN



See General Information section for packaging

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

procedures are shown for only one The other gates are tested in the same manner.

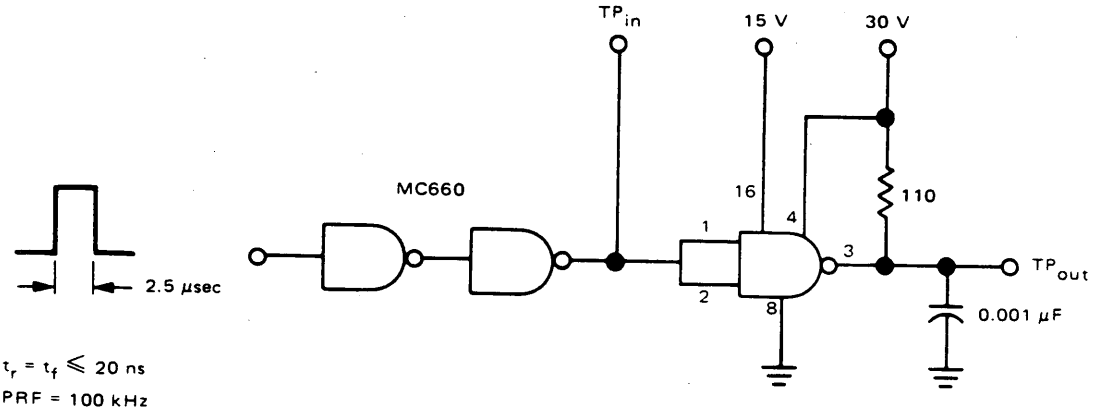
Pin 8 is grounded for all tests. All Pins are open unless indicated otherwise.

Characteristic	Symbol	Pin Under Test	V_{CC} Vdc	−30° C Min	−30° C Max	+25° C Min	+25° C Max	+75° C Min	+75° C Max	Unit
Input Reverse Current	I_R									μA
(Pin 1 = 15 V, Pin 2 = Gnd)		1	15	–	2.0	–	2.0	–	2.0	
(Pin 2 = 15 V, Pin 1 = Gnd)		2	15	–	2.0	–	2.0	–	2.0	
(Pin 1 = 20 V, Pin 2 = Gnd)		1	20	–	5.0	–	5.0	–	5.0	
(Pin 2 = 20 V, Pin 1 = Gnd)		2	20	–	5.0	–	5.0	–	5.0	
Forward Current	I_F									mA
(Pin 1 = 0.4 V)		1	5.0	–	−0.25	–	−0.2	–	−0.2	
(Pin 2 = 0.4 V)		2	5.0	–	−0.25	–	−0.2	–	−0.2	
(Pin 1 = 0.4 V)		1	10	–	−0.45	–	−0.4	–	−0.35	
(Pin 2 = 0.4 V)		2	10	–	−0.45	–	−0.4	–	−0.35	
(Pin 1 = 1.5 V)		1	15	–	−0.55	–	−0.5	–	−0.45	
(Pin 2 = 1.5 V)		2	15	–	−0.55	–	−0.5	–	−0.45	
Supply Current, Inputs High	I_{CCH}									mA
		16	5.0	–	15	–	12	–	10	
		16	10	–	23	–	18	–	16	
		16	15	–	31	–	26	–	23	
Supply Current, Inputs Low	I_{CCL}									mA
		16	5.0	–	7.0	–	6.0	–	6.0	
		16	10	–	14	–	12	–	11	
		16	15	–	21	–	18	–	17	
Output Breakdown Voltage	V_{BD}									V
(Pins 1, 2 = Gnd, I_{BD} (Pin 3) = 100 μA)		3	5.0	30	–	30	–	30	–	
(Pins 1, 2, 3 = Gnd, I_{BD} (Pin 4) = 100 μA)		4	5.0	30	–	30	–	30	–	
Output Voltage in Low State, (I_{OL} = 250 mA)	V_{OL}									V
(Pins 1, 2 = 3.5 V)		3	5.0	–	1.5	–	1.4	–	1.3	
(Pins 1, 2 = 7.0 V)		3	10	–	1.5	–	1.4	–	1.3	
(Pins 1, 2 = 10.5 V)		3	15	–	1.5	–	1.4	–	1.3	
Clamp Diode Forward Voltage	D_{FV}									V
(Pin 4 = Gnd, I_{FD} = 250 mA)		3	–	–	1.6	–	1.5	–	1.5	
Switching Times						Typ	Max			ns
	t_{1-3+}	3	15	–	–	400	800	–	–	
	t_{1+3-}	3	15	–	–	250	500	–	–	

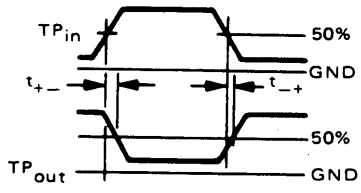
INPUT THRESHOLD VOLTAGES (All Temperatures)

Threshold	Symbol	V_{CC} Vdc	Value (Vdc) Min	Typ	Max
High-Level Threshold	V_{IH}	5.0	–	3.0	3.5
		10	–	6.0	6.5
		15	–	9.0	9.5
		20	–	12.0	12.5
Low-Level Threshold	V_{IL}	5.0	0.75	1.0	–
		10	1.5	2.0	–
		15	2.5	3.0	–
		20	3.5	4.0	–

SWITCHING TIME TEST CIRCUIT and WAVEFORMS



$t_r = t_f \leqslant 20$ ns
PRF = 100 kHz
Duty Cycle = 25%



ABSOLUTE MAXIMUM RATINGS (T_A = 25° C)

Rating	Symbol	Value	Unit
Power Supply Voltage — Continuous Pulsed, 1.0 s	V_{CC}	20 22	Vdc
Output Collector — Voltage (Off Condition)	V_{CE}	30	Vdc
Output Current — Continuous Pulsed, 1 ms	I_{OL}	300 600	mAdc
Maximum Operating Frequency	f	300	kHz
Input Voltage Maximum Minimum	V_{in}	 +20 −1.0	Vdc
Power Dissipation and Thermal Characteristics Dual-In-Line Ceramic Package Maximum Junction Temperature Maximum Internal Dissipation @ T_A = 25°C *Thermal Resistance, Junction to Air *Thermal Resistance, Junction to Case Dual-In-Line Plastic Package Maximum Junction Temperature Maximum Internal Dissipation @ T_A = 25° C *Thermal Resistance, Junction to Air *Thermal Resistance, Junction to Case	 T_J P_D $R_{\theta JA}$ $R_{\theta JC}$ T_J P_D $R_{\theta JA}$ $R_{\theta JC}$	 175 1000 0.15 0.09 150 1.8 0.07 0.15	 °C mW °C/mW °C/mW °C W °C/mW °C/mW
†Operating Temperature Range L, P Suffix tL Suffix	T_A	−30 to +75 −55 to +125	°C
Storage Temperature Range (All)	T_{stg}	−55 to +125	°C

*Note: Thermal Resistance values are specified with the device mounted in a socket in still air.

†Note: Consideration must be given to electrical conditions in conjunction with the power dissipation derating curves of Figure 6.

TYPICAL CHARACTERISTICS

FIGURE 1 – INPUT FORWARD CURRENT versus POWER SUPPLY VOLTAGE

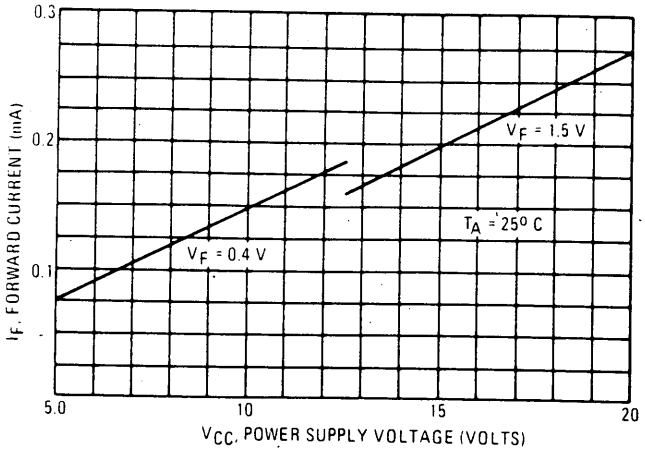


FIGURE 2 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

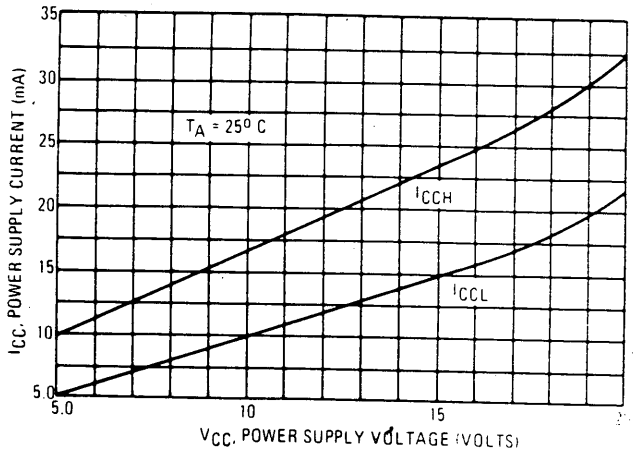


FIGURE 3 – COLLECTOR CURRENT versus OUTPUT VOLTAGE

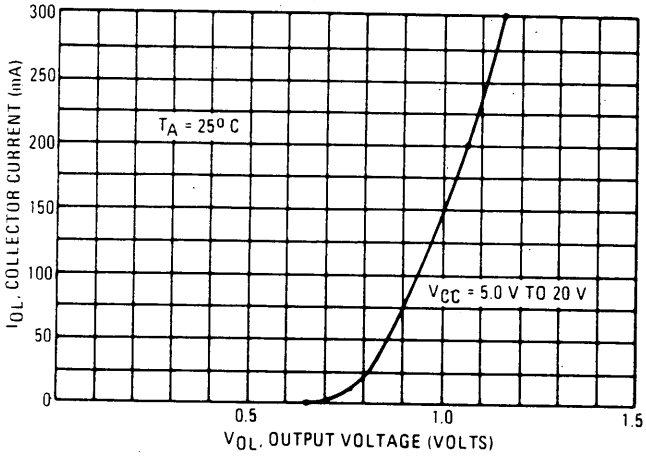


FIGURE 4 – PROPOGATION DELAY TIME versus POWER SUPPLY VOLTAGE

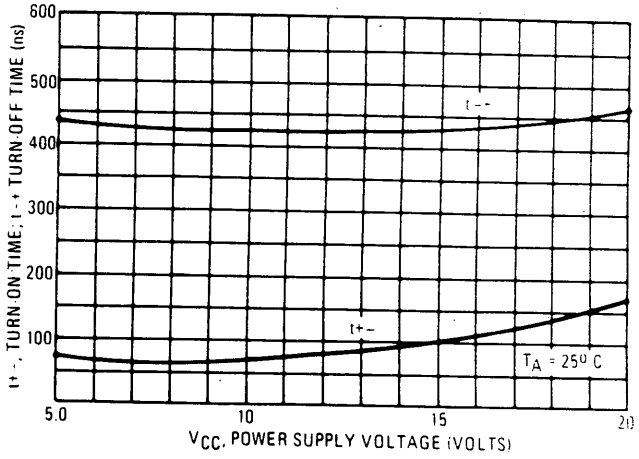


FIGURE 5 – THRESHOLD VOLTAGES AND HYSTERSIS WIDTH versus POWER SUPPLY VOLTAGE

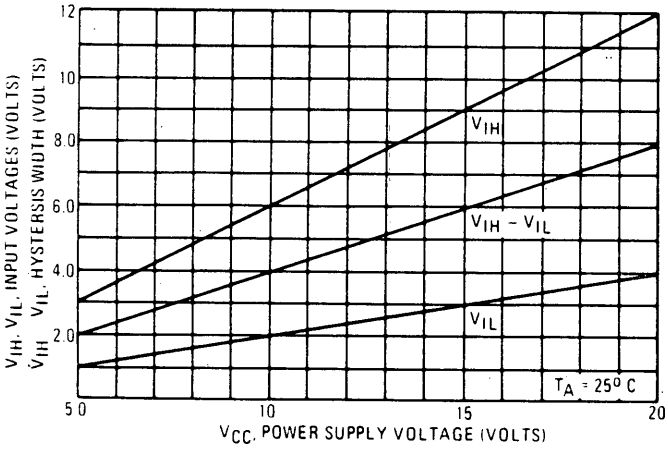


FIGURE 6 – FREE AIR TEMPERATURE DISSIPATION DERATING

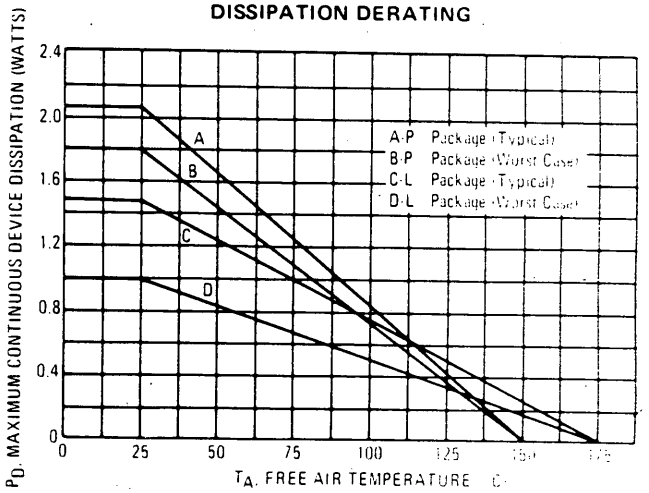
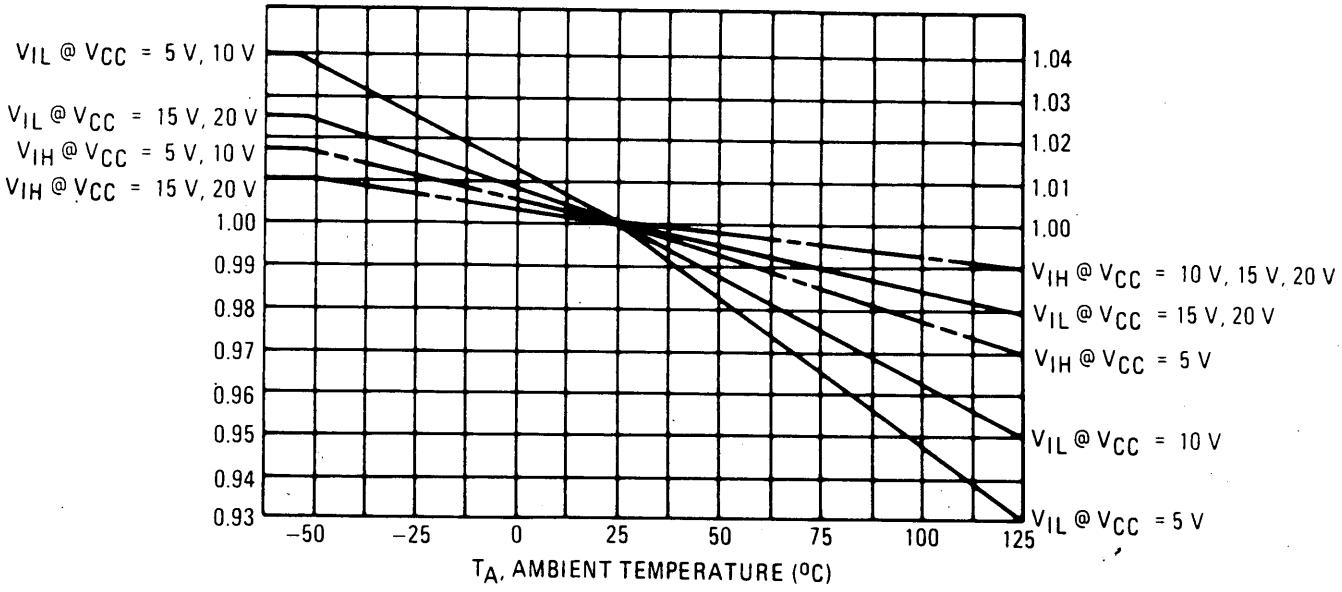


FIGURE 7 – TYPICAL VARIATION IN THRESHOLD VOLTAGE versus TEMPERATURE, NORMALIZED TO 25°C

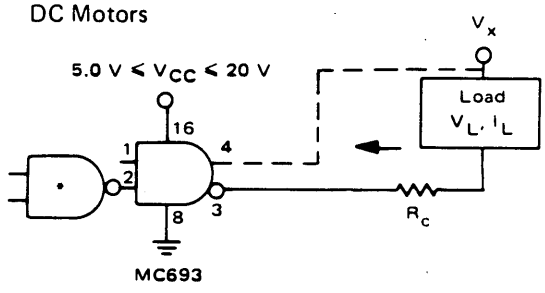


APPLICATION INFORMATION

The MC693 is designed primarily for use as an output interface with its high current, open collector outputs. An internal clamp diode is available for suppressing over voltages due to inductive loads.

Sink Configuration

Common loads are: Lamps
Relays
Common Cathode LEDs
PNP Power Transistors
DC Motors



MC693

$V_X \leq 30$ V
$I_L \leq 250$ mA
$V_L \leq 28.5$ V
R_c is a current limiting resistor to be used when required. Its value is determined by:

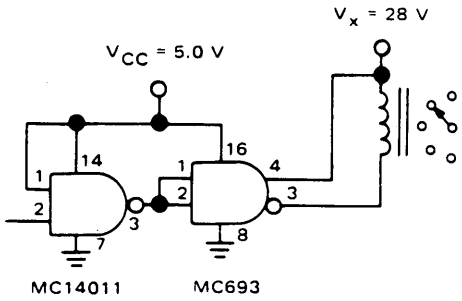
$$R_c = \frac{V_X - V_L - V_O}{I_L}$$

where V_O may be the maximum value of 1.4 V or may be a typical voltage selected from Figure 3.

*McMOS	MC14011
MTTL	MC7400
MDTL	MC846
MHTL	MC668

or Equiv.

Example: Stepper Switch/Stepper Motor Driver

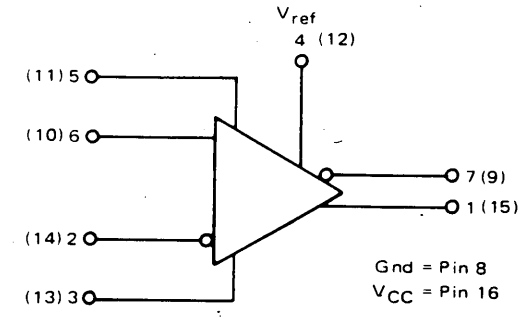


MC14011 MC693

MC696

ISSUE B

BLOCK DIAGRAM
(1/2 Device Shown)

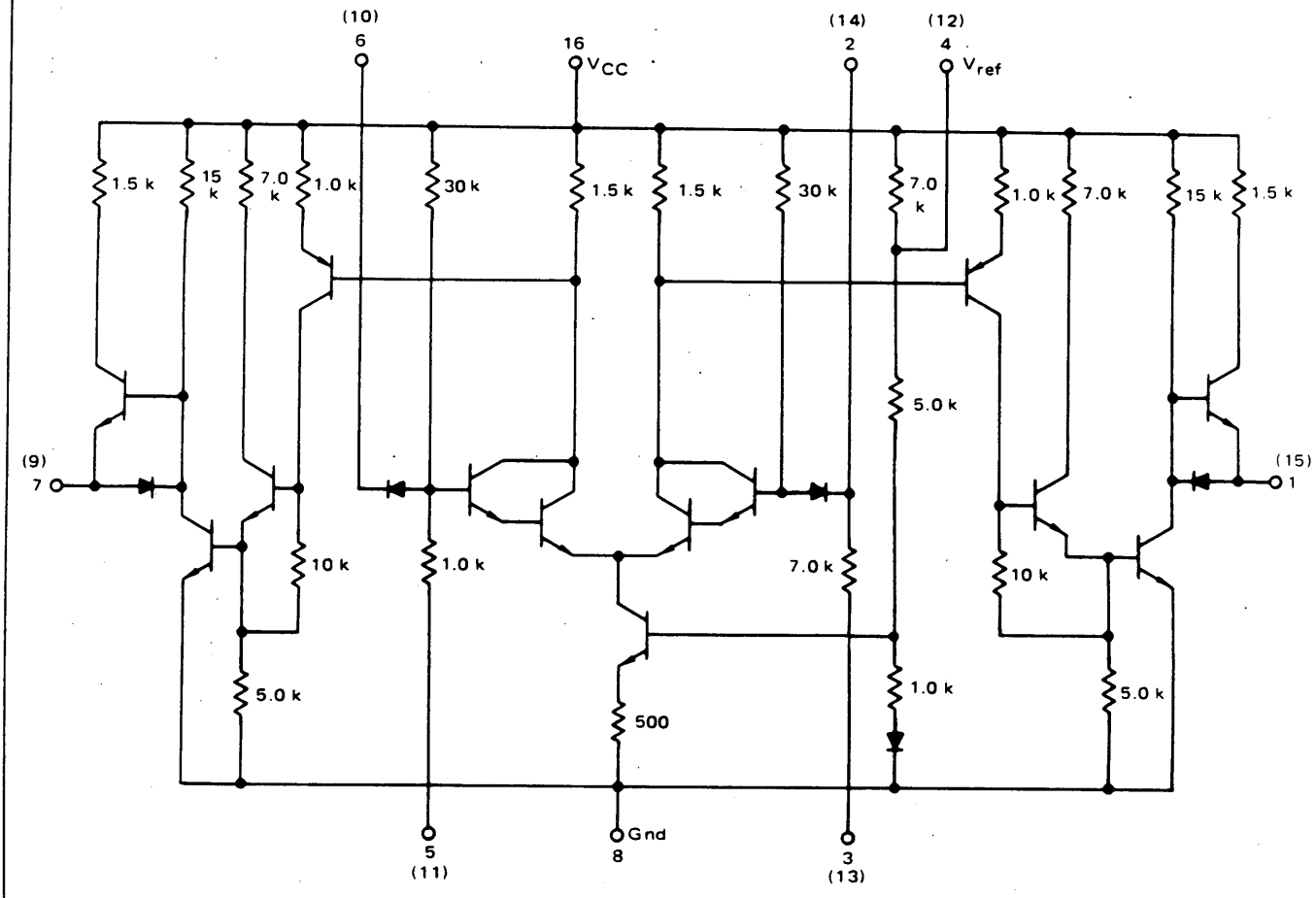


Numbers in parenthesis denotes pin numbers for other half of device

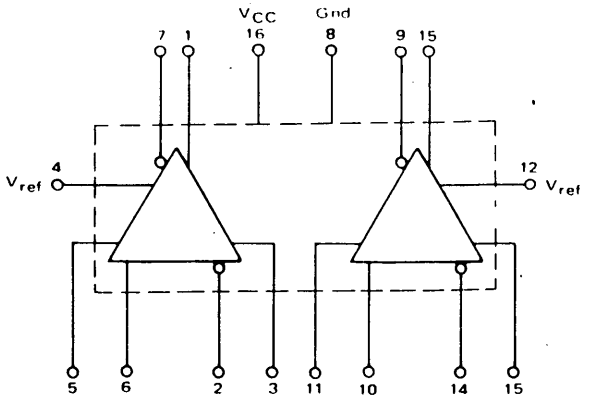
The MC696 dual Line Driver/Receiver/Repeater is designed for industrial logic applications requiring high immunity to electrical noise. Because of its high input impedance (≈ 20 k Ω), the MC696 is suitable for interfacing between logic families (MECL to MTTL, McMOS to MTTL). Other attributes of the MC696 include:

- Low output impedance (≈ 20 Ω in LOW state).
- Differential inputs and outputs.
- Internal bias, reference, and hysteresis sources.
- Useful for single-wire input/output applications
- McMOS compatibility
- Capability for operation over a wide range of power supply voltage (10 V ≤ V_{CC} ≤ 25 V)

1/2 of CIRCUIT SHOWN



See General Information Section for packaging.



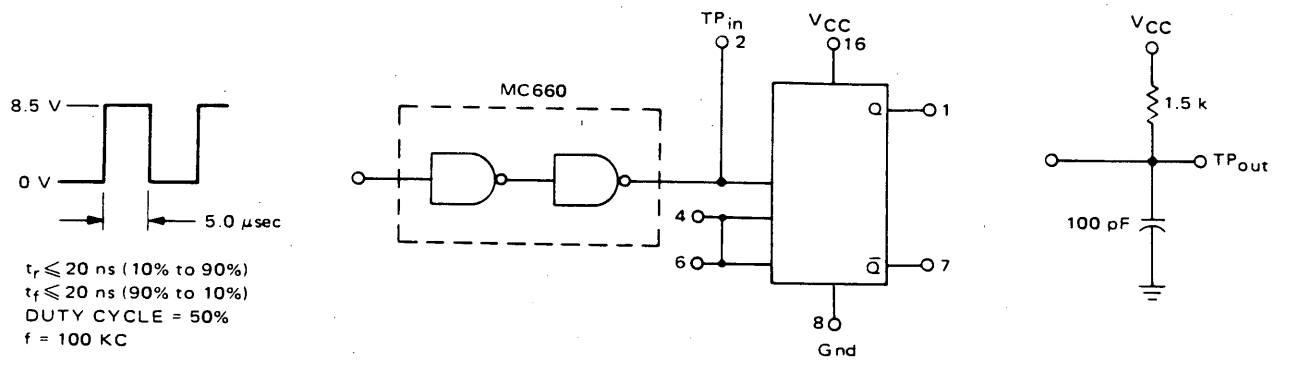
ELECTRICAL CHARACTERISTICS

Test procedures are shown for one half of the device. The other half of the device is tested in the same manner

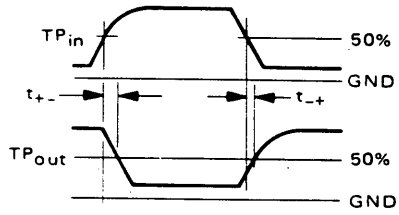
			MC696 Test Limits							TEST CURRENT/VOLTAGE VALUES (All Temperatures)																					
			-30°C		+25°C		+75°C			mAdc				µAdc		VOLTS															
										I_{OL1}	I_{OL2}	I_{OL3}	I_{OH2}	I_{OH}	I_{ref}	V_{IL}	V_{IL1}	V_{IL2}	V_{IL3}	V_{IH}	V_{IH1}	V_{IH2}	V_{IH3}	V_{CEX}	V_{CC}	V_{CC1}	V_{CC2}	V_{CCL}	V_{CCH}		
										12.0	15.0	20.0	-1.0	-30	0.0	1.5	4.0	6.5	10.5	25.0	6.0	8.5	14.5	25.0	15.0	14.0	16.0	10.0	25.0		
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:																					
Characteristic	Symbol	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	I_{OL1}	I_{OL2}	I_{OL3}	I_{OH2}	I_{OH}	I_{ref}	V_{IL}	V_{IL1}	V_{IL2}	V_{IL3}	V_{IH}	V_{IH1}	V_{IH2}	V_{IH3}	V_{CEX}	V_{CC}	V_{CC1}	V_{CC2}	V_{CCL}	V_{CCH}	See Note	Gnd
Output Voltage	V_{OH1}	1	8.5	--	8.5	--	8.5	--	Vdc	--	--	--	--	1	--	--	2	--	--	--	--	--	--	--	--	--	--	16	--	4,6	8
		7	8.5	--	8.5	--	8.5	--	Vdc	--	--	--	--	7	--	--	6	--	--	--	--	--	--	--	--	--	--	16	--	2,4	8
	V_{OH2}	1	12.5	--	12.5	--	12.5	--	Vdc	--	--	--	--	1	--	--	--	2	--	--	--	--	--	--	--	16	--	--	--	4,6	8
		7	12.5	--	12.5	--	12.5	--	Vdc	--	--	--	--	7	--	--	--	6	--	--	--	--	--	--	--	16	--	--	--	2,4	8
	V_{OH3}	1	23.0	--	23.0	--	23.0	--	Vdc	--	--	--	--	1	--	--	--	--	2	--	--	--	--	--	--	--	--	--	16	4,6	8
		7	23.0	--	23.0	--	23.0	--	Vdc	--	--	--	--	7	--	--	--	--	6	--	--	--	--	--	--	--	--	--	16	2,4	8
	V_{OH4}	1	22.0	--	22.0	--	22.0	--	Vdc	--	--	--	1	--	--	--	--	--	2	--	--	--	--	--	--	--	--	--	16	4,6	8
		7	22.0	--	22.0	--	22.0	--	Vdc	--	--	--	7	--	--	--	--	--	6	--	--	--	--	--	--	--	--	--	16	2,4	8
	V_{OL1}	1	--	1.5	--	1.5	--	1.5	Vdc	1	--	--	--	--	--	--	--	--	--	--	2	--	--	--	--	--	--	16	--	4,6	8
		7	--	1.5	--	1.5	--	1.5	Vdc	7	--	--	--	--	--	--	--	--	--	--	6	--	--	--	--	--	--	16	--	2,4	8
	V_{OL2}	1	--	1.5	--	1.5	--	1.5	Vdc	--	1	--	--	--	--	--	--	--	--	--	--	2	--	--	16	--	--	--	--	4,6	8
		7	--	1.5	--	1.5	--	1.5	Vdc	--	7	--	--	--	--	--	--	--	--	--	--	6	--	--	16	--	--	--	--	2,4	8
	V_{OL3}	1	--	1.5	--	1.5	--	1.5	Vdc	--	--	1	--	--	--	--	--	--	--	--	--	--	2	--	--	--	--	--	16	4,6	8
		7	--	1.5	--	1.5	--	1.5	Vdc	--	--	7	--	--	--	--	--	--	--	--	--	--	6	--	--	--	--	--	16	2,4	8
Reference Voltage	V_{ref1}	4	4.0	6.0	4.0	6.0	4.0	6.0	Vdc	--	--	--	--	--	4	--	--	--	--	--	--	--	--	--	--	--	--	16	--	2,4	8
	V_{ref2}	4	6.5	8.5	6.5	8.5	6.5	8.5	Vdc	--	--	--	--	--	4	--	--	--	--	--	--	--	--	--	16	--	--	--	--	2,4	8
	V_{ref3}	4	11.0	14.0	11.0	14.0	11.0	14.0	Vdc	--	--	--	--	--	4	--	--	--	--	--	--	--	--	--	--	--	--	--	16	2,4	8
Forward Current	I_{IH}	2	--	10.0	--	10.0	--	15.0	µAdc	--	--	--	--	--	--	--	--	--	--	2	--	--	--	--	--	--	--	--	16	--	8
		6	--	10.0	--	10.0	--	15.0	µAdc	--	--	--	--	--	--	--	--	--	--	6	--	--	--	--	--	--	--	--	16	--	8
	I_{IL1}	2	--	-0.45	--	-0.40	--	-0.40	mAdc	--	--	--	--	--	--	--	2	--	--	--	--	--	--	--	--	--	--	16	--	4,6	8
		6	--	-0.45	--	-0.40	--	-0.40	mAdc	--	--	--	--	--	--	--	6	--	--	--	--	--	--	--	--	--	--	16	--	2,4	8
	I_{IL2}	2	--	--	--	-1.0	--	--	mAdc	--	--	--	--	--	--	2	--	--	--	--	--	--	--	--	--	--	--	--	16	4,6	8
		6	--	--	--	-1.0	--	--	mAdc	--	--	--	--	--	--	6	--	--	--	--	--	--	--	--	--	--	--	--	16	2,4	8
Output Leakage Current	I_{CEX}	1	--	100	--	100	--	100	µAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	1	--	--	--	--	16	4,6	2,8
		7	--	100	--	100	--	100	µAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	7	--	--	--	--	16	2,4	6,8
Short-Circuit Current	I_{SC1}	1	-3.9	-10.0	-3.9	-10.0	-3.9	-10.0	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	4,6	1,2,8
		7	-3.9	-10.0	-3.9	-10.0	-3.9	-10.0	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	2,4	6,7,8
	I_{SC2}	1	-6.5	-16.0	-6.5	-16.0	-6.5	-16.0	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	--	4,6	1,2,8
		7	-6.5	-16.0	-6.5	-16.0	-6.5	-16.0	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	--	2,4	6,7,8
	I_{SC3}	1	-12.5	-25.0	-12.5	-25.0	-12.5	-25.0	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	4,6	1,2,8
		7	-12.5	-25.0	-12.5	-25.0	-12.5	-25.0	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	2,4	6,7,8
Power Drain Current	I_{CCL1}	16	--	--	--	12	--	--	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	--	--	2,6,8,10,14
	I_{CCL2}	16	--	--	--	15	--	--	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	16	--	2,6,8,10,14
Total Device	I_{CCH1}	16	--	--	--	25	--	--	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	--	2,4,12,14	8
	I_{CCH2}	16	--	--	--	30	--	--	mAdc	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	16	2,4,12,14	8
										Pulse In	Pulse Out																				
Switching Time	t_{2+1-}	1				500		--	ns	2	1	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	--	--	--	4,6	8
	t_{2-1+}	1				1.0		--	µs	2	1	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	--	--	--	4,6	8
	t_{6+7-}	7				500		--	ns	6	7	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	--	--	--	2,4	8
	t_{6-7+}	7				1.0		--	µs	6	7	--	--	--	--	--	--	--	--	--	--	--	--	--	16	--	--	--	--	2,4	8

*Note: Pin numbers listed should be tied together before performing test.

SWITCHING TIME TEST CIRCUIT and WAVEFORMS



Note: Circuit schematic is shown for 1/2 of device only.



Notes to parameters and limits:

1) Common mode rejection ratio: Typical rejection ratio for the MC696 in the common mode (see application note) is 75 dB.
2) Common mode range: Typical common mode range for the MC696 is from 1.5 volts to 1.5 volts less than the V_{CC} voltage.

APPLICATION INFORMATION

HYSTERESIS MODES OF THE MC696

The MC696 has very flexible hysteresis capability, enabling the designer to adjust the switching thresholds (and thus the noise immunity) of the device to suit his needs. The hysteresis thresholds (V_{IL}, V_{IH}) and widths (V_{HW}) for various feedback resistor values of the test circuit shown in Figure 1 are plotted in Figure 2. The power supply is set at 15 V, so that with the inverting input tied to the internal reference voltage of the circuit (approximately 1/2 V_{CC}), the high-level and low-level switching points of the device are centered about the 7.0 volt level.

Note that both switching points change symetrically about that reference level until the feedback resistor is decreased below 5.0 k ohm, giving a very wide range of widths. The variation of hysteresis width with changes in the power supply voltage is quite linear over the operating range as shown in Figure 3; the internal 7.0 k resistor is used in that test for the hysteresis feedback.

FIGURE 1 – HYSTERESIS CIRCUIT

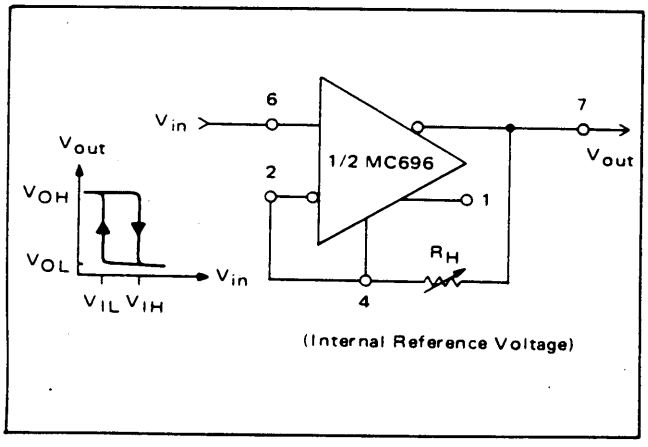


FIGURE 2 – TYPICAL HYSTERESIS VOLTAGE (V_{IL}, V_{IH}) versus FEEDBACK RESISTANCE (R_H).

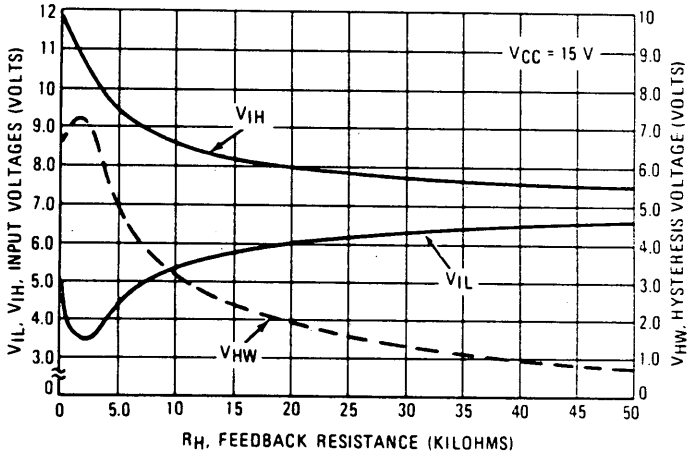
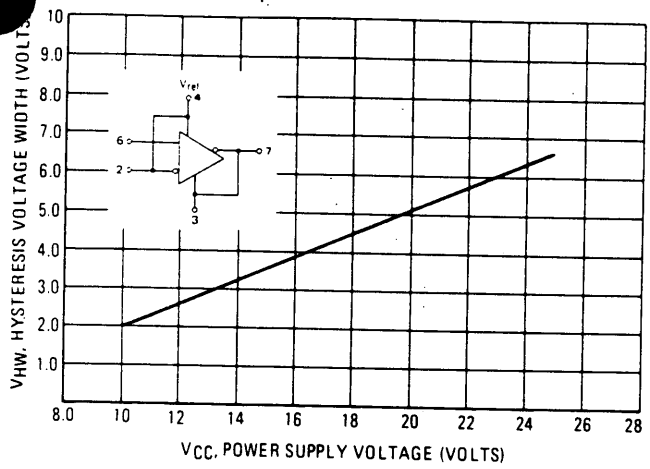
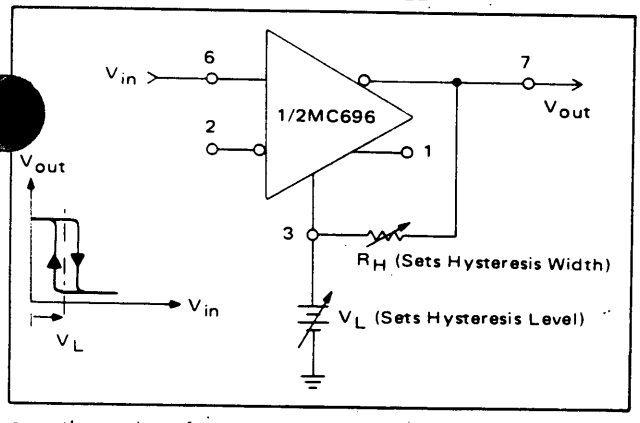


FIGURE 3 – HYSTERESIS WIDTH versus POWER SUPPLY VOLTAGE (Using Internal 7.0 kΩ Resistor)



The hysteresis center-point level can be changed by varying the reference voltage level as shown in Figure 4, giving complete control

FIGURE 4 – HYSTERESIS CIRCUIT WITH VARIABLE HYSTERESIS LEVEL



over the setting of the hysteresis levels. The only limitation is that the levels must remain within the common-mode range (CMR) of the device (1.5 V above ground to 1.5 V less than V_{CC}). If a reference voltage level is not available or is inconvenient, the hysteresis may be varied in width and centered by using two external resistors as shown in Figure 5. Figures 6, 7, 8 are plots giving

FIGURE 5 – HYSTERESIS CIRCUIT – CENTERING V_{HW} WITHOUT EXTERNAL REFERENCE VOLTAGE V_L

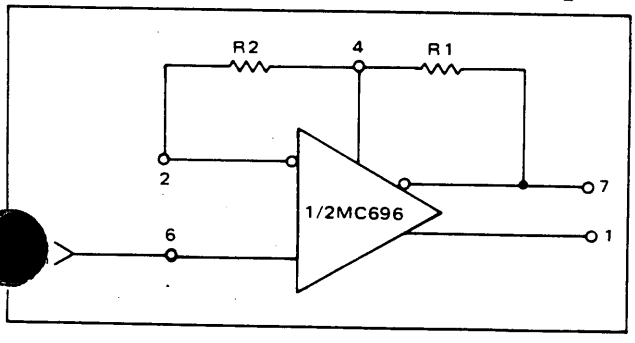


FIGURE 6 – FEEDBACK RESISTANCE versus HYSTERESIS WIDTHS

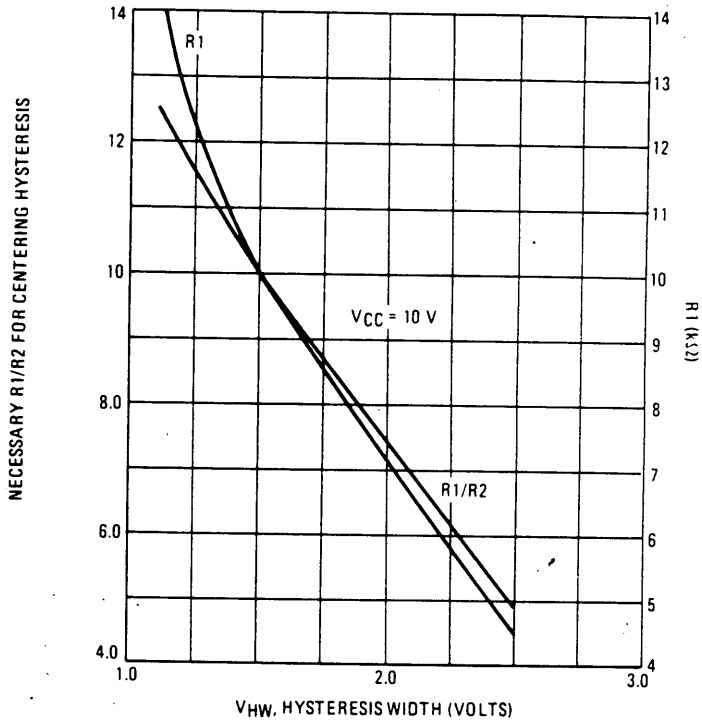
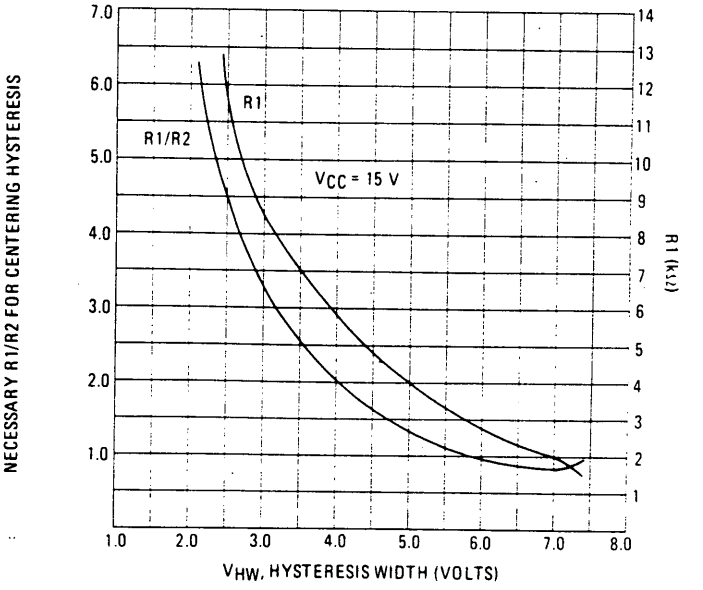


FIGURE 7 – FEEDBACK RESISTANCES versus HYSTERESIS WIDTHS



typical values for R1, R1/R2, and width V_{HW} versus V_{CC} of 10 V, 15 V, and 25 V when the hysteresis is approximately centered. If exact centering of the hysteresis is desired best results are generally obtained by empirically choosing values of R1 and R2 for the V_{CC} voltage used.

MCC696 Slow-Down Receiver

The MC696 can be used as a single-ended slow-down receiver as shown in Figure 9. By connecting a capacitor to the internal 1.0 k resistor, the device can be made insensitive to pulses with widths shorter than a predetermined value. The graph in Figure 10

FIGURE 8 – V_{HW}, HYSTERESIS WIDTH (VOLTS)

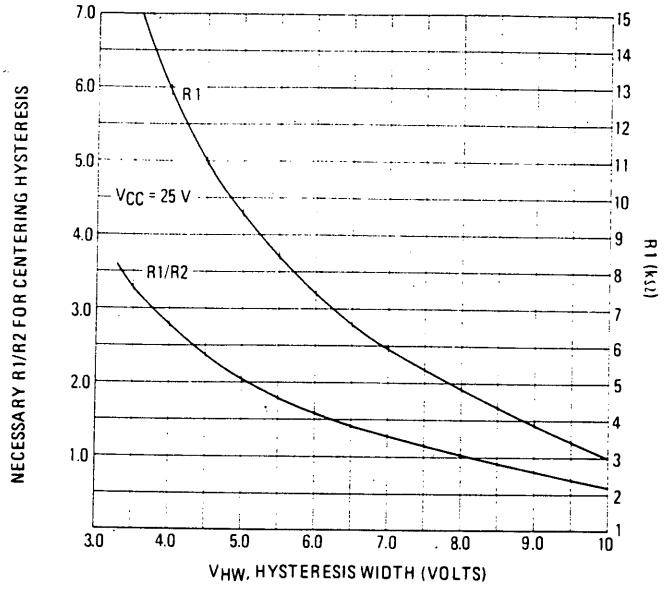


FIGURE 9 – MC696 AS SINGLE-ENDED SLOW-DOWN RECEIVER

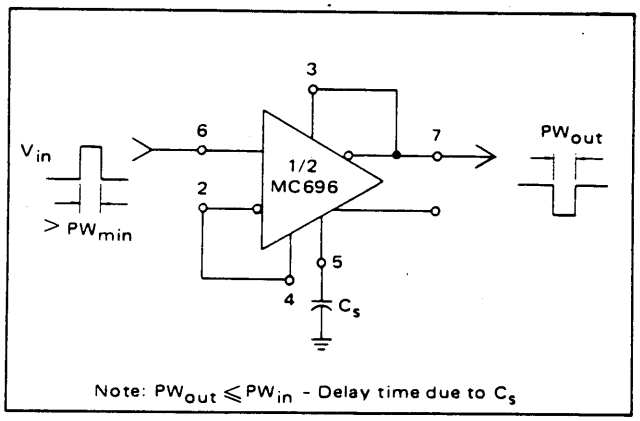
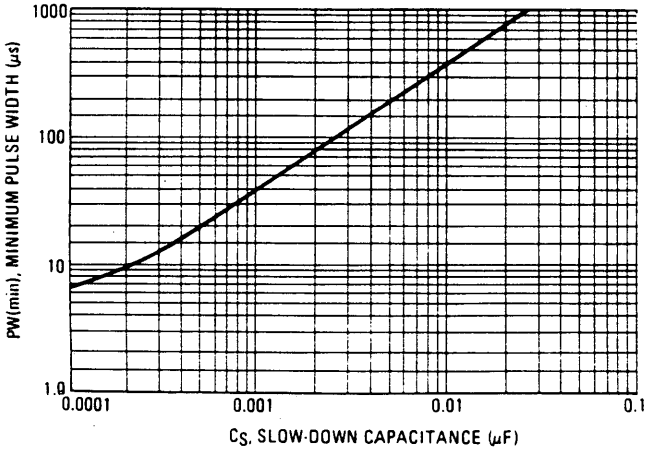


FIGURE 10 – MINIMUM PULSE WIDTH versus SLOW-DOWN CAPACITANCE



shows the minimum input signal pulse width necessary to trigger the circuit versus capacitance.

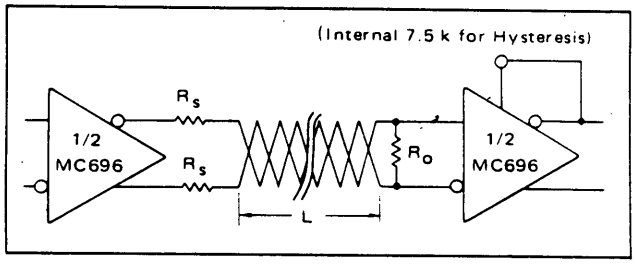
In order to avoid oscillations that might occur as a result of the slowly changing input voltage, hysteresis must be added to the circuit using the internal 7.0 k resistor, or a suitable value of resistance externally.

MC696 as Line Driver/Receiver/Repeater

One of the best applications of the MC696 is, of course, as a line driver/receiver/repeater, and because of its low frequency operation (< 500 kHz), many of the complicated effects associated with line driving and receiving can be ignored and calculations become straightforward.

In Figure 11, one device is used as a twisted-pair line driver and another as a line receiver. The balanced series resistance, R_S,

FIGURE 11 – USING MC696 AS DIFFERENTIAL LINE DRIVER/RECEIVER



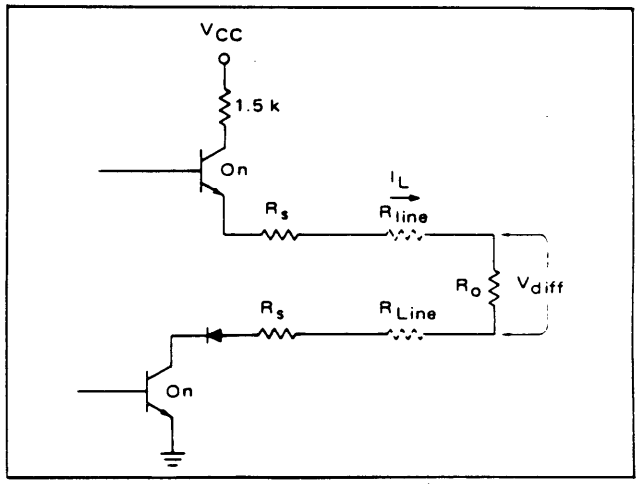
adds some series damping and limits the current through the line at higher power supply levels while setting the voltage levels at the input of the receiver for maximum common-mode noise rejection (i.e., bias the input differential voltage in the middle of the common-mode range). R_O merely terminates the line in its characteristic impedance (≈ 100 ohm for 30 turns/ft, AWG 24-28; twisted-pair) so that capacitive effects on the line may effectively be ignored.

The worst-case limits of the series resistor can be calculated roughly by looking at the dc equivalent circuit shown in Figure 12. The three major constraints are

1) $V_{diff.} < V_{diff.\ min} \approx 50$ mV
   (For safety margin use $V_{diff.} = 150$ mV)
2) $I_L < I_{SC}$ max.
3) Receiver input common-mode voltage centered in common-mode range (1.5 V < CMR < V_{CC} -1.5 V)

For V_{CC} = 15 V, these constraints require R_S to be about 5.0 k.

FIGURE 12 – DC EQUIV. CIRCUIT



If necessary, hysteresis can be added to the receiver to improve switching characteristics, and for upgrading the signal along extremely long lines, the MC696 can be used in a repeater configuration as shown in Figure 13.

FIGURE 13 – USING MC696 AS LINE REPEATERS

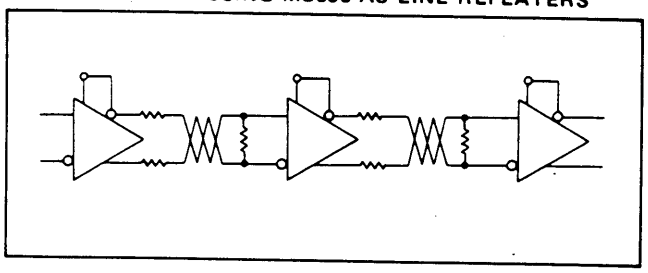
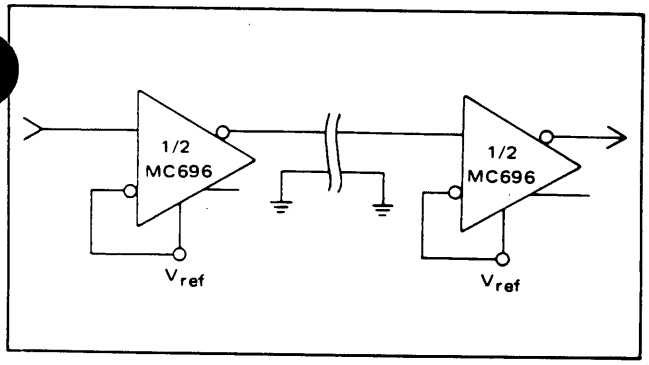


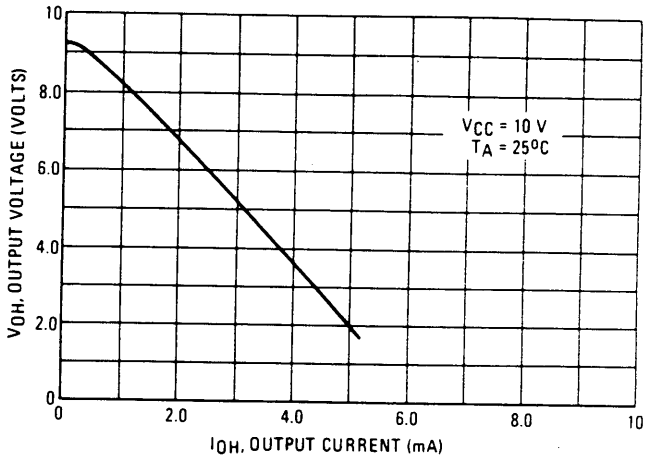
FIGURE 14 – USING MC696 AS SINGLE-ENDED LINE DRIVER/RECEIVER



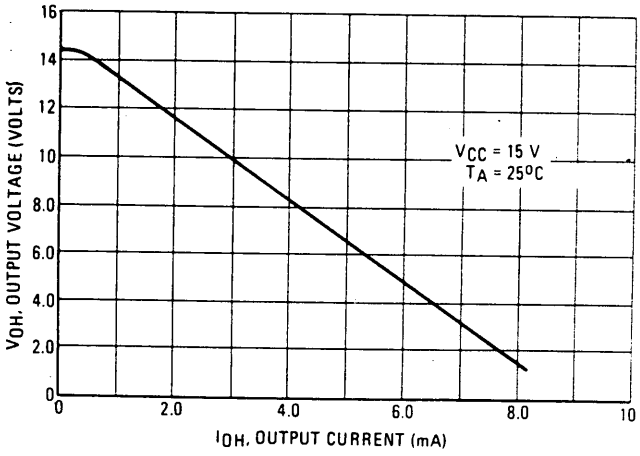
The MC696 can also be used as a single-ended line driver/receiver, as shown in Figure 14, with some sacrifice in noise immunity. With both the transmitter and receiver reference voltage set at the internal reference (1/2 V_{CC}), the noise immunity of the circuit is that of a typical MHTL gate (see application note AN-298 "Noise Immunity with High Threshold Logic"). By using the hysteresis and capacitor slow-down configurations discussed previously, improved immunity can be realized.

The following graphs portray typical MC696 electrical characteristics at +25°C.

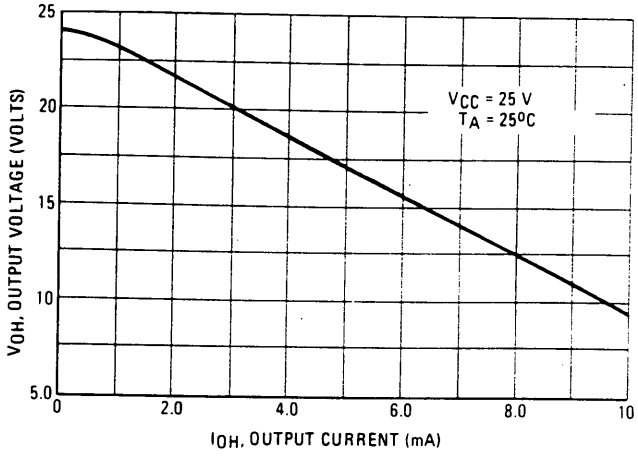
TYPICAL V_{OH} versus I_{OH}



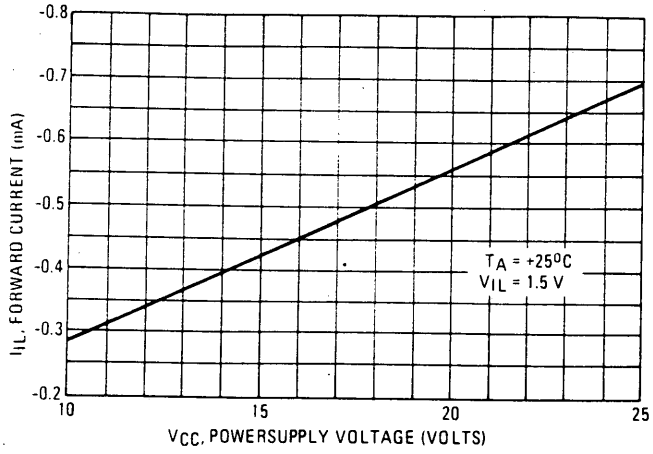
TYPICAL V_{OH} versus I_{OH}



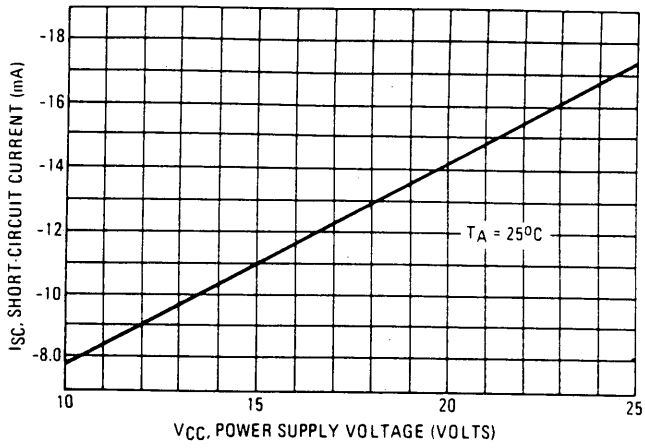
TYPICAL V_{OH} versus I_{OH}



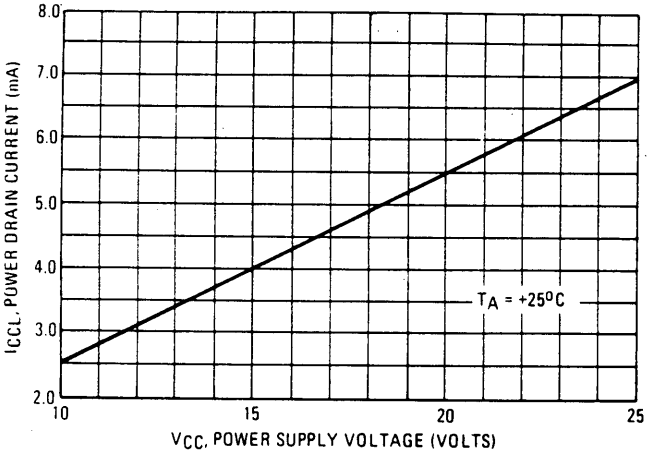
FORWARD CURRENT versus POWER SUPPLY VOLTAGE



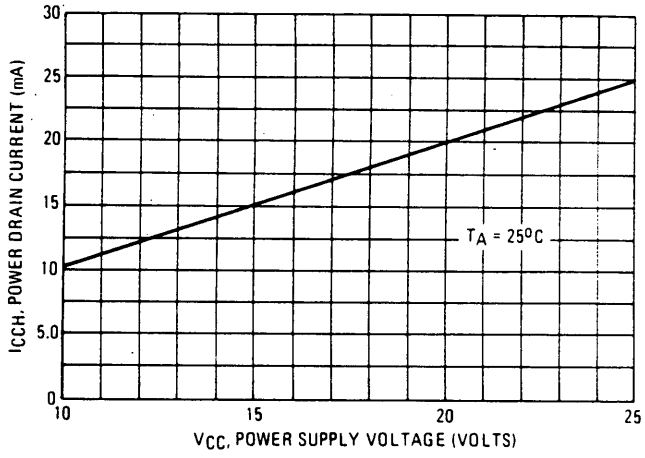
OUTPUT SHORT CIRCUIT CURRENT versus POWER SUPPLY VOLTAGE



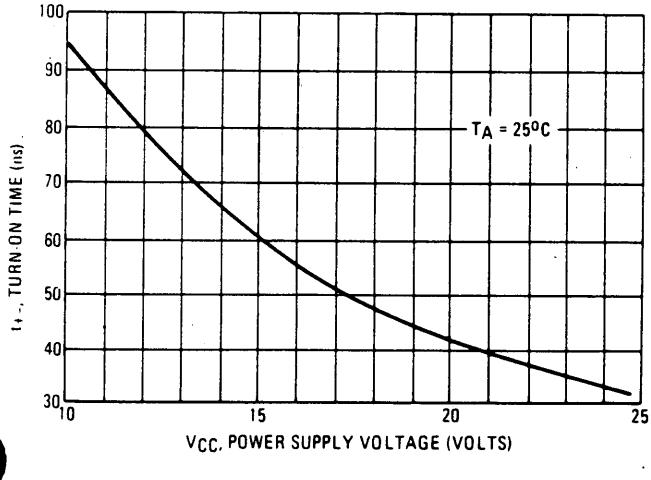
POWER SUPPLY DRAIN CURRENT versus POWER SUPPLY VOLTAGE



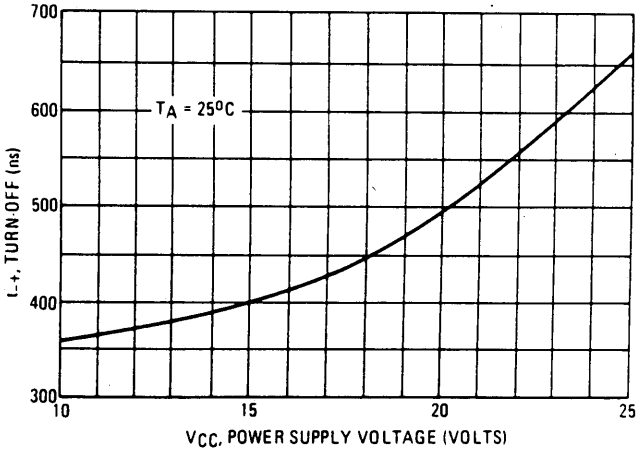
POWER SUPPLY DRAIN CURRENT versus POWER SUPPLY VOLTAGE



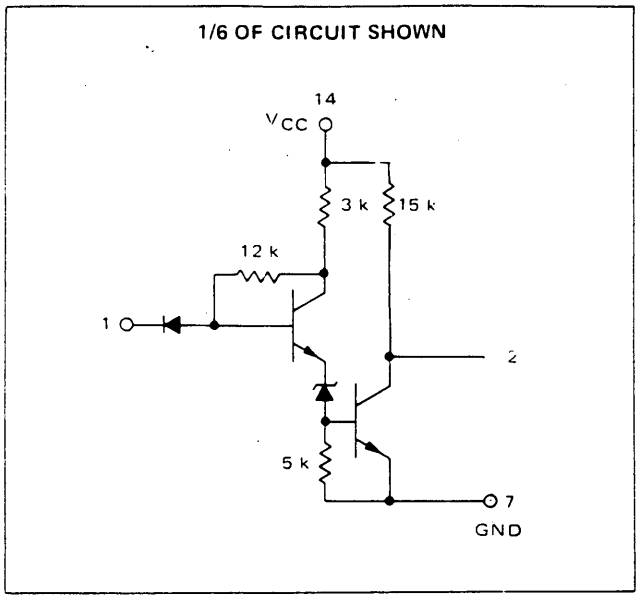
PROPOGATION DELAY TIME versus POWER SUPPLY VOLTAGE



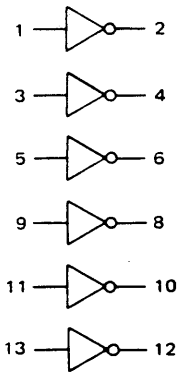
PROPOGATION DELAY TIME versus POWER SUPPLY VOLTAGE



MC697



The MC697 consists of six high threshold inverter gates with passive pull-up outputs.



Positive Logic: $2 = \overline{1}$

Input Loading Factor = 1
Output Loading Factor = 10
Propagation Delay Time = 125 ns typ
Typical Total Power Dissipation:
Inputs High = 246 mW
Input Low = 96 mW

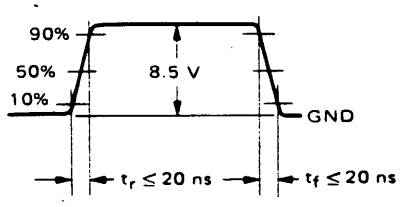
ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one inverter. The other inverters are tested in the same manner.

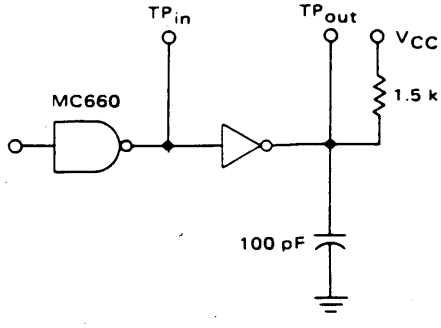
			TEST CURRENT / VOLTAGE VALUES (All Temperatures)										
			mA		Volts								
			I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	
			12.0	-0.03	6.50	8.50	1.5	16.0	16.0	15.0	14.0	16.0	
			MC697 Test Limits							TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:										
Characteristic	Symbol	Pin Under Test	−30°C		+25°C		+75°C		Unit	I_{OL}	I_{OH}	V_{IL}	V_{IH}	V_F	V_R	V_{CEX}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
			Min	Max	Min	Max	Min	Max												
Output Voltage	V_{OL}	2	-	1.5	-	1.5	-	1.5	Vdc	2	-	-	1	-	-	-	-	14	-	7
	V_{OH}	2	12.5	-	12.5	-	12.5	-	Vdc	-	2	1	-	-	-	-	-	14	-	7
Short-Circuit Current	I_{SC}	2	-0.5	-1.5	-0.6	-1.5	-0.6	-1.5	mAdc	-	-	-	-	-	-	-	-	-	14	1,2,7
Reverse Current	I_R	1	-	2.0	-	2.0	-	2.0	μAdc	-	-	-	-	-	1	-	-	14	-	7
Output Leakage Current	I_{CEX}	2	-	-	-	100	-	100	μAdc	-	-	-	-	-	-	2,14	-	-	-	1,7
Forward Current	I_F	1	-	-1.20	-	-1.20	-	-1.20	mAdc	-	-	-	-	1	-	-	-	-	14	7
Power Drain Current (Total Device)	I_{CCL}	14	-	-	-	9.0	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	1,3,5,7,9,11,13
	I_{CCH}	14	-	-	-	30	-	-	mAdc	-	-	-	-	-	-	-	-	-	14	7
Switching Times										Pulse In	Pulse Out									
	t_{1-2-}	2	-	-	-	250	-	-	ns	1	2	-	-	-	-	-	14	-	-	7
	t_{1-2-}	2	-	-	-	100	-	-	ns	1	2	-	-	-	-	-	14	-	-	7

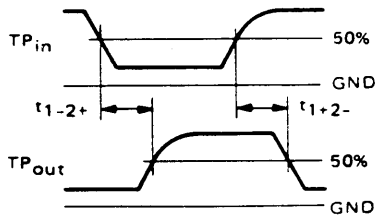
Pins not listed are left open.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



f = 500 kHz
DUTY CYCLE = 50%





See General Information section for packaging.

TELEDYNE SEMICONDUCTOR

TSC383
Decoder/Driver
• BCD-to-Seven-Segment

T-51-17

Features

- 40 mA OUTPUT SINK CAPABILITY
- BLANKING CAPABILITY PROVIDED
- LAMP TEST INPUT
- PIN AND FUNCTION EQUIVALENT OF TTL 7447A

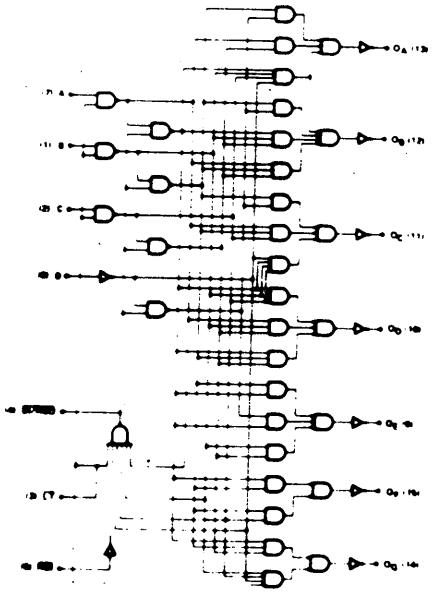
General Description

This device is characterized by seven open-collector outputs corresponding to the segments in LED display units such as the Monsanto Man-1. A 4-bit binary code applied to the data inputs causes the outputs to turn on in the conventional 7 segment code.

A blanking input is provided that turns all of the outputs off whenever it is low (regardless of the state of any other inputs). Also provided is a lamp test input that can be operated whenever the blanking input is high. A logical zero on the lamp test input will turn all seven outputs on. A ripple-blanking input is provided that has no effect except when each of the four data inputs are at logic zero. Then if the ripple-blanking input is at zero, when (and only when) the four data inputs are at zero, all seven outputs will be at logic one (display off). If the ripple-blanking input is at logic one (and the four data inputs are at zero), all outputs except O_G will be at zero ("0" displayed). If any of the data inputs are at logic one, the ripple-blanking input will have no effect.

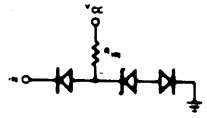
One pin brought out from the internal logic of the device can be used as either an input or an output. If the blanking input/ripple-blanking output is tied low (treating the pin as an input), all seven outputs will be at logic one. If the lamp test input is at one and the ripple-blanking input and the four data inputs are at zero, the ripple-blanking output will be at zero and the seven other outputs will be high.

Logic Diagram

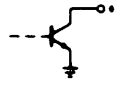


Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



CURT 3373

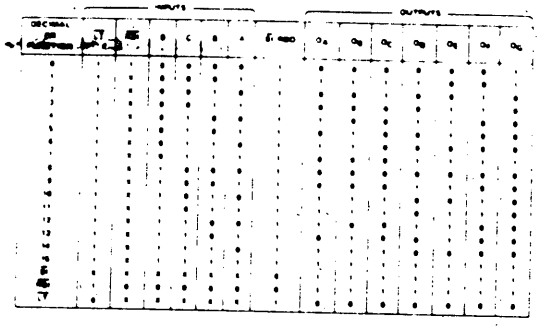
8918336 TELEDYNE SEMICONDUCTOR

Decoder/Driver 383

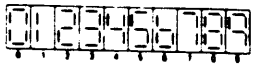
46C 04470 D

T-51-17

Truth Table



SEGMENT IDENTIFICATION



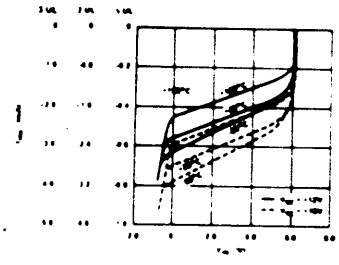
Loading Table

PINS	FUNCTION	LOADING
A,B,C,D	Inputs	1 UL
$\overline{RBI}$	Ripple-Blanking Input	1 UL
$\overline{LT}$	Lamp Test	3 UL
$\overline{BI}$	Blanking Input	2 UL
O_{A-G}	Outputs	See Electrical Characteristics
RBO	Ripple-Blanking Output	2 UL

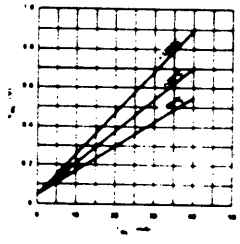
See page 20 for general electrical characteristics.

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT VOLTAGE OUTPUT LOW



Typical Applications

This device is characterized by seven open collector outputs corresponding to the segments in LED display units such as the Monsanto Man-1. A 4-bit binary code applied to the data inputs causes the outputs to turn on in the conventional 7 segment code.

CURRENT LIMITING RESISTORS

LED displays require that the current through them be limited by series resistors. The maximum current flow may be determined by either the LED display or the 383. Since the 383 is specified for 20 mA max. continuous duty (40 mA max. 50% duty cycle), displays that require their current to be held to 20 mA or less should have their resistor values calculated on the basis of the max. display current. Displays that must be limited to currents greater than 20 mA should have their resistor values calculated on the basis of the 20 mA max. current of the 383 (strobed applications will be considered separately).

Sample calculation - Monsanto MAN-1 has a 20 mA max. forward current and a voltage drop per segment of 3.4V typ.

$$R_{LIM} = \frac{V_{CC} - V_F - V_{OL}}{I_F} = \frac{13.0V - 3.4V - 0.7V}{20\ mA} = 445\Omega$$

(Fig. 1)

STROBING OPERATION

One popular technique for increasing the apparent brightness of displays is to pulse the displays with high currents and "average down" the power dissipation by lowering the duty cycle accordingly. The display manufacturers should be consulted as to the max. current vs. duty cycle that should be used with their units. The 383 should not be used with a display current of more than 40 mA NO MATTER WHAT THE DUTY CYCLE! Failure to observe this precaution can cause permanent damage to the device. In addition, the 40 mA figure should not be used unless the duty cycle is 50% or less. Limiting resistor values should be calculated on the basis of the strobed current.

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Sample Calculation - Assume the MAN-1 display is to be run at the max. current allowed by the 383 - 40 mA @ 50% duty cycle.

$$R_{LIM} = \frac{V_{CC} - V_F - V_{OL}}{I\ STROBE} = \frac{13.0V - 3.6V - 1.2V}{40\ mA} = 205\Omega$$

The strobing operation itself is accomplished by use of the Blanking Input (Figure 2).

A suggested circuit for an intensity modulator is shown in Figure 3.

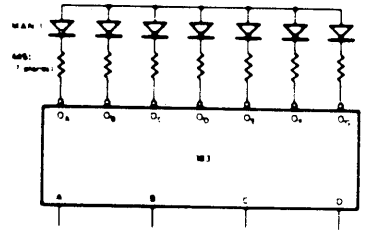
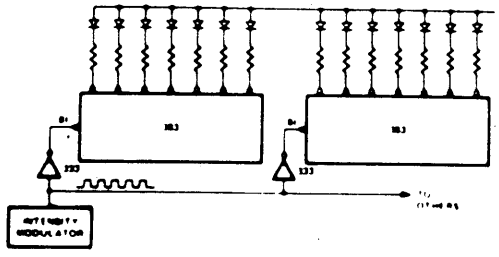
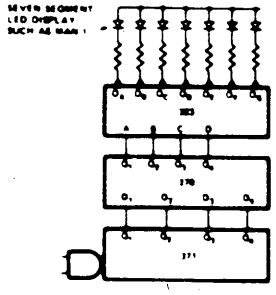


Figure 1





This application demonstrates the use of the 383 to drive seven-segment displays such as the Man-1. Since each output of the 383 will sink 20 mA, the display can be driven directly without external components other than current limiting resistors. Also illustrated is the 370 quad latch and 371 decade counter being used to acquire and store the number to be displayed.

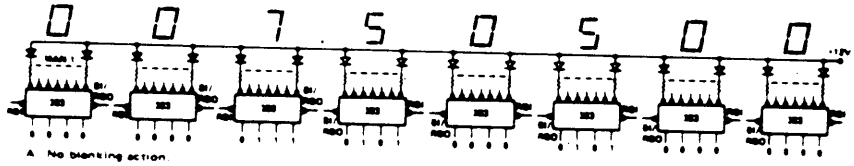
Figure 3. Intensity Modulator Circuit – Output duty cycle varies from 0% – 100% depending on switch setting.

Typical Applications (contd.)

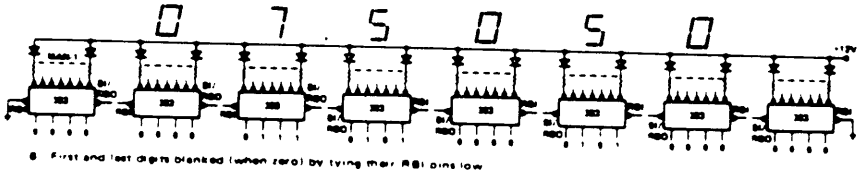
RIPPLE BLANKING

Provision has been made on the 383 for blanking out insignificant zeroes to increase legibility. Thus 007.50500 would be displayed at 7.505 if the ripple-blanking provisions were used. If the RBI pin is tied low, the display will be blanked every time a BCD zero is applied to the data inputs. This is normally done for the first and last digits of a display. In the previous example, 007.50500 would be displayed at 07.5050, the first and last digits being blanked since they are zero.

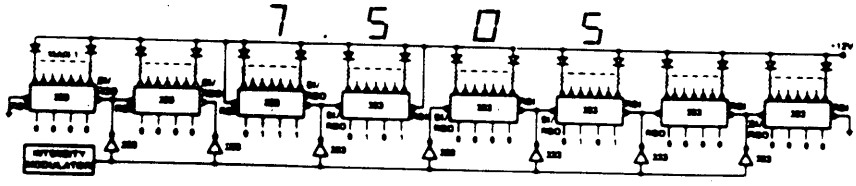
This scheme cannot be applied directly to all of the digits since it would cause 007.50500 to be displayed at 7.5_5. This problem is eliminated by the RBO output pin which delivers a logic zero whenever a BCD zero is on the data inputs. By feeding this information to the RBI inputs of the next 383, blanking will be accomplished only on nonsignificant zeroes. The RBO pin must be used with an 8.2k discrete pullup resistor.



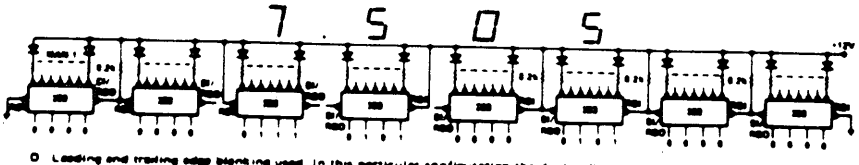
A. No blanking action.



B. First and last digits blanked (when zero) by tying their RBI pins low.



C. Leading and trailing edge blanking, combined with intensity modulation. Notice the 333's supply pullup resistors to the RBO pins, eliminating the need for discrete resistors.



D. Leading and trailing edge blanking used. In this particular configuration the digits adjacent to the decimal point will be displayed even if zero. This is usually considered desirable.

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Bipolar Interface Logic
Electrical Summary Data

Parameter	Definition	Type C* (V_{CC} = +12V ±1V) -30° C ≤ T_A ≤ +85° C	Test Conditions
V_{CC}	Supply Voltage	13V max 12V nominal 11V min	Voltage for other tests — see below
V_{INL}	Input Threshold Voltage Low	5.0V min	Guaranteed input low threshold for all inputs except 311 T_2 = 4.8V min @ 15V
V_{INH}	Input Threshold Voltage High	6.5V max	Guaranteed input high threshold for all inputs except 311 S&R inputs = 7.0V max
I_{INL}	Input Current Low, 1 Unit Load UL	2.1 mA max	At Vcc max with V_{IN} = V_{OL}
I_{INH}	Input Leakage Current, 1 Unit Load UL	10 µA max	At Vcc = max with V_{IN} = Vcc max
I_{MAX} 382	Output High Breakdown Current Open Collector Devices	2 mA max	V_{CEX} = +65V
V_{OL}	Output Low Voltage see Loading Table on Data Sheet	1.5V max	I_{OL} = F.O. x UL at Vcc min with V_{INL} = 5.0V and V_{INH} = 6.5V
V_{OL} 302 323 332 334 380 382 383 383	Output Low Voltage Open Collector Devices	4V max 4V max 4V max 4V max 1.2V max 2.5V max 7V max 1.2V max	I_{OL} = 16 mA 10 TTL UL I_{OL} = 6.4 mA 4 TTL UL I_{OL} = 6.4 mA 4 TTL UL I_{OL} = 6.4 mA 4 TTL UL I_{OL} = 30 mA I_{OL} = 7 mA I_{OL} = 20 mA 100% Duty Cycle I_{OL} = 40 mA 50% Duty Cycle
V_{OH}	Output High Voltage of all Devices Without Open Collector Except 382 and 386	10.0V min	At Vcc min, V_{INL} = 5.0V, V_{INH} = 6.5V, I_{OH} = F.O. x UL
V_{MAX} 302 323 332 334 380 381 380-386	Output High Breakdown Voltage Open Collector Devices	13.0V min 20.0V min 24.0V min 15.0V min 30.0V min	I_{MAX} = 4 mA I_{MAX} = 4 mA I_{MAX} = 0.5 mA I_{MAX} = 0.5 mA
V_{OHL}	Output High Voltage, Loaded of Active Pullup Devices Except 382 and 386	7.0V min	At Vcc nominal, V_{INL} = 5.0V V_{INH} = 6.5V, I_{OH} = -5 mA except -15 mA for 301 and -12 mA for 350 351
I_{CEX} 302.323.307 332.334 380.381 382 383 380-386	Output High Leakage Current Open Collector Devices	25 µA max 25µA max 25 µA max 50 µA max 25 µA max 100 µA max	V_{CEX} = Vcc max V_{CEX} = Vcc max V_{CEX} = Vcc max V_{CEX} = +55V V_{CEX} = Vcc max V_{CEX} = 30V
"0" NI	Zero State Noise Immunity	3.5V min	Guaranteed zero state noise immunity across temp range and Vcc ± 1V V_{INL} — V_{OL}
"1" NI	One State Noise Immunity	3.5V min	Guaranteed one state noise immunity across temp range and Vcc ± 1V V_{OH} — V_{INH}

Notes: F.O. is fanout in unit loads UL. Unit loadings are given in the pin tables on the individual data sheets. A unit load for High Noise Immunity Logic is defined by the above input specifications.

See individual data sheets for additional specifications.

*Military spec Type B Vcc = 12V and Type M Vcc = 15V are available to meet -55°C to +125°C temperature requirements. Available in ceramic package only. See ordering data.

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Electrical Summary Data (Continued)

Absolute Maximum Ratings

	L Package, Ceramic	J Package, Plastic
Storage Temperature	-65° C to +150° C	-55° C to +100° C
Lead Temperature 1/16 inch from case, 10 sec max	300° C	300° C
Continuous Supply Voltage		
Type C*, B*	+15.0V	+15.0V
Type A*, M*	+16.5V	+16.5V
Pulsed Supply Voltage less than 100 msec	+18.0V	+18.0V
Input Voltage any input		
Type C*, B*	-0.5 to +15V	-0.5 to +15V
Type A*, M*	-0.5 to +18V	-0.5 to +18V
Surge Sink Current less than 100 msec at 25° C T_A		
Standard Outputs	20mA	20mA
301, 302 and 303	100mA	100mA
306, 307, 332 through 335, 350, 351, 380, 381, 383	35mA	35mA
380-386	300mA	—
356	150mA	150mA
Expander Input Currents	-0.5 to +0.5mA	-0.5 to +0.5mA

Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

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Bipolar Interface Logic

Input Current Requirements

Device Number	I_{IHL} @ V_{CC} = 12V and V_{IL} = 1.5V (mA)	I_{IHL} @ V_{CC} = 15V and V_{IL} = 1.5V (mA)	I_{IHH} @ V_{CC} = 12 or 15V, V_{IHH} = V_{CC} (mA)
301	2.1	2.6	10
302	2.1	2.6	10
303	2.1	2.6	10
304	2.1	2.6	10
306	1.3	1.6	10
307	1.3	1.6	10
311	2.1-4.2	2.6-5.2	10-20
312	2.1-4.2	2.6-5.2	10-20
313	2.1-4.2	2.6-5.2	10-20
321	2.1	2.6	10
322	2.1	2.6	10
323	2.1	2.6	10
324	2.1	2.6	10
325	2.1	2.6	10
326	2.1	2.6	10
332	2.1	2.6	10
333	2.1	2.6	10
334	2.1	2.6	10
335	2.1	2.6	10
341	2.1	2.6	10
342	2.1	2.6	10
343	2.1-4.2	2.6-5.2	10-20
347	2.1-4.2	2.6-5.2	10-20
349	2.1	2.6	10
350	2.1	2.6	10
351	2.1	2.6	10
355	0.01	0.01	10
361	2.1	2.6	10
362	0.47	0.47	10
363	1.6	1.6	10
367	2.1	2.6	40
368	2.1	2.6	40
370	2.1-4.2	2.6-5.2	10-20
371	2.1-4.2	2.6-5.2	10-20
372	2.1-4.2	2.6-5.2	10-20
373	2.1	2.6	10
374	2.1	2.6	10
375	2.1	2.6	10
380	2.1	2.6	10
381	2.1	2.6	10
382	2.1	2.6	10
383	4.1-6.3	2.6-7.8	10-30
390	0.7	1.0	10
391	0.7	1.0	10
392	0.7	1.0	10
393	0.7	1.0	10
394	0.7	1.0	10
395	0.7	1.0	10
396	0.4	1.0	10

Notes

1. If there are several types of inputs on a device, then the currents listed above are the range of values for the various inputs. Check the individual data sheets to determine what the input current requirements are for each input.
2. A unit load is defined as I_{IHL} @ 12V = 2.1mA max, I_{IHL} @ 15V = 2.6mA max and I_{IHH} = 10μA max at 12 or 15V.
3. CMOS operated at 12 or 15V can be used to drive these devices even if the V_{OL} rating of the CMOS device does not appear to give enough sink current. This is possible since the 300 series of devices has input low rated at 1.5V instead of 0.8V as is common with TTL parts. The result is the CMOS output will be operated at a V_{OL} larger than is typical for CMOS or TTL systems.

Bipolar Interface Logic

T-43-13

Output Sink Current vs. Output Voltage

Device Number	V_{OL} (V)	I_{OL} (mA)
301	1.5	42
302	.4	42
303	.4	42
304	.4	42
306	1.5	18
307	.4	10
311	1.5	12
312	1.5	10
313	1.5	10
321	1.5	10
322	1.5	10
323	.4	10
324	.4	10
325	1.5	10
326	.4	10
332	.4	10
333	.4	10
334	.4	10
336	.4	10
341	1.5	10
342	1.5	10
343	1.5	10
347	1.5	10
349	1.5	10

Device Number	V_{OL} (V)	I_{OL} (mA)
350	1.5	16
351	1.5	16
355	2.0	75
361	.4	10
362	.4	10
363	.4	30
367	1.5	10
368	.4	10
370	.4	10
371	.4	10
372	.4	10
373	1.5	10
374	1.5	10
375	1.5	6
380	.4	20
381	.4	10
382	2.5	7
383	.7	20
390	.7	250
391	.7	250
392	.7	250
393	.7	250
394	.7	250
395	.7	250
396	1.5	12

Digital Logic — 300 Series

Ordering Information

PACKAGED DEVICES — TSC XXX X X

1. TELEDYNE SEMICONDUCTOR DEVICE
2. DEVICE NUMBER
3. ELECTRICAL GRADE AND TEMPERATURE RANGE
   - A – Industrial Temperature Range, 15 V, (−30 to +70°C)
   - B – Military Temperature Range, 12 V, (−55 to +125°C)
   - C – Industrial Temperature Range, 12 V, (−30 to +85°C)
   - M – Military Temperature Range, 15 V, (−55 to +125°C)
4. PACKAGE TYPE
   - G – Metal Can (TO–8)
   - H – Flatpack
   - J – Plastic Package
   - L – Ceramic Package (CerDIP)
   - Y – Dice

EXAMPLE: 303AL Operates Over an Industrial Temperature Range at 15 V and is a CerDIP Package

Product List — Digital Logic

301 Power NAND Gates Dual 5-Input
302 Power NAND Gates Quad 2-Input
303 Power NAND Gates Quad 2-Input
304 Power NAND Gates Triple 4, 3, 4-Input
306 NOR Gate Quad 2, 2, 3, 3-Input
307 NOR Gate Quad 2, 2, 3, 3-Input
311 Flip Flops Master/Slave RST
312 Flip Flops Dual J-K Edge Triggered
313 Flip Flops Dual J-K Master/Slave
321 NAND Gates Quad 2-Input
322 NAND Gates Dual 5-Input
323 NAND Gates Quad 2-Input
324 NAND Gates Quad 2-Input
325 NAND Gates 2, 2, 3, 3-Input
326 NAND Gates 2, 2, 3, 3-Input
331 Gate Expander Dual 5-Input
332 Hex Inverter Gates 4-Inverter 2-NAND
333 Hex Inverter Gates 4-Inverter 2-NAND
334 Hex Inverter Gates Strobed Hex NAND
335 Hex Inverter Gates Strobed Hex NAND
341 Multifunction Gates Dual 2-Wide 2-Input and/or Invert
342 Dual Monostable Multivibrator
343 Digital Comparator 4-Bit
344 Multifunction Gates Dual Expandable AND-NOR
347 Dual Retriggerable Monostable Multivibrator
349 Dual Retriggerable Pulse Stretcher
350 Multiplexers 8-Bit
351 Multiplexers Dual 4-Bit
355 Timer
361 Dual 11-16V to 5V Interface Voltage Translator
362 5V to 11-16V Interface Dual Translator
363 5V to 11-16V Interface Quad 2-Input NAND
367 Schmitt Trigger Quad(Active Pullup)
368 Schmitt Trigger Quad(Open Collector)
370 Flip Flop Quad D
371 Counters Decade
372 Counters Hexadecimal
373 Up-Down Counters Decade
374 Up-Down Counters Hexadecimal
375 Shift Register 4-Bit
380 BCD-to-Decade Decoder Drivers Lamp Driver
381 BCD-to-Decade Decoder Drivers Logic Driver
382 BCD-to-Decade Decoder Drivers Gas Tube Driver
383 Decoder Driver BCD-to-7 Segment
390 Dual Interface Buffers 4-Input Expandable AND
391 Dual Interface Buffers 2-Input AND
392 Dual Interface Buffers 2-Input NAND
393 Dual Interface Buffers 2-Input OR
394 Dual Interface Buffers 2-Input NOR
395 Dual Interface Buffers 4-Input Expandable NAND
398 Line Driver Receiver Dual Differential

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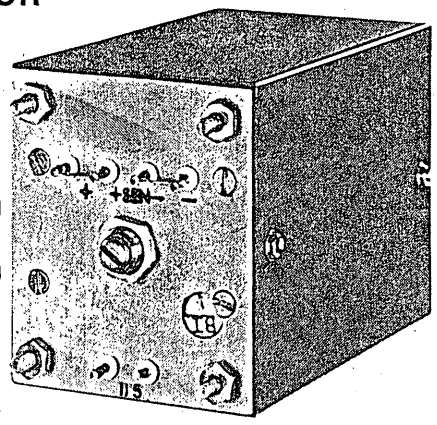
CEA3 SERIES — IMPROVED SWITCHING REGULATOR

STANDARD FEATURES INCLUDE



- OUTPUTS from 4.0 to 256VDC, .1 to 60 AMPS, to 640 WATTS.
- INPUTS 50 to 420 Hz, 95 to 135VAC or 105-190VDC.
- REGULATION, 1% or .1% for line plus load.
- 80°C BASE TEMPERATURE without derating.
  - Floating outputs, + or − output may be ±500VDC from case.
  - Remote sensing standard, all models, eliminates load lead effects.
  - Adjustment of output voltage, 50% to 100% is standard. Ranges tabulated below.
  - Remote adjustment optional at no charge.
  - Series starting with rated load, for multiple supply to a common load application.
  - Short circuit and overload output currents will not damage supplies.
  - No voltage overshoot on turn-on or turn-off.
  - MIL-T-27 modular case sizes with removable covers for servicing.
  - Critical components pretested, aged, and graded.
- BURN-IN (stabilization), 16 hrs. min. at rated load and high base temperature.
- 100% TESTING after burn-in, test data with shipment. **Specifications guaranteed, not just typical.**
- 3 YEAR WARRANTY for parts and labor against defects in workmanship and materials.

SPECIFICATIONS — IMPROVED

REGULATION — STABILITY — RIPPLE — BASE MODEL PRICE

Class of Regulation	Line Plus Load Regulated	Line Regulation for 10% Line Change	Load Regulation 10% Load to Full Load	Temperature Coefficient Per Degree C	Stability for 40 Hours	Ripple P-P	BASE MODEL PRICE
A	0.5%	0.25%	0.25%	0.5%	0.5%	1.0%	Tabulated below
B	±0.1%	±0.05%	±0.05%	±0.02%	±0.1%	0.2%	A plus $30.00

Input Voltage and Frequency: 105 to 125 volts, 50 to 420 Hz or 120 to 180VDC.

Output Voltage and Current: 4.0 to 256VDC, 0.1 to 60A. See correlation in table below.

Efficiency: Up to 80%. The output rectifier voltage drop of 1.2 volts is a major loss, hence a 5V output is 64% on some models.

Recovery Time: Typically less than 1ms for a 50% to 100% load change.

Insulation Resistance: 100 Megohm DC standard for input, output and case.

Temperature, Base: −20°C to +80°C operating, −40°C to +85°C storage.

Thermal Data: Details associated with thermal curve numbers (4 thru 9) in table below are shown on page 19.

Size-Weight-Terminations: Details associated with MIL-T-27 case (GA thru RA), tabulated below, are shown on pages 10 and 20.

PART NUMBERS

Example: .1% Reg, 5V, 60A, with options "F" and "W"; "CEA3B50X603FW"

YOUR SELECTION: **CEA3**_____

Specify regulation — Insert A or B

Specify output voltage — Insert any digit, 40 to 256

Specify voltage decimal — Insert X, Y or Z

Specify desired options — Insert option symbols

Specify output currents — Insert bracketed digits

OUTPUT VOLTAGE		OUTPUT RATED CURRENT																														
2 Digits Under 10V 3 Digits 10V and Over	Decimal Code	.1A (101)			.25A (251)			.5A (501)			1A (102)			2.5A (252)			5A (502)			10A (103)			20A (203)			40A (403)			60A (603)		
† Specify max. voltage listed for adjustable standards Select any voltage between limits for "F" option		Size	Thermal	A-Reg. Price	Size	Thermal	A-Reg. Price	Size	Thermal	A-Reg. Price	Size	Thermal	A-Reg. Price	Size	Thermal	A-Reg. Price	Size	Thermal	A-Reg. Price	Size	Thermal	A-Reg. Price	Size	Thermal	A-Reg. Price	Size	Thermal	A-Reg. Price	Size	Thermal	A-Reg. Price
4.0 to 8.0	X													GA	5	237	HA	6	286	JA	7	314	MA	7	385	NA	9	446	PA	9	501
*8.0 to 9.9 10.0 to 16.0	X Y										GA	5	237	HA	6	286	JA	7	330	KA	8	352	NA	9	446	RA	8	622			
16.0 to 32.0	Y							GA	5	237	NA	5	275	JA	7	330	KA	8	352	NA	8	446	RA	7	622						
32.0 to 64.0	Y				GA	5	237	HA	5	275	HA	6	330	KA	8	352	NA	8	440	RA	7	622									
*64.0 to 99.9 100 to 128	Y Z	GA	4	237	HA	5	275	JA	6	314	KA	7	330	NA	8	446	RA	7	622												
128 to 256	Z	HA	5	275	JA	6	314	KA	7	352	NA	7	446	RA	7	622															

† Adjustment from 50% to 100% is standard for the ranges shown.

* These are single standard supplies for the ranges (8.0 to 16.0VDC) & (64.0 to 128VDC), they are shown split to indicate decimal code for application of "F" options.

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1 Aerovista Park, San Luis Obispo, Calif. 93401
Toll-Free: Phone 800-235-4150 • In Calif. 800-592-5910

AC/DC-DC HF Regulated COMPACT MODULAR POWER SUPPLIES

CEA3 SERIES

OPTIONS

The extra charge for each option is either a flat rate or percentage of the base model price; add the larger number to the base price.

Symbol Option	Option Description	Prices	Delivery (Weeks Added)	REMARKS
	FIXED OUTPUTS			
F	Fixed output ±1.0%	No charge	None	Not available with "R" options.
F1	Fixed output ±0.2%	$15	1	Available in both classes of regulation. Available in class B only
	ADJUSTABLE OUTPUTS			
G1	Output adjust range ±10%	No charge	None	Increases resolution of adjustment output.
	EXTENDED TEMPERATURE RANGE			
H1	Temperature range −55°C to +80°C	$100 or 50%	4	Requires next larger case size. Storage to −62°C.
H2	Temperature range −40°C to +80°C	$20 or 20%	4	Storage to −55°C
H3	Temperature range −55°C to +115°C	$200 or 100%	6	Requires next larger case size. Storage to −62°C.
	INPUT VOLTAGE AND FREQUENCY			
L	Input 95-135VAC, 50-420 Hz or 105-190VDC	$20 or 10%	1	Derate maximum current to 60% of rated output.
	SPECIAL CONNECTIONS			
N	Octal plug in lieu of standard terminations	$15	3	Specify option "R" or "F" with "N". Sizes GA or larger, 5 amps or less.
N1	Screw terminals #6-32	$15	3	Used for connections of 20A or less. HA size or larger.
	PROTECTION CIRCUITS			
Std.	Current limiting	No Charge	1	Limits current to protect system circuit.
P2	Overtemperature cutout	$20	1	Limits base temperature to maximum rated. Self restarting.
P3	Crowbar voltage limit	$30 or 15%	1	Protects power supply and system circuit under all circumstances. Operates at 10% or 1 volt, whichever is greater over maximum settable voltage. Remove input power to restart.
	REMOTE PROGRAMMING			
R	Remote adjust (no pot provided)	No charge	None	Remote programming options allow power supply to be externally adjusted.
R2	Remote adjust plus internal pot	$5	1	
R3	Remote adjust with pot provided	$5	1	
	HIGH FLOAT VOLTAGE			
U	Output float up to ±1000V	$10 or 10%	1	Either output terminal will withstand ±1000 volts to case or input.
	RUGGEDIZED			Weight increased about 50% (except W2).
W	Potted for ruggedization in polyurethane resin. GA, HA, JA	$10	1	Fixed output or remote programming option is required with option "W".
	KA, LA	$15	1	
	MA, NA	$20	1	
	PA	$25	1	
	QA	$30	1	
	RA	$35	1	
W2	Light weight rigid foam	"W" + $20.00	1	

CASE SIZES AND WEIGHTS (UNPOTTED)

CASE SIZE	GA	HA	JA	KA	LA	MA	NA	PA	QA	RA
WIDE	2¾	3 1/16	3 1/16	3 13/16	4 13/16	4 11/16	5 1/16	6 1/16	7 1/16	8 1/16
DEEP	2⅜	2⅜	3 1/16	3⅜	3 11/16	4	4 5/16	4 13/16	5 1/16	6 1/16
HIGH	3 13/16	4¼	4⅞	5¼	5 5/16	6	6 13/16	6 13/16	7 1/16	7 1/16
WT (lbs)	1	1½	1⅞	2½	3⅓	4¼	5⅜	7¼	10	18

PRICE

The **total price** is the **base model price** from the regulation table, **plus** the **price of optional features** selected.

PRICE EXAMPLE: "CEA3B160Y102LRW"

"B"	$20	"B" REGULATION BASE MODEL PRICE	$257.00
"160Y102"	237		
"L"		OPTION	23.50
"R"		OPTION	NO CHARGE
"W"		OPTION	5.00
		TOTAL PRICE	$285.50

Discount Schedule

Quantity	Discount
1-4	net
5-9	less 5%
10-24	less 10%
25-99	less 15%
100-	factory

TERMS

NET 30 days, F.O.B. San Luis Obispo, California.

DELIVERY

Regulation class "A" and "B" supplies 4 weeks. Some options extend delivery as shown above. Shipments will be as directed, United Parcel where serviced, or Parcel Post for the remaining.

1 AEROVISTA PARK, SAN LUIS OBISPO, CA. 93401 TOLL-FREE: PHONE 800-235-4150 • IN CA. 800-592-5910
CEA
A Division of Berkleonics, Inc.

THERMAL DATA

Heat flows from regions of high temperature to regions of low temperature by:

1. CONDUCTION — heat flow within a material without material motion required.
2. CONVECTION — heat flow by physical motion of a material; e.g., liquids and gases.
3. RADIATION — heat flow by radiant energy, materials for the flow path not required.

The heat conductivity of various substances are: Silver 1.0, Copper .9, Gold .7, Aluminum .5, Iron .15, Steel .1, Silica .0024, Mica .0018 (.5 conductivity corresponds to about 1°C per inch or a heat flow of 5.3 watts per square inch).

The conductivity of some aluminum alloys are three times better than others, 1100F and 6063T5 are two of the better alloys.

Convection by natural means can vary about 2 to 1 for flat surface up versus a flat surface down.

Forced convection (fan-driven air) is a common cooling procedure and has the effects shown in the curve below.

Radiation depends to a large extent on the roughness of the surface. The rougher the better (e.g., the emissivity of aluminum unoxidized is .02 vs .3 oxidized).

From the above it is clear that heat flow is complex and quite variable. THE DATA GIVEN BELOW IS PRESENTED NOT AS ABSOLUTE BUT RATHER AS A GUIDE.

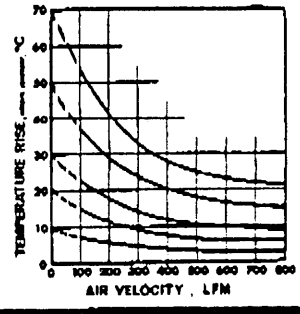
THERMAL DATA — Worst Case Condition: high input voltage, full load, no forced air.
(a) Power Dissipated Internally (watts) (b) Temp. Rise, chassis mounted (°C) (c) Temp. Rise, chassis & thermal radiator mounted (°C)

THERMAL NUMBERS	DATA	CASE SIZE FA	BA	HA	JA	KA	LA	MA	NA	PA	QA	RA	SA	TA
1	(a)	2.9	3.9	4.8	6.5	8.0	9.5	11	13	17	24	32	39	47
	(b)	2.9	3.9	4.8	6.5	8.0	9.5	8	9	12	11	14	17	20
	(c)	—	—	—	—	—	—	6	7	8	6	9	7	9
2	(a)	3.8	5.2	6.4	8.6	11	13	15	17	23	31	43	52	63
	(b)	3.8	5.2	6.4	8.6	11	13	10	12	15	13	18	22	26
	(c)	—	—	—	—	—	—	8	10	10	8	11	10	12
3	(a)	5.7	7.8	9.6	13	16	19	22	26	34	47	65	78	94
	(b)	5.7	7.8	9.6	13	15	18	14	17	22	20	27	31	37
	(c)	—	—	—	—	—	—	12	14	15	12	17	14	17
4	(a)	7.6	10	13	17	21	25	30	35	45	63	86	100	130
	(b)	7.6	10	13	16	20	23	20	22	28	26	34	38	46
	(c)	—	—	—	—	—	—	16	18	19	16	22	18	24
5	(a)	11	16	19	26	32	38	45	52	68	94	130	160	190
	(b)	11	15	18	24	29	34	29	32	40	37	46	53	58
	(c)	—	—	—	—	—	—	23	26	28	24	31	28	32
6	(a)	15	21	26	35	43	51	60	70	91	130	170	210	250
	(b)	14	20	24	32	38	42	36	41	49	46	55	62	67
	(c)	—	—	—	—	—	—	30	34	36	31	39	35	40
7	(a)	23	31	39	52	64	76	90	100	140	190	260	310	380
	(b)	22	28	35	43	49	55	49	52	63	58	69	75	—
	(c)	—	—	—	—	—	—	42	45	49	42	52	47	53
8	(a)	30	42	51	69	85	100	120	140	180	250	340	420	500
	(b)	27	37	42	52	59	64	58	63	71	67	78	—	—
	(c)	—	—	—	—	—	—	50	56	58	50	61	57	62
9	(a)	43	63	77	100	130	150	180	210	270	380	520	620	750
	(b)	38	49	55	64	73	78	71	77	—	—	—	—	—
	(c)	—	—	—	—	—	—	64	69	71	64	75	69	76
CHASSIS ⅛" x (in. x in.)		10x10	10x10	10x10	10x10	10x10	10x10	12x12	12x12	12x12	15x15	15x15	15x15	15x15
RADIATORS (Qty.) P/N		—	—	—	—	—	—	(1) CEATR1	(1) CEATR1	(2) CEATR1	(2) CEATR2	(2) CEATR2	(4) CEATR2	(4) CEATR2

Example: Thermal No. 5, Case SA may dissipate 160 watts, have a base temperature of 53°C above ambient for a 15" x 15" x ⅛" aluminum chassis mounting, reduce the 53°C to 28°C by adding four CEATR2 THERMAL RADIATORS (mounted thru chassis to base), and then have the 28°C decreased to 11°C by 400LFM air velocity to all surfaces.

The base limitation to the life of your CEA Power Supply is the upper temperature of the internal components. As with most temperature-affected items, the cooler the unit the greater the life expectancy. Keeping the base temperature of your power supply under +60°C during normal operation will cause the internal components to be safe and give a good life.

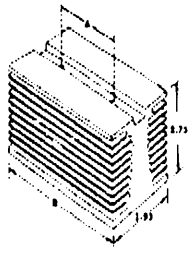
Temperature stability may require from 10 to 40 minutes after a change, e.g., turn-on. This can be an aid during intermittent duty, and should be remembered when performing a steady-state systems analysis.



THERMAL RADIATORS

Models CEATR1 and CEATR2 Thermal Radiators, designed for use with CEA Power Supplies, may be mounted directly into the module base or on the opposite side of the mounting body. The mounting hole configuration in the Thermal Radiators and the base of each Module are symmetrical so that the radiators may be mounted for airflow in either direction across the base of the Module. A coating of silicon grease should be applied on each mating surface of the Module, mounting body and Thermal Radiator. The mounting body must be a smooth, highly thermal conductive metallic surface. (Minimum $25.00 order.)

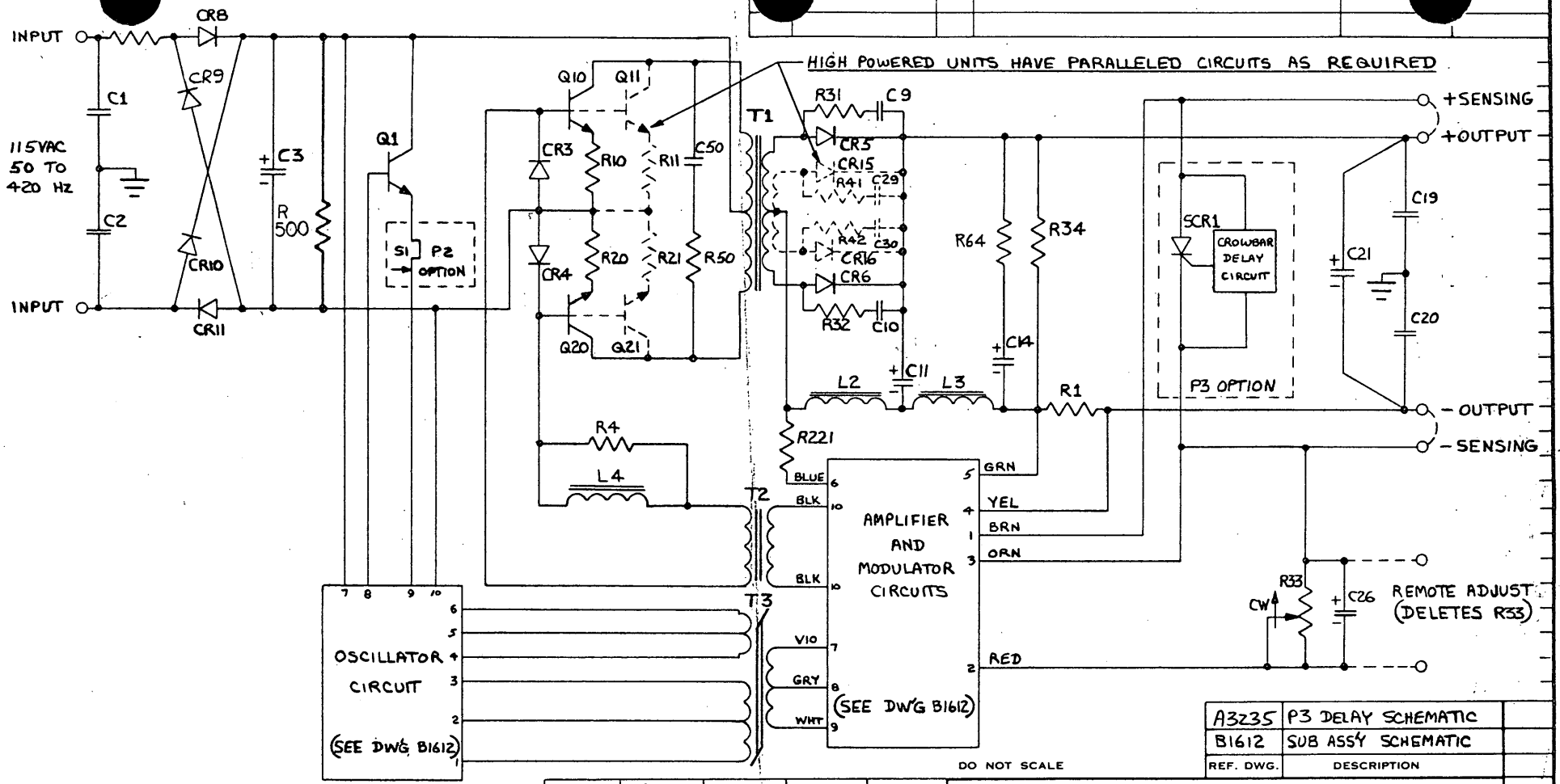
Thermal Radiator Model No.	Radiation Area (sq. in.)	Dimensions A	Dimensions B	Weight (Pounds)	Price Each
CEATR1	75	1.000	1.93	0.75	$18.00
CEATR2	150	2.000	3.93	1.50	22.00



(Subject to Change Without Notice)

D-8000

PART NO.	NO. REQ'D	DESCRIPTION	MATERIAL	FINISH



DO NOT SCALE

REF. DWG.	DESCRIPTION
A3235	P3 DELAY SCHEMATIC
B1612	SUB ASSY SCHEMATIC

REV.	E.C.O.	CHG'D. BY	DATE	APP'D.
D	8197	AU	12-9-81	MW
C	6441	NKE	4/25/78	
B	ADDED R61 + R64	NKE	1-4-78	
A	4178	NKE	1-28-74	
E	10363	AU	6/10/87	KAA

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TITLE SCHEMATIC - CEA 3 SERIES, POWER SUPPLIES

DRAWN BY	DATE	SCALE	DRAWING NO.	REV.
NKE	8-12-71	-	B1660	E

CHECKED BY — APPROVED BY — FIRST JOB NO. -

NEXT ASSY.

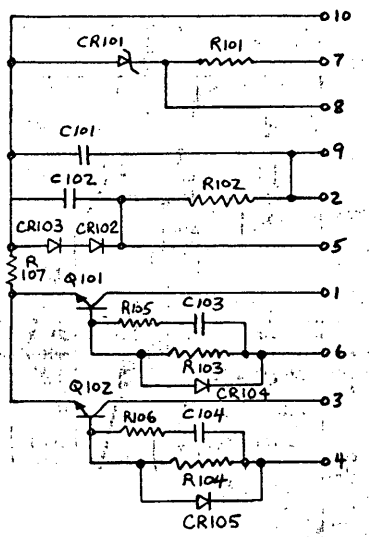
NOTES: UNLESS OTHERWISE SPECIFIED

TOLERANCE UNLESS NOTED	.XX ± .030 .XXX ± .015	FRACTIONS ±	ANGLES ±

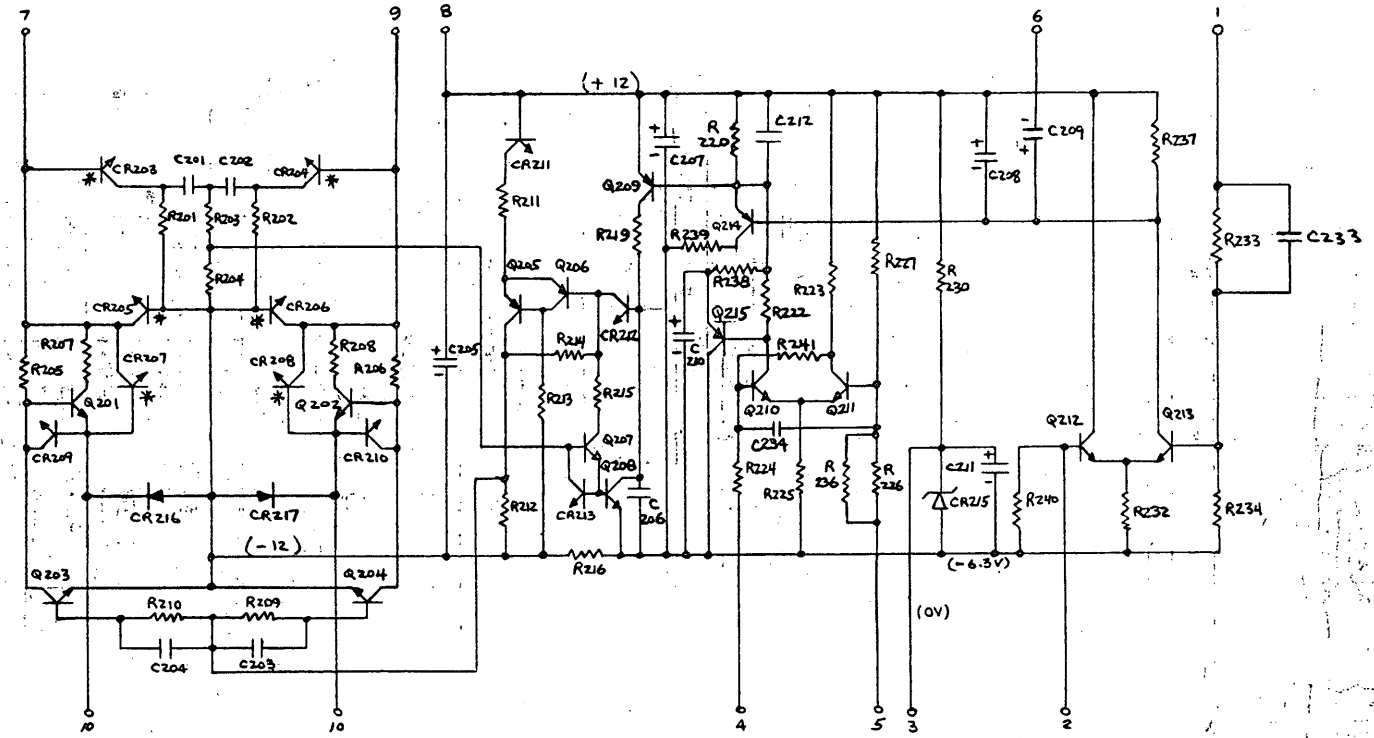
DIETERICT-POST CLEARPRINT 1025-6 FORM 3001

D-0-N

PART NO.	NO. REQ'D	DESCRIPTION	MAT'L	FINISH



OSCILLATOR CIRCUIT



MODULATOR AND AMPLIFIER CIRCUIT

* SELECTED FOR V_{CBO} = 60V (A2360)

NOTES: UNLESS OTHERWISE SPECIFIED

REV.	E.C.O.	CHG'D. BY	DATE	APP'D.
G	10749		8/28/89	
F	6846	Cwm	9/11/78	Cwm
E	ADDED R107		1/4/78	
D	ADDED R241, Q215		5/8/74	
C	ADDED C211, C212, CR214, 215		4/4/74	
B	COMPLETE REVISION		12/13/72	
A	ADDED Q214, R237, R238, C230		3/28/72	

TOLERANCE UNLESS NOTED	.XX ± .030 .XXX ± .015	FRACTIONS ±	ANGLES ±

DO NOT SCALE

REF. DWG.	DESCRIPTION
A3235	P3 DELAY SCHEMATIC
B1660	CEA3 SCHEMATIC
B1611	CEA2C SCHEMATIC

CEA a division of Berkleonics, Inc.

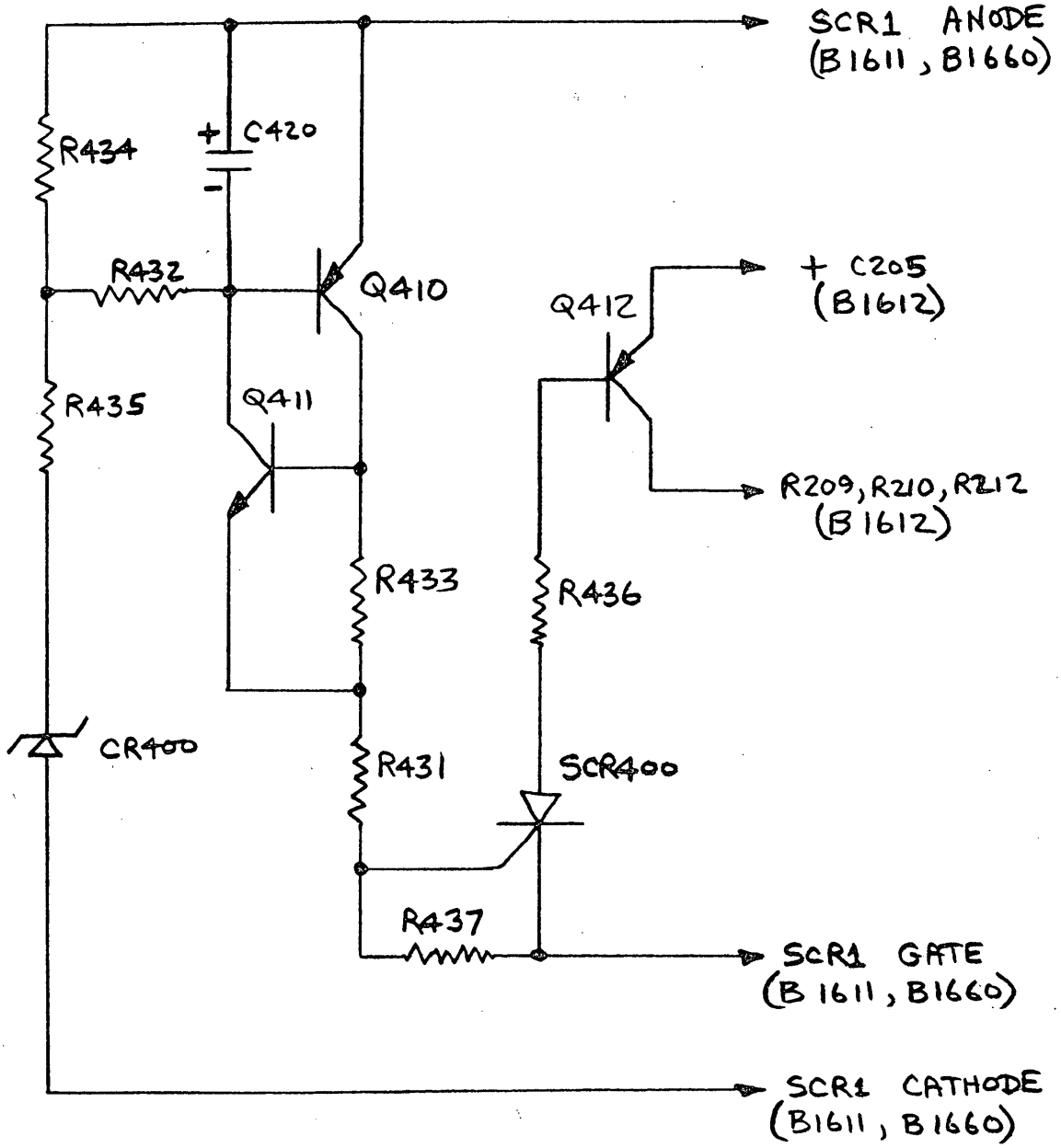
TITLE SUB ASS'Y SCHEMATIC - CEA2C AND CEA3 SERIES

DRAWN BY	DATE	SCALE	DRAWING NO.	REV.
	8/20/71	-	B1612	G
CHECKED BY	APPROVED BY	FIRST JOB NO.		NEXT ASSY.

DIETERICT-POST CLEARPRINT 1025-6 FORM 2001

ITEM	PART NO.	NO. REQ'D.	DESCRIPTION	MATERIAL	FINISH

A3235



ASS'Y DWG: A3227

L/M: 1372

REV.	E.C.O.	DATE	CK BY	APP'D.

CEA a division of Berkleonics, Inc.

TITLE P3 DELAY + FOLDBACK SCHEMATIC-CEA3, CEA2C

TOLERANCE UNLESS NOTED	.X ± .060 .XX ± .030 .XXX ± .015	FRACTIONS ± 1/32	ANGLES	DRAWN BY NKE	DATE 4/4/74	SCALE —	DRAWING NO. A3235	REV.
				CK BY	APP BY			

FTI

P.O. Box 261
Ashton, MD 20861
(301) 570-8934
(301) 570-8790 (Fax)

Installation Instructions Replacement of LSSP Power Supplies at Grand Gulf Nuclear Station

Prepared for Entergy Operations, Inc.

Purchase Order MPY00669

Report # 99110390
April 10, 2001
Revised -

Michael J. Bandarenko — 4/10/01 (date)
Engineering Manager

David J. FitzGerald — 4/10/01 (date)
Engineering Intern

1. BACKGROUND

FTI was tasked to develop replacement power supplies for the Load Shedding Sequencing Panels (LSSP) for Entergy Operations. The existing power supplies used in the LSSP cabinets are obsolete, because the company that manufactured them, a power supply vendor known as CEA, has gone out of business.

Because the power supplies can no longer be acquired, new assemblies were designed to do the same job, in the same space, within the same tolerances. Suitable power supplies manufactured by another power supply company (Lambda) were identified which, when appropriately packaged, require no mounting modifications to the LSSP cabinet. The replacement power supplies physical dimensions and mounting hole locations are different than the existing power supplies. Consequently, replacement of the existing LSSP power supplies required the design and manufacture of a new power supply mounting plate to simulate the CEA power supplies mounting characteristics.

The new power supplies with their associated heat sinks are mounted to this bracket/plate and the bracket has mounting studs that duplicate the CEA power supplies mounting stud arrangement. Fabricating a new mounting plate and assembling the replacement power supply to this plate permits installation of a power supply assembly which duplicates the mounting of the current power supplies. This alleviates any modifications to the current power supply chassis installed in the LSSP cabinet.

The new power supplies also require an external resistor to adjust the output voltage. This external resistor is required even if the output voltage is fixed. This resistor is mounted (soldered) across the power supply terminal pins. Installation of the current power supplies requires soldering of the supply terminals to the cabinet wiring. This will not be true of the replacement supplies. New wiring between the power supplies and the cabinet equipment is part of the replacement power supplies since the existing wire lengths are not compatible with the new power supply terminal locations.

Step-by-step installation instructions for field technicians are required to ensure proper procedures are followed. This document contains unpacking procedures, instructions for the removal of the existing power supply, installation of the replacement power supply, and wiring procedures. The procedures in this document will ensure that the power supply is installed correctly and in a safe manner for equipment and personnel.

2. UNPACKING PROCEDURES

The replacement power supply is individually boxed and sealed in a vapor proof bag that contains desiccant. Open the box by cutting the sealing tape. Remove the vapor proof bag containing the power supply form the box. Open the vapor proof bag by cutting the bag near the point of heat sealing. This will allow resealing of the bag if necessary. Remove the power supply from the bag and the bubble wrap from the power supply.

3. REMOVAL OF EXISTING POWER SUPPLY

Technicians need to remove the old power supply from the LSSP equipment. To do this, first open the LSSP panel door and turn off the ESF power to the LSSP. Then access the interior of the LSSP by swinging open the Control Panel. Disconnect the wires from the power supply to the terminal blocks (TB) and/or relay. Do this by removing the screws securing the wires at the TB or relay and removing the wires. Remove the nuts from the underside of the Control Panel securing the power supply using a 3/8-inch wrench for the 15-volt power supply and 7/16-inch wrench for the 24-volt power supply. Set nuts aside for reinstalling the new power supply. Remove and dispose of the old power supply in accordance with local procedures.

4. INSTALL REPLACEMENT POWER SUPPLY

Once the old power supply is removed, the new power supply may be installed. First remove the bottom nut, lock washer and flat washer from each power supply mounting stud.

DO NOT REMOVE THE NUTS CLOSEST TO THE MOUNTING PLATE THAT FASTEN THE BOLTS TO THE POWER SUPPLY ASSEMBLY.

Orient the power supply so that the plate on the back of the power supply faces toward the back of the LSSP when the Control Panel is closed. See Figure 1 for correct orientation of new power supply. This orientation is necessary to satisfy seismic qualification. As a further orientation check, the hole in the bottom of the power supply bracket should line up with the large hole in the power panel plate. Then set the power supply mounting bolts in their respective holes in the bottom of the Power Panel Plate. Use the mounting hardware removed above to remount the new power supply or use the mounting hardware from the previously removed supply to secure the power supply to the Power Panel Plate. Discard excess material or save for spare parts.

5. WIRING OF POWER SUPPLY

Reconnect wiring to the TB and/or relay. Output voltage wires may need to be routed through the clearance holes in the mounting bracket and power supply panel to access TB1 and TB 2 terminals. Other wires can be routed on top of the power panel plate. Follow the identifying wire markers to determine correct connection points.

CAUTION – POWER SUPPLY WILL BE DAMAGED BY APPLICATION OF REVERSE POLARITY OF THE INPUT SUPPLY VOLTAGE (+125 VDC). ENSURE CORRECT CONNECTION OF POWER SUPPLY LEADS PRIOR TO ENERGIZING EQUIPMENT.

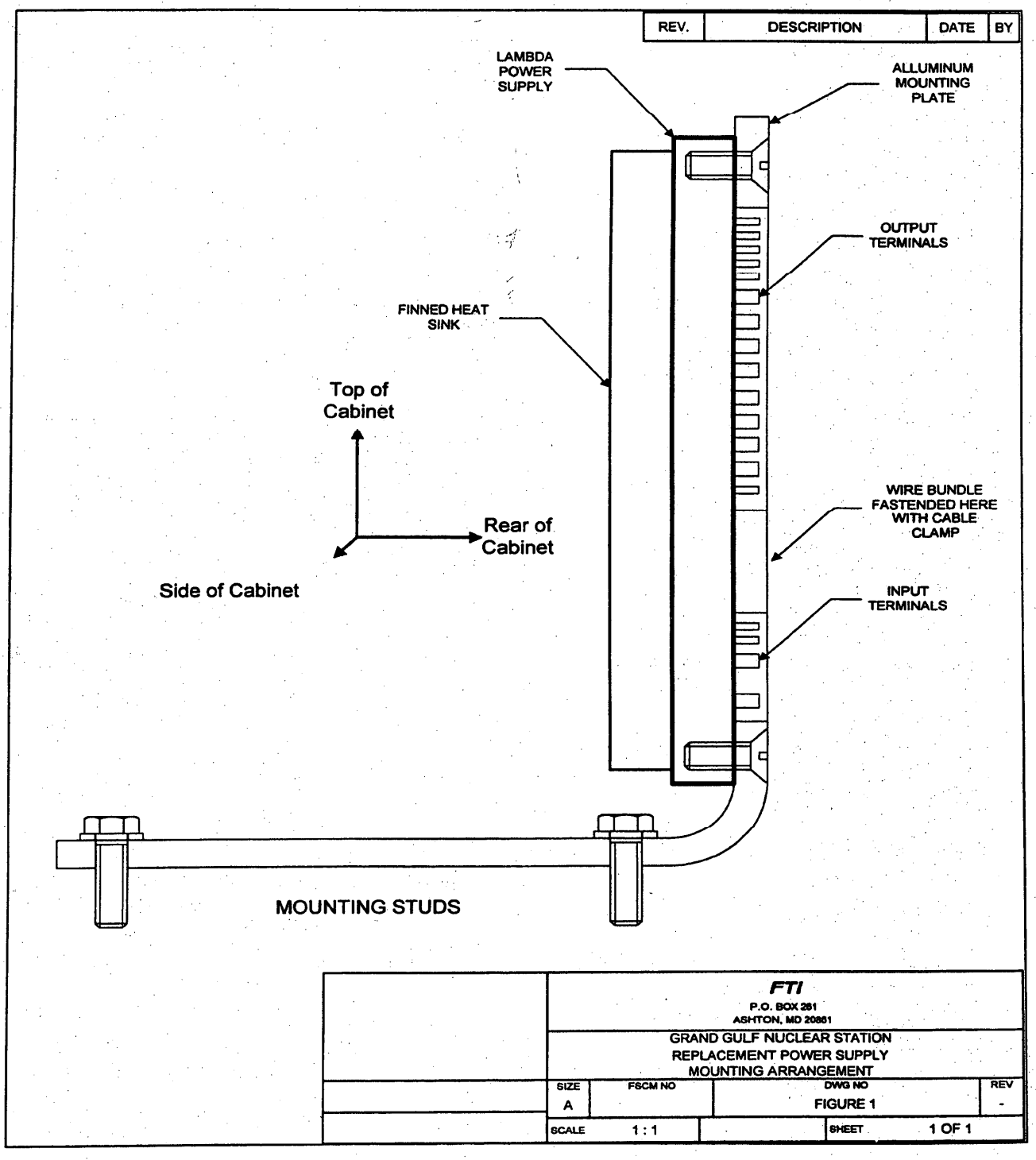


Figure 1. Correct Orientation of Power Supply

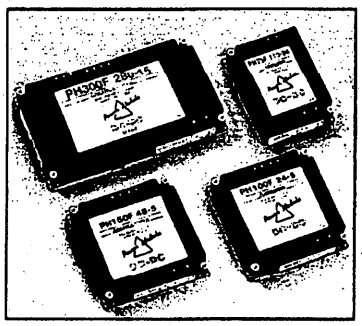
Replace screws at the TB or relay to secure the wires. Tie down all wires to existing wire bundles with cable ties and verify wires are not left in a position where they can be pinched when the Control Panel door is closed. Verify all power supply terminations are properly connected.

6. POWER SUPPLY ADJUSTMENT

Power supply voltage can be adjusted with the potentiometer mounted to the side of the power supply case. A small straight blade screwdriver should be used for this purpose. Care must be exercised to adjust the potentiometer in small increments to avoid over voltage of the power supply output. If the power supply output voltage is adjusted to be above the over voltage crowbar limit, the power supply will need to be reset by cycling input power.

Reapply power to the LSSP. Using the potentiometer, adjust the power supply for the nominal voltage (+15 Vdc or +24 Vdc) + 0.1/-0.0 Vdc at the terminal lug connection points in the LSSP. Remove power from the LSSP.

Close the Control Panel door. Reapply power to the LSSP according to the Initial Start-up procedure documented in paragraph 7.5 in the LSSP Instruction Manual.



Lambda's PH Series of full function modules offers the ability to power external monitoring signals, accommodation for N + 1 and scaleable power systems, and 90% efficiency - all at the lowest prices available.

TECHNICAL DATA

PH300F-110 Series of DC-DC Converters

Lambda Electronics Inc.
515 Broad Hollow Rd. • Melville, NY 11747
Tel: 516-694-4200 • 1-800-LAMBDA-4/5 • Fax: 516-293-0519

5/96
TDPH300F-110

Table of Contents

8/8/7/02

I. SCOPE

This Technical Data manual contains specifications and typical performance characteristics to aid in designing the power supply into an application. Due to component and manufacturing tolerances, Lambda cannot guarantee that all power supplies will produce identical performances to the characteristics enclosed. Lambda does guarantee conformance to the published specifications included below. For other information, refer to the instruction manual.

II. SPECIFICATIONS

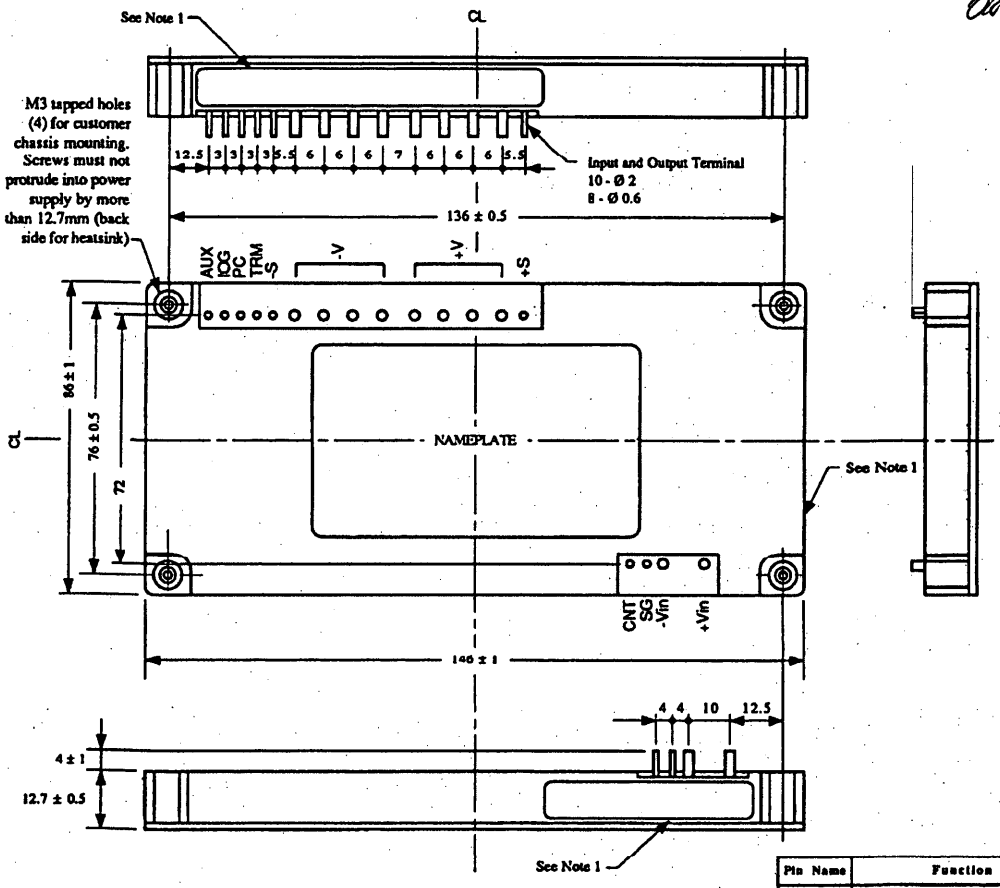
MODEL / ITEMS		PH300F-110						
		PH300F-110-2	PH300F-110-3	PH300F-110-5	PH300F-110-12	PH300F-110-15	PH300F-110-24	PH300F-110-28
Nominal Output Voltage	V	2	3	5	12	15	24	28
Maximum Output Current	A	60	60	60	25	20	12.6	10.8
Nominal Output Power	W	120	180	300	300	300	302.4	302.4
Efficiency (Typ.) *1	%	68	73	83	86	87	89	90
Input Voltage Range	-	88 - 185Vdc						
Input Current (Typ.) *1	A	1.60	2.24	3.29	3.17	3.13	3.09	3.05
Output Voltage Accuracy *1	%	±1						
Output Voltage Range *9	%	±20%		+20% to -60%				
Maximum Ripple & Noise *8	mV	100	100	100	150	150	240	280
Maximum Line Regulation *2	-	20mV	20mV	20mV	48mV	60mV	96mV	112mV
Maximum Load Regulation *3	-	40mV	40mV	40mV	96mV	120mV	192mV	224mV
Overcurrent Protection *4	A	105% - 140%						
Overvoltage Protection *5	V	165% - 240%		125% - 145%				
Remote Sensing *7	-	Possible						
Remote ON/OFF Control *7	-	Possible (Short : ON, Open : OFF)						
Parallel Operation *7	-	Possible						
Series Operation *7	-	Possible						
I.O.G. Signal *7	-	Possible (Open collector output)						
Operating Temperature	-	-20°C - +85°C (Baseplate); Ambient Temperature min. = -20°C						
Operating Humidity	-	30% - 95% RH						
Storage Temperature	-	-40°C - +85°C						
Storage Humidity	-	10% - 95% RH						
Cooling *6	-	Conduction cooled						
Temperature Coefficient	(%)	0.02%/°C						
Isolation Voltage (for 1 minute)	-	Input - Chassis : 2.5kVac, Input - Output : 3.0kVac, Output - Chassis: 500Vdc						
Isolation Resistance	-	More than 100MΩ @ 25°C and 70% RH Output-Chassis : 500Vdc						
Vibration	-	10 - 55Hz amplitude (1 minute sweep) less than 5G X, Y, Z 1 hour each						
Shock	-	Less than 20G						
Weight	-	250 g / 0.551 lbs.						
Size (W.H.D.)	-	146 x 12.7 x 86mm / 5.75" x 0.5" x 3.39"						

*1. At 110Vdc and maximum output current.
*2. 88 - 185Vdc, constant load.
*3. No load to Full load, constant input voltage.
*4. Constant current limiting with automatic recovery.
*5. Inverter shutdown method, manual reset.
*6. Heatsink has to be chosen according to the Instruction Manual.
*7. Refer to the Instruction Manual.
*8. External capacitor is required
*9. At 110Vdc input. Refer to the Instruction Manual.

8/5/7/02

Outline Drawing for the PH300F-110

- Dimensions are in inches (millimeters)



Pin Name	Function
AUX	Bias Voltage Output (secondary ref.)
POG	Inverter Good Signal
PC	Parallel Connection
TRM	Vout Adjust Pin
-S	Negative Output Voltage Sense
-V	Output Voltage Return
+V	Positive Output Voltage
+S	Positive Output Voltage Sense
CNT	Remote ON/OFF Control
SG	Signal (CNT RTN)
-Vin	Input Voltage Return
+Vin	Positive Input Voltage

Note 1 : Model name, input voltage range, Nom. output voltage and Max. output current are shown here in accordance with the specifications.

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III. TEST DATA
Steady State Data

Regulation - Line and Load, Temperature Drift

5V

1. Regulation - Line and Load

Conditions Ta : 25°C

Iout \ Vin	88Vdc	110Vdc	185Vdc	Line Regulation	
0 %	5.000 V	5.000 V	5.000 V	0 mV	0 %
50%	5.002 V	5.002 V	5.002 V	0 mV	0 %
100%	5.006 V	5.006 V	5.006 V	0 mV	0 %
Load Regulation	6 mV	6 mV	6 mV		
	0.12 %	0.12 %	0.12 %		

2. Temperature Drift

Conditions Vin : 110 Vdc
Iout : 100%

Ta	-20 °C	25 °C	85 °C	Temp. Stability
Vout	4.992 V	5.006 V	5.006 V	14mV / 0.28%

12V

1. Regulation - Line and Load

Conditions Ta : 25°C

Iout \ Vin	88Vdc	110Vdc	185Vdc	Line Regulation	
0 %	12.000 V	12.000 V	12.000 V	0 mV	0 %
50%	12.000 V	12.001 V	12.001 V	1 mV	0.01 %
100%	12.000 V	12.000 V	12.000 V	0 mV	0 %
Load Regulation	0 mV	1 mV	1 mV		
	0 %	0.01 %	0.01 %		

2. Temperature Drift

Conditions Vin : 110 Vdc
Iout : 100%

Ta	-20 °C	25 °C	85 °C	Temp. Stability
Vout	11.972 V	12.000 V	12.003 V	31mV / 0.26%

Regulation - Line and Load, Temperature Drift

24V

1. Regulation - Line and Load Conditions Ta : 25°C

Iout \ Vin	88Vdc	110Vdc	185Vdc	Line Regulation	
0 %	24.010 V	24.010 V	24.010 V	0 mV	0 %
50%	24.010 V	24.010 V	24.010 V	0 mV	0 %
100%	24.010 V	24.010 V	24.010 V	0 mV	0 %
Load Regulation	0 mV	0 mV	0 mV		
	0 %	0 %	0 %		

2. Temperature Drift Conditions Vin : 110 Vdc
Iout : 100%

Ta	-20 °C	25 °C	85 °C	Temp. Stability
Vout	23.930 V	24.010 V	24.020 V	90mV / 0.37%

Output Voltage and Ripple Voltage vs. Input Voltage

Conditions Iout : 100%
Ta : -20°C - - - -
25°C —·—
85°C ——

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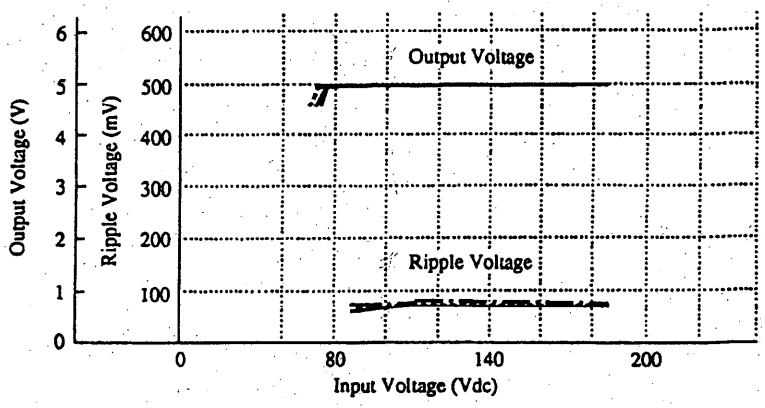
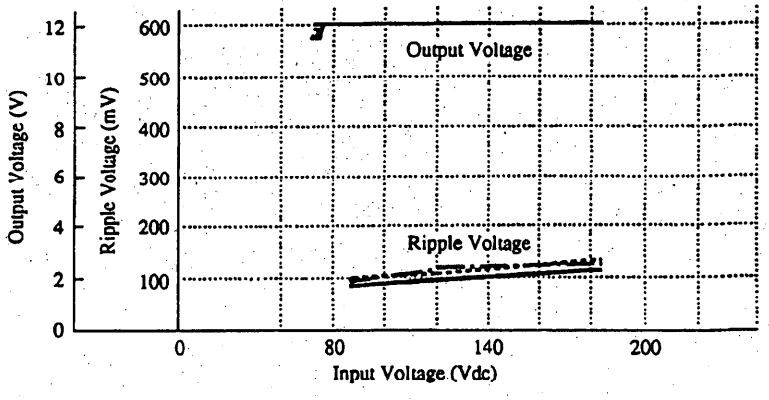
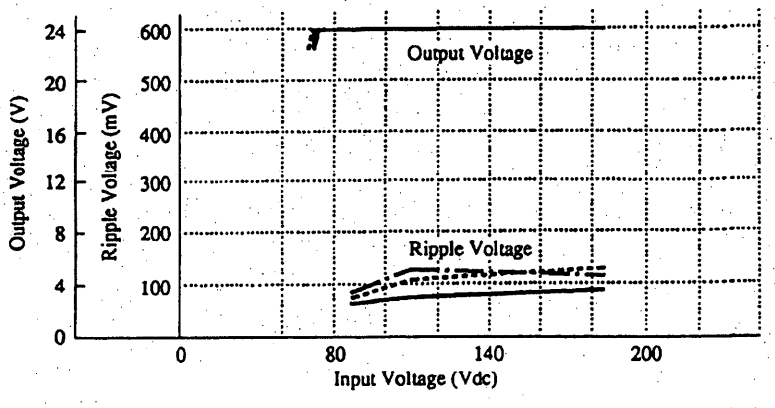
5V



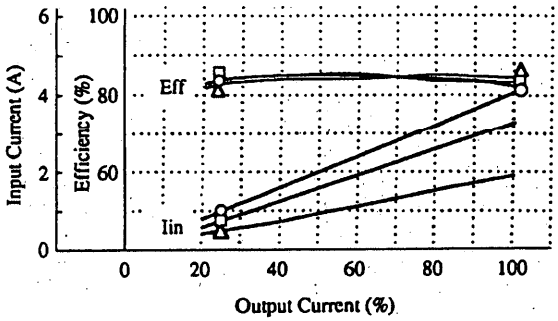
12V



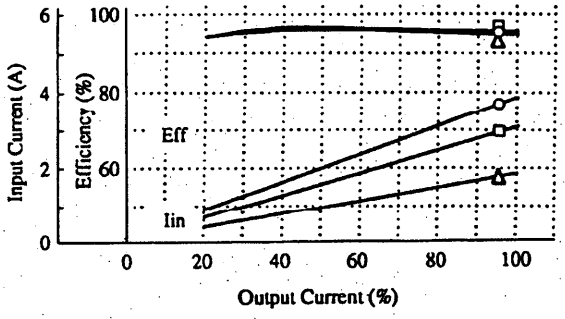
24V



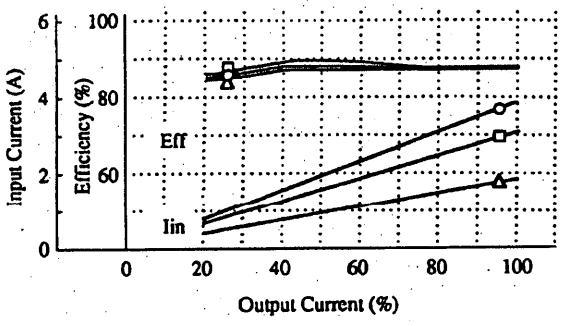
5V


Input Current (A)
Efficiency (%)
Eff
Iin
Output Current (%)
0
2
4
6
60
80
100
0
20
40
60
80
100

12V


Input Current (A)
Efficiency (%)
Eff
Iin
Output Current (%)
0
2
4
6
60
80
100
0
20
40
60
80
100

24V


Input Current (A)
Efficiency (%)
Eff
Iin
Output Current (%)
0
2
4
6
60
80
100
0
20
40
60
80
100

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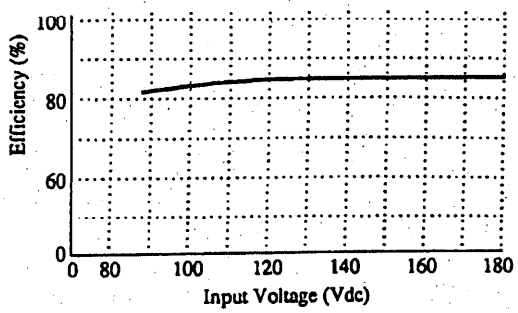
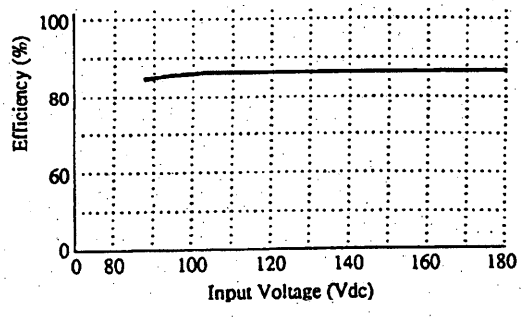
Efficiency vs. Input Voltage

Conditions Iout : 100%
Ta : 25°C

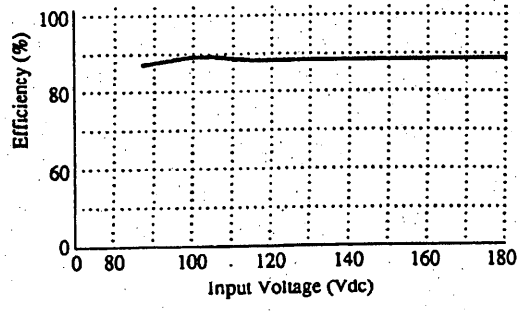
5V



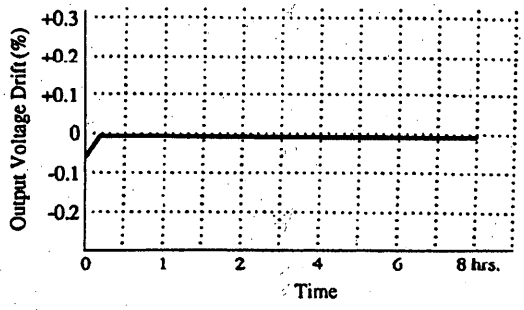
12V



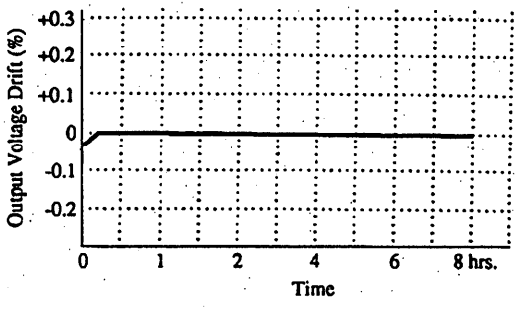
24V



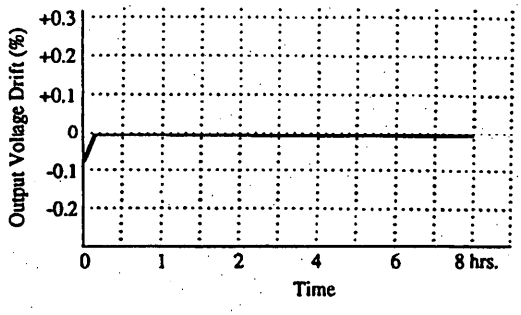
5V


+0.3
+0.2
+0.1
0
-0.1
-0.2
Output Voltage Drift (%)
0
1
2
4
6
8 hrs.
Time

12V


+0.3
+0.2
+0.1
0
-0.1
-0.2
Output Voltage Drift (%)
0
1
2
4
6
8 hrs.
Time

24V


+0.3
+0.2
+0.1
0
-0.1
-0.2
Output Voltage Drift (%)
0
1
2
4
6
8 hrs.
Time

O.C.P. Characteristics

Conditions Vin : 88Vdc ———
110Vdc - - - -
185Vdc — · —
Ta : 25°C

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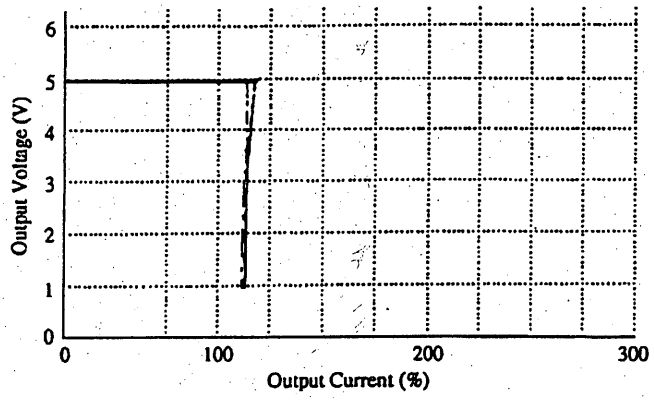
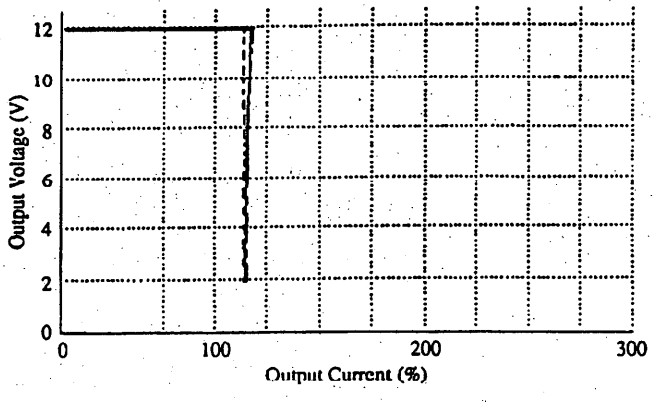
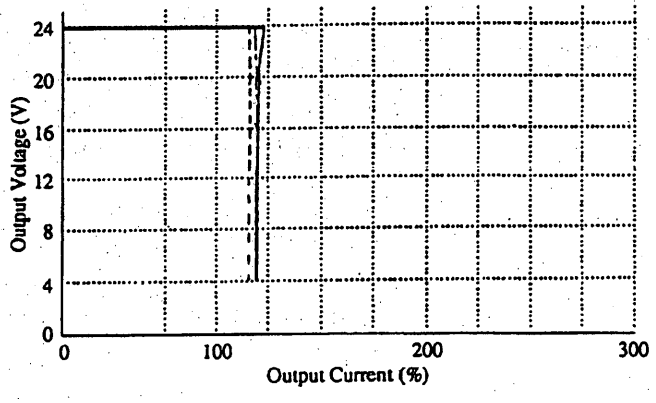
5V



12V



24V



Conditions Vin : 110Vdc
Ta : -20°C ——
25°C - - - -
85°C —·—

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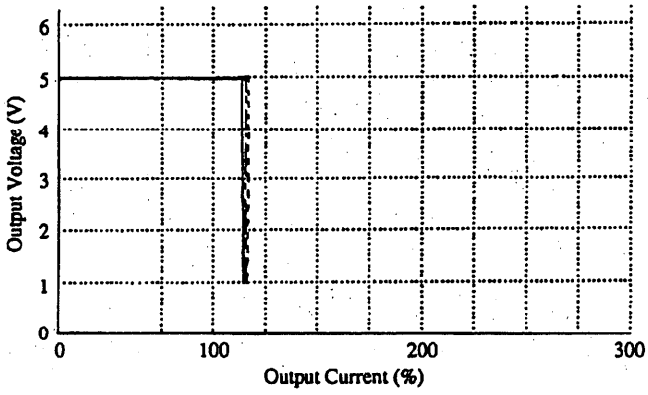
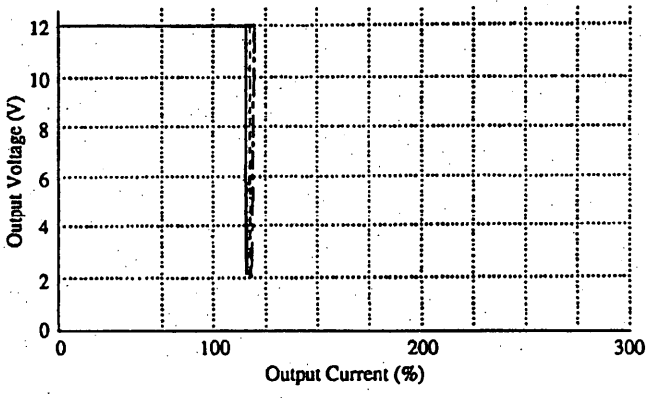
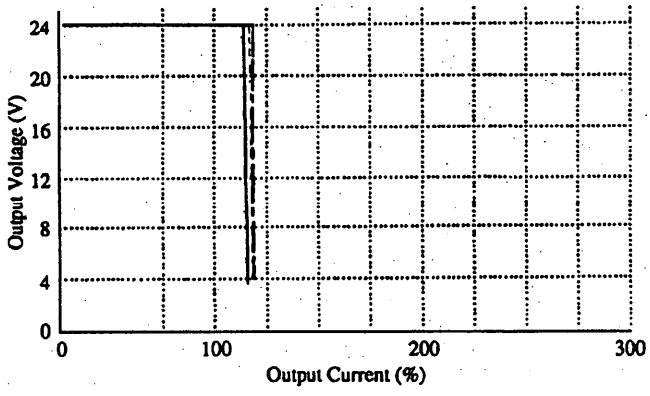
5V



12V



24V



O.V.P. Characteristics

Conditions Vin : 110Vdc
Iout : 0%
Ta : 25°C

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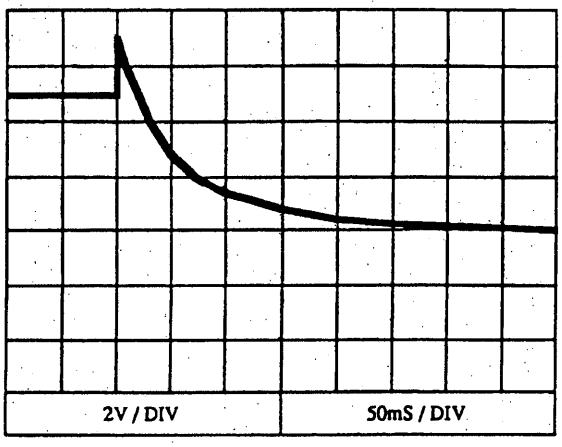
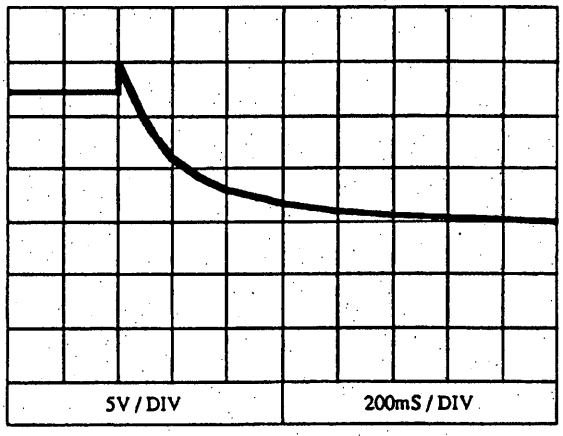
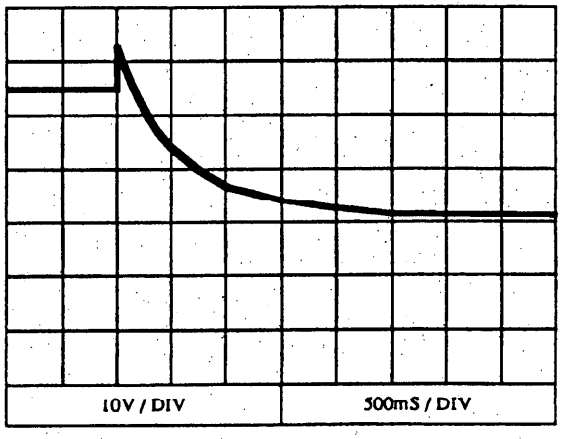
5V



12V



24V



Output Rise Characteristics

Conditions Vin : 110Vdc
Iout : 0%
Ta : 25°C

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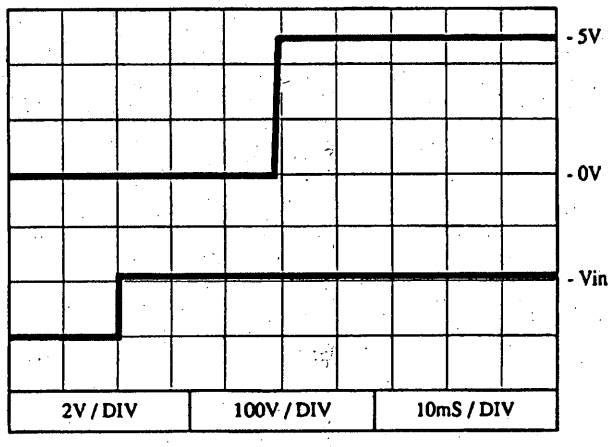
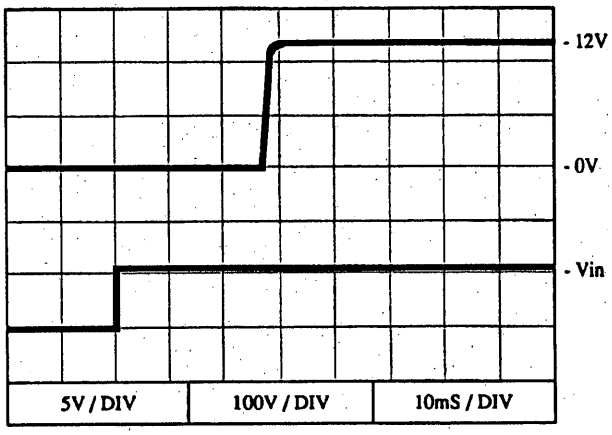
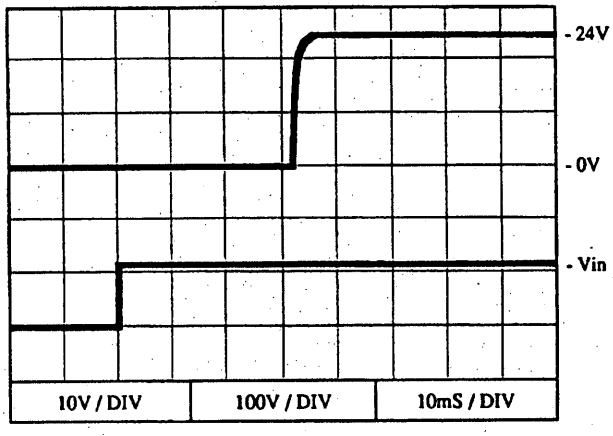
5V



12V



24V



Output Rise Characteristics

Conditions Vin : 110Vdc
Iout : 100%
Ta : 25°C

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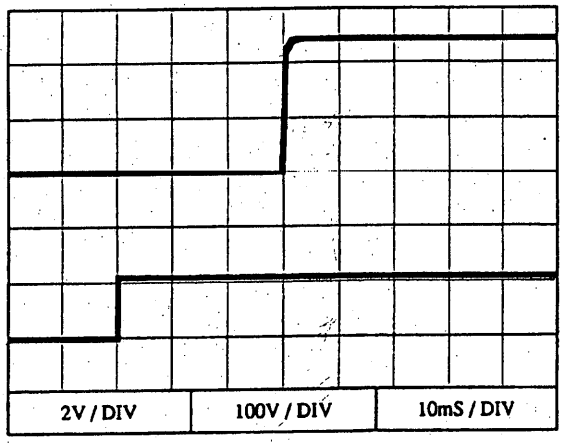
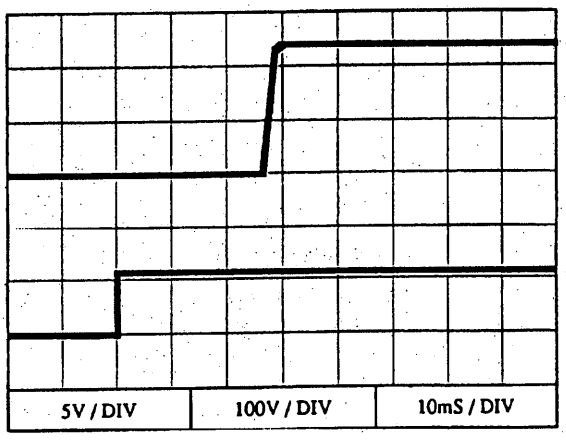
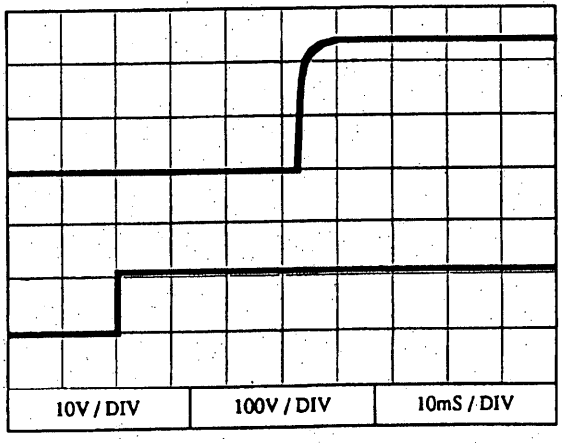
5V



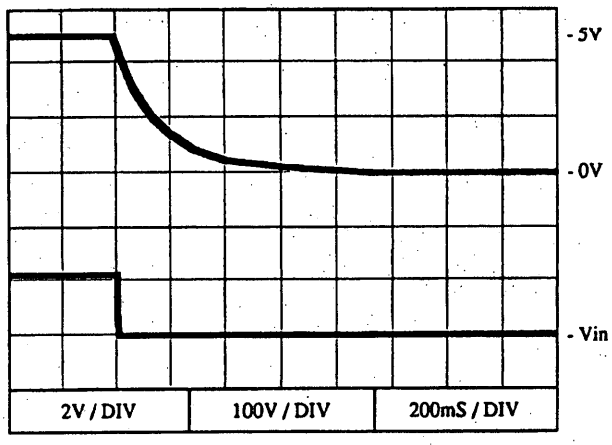
12V



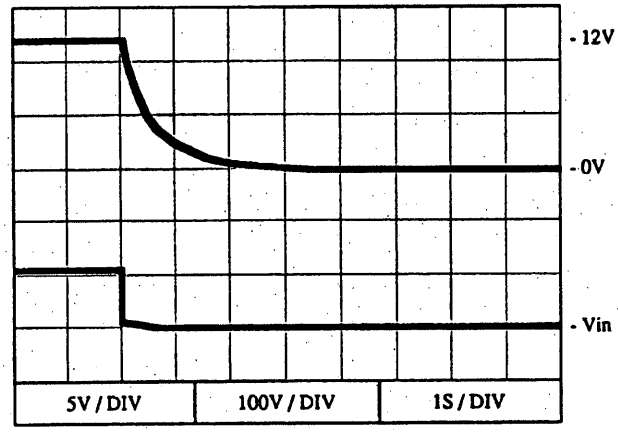
24V



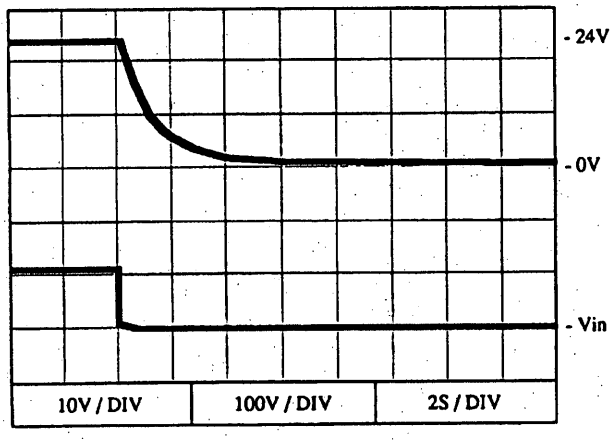
5V


- 5V
- 0V
- Vin
2V / DIV
100V / DIV
200mS / DIV

12V


- 12V
- 0V
- Vin
5V / DIV
100V / DIV
1S / DIV

24V


- 24V
- 0V
- Vin
10V / DIV
100V / DIV
2S / DIV

Output Fall Characteristics

Conditions Vin : 110Vdc
Iout : 100%
Ta : 25°C

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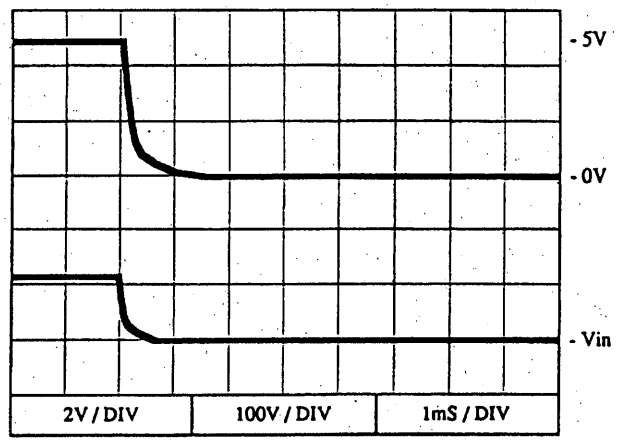
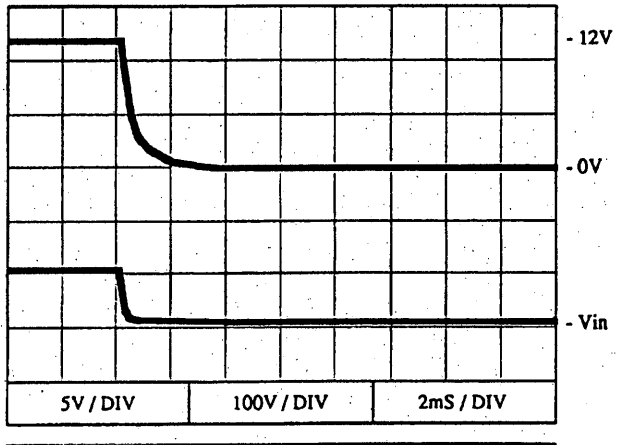
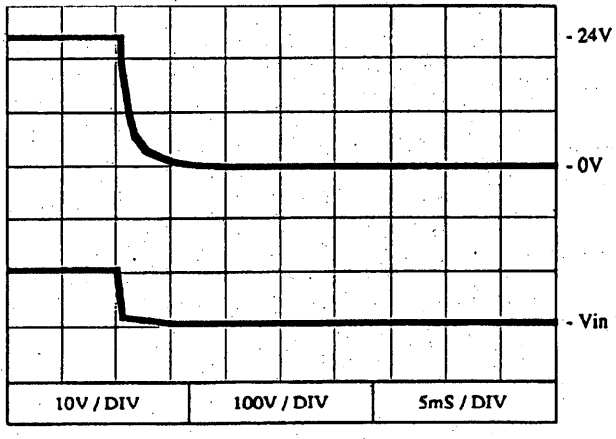
5V



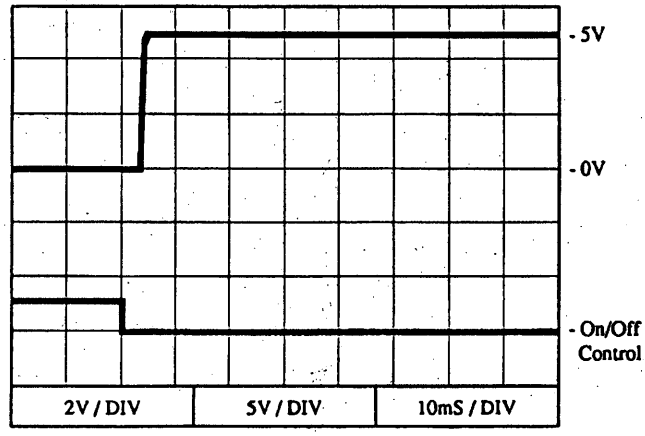
12V



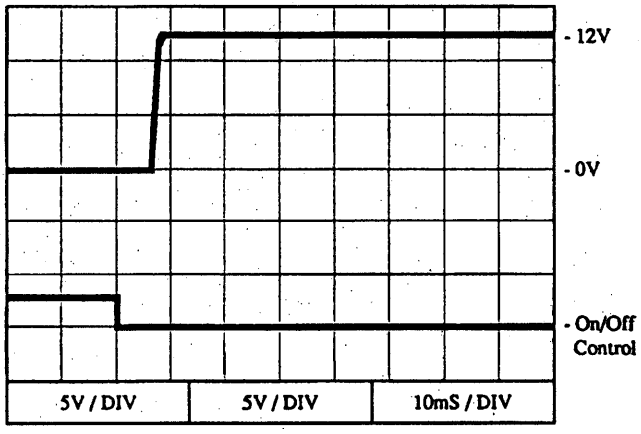
24V



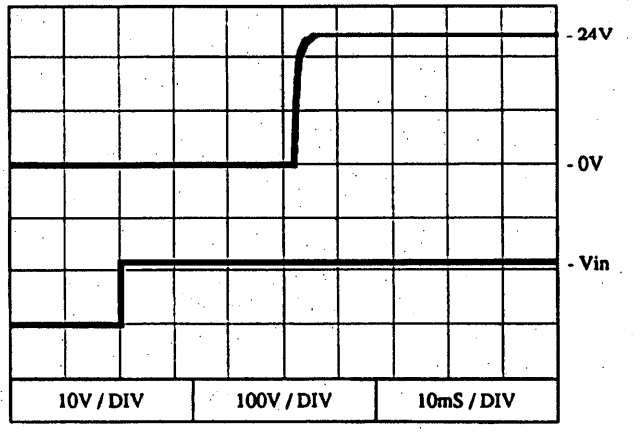
5V


- 5V
- 0V
- On/Off Control
2V / DIV
5V / DIV
10mS / DIV

12V


- 12V
- 0V
- On/Off Control
5V / DIV
5V / DIV
10mS / DIV

24V


- 24V
- 0V
- Vin
10V / DIV
100V / DIV
10mS / DIV

Output Rise Characteristics with ON/OFF Control

Conditions Vin : 110Vdc
Iout : 100%
Ta : 25°C

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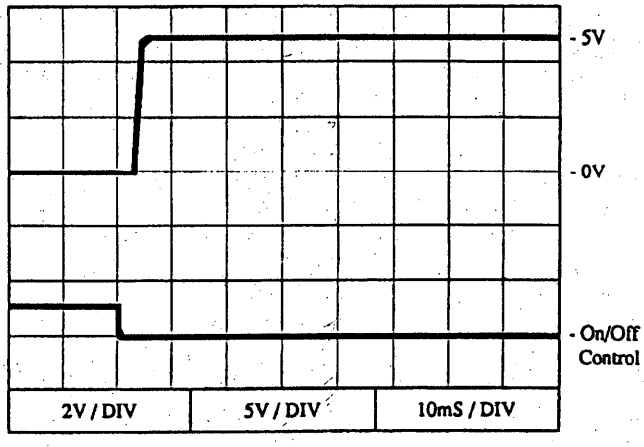
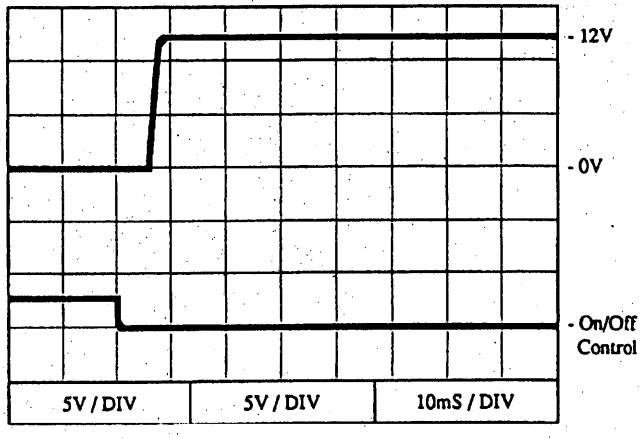
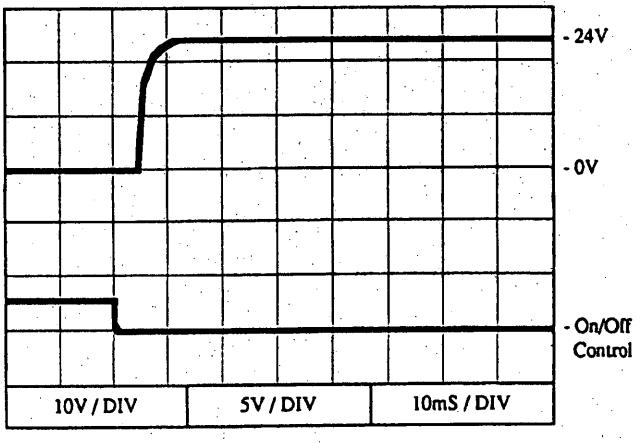
5V



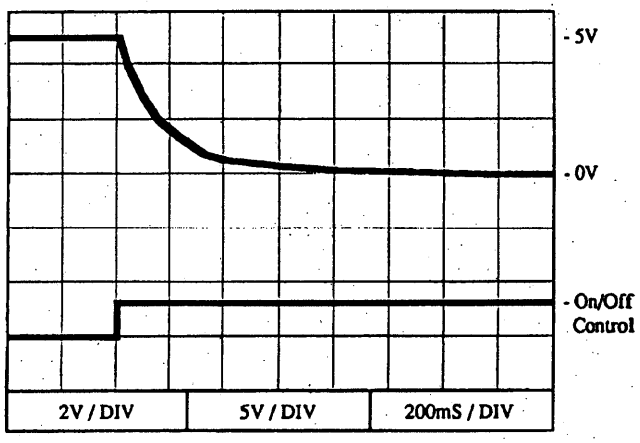
12V



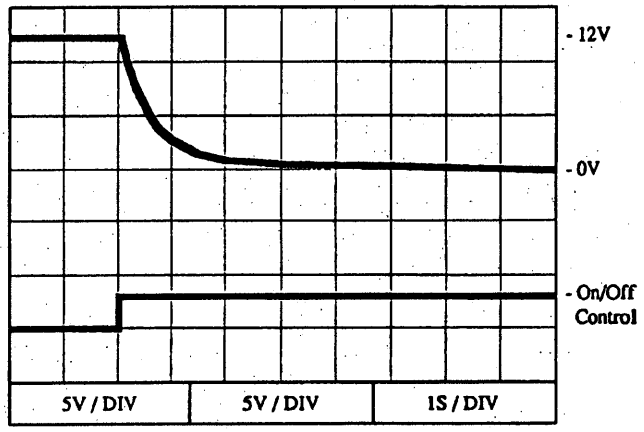
24V



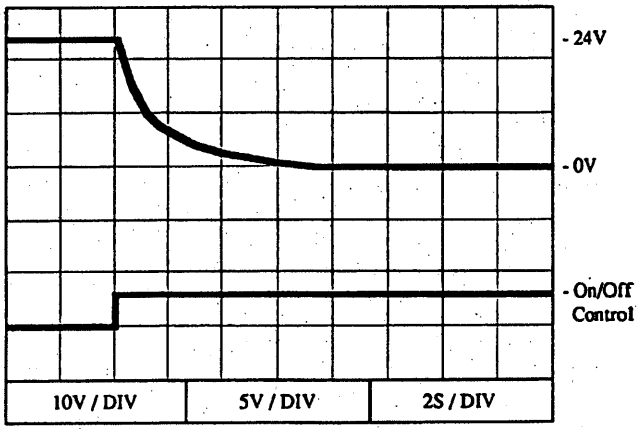
5V


- 5V
- 0V
- On/Off Control
2V / DIV
5V / DIV
200mS / DIV

12V


- 12V
- 0V
- On/Off Control
5V / DIV
5V / DIV
1S / DIV

24V


- 24V
- 0V
- On/Off Control
10V / DIV
5V / DIV
2S / DIV

Output Fall Characteristics with ON/OFF Control

Conditions Vin : 110Vdc
Iout : 100%
Ta : 25°C

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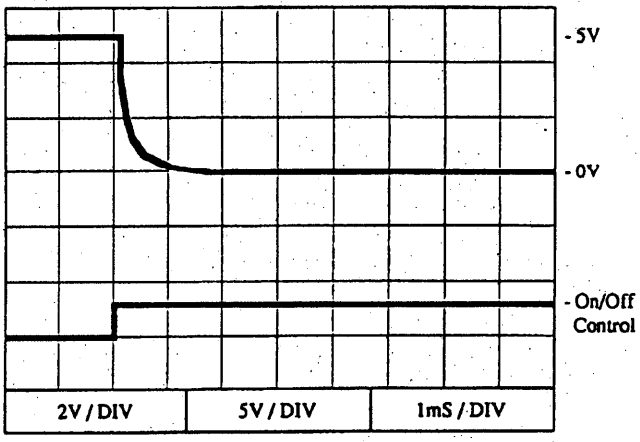
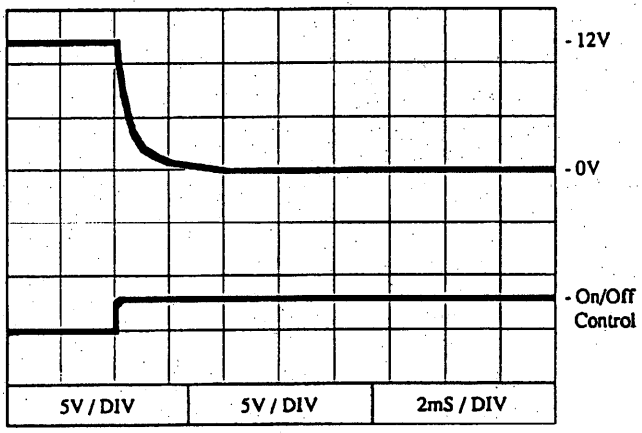
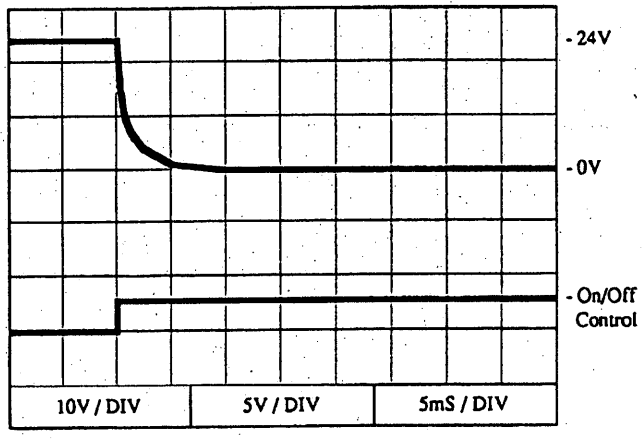
5V



12V

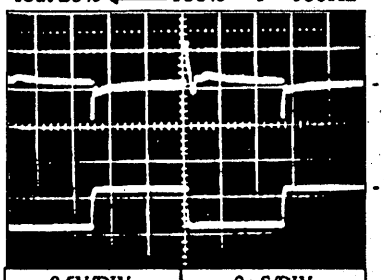


24V



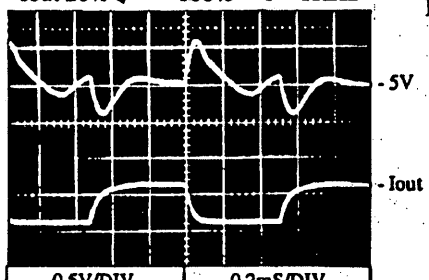
5V

Iout 20% ⇄ 100% f = 100Hz



0.5V/DIV	2mS/DIV
+12.0%	-8.0%

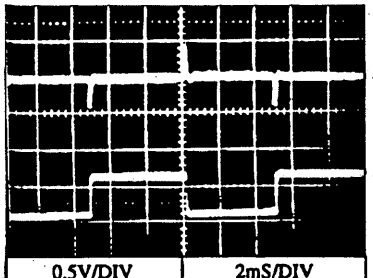
Iout 20% ⇄ 100% f = 1KHz



0.5V/DIV	0.2mS/DIV
+12.0%	-8.0%

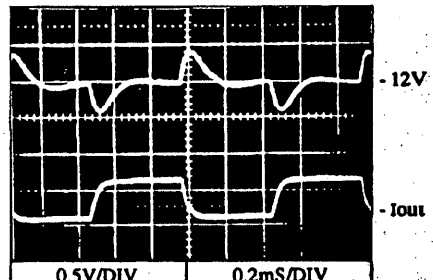
12V

Iout 20% ⇄ 100% f = 100Hz



0.5V/DIV	2mS/DIV
+3.3%	-3.8%

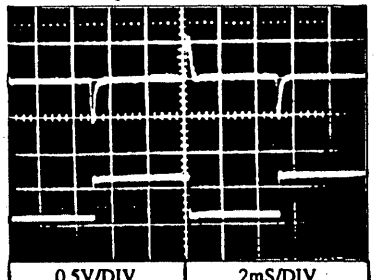
Iout 20% ⇄ 100% f = 1KHz



0.5V/DIV	0.2mS/DIV
+3.3%	-3.8%

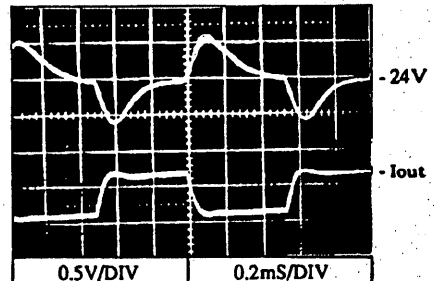
24V

Iout 20% ⇄ 100% f = 100Hz



0.5V/DIV	2mS/DIV
+2.3%	-2.3%

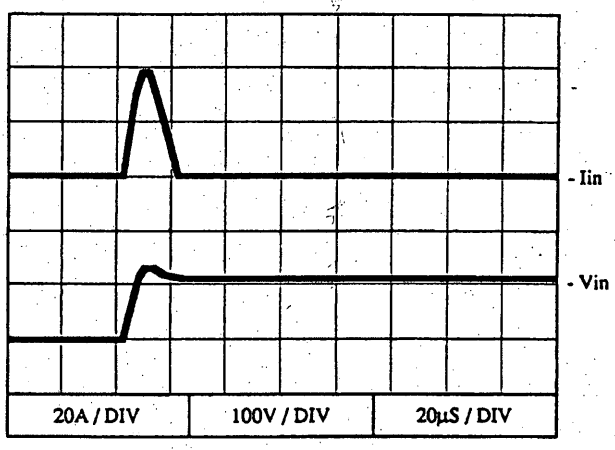
Iout 20% ⇄ 100% f = 1KHz



0.5V/DIV	0.2mS/DIV
+2.3%	-2.7%

Inrush Current Waveform

Conditions Vin : 110Vdc
Iout : 100%
Ta : 25°C

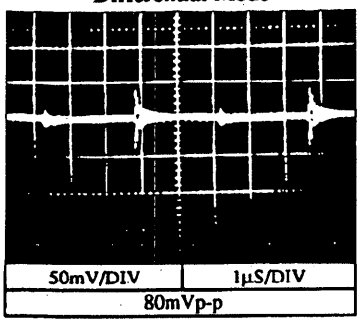


Output - Ripple, Noise

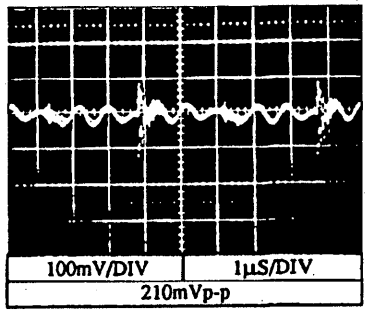
Conditions Vin : 110Vdc
Iout : 100%
Ta : 25°C

5V

Differential Mode

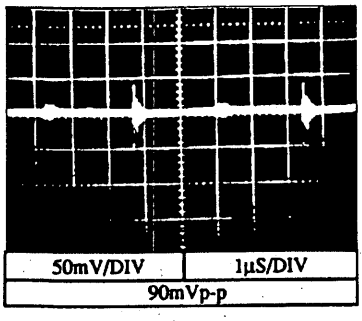


Common and Differential Mode

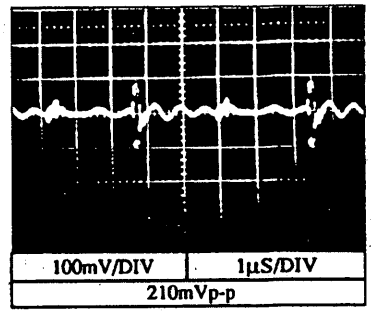


12V

Differential Mode

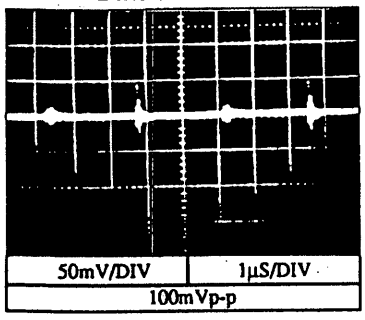


Common and Differential Mode

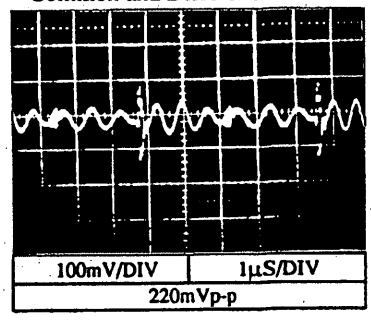


24V

Differential Mode



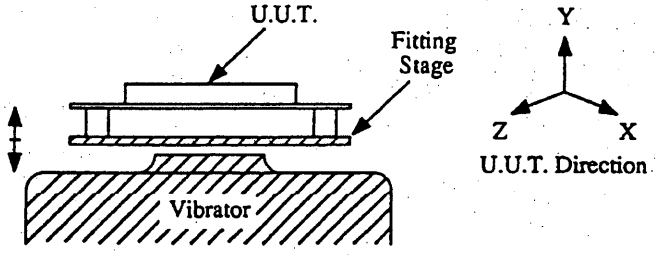
Common and Differential Mode



IV. ENVIRONMENTAL DATA
Vibration Test

1. Equipment Used - vibration test system F-400-BM-DCS-7800 from Emic Corp.
   905-FN Vibrator Generator

2. Test Setup



3. Test Conditions:
   Sweep Frequency : 10 - 55Hz
   Sweep time : 1 minute
   Acceleration : constant
   Test Time : 1 Hour each
   Tested to 5G in the X, Y, Z direction

4. Acceptance Criteria - The following parameters must remain within their specified limits in order for the test to be considered successful:

   a. Output Voltage
   b. Ripple Voltage (at nominal input and output)
   c. Mechanical condition (no breakage)

5. Test Results

PASS	FAIL
√	

Check Item		Output Voltage	Ripple Voltage	U.U.T. State
Before Test		5.000V	64mV	OK
After Test	X	5.000V	64mV	OK
	Y	5.000V	64mV	
	Z	5.000V	64mV	

Drop Test (National Safety Transit Test)

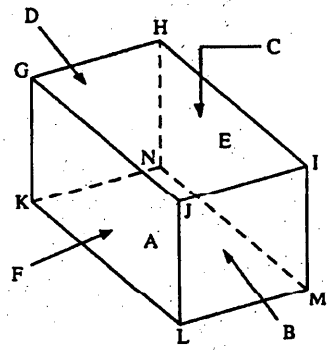
1. Scope

This procedure is performed on all Lambda power supplies weighing less than 100 lbs.

2. Test Method

The power supply is packed into a shipping container and then dropped on a bare concrete surface from a height of 24 inches for units with a gross weight between 10 and 100 lbs., and 30 inches for units with a gross weight less than 10 lbs. A total of 14 drops are made, 6 on the different faces of the unit, and 8 on each of the corners.

After each drop, the container is opened and the unit is inspected for damage. If there is no evidence of damage, the unit is re-packed and the test is continued. The results are then recorded.



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3. Test Results

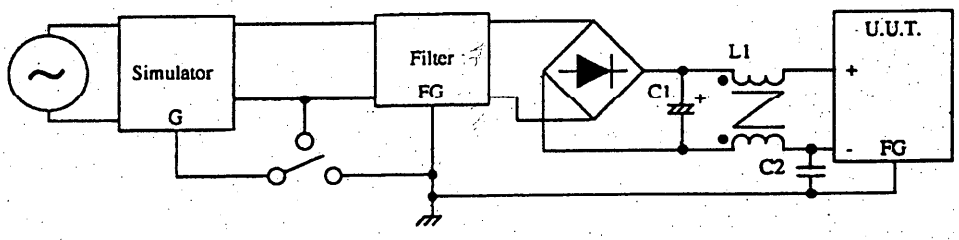
	Pass	Fail
A	√	
B	√	
C	√	
D	√	
E	√	
F	√	

	Pass	Fail
G	√	
H	√	
I	√	
J	√	
K	√	
L	√	
M	√	
N	√	

Noise Simulation Test

1. Equipment Used - Noise Simulator : INS-4420 (Noise Laboratory Co., LTD)
   Filter : MBS-1205-22 (Nemic Lambda)
   Bridge Rectifier : PGH758A (Nihon International)
   Electrolytic Capacitor C1 : 200V, 1000μF x 6
   Ceramic Capacitor C2 : 400V, 4700pF
   Choke Coil L1 : 1mH

2. Test Setup



3. Test Conditions

Input Voltage : 110Vdc
Output Voltage : 5Vdc
Output Current : 0A, 30A
Baseplate Temperature : 25°C
Pulse Width : 50ns - 1000ns
Noise Level : 0 - 2kV
Phase Shift : 0 - 360°
Polarity : +,-
MODE : NORMAL, COMMON
TRIG SELECT : LINE

4. Acceptance Criteria

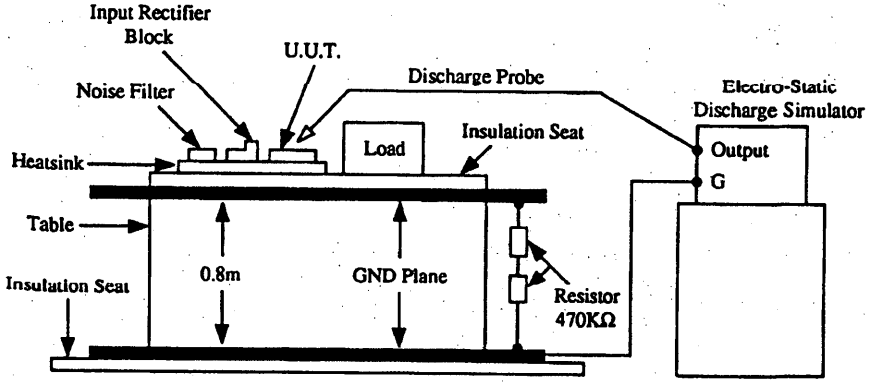
a. No damage to U.U.T.
b. No output failure
c. No other malfunction

5. Test Results

PASS	FAIL
√	

1. Equipment Used : ESS-630A (Noise Laboratory Co., LTD.)
   Discharge resistance : 330Ω
   Capacity : 150pF
   Noise Filter : MBS-1205-22 (Nemic-Lambda)

2. Test Setup and Methodology
   Verify that the output is within normal operating specifications when the testing voltage is applied to the operating U.U.T. Test voltage is applied to the input terminal, output terminal and FG (baseplate) terminal. Testing cycle is at +, - for three times each, and the applied voltage is to be gradually increased from 3KV to 15KV.



3. Test Conditions
   Ambient temperature : 25°C
   Input voltage : Rated
   Output voltage : Rated
   Output Current : Rated
   Test voltage : ± 3KV, ± 5KV, ± 10KV, ± 15KV

4. Acceptance Criteria
   a. No damage to U.U.T.
   b. No output failure
   c. No other malfunction

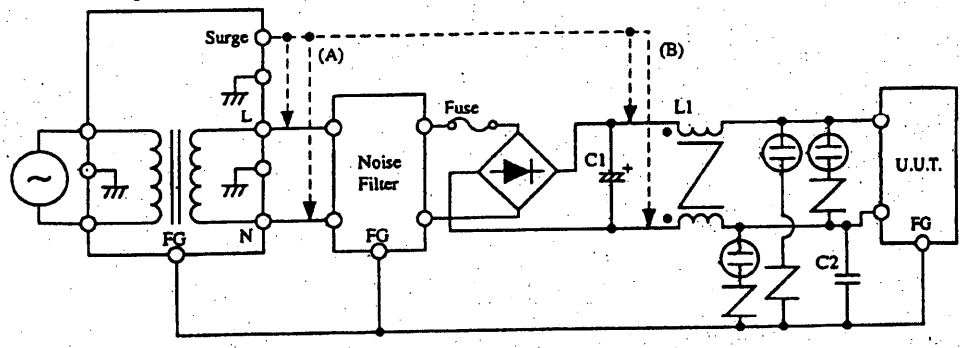
5. Test Results

PASS	FAIL
√	

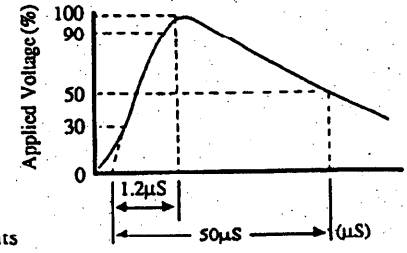
Impulse Test

1. Equipment Used : LSS-720-T54 (Noise Laboratory Co., LTD)
   Noise Filter : MBS-1205-22 (Nemic-Lambda)
   Bridge Rectifier : PGH758A (Nihon Inter.)
   Electrolytic Capacitor C1 : 200V, 1000μF x 6
   Ceramic Capacitor C2 : 400V, 4700pF
   Micro Gap Absorbers : DSA-501MA-0.6 (MMCC)
   ZNR Transient / Surge Absorbers : ERZ-C10DK471 (Matsushita Elec.)
   Choke Coil L1 : 1mH

2. Test Setup



Test voltage form



3. Test Conditions

   Input voltage : Rated
   Output voltage : Rated
   Output current : Rated
   Ambient temperature : 25°C
   Test voltage : from 0KV to 5KV in 0.5KV increments
   Test point : AC applied between FG-AC (L, N), and FG-DC (+V, -V)
   Test cycles : 3 times per test voltage
   Polarity : +,-

4. Acceptance Criteria
   a. No damage to U.U.T.
   b. No output failure
   c. No other malfunction

5. Test Results

PASS	FAIL
√	

Test Number	Test Voltage	Test Result
1	2.0KV	OK
2	5.0KV	OK

High Temperature Storage Test

1. Equipment Used : Platinous Lucifer PL-2G from Tabai Espec Corp.

2. Test Conditions

   # of U.U.T.'s : 3 units
   Ambient Temperature : 85°C
   Test Time : 96 Hours, non-operating

3. Test Setup and Methodology

   It is verified that the output is within normal operating specifications when the testing voltage is applied to the U.U.T. The unit is then put into a testing chamber, and the temperature is gradually increased from 25°C to 85°C. After a period of 96 hours at 85°C, the unit is taken out and left for 1 hour at room temperature. The output is then checked again.

4. Acceptance Criteria
   a. No damage to U.U.T.
   b. No output failure
   c. No other malfunction

5. Test Results

PASS	FAIL
√	

Check Item	No. 1		No. 2		No. 3	
	Before	After	Before	After	Before	After
Output Voltage	5.005V	5.005V	5.002V	5.001V	5.003V	5.005V
Ripple Voltage	65mV	65mV	62mV	61mV	60mV	61mV
Line Regulation	0mV	0mV	1mV	1mV	1mV	1mV
Load Regulation	5mV	5mV	6mV	6mV	5mV	5mV
Isolation Resistance	OK	OK	OK	OK	OK	OK
Withstand Voltage	OK	OK	OK	OK	OK	OK
Appearance	OK	OK	OK	OK	OK	OK

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Low Temperature Storage Test

1. Equipment Used : Platinous Lucifer PL-2G from Tabai Espec Corp.

2. Test Conditions

   # of U.U.T.'s : 3 units
   Ambient Temperature : -40°C
   Test Time : 96 Hours, non-operating

3. Test Setup and Methodology

   It is verified that the output is within normal operating specifications when the testing voltage is applied to the U.U.T. The unit is then put into a testing chamber, and the temperature is gradually decreased from 25°C to -40°C. After a period of 96 hours at -40°C, the unit is taken out and left for 1 hour at room temperature. The output is then checked again.

4. Acceptance Criteria
   a. No damage to U.U.T.
   b. No output failure
   c. No other malfunction

5. Test Results

PASS	FAIL
√	

Check Item	No. 1		No. 2		No. 3	
	Before	After	Before	After	Before	After
Output Voltage	5.005V	5.005V	5.000V	5.001V	5.003V	5.003V
Ripple Voltage	62mV	62mV	60mV	60mV	60mV	60mV
Line Regulation	0mV	0mV	0mV	0mV	1mV	1mV
Load Regulation	8mV	8mV	5mV	5mV	6mV	6mV
Isolation Resistance	OK	OK	OK	OK	OK	OK
Withstand Voltage	OK	OK	OK	OK	OK	OK
Appearance	OK	OK	OK	OK	OK	OK

Resistance to Soldering Heat Test

1. Equipment Used : Automatic dip soldering machine from Osaka Asahi Kagaku

2. Test Conditions

   # of U.U.T.'s : 1 unit
   Dip Soldering Temperature : 260°C
   Dip Time : 10 seconds
   Pre-heating Temperature : 120°C
   Pre-heating Time : 60 seconds

3. Test Setup and Methodology

   It is verified that the output is within normal operating specifications when the testing voltage is applied to the U.U.T. The unit is then put on a universal circuit board, and transfered to flax-dripping, pre-heating and soldering in the dip machine. It is then left at room temperature for one hour. The output is then checked again.

4. Acceptance Criteria
   a. No damage to U.U.T.
   b. No output failure
   c. No other malfunction

5. Test Results

PASS	FAIL
√	

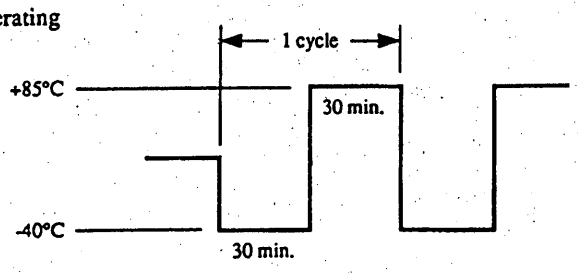
Check Item	No. 1	
	Before	After
Output Voltage	5.005V	5.004V
Ripple Voltage	60mV	60mV
Line Regulation	2mV	2mV
Load Regulation	8mV	8mV
Isolation Resistance	OK	OK
Withstand Voltage	OK	OK
Appearance	OK	OK

Thermal Shock Test

1. Equipment Used : Thermal shock chamber TSV-40 from Tabai Espec Corp.

2. Test Conditions

   # of U.U.T.'s : 5 units
   Standard : subjected to JIS C5030
   Ambient Temperature : -40°C to 85°C
   Test Time : See drawing at right
   Test Cycle : 50, 100 cycles, non-operating



3. Test Setup and Methodology

   It is verified that the output is within normal operating specifications when the testing voltage is applied to the U.U.T. The unit is then put into a testing chamber, and is tested according to the above cycle. After 50 and 100 cycles, the unit is left for 1 hour at room temperature. The output is then checked again.

4. Acceptance Criteria
   a. No damage to U.U.T.
   b. No output failure
   c. No other malfunction

5. Test Results

PASS	FAIL
√	

1. Part count reliability projection

The calculation is based on MIL-HDBK-217F Parts Count Reliability. One environment is given as applicable for a power supply. The definition of this environment is:

> Ground, Fixed - Conditions less than ideal such as installation in permanent racks with adequate cooling air and possible installation in unheated buildings; includes permanent installation of air traffic control, radar and communications facilities.

The Electronic Industry Association of Japan (EIAJ) has a technical committee for power supplies which publishes reliability data giving a combined π_Q and λ_G for use in reliability prediction.

MIL-HDBK-217F

$$MTBF = \frac{1}{\lambda equip} = \frac{1}{\sum_{j=1}^{n} Ni\,(\lambda_G)\,i\,(\pi_Q)\,i} \times 10^6 (Hours)$$

where:

$\lambda equip$: Total Equipment Failure Rate (Failure / 10^6 Hour)

λ_G : Generic Failure Rate for the 'ith Generic Part (Failure / 10^6 Hour)

π_Q : Quality Factor

Ni : Quantity of the 'ith Generic Part

n : Number of different Generic Part categories

2. Results : MTBF @ Ground, Fixed = 297,359 Hours

LAMBDA QUALITY

DEFINITION

Quality at Lambda means error-free output which meets the needs and exceeds the expectations of our internal and external customers.

IMPLEMENTATION

It is each individual's responsibility to understand his or her customer's needs and expectations and deliver products and services which achieve Lambda Quality.

LAMBDA Electronics Inc.
Lambda Group of Unitech plc

Attachment 5
to GNRO-2015/00012

LSS Vendor Information

FTI

1. Data Review Scope

Under Entergy Contract 10292342-00 FTI was tasked with reviewing legacy Grand Gulf Load Shedding Sequencing (LSS) system data to try and determine the basis for the 1% accuracy specified in the vendor manual for the LSS Undervoltage Bistable card. Specifically, FTI was asked to:

1) Review their archived data files to identify the basis for the 1% uncertainty value for the LSS Bistable card. This will include identifying the drift interval included in the 1% value and what allowance is made for temperature effect and power supply effect.

2) If no basis for the 1% accuracy value can be located, FTI will review the Vitro qualification reports and provide temperature effect and power supply effect specifications for the Bistable cards if it is contained in the qualification reports. No analysis is required if the data is not contained in these reports.

2. Background

Grand Gulf received a finding in the last INPO assessment concerning the setpoint validation calculation for the 90% (degraded voltage) setpoint. In the existing calculation, a total uncertainty is determined utilizing a 1% accuracy value, M&TE error, and bistable drift. The drift is statistically calculated based on actual calibration data history. The calculated drift value is considered conservative since it includes accuracy, M&TE, temperature effects, and power supply effects.

The System Instruction Manual For Load Shedding and Sequencing Panel, dated March 1978, paragraph 4.3.2 states "The trip point of any bistable card may be adjusted from 65% to 95% of 120 Vac by means of a multi-turn potentiometer on each card and will maintain a long term accuracy of ± 1% of initial setting". FTI interprets this to be the accuracy considering all factors including basic design tolerances, environmental factors (temperature, humidity), and component drift (not related to temperature and humidity), just based on how it is stated.

Instead of utilizing the ± 1% accuracy value stated in the system manual, Grand Gulf has utilized ± 0.2 V specified in a plant calibration procedure.

FTI

3. Findings

FTI reviewed the archived data specifically designated as being for the Grand Gulf LSS System. There is extensive data on system spare parts, modifications, and initial problems with the system when originally installed, but this doesn't help answer the setpoint validation question.

There was some factory acceptance test data for individual Bistable cards delivered as spare parts. The Bistable card is what Vitro referred to as a "Standard Card" that was designed to be used in multiple systems (as denoted by the 0423 drawing number prefix). The AC Bistable Card test procedure (TP 0423-2757, Rev A) paragraph 1.3.3 establishes a power supply baseline of 15Vdc ± 15 mV (±0.1%). Paragraph 1.3.8 adjusts the trip point to 108 ± 0.1 Vac, then paragraph 1.3.11 tests the actual trip to be 108 ± 1.2 Vac (±1.1%). Actual test result data shows the trip point to be much closer than this tolerance. The ambient temperature trip point result was 107.98 Vac or 0.02%. There is no indication on whether the tolerance value considers power supply effects or long term drift.

The system test procedure (TP 2699-1005, Rev C, dated 1-18-79) tests the set and reset points of the AC Bistable which indicate the deadband and provide some evidence of tested accuracy. Pages 14 and 15 of this procedure tests each of the Bistable cards at three input voltage values (84 Vac, 96 Vac, and 108 Vac) and verifies the trip setting and reset values. For the 96 Vac test, the trip voltage is set to 96 ± 0.05 Vac and the reset is verified to occur at 96.7 ± 0.5 Vac.

We also identified some pertinent qualification test data. Most of the qualification data was related to seismic qualification as opposed to environmental qualification. This system was originally qualified as part of a real time aging program called the Sequencer Pacer and consequently the LSS was not qualified as a complete system configured just like the Grand Gulf LSS. What that means is that there isn't any qualification data that pertains to string accuracies, drift, or combined tolerances at the system level. However, since this was a real time aging program it could be assumed that the qualification tolerances consider all effects including power supply effects and long term drift.

What does exist in the Qualification Report Load Shedding and Sequencing Panel, dated October 31, 1978, are environmental test results. Appendix A or this report is test procedure TP 2699-1005-1, Rev B. This test data is taken at ambient conditions and section 5.11 adjusts the trip point to be within ± 0.5 Vac. Appendix B contains multiple copies of TP 0423-2757, Rev A (card level test procedure) performed at different temperatures. Paragraph 1.3.7 adjusts the trip point to 108 ± 0.1 Vac. Paragraph 1.3.11 verifies the trip voltage. The stated tolerance is 108 ± 1.2 Vac (±1.1%) but the actual measurements were much closer at 107.94 Vac at 0°C (0.06%) and 107.37 Vac at 60°C (0.6%).

FTI engineers also reviewed the engineering notebooks for the engineer responsible for the system, and we expanded the data search beyond the Grand Gulf specific data and reviewed other engineering notebooks in the same time frame (33 years ago) to see if a different engineer may have performed calculations related to the Bistable card. Page 6 of Engineering Notebook #503 (Robert L. Wolkowitz0 shows calculated bistable circuit variations over temperature from 23° C to 60° C at input voltages from 80 Vac to 140 Vac. The maximum variation in the trip point across this range is 0.941%.

4. Conclusions

The data identified that relates to the Bistable setpoint accuracy is summarized in the table below. We were not able to identify specific analytical calculations related to the Bistable accuracy, or the basis for the statement in the System Instruction Manual. It was determined that the power supply accuracy is specified to be 0.1% for testing purposes, the temperature effect data is contained in the system qualification report (worst case tested 0.6%), and no data specifically related to long term drift was identified. The data is summarized below.

	Reference Accuracy	Temp Effect	Power Supply Effect	Drift
Tolerance	1.1%	NA	0.1%	NA
Measured	0.02%	0.6%	NA	NA

NA – Not Available

The test data while not specifically testing individual parameters, does provide evidence that all factors are included in the 1% stated accuracy including temperature effect, power supply effect, and drift.

Attachment 6
to GNRO-2015/00012

LSS Reset Information

GEXI 2011-00032

-----Original Message-----
From: joseph.fitzgerald@ftiengineering.com
[mailto:joseph.fitzgerald@ftiengineering.com]
Sent: Thursday, December 08, 2011 11:04 AM
To: BRYANT, TIMOTHY M
Subject: Re: another LSS bistable question

Tim:

The reset would have the same accuracy as the trip, but that isn't the number you have cited here. The deadband is basically generated by a diode forward voltage drop. The diode forward voltage drop is typically 0.7 vdc, but can vary +/- 0.5 vdc depending on the diode. However, for any given diode it will be very repeatable. So the 0.5vdc isn't an accuracy, it is a range.

Joe

Joe
>
As discussed previously, we are assuming a reference accuracy of 0.2 volts for the setpoint accuracy of the bistable trip which is conservative based on the FTI report 10090230. We also assume a drift of 1.03 volts based on a review of actual calibration data. For some reason we are also assuming a reset deadband of 0.7 +/- 0.5 volts. Would it not be reasonable to assume the same accuracy for the reset as for the trip? I should have asked this question earlier but apparently neglected to do so. Your help is greatly appreciated.
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> Thanks,
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> Tim
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