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UTLR-0020NP Part II Rev. 1,

Licensing Topical Report for Toshiba NRW-FPGA-based

Instrumentation and Control System for Safety-Related Application

(Non-Proprietary)

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UTLR-0020NP Part II Rev.1
March 2013

Topical Report

Licensing Topical Report for Toshiba NRW-FPGA-based Instrumentation and Control System for Safety-Related Application

Part II
Design Description of the Platform with Application Guide

Approved by
Instrumentation & Control Systems
Design and Engineering Dept.

Toshiba Corporation
Nuclear Energy Systems & Services Division

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Note for Acronyms and References

Acronyms and references are listed in the Acronym and Reference Part that is prepared as a separate part of this LTR.

II-1 Introduction

This part II of the Licensing Topical Report for Toshiba NRW-FPGA-based Instrumentation and Control System for Safety-Related Application (LTR) addresses Design Description of the Platform with Application Guide.

II-1.1 Background

Toshiba has extensive experience in supplying nuclear safety-grade Instrumentation and Control (I&C) systems in Japan. This experience ranges from supplying digital I&C systems, such as Power Range Neutron Monitors for individual plants, up to designing and manufacturing the world's first fully integrated digital CPU-based I&C systems for Advanced Boiling Water Reactors (ABWRs). These systems were first installed at Kashiwazaki-Kariwa Unit 6, and are in use at Kashiwazaki-Kariwa Unit 6 and Hamaoka Unit 5.

Following the installation of the CPU-based BWR digital system, Toshiba started development of I&C technology based on Non-Rewritable (NRW) Field Programmable Gate Arrays (FPGAs) and supplied the NRW-FPGA-based I&C products to Japanese Nuclear Power Plants under Toshiba's ISO 9001 program. NRW-FPGA-based products have been installed in 11 nuclear power plants including 254 NRW-FPGA-based units for non-safety-related systems, 91 units for safety-related process radiation monitors and 60 units for safety-related neutron monitoring systems.

Toshiba also has been working on establishing of a 10 CFR 50 Appendix B (Reference (a2)) Quality Assurance (QA) process to permit the use of Toshiba FPGA-based system in the US for safety-related applications in nuclear power plants. Toshiba implemented Appendix B QA processes in a phased approach as follows to ensure a smooth transition of the processes at the affected organizations.

- Original Process:
  Initial establishment of the Appendix B QA process in the system engineering organization, this process was applied to the development and the qualification of the Power Range Monitor (PRM) for a BWR-5. This process is referred as original process hereafter.
- Current Process:
  Improved the original process by extending Appendix B QA process into design organization and closer to manufacturing in which other Toshiba NRW-FPGA-based I&C products to be developed. This process is referred as current process hereafter in this LTR.

Toshiba has used the original process to develop and qualify a NRW-FPGA-based Power Range Monitor (PRM) for a BWR-5.

After the development of the PRM, Toshiba was selected as the Engineering, Procurement, and Construction (EPC) Contractor for two new Advanced Boiling Water Reactors (ABWRs) to be constructed at the South Texas Project (STP) site. South Texas Project – Nuclear Operating Company (STPNOC) selected the NRW-FPGA-based systems for the Reactor Trip and Isolation System (RTIS) and the Neutron Monitoring System (NMS).

STPNOC elected to license the NRW-FPGA platform using the Design Acceptance Criteria (DAC) inspection process. Key platform design information regarding platform independence, determinism, diversity, redundancy, and simplicity is included in the STP 3&4 COL and has been reviewed by USNRC Staff and the Advisory Committee for Reactor Safeguards (ACRS).

In April 2011, the schedule for procurement and engineering activities for the STP 3&4 project including the post-COL DAC Inspection activities has been extended and is no longer predictable. COL related activities continue.

Toshiba desires the USNRC platform review to continue, so this LTR has been drafted for submittal. This LTR consists of the following five Parts and Acronym and Reference Part. Another Part VI will be submitted when the qualification of the OPRM is completed.

Part I describes software lifecycle and development processes.

Part II describes design description of the platform with application guide.

Part III describes the qualification results of the PRM except the OPRM.

Part IV describes the compliance to the Codes and Standards.

Part V is V&V report of the PRM (not including OPRM).

Acronym and Reference Part lists all the acronyms and references used in the all Parts except Part V of the LTR. Part V has its own acronym and reference list because it is existing PRM V&V Report.

In the near future, Part VI of the LTR will be submitted. The part VI is V&V report of the OPRM.

This is Part II of the LTR.

II-1.2 Purpose

The purpose of Part II of the LTR is to describe the design features and the application guide of Toshiba NRW-FPGA-based Safety-Related I&C Systems

II-1.3 Scope

This report is being submitted to the USNRC for review and approval of Toshiba NRW-FPGA-based Safety-Related Systems as platform.

The NRW-FPGA-based systems have been implemented on several different plant systems, as described in Section I-1.1 in this LTR. The following systems are provided as examples to describe the Toshiba NRW-FPGA-based Safety-Related Systems for qualification:

- Power Range Monitor (PRM) for BWR-5
- Oscillation Power Range Monitor (OPRM) for ABWR.

The Application Guide in this LTR also describes the adaptation of these systems to other types of boiling water reactors, including BWR-3, -4, -5, -6, and ABWR.

In addition, the Toshiba NRW-FPGA-based systems can be applied to several other safety-related systems. Included in this LTR are the descriptions of the:

- Reactor Protection System (RPS)
- Main Steam Isolation Systems, combined with RPS functions into a single Reactor Trip and Isolation System (RTIS) in the ABWR DCD (Reference (a49))
- Suppression Pool Temperature Monitoring (SPTM) (also part of the RTIS)
- Startup Range Neutron Monitoring System (SRNM)

The Part II of this LTR describes the platform design description and design principles for the systems listed above. This Part II of this LTR also provides the application guide of the systems listed above. This Part II includes the following information:

- Section II-1 provides introductory material like the report purpose and scope,
- Section II-2 provides descriptions of the platform and its application systems.
- Appendix II-A provides the application guide for various applications
  Toshiba believes that the Application Guide should be considered as part of the SER.
- Appendix II-B provides the Module Summary Descriptions (MSDs) of the modules used in the platform.

II-2 FPGA System Description

II-2.1 FPGA Platform

II-2.1.1 FPGAs

An FPGA is a type of integrated circuit that can be programmed. The FPGA incorporates thousands of logic cells linked by one-time programmable connections that logically interconnect cells to meet different function requirements. Logic cells are Register cells (R-cells) and Combinatorial cells (C-cells) in the FPGA Toshiba uses. In addition to logic cells, other programmable elements of an FPGA are input and output (I/O) blocks, which serve as the interface between internal signal lines and the chip's external pins, and interconnects, which route I/O signals to appropriate destinations. The FPGA chosen by Toshiba can only implement digital logic.

In this section and the following sections, how the FPGAs are used and configured to build the NRW-FPGA-based Safety-Related I&C Systems is described, taking the PRM system as an example.

The NRW-FPGA Safety-Related I&C Systems are based on pure logic implementations of the algorithms. Toshiba does not include a microprocessor emulator or traditional software. There is no operating system. The software issues associated with multi-tasking, interrupts, serial execution, semaphores, and other software issues are eliminated. Toshiba builds custom design logic, built solely from function blocks Toshiba built under this software program, to implement these systems.

Figure II-2-1 shows the example of PRM system and illustrates the architecture of the NRW-FPGA-based platform. A PRM system consists of the LPRM, LPRM/APRM, and FLOW units. Each unit contains a defined set of modules.

Figure II-2-1 includes example of the LPRM module, which illustrate how a module contains electronics and one or more FPGAs that implement logic cells. The FPGA logic is comprised of combinations and connections of software elements called Functional Elements (FEs). Discrete logic cells are captured in FEs, as shown at the bottom of Figure II-2-1.

The module supplier, under their ISO 9001 QA program, has designed, verified, and registered all standard, reusable FEs. The FEs are treated as Commercial-off-the-Shelf (COTS) software,

registered in the FE library, and controlled by the module supplier. In the case that the design changes are required to FPGA-based safety related system, NICSD shall evaluate the contents of each design change to determine whether new development of FEs are necessary. If new FE development is necessary as the result of design change evaluation, NICSD instructs the module supplier to develop new FEs, and evaluate the new FEs. The evaluation processes for the Fes under the NICSD CGD process is described in Section I-3.3.2.5 of this LTR.

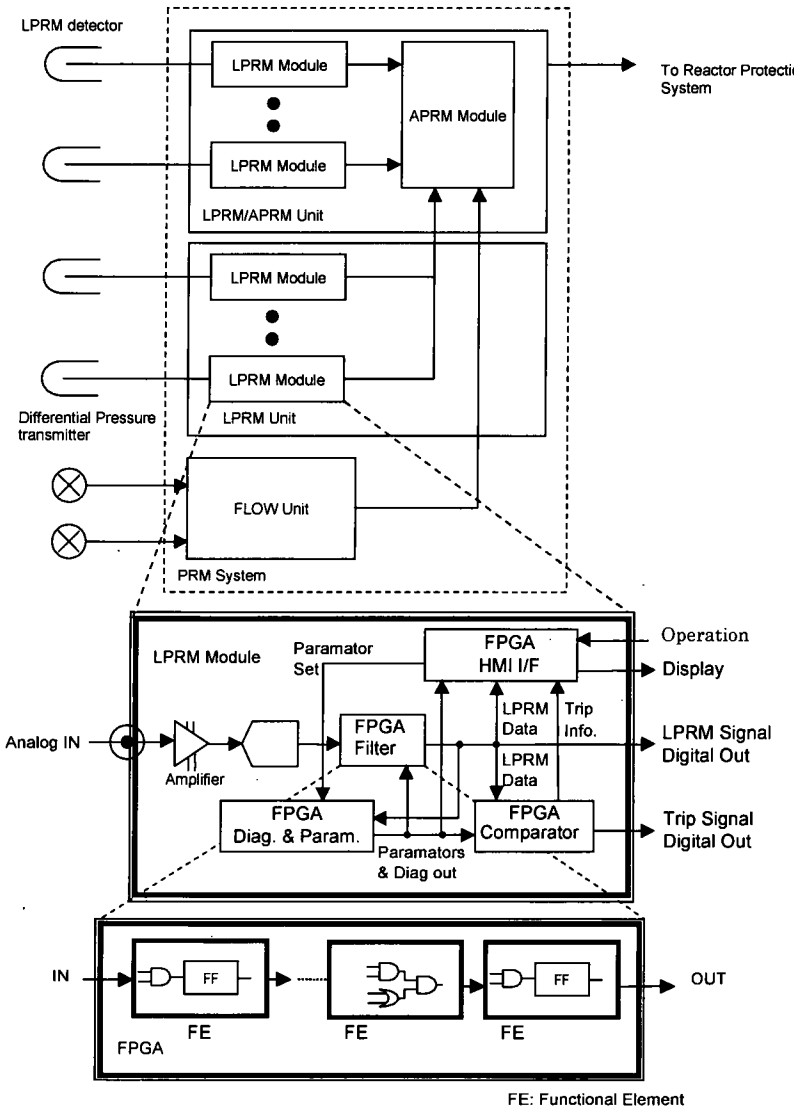


Figure II-2-1 Architecture of FPGA-Based System (Example of PRM System)

II-2.1.2 Modules

Each module consists of one or more printed circuit boards, on which the FPGAs and other circuitry are mounted, and a front panel. Some modules require two printed circuit boards, including a small printed circuit board for the Human Machine Interface (HMI) on each module's front panel. The purpose of the front panel is to fix circuit boards to the unit and to provide mounting for the HMI. The front panel HMI provides a flat, front surface for discrete Light Emitting Diodes (LEDs) for status, numeric LEDs for values, and dedicated function pushbutton switches. The panel also provides captive screws, to ensure that the printed circuit boards remain in the unit and operable through seismic events. Analog and digital components, including the FPGA chips, are soldered to the printed circuit boards. The module configuration and module list for typical applications are described in Section II-2.2.1.4 and Section II-2.2.2.4.

II-2.1.3 Units

Figure II-2-2 shows the LPRM/APRM unit. The unit is a chassis that has front slots and back slots to mount modules. Each unit consists of several modules. There is a vertical middle plane between the front and back slots in each unit. This plane consists of two circuit boards. These circuit boards provide backplanes for the front and rear modules. Modules plug into the backplanes using connectors. Once a module is plugged into the appropriate connector, it exchanges data with other modules in the unit, connects to other units and any external field equipment, and is powered.

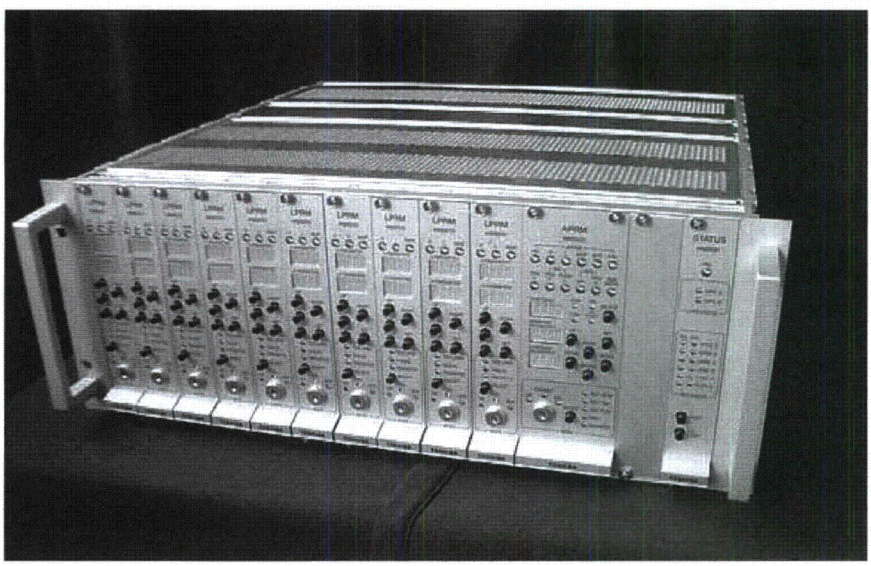


Figure II-2-2 Example of LPRM/APRM Unit

II-2.1.4 Communication

II-2.1.4.1 Communication between FPGAs

Data is transferred between FPGAs over serial and parallel communication links. For serial communication between FPGAs on a module, the design uses a clock, a data stream signal, and a synchronizing signal. For parallel data communication, the design uses a clocked transfer. As part of each data transfer, the logic sends all newly computed data and a completion signal. Failure of the completion signal to change state would result in the receiving FPGA declaring the transmitting FPGA failed. This signal is used to send data from the originating module to the destination module.

II-2.1.4.2 Communication between Modules on Middle Plane

The modules mounted in a same unit communicate over copper connections printed on the two middle backplanes. For these transmissions, three-wire electrical communication links are used. In the three-wire copper links, the first line conveys the data, the second line conveys the clock signal, and the third line is a load pulse that marks the end of the frame. In the copper lines, the data are transmitted as Complementary Metal Oxide Semiconductor (CMOS) level signals on the three associated copper lines, and the data are transmitted over serial communication links.

The middle plane also provides separate three-wire electrical communication links for each analog input or output modules. The middle plane provides hardwired discrete input or output wirings for discrete input and/or output modules. The three-wire electrical communication links and the hardwired discrete input or output wirings are configured in accordance with the configuration of IO modules in each unit.

II-2.1.4.3 Communication on Fiber Optic Link between Units

Fiber optic serial link is used for the communication between the units.

To detect failures, the fiber optic link is always operating, using a clock generated on each module. The data link uses Manchester encoding to send zeros and ones. Each message includes parity, which makes it very unlikely that silent failure would remain undetected by the logic, and Cyclic Redundancy Check (CRC) which detects data corruption.

When data needs to be transferred, a special pattern is sent to indicate the start of a data packet. The fixed length data packet is sent.

The transmitting module is configured to send all required data from the unit to external equipment. The serial communication link to the outside world is electrically isolated using uni-directional fiber optic communication. The fiber optic cables provide the required electrical isolation. The fiber optic transmitter provides the required communication isolation, making it impossible for external devices to send data back to the unit and adversely affect safety-related functions. These ports comply with the recommendations made in IEEE Std 7-4.3.2-2003 (Reference (a30)), Annex E.

II-2.1.4.4 Intradivision communication

Intradivision communication means the data transfer among the units within the same division. All Toshiba FPGA based Safety-Related Application has this communication. The communication utilizes uni-directional fiber optic serial data link and communication methods described in the previous section II-2.1.4.3 to comply with ISG-04 (reference (a22)). The compliance table is attached in Section IV-5 in this LTR. Discussion of communication independence is provided in Section II-2.2.3.2.2.

II-2.1.4.5 Interdivision communication

Interdivision communication means the data transfer among the units in different divisions. RTIS has this communication, but NMS that includes SRNM and PRM does not have this communication. The communication utilizes uni-directional fiber optic serial data link and communication methods described in the previous section II-2.1.4.3 to comply with ISG-04 (Reference (a22)). The compliance table is attached in Section IV-5 of this LTR. For communication independence discussion, see section II-2.2.3.2.2.

The interdivision communication in the RTIS communicates only discrete trip status for votes to trip across divisional boundaries, and has no engineering unit data between divisions.

II-2.1.5 FPGA Design Principles

Normally, a set of coding guidelines are written to reduce risk and facilitate development of consistent code for software development. For Toshiba's FPGA-based systems, the module supplier has developed a set of rules and guidance for designing logic and writing VHDL code for the FPGAs.

This section describes the general rules and considerations followed by the design engineers of the module supplier. In addition, this section describes the measures taken by the module

supplier to reduce the risk of inappropriate or incorrect system operation. This section also identifies exemptions that may be necessary in FPGA design and requirements for management approval of such exemptions.

II-2.1.5.1 General Rules

The following bulleted items summarize the design rules:

- Each FPGA is partitioned based on module functionality requirements and the ability to verify and validate the FPGA functionality.
- Design language of FPGA logic is VHDL as defined in IEEE Std 1076-2000 (Reference (a40)).
- FPGA is designed for synchronous operation.
- FPGA logic is designed by combining verified Functional Elements (FEs).
- All signal paths in each Functional Element are completely tested.
- If required, the FPGA design can include test input and output pins for verification.
- The internal clear signal of the FPGA is asynchronous. The internal clear signal is used for power on reset of the FPGA. Any adverse effect from an asynchronous reset is evaluated as part of the design and any required, appropriate countermeasures are incorporated.
- Antifuse FPGA architecture that is non-volatile and non-rewriteable is used.
- The structure of connections of FEs in an FPGA design is retained. Toshiba allows the logic synthesis program to optimize the FEs prior to test. Once optimized and successfully tested, the FE contents are fixed and not allowed to change. As a general rule, Toshiba does not allow the logic synthesis program to optimize the connections of FEs into an FPGA. However, if the module supplier decides to use optimization, then the optimized connections will be reviewed thoroughly.

II-2.1.5.2 General Considerations

The design engineer of the module supplier compares the cell patterns generated by the software tools against those expected based on interconnections of the FEs. Since this is important for verification and validation efforts, all optimization of interconnected FEs in the software tools is disabled.

The design engineers use simulation tools to verify that the FPGA logic works correctly, using

test vectors written by the engineers of the module supplier. The test vectors are designed to verify the FPGA logic works as intended. The test cases are added to ensure that all logic connections are exercised in their transitions from logic zero to logic one state, and from logic one to logic zero state. Functional test cases are added to the test vector as the design engineer deems necessary. The test vectors include both the patterns to be applied and the expected state. After the source code and logic are verified, the design engineer uses the software tools to create the fuse map and embed the fuse map into an FPGA. The same test vectors are used to validate the hardware design.

(1) Testability, Feedback Loop and State Machine

If feedback is required to make the logic in an FPGA work correctly, the design engineer of the module supplier routes the feedback loops external to the FPGA. By so doing, the testability of the FPGA is increased, since one can now set the FPGA state with a simple sequence, rather than having to go through many test vectors to achieve a given state. The other simplifying requirement is that state machines are used only when necessary and the states are clearly defined by the combination of the signals.

An example of an exception to these requirements is in the low pass filter for the Local Power Range Monitor module, where the filter requires so much feedback that there are not sufficient pins on the FPGA to support external feedback loops. Therefore, the feedback has to be performed within the FPGA. A design engineer of the module supplier functionally tests the low pass filter's operation by inputting data values into the logic and comparing the output values to the expected test vector values and verifying that they match.

(2) FPGA Resource

Microsemi states that 100% of the resources in the SX-A family FPGA can be used, including all of the input/output pins. The designer of the module supplier is still required to pay close attention to the percent utilization of various logic cells in an FPGA. The cell use and clock rates indicate an appropriately conservative design philosophy. Conservatively, Toshiba does not intend to make use of every cell in the FPGA, but leaves cells for future expansion and for correcting any design errors found during review and test.

(3) Word Size

The Toshiba FPGA design has no fixed requirements for word size. Rather, design engineers of the module supplier evaluate the mathematical functions required, and

determine the appropriate number of bits required to maintain the specified device accuracy. Thus, the low pass filter on the LPRM module stores twelve-bit quantities, since that is the resolution produced by the analog-to-digital converter. When the Finite Impulse Response (FIR) filter operates, it produces mathematical results in scaled, fixed point integer arithmetic as needed for accuracy. All FPGA logic works in fixed-point integer mode. Fractional bits are added to and removed from the design as necessary for the required mathematical accuracy.

(4) FPGA Interface Design

The design engineers of the module supplier design the FPGAs on a given module based on defined time constraints for the module and between FPGAs specified in a Module Design Specification. No matter how many FPGAs operate in series, the FPGA interface design must ensure that the module provides data to the next module as specified in the Module Design Specification.

If the input to the FPGA is provided over a communication link from another FPGA-based module, the FPGA can start processing without the data, but it will detect that data is not available and generate a fail signal. When an FPGA is intended to receive data from another FPGA on the module, engineers of the module supplier will design the FPGA so that the FPGA starts processing only when data is available.

II-2.1.5.3 Timing

Clocked synchronous design is performed in order to avoid timing errors due to glitches (as described later in Section II-2.1.5.4), or other timing issues. The mechanisms that create timing errors and reasons why Toshiba's rules eliminate timing errors are explained below. Engineers of the module supplier evaluate all FE and FPGA timing by design or simulation using FPGA simulation tool.

In logic design, sequential logic can be either asynchronous or synchronous. The asynchronous class describes circuits in which the application of an input control signal propagates through the logic immediately, with no clock synchronization, and with the possibility of responding incorrectly to transient signals. In the synchronous class, changes of state occur only at selected times, controlled by a clock signal. In the logic design of FPGAs, designers may generally use two types of FEs: synchronous logic with flip-flops (FFs) and pure asynchronous logic with combinatorial gates and no memory (no FFs).

Synchronous logic design is less sensitive to certain hazard conditions, whereas asynchronous

circuits are more likely to have issues related to timing and metastability. In addition, when asynchronous data is synchronized by a clocked flip-flop, there is a probability of setup or hold time violation on the inputs to the flip-flops.

These issues originate in the propagation delays in asynchronous logic. These delays are usually very small, and are responsible for introducing differential delays between signals that must travel through different numbers of logic layers and different length signal paths. Unwanted signal combinations may appear for short periods, and the logic reading those signals may interpret the short unwanted signals erroneously (refer to the discussion of glitches, provided in Section II-2.1.5.4). Well-designed synchronous circuits do not suffer from this limitation, because they conform to the control signals only when the clock pulse is present, usually after the transient spurious combinations are over.

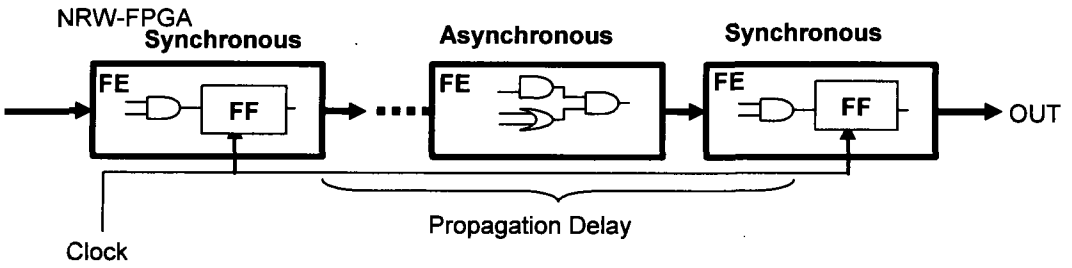


Figure II-2-3 Timing Delay

Minimizing delay is achieved by designing synchronous instead of asynchronous logic. In synchronous logic, all state changes occur on the same rising edge of the clock signal. The only remaining requirement is to allow enough time between clock pulses for signal propagation through the circuit between synchronizing registers, formed of flip-flops.

Toshiba avoids this type of timing problem discussed above through control of signal propagation delays, and using carefully designed combinations of synchronous and asynchronous functional elements within the FPGA logic. To avoid timing errors, the module supplier established FPGA design rules. According to the rules, the engineer must use synchronous design techniques, by placing synchronous logic at the input and output of all asynchronous sections as shown in Figure II-2-3.

Excess use of asynchronous FEs can lead to timing errors. The engineers of the module supplier design FPGAs to minimize propagation delays between synchronous FEs. The Toshiba design timing criteria for synchronous circuits state that the input signals should arrive at the gate inputs within much shorter period than the operation period at the actual clock frequency. In other

words, in order to latch the input signal correctly, the input signal to the synchronizing FE shall arrive at the gate inputs far before next actual clock signal comes. The propagation delay for input signals to the synchronous FEs will arrive at the gate inputs much earlier before actual operation period elapses, so correct information will be latched into the synchronous FE.

To verify that the FPGAs are designed to minimize propagation delays between synchronous FEs in accordance with this rule, the total timing evaluation for the logic is performed after place and route in the design step. The result of this analysis will be compared to specific design criteria. If the criteria are exceeded, the module supplier will take corrective action as needed.

If the designer of the module supplier implements an incorrect design and the duration for the input signal between synchronizing FEs exceeds the criteria, the signal from the output synchronous FE is likely to not represent the logic associated with the signal from the input synchronous FE. Part of the design simulation activities and FPGA testing activities include actions for the designer to look for such events.

Clock skew within the FPGA can be an issue, depending on the logic design. Clock skew is an important factor in design performance; however, clock skew problems may be independent of operating clock frequency. Clock skew is a key factor in setup and hold time verification of the registers. A large clock skew could lead to hold time violations or incorrect register states. The Actel static timing analysis tool performs static timing analysis taking clock skew into account. The clock skew is also evaluated during dynamic timing simulation.

To minimize risks associated with timing, Toshiba performs timing analysis and simulation during their design process. This two-part process includes static timing analysis and dynamic timing simulation. Static timing analysis evaluates the setup and hold times on each path within the FPGA design. The static timing analysis tool evaluates the propagation delay to each element in the code in order to determine each timing path in the code. The result from this static analysis can be interpreted by the FPGA simulation tool program. Engineers of the module supplier then use the FPGA simulation tool to validate the design with dynamic simulation, using accurate propagation delays.

Static timing analysis is the most accurate approach to analyze the timing performance of a design. Once static timing analysis is complete, engineers of the module supplier perform dynamic timing analysis using a separate software tool, verifying the results through extensive bench tests.

II-2.1.5.4 Glitches

A glitch is an unwanted fast "spike" in an electronic signal that is produced by timing hazards inherent in a poorly designed circuit. Glitches are undesirable switching activities that occur before a signal settles to its intended value. Glitches can cause incorrect values to be latched by asynchronous circuits within the electronic device. In particular, glitches can cause improper registering of memory values. Therefore, flip-flops are inserted in the logic to implement synchronous logic and avoid timing issues.

Figure II-2-4 shows how a glitch occurs on a basic "static-zero" hazard circuit. During the input transition, the inherent delay of the inverter circuit creates a transient, unintended logical "ON" signal at the inputs of the AND gate for a time equal to the inverter signal propagation delay. This creates a short output glitch from the AND gate, which can cause improper operation of downstream circuits. Complex digital circuits can include embedded circuit element combinations that reduce to the basic static-zero hazard circuit and produce output glitches.

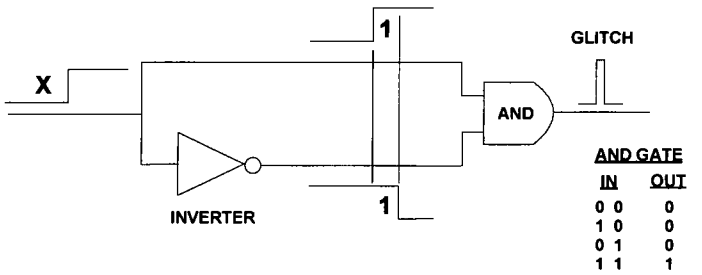


Figure II-2-4 Glitches

Registers are provided as necessary to eliminate glitches. This use of synchronous logic also eliminates other hazard conditions, such as timing errors and metastability. Whenever asynchronous logic is synchronized by a clocked flip-flop, the logic is designed to ensure that the logic has settled to a stable state before clocking the data into the register. Figure II-2-5 shows an example of synchronous design, where the flip-flop in the back-end synchronous FE eliminates a glitch that may be generated in the asynchronous FE.

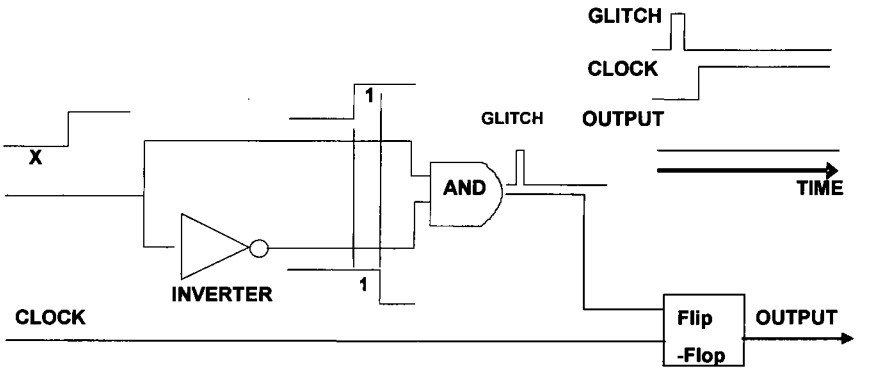


Figure II-2-5 Application of Clocked Flip-Flop

II-2.1.6 Development and Using Functional Elements

II-2.1.6.1 FE Design and Development

The design and development of an FE starts by reviewing the current FE Library. If the FE necessary for the application is available in the module supplier FE Library, the module supplier makes use of the existing FE. All existing FEs were created using the process outlined below. If a new FE needs to be created, then the module supplier follows the process outlined below as well.

The development activities for each FE consist of the following steps:

1. Define FE requirements and document an FE Requirements Specification
2. Perform detailed design and document an FE Specification
3. Prepare an FE Test Procedure
4. Generate a requirements traceability matrix
5. Generate a VHDL source code that implements the FE Specification
6. Perform logic synthesis with optimization and verify that the FE works correctly in simulation
7. Map the FE to an FPGA with appropriate input and output pins and program an FPGA.

8. Perform an FE validation using hardware stimulation of the programmed FPGA

9. Register the FE into the library

Step 1 in developing an FE starts with an FPGA Requirements Specification. The FPGA requirements are traced back to the requirements from NICSD Job Order. The FPGA requirements include evaluation of the FPGA-based system Input/Output signals, as well as interfaces and interactions with other FEs. The module supplier develops the FE Requirements Specification based on the FPGA requirements.

The FE Requirements Specification includes functional and interface requirements for the FE. The functional requirements are generally so simple that the requirements are frequently presented in the form of a block diagram. The interface requirements for the FE include the list of input and output signals. The input and output signals of the FE have the data types of "standard logic" and "standard logic vector" defined in the IEEE Std 1164-1993 "IEEE Standard Multivalue Logic System for VHDL Model Interoperability" (Reference (a41)). The interface description states whether the signal is synchronous or asynchronous. Because most FEs only perform a simple function, an FE Requirements Specification may include requirements for multiple FEs.

In Step 2, the design engineer of the module supplier develops the FE Specification (also referred to as a Software Design Description). The FE Specification defines how the requirements specified in the FE Requirements Specification are implemented. In addition, the FE Specification states the criteria to be used for verification and validation of the FE. The FE Specification depicts the FE functions in the form of block diagrams. The block diagrams include the input signals, the internal processes applied on the input signals, and the output signals. The internal processes are implemented with combinatorial logic or sequential logic. The FE Specification includes the code name and code number, which uniquely identifies the FEs. An FE Specification may include specifications for multiple FEs.

In Step 3, a design engineer of the module supplier, who is not the same person who performs the design work for the corresponding FE, prepares the FE Test Procedure for verification and validation. This procedure defines how the requirements defined in the FE Specification are verified, identifies the software tools to be used for embedding the FE logic onto the FPGA chip, and identifies the software tools to be used for exhaustive tests.

In Step 4, the design engineer prepares the Requirements Traceability Matrix, tracing the FE requirements to FE Specification, as well as tracing the FE Test Procedure to the FE

Specification.

In Step 5, the design engineer generates VHDL source code. The FE is coded using text editors to design logic that will implement the specification in FE Specification. The FE coding follows the VHDL coding rules established by the module supplier.

In Step 6, the design engineer uses the logic synthesis tool to convert the VHDL source code into optimized gate-level netlists. At this point, the design engineers perform functional testing of the FE to verify that the FE meets the requirements defined in the FE Specification using the FPGA simulation tool. In addition, the design engineer generates the test vectors, desired output values, and FE Test Procedure used in Step 8.

Figure II-2-6 is a copy of the graphical output of the FPGA simulation tool for a test of a one-bit full adder[ ] a, c

[ ] a, c

Figure II-2-6 FPGA Simulation Tool Graphical Output for a Test of One Bit Full Adder

In this step, the design engineer verifies correct operation of the FE in the FPGA simulation tool, using the test vectors containing all possible input combinations for functional test coverage. The design engineer verifies that all logic states are correct, and that test coverage is adequate. The test engineer verifies that the test vector toggles each movable digital signal from logic zero to logic one state, and from logic one to logic zero state. The FE validation testing requires a 100% pattern test. That is to say, every possible pattern is applied to the FE, and the outputs from that FE are checked against expected values. Since FEs are combinational, there is no

issue with memory or states within the FE requiring additional combinations of test vectors to exercise memories or state machines. The engineers of the module supplier create the validation test patterns necessary to test individual FEs. The test vectors contain every possible input combination for the FE. The test vectors are validated on a simulation of the FPGA, using tools provided by Microsemi SoC (formerly Actel). The engineer of module supplier will then program the FE into an FPGA, and validate the configured FPGA on a tester, using the FPGA simulation tool and the FPGA adaptor in Step 8.

Like FPGAs, FEs are tested in simulation and then embedded in FPGAs, using the same software and hardware that is used on more complex and complete FPGAs. However, testing for FEs is slightly different from testing of FPGAs. For FEs, every possible input combination is applied to the FE, to ensure complete testing. The outputs from that FE are checked against expected values. FEs that implement simple register memories are tested by exhaustive pattern tests. Except in very limited circumstances, feedback is routed through input and output pins outside the FPGA, simplifying testing since the feedback inputs can be set independently as part of the test vector and the feedback outputs verified. Since the remaining FEs are comprised solely of combinatorial logic, there is no need to apply sequences to move through states.

The FE Requirements Specification and FE Specification will identify one or more logic equations that define the expected output values for all input signal combinations. For very simple logic cells, the test vectors may be generated manually. For logic of any complexity, the test vectors are generated using a spreadsheet. The test vector used for both software- and hardware-based testing is then created from this spreadsheet. For both manually and automatically generated test vectors, the test vectors are generated in a diverse means, and do not depend on the same logic tools used to perform the tests. This alternative means provides checks for the design that would not otherwise exist, if the test vectors were generated by the software tools used to create the FPGAs.

To test the code in the FE, the design engineers prepare an FE Test Procedure prior to testing. The FE Test Procedure includes the desired output values of the FPGA for each test case.

In Step 7, the design engineer embeds the fuse map into an FPGA with the FPGA programming tool.

In Step 8, the design engineer tests the FE in an FPGA integrated circuit using the FPGA adaptor and the FPGA simulation tool. The FPGA simulation tool generates inputs to the FPGAs according to the test vectors, which are generated prior to the FE validation testing. The FE test process is detailed in the FE Test Procedure.

For Steps 6, 7, and 8, software tools are used. The results of software tool errors may not be obvious to the developer. So, the verification and testing activities and FE Test Reports are carefully reviewed by other design engineers.

In Step 9, each FE is registered into the FE Library after confirming that its FE Test Report is issued and is acceptable. The FE library is controlled using an FE Control Sheet that includes:

- Code number, which uniquely identifies the FE
- Code name
- FE Specification
- FE Test Report
- FE source code file name and the media number
- Netlist file name and the media number
- Name and revision numbers of the software tools used

The design engineers place the FE under configuration control, by storing the FE Control Sheet and electronic media containing the FE and associated design documents in the design group's storage locker.

II-2.1.6.2 FE Verification and Validation

In order to simplify peer review and test design, the design engineers of the module supplier do not allow the software tools to perform any automatic optimization on the logic circuits built from FEs. However, optimization is allowed on the FEs. The optimized FEs are captured, peer reviewed, tested, and registered in the FE library with this specific optimization.

The verification process for the FEs permits a more traceable process than for complete FPGA logic verification. Because of the simplicity of the FEs, shorter simulations are possible, with more thorough verification at this level. By using more thoroughly verified FEs in the complete logic, Toshiba eliminates the need for starting complete verification with more complex, unverified logic. Note that FEs are 100% tested as well as reviewed. The connections of FEs are verified in the design of the FPGA, as described later in the LTR. This extensive testing approach at the FE level minimizes the risk of unobserved problems within the total logic in the FPGA. Toshiba believes that by creating good engineering practices and designs for the FEs and by extensive testing of these designs, the verification process for the total FPGA improves, by reducing the number of problems from low-level functional errors.

The module supplier verification and validation processes for the FEs include peer reviews and pattern testing. All tests are performed in accordance with the FE Test Procedure. Results and deviations are recorded in the FE Test Report.

The design engineers document any test failures, any product or configuration nonconformance, or any errors in the test procedure itself in accordance with the steps defined in module supplier procedure. The design engineers resolve the problems by modifying design documentation, logic, testing plans, procedures, and test vectors as necessary. The design engineers revise all previous materials and perform reviews as necessary to incorporate the changes, document the amount of retest required for these changes, and perform retests as needed to resolve the problems.

II-2.1.6.3 Unused FPGA Cells

As defined in the Actel CDR report (Reference (d33)), the FPGA programming tool is used to program the FPGA and to verify the correct connections of FPGA cells within the FPGA. There are checks that are performed by the FPGA programming tool when the FPGA is first inserted, while the fuse map is being loaded into the FPGA, and while programming is being performed. These checks include the following:

- Verify that the file provided to the FPGA programming tool has a valid checksum.
- Prior to programming, the FPGA programming tool verifies that no antifuses are connected in the FPGA.
- The FPGA programming tool verifies that the file provided was compiled for the type of device installed in the programming port.
- Prior to programming, the FPGA programming tool verifies that the standby current is within specified limits for the device type installed in the programming port.
- While programming, the tool measures the impedance and current of each fuse programmed to verify that the programming succeeded.
- The tool anneals the antifuse using controlled-shape current pulses to enhance quality, reliability, and life. The FPGA programming tool verifies the current flow during the annealing to validate the connection's impedance.
- While programming the FPGA, the FPGA programming tool periodically checks all unprogrammed antifuses within the FPGA and verifies that only the expected antifuses have been programmed, and that the unprogrammed antifuses were not inadvertently programmed by integrated circuit hardware failures.

- While programming the FPGA, the FPGA programming tool periodically checks the quality of the already programmed antifuse connections.
- After programming the FPGA, the FPGA programming tool measures the standby current and verifies that it is still within specified limits to show that the programming did not damage the FPGA.
- After programming the FPGA, the FPGA programming tool verifies that the FPGA outputs work correctly, to ensure that outputs are not shorted together.
- After programming the FPGA, the FPGA programming tool verifies that the checksum read from the FPGA matches that provided by the fuse map file, using proprietary methods.

When one of the tests described above finds an error on an FPGA, the design engineer of the module supplier or the technician of the printed circuit board fabricator who embeds FPGA logic into chip for production discards the FPGA. If the tests succeed, the FPGA is used for testing or stored for future module manufacturing.

II-2.1.7 FPGA Simulation Testing and Creating Test Vector

Simulation testing, using the FPGA simulation tool, is performed on the netlist to create a 100% toggle coverage test vector. The test vectors are prepared so that the FPGA is tested functionally and every operative connection between FEs is tested.

The design engineer of module supplier, who is not the same person who performs the design work for the corresponding FPGA logic, is responsible for creating the test vector and FPGA Test Procedure. The design engineer creates the test vector, which is used later for both simulation testing and hardware-based testing. The test vector design starts with testing the complete functional requirements of the logic, including any transitions such as alarm limits. After the design engineer has created an initial test vector to verify all functional requirements, additional test vectors are added repeatedly to verify that each non-static logical connection can toggle from logic zero state to logic one state as well as from logic one state to logic zero state completing the development of the 100% toggle coverage test vector. This toggle testing is performed on simulated logic. The FPGA simulation tool verifies the test coverage percentage for all non-static connections. The design engineer uses the toggle coverage percentage computed by the to judge if the test cases are sufficient, and will add test cases until 100% toggle test coverage is achieved. Figure II-2-7 shows a flowchart for developing the 100% toggle test vector.

For simple logic cells, the test vector may be generated manually. For complex logic cells, the

test vector may be generated using formulas in a spreadsheet. Both manually and automatically generated test vectors are prepared separate from the FPGA simulation tool.

The FPGA simulation tool is used to simulate the internal operation of the logic, providing the design engineer with the capability to watch individual signals within the FPGA and validate that the FPGA logic works as the design engineer intended.

In order to reduce the occurrence of design flaws, NICSD performs an independent review of the FPGA Test Procedure. The FPGA Test Procedures specify the test equipment used in the FPGA testing as well as the test cases.

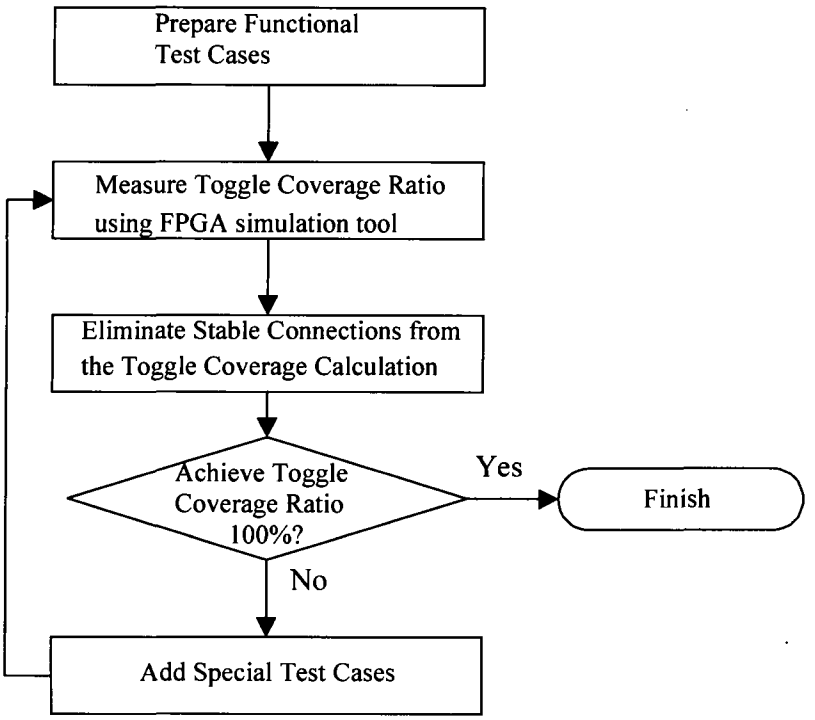


Figure II-2-7 Flowchart for Developing a 100% Toggle Coverage Test Vector

The FPGAs are also toggle tested to verify that the antifuse interconnections between FEs are correct. The toggle tests verify that each of the logic connections that can change between logic zero and one states (i.e., the logic connections that are not forced to logic zero or logic one), can be set into both zero and one states. Due to the large number of possible inputs to the FPGA circuit, it is impractical to test 100% of possible input combinations. Therefore, the design engineer develops a set of test patterns, known as a test vector, which will be used to validate the

FPGA.

The design engineer measures the toggle coverage ratio resulting from the functional test cases. Toggle coverage ratio is defined as the number of toggled connections during testing divided by the number of all used non-static connections. Toggle testing is used to ensure that every non-constant connection between FEs toggles and is thus tested in logic zero and one states.

Figure II-2-8 is a copy of graphical output that shows partial results of a toggle test.

[ ] a, c

Figure II-2-8 Graphical Output that Shows Partial Results of a Toggle Test

The final test vector is fully verified to ensure the completeness of the logic testing of the FPGA circuit design. NICSD reviews the results of the toggle coverage. NICSD may ask for additional tests, as necessary for both functional test completeness and toggle coverage. NICSD verifies sufficiency of the functional and toggle tests, which use test vectors applied for both simulation testing and for testing of a programmed FPGA.

II-2.2 Applications

II-2.2.1 Reactor Trip and Isolation System (RTIS) for Advanced Boiling Water Reactor (ABWR)

While the product designed as been specifically designed and configured for application to an ABWR, the product can be modified to support any Boiling Water Reactor. With appropriate modifications, the design could be adapted to Pressurized Water Reactors and other less-common reactor types, including new Small Modular Reactors.

II-2.2.1.1 System Function

The ABWR Reactor Trip and Isolation System (RTIS) evaluates safety-related plant variables and performs reactor protective actions. Typical functions of the RTIS are described below.

The Reactor Trip and Isolation System (RTIS) implements most of the functions required for the Reactor Protection System (RPS) and includes the Suppression Pool Temperature Monitor (SPTM) and the Main Steam Isolation Valve (MSIV) functions of the Leak Detection and Isolation system (LDS).

The RPS function evaluates safety-related plant variables, generates trip signals, and accomplishes automatic reactor shutdown (scram). The safety-related plant conditions that cause the RPS to force a reactor shutdown are as follows:

- Neutron Monitoring System (NMS) monitored condition exceeds acceptable limit
- Low Reactor Water Level
- High Reactor Pressure
- Main Steam Line Isolation Valve Closure (Inboard or Outboard)
- Low Control Rod Drive (CRD) Hydraulic Control Unit (HCU) Accumulator Charging Header Pressure
- Turbine Stop Valve Closure
- High Suppression Pool Temperature

Operator-initiated manual scram is included in the RPS function.

The MSIV function evaluates safety-related plant variables, generates trip signals and accomplishes automatic MSIV closure. The safety-related plant conditions that force an MSIV closure are as follows:

- Low Reactor Water Level
- Low Main Steam Line Turbine Inlet Pressure
- High Main Steam Line Flow
- High Main Steam Line Tunnel Area Ambient Temperature
- High Main Steam Line Turbine Area Ambient Temperature

Operator-initiated manual MSIV closure is included in the MSIV function.

The SPTM function calculates the averaged suppression pool temperature and generates a trip signal if the calculated temperature is above the setpoint.

II-2.2.1.2 Response Time

RTIS Response time is defined as the delay time from an input signal change to the corresponding output signal change. The RPS trip and MSIV closure response time is defined measured as a delay time from a sensor signal change to the LD output change. The response time shall be validated in the system validation test, where all RTIS units will be integrated.

RTIS Response time is divided into five cases as described in the following subsections

II-2.2.1.2.1. Response time of RPS Trip (including SPTM Trip)

The response time shall be measured as an interval between the instant at which a sensor signal makes a step change, or a discrete signal changes, and the instant at which the LD contact opens.

The response time is defined as following cases:

Case 1: The DTF-RPS generates a plant condition trip signal as a sensor channel trip.

In Case 1, response time from sensor input step change to a value that exceeds the setpoint to DTF-RPS output varies typically [ ] a, c including sensor response time, depending on the sensor channels. The DTF-RPS shall be fast enough to meet these requirements. Response time from DTF-RPS output to LD-RPS contact opening shall not exceed 50 ms.

Case 2: A process switch generates the trip signal and it passes through the DTF-RPS.

In Case 2, response time from discrete switch output to LD-RPS contact opening shall not exceed

50 ms.

Case 3: The NMS generates the trip signal as a NMS trip.

In Case 3, response time from discrete switch output of the NMS to LD-RPS contact opening shall not exceed 50 ms.

Case 4: The SPTM generates the trip signal as a SPTM trip.

In Case 4, response time from sensor output to LD-RPS contact opening shall not exceed[ ]a, c

II-2.2.1.2.2. Response Time of MSIV Closure

The response time is measured as an interval between the instant at which a sensor signal makes a step change to a value that exceeds the setpoint, and the instant at which the LD contact opens.

The response time is defined as following case (Note: Case numbers are continued from previous section):

Case 5: The DTF-MSIV generates a plant condition trip signal as a sensor channel trip.

The response time from sensor input step change to a value that exceeds the setpoint to LD-MSIV contact opening output varies[ ]a, c including sensor response time, depending on the sensor channels.

II-2.2.1.3 System Configuration

Figure II-2-9 provides a typical diagram of one RPS division of trip logic. A diagram of one division of MSIV closure trip logic is similar.

The RPS and MSIV functions are implemented in four redundant divisions of RTIS. Sensor signals are hardwired to the Digital Trip Function (DTF) inputs for each division. Each division's DTF determines the trip status for each signal. The DTF communicates its division's trip status information to the Trip Logic Function (TLF) in all divisions over individual point-to-point fiber optic communication links, because individual divisional trip determinations must be shared between divisions to support two-out-of-four voting logic for divisional trip outputs. The links provide a qualified and isolated, point-to-point, uni-directional communication path between divisions to preserve divisional independence.

The TLF in each division independently determines the system-level actuation of RPS and MSIV

safety functions using two-out-four voting logic. In each division, the TLF communicates trip status information to the Output Logic Unit (OLU) by uni-directional fiber optic communication links. The OLU in each division communicates with the Load Drivers (LDs) that initiate the safety function. The LD-RPSs are hardwired to its scram solenoid valves, and the LD-MSIVs are hardwired to its MSIV solenoid valves.

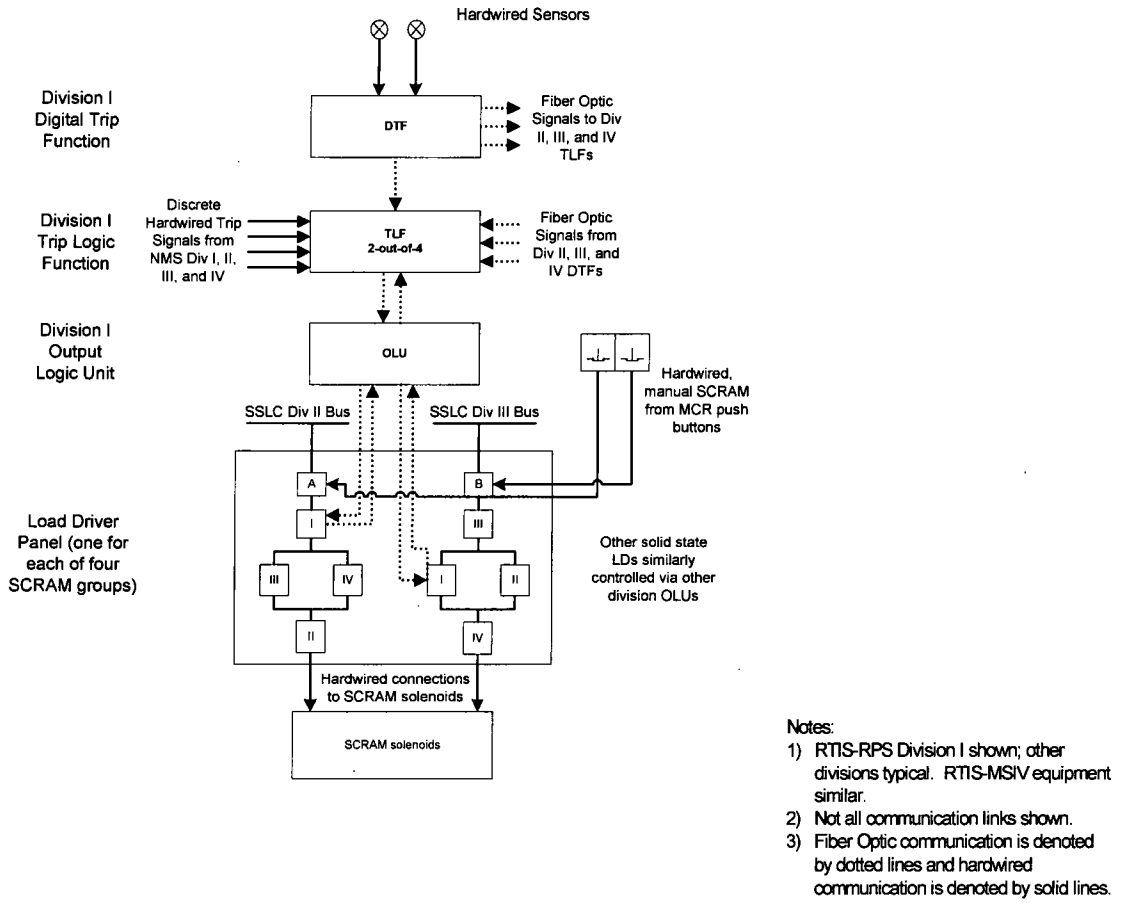


Figure II-2-9 Typical Diagram of One RPS Division of Trip Logic

II-2.2.1.4 Unit/Module Configuration

This section describes Unit/module configuration of the RTIS. Figure II-2-10 shows the Module and Unit configuration of one RPS division of trip logic for the reactor.

Figure II-2-11 shows the Module and Unit configuration of one MSIV closure logic trip function.

Table II-2-1 lists modules used in each unit in the RTIS.

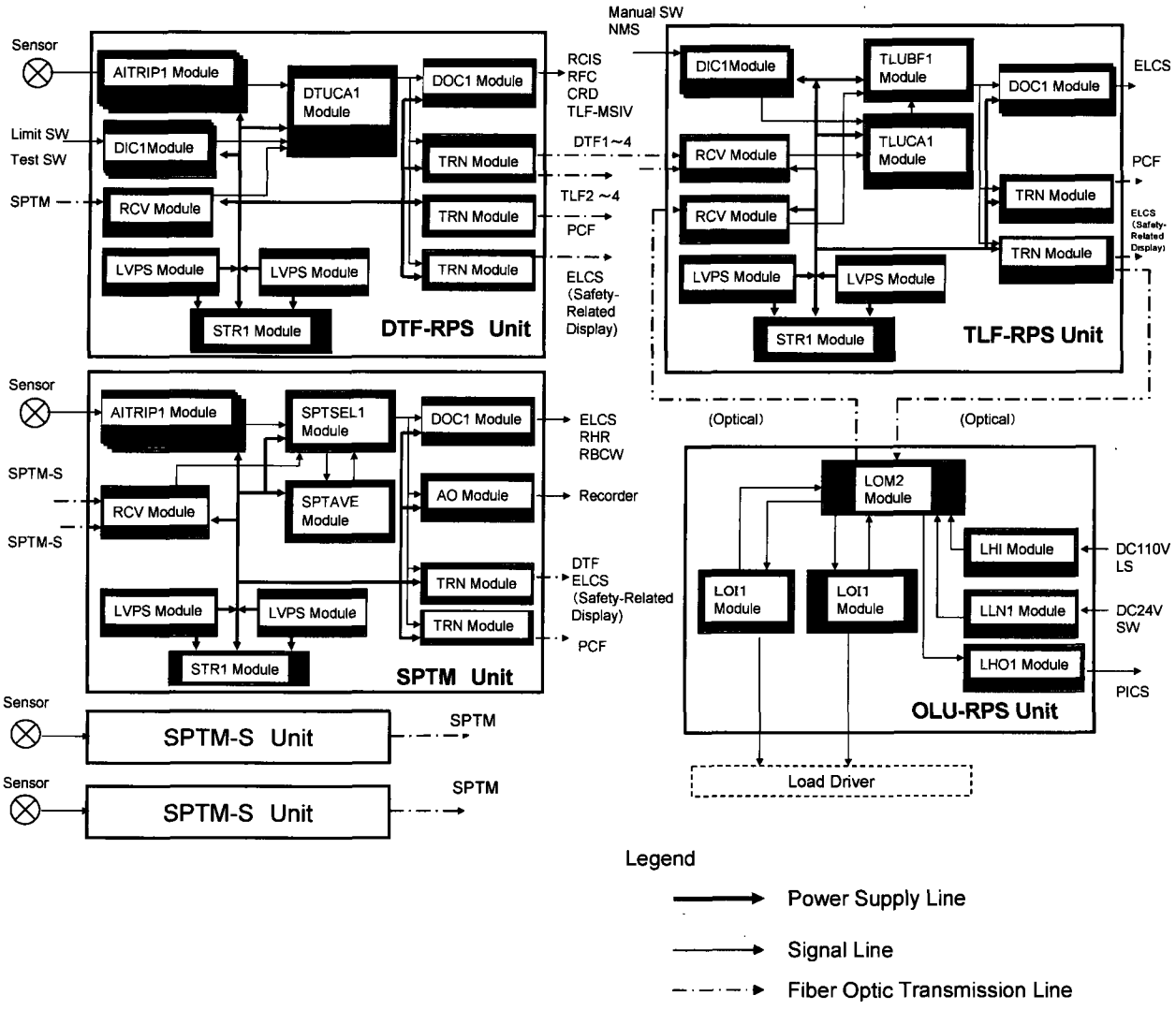


Figure II-2-10 Module and Unit Configuration of One RPS Division of Trip Logic in RTIS

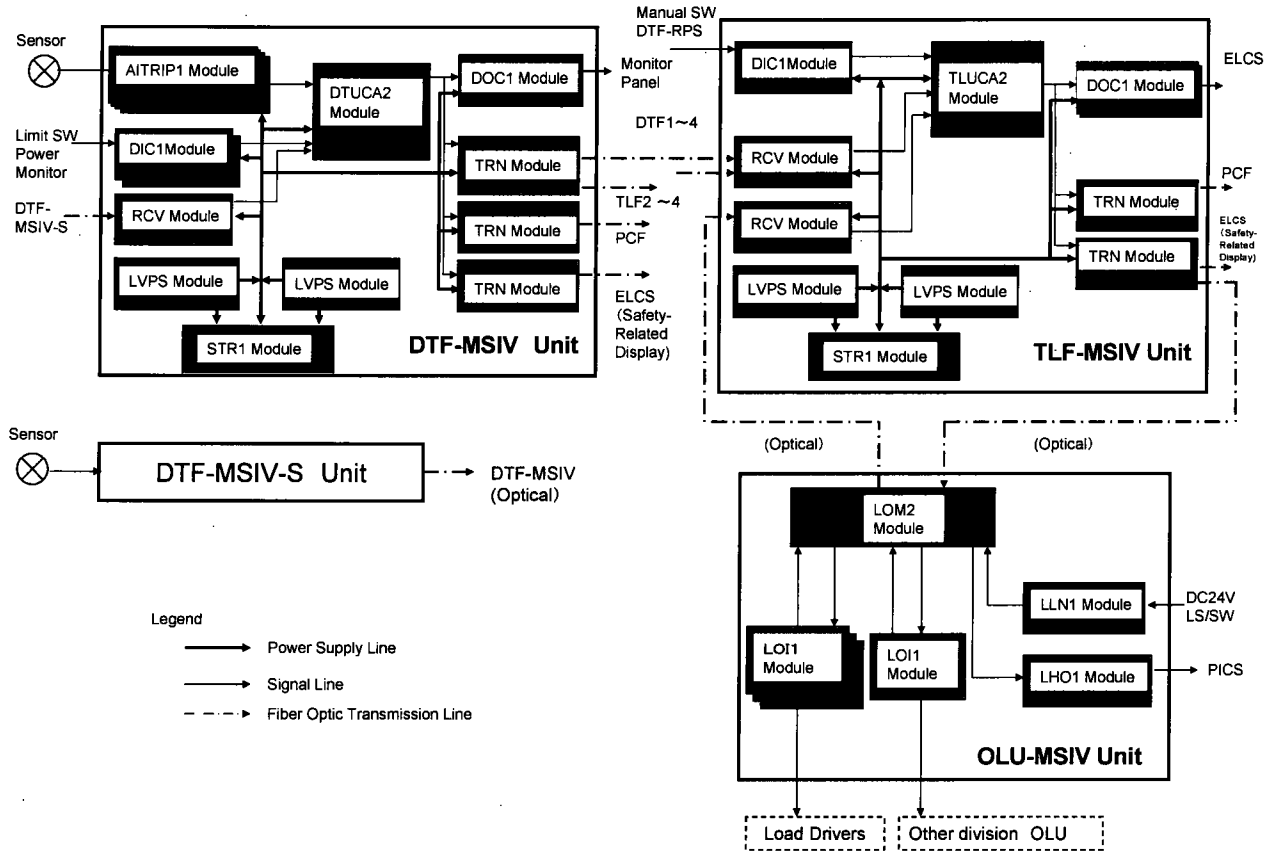


Figure II-2-11 Module and Unit Configuration of One Division MSIV Closure Logic

Table II-2-1 Module List of RTIS

Module Name	Module Model Number*1	Number of Applied Module for 4 divisions of RTIS in Figure II-2-10 and Figure II-2-11		Functional Description
		Total Number	Description Note: The system consists of 4 RPS divisions and 4 MSIV divisions.	
AITRIP1 Module	HNS1100	192	- 8 modules in a SPTM unit - 8 modules in each unit of 2 SPTM-S units - 7 modules in a DTF-RPS unit (in each RPS Division) - 8 modules in a DTF-MSIV unit - 9 modules in a DTF-MSIV-S unit (in each MSIV Division)	Analog voltage signal processing and Trip Decision

Module Name	Module Model Number*1	Number of Applied Module for 4 divisions of RTIS in Figure II-2-10 and Figure II-2-11		Functional Description
		Total Number	Description Note: The system consists of 4 RPS divisions and 4 MSIV divisions.	
SPTAVE1 Module	HNS1110	4	- 1 module in a SPTM unit (in each RPS Division)	Sensor signal average calculation and transfer data to AITRIP1 Module for Trip decision
SPTSEL1 Module	HNS1120	4	- 1 module in a SPTM unit (in each RPS Division)	Sensor signal Select and other data multiplexing
MLTPL1 Module	HNS1130	8	- 1 module in each unit of 2 SPTM-S units (in each RPS Division)	Serial Data Packet Conversion
DTUCA1 Module	HNS1141	4	- 1 module in a DTF-RPS unit (in each RPS Division)	Test Logic and Transfer Data multiplexing
DTUCA2 Module	HNS1142	4	- 1 module in a DTF-MSIV unit (in each MSIV Division)	Test Logic and Transfer Data multiplexing
TLUCA1 Module	HNS1151	4	- 1 module in a TLF-RPS unit (in each RPS Division)	4 division DTF signals input and 2 out of 4 Trip or 2 out of 3 Logic Decision
TLUCA2 Module	HNS1152	4	- 1 module in a TLF-MSIV unit (in each MSIV Division)	4 division DTF-MSIV signals input and 2 out of 4 Trip or 2 out of 3 Logic Decision
STR1 Module	HNS1161	4	- 1 module in a SPTM unit (in each RPS Division)	unit error diagnosis data display
STR1 Module	HNS1162	8	- 1 module in each unit of 2 SPTM-S units (in each RPS Division)	unit error diagnosis data display
STR1 Module	HNS1163	4	- 1 module in a DTF-RPS unit (in each RPS Division)	unit error diagnosis data display
STR1 Module	HNS1164	4	- 1 module in a DTF-MSIV unit (in each MSIV Division)	unit error diagnosis data display
STR1 Module	HNS1165	4	- 1 module in a TLF-RPS unit (in each RPS Division)	unit error diagnosis data display
STR1 Module	HNS1166	4	- 1 module in a TLF-MSIV unit (in each MSIV Division)	unit error diagnosis data display
STR1 Module	HNS1167	4	- 1 module in a DTF-MSIV-S unit (in each MSIV Division)	unit error diagnosis data display
MLTPL2 Module	HNS1170	4	- 1 module in a DTF-MSIV-S unit (in each MSIV Division)	Serial Data Packet Conversion
TLUBF1 Module	HNS1180	4	- 1 module in a TLF-RPS unit (in each RPS Division)	OLU data buffering and data multiplexing
LVPS Module	HNS0500	64	- 2 modules in a SPTM unit - 2 modules in each unit of 2 SPTM-S units - 2 modules in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 2 modules in a DTF-MSIV unit - 2 modules in a DTF-MSIV-S unit - 2 modules in a TLF-MSIV unit (in each MSIV Division)	+5V and ±15V power supply to each module

Module Name	Module Model Number*1	Number of Applied Module for 4 divisions of RTIS in Figure II-2-10 and Figure II-2-11		Functional Description
		Total Number	Description Note: The system consists of 4 RPS divisions and 4 MSIV divisions.	
AO Module	HNS0515	4	- 1 module in a SPTM unit (in each RPS Division)	Analog outputs to the mimic display on the main control panel and the Transient Monitor (+1 to +5V)
TRN Module	HNS0531	64	- 2 modules in a SPTM unit - 1 module in each unit of 2 SPTM-S units - 3 modules in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 3 modules in a DTF-MSIV unit - 2 modules in a DTF-MSIV-S unit - 2 modules in a TLF-MSIV unit (in each MSIV Division)	Optical data transmission module
RCV Module	HNS0541	28	- 1 module in a SPTM unit - 1 module in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 1 module in a DTF-MSIV unit - 2 modules in a TLF-MSIV unit (in each MSIV Division)	Optical data reception module
DIC1 Module	HNS0730	32	- 3 modules in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 2 modules in a DTF-MSIV unit - 1 module in a TLF-MSIV unit (in each MSIV Division)	Discrete signal input
DOC1 Module	HNS0740	28	- 1 module in a SPTM unit - 1 module in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 1 module in a DTF-MSIV unit - 2 modules in a TLF-MSIV unit (in each MSIV Division)	Discrete signal output
LOM2_1 Module	HNS1201	4	- 1 module in a OLU-MSIV unit (in each MSIV Division)	Optical Transmission data received from TLF unit and sequential signal processing
LOM2_2 Module	HNS1202	4	- 1 module in a OLU-RPS unit (in each RPS Division)	Optical Transmission data received from TLF unit and sequential signal processing
LOI1 Module	HNS1211	28	- 2 modules in a OLU-RPS unit (in each RPS Division) - 5 modules in a OLU-MSIV unit (in each MSIV Division)	Optical Transfer to Load Drivers
LOI1 Module	HNS1212	4	- 1 module in a OLU-MSIV unit (in each MSIV Division)	Optical Transfer to other division OLU

Module Name	Module Model Number*1	Number of Applied Module for 4 divisions of RTIS in Figure II-2-10 and Figure II-2-11		Functional Description
		Total Number	Description Note: The system consists of 4 RPS divisions and 4 MSIV divisions.	
LLN1 Module	HNS1220	8	- 1 module in a OLU-RPS unit (in each RPS Division) - 1 module in a OLU-MSIV unit (in each MSIV Division)	Discrete signal input (DC24V)
LHI1 Module	HNS1230	4	- 1 module in a OLU-RPS unit (in each RPS Division)	Discrete signal input (DC110V)
LHO1 Module	HNS1240	8	- 1 module in a OLU-RPS unit (in each RPS Division) - 1 module in a OLU-MSIV unit (in each MSIV Division)	Discrete signal output (AC/DC110V)
LDC1 Module	HNS1250	112	- 1 module in each RPS LD unit (32 RPS LD units in the system) - 2 modules in each MSIV LD unit (40 MSIV LD units in the system)	LD control module
LDD1 Module	HNS1261	80	- 2 modules in each MSIV LD unit (40 MSIV LD units in the system)	LD driver module for MSIV
LDD1 Module	HNS1262	32	- 1 module in each RPS LD unit (32 RPS LD units in the system)	LD driver module for RPS
LDB1 Module	HNS1270	32	- 1 module in each RPS LD unit (32 RPS LD units in the system)	LD booster module for RPS
SLD1 Module	-	120	- 1 module in OLU-RPS unit (in each RPS Division) - 1 module in OLU-MSIV unit - (in each MSIV Division) - 1 module in each RPS LD unit (32 RPS LD units in the system) - 2 modules in each MSIV LD unit (40 MSIV LD units in the system)	Shield(blank) Panel

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-2.2.1.5 Design Features in Focus

II-2.2.1.5.1 Interface with Field Sensors and Actuators

The DTF-RPS unit receives voltage signals converted from sensor current signals, discrete signals (trip signals) via several converters (including relays), and receives a Suppression Pool Temperature Monitoring (SPTM) trip signal from the SPTM unit over fiber optical cables.

For each sensor signal, the DTF-RPS unit generates a sensor channel trip signal by comparing the sensor signal with the setpoint provided for that sensor signal. Each trip signal or sensor channel trip signal represents whether the reactor trip condition is fulfilled, such as "the reactor pressure is High."

The DTF-RPS unit transmits these signals to the TLF-RPS unit in each of the four divisions independently over point-to-point the fiber optical cables.

Besides, the DTF-RPS unit receives trip test signals from the manual switches for trip testing via hardwired connection. The DTF-RPS unit transmits DTF-RPS trip signals to RCIS, Control Rod Drive System (CRD) and TLF-MSIV, and transmits bypass signal to the Reactor Recirculation Flow Control System (RFC) using relays for isolation.

The TLF-RPS unit receives DTF-RPS trip signals from the DTF-RPS unit in four divisions, and NMS trip signals from the NMS in four divisions via several converters including relays. The NMS trip signals are discrete signals to show whether the NMS reactor trip conditions have been met. The TLF-RPS unit applies 2-out-of-4 voting logic on a set of signals which are received from each of four NMS divisions, and then the unit generates a TLF-RPS trip signal by voting. The unit transmits a TLF-RPS trip signal to the OLU-RPS unit in the same division by fiber optic cable.

The TLF-RPS unit receives bypass signals from manual switches in the Main Control Room (MCR) area by hardwired connections, and then performs bypass function for testing or maintenance.

The OLU-RPS unit receives a TLF-RPS trip signal from the TLF-RPS unit in the same division by fiber optic cable, and seals the signal in until reset manually by the MCR operator. The OLU-RPS unit transmits the LD energize signal to the LD-RPSs through the fiber optical cables until a SCRAM is required, and outputs contact signals to the backup scram solenoids.

The LD-RPS units de-energize the scram pilot valve solenoid when the LD-RPS unit receives an Auto-Scram signal.

The DTF-MSIV unit receives voltage signals converted from sensor current signals including relays, and receives a trip signal from the DTF-MSIV-S unit through a fiber optic cable. For each sensor signal, the DTF-MSIV unit generates a sensor channel trip signal by comparing the sensor signal with the reset point. Each trip signal from the DTF-MSIV-S unit or sensor channel trip signal represents whether the MSIV closure trip condition is fulfilled, such as "the main steam line pressure is Low." The DTF-MSIV unit transmits these signals to the TLF-MSIV unit in four divisions through individual fiber optical cables.

The DTF-MSIV unit receives trip test signals from the manual switches for trip testing by hardwired connection.

The DTF-MSIV-S unit receives voltage signals converted from sensor signals. For each sensor signal, the DTF-MSIV-S unit generates a sensor channel trip signal by comparing the sensor signal with the reset point. The DTF-MSIV-S transmits these signals to the DTF-MSIV unit in same division through a point-to-point fiber optic cable.

The TLF-MSIV unit receives the DTF-MSIV trip signals from the DTF-MSIV unit in four divisions over fiber optical cables. The TLF-MSIV unit applies 2-out-of-4 voting logic on the signals that are received from four divisions, and generates a TLF-MSIV trip signal. The unit transmits a TLF-MSIV trip signal to the OLU-MSIV unit in the same division through a point-to-point fiber optic cable.

The TLF-MSIV unit performs bypassing and relating interlocking based on the bypass and reactor mode signals from the manual switches using hardwired connection.

The OLU-MSIV unit receives a TLF-MSIV trip signal from the TLF-MSIV unit in the same division, and seals the signal in until reset by the MCR operator. The OLU-MSIV unit transmits LD energize signal to the LD-MSIVs through point-to-point fiber optic cables.

The LD-MSIV units de-energize the MSIV pilot valve solenoid when the LD-MSIV unit receives an auto MSIV closure signal.

II-2.2.1.5.2 Power Supply

RTIS has redundant power supply module called the Low Voltage Power Supply (LVPS) in the following units:

- DTF-RPS Unit
- TLF-RPS Unit
- SPTM Unit
- SPTM-S Unit
- DTF-MSIV Unit
- DTF-MSIV-S Unit
- TLF-MSIV Unit

The LVPS Module supplies +5V DC and ±15V DC.

The OLU-RPS and the OLU-MSIV unit are provided with +5V DC external power.

The requirements for external power source are described in Section II-2.2.3.1.3

II-2.2.1.5.3 Annunciation of Failures

The RTIS generates Inoperative signal when faults occur that affect the execution of the RTIS safety functions. The following Units generate Inoperative signals:

- DTF-RPS Unit
- TLF-RPS Unit
- SPTM Unit
- SPTM-S Unit
- OLU-RPS Unit
- DTF-MSIV Unit
- DTF-MSIV-S Unit
- TLF-MSIV Unit
- OLU-MSIV Unit

These Units have LED indicators in the Unit's front panel to show the generation of each Inoperative signal. Inoperative signals generated in DTF-RPS Unit and DTF-MSIV Unit are transferred to other divisions as part of the RPS or MSIV Trip voting functions. Either of OLU or TLF Inoperative signal in a division causes a divisional trip. Generating either OLU or TLF Inoperative signals from two or more divisions leads to the RPS Trip or MSIV Trip.

All Inoperative signals are transferred to safety and non-safety displays by unidirectional fiber communication links. The conditions for generating Inoperative signals are defined in the Equipment Design specifications for each application.

II-2.2.1.5.4 Boundary between Safety and Non-Safety

The RTIS has signal connections to non-safety systems using both isolation through hardwired relays and uni-directional fiber optic links. Those are the boundary from the safety system into the non-safety system. Figure II-2-10 and Figure II-2-11 describe these boundary points.

II-2.2.2 Neutron Monitoring System

In this section, the functions, response time, system configuration, Unit/Module configuration of the NMS, and important design features are described.

Section II-2.2.2.1 describes general functions of the NMS.

Section II-2.2.2.2 describes response time requirements.

Section II-2.2.2.3 describes the system configurations of the NMS in BWRs and ABWR. System configurations for various BWR types are described in Appendix II-A.

Section II-2.2.2.4 describes the Unit/Module configuration of the NMS for BWR-5. The PRM for BWR-5 is used for qualification.

Section II-2.2.2.5 describes design features in focus of the NMS for BWR-5 in accordance with Section II-2.2.2.4.

II-2.2.2.1 System Function

The Neutron Monitoring System (NMS) monitors the core neutron flux during shutdown, during fuel loading, and from the startup source range to beyond rated power. The NMS monitors power generation and provides trip signals to the Reactor Protection System (RPS) to initiate

reactor scram under excessive neutron flux (and power) condition (high level), core oscillation, or neutron flux fast rising (short period) conditions.

The NMS has following 3 safety-related subsystems:

- Startup Range Neutron Monitor (SRNM)
- Local Power Range Monitor (LPRM)
- Average Power Range Monitor (APRM) which includes Oscillation Power Range Monitor (OPRM)

The SRNM monitors neutron flux from the source range to 15% of the rated power. The SRNM is the integrated system of the Source Range Monitor (SRM) and the Intermediate Range monitor (IRM). The SRM and the IRM can be replaced by the SRNM. Over the 10 decade power monitoring range, two monitoring methods are used. For the lower ranges, the counting method is applied. And for the higher ranges, the Campbelling technique (mean square voltage (MSV)) is applied. In the counting range, the discrete pulses produced by the sensors are applied to a discriminator after preamplification. The neutron pulses are then counted. The reactor power is proportional to the count rate. In the MSV range, where it is difficult to distinguish the pulses, a mean square value of the input signal is produced. The reactor power is proportional to this mean square value. In region that overlaps these two ranges, the SRNM unit calculates the neutron flux based on a weighted interpolation of the two flux values calculated by both methods. A continuous and smooth flux reading transfer is achieved in this manner. There is also the calculation algorithm of the period-based trip circuitry that generates the trip margin setpoint for the period trip protection function.

The LPRM monitors local neutron flux in the power range between 1 % and 125 % of the rated power, and provides local neutron flux to APRM and OPRM.

The APRM averages the output signals from its assigned LPRMs. The averaging circuit automatically corrects for the number of unbypassed LPRMs providing input signals. APRM also includes a flow measurement function. The flow measurement function receives signals from transmitters, and converts them to the core flow rate for ABWR or the recirculation flow rate for BWR. APRM provides a simulated thermal power value in each APRM channel by giving a first order time delay to the averaged power. Reactor core flow or recirculation flow signals are used in the APRM to provide the flow biasing for the APRM rod block and simulated thermal power trip setpoint functions.

The OPRM receives the same LPRM signals as the corresponding APRM channel as inputs.

The OPRM determines whether there is thermal hydraulic instability and provides trip signals to the RPS to suppress neutron flux oscillation prior to violation of safety thermal limits. The LPRMs and APRM combine to form the Power Range Neutron Monitor (PRM)

II-2.2.2.2 Response Time

II-2.2.2.2.1 Startup Range Neutron Monitor (SRNM)

The response time of the SRNM shall be as follows.

1. The response time of the SRNM for a trip output to RTIS shall not exceed 150 ms.

For the SRNM for ABWR, the following additional requirement shall be met.

2. The SRNM ATWS Permissive signal response time for the output of the signal shall not exceed[ ]a, c

II-2.2.2.2.2 Power Range Neutron Monitor (PRM)

The response time of the PRM shall be as follows.

1. APRM Upscale Flux Trip
   The APRM Upscale Flux Trip response time from the change of the LPRM input signal above the setpoint limit to the occurrence of trip from Relay unit shall not exceed 40 ms.
2. Simulated Thermal Power Upscale Trip
   The Simulated Thermal Power Upscale Trip response time from the simulated thermal power exceeding the setpoint limit to the occurrence of trip from Relay unit shall not exceed 40 ms

For the Power Range Neutron Monitor for ABWR, the following additional requirements shall be met.

3. Core Flow Rapid Coastdown
   The core flow rapid coastdown trip is required to deal with the Reactor Internal Pumps, which do not have the inertial coastdown characteristics of the reactor recirculation pumps in a BWR-3, -4, -5, or -6. The core flow rapid coastdown response time shall not exceed[ ]a, c
4. APRM ATWS Permissive
   The APRM ATWS Permissive signal response time from the change of the LPRM input signal above the setpoint limit to the output of ATWS Permissive signal shall not exceed[ ]a, c ms.

II-2.2.2.3 System Configuration

The safety-related portion of the NMS consists of the SRNM, the LPRM, and the APRM. The OPRM is a functional subsystem of the APRM.

In ABWR, SRNM channels are arranged into four divisions such that each of the four RPS divisions receives all of the SRNM input signals from each of the four SRNM divisions. SRNM are not considered redundant, as each detector monitors a different portion of the reactor core.

In BWRs, SRNM systems are typically configured with six or eight SRNM channels. The SRNM channels are mapped to four trip channels that make two groups having two trip channels each. When more than one SRNM provides trip signals in both groups, a reactor scram is initiated through RPS function. Failure of a single SRNM channel, once bypassed, will not cause a trip signal to be sent to the RPS. Failure of a single SRNM channel will not prevent proper operation of the remaining trip channels in performing their safety functions and satisfying the IEEE STD 603 (Reference (a36)) Single Failure Criterion (Clause 5.1).

For power range neutron flux monitoring, the LPRMs provide data to the APRM and OPRM. LPRM, APRM, and OPRM are provided in each of the four divisions. The LPRM detector sensors are divided into four redundant groups, each group providing local power range signals to its assigned divisional APRM. Each LPRM detector can be individually bypassed, with a minimum required number of LPRMs in each division. Each LPRM detector assembly contains four LPRM detectors, monitoring four distinct levels in the reactor core. Each LPRM detector assembly provides one LPRM input to each of the four independent and redundant APRM and OPRM channels in the same division. LPRM detectors are mapped to divisions to ensure that each APRM and OPRM channel has a representative view of the reactor core.

There are four redundant, independent channels of APRM in the ABWR design, and six or eight channels of APRM in BWR designs, with each channel providing a trip signal to the RPS. In the ABWR design, any two of the four APRM channels that indicate an abnormal condition will initiate a reactor scram through the RPS two-out-of-four trip logic. In the other BWR designs, the six or eight APRMs are divided into two groups where each group consists of three or four APRMs. When more than one APRM provides trip signals in both groups, a reactor scram is initiated through RPS function. The redundancy criteria are met so that in the event of a single failure under permissible APRM channel bypass conditions, a scram signal will still be generated in the RPS as required. Thus, the IEEE Std 603 Single Failure Criterion (Clause 5.1) is satisfied.

There are independent and redundant channels of OPRM. The above APRM channel redundancy condition also applies to OPRM channels. Bypassing a division of APRM bypasses the same division of OPRM. The OPRM trip outputs are separate from the APRM trips to RPS and use similar RPS two-out-of-four voting logic as the APRM, satisfying the IEEE Std 603 Single Failure Criterion (Clause 5.1). The arrangement and assignment of LPRMs provide core regional monitoring by redundant OPRM channels.

Figure II-2-12 and Figure II-2-13 show the configuration of the safety-related NMS for the ABWR and BWR designs, respectively.

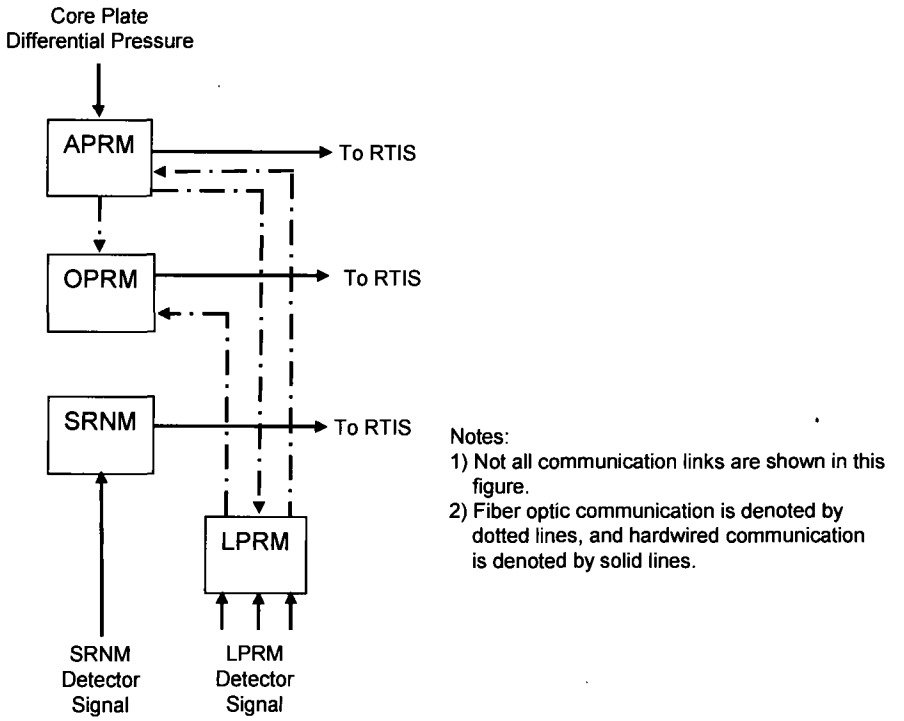


Figure II-2-12 Overview of System Configuration of NMS (ABWR)

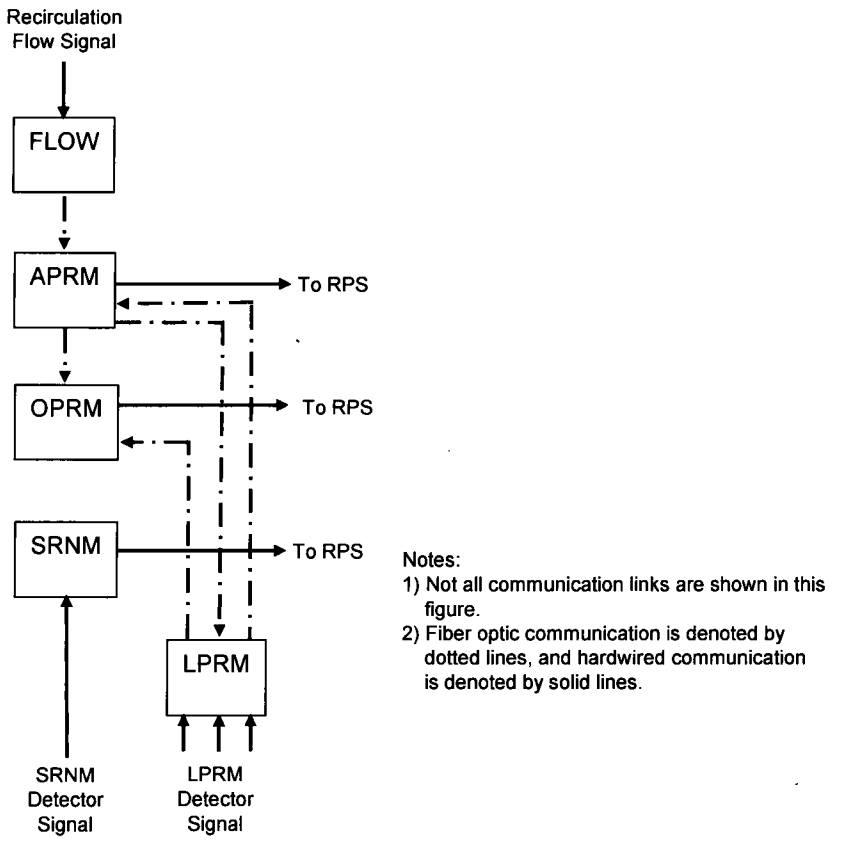


Figure II-2-13 Overview of System Configuration of NMS (BWR)

II-2.2.2.4 Unit/Module Configuration

This section describes Unit/module configuration of the NMS. Figure II-2-14, Figure II-2-15, Figure II-2-16 and Figure II-2-17 show typical Module and Unit configuration of the PRM for BWR-5, PRNM for ABWR, OPRM and SRNM, respectively. Table II-2-2 through Table II-2-5 list Modules used in the NMS in accordance with the Module and Unit configuration shown in Figure II-2-14 through Figure II-2-17.

Appendix II-A describes the detailed configuration for the application of the NMS to various BWR types.

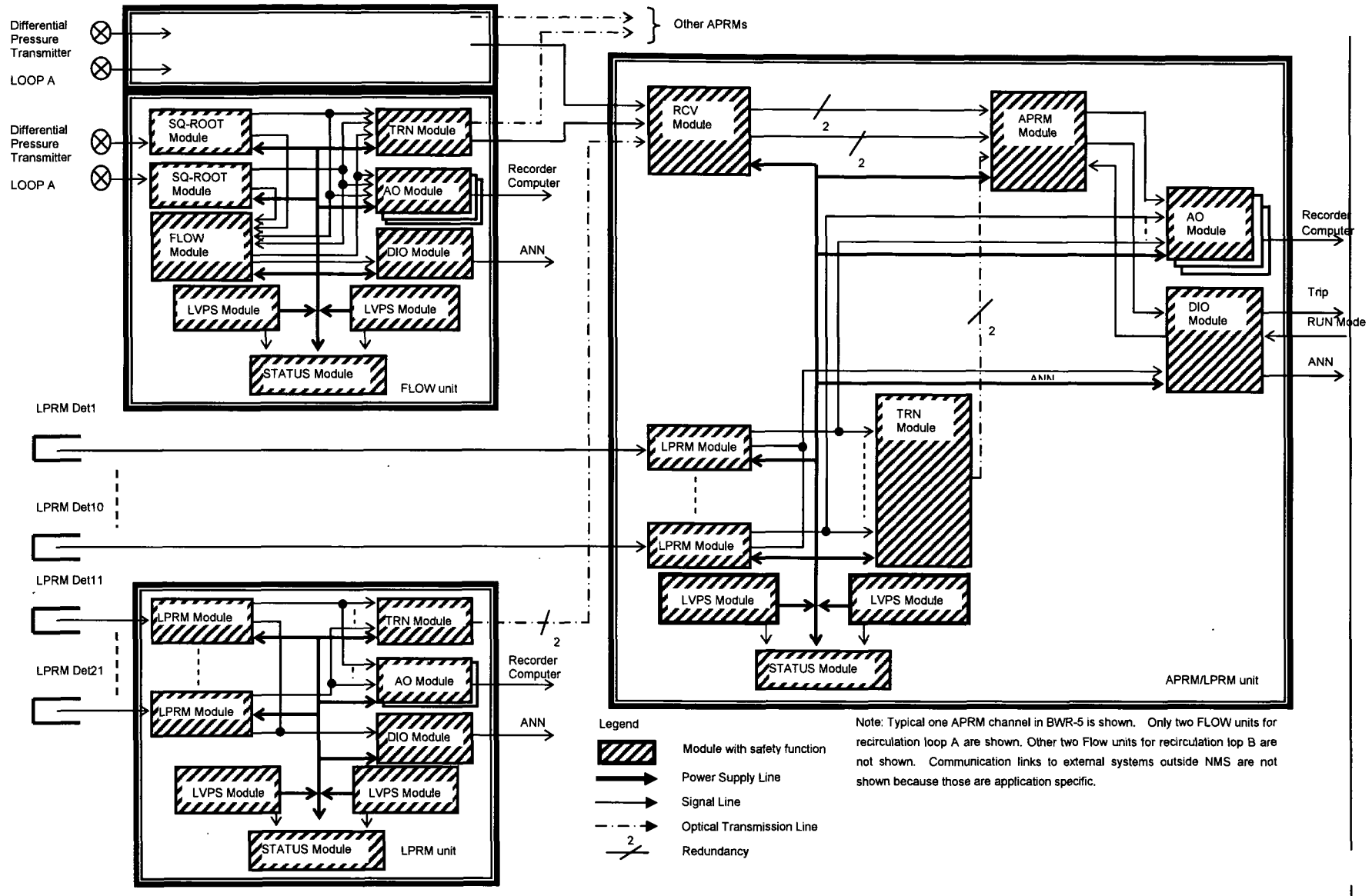


Figure II-2-14 Module and Unit Configuration of PRM for BWR-5 (OPRM Not Shown)

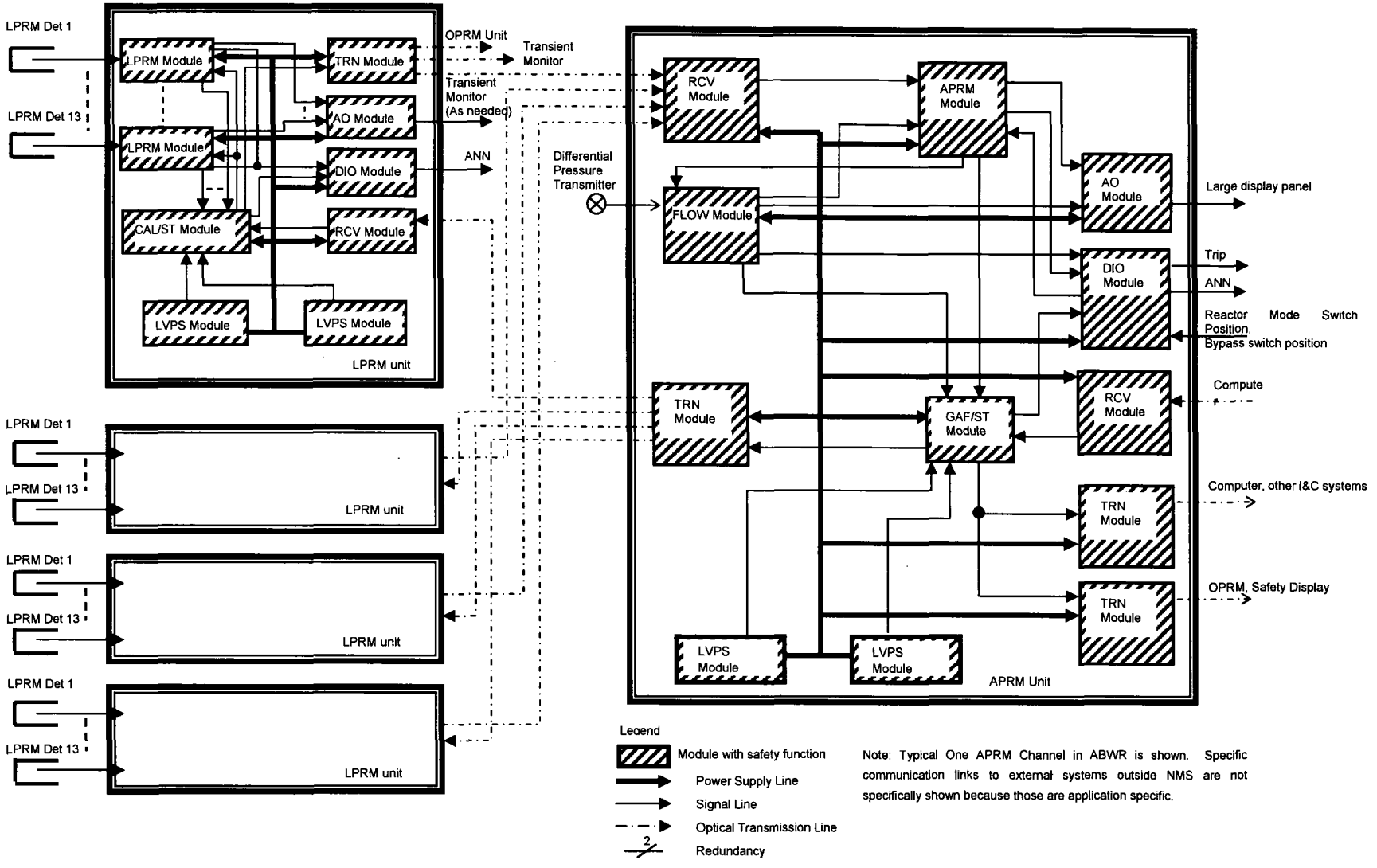


Figure II-2-15 Module and Unit Configuration of PRM for ABWR (OPRM Not Shown)

Table II-2-2 Module List of PRM for BWR-5 (OPRM Not Shown)

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-2-14		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 4 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 4 FLOW units in the system accordingly.	
LPRM Module	HNS013	172	- 11 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM A, C and E channels. - 12 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM B, D, and F channels - 11 modules in the first LPRM unit and 10 modules in the second LPRM unit in LPRM A channel - 12 modules in the first LPRM unit and 10 modules in the second LPRM unit in LPRM B channel	LPRM function
APRM Module	HNS020	6	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030	8	- 2 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040	4	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091	6	- 1 module in an LPRM/APRM unit	Data reception status and power supply voltage monitoring status indications.
STATUS Module	HNS093	14	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
MUX Module	HNS260	2	- 1 module in one of the 2 LPRM units in an LPRM channel	Multiplexing module for LPRM data transmission
BLANK Module	HNS490	12	- 2 modules in an LPRM unit for APRM A, C and E channels. - 2 modules in one of the 2 LPRM units in LPRM A channel - 1 module in an LPRM unit for APRM B, D and F channels. - 1 module in one of the 2 LPRM units in LPRM B channel	Dummy LPRM module to fill open slots when the LPRM unit is not filled with 13 LPRM Modules.
LVPS Module	HNS500	40	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515	16	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit	Analog outputs to the Transient Monitor

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-2-14		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 4 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 4 FLOW units in the system accordingly.	
AO Module	HNS516	10	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders
AO Module	HNS517	4	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518	20	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520	20	- 1 module in each unit in the system	Discrete signal input and output module
TRN Module	HNS0531	24	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541	8	- 1 module in an LPRM/APRM unit - 1 module in one of the 2 LPRM units in an LPRM channel	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

Table II-2-3 Module List of PRNM for ABWR (OPRM Not Shown)

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-2-15		Functional Description
		Total Number	Description Note: The system consists of 4 divisions with 1 APRM unit and 4 LPRM units in each division.	
LPRM Module	HNS0302	208	- 13 modules in a LPRM unit	LPRM function
APRM Module	HNS0311	4	- 1 module in an APRM unit	APRM function
FLOW Module	HNS0321	4	- 1 module in an APRM unit	Core-flow calculation, trip and alarm functions
CAL/ST Module	HNS0330	16	- 1 module in an LPRM unit	Power status and Input status indications. LPRM calibration currents are calculated and provided to LPRM modules.

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-2-15		Functional Description
		Total Number	Description Note: The system consists of 4 divisions with 1 APRM unit and 4 LPRM units in each division.	
GAF/ST Module	HNS0341	4	- 1 module in an APRM unit	Power status and Input status indications. Gain Adjustment Factor (GAF) download and output to LPRM units
LVPS Module	HNS0500	40	- 2 modules in each unit	+5V and ±15V power supply to each module
AO Module	HNS0515	20	- 1 module in LPRM unit - 1 module in APRM unit	Analog outputs to the mimic display on the main control panel and the Transient Monitor
DIO Module	HNS0520	20	- 1 module in a LPRM unit - 1 module in a APRM unit	Discrete signal input and output module
TRN Module	HNS0531	28	- 1 module in a LPRM unit - 3 modules in a APRM unit	Optical data transmission module
RCV Module	HNS0541	24	- 1 module in a LPRM unit - 2 modules in a APRM unit	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

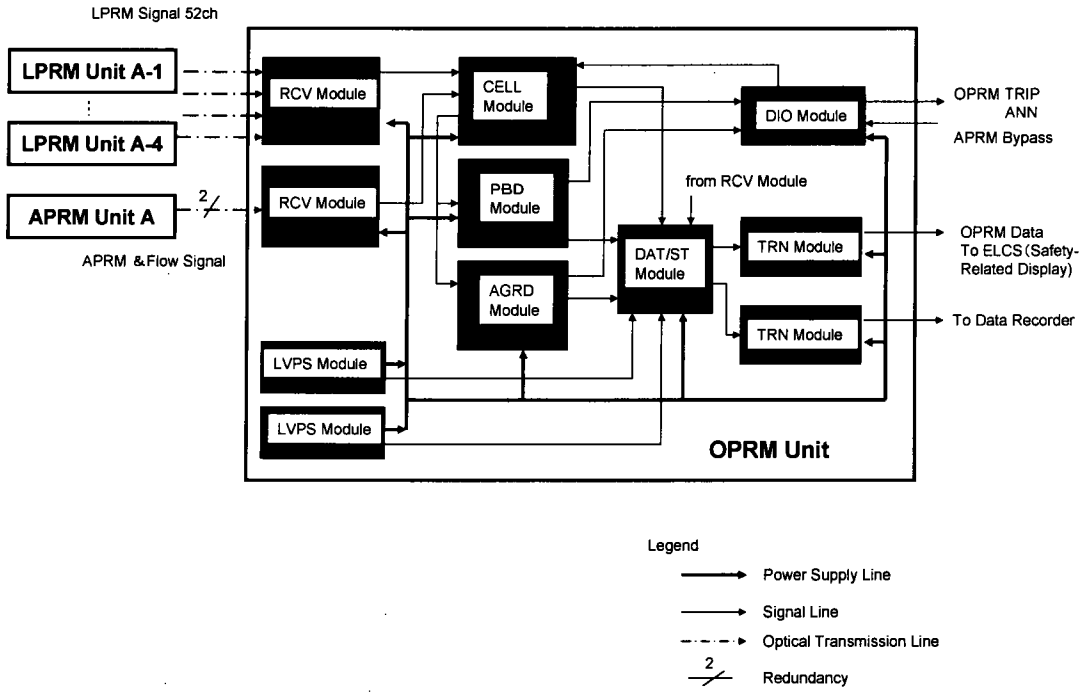


Figure II-2-16 Module and Unit Configuration of OPRM for ABWR

Table II-2-4 Module List of OPRM for ABWR

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-2-16		Functional Description
		Total number	Description Note: The system has 4 divisions with 1 OPRM unit in each division.	
CELL Module	HNS0400	4	- 1 module in each OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410	4	- 1 module in each OPRM unit	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420	4	- 1 module in each OPRM unit	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-2-16		Functional Description
		Total number	Description Note: The system has 4 divisions with 1 OPRM unit in each division.	
PBD Module	HNS0430	4	- 1 module in each OPRM unit	Period-based Detection Algorithm judgment is performed.
LVPS Module	HNS0500	8	- 2 modules in each OPRM unit	+5V and ±15V power supply to each module
DIO Module	HNS0520	4	- 1 module in each OPRM unit	Discrete signal input and output module
TRN Module	HNS0531	8	- 2 modules in each OPRM unit	Optical data transmission module
RCV Module	HNS0541	8	- 2 modules in each OPRM unit	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

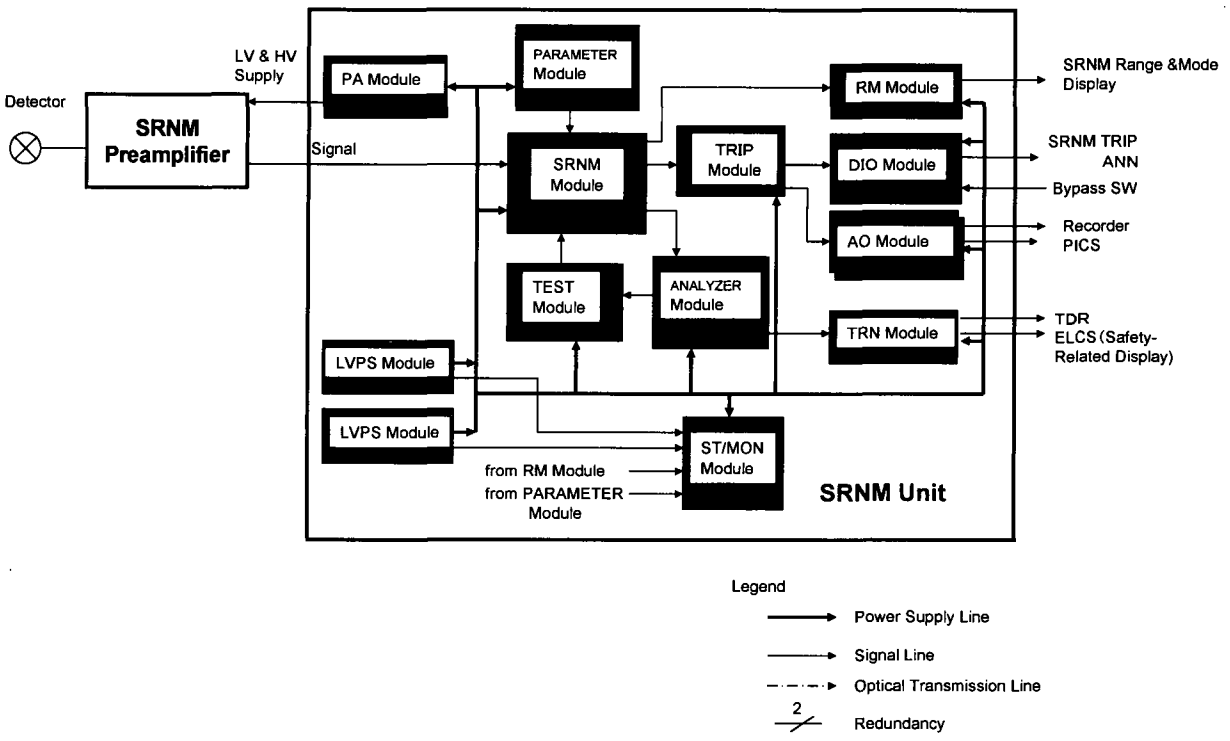


Figure II-2-17 Module and Unit Configuration of SRNM

Table II-2-5 Module List of SRNM

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-2-17		Functional Description
		Total Number	Description Note: The system has 8 channels with 1 SRNM unit in each channel.	
SRNM Module	HNS0101	8	- 1 module in a SRNM unit	SRNM signal processing function: Count rate, neutron flux, logarithmic % power, and linear % power are calculated from the neutron flux signal and are displayed them.
TRIP Module	HNS0117	8	- 1 module in a SRNM unit	Changing and display of trip setpoints and Trip judgment
PARAMETER Module	HNS0121	8	- 1 module in a SRNM unit	Display and changing of setpoints and parameter
ST/MON Module	HNS0131	8	- 1 module in a SRNM unit	Error diagnosis. Power voltage monitor display
ANALYZER Module	HNS0141	8	- 1 module in a SRNM unit	Transmission function with inspection tool for Plateau and/or Discrimination characteristics measurement
TEST Module	HNS0151	8	- 1 module in a SRNM unit	Trip and alarm test function
LVPS Module	HNS505	16	- 2 modules in a SRNM unit	+5V and ±15V power supply to each module Power Input 48V DC Type
AO Module	HNS0516	8	- 1 module in a SRNM unit	Analog outputs to the indicator and recorder on the main control panel
AO Module	HNS0518	8	- 1 module in a SRNM unit	Analog outputs to the process computer
DIO Module	HNS0520	8	- 1 module in a SRNM unit	Discrete signal input and output module
TRN Module	HNS0531	8	- 1 module in a SRNM unit	Optical data transmission module
RM Module	HNS0550	8	- 1 module in a SRNM unit	SRNM Range number and Mode signal output
PA Module	HNS0560	8	- 1 module in a SRNM unit - 1 PA module supplies the power to 1 SRNM preamplifier.	High Voltage and Low Voltage power supply are supplied to SRNM preamplifier.

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.
The configurations of SRNM for various BWR types are same. The only difference is the number of detectors.

II-2.2.2.5 Design Features in Focus

II-2.2.2.5.1 Interface with Field Sensors and Actuators

(1) LPRM UNIT

a. Analog Input Interface
The LPRM unit has analog input interface to receive one low level analog signal. The analog interface also provides power to the sensor.

Note: In ABWR, LPRM unit has fiber optic transmission input interface to accept LPRM data from the APRM.

b. Optical Transmission Output Interface
The LPRM unit has a fiber optic transmitter interface to provide broadcast data to external safety or non-safety systems, such as the Engineered Safety Features Logic and Control System and the Transient Data Recorder, respectively. However, these interfaces are plant specific interface and vary depending on the application.

(2) APRM UNIT

a. Analog Input Interface
The APRM unit has analog input interface to receive analog signals.

b. Analog Output Interface
The APRM unit has analog output interface to generate analog signals.

c. Discrete Input Interface
The APRM unit has discrete input interface to receive digital signals.

d. Discrete Output Interface
The APRM unit has discrete output interface to generate digital signals. The output interface requires external power.

e. Optical Transmission Input Interface
The APRM unit has fiber optic receivers to accept LPRM and FLOW data within a division.

Note: In ABWR, the APRM unit has fiber optic transmission input interface to accept

LPRM data from the core monitoring system.

f. Optical Transmission Output Interface
The APRM unit has fiber optic transmitter interfaces to provide broadcast data to the OPRM and other external safety or non-safety systems. However, these interfaces are plant specific interface and vary depending on the application.

(3) OPRM Unit

a. Discrete Input Interface
The OPRM unit has discrete input interface to receive digital signal.

b. Discrete Output Interface
The OPRM unit has discrete output interface to generate digital signals.

c. Optical Transmission Input Interface
The OPRM unit has fiber optic receivers to accept LPRM data within a division.

Optical Transmission Output Interface
The OPRM unit has fiber optic transmitter interfaces to provide broadcast data to other external safety or non-safety systems.

(4) SRNM Unit

a. Analog Input Interface
The SRNM unit has analog input interface to receive an analog input from an SRNM pre-amplifier.

b. Analog Output Interface
The SRNM unit has analog output interface to generate analog signals representative of the current neutron flux.

c. Discrete Input Interface
The SRNM unit has discrete input interface to the bypass switch.

d. Discrete Output Interface
The SRNM unit has discrete output interface to generate digitals. The output interface requires external power.

e. Optical Transmission Output Interface

The SRNM unit has fiber optic transmitter interfaces to provide broadcast data to other external safety or non-safety systems.

II-2.2.2.5.2 Power Supply

NMS has redundant LVPS power supply module in the following units:

- Flow Unit
- LPRM Unit
- APRM Unit
- OPRM Unit
- SRNM Unit

The LVPS Module supplies +5V DC and ±15V DC.

The requirements for external power source are described in Section II-2.2.3.1.3

II-2.2.2.5.3 Annunciation of Failures

The NMS generates a divisional Inoperative signal when faults occur that affect the execution of the safety functions of the NMS. APRM Unit, OPRM Unit and SRNM Unit have LED indicators on their front panels to show the generation of each Inoperative signal The LPRM Inoperative signals are transferred to the APRM unit through communication link. The APRM Inoperative, the OPRM Inoperative, and SRNM Inoperative Signals are transferred by relay to the RTIS to be used in the voting for a the rector trip.

All Inoperative Signals are transferred to safety and non-safety systems display over unidirectional fiber communication links. The conditions for generating each Inoperative Signal is defined in the Equipment Design specifications for each application.

II-2.2.2.5.4 Boundary between Safety and Non-Safety

The NMS provides data to non-safety system over qualified isolators using hardwired relays and unidirectional fiber optic links. The NMS also has an incoming fiber optic communication link for calibration data. The calibration data transfer occurs only when the division is bypassed, administratively controlled keys have been inserted in the unit, the MCR operator has pressed a key-lock enabled switch to request such data, and the MCR operator has verified each piece of

data to match the values calculated by the core monitoring computer. This process is then repeated for each division, as required. This process is described in Section II-2.2.3.2.2.

Figure II-2-14 through Figure II-2-17 depict these boundary points.

II-2.2.3 FPGA Application Principles

The purpose of this section is to consolidate information regarding key design features of the safety-related applications as they would be implemented by NRW-FPGA-based platforms. The scope of this section is limited to safety-related applications to implement the design and functionality of the Reactor Trip and Isolation System (RTIS) and the Neutron Monitoring System (NMS).

The FPGA-based platform has been designed in large part based on four essential design principles: (1) redundancy, (2) independence, (3) the need for defined determinism in data processing and communication, and (4) implementation of a diversity and defense-in-depth (D3) philosophy, as well as one subjective attribute–simplicity. The four principles and one attribute are embodied in the underlying basis of IEEE Std 603 (Reference (a36)).

The discussion in this section is structured to summarize the key design features of the FPGA-based platform to address the above in the design of application systems such as RTIS and safety-related NMS.

II-2.2.3.1 Redundancy

The RTIS and safety-related NMS implementation in the FPGA platform conforms to the Single Failure Criterion (Clause 5.1) of IEEE Std 603 (Reference (a36)). To meet this criterion, the redundancy designed into each of these systems is discussed below.

II-2.2.3.1.1 Reactor Trip and Isolation System

To permit surveillance testing or maintenance, bypassing of any single division of sensors (i.e., those sensors whose status is part of a two-out-of-four logic) can be accomplished by means of the manually operated bypass. This Division-of-Sensors Bypass bypasses the divisional DTF and leaves the DTF's output in a non-tripped state. The Division-of-Sensors Bypass is designed to allow only one division to be bypassed at a time. When such bypass is made, all four divisions of two-out-of-four voting logic become two-out-of-three voting logic, a credible failure can occur, and RTIS can still meet the IEEE Std 603 (Reference (a36)) Single Failure Criterion

(Clause 5.1).

Bypassing a division of trip logic (i.e., taking a logic channel out of service) can be accomplished by means of the Trip-Logic-Output Bypass. When a Trip-Logic-Output Bypass is in effect, the TLF trip output in the bypassed division is inhibited from affecting the output load drivers, maintaining that division's load drivers in an energized state. Only one divisional TLF can be bypassed by the Trip-Logic-Output Bypass. The two-out-of-four voting logic arrangement of output load drivers for the RPS and MSIV functions effectively becomes two-out-of-three voting logic. A credible failure can occur with one divisional TLF bypassed, and RTIS can still meet the IEEE Std 603 Single Failure Criterion (Clause 5.1).

II-2.2.3.1.2 Safety-Related Neutron Monitoring System

There are four redundant, independent channels of APRM in the ABWR design and six channels of APRM in BWR designs, with each channel providing a trip signal to the RPS. In the ABWR design, any two of the four APRM channels that indicate an abnormal condition will initiate a reactor scram through the RPS two-out-of-four trip logic. In BWR designs, six APRM channels are divided into two groups where each group consists of three APRM channels. When more than one APRM channel provides a trip signal in both groups, a reactor scram is initiated through RPS function. The redundancy criteria are met so that in the event of a single failure under permissible APRM channel bypass conditions, a scram signal will still be generated in the RPS as required. Thus, the IEEE Std 603 Single Failure Criterion (Clause 5.1) is satisfied.

There are independent and redundant channels of OPRM. The above APRM channel redundancy condition also applies to OPRM channels. Bypassing a division of APRM bypasses the same division of OPRM. The OPRM trip outputs are separate from the APRM trips to RPS and use similar RPS two-out-of-four voting logic as the APRM, satisfying the IEEE Std 603 Single Failure Criterion (Clause 5.1). The arrangement and assignment of LPRMs provide core regional monitoring by redundant OPRM channels.

II-2.2.3.1.3 Power Supply Redundancy

Power supply redundancy of the RTIS and the safety-related portion of NMS are provided through four redundant, Class 1E, 120V AC power sources in the ABWR design. In BWR-3, 4 and 5, power supply redundancy of the RTIS and the safety-related portion of NMS are provided through two redundant, Class 1E, 120V AC power sources. The power sources provide an uninterruptible supply of electrical power, one to each division. A loss of one power supply will

neither inhibit protective action nor cause a scram, satisfying the IEEE Std 603 (Reference (a36)) Single Failure Criterion (Clause 5.1).

II-2.2.3.2 Independence

Each division of RTIS and NMS can accomplish its safety function regardless of the operability or adverse impact of other redundant divisions or other systems. For RTIS and NMS, functional, physical, electrical, and communication independence exists between redundant safety-related divisions, between each safety-related division and other divisions in other safety-related systems, and between safety-related systems and non-safety-related systems.

Data independence is exhibited in RTIS and NMS in that only votes to trip and status information are provided across divisional boundaries. The data link information is transmitted in packets with a fixed length, fixed content, and predefined format. Failures in the communication links do not adversely affect operation of the divisions receiving malformed, incorrect, or inappropriate data messages.

II-2.2.3.2.1 Physical and Electrical Independence

Each of the divisions of safety-related NMS and RTIS are physically separated from the other redundant divisions. NMS and RTIS comply with the criteria set forth in IEEE Std 603 (Reference (a36)), Clause 5.6, and follow the guidance of Regulatory Guide 1.75 (Reference (a9), which endorses IEEE Std 384 (Reference (a34)). Class 1E circuits are identified and separated from redundant circuits and non-Class 1E circuits. Qualified electrical isolation devices are provided in the design when an interface exists between redundant Class 1E divisions and between non-Class 1E and Class 1E circuits.

Physical and electrical independence of the instrumentation devices of the system is provided by channel independence for sensors exposed to each process variable. Trip logic outputs are separated in the same manner as the channels. Signals between redundant RPS divisions are electrically and physically isolated by Class 1E isolators, including fiber optic cables. Figure II-2-18 provides a high-level overview of the RTIS safety function communication between redundant divisions.

II-2.2.3.2.2 Communications Independence

For the FPGA-based systems, the signals from the instrumentation are hardwired to the RTIS and

NMS channels. The modules used to construct the RTIS and NMS systems communicate using dedicated communication links internal to the division. Each communication link has its own independent communications buffer.

The communication data links to be provided to systems external to the FPGA-based system use uni-directional fiber optic communication links from each division. The communication links provide only fixed data sets to the non-safety-related systems, provide Class 1E to non Class 1E electrical and functional isolation, and offer no possibility of data transfer from the non-safety to safety equipment during normal operation. The NMS allows non-safety calibration data to be transferred only to one channel of NMS when that channel is out of service.

The FPGA-based system includes self-diagnostic functions that continuously verify proper FPGA and communications performance, and provide outputs used to alert the operator. If a failure is detected, the division is marked as inoperable (i.e., tripped). When the predetermined divisions are in a tripped state, the voting logic in the RPS will cause the safety function to occur. For example, the two-out-of-four voting logic will cause the safety action to occur (e.g., two tripped RPS divisions will scram the reactor) in the ABWR design.

Each RTIS and safety-related NMS division has fiber optic communication links to the other safety systems in the same division. The links provide a qualified and isolated, point-to-point, uni-directional communication path to preserve independence between the originating RTIS/NMS division and the other safety system.

Each RTIS and safety-related NMS division communicates data and status to the non-safety-related systems through dedicated communication interfaces in each system's modules. The communication interface for each division consists of uni-directional fiber optic communication links that broadcast fixed data sets from each safety division to the non-safety-related systems. The communication interface is designed to prevent any data transfer from the non-safety systems to the originating safety-related division. The fiber optic cable provides electrical isolation and the safety-related transmitter provides the functional isolation.

No other capabilities exist for communication with external devices. Communications information specific to RTIS and NMS are discussed briefly below in the following subsections.

II-2.2.3.2.3 Reactor Trip and Isolation System

The DTF communicates its division's trip status information to the TLF by fiber optic

communication links. Because individual divisional trip determinations must be shared between divisions to support two-out-of-four voting logic for divisional trip outputs, the DTF also communicates its trip status information to the other three divisional TLFs by means of isolated fiber optic communication links. The links provide a qualified and isolated, point-to-point, uni-directional communication path between divisions to preserve divisional independence.

Data communicated between RTIS divisions for use in two-out-of-four voting has their own independent communication buffer in the receiving division's TLF for each set of incoming data. Only discrete (vote to trip only) information is transmitted across division boundaries in fixed format, fixed length, and pre-defined messages. This preserves data independence between divisions in accordance with IEEE Std 603 (Reference (a36)) Clause 5.6.

In each division, the TLF communicates trip status information to the OLU by uni-directional fiber optic communication links. The OLU in each division communicates with the Load Drivers (LDs) that initiate the safety function. The LD-RPSs are hardwired to its scram solenoid valves, and the LD-MSIVs are hardwired to its MSIV solenoid valves.

II-2.2.3.2.4 Safety-Related Neutron Monitoring System

The safety-related NMS consists of LPRM, APRM, and SRNM subsystems. OPRM is a functional subsystem of the APRM. There is no communication between redundant divisions in the safety-related NMS. All trip voting is performed in RTIS.

The LPRM monitors neutron flux in the power range. For each of the NMS divisions, the LPRMs monitor neutron flux levels from the hardwired LPRM detector inputs. Each division has a number of LPRM detectors and LPRM modules that provide data to the APRM and OPRM in its division. The number of LPRM detectors is different depending on the BWR model. The LPRM modules in one division communicate internally with the APRM in that division over uni-directional fiber optic communication links, providing fixed data sets of LPRM information.

For each NMS division, the APRM uses the divisional LPRM detectors and a divisional core plate differential pressure input. When an APRM division detects a trip condition, it provides a hardwired, discrete (vote to trip only) signal to all divisions of RTIS or equivalent existing RPS. The hardwired signals are electrically isolated.

For each NMS division, the divisional OPRM receives local power level data from the divisional LPRMs and core flow and average power level data from the same divisional APRMs over uni-directional fiber optic communication links. The divisions of the OPRM trip protection

algorithm independently detect thermal hydraulic instability and provide hardwired, discrete (vote to trip only) signals to all divisions of the RTIS's OPRM voter logic or voter logic to be provided in the existing RPS.

The divisional SRNM monitors neutron flux while in the start-up range. Each SRNM receives input from a hardwired detector. SRNM detectors are distributed throughout the reactor core. Each SRNM detects high neutron flux or a short period condition and provides a hardwired, discrete (vote to trip only) signal to all division of the RTIS TLFs or existing RPS for reactor trip determination.

The NMS also includes an off-line capability to transfer calibration data from a non-safety related source to the NMS. When NMS is online and not bypassed, data transfer to NMS from the non-safety system is blocked by a key lock switch in each LPRM module. The APRM Unit and the LPRM unit have a key switch to select a mode when downloading the calibration data to prevent unauthorized downloads When calibration data is to be transferred, the NMS division desired to receive the information must be bypassed by the control room operator, placed in an inoperative status, and the key lock switch on that NMS division must be enabled to request and allow the data transfer. Only a limited data set in a predefined format will be accepted by the NMS. Before the data can be used by the NMS, manual verification and acceptance of each data item at the NMS human-system interface is required. No online data transmission from non-safety systems to safety-related systems is permitted.

The user's manual that defines the methods of the operations to be used to download and install the calibration data will be provided.

II-2.2.3.3 Determinism

The response time requirement for each NMS and RTIS safety-related function is determined by the safety analysis. The response time must be predictable and repeatable to be considered deterministic. The response time for all NMS and RTIS safety functions is deterministic. A description of the FPGA platform features that make the NMS and RTIS response deterministic is provided below.

The FPGA-based system designs use multiple FPGAs on some modules. To enhance testability and reduce undesirable circuit behavior, the basic architecture within each FPGA is a clocked sequential circuit, with periodic synchronizing registers within the FPGAs. Each FPGA only starts processing data when data is transferred into that FPGA, and sends data to the next FPGA or module when processing is complete. Thus, the functions in a given module execute in

sequence that is inherently deterministic based on the clocked sequence. The first FPGA completes its function, and then provides data to the next FPGA. When that FPGA completes its function, it provides data to the next FPGA. In addition, when all signal processing FPGAs have finished passing data to the next, the signal processing watchdog timer on the module resets and restarts timing. Failure of a signal processing FPGA to complete and pass data to the next FPGA will result in all subsequent FPGAs on that module failing to start. If this occurs in the FPGAs that implement the signal processing and thus the safety functions, then the module is marked as failed, the watchdog timer times out, resulting in the tripped division, and an alarm is provided to the operator. Predetermined number of tripped divisions will result in a reactor scram via the voting arrangement. In the ABWR design, two tripped divisions will result in a reactor scram via the two out of four voting arrangement. The watchdog timer on each module is designed to be fully testable.

Because FPGAs are arrays of logic cells and registers, each cell connected in series adds defined delay to the logic circuit. As a result, the logic within each FPGA is designed, verified, and validated to ensure operation within timing constraints under expected operating conditions. The clocked synchronous design is used within each FPGA to avoid timing errors and to ensure timing constraints are satisfied. For synchronous design, changes of state within the FPGA occur only at selected times, controlled by a timing signal. The logic within each FPGA is designed to ensure that the design provides adequate shaping on the inputs to the FPGA.

To avoid timing errors within FPGAs, analysis and simulation are performed during the design process. This two-part process includes static timing analysis and dynamic timing simulation. Static timing analysis demonstrates that the setup and hold times on each path within the FPGA design are within predetermined parameters. Software tools used to perform the static timing analysis also are used to evaluate the propagation delay to each element in the code to confirm each timing path in the code is within predetermined parameters. Also, a diverse set of dynamic simulation software tools are used to validate the design, using predetermined, accurate propagation delays, which are set based on the chosen cells and paths within the FPGA. These analyses provide data to the designer to verify that appropriate logic implementation has been achieved, eliminating any potential concerns regarding signal races, signal setup and hold times, and clock skew. A report is generated for implementation including safety analyses.

The communication protocols used in the FPGA platforms are deterministic because they are pre-defined, fixed length, fixed format, and generated at specific times in the FPGA logic execution. The communication links that perform safety functions include data and time out error checking to ensure determinism. All detected errors are alarmed. The communication

protocols and logic in the communication receivers include self-diagnostics that will generate module failure signals upon detection of communication failures, alerting operators.

In summary, the FPGA-based, safety-related NMS and RTIS are deterministic. The FPGA platform does not utilize any non-deterministic data communication, non-deterministic computation, interrupts, multitasking, dynamic scheduling, or event driven design. The logic design of the FPGA circuits is fixed and clocked. The response times for the system elements, including architecture, communications (including timing and loading) and processing elements are tested to verify that the systems' performance characteristics are consistent with the safety requirements established in the design basis for these systems. The analyses are performed to satisfy the design timing requirements set forth in Clause 4.10 of IEEE Std 603 (Reference (a36)). A report is generated to demonstrate the adequacy of the timing analysis.

II-2.2.3.4 Diversity

Diversity is the responsibility of the overall NSSS designer or licensee. The FPGA platform does not provide diversity within a given channel by itself. An example diversity strategy for the ABWR design is discussed below.

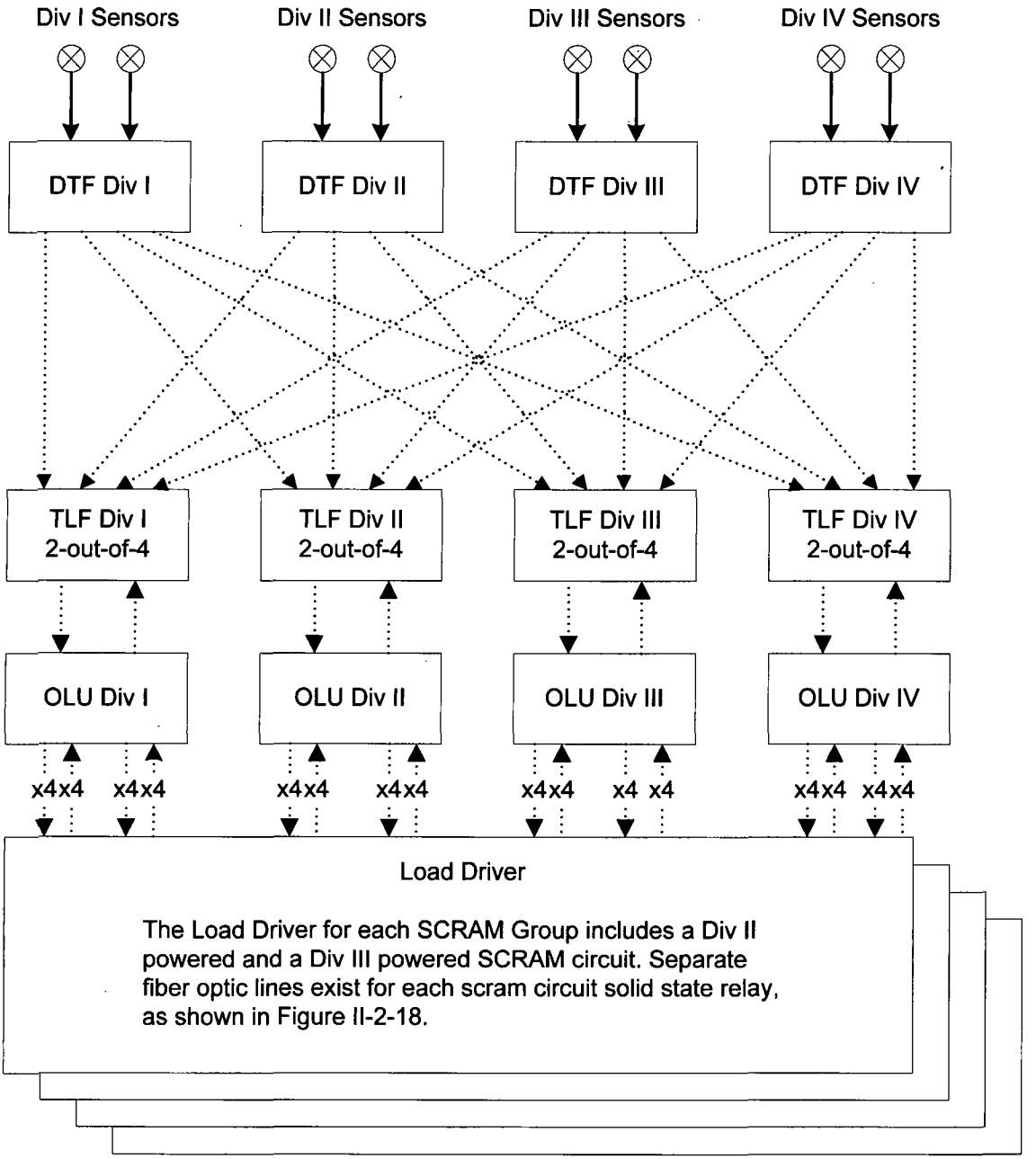
The RTIS and NMS platforms satisfy all IEEE Std 603 (Reference (a36)) requirements and are developed using a robust hardware/software development process described in Section 4 of this report that meets Tier 1 Section 3.4B of the ABWR DCD (Reference (a49)), NUREG-0800 (Reference (a4)), and BTP 7-14 (Reference (a5)).

The RTIS and NMS are diverse to the Engineered Safety Features (ESF) Logic and Control System (ELCS), which actuates the ESF actions. RTIS and NMS are implemented through FPGA-based platforms, which use configurable logic devices. The ELCS equipment could be the hard wired logic system or digital system using diverse technology from the FPGA, like microprocessor-based controllers where the logic is implemented in software. The RTIS and NMS shall be diverse from the non-safety platforms used for the Nuclear Steam Supply System (NSSS) and Balance of Plant (BOP) control and display.

The design includes features that enhance the diversity of RPS and MSIV closure functions, including a diverse system for mitigation of Anticipated Transient Without Scram (ATWS) events. The diversity should be maintained through the combination of other diverse safety systems, a diverse system for mitigation of Anticipated Transient Without Scram (ATWS) events, and/or the hardwired control and display of the selected ECCS control functions.

II-2.2.3.5 Simplicity

The FPGA-based platform that implements safety-related NMS and RTIS is designed for simplicity. The systems have some analog circuits that process detector signals as inputs. The analog signals are converted to digital signals, and then processed by FPGA circuits. The FPGA circuits are constructed of discrete logic blocks that are similar to older, analog and discrete relay circuits in existing operating plants. The FPGA-based DI&C implements the required functionality in fixed gates with deterministic timing that cannot be changed after being programmed at the vendor facility. Toshiba has not created or designed systems that require priority modules. The FPGA-based platform is designed such that non-safety-related equipment cannot control or influence the operation of safety-related functions; non-safety-related functions are not performed in the safety-related equipment, which simplifies the safety-related equipment by elimination of non-essential functionality. Data can only be transferred from each safety division over independent, uni-directional communication links to non-safety-related equipment for several purposes, including diverse display of safety data, preserving data for historical purposes, and performing channel cross checks. This transfer of data shifts these complex activities to the non-safety equipment, preserving simplicity in the safety systems. The only communication between divisions is to vote on trip logic decisions in RTIS; NMS has no inter-division communication. Thus, the RTIS and NMS platform design satisfies the subjective attribute of simplicity.



Notes:
1) RTIS-MSIV equipment Is similar.
2) Not all communication links are shown.
3) Scram solenoids and hardwired connections to scram solenoids are not shown.
4) Fiber Optic communication is denoted by dotted lines and hardwired communication is denoted by solid lines.

Figure II-2-18 RTIS Interdivision Communication Simplified Block Diagram (ABWR)

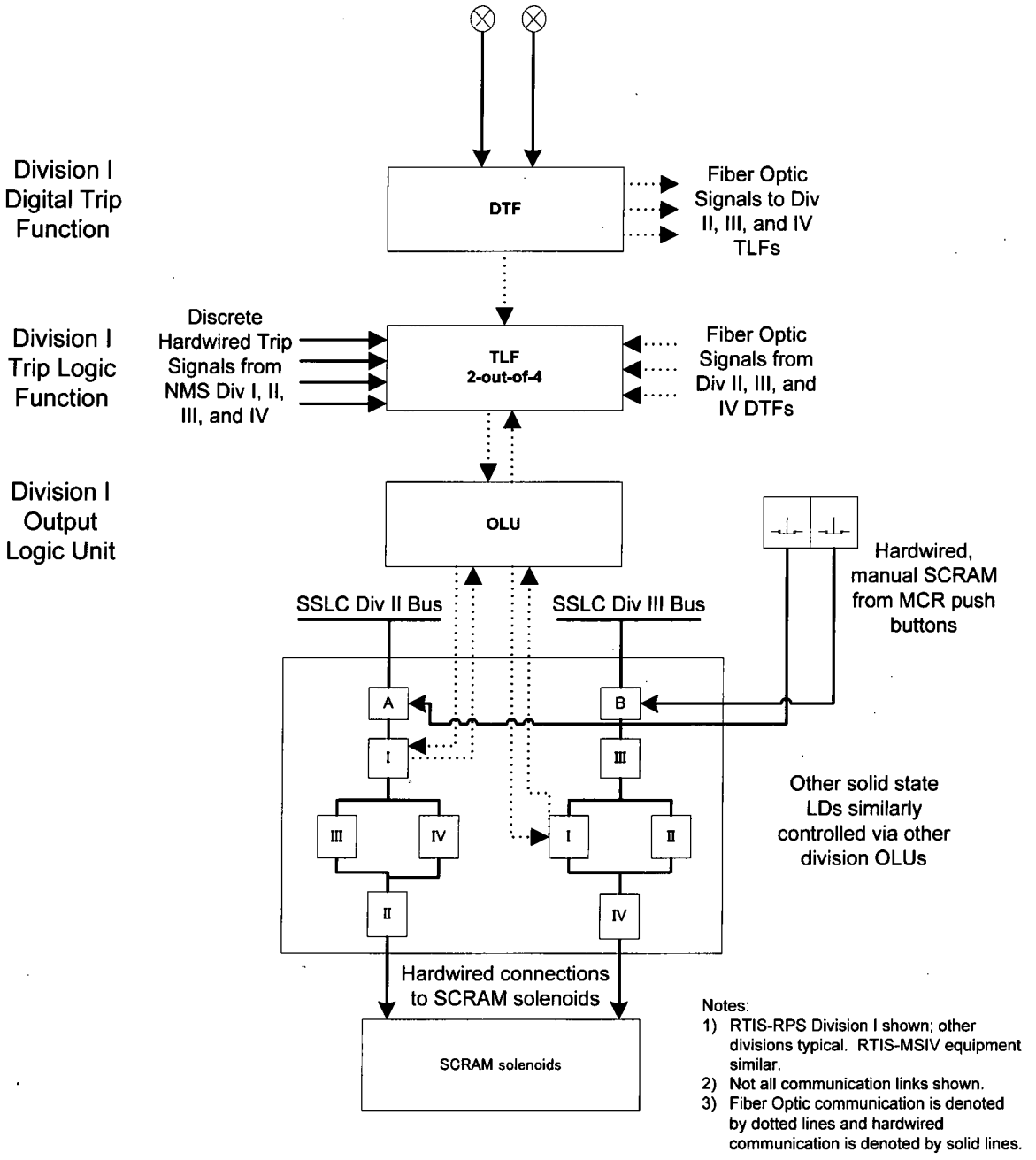


Figure II-2-19 RTIS Divisional Simplified Block Diagram

II-2.2.4 Qualified Module List

Table II-2-6 lists all the modules in NRW-FPGA based Safety-Related I&C Systems and the qualified modules reported in this LTR.

Table II-2-6 also indicates that multiple IO Modules and Communication Modules are designed and used commonly in multiple Units. In this table, modules that have been completely qualified are shown in bold font and highlighted in light dot pattern. Modules that are being qualified are shown in bold and italic font and highlighted in dark dot pattern. Modules with no backgrounds may require additional qualification in the future. The amount of additional qualification will be based on the differences in these modules and modules currently qualified. Existing qualifications will be used to the maximum extent practicable. For example, a future development of an RTIS module would likely require additional electromagnetic compatibility testing but existing seismic and/or environmental qualification may be used with justification depending on the significance of the changes.

Table II-2-7 provides the cross-references that show the systems and the units where each module is used.

Table II-2-6 List of All Modules and Qualified Modules

System	Unit	Module							
		I/O Function		Comunication Function		Signal Processing		Power Supply	
		Module Name	Type Number	Module Name	Type Number	Module Name	Type Number	Module Name	Type Number
PRM	LPRM	DIO	HNS520	TRN	HNS530	LPRM	HNS013	LVPS	HNS500
		AO	HNS515	RCV	HNS540	STATUS	HNS093		
		AO	HNS518			BLANK	HNS490		
						MUX	HNS260		
	LPRM/APRM	DIO	HNS520	TRN	HNS530	LPRM	HNS013	LVPS	HNS500
		AO	HNS515	RCV	HNS540	APRM	HNS020		
		AO	HNS516			STATUS	HNS091		
		AO	HNS518						
	FLOW	DIO	HNS520	TRN	HNS530	SQ-ROOT	HNS030	LVPS	HNS500
		AO	HNS516			FLOW	HNS040		
		AO	HNS517			STATUS	HNS093		
		AO	HNS518						
PRNM for ABWR	LPRM	DIO	HNS520	TRN	HNS530	LPRM	HNS0302	LVPS	HNS500
		AO	HNS515	RCV	HNS540	CAL/ST	HNS0330		
	APRM	DIO	HNS520	TRN	HNS530	APRM	HNS0311	LVPS	HNS500
		AO	HNS515	RCV	HNS540	FLOW	HNS0320		
						GAF/ST	HNS0341		
OPRM	OPRM	DIO	HNS520	*TRN*	*HNS531*	*CELL*	*HNS0400*	LVPS	HNS500
				RCV	*HNS541*	*AGRD*	*HNS0420*		
						PBD	*HNS0430*		
						DAT/ST	*HNS0410*		
SRNM	SRNM	DIO	HNS520	TRN	HNS530	SRNM	HNS0101	LVPS	HNS500
		AO	HNS516			PARAMETER	HNS0121	LVPS	HNS505
		AO	HNS518			TRIP	HNS0117		
		RM	HNS0550			ST/MON	HNS0131		
		PA	HNS0560			ANALYZER	HNS0141		
						TEST	HNS0151		
RTIS	DTF-RPS	DIC1	HNS0730	TRN	HNS530	AITRIP1	HNS1100	LVPS	HNS500
		DOC1	HNS0740	RCV	HNS540	DTUCA1	HNS1141		
						STR1	HNS1163		
	DTF-MSIV	DIC1	HNS0730	TRN	HNS530	AITRIP1	HNS1100	LVPS	HNS500
		DOC1	HNS0740	RCV	HNS540	DTUCA2	HNS1142		
						STR1	HNS1164		
	DTF-MSIV-S			TRN	HNS530	AITRIP1	HNS1100	LVPS	HNS500
						MLTPL2	HNS1170		
						STR1	HNS1167		
	TLF-RPS	DIC1	HNS0730	TRN	HNS530	TLUCA1	HNS1151	LVPS	HNS500
		DOC1	HNS0740	RCV	HNS540	STR1	HNS1165		
						TLUBF1	HNS1180		
	TLF-MSIV	DIC1	HNS0730	TRN	HNS530	TLUCA2	HNS1152	LVPS	HNS500
		DOC1	HNS0740	RCV	HNS540	STR1	HNS1166		
	OLU-RPS	LOM2_2	HNS1202					LLN1	HNS1220
		LOI1	HNS1211					LHI1	HNS1230
								LHO1	HNS1240
								SLD1	–
	OLU-MSIV	LOM2_1	HNS1201					LLN1	HNS1220
		LOI1	HNS1211					LHO1	HNS1240
		LOI1	HNS1212					SLD1	–
SPTM	SPTM	AO	HNS517	TRN	HNS530	AITRIP	HNS1100	LVPS	HNS500
		DOC1	HNS0740	RCV	HNS540	SPTAVE1	HNS1110		
						SPTSEL1	HNS1120		
						STR1	HNS1161		
	SPTM-S			TRN	HNS530	AITRIP	HNS1100	LVPS	HNS500
						MLTPL1	HNS1130		
						STR1	HNS1162		

Qulified Module *Next EQ/EMC Testing*

Table II-2-7 Cross Reference Table of All Modules

Module Name	Type Number	Has FPGA Module?	System used	Unit used
LPRM	HNS013	yes	PRM(BWR-2,3,4,5,6)	LPRM, LPRM/APRM, FLOW, SRNM
LPRM	HNS0302	yes	PRM for ABWR	LPRM(ABWR)
APRM	HNS020	yes	PRM(BWR-2,3,4,5,6)	LPRM/APRM
APRM	HNS0311	yes	PRM for ABWR	APRM(ABWR)
SQ-ROOT	HNS030	yes	PRM(BWR-2,3,4,5,6)	FLOW
FLOW	HNS040	yes	PRM(BWR-2,3,4,5,6)	FLOW
FLOW	HNS0321	yes	PRM for ABWR	APRM(ABWR)
STATUS	HNS091	yes	PRM(BWR-2,3,4,5,6)	LPRM/APRM
STATUS	HNS093	yes	PRM(BWR-2,3,4,5,6)	LPRM, FLOW
MUX	HNS260	yes	PRM(BWR-2,3,4,5)	LPRM
CAL/ST	HNS0330	yes	PRM for ABWR	LPRM(ABWR)
GAF/ST	HNS0341	yes	PRM for ABWR	APRM(ABWR)
TRN	HNS530	yes	PRM(BWR-2,3,4,5,6)	LPRM, LPRM/APRM, FLOW
TRN	HNS0531	yes	OPRM, PRM(BWR-2,3,4,5,6), PRM for ABWR, SRNM, RTIS, SPTM	OPRM, LPRM, LPRM/APRM, FLOW, LPRM(ABWR), APRM(ABWR), SRNM, DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S
RCV	HNS540	yes	PRM(BWR-2,3,4,5,6)	LPRM, LPRM/APRM
RCV	HNS0541	yes	OPRM, PRM(BWR-2,3,4,5,6), PRM for ABWR, RTIS, SPTM	OPRM, LPRM, LPRM/APRM, LPRM(ABWR), APRM(ABWR), DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, SPTM
LVPS	HNS500	no	PRM, PRM for ABWR, OPRM, SRNM, RTIS, SPTM	LPRM, LPRM/APRM, FLOW, LPRM(ABWR), APRM(ABWR), OPRM, SRNM, DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S
AO	HNS515, 516, 517, 518	no	PRM(BWR-2,3,4,5,6), PRM for ABWR	LPRM, LPRM/APRM, LPRM(ABWR), APRM(ABWR), FLOW, SRNM, SPTM
DIO	HNS520	no	PRM(BWR-2,3,4,5,6), PRM for ABWR, OPRM, SRNM	LPRM, LPRM/APRM, FLOW, LPRM(ABWR), APRM(ABWR), OPRM, SRNM
BLANK	HNS490	no	PRM(BWR-2,3,4,5,6)	LPRM
CELL	HNS0400	yes	OPRM	OPRM
DAT/ST	HNS0410	yes	OPRM	OPRM
AGRD	HNS0420	yes	OPRM	OPRM
PBD	HNS0430	yes	OPRM	OPRM
SRNM	HNS0101	yes	SRNM	SRNM
TRIP	HNS0117	yes	SRNM	SRNM
PARAMETER	HNS0121	yes	SRNM	SRNM
ST/MON	HNS0131	yes	SRNM	SRNM
ANALYZER	HNS0141	yes	SRNM	SRNM
TEST	HNS0151	yes	SRNM	SRNM

Module Name	Type Number	Has FPGA Module?	System used	Unit used
LVPS	HNS505	no	SRNM	SRNM
RM	HNS0550	no	SRNM	SRNM
PA	HNS0560	no	SRNM	SRNM
AITRIP1	HNS1100	yes	RTIS, SPTM	DTF-RPS, DTF-MSIV, DTF-MSIV-S, SPTM, SPTM-S
SPTAVE1	HNS1110	yes	SPTM	SPTM
SPTSEL1	HNS1120	yes	SPTM	SPTM
MLTPL1	HNS1130	yes	SPTM	SPTM-S
DTUCA1	HNS1141	yes	RTIS	DTF-RPS
DTUCA2	HNS1142	yes	RTIS	DTF-MSIV
TLUCA1	HNS1151	yes	RTIS	TLF-RPS
TLUCA2	HNS1152	yes	RTIS	TLF-MSIV
STR1	HNS1161, 1162, 1163, 1164, 1165, 1166, 1167	no	SPTM, RTIS	SPTM, SPTM-S, DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, DTF-MSIV-S
MLTPL2	HNS1170	yes	RTIS	DTF-MSIV-S
TLUBF1	HNS1180	yes	RTIS	TLF-RPS
LOM2_1	HNS1201	yes	RTIS	OLU-MSIV
LOM2_2	HNS1202	yes	RTIS	OLU-RPS
LOM2_1	HNS1203	yes	RTIS	OLU-MSIV
LOM2_2	HNS1204	yes	RTIS	OLU-RPS
DIC1	HNS0730	no	RTIS	DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV
DOC1	HNS0740	no	RTIS	DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, SPTM
LOI1	HNS1211,1212	no	RTIS	OLU-RPS, OLU-MSIV
LLN1	HNS1220	no	RTIS	OLU-RPS, OLU-MSIV
LHI1	HNS1230	no	RTIS	OLU-RPS
LHO1	HNS1240	no	RTIS	OLU-RPS, OLU-MSIV

Appendix II-A. Application Guide

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II-A-1 Introduction

This application guide provides generic guidelines and data for applying any Toshiba Non-Rewritable Field Programmable Gate Array (NRW-FPGA) based safety-related system in nuclear power plant. The guidance provided in this document is intended to simplify use and application of the Toshiba NRW-FPGA-based system by consolidating design requirements, operational limitations, and other important data derived from the generic qualification program. The Toshiba NRW-FPGA-based system has been used to build Power Range Neutron Monitoring (PRM) systems for Boiling Water Reactor-5 (BWR-5); Power Range Neutron Monitoring (PRNM) systems for Advanced Boiling Water Reactors (ABWR), Startup Range Neutron Monitoring (SRNM) system for an ABWR and BWR-5, and a Reactor Trip and Main Steam Isolation System (RTIS) for an ABWR. Using the hardware and modified programmable logic, the NRW-FPGA-based systems can be supplied for PRM and reactor trip systems for BWR-3, BWR-4, BWR-5, and BWR-6. The NRW-FPGA-based equipment can also be used in radiation monitoring system (RMS) applications at any nuclear facility. This application guide does not contain hardware or programmable logic to support radiation monitoring systems.

The requirements and limitations of each system shall be considered when the system is applied to a plant-specific application. Where a Toshiba NRW-FPGA-based system is installed to replace existing equipment in multiple channels (divisions), existing channel independence and separation shall not be compromised, and, depending on rules and regulations, additional independence and separation can be supported in the Toshiba-supplied systems.

Guidelines are provided for design, licensing, installation, operation, and maintenance of the system. Many of the guidelines in this document are interrelated. As an example, consider the generation of fault alarms. The fault alarm has implications in design, operating and maintenance procedures, plant interface, main control room impacts, and several other seemingly unrelated topics, including system power supply and core damage frequency. Therefore, the guidelines should be considered as a whole, rather than in separated, individual pieces.

In addition to the guidelines presented in this document, the system specific manufacturer's recommendations in the users manuals and/or System Operations and Maintenance (O&M) manuals provided by Toshiba shall be implemented.

II-A-2 System Design Guidance

The system- and plant-specific User's Manual and/or System O&M Manual provide technical information on the application of the NRW-FPGA-based systems, and on operation and maintenance of the systems. This application guide provides generic guidelines and data for applying the NRW-FPGA-based safety-related system in nuclear power plant.

II-A-2.1 Power Supply

Each system has been validated to operate from redundant AC sources operating between 90 to 150V AC and over a frequency range of 57 to 63 Hz.

During system startup, the power on reset circuit for each module monitors the input voltages and the FPGAs are held in a reset state until the power supply voltages are within specified bounds. This prevents spurious signals on the device outputs from occurring before the appropriate stable module performance is achieved.

The User's Manual and/or System O&M Manual provide power supply requirements specific to system based on each system's System Design Description (SDD) and Equipment Design Specification (EDS) if necessary.

II-A-2.2 NRW-FPGA-Based System Configuration

The User's Manual and/or System O&M Manual provide each system configuration information based on the SDDs, IEDs, IBDs and EDSs for each system.

II-A-2.3 NRW-FPGA-Based System Interfaces

The User's Manual and/or System O&M Manual provide the interface specification for each unit in the system, and provide detailed information on the human-system interface (HSI). Each system has specific interface details based on the system EDS.

II-A-2.4 Failure Analysis

(1) A Failure Modes and Effects Analysis (FMEA) Report specific to each system is provided to the customer. The FMEA documents all identified failure modes which affect the safety-related functions. Through the analysis activities, all identified failures are shown

to be unlikely and detectable. This result conforms to the failure state and FMEA requirements shown in the EDS for each system.

The FMEA for the BWR-5 PRM system was conducted and documented in the Requirements Definition Phase Preliminary Hazard Analysis Report (Reference (d11)).

(2) An Availability and Reliability Analysis Report specific to each system is provided to the customer. This report is generated using MIL-HDBK-217F (Reference (a24)). The reliability values are calculated by summing failure rates of whole devices.
The reliability and availability analysis for the BWR-5 PRM system configured with the LPRM, LPRM/APRM, and FLOW units was conducted and documented in the Availability/Reliability Analysis Report (Reference (d30)).

(3) Each NRW-FPGA-based system is designed and tested to minimize the possibility of programmable logic common cause failure (CCF). However, should a CCF occur, it would likely result in a complete loss of system function or incorrect indications or outputs. Toshiba recommends that operational procedures include instructions for operator actions in the unlikely event of a CCF, including complete loss of system function or incorrect indications or outputs.

II-A-2.5 Diversity and Defense-in-Depth

There is no attempt to design diversity or defense-in-depth into a NRW-FPGA-based system. Diversity and defense-in-depth analyses are a plant-specific evaluation of overall system considerations and general characteristics of devices rather than the specifications of any individual device in the system. The qualification of NRW-FPGA-based systems provides assurance of a qualified device and logic.

II-A-2.6 Setpoint Support Analysis

Each Setpoint Support Analysis for the NRW-FPGA-based systems is performed to meet the requirements of EPRI TR-107330 (Reference (a46)), Section 4.2.4 and RG 1.105 (Reference (a10)).

For the BWR-5 PRM system, the data necessary to perform a setpoint analysis is provided in the system-specific Setpoint Support Analysis Report (Reference (d31)) which is provided to the customer.

II-A-2.7 Self-Diagnostic Capabilities

Each module and each system provides self-test and self-diagnostic capabilities. These capabilities are documented in the system-specific FMEA Report. Each FMEA Report is based on the system's EDSs, which documents the self-test capability of modules making up the system as well as the overall system's self-test capabilities. Details of the HSI indications for self-diagnostics are provided in each unit's users manual.

Each module and each system includes operator-initiated surveillance test and calibration features. Failures detected by hardware and surveillance testing are consistent with the failure detectability assumptions of the single-failure analysis and the FMEA.

When the NRW-FPGA-based system is operating, improper operation of any modules by an identified fault will be detected by module continuous self-diagnostics in a few seconds.

Continuous self-diagnostics is accomplished by monitoring outputs of power supplies, using watchdog timers on individual modules, monitoring outputs of various modules, and monitoring inputs from communications links.

Each module which has EEPROMs to store constants for the setpoint value storage verifies the stored values in the EEPROM with parity bits or dual storage. If an error is detected, a minor failure alarm signal is generated, which may result in a channel being designated as inoperable.

Since the self-diagnostic features are integral to the modules, the features meet all safety-related requirements.

Should a failure be detected during continuous self-test, a fault indicator LED is lit on the front panel of the affected module and a dry contact signal changes state. A dry contact output is provided which the customer shall wire into the control room annunciator system, as specified in the plant-specific design. Operator notification of detected failures complies with the system status indication provisions of IEEE Std 603-1991 (Reference (a36)). The utility shall provide instructions in plant procedures to ensure consistency with, and support of, plant technical specifications, operating procedures, and maintenance procedures.

II-A-2.8 Surveillance Capabilities

This section discusses considerations for changes to existing plant surveillance tests based on the design features incorporated in the NRW-FPGA-based systems (including the self-test features

discussed above). These considerations are provided here to assist plants in identifying areas in which use of the NRW-FPGA-based systems will have a beneficial effect on the surveillance program.

Modifications to the existing surveillance tests and licensing commitments will be required, as is identified in USNRC Standard Review Plan, Chapter 7, Branch Technical Position (BTP) 7-17 (Reference (a6)). Self tests could be used to reduce the surveillance testing requirements for the NRW-FPGA-based systems. The self-test capabilities of the systems could be credited with some of the test functions for channels and devices currently provided by manual surveillance tests. The systems provide at least as much test coverage as the existing surveillance tests, through the fault tolerance and detection capabilities inherent in the system design.

(1) Because of design and architectural differences between analog and digital systems, traditional surveillance test provisions for analog systems may not be adequate or appropriate for digital systems. The required surveillance test capabilities to be included in this design will have to be evaluated to assure adequacy to fulfill the requirements and the intent of the surveillance tests. The replacement system design should provide the ability to conduct periodic testing consistent with the modified technical specifications and plant procedures.

(2) The NRW-FPGA-based systems application can be designed to provide these capabilities, in accordance with the requirements established in the regulatory guidance Referenced in BTP 7-17. There is nothing inherent in the NRW-FPGA-based system design that does not comply with the requirements of IEEE Std 603 (Reference (a36)), as required in BTP 7-17. The NRW-FPGA-based system design also complies with the recommendations made in IEEE Std 7-4.3.2 (Reference (a30)).

(3) Plant procedures should specify manual compensatory actions for recovery indications of the NRW-FPGA-based system equipment problems.

(4) Utility surveillance tests shall be designed to validate correct operation of each system and the system's self-tests, to the extent practical. For the BWR-5 PRM system, a method of failure detection for each of the failure modes listed in the appendix of the Requirements Definition Phase Preliminary Hazard Analysis Report (Reference (d11)) should be considered developing the required content for surveillance testing.

(5) Surveillance test frequency in a nuclear plant is based on the expected reliability of the installed system. The technology used in the NRW-FPGA-based systems should enhance

the reliability and reduce the possibility of undetected in-service degradation.

For the PRM system, Toshiba concludes that a surveillance frequency of once per month is reasonable. Utility experience with the system may be used by the utility to decrease surveillance frequency.

II-A-3 System Configuration

This section describes the configuration of FPGA-based I&C systems that have been qualified. Subsections will be added to this application guide as a qualification testing is performed for future application. Configuration Management method is described in I-3.12.2.

II-A-3.1 PRM System Configuration

The PRM Qualification Project used a test specimen composed of units like those that would be used in the PRM system for a BWR-5 design. The logic inside each FPGA was identical to what would be shipped to a BWR-5. The PRM system consists of LPRM units, APRM/LPRM units, FLOW units, and RBM units. Each unit is comprised of modules and a unit chassis specific to each unit design. The RBM unit that has non-safety-related functions only is not part of the scope of the PRM Qualification Project.

The Unit/Module configuration qualified in these qualification activities is shown in Table II-A-3-1.

Table II-A-3-1 Unit/Module Configuration Qualified in PRM Qualification Project

(Slot ID) Module Name	Module Model Number	Functional Description
LPRM Unit (HNU100)		
(FSL01) LPRM Module	HNS013	LPRM function for LPRM Detector CH 11
(FSL02) LPRM Module	HNS013	LPRM function for LPRM Detector CH 12
(FSL03) LPRM Module	HNS013	LPRM function for LPRM Detector CH 13
(FSL04) LPRM Module	HNS013	LPRM function for LPRM Detector CH 14
(FSL05) LPRM Module	HNS013	LPRM function for LPRM Detector CH 15
(FSL06) LPRM Module	HNS013	LPRM function for LPRM Detector CH 16
(FSL07) LPRM Module	HNS013	LPRM function for LPRM Detector CH 17
(FSL08) LPRM Module	HNS013	LPRM function for LPRM Detector CH 18
(FSL09) LPRM Module	HNS013	LPRM function for LPRM Detector CH 19
(FSL10) LPRM Module	HNS013	LPRM function for LPRM Detector CH 20
(FSL11) LPRM Module	HNS013	LPRM function for LPRM Detector CH 21
(FSL12) LPRM Module	HNS013	LPRM function for LPRM Detector CH 22
(FSL13) BLANK Module	HNS490	Dummy LPRM module. When the unit is not filled with 13 LPRM Modules, this module is used to fill the open slots to provide necessary connections and signals simulating the LPRM Module operation in the open slots.
(FSL14) STATUS Module	HNS093	Power supply voltage monitoring status indication

(Slot ID) Module Name	Module Model Number	Functional Description
(PSSL01) LVPS Module	HNS500	+5V and ±15V power supply to each module
(BSL01) AO Module	HNS518	Analog output (AO) of LPRM levels (Ch. 11 to 22) to the process computer.
(BSL02) Blank Panel	---	Blank panel
(BSL03) AO Module	HNS515	Analog output of LPRM levels (Ch. 11 to 22) to the Transient Monitor or OPRM
(BSL04) DIO Module	HNS520	Digital Input / Output (DIO) used for digital output of LPRM Upscale, Downscale, and Inoperable signals to the trip auxiliary unit
(BSL05) Blank Panel	---	Blank Panel
(BSL06) Blank Panel	---	Blank Panel
(BSL07) Blank Panel	---	Blank Panel
(BSL08) TRN Module	HNS530	Optical data transmission (TRN) of LPRM level (Ch.11-22), Inoperable and LVPS failure information to LPRM/APRM unit
(PSSL02) LVPS Module	HNS500	+5V and ±15V power supply to each module
LPRM/APRM Unit (HNU200)		
(FSL01) LPRM Module	HNS013	LPRM function for LPRM Detector CH 1
(FSL02) LPRM Module	HNS013	LPRM function for LPRM Detector CH 2
(FSL03) LPRM Module	HNS013	LPRM function for LPRM Detector CH 3
(FSL04) LPRM Module	HNS013	LPRM function for LPRM Detector CH 4
(FSL05) LPRM Module	HNS013	LPRM function for LPRM Detector CH 5
(FSL06) LPRM Module	HNS013	LPRM function for LPRM Detector CH 6
(FSL07) LPRM Module	HNS013	LPRM function for LPRM Detector CH 7
(FSL08) LPRM Module	HNS013	LPRM function for LPRM Detector CH 8
(FSL09) LPRM Module	HNS013	LPRM function for LPRM Detector CH 9
(FSL10) LPRM Module	HNS013	LPRM function for LPRM Detector CH 10
(FSL11) APRM Module	HNS020	APRM function
(FSL13) Blank Panel	---	Blank Panel
(FSL14) STATUS Module	HNS091	Data reception status, power supply voltage monitoring status indications.
(PSSL01) LVPS Module	HNS500	+5V and ±15V power supply to each module
(BSL01) AO Module	HNS518	Analog outputs of LPRM levels (Ch. 1 to 10), APRM level, APRM Upscale (High) setpoint, Simulated Thermal Power level, and Simulated Thermal Power Upscale setpoint to the process computer
(BSL02) AO Module	HNS516	Analog outputs of APRM level and APRM Upscale (High) setpoint to the recorder
(BSL03) AO Module	HNS515	Analog outputs of LPRM levels (Ch. 1 to 10) and APRM level to the Transient Monitor or OPRM
(BSL04) DIO Module	HNS520	Digital outputs of LPRM Upscale, Downscale, Inoperable, and APRM trip signals to the trip auxiliary unit Digital inputs of reactor mode and APRM bypass signal
(BSL05) RCV Module	HNS540	Optical data reception of the recirculation flow values from the Flow units Optical data reception of LPRM levels (Ch. 11 to 22), Inoperable, and LVPS failure information from the LPRM unit
(BSL06) Blank Panel	---	Blank panel
(BSL07) Blank Panel	---	Blank panel

(Slot ID) Module Name	Module Model Number	Functional Description
(BSL08) TRN Module	HNS530	Optical data transmission of LPRM level (Ch. 1 to 22), APRM level, APRM Upscale (High) setpoint, Simulated Thermal Power level, Simulated Thermal Power Upscale setpoint, and Recirculation Flow values to RBM unit
(PSSL02) LVPS Module	HNS500	+5V and ±15V power supply to each module
FLOW Unit Configuration (HNU300)		
(FSL01) Blank Panel	---	Blank Panel
(FSL02) Blank Panel	---	Blank Panel
(FSL03) Blank Panel	---	Blank Panel
(FSL04) Blank Panel	---	Blank Panel
(FSL05) Blank Panel	---	Blank Panel
(FSL06) Blank Panel	---	Blank Panel
(FSL07) Blank Panel	---	Blank Panel
(FSL08) Blank Panel	---	Blank Panel
(FSL09) Blank Panel	---	Blank Panel
(FSL10) SQ-ROOT Module	HNS030	Square root arithmetic function for Recirculation Loop "a"
(FSL11) SQ-ROOT Module	HNS030	Square root arithmetic function for Recirculation Loop "b"
(FSL12) FLOW Module	HNS040	Recirculation-flow calculation, trip and alarm functions
(FSL14) STATUS Module	HNS093	Flow unit status indication function
(PSSL01) LVPS Module	HNS500	+5V and ±15V power supply to each module
(BSL01) AO Module	HNS518	Analog outputs to the process computer.
(BSL02) AO Module	HNS516	Analog outputs to the recorders.
(BSL03) AO Module	HNS517	Analog outputs to the Transient Monitor.
(BSL04) DIO Module	HNS520	Digital outputs of the trip signals to the trip auxiliary unit. Digital input of Bypass signal.
(BSL05) Blank Panel	---	Blank Panel
(BSL06) Blank Panel	---	Blank Panel
(BSL07) TRN Module	HNS530	Optical serial transmission to RBM unit
(BSL08) TRN Module	HNS530	Optical serial transmission to APRM unit
(PSSL02) LVPS Module	HNS500	+5V and ±15V power supply each module

II-A-4 Environment and Location

Specific environmental requirements for safety-related NRW-FPGA-based systems are discussed in this section. These environment and location requirements are based on the recommendations in the User's Manual, System O&M Manual, and the results of the qualification testing.

All temperature, humidity, radiation, seismic, and EMC conditions shall be verified by type test, or by analysis. Additional system-specific environment and location requirements derived from qualification testing will be documented in this application guide after the qualification testing is complete.

II-A-4.1 Mounting

Each chassis shall be installed in a cabinet. The cabinet shall provide access for both the front and the rear of each chassis. The cabinet shall be provided with locking doors on the front and rear. The front door may be equipped with a window allowing visual access to the module fronts. Opening any door shall provide annunciation in the main control room. For cyber security purposes, provision shall be made for separate annunciation in one or more physical security locations.

The chassis that is used as the enclosure of each unit shall be suitable for mounting in a standard 19 inch rack. The hole spacing of the chassis shall be compatible with the EIA standard. A chassis is fixed in the rack with four M5 screws in the front side and eight M4 screws in the back side. The torque to tighten the screws is 2.6 to 3.4 N・m in the front side, and 1.3 to 1.7 N・m on the back side.

During normal plant operation, no access is required to the unit rear modules.

II-A-4.2 Temperature, Humidity, and Radiation

The NRW-FPGA-based systems shall be located in an area that controls temperature, humidity, and radiation within the performance requirements defined by the environmental conditions shown in Table II-A-4-1. Type testing in a temperature and humidity test chamber shall be performed in accordance with the methods defined in EPRI TR-107330 (Reference (a46)). Radiation exposure shall be performed in accordance with the methods defined in EPRI TR-107330. Type testing is not performed within cabinets.

Table II-A-4-1 Environmental Conditions

	Normal Environmental Basic Requirements	Abnormal Environmental Basic Requirements
Temperature Range	16 to 40°C (60 to 104°F)	4 to 50°C (40 to 120 °F)
Humidity Range	40 to 95% (non-condensing)	10 to 95% (non-condensing)
Radiation Exposure	Up to 10 Gy (10^3 RADS)	Up to 10 Gy (10^3 RADS)

(1) Environmental Test Profiles for BWR-5 PRM System

The BWR-5 PRM system has been type tested to these limits, using the temperature and humidity curve provided in Figure 4-4 of EPRI TR-107330. The actual test pattern achieved during Environmental Testing is shown in Figure II-A-4-1 and Figure II-A-4-2. The testing complied closely, but not identically, to the test curve in EPRI TR-107330, due to test equipment limitations.

The testing complied closely, but not identically, to the test curve in EPRI TR-107330, due to test equipment limitations.

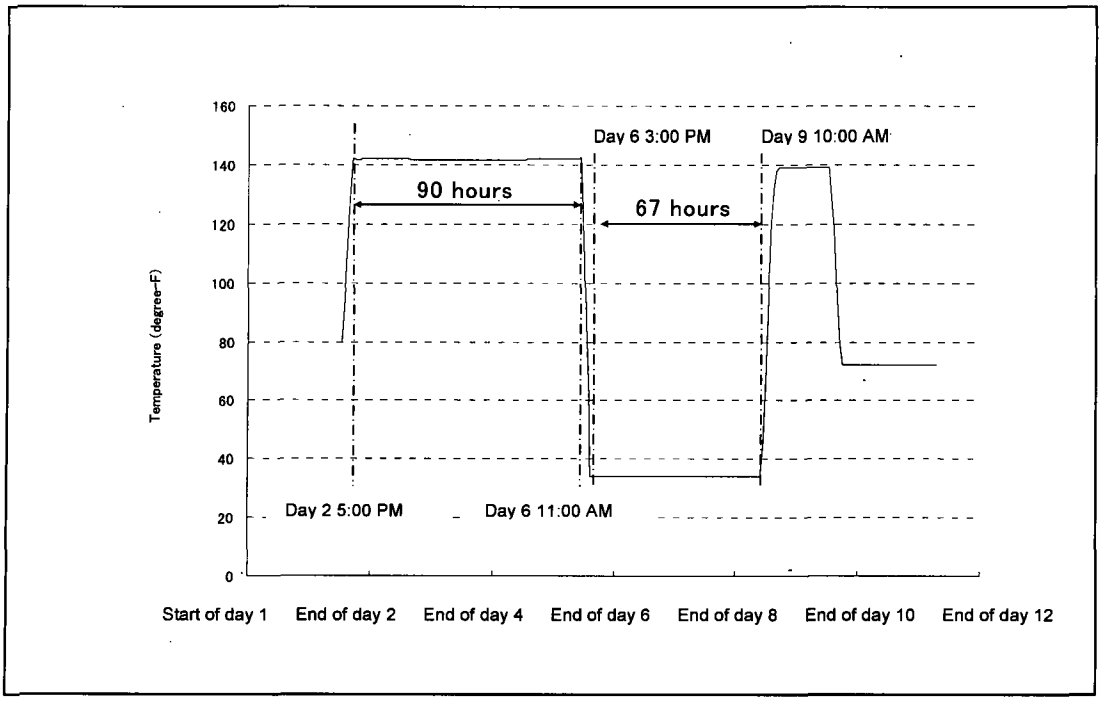


Figure II-A-4-1 Environmental Test Temperature Profile

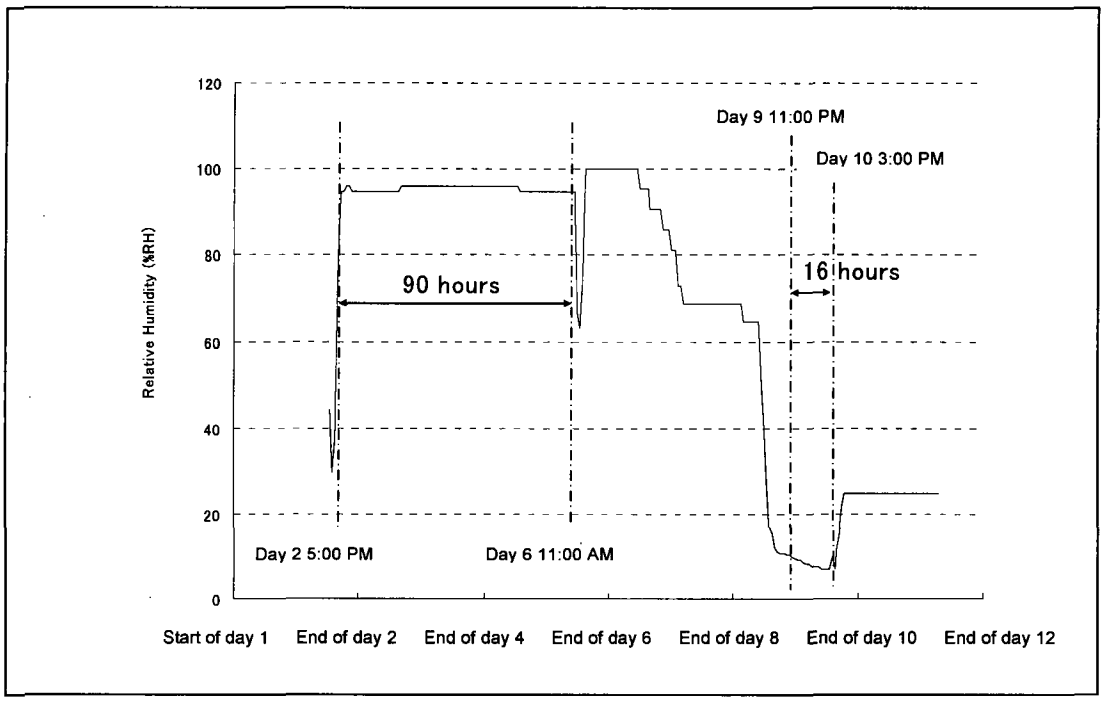


Figure II-A-4-2 Environmental Test Humidity Profile

The value of relative humidity at the low temperature condition was not established due to test facility capability. Toshiba performed the low temperature test independently of the low humidity test. This is acceptable because EPRI TR-107330 states that if the specified relative humidity cannot be achieved for the specified temperature, then run the test for the specified time at the lowest relative humidity that can be achieved at the specified temperature followed by running the test at the lowest temperature where the specified relative humidity can be achieved.

Details of the tests results and test data of Environmental Test are reported in the Qualification Test Summary Report (Reference (d16)). The test achieved the objective of exposing the tested equipment to a wide range of humidity conditions. Also, review of the data collected during the test shows that the Test Specimen operated as intended.

At the end of the test, a Performance Proof Test was performed. This test showed that all safety functions were confirmed to be within the required tolerance after subjecting the Test Specimen to temperature and humidity extremes. The evaluation concludes that this exposure will not prevent the PRM System from performing its safety-related function.

The type test performed during the PRM Qualification Project demonstrated that the PRM system survives and operates correctly throughout temperature and humidity testing.

(2) Radiation Exposure for BWR-5 PRM System

The gamma irradiation on the Test Specimen was performed to 11 Gy to provide 10% margin above the requirement of 10 Gy. The 10 Gy exposure requirement is stated in Section 4.3.6.1 of EPRI TR-107330 (Reference (a46)). The test was performed in accordance with the guidance provided on IEEE Std 323-1983 (Reference (a31)). The irradiation was performed at high level radiation effects test facility. For this irradiation, a [ ]$^{a, c}$ curie (Ci) Co-60 source was used.

Details of the tests results and test data of Environmental Test are reported in the Qualification Test Summary Report (Reference (d16)). At the end of the test, a Performance Proof Test was performed. This test showed that all safety functions were confirmed to be within the required tolerance after subjecting the Test Specimen to the aging due to this exposure. The evaluation concludes that this exposure will not prevent the PRM System from performing its safety-related function.

II-A-4.3 Heat Loads in Cabinets and Rooms

Heat Loads in the cabinets and the rooms are as follows.

(1) When mounting each NRW-FPGA-based system chassis into enclosures, heat management calculations shall be made to avoid exceeding the qualified ambient temperature ratings of the each system. For purposes of these calculations, all power consumed by the system shall be assumed to be dissipated inside the enclosure where the chassis is mounted.

(2) If the room temperature plus any heat rise within the cabinet exceeds the limits supplied in Table II-A-4-1, additional provision must be made for temperature control to ensure that temperature remains within the qualified temperature condition.

(3) The system temperature range must be computed with cabinet doors open and closed.

II-A-4.4 Seismic Acceleration Limits

All safety-related NRW-FPGA-based systems shall be qualified as Category I seismic devices within the test levels shown on Figure II-A-4-3 and Table II-A-4-2. A plant-specific evaluation shall be needed to determine whether the as-tested limits bound the plant seismic acceleration requirements. If not, additional evaluation or seismic testing is required.

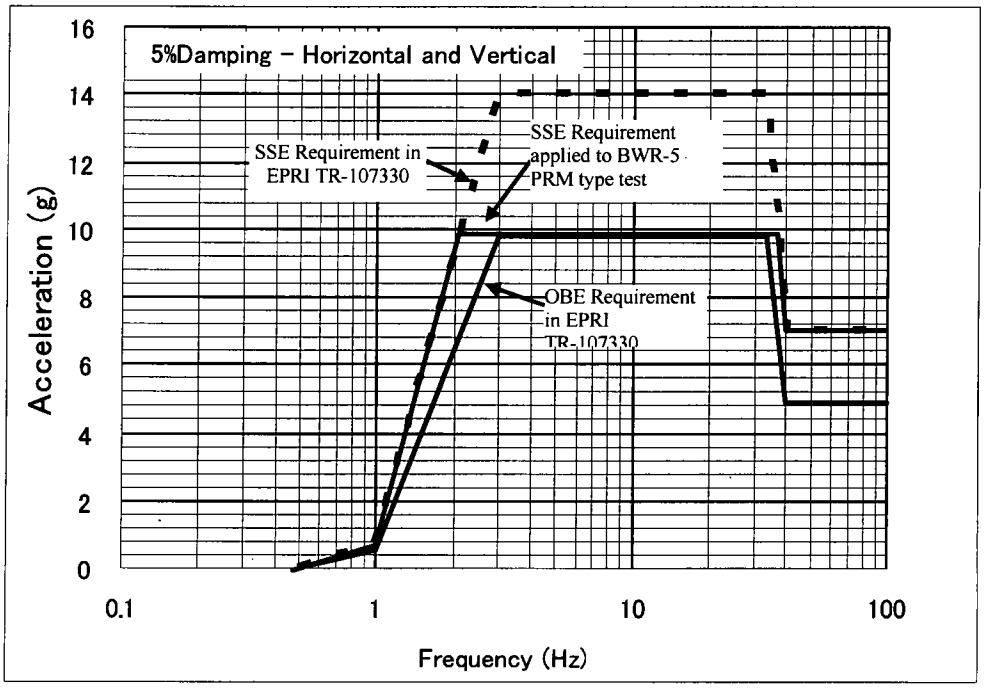


Figure II-A-4-3 Required Response Spectrum

Table II-A-4-2 Seismic Levels

Seismic Event	Maximum Acceleration Requirement	Reference Spectrum
OBE	9.8 g	EPRI TR-107330 Figure 4-5
SSE	14g (9.8 g was applied to type test for PRM Qualification Project due to the limitation of test facility)	EPRI TR-107330 Figure 4-5

For the BWR-5 PRM System, the type test was performed during the PRM Qualification Project. The required peak amplitude of the SSE is 14 g according to Figure 4-5 of EPRI-TR-107330, however, due to the limitation of the test facility's vibration table, the peak amplitude of SSE was 9.8 g. The following tests were performed.

(1) Resonance Search.

A low-level (approximately 0.2 g) single-axis sine sweep was performed in each of the three orthogonal axes to determine major resonance of the Test Specimen Units.

(2) Random Multifrequency Tests (5 OBEs and 1 SSE).

The Test Specimen was subjected to 30 second duration triaxial multi-frequency, random motion which was amplitude-controlled in one-sixth octave bandwidth spaced one-sixth octave apart over the frequency range of 1 to 100 Hz. The test response spectrum (TRS) obtained is shown in the Qualification Test Summary Report (Reference (d16)).

Figure II-A-4-4 is a representative figure showing the TRS for 1st OBE for Horizontal Axis. The figure is based on a damping value of 5% used in the data analysis. See the Qualification Test Summary Report Appendix A for the remaining test figures.

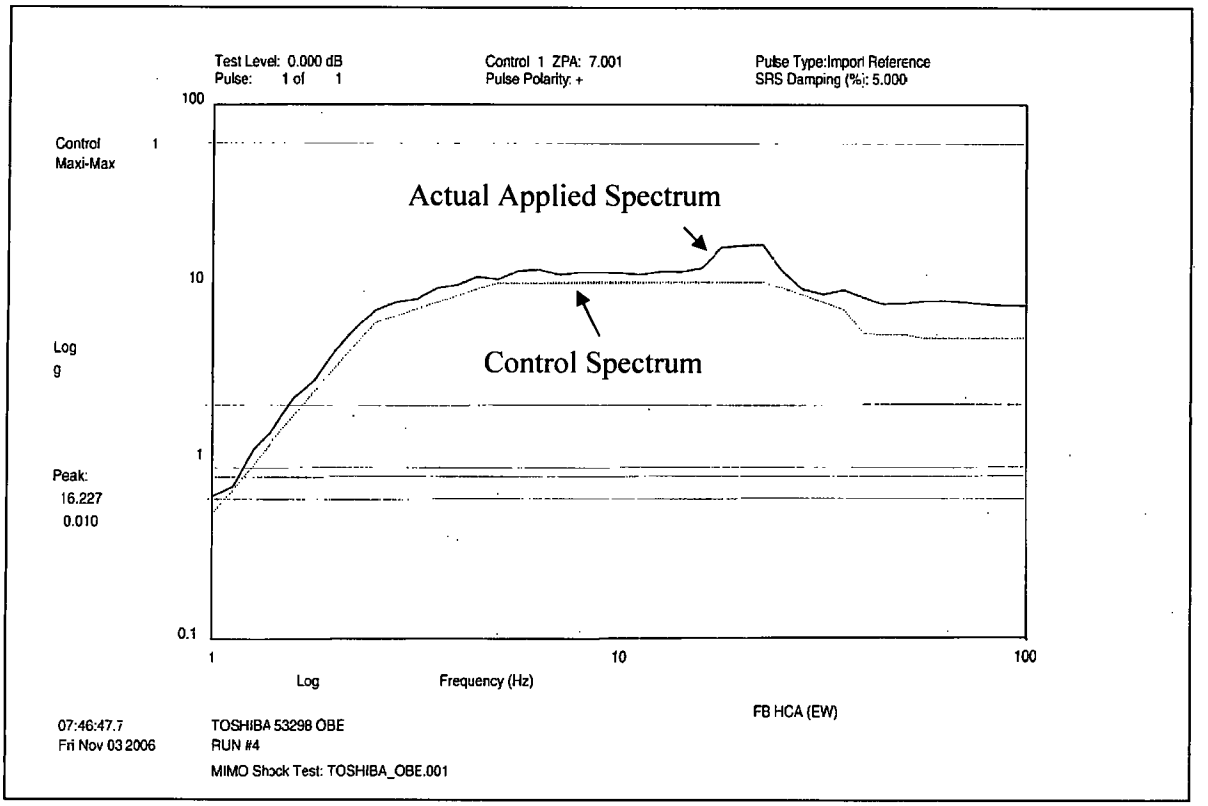


Figure II-A-4-4 TRS for 1st OBE for Horizontal Axis (East to West)

Details of the test results and test data of the Seismic Test are reported in the Qualification Test Summary Report (Reference (d16)). Data collected during and after each OBE and SSE test demonstrate that the Test Specimen operated as intended throughout the testing. The Test Specimen was visually inspected for damage or degradation following each OBE and SSE test. Results of these inspections showed no physical damage or degradation of the Test Specimen.

The type test performed during the PRM Qualification Project demonstrated that the PRM system survives and operates correctly during and after seismic event up to the tested accelerations.

II-A-4.5 Electro-Magnetic Compatibility (EMC)

An understanding of the electromagnetic susceptibility of a device is necessary to ensure that its operation will not be adversely affected by EMI/RFI or surge levels already present or permitted in the area where the device will be located. An understanding of the electromagnetic emissions of a device is necessary to ensure that operation of the device being tested would not result in adverse effects on other systems installed electrically close to the device being tested. Toshiba performs type testing of systems prior to making them available for installation in plants. The EMC environmental requirements documented in this section are based on the results of the qualification type test. The utility must evaluate the environmental data to ensure that the qualification envelope is sufficient for the planned location. This may require the utility to perform one or more of the following:

(1) Conduct an EMI/RFI survey to evaluate the EMI/RFI levels to ensure that the environment is within the assumptions on which USNRC Regulatory Guide 1.180, Revision 1 (Reference (a19)) is based.

(2) Recommend actions to mitigate unacceptable EMI/RFI sources. Toshiba does not perform qualification testing using a secondary enclosure, additional cable and wire shielding, or power line filtering beyond the devices installed during type testing. Mitigating actions to address system susceptibility levels would likely incorporate these common in-plant installation features. Mitigating actions might also include administrative controls on the EMI/RFI sources.

(3) Recommend additional qualification testing to address those cases where the recorded EMI/RFI test data provides inconclusive evidence of the susceptibility of particular modules, and therefore the modules are assumed to be susceptible. Additional testing may demonstrate that some modules are not actually susceptible to the applied EMI/RFI test levels.

The test methods to be applied to EMC qualification testing are summarized in Table II-A-4-3 and Table II-A-4-4. Test types listed in the tables comply with USNRC Regulatory Guide 1.180, Revision 1. The test methodologies shall be established to meet the requirements in each military or International Electrotechnical Commission (IEC) standard listed in the table.

Table II-A-4-5 and Table II-A-4-6 show the results of EMI/RFI Test and EFT/B tests.

Table II-A-4-3 EMI/RFI Test Method

Test Type	MIL Std 461 E Test Method
(a) Low-Frequency Conducted Susceptibility (Power):	CS101
(b) High-Frequency Conducted Susceptibility (Power):	CS114
(c) High-Frequency Conducted Susceptibility (Signal):	CS114
	CS115
	CS116
(d) Radiated Susceptibility, Magnetic Field:	RS101
(e) Radiated Susceptibility, Electric Field:	RS103
(f) Low-Frequency Conducted Emissions:	CE101
(g) High-Frequency Conducted Emissions:	CE102
(h) Radiated Emissions, Magnetic Field:	RE101
(i) Radiated Emissions, Magnetic Field:	RE102

Table II-A-4-4 Surge, EFT/B Test Method

Test Type	Applicable IEC Standard
(a) Ringwave Surge (±2 kV)(Power)	IEC 61000-4-12
(b) Combination Wave (±2 kV)(Power)	IEC 61000-4-5
(c) EFT/B (±2 kV)(Power)	IEC 61000-4-4

Table II-A-4-5 EMI/RFI Test Results

	RG 1.180R1			Test Results	TR-107330				
Published	October 2003				December 1996				
EMI/RFI Test	Standard	Condition	Section		Requirement	Section	TR-102323 R1	Condition	Standard
Low Frequency Conducted Susceptibility (Power)	MIL-Std 461E CS101	30(120)Hz-150kHz	4.1.1	Comply	Conducted Susceptibility	4.3.7 B	B 3.2	30Hz-50kHz	MIL-STD 461D CS101
High Frequency Conducted Susceptibility (Power)	MIL-Std 461E CS114	10kHz-30MHz	4.1.2	Comply				50kHz-400MHz	MIL-STD 461D CS114
High Frequency Conducted Susceptibility (Signal)	MIL-Std 461E CS114	10kHz-30MHz	4.2	Comply					
	MIL-Std 461E CS115	Impulse Excitation	4.2	Comply	-	-	-	-	
	MIL-Std 461E CS116	Damped Sinusoidal Transients 10kHz-100MHz	4.2	Comply	-	-	-	-	-
Low Frequency Radiated Susceptibility	MIL-Std 461E RS101	30Hz-100kHz	4.3.1	Comply	-	-	-	-	-
High-Frequency Radiated Susceptibility	MIL-Std 461E RS103	30MHz-10GHz	4.3.2.6	Comply	Radiated Susceptibility	4.3.7 A	B 3.1	10kHz-1GHz	MIL-STD 461D RS103

Table II-A-4-6 EFT/B Test Results

	RG 1.180R1			Test Results	TR-107330				
Published	October 2003				December 1996				
EMI/RFI Test	Standard	Condition	Section		Requirement	Section	TR-102323 R1	Condition	Standard
SURGE(Ring Wave, Power)	IEC61000-4-12	2kV/4kV	5.	Comply	Surge Withstand Capability	4.6.2	B 3.3	3kV	MIL-STD 461D CS116, IEEE C62.41-1991
SURGE (Combination Wave, Power)	IEC61000-4-5	2kV/4kV	5.	Comply					
EFT/B (Power)	IEC61000-4-4	2kV/4kV	5.	Comply			B 3.4	3kV	IEC 801-4

II-A-4.5.1 EMI/RFI Test for BWR-5 PRM System

For the BWR-5 PRM System, the test was conducted. Details of the test results and test data of EMI/RFI testing are reported in the Qualification Test Summary Report (Reference (d35)). Results of the susceptibility testing show that the Test Specimen continued to function correctly throughout all test exposure levels. The transfer of input and output data was not interrupted. There were no interruptions or inconsistencies in the operation of the system.

For the emissions tests, the Test Specimen was found to comply with the allowable equipment emissions levels for radiated magnetic field emissions from 30 Hz to 100 kHz (RE101). A specific exceedance was found during CE101 in the power leads. From approximately 100 Hz to 700 Hz, emissions exceed the limit shown in RG 1.180 Revision 1. This excess comes from the waveform distortion due to the AC/DC power supply (i.e. LVPS module) in the units in PRM system. To suppress this emission, Toshiba inserted a filter into the AC power line to the LVPS module, and confirmed that the test results met the requirement with this corrective measure as shown in Table II-A-4-7. In Table II-A-4-7, the requirements of EPRI-TR-107330 are listed as well for reference.

Table II-A-4-7 Test Results of the Emission Test

	RG 1.180R1			Test Results	TR-107330				
Published	October 2003				December 1996				
EMI/RFI Test	Standard	Condition	Section		Requirement	Section	TR-102323 R1	Condition	Standard
Low Frequency Conducted Emissions	MIL-Std 461E CE101	30(120)Hz-10kHz	3.1	Comply with corrective measure	Conducted Emission	4.3.7D	7	30Hz-50kHz	MIL-STD 461D CE101
High-Frequency Conducted Emissions	MIL-Std 461E CE102	10kHz-2MHz	3.2	Comply				50kHz-400MHz	MIL-STD 461D CE102
Low-Frequency Radiated Emissions	MIL-Std 461E RE101	30Hz-100kHz	3.3	Comply	Radiated Emission	4.3.7C		30Hz-100kHz	MIL-STD 461D RE101
High-Frequency Radiated Emissions	MIL-Std 461E RE102	2MHz-1GHz	3/4	Comply				10kHz-1GHz	MIL-STD 461D RE102

II-A-4.5.2 Surge Withstand Capability (SWC) Test for BWR-5 PRM System

For the BWR-5 PRM System, the SWC Test was performed to ensure that the PRM System withstands the surge limits given in Table 22 of RG 1.180. Surges were applied in accordance with IEC 61000-4-12 (for Ring Wave) (Reference (a29)) and IEC 61000-4-5 (for Combination Wave) (Reference (a28)). Details of the test results and test data of SWC Test are reported in the Qualification Test Summary Report (Reference (d16)). The surges were applied to the test points, and the Test Specimen kept normal operation during the surge application. Based on the results reported in the Qualification Test Summary Report, the Test Specimen continued to operate in accordance with the test acceptance criteria following application of the surge test voltages. The repetition rate for the ring wave was 12 per minute, which is within the repetition rate required by the IEC standard."

II-A-4.5.3 EFT/B Test for BWR-5 PRM System

For the BWR-5 PRM System, the EFT/B Test was performed to ensure that the PRM Test Specimen withstands the surge limits given in the Table 22 of RG 1.180 and IEC 61000-4-4 (Reference (a27)). Details of the test results and test data of EFT/B Test are reported in the Qualification Test Summary Report (Reference (d16)). The EFT/B wave forms were applied to the defined test points. Results of the EFT/B testing show that the Test Specimen continued to operate in accordance with the test acceptance criteria.

II-A-4.6 Class 1E to Non-Class 1E Isolation

Isolation features of the NRW-FPGA-based system conform to IEEE Std 384-1992 (Reference (a34)).

- Each isolation device prevents shorts, grounds, and open circuits on the Non-Class 1E side from unacceptably degrading the operation of the circuits on the Class 1E side.
- Each isolation device prevents application of the maximum credible voltage on the Non-Class 1E side from unacceptably degrading the operation of the Class 1E circuits.

For the BWR-5 PRM System, the communication data link provided in each PRM System has a one-way fiber optic communication link, providing fixed data sets from each safety-related PRM division individually to the non-safety-related Rod Block Monitor (RBM), providing 1E to non-1E isolation, and offering no possibility of data transfer from the non-safety to the safety equipment. This design eliminates any potential for data from one division being supplied to

another division. Based on this system design, only the devices installed in the main chassis are required to provide Class 1E to Non-1E electrical isolation capability (if these modules are used to interface to Non-1E equipment). Accordingly, the following devices that are used to provide analog output signals to Non-1E portion were tested for Class 1E isolation capability:

- HNS518 and HNS515 AO modules installed in LPRM Units
- HNS518, HNS516, and HNS515 AO modules installed in LPRM/APRM Units
- HNS518, HNS517, and HNS516 AO modules installed in Flow Unit

For the BWR-5 PRM System, the type test was performed. Details of the test results and test data of the Class 1E to Non-1E test are reported in the Qualification Test Summary Report (Reference (d16)). Test level voltages were applied to the test points and the safety-related portion of the Test Specimen operated normally during and after the application. As expected, damage occurred to the non-1E AO module, which did not propagate to the Class 1E equipment.

II-A-4.7 Electrostatic Discharge (ESD)

ESD features of NRW-FPGA-based systems conform to IEC 61000-4-2 (Reference (a26)). The ESD levels comply with the levels of EPRI TR-107330 and EPRI TR-102323 ($\pm$8 kV for contact discharge or $\pm$15 kV for air discharge).

Despite this testing, in order to further reduce the possibility of undetected ESD damage resulting in shortened equipment life or decreased reliability, Toshiba requires use an anti-ESD wrist band when maintenance is performed on any equipment. Toshiba also requires all modules and power supplies to be handled using ESD protection, including ESD pads and ESD packing materials.

For the BWR-5 PRM System, ESD test was performed. Details of the test results and test data for the ESD test are reported in the Qualification Test Summary Report (Reference (d16)). Results of the ESD testing show that the Test Specimen did not present any temporary degradation or loss of function or performance when the ESD was applied to the front panels, components on the front panels, and side panels, which can all be touched during normal operation. However, testing showed temporary degradation/loss of function when ESD was applied to back panels. System functionality was recoverable. These panels are not generally exposed to ESD during normal operation. For the PRM System, ESD can be mitigated by preventing access to the back panel during plant operation, or by requiring personnel to wear anti-ESD wristbands when accessing the equipment back panel during plant operation. For RTIS, Toshiba will determine that conservative wearing of ESD wrist straps while touching or

having the potential to touch equipment is appropriate. Therefore, administrative controls (e.g., procedures requiring use of static discharge control devices such as grounding straps) will be required to prevent or reduce exposure to electrostatic discharges.

Administrative procedures should restrict maintenance access to the rear of the rack in which the units of PRM system are installed during normal plant operation.

II-A-5 Plant Interface

II-A-5.1 Response Time

The NRW-FPGA-based systems are validated during System Validation Tests to assure meeting the response time requirements described in the EDS for each system. The data for the EDS is based on the standard BWR requirements for trip or action times.

For the BWR-5 PRM, response time testing was performed as reported in the Part V of this LTR. The test results confirmed to meet that the response times of the APRM Upscale (High-High) and the Simulated Thermal Power Upscale trips were less than the required 40 ms.

II-A-5.2 Loss of Power Fault Indication

The NRW-FPGA-based systems units generate an inoperable signal from DIO module when power loss occurs, which is treated as an inoperable channel and, therefore, initiates a single-channel vote to trip signal. This capability is validated during System Validation Tests.

For the BWR-5 PRM, response time testing was performed as reported in the Verification and Validation Final Report (included in the Part V of this LTR). The loss of power testing demonstrated that the PRM system generates an inoperable signal from DIO module when power loss occurs.

II-A-6 Installation, Commissioning, and Maintenance

This section discusses considerations for installation, commissioning, and long term maintenance of the safety-related NRW-FPGA-based systems.

II-A-6.1 Required Testing

After a safety system is commissioned, no changes to the system can be performed without Toshiba redesigning the affected portions of the system and Toshiba and the utility re-commissioning the system.

The utility shall perform periodical testing to the requirements established by Toshiba in the User's Manual and/or System O&M Manual. Credit for self-tests can be used to reduce the requirement for surveillance testing, based on utility changes to the unit's Technical Specifications.

II-A-6.2 Operations Procedures

Operating procedures for the safety system being replaced will have to be modified to accommodate the NRW-FPGA-based systems. Procedures for new fault alarms will have to be created. Procedures for entry and performance of maintenance and surveillance testing procedures will have to be modified to account for the differences between an analog system and the NRW-FPGA-based systems.

II-A-6.3 Maintenance Procedures

Specific maintenance considerations for the NRW-FPGA-based systems include the following:

- User's Manual and/or System O&M Manual contain recommendations for maintenance.
- The utility should write their maintenance procedures in accordance with the guidance from the Toshiba User's Manual and/or System O&M Manual.
- For the BWR-5 PRM, the minimum surveillance frequency is once per month.

II-A-6.4 Maintenance and Bypass Capabilities

Existing safety-related systems in nuclear power plants typically include bypass capabilities for maintenance and testing. Implementation of these capabilities in a digital system requires

particular attention to prevent undesired bypass, or incomplete bypass when intended, of the system. Generic guidance on the implementation of bypass capabilities is provided in User's Manual and/or System O&M Manual.

The BWR-5 PRM provides bypass features that allow the operator to bypass any one of the three APRM channels for one RPS division during normal plant operation. The APRM channel bypassed status is displayed on the PRM front panel and provided to the main control room.

II-A-7 PRM or PRNM System Configuration for BWRs (BWR-2, BWR-3, BWR-4, BWR-5, BWR-6) and ABWR

The number of units which would be used for BWR designs varies based on the size of the core and the number of local power range monitors installed to monitor the core. This section provides a comparison between the PRM and/or PRNM system that would be used for the various types of BWRs.

This guidance provides a method to apply the modules and units qualified for BWR-5 PRM system, and method to modify and customize the neutron monitoring system for other BWR types.

Since the BWR-2, -3, -4, and -6 PRM are bounded by the BWR-5 PRM, no additional type testing will be performed. The ABWR PRNM system has a sufficiently different configuration from the BWR PRM systems to require repeating type testing completely. Since the OPRM, SRNM, and RTIS use new modules, each will be type tested completely.

Specifically, the table below shows the number of units for the typical BWR-5 PRM system. The table also shows the equivalent information for other BWR types, namely, BWR-2, BWR-3, BWR-4, BWR-6, and the Advanced BWR (ABWR) design.

Typical system configurations for BWR-5, BWR-2, BWR-3, BWR-4, BWR-6, and the ABWR are shown in Table II-A-7-1.

The PRM system provides the signals of the LPRM levels to the OPRM system through analog outputs or a fiber communication link. The analog signals are identical to the signals that are provided to the existing OPRM and the transient monitor. Replacement of the LPRM, APRM, and OPRM together is best performed using this fiber optic communication over modules that have already been type tested. When the fiber communication is applied, a TRN module, which provides the LPRM level data using same data provided to RBM, is added to the LPRM unit and LPRM/APRM unit, as defined in Section II-A-3.1.

Table II-A-7-1 Configuration of BWR-5, BWR-2, BWR-3, BWR-4, BWR-6, and ABWR

BWR	Number of LPRM Units	Number of LPRM/APRM Units	Number of FLOW Units	Number of OPRM Units
BWR-2 with 68 LPRM signals	2	6	2	N/A
BWR-3 with 88 LPRM signals	4	6	2	4
BWR-4 with 124 LPRM signals	10	6	2	4
BWR-5 with 172 LPRM signals	10	6	4	4
BWR-6 with 132 LPRM signals	8	8	4	4
ABWR with 208 LPRM signals	16	4 (Only APRM Units)		4

The following sections describe the individual PRM systems.

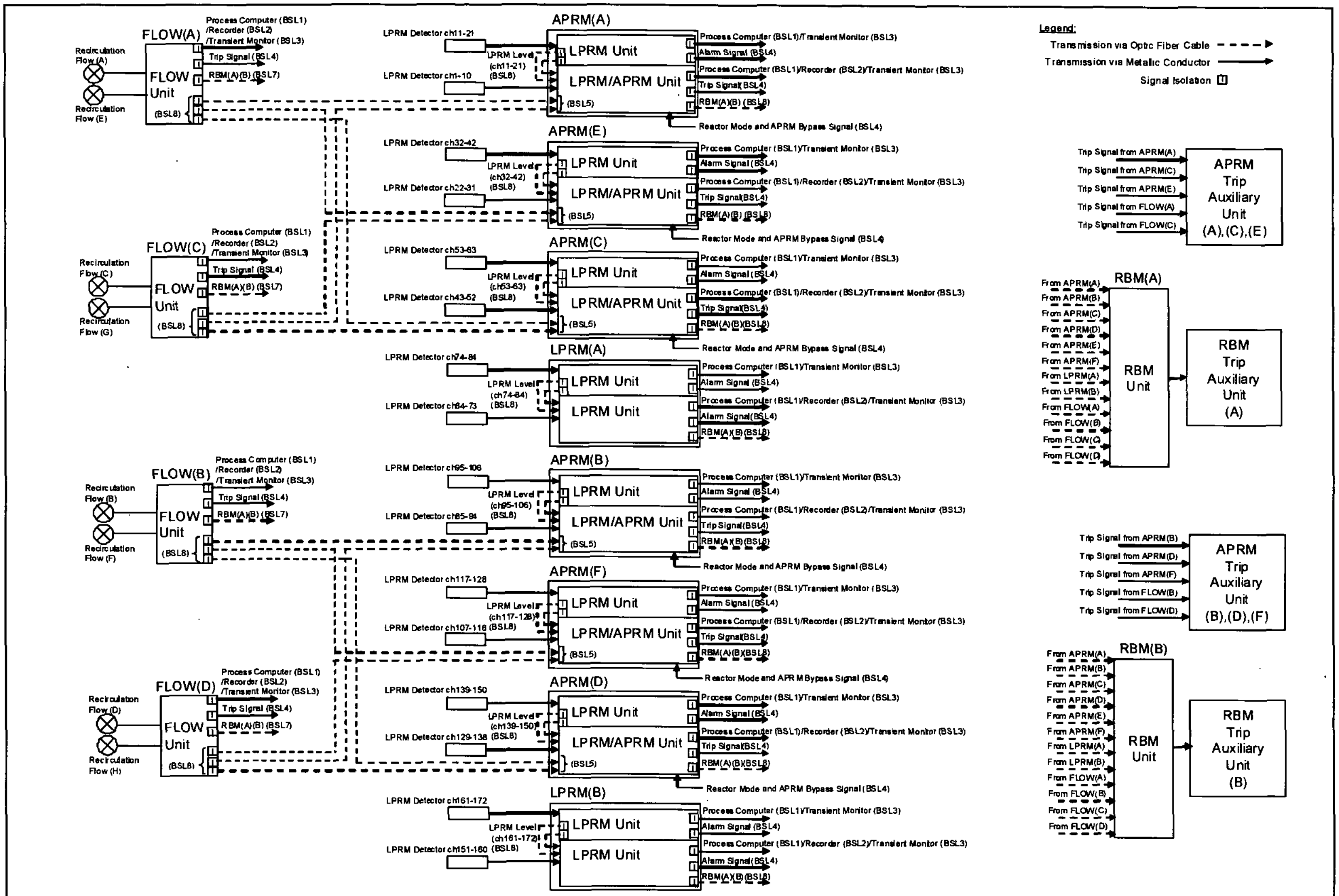
II-A-7.1 System Configuration for BWR-5 with 172 LPRM Signals

Typical PRM system configuration for BWR-5 with 172 LPRM signals is shown in Figure II-A-7-1. The applied modules for this configuration are listed in Table II-A-7-2.

At the PRM system for BWR-5, there are six APRM channels, two LPRM channels and four Recirculation Flow Measurement (FLOW) channels. The LPRM detector sensors are divided into six APRM channels and two LPRM channels. APRM channels, LPRM channels and FLOW channels are divided into two groups where each group consists of three APRM channels, one LPRM channel and two FLOW channels. Each APRM channel contains one LPRM unit and one LPRM/APRM unit. Each LPRM channel contains two LPRM units. Each FLOW channel contains one FLOW unit. Trip auxiliary units which have no FPGA are used for relaying trip signals to other systems. Therefore, FPGA-based safety-related equipment in a typical BWR-5 with 172 LPRM detectors consists of ten LPRM units, six LPRM/APRM units, and four FLOW units. The PRM System can provide the analog signals of the LPRM levels to the OPRM system by a fiber communication as shown in Section II-A-7.7.

The LPRM units identified in Section II-A-4 do not have a function that receives fiber optic communicated data from other units. Therefore, when the PRM system is applied to BWR-5 with 172 LPRM signals, the LPRM/APRM unit is modified from the hardware identified in Section II-A-4 by adding communication receiving capabilities to the specific LPRM unit in LPRM (A) and LPRM (B) channel. This specific LPRM receives LPRM data from the other LPRM in the same LPRM channel, and transmits the LPRM data to RBM. APRM module is replaced by a module which transmits LPRM data from the LPRM units to RBM using a standard, type tested, qualified TRN module.

The modifications described above are minor changes from the hardware identified in Section II-A-4 of this guide and use hardware that has already been type tested and qualified, so additional qualification tests are not required for the modified BWR-5 PRM system.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-1 Typical PRM System Configuration for BWR-5 with 172 LPRM Signal

Table II-A-7-2 Applied Module for BWR-5 PRM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-1		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 4 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 4 FLOW units in the system accordingly.	
LPRM Module	HNS013	172	- 11 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM A, C and E channels. - 12 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM B, D, and F channels - 11 modules in the first LPRM unit and 10 modules in the second LPRM unit in LPRM A channel - 12 modules in the first LPRM unit and 10 modules in the second LPRM unit in LPRM B channel	LPRM function
APRM Module	HNS020	6	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030	8	- 2 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040	4	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091	6	- 1 module in an LPRM/APRM unit	Data reception status and power supply voltage monitoring status indications.
STATUS Module	HNS093	14	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
MUX Module	HNS260	2	- 1 module in one of the 2 LPRM units in an LPRM channel	Multiplexing module for LPRM data transmission
BLANK Module	HNS490	12	- 2 modules in an LPRM unit for APRM A, C and E channels. - 2 modules in one of the 2 LPRM units in LPRM A channel - 1 module in an LPRM unit for APRM B, D and F channels. - 1 module in one of the 2 LPRM units in LPRM B channel	Dummy LPRM module to fill open slots when the LPRM unit is not filled with 13 LPRM Modules.
LVPS Module	HNS500	40	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515	16	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit	Analog outputs to the Transient Monitor
AO Module	HNS516	10	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-1		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 4 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 4 FLOW units in the system accordingly.	
AO Module	HNS517	4	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518	20	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520	20	- 1 module in each unit in the system	Discrete signal input and output module
TRN Module	HNS0531	24	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541	8	- 1 module in an LPRM/APRM unit - 1 module in one of the 2 LPRM units in each LPRM channel	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-7.2 System Configuration for BWR-2 with 68 LPRM Signals

A typical PRM system configuration for BWR-2 with 68 LPRM signals is shown in Figure II-A-7-2. The applied modules for this configuration are listed in Table II-A-7-3. In the BWR-2, FLOW units are classified as non-safety.

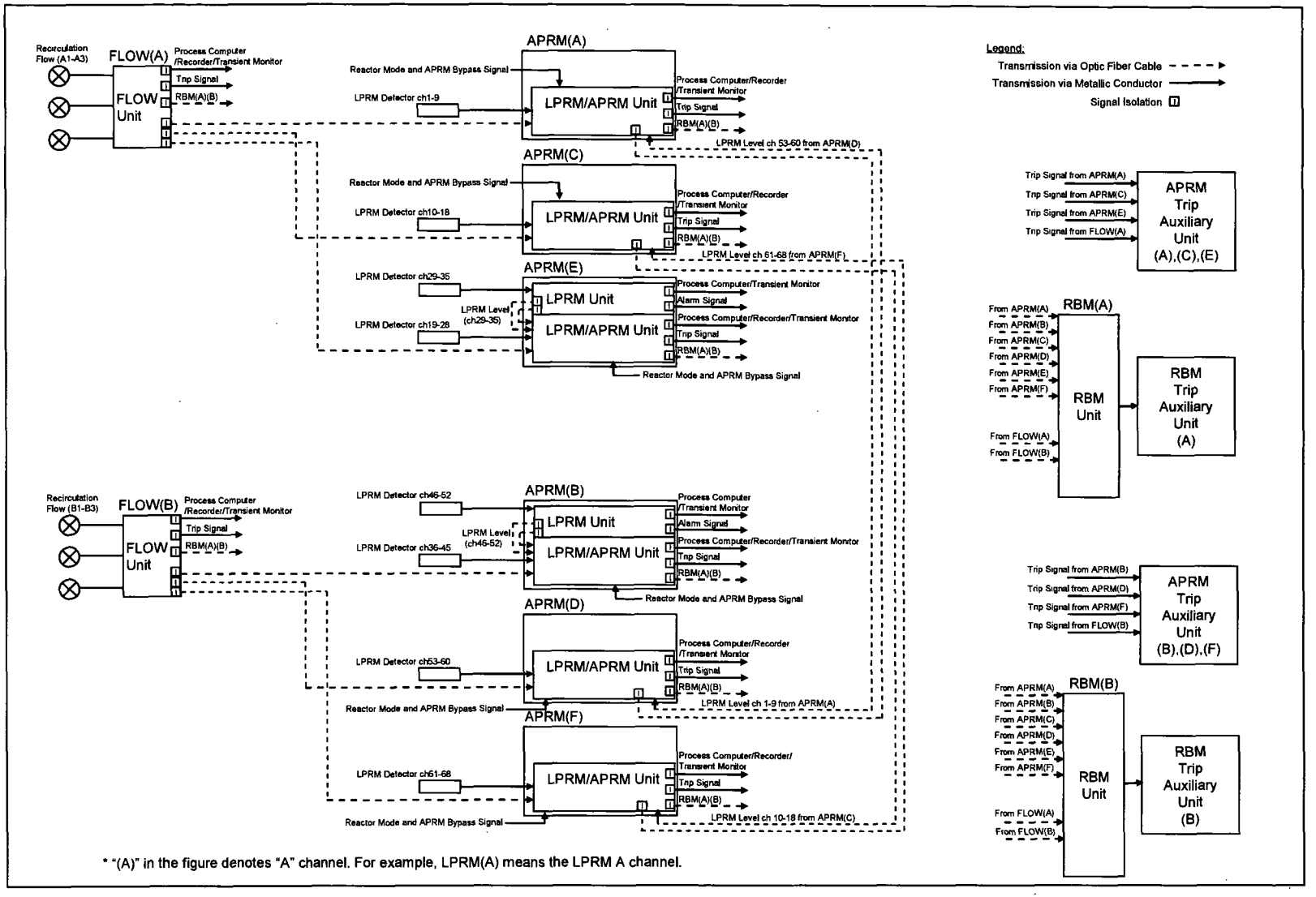
When the PRM system is applied to BWR-2 with 68 LPRM signals, some LPRM detector signals are shared between two common APRM channels as shown in Figure II-A-7-2. To adapt for this signal sharing, the chassis and APRM module for LPRM/APRM unit of APRM (A), (C), (D), and (F) (shown by gray shading in Figure II-A-7-2) needs to be modified from the hardware identified in II-A-4 of this guide as follows:

- Middle plane of the chassis for an LPRM/APRM unit is modified to achieve following functions:
  - Additional TRN module sends common LPRM detector signals to another LPRM/APRM unit in common channels.
  - DIO module sends inoperable status signal of the unit to another LPRM/APRM unit in common channels.
  - APRM module receives inoperable status signal of another LPRM/APRM unit in common channels via DIO module.
- APRM module is modified to change allowable LPRM bypass number in accordance with the inoperative status signal from another LPRM/APRM unit in common channels.
- OPRM units are not applicable for BWR-2.

Since the Reactor Recirculation System for BWR-2 consists of three or five external recirculation loops, the chassis and FLOW module for FLOW unit of FLOW (A) and (B) need to be modified from the hardware identified in Section II-A-4 as follows:

- Middle plane of the chassis for FLOW unit is modified to install and to connect three or five SQ-ROOT modules
- FLOW module is modified to connect three or five SQ-ROOT modules and to calculate total flow rate using loop flows from all of SQ-ROOT modules installed in FLOW unit

The modifications described above are minor changes from the hardware identified in Section II-A-4 of this guide and use hardware that has already been type tested and qualified, so additional qualification tests are not required for the modified BWR-2 PRM system.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-2 Typical PRM System Configuration for BWR-2 with 68 LPRM Signal

Table II-A-7-3 Applied Module for BWR-2 PRM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-2		Functional Description
		Total number	Description Note: The system consists of 6 APRM channels (A through F) and 2 FLOW units. The APRM channels B and E have 1 LPRM/APRM unit and 1 LPRM unit. The APRM channels A, C, D and F have 1 APRM/LPRM unit. There are 6 APRM/LPRM units, 2 LPRM units and 2 FLOW units in the system accordingly.	
LPRM Module	HNS013	68	- 7 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM B and E channels - 9 modules in an LPRM/APRM unit for APRM A and C channels - 8 modules in an LPRM/APRM unit for APRM D and F channels	LPRM function
APRM Module	HNS020	6	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030	6	- 3 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040	2	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091	6	- 1 module in an LPRM/APRM unit	Data reception status, power supply voltage monitoring status indications
STATUS Module	HNS093	4	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
BLANK Module	HNS490	18	- 6 modules in an LPRM unit for APRM B and E channels - 1 module in an LPRM/APRM unit for APRM A and C channels - 2 modules in an LPRM/APRM unit for APRM D and F channels	Dummy LPRM module to fill open slots
LVPS Module	HNS500	20	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515	8	- 1 module in an LPRM unit - 1 module in an LPRM/APRM unit	Analog outputs to the Transient Monitor
AO Module	HNS516	8	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders
AO Module	HNS517	2	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518	10	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520	10	- 1 module in each unit in the system	Discrete signal input and output module

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-2		Functional Description
		Total number	Description Note: The system consists of 6 APRM channels (A through F) and 2 FLOW units. The APRM channels B and E have 1 LPRM/APRM unit and 1 LPRM unit. The APRM channels A, C, D and F have 1 APRM/LPRM unit. There are 6 APRM/LPRM units, 2 LPRM units and 2 FLOW units in the system accordingly.	
TRN Module	HNS0531	16	- 1 module in an LPRM unit and 1 module in an LPRM/APRM unit for APRM B and E channels - 2 modules in an LPRM/APRM unit for APRM A, C, D and F channels - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541	6	- 1 module in an LPRM/APRM unit	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-7.3 Configuration for BWR-3 with 88 LPRM Signals

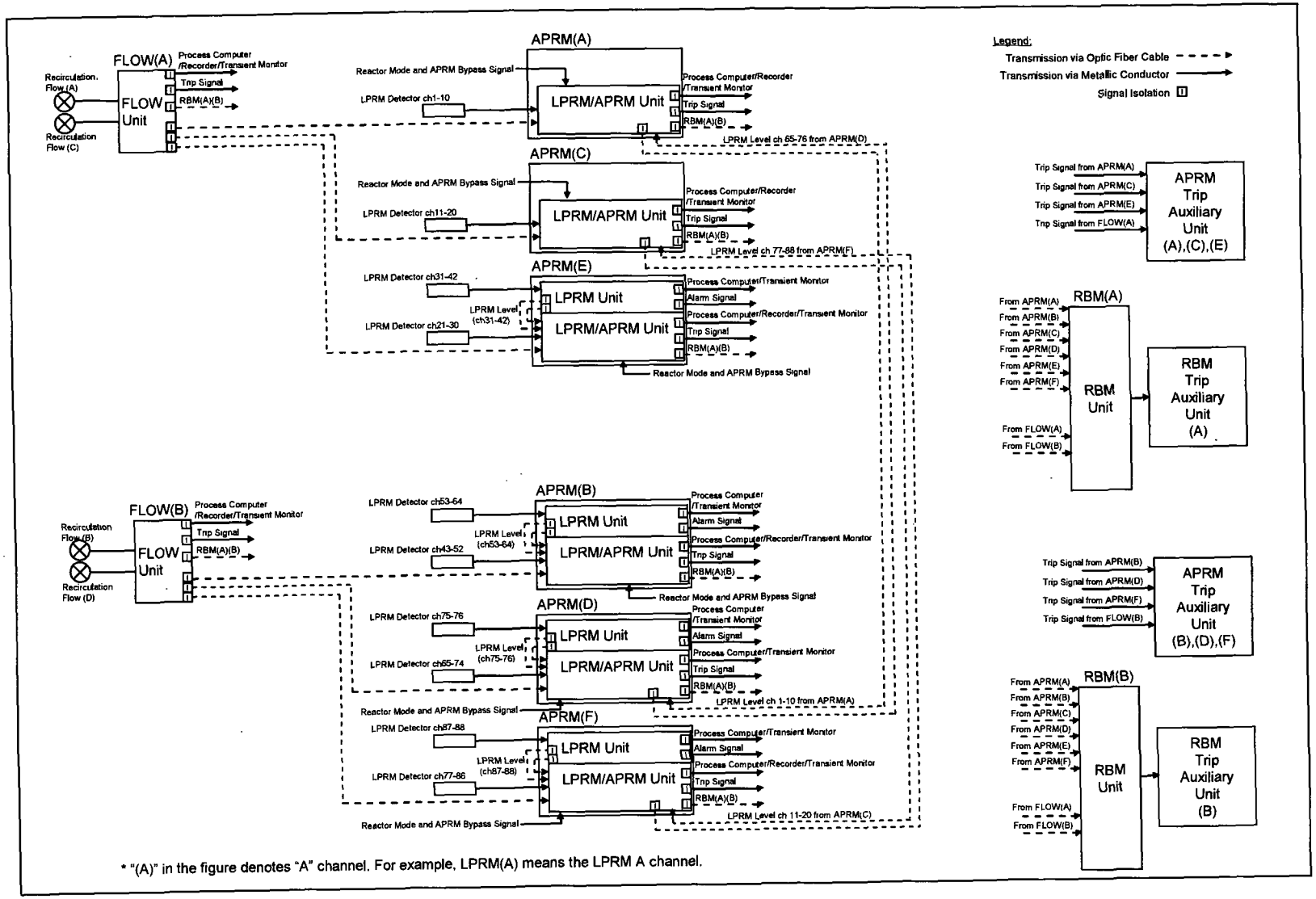
A typical PRM system configuration for BWR-3 with 88 LPRM signals is shown in Figure II-A-7-3. The applied modules for this configuration are listed in Table II-A-7-4.

The PRM system provides the analog signals of the LPRM levels to the OPRM system through a fiber communication link as shown in Section II-A-7.8.

When the PRM system is applied to BWR-3 with 88 LPRM signals, some LPRM detector signals are shared between two common APRM channels as shown in Figure II-A-7-3. To adapt for this signal sharing, the chassis and APRM module for LPRM/APRM unit of APRM (A), (C), (D), and (F) (shown by gray shading in Figure II-A-7-3. need to be modified from the hardware identified in Section II-A-4 of this guide as follows:

- Middle plane of the chassis for LPRM/APRM unit is modified to achieve following functions:
  - Additional TRN module sends common LPRM detector signals to another LPRM/APRM unit in common channels.
  - DIO module sends inoperable status signal of the unit to another LPRM/APRM unit in common channels.
  - APRM module receives inoperable status signal of another LPRM/APRM unit in common channels via DIO module.
- APRM module is modified to change allowable LPRM bypass number in accordance with the inoperative status signal from another LPRM/APRM unit in common channels.

The modifications described above are minor changes from the hardware identified in Section II-A-4 of this guide and use hardware that has already been type tested and qualified, so additional qualification tests are not required for the modified BWR-3 PRM system.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-3 Typical PRM System Configuration for BWR-3 with 88 LPRM Signals

Table II-A-7-4 Applied Module for BWR-3 PRM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-3		Functional Description
		Total number	Description Note: The system consists of 6 APRM channels (A through F) and 2 FLOW units. The APRM channels E, B, D and F have 1 LPRM/APRM unit and 1 LPRM unit. The APRM channels A and C have 1 APRM/LPRM unit. There are 6 APRM/LPRM units, 4 LPRM units and 2 FLOW units in the system accordingly.	
LPRM Module	HNS013	88	- 12 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM B and E channels - 10 modules in an LPRM/APRM unit for APRM A and C channels - 2 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM D and F channels	LPRM function
APRM Module	HNS020	6	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030	4	- 2 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040	2	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091	6	- 1 module in an LPRM/APRM unit	Data reception status, power supply voltage monitoring status indications.
STATUS Module	HNS093	6	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
BLANK Module	HNS490	24	- 1 module in an LPRM unit for APRM B and E channels - 11 modules in an LPRM unit for APRM D and F channels	Dummy LPRM module to fill open slots
LVPS Module	HNS500	24	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515	10	- 1 module in an LPRM unit - 1 module in an LPRM/APRM unit	Analog outputs to the Transient Monitor
AO Module	HNS516	8	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders
AO Module	HNS517	2	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518	12	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520	12	- 1 module in each unit in the system	Discrete signal input and output module

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-3		Functional Description
		Total number	Description Note: The system consists of 6 APRM channels (A through F) and 2 FLOW units. The APRM channels E, B, D and F have 1 LPRM/APRM unit and 1 LPRM unit. The APRM channels A and C have 1 APRM/LPRM unit. There are 6 APRM/LPRM units, 4 LPRM units and 2 FLOW units in the system accordingly.	
TRN Module	HNS0531	20	- 1 module in an LPRM unit and 2 modules in an LPRM/APRM unit for APRM B, D,E and F channels - 2 modules in an LPRM/APRM unit for APRM A and C channels - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541	8	- 1 module in an LPRM/APRM unit for APRM A, B, C and E channels - 2 module in an LPRM/APRM unit for APRM D and F channels	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-7.4 Configuration for BWR-4 with 124 LPRM Signals

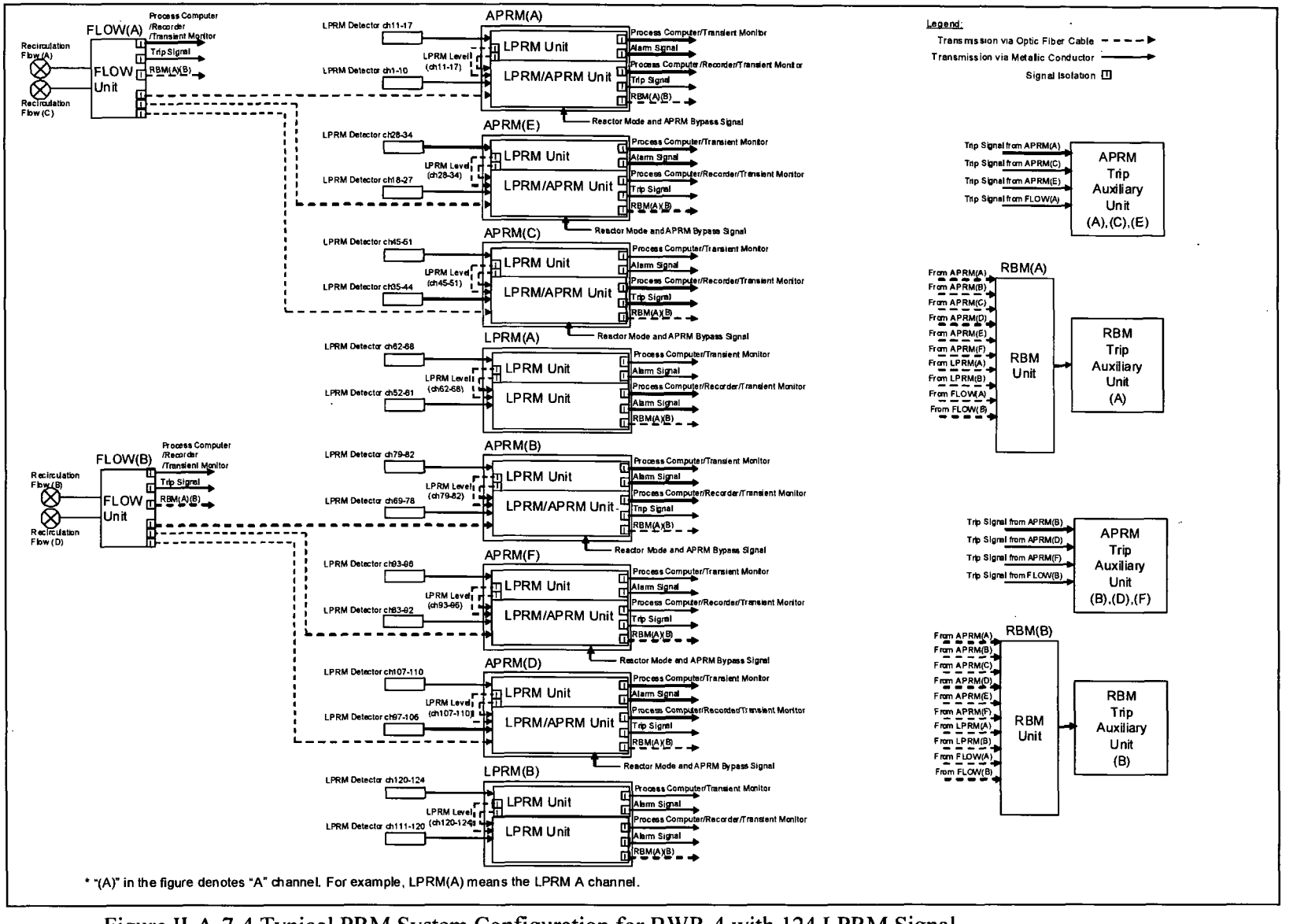
A typical PRM system configuration for BWR-4 with 124 LPRM signals is shown in Figure II-A-7-4 The applied modules for this configuration are listed in Table II-A-7-5.

The PRM system provides the analog signals of the LPRM levels to the OPRM system through a fiber communication link as shown in Section II-A-7.7.

When the PRM system is applied to BWR-4 with 124 LPRM signals, LPRM/APRM unit needs to be modified from the hardware identified in Section II-A-4 of this guide as follows, which is used for the specific LPRM unit in LPRM (A) and LPRM (B) channel. This specific LPRM receives LPRM data from the other LPRM unit in the same LPRM channel, and transmits the LPRM data to RBM.

- APRM module is replaced with a module which transmits LPRM data from both LPRM units to the RBM using a TRN module.

The modifications described above are minor changes from the hardware identified in Section II-A-4 of this guide and use hardware that has already been type tested and qualified, so additional qualification tests are not required for the modified BWR-4 PRM system.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-4 Typical PRM System Configuration for BWR-4 with 124 LPRM Signal

Table II-A-7-5 Applied Module for BWR-4 PRM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-4		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 2 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 2 FLOW units in the system accordingly.	
LPRM Module	HNS013	124	- 7 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM A, C and E channels. - 4 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM B, D, and F channels - 7 modules in the first LPRM unit and 10 module in the second LPRM unit in LPRM A channel - 4 modules in the first LPRM unit and 10 module in the second LPRM unit in LPRM B channel	LPRM function
APRM Module	HNS020	6	- 1 module in an LPRM/APRM unit	APRM function
SQ-ROOT Module	HNS030	4	- 2 modules in a FLOW uni	Square root arithmetic function
FLOW Module	HNS040	2	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091	6	- 1 module in an LPRM/APRM unit	Data reception status, power supply voltage monitoring status indications
STATUS Module	HNS093	12	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
MUX Module	HNS260	2	- 1 module in one of the 2 LPRM units in an LPRM channel	Multiplexing module for LPRM data transmission
BLANK Module	HNS490	60	- 6 modules in an LPRM unit for APRM A, C and E channels. - 6 modules in one of the 2 LPRM units in LPRM A channel - 9 modules in an LPRM unit for APRM B, D and F channels. - 9 modules in one of the 2 LPRM units in LPRM B channel	Dummy LPRM module to fill open slots when the LPRM unit is not filled with 13 LPRM Modules.
LVPS Module	HNS500	36	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515	16	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit	Analog outputs to the Transient Monitor
AO Module	HNS516	8	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-4		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through F) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, 2 LPRM channels (A and B) with 2 LPRM units in each LPRM channel, and 2 FLOW units. There are 6 APRM/LPRM units, 10 LPRM units and 2 FLOW units in the system accordingly.	
AO Module	HNS517	2	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518	18	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520	18	- 1 module in each unit in the system	Discrete signal input and output module
TRN Module	HNS0531	20	- 1 module in an LPRM/APRM unit - 1 module unit in an LPRM unit - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541	8	- 1 module in an LPRM/APRM unit - 1 module in one of the 2 LPRM units in each LPRM channel	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-7.5 Configuration for BWR-6 with 132 LPRM Signals

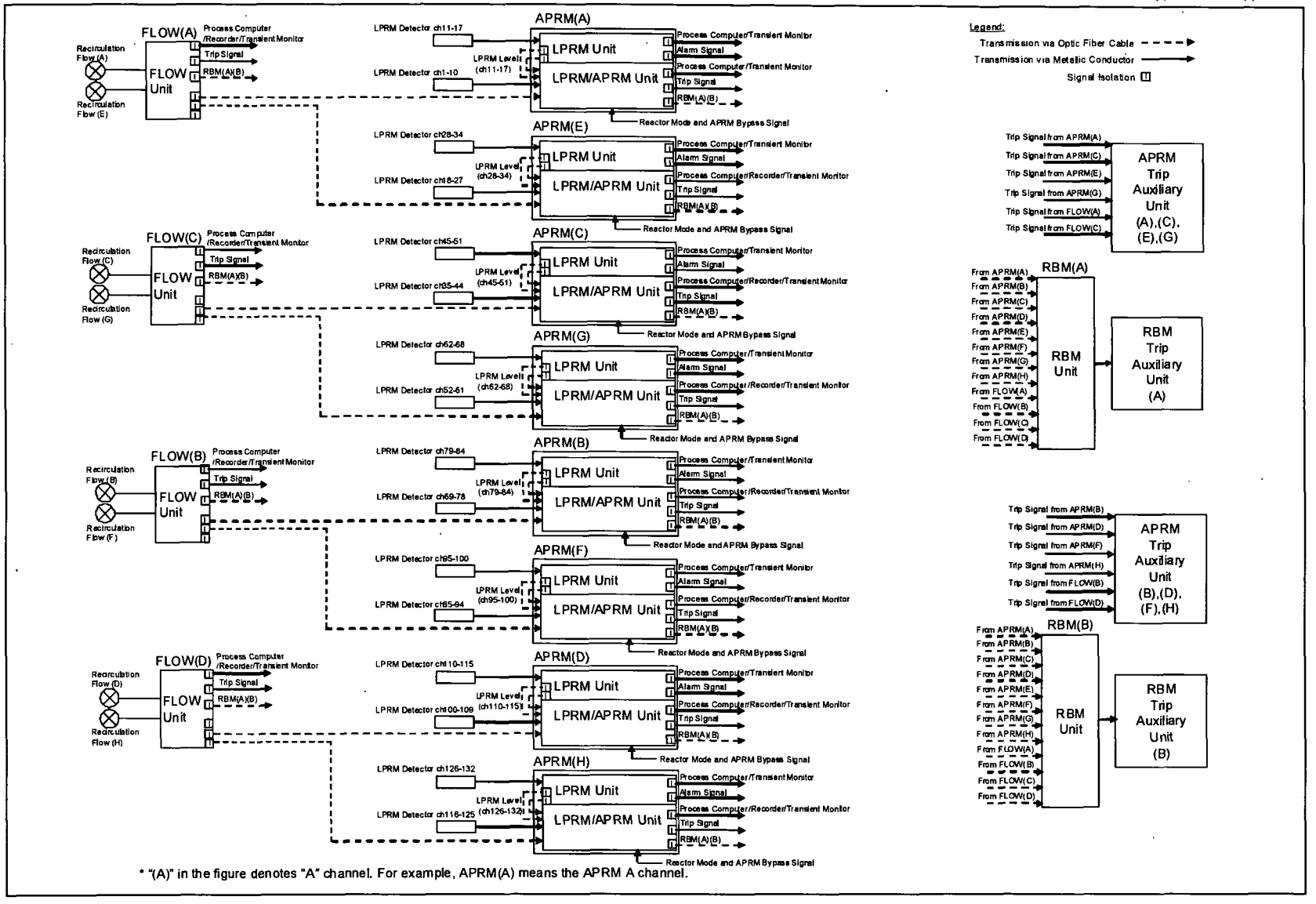
A typical PRM system configuration for BWR-6 with 132 LPRM signals is shown in Figure II-A-7-5. The applied modules for this configuration are listed in Table II-A-7-6.

The PRM system provides the signals of the LPRM levels to the OPRM system through a fiber communication link as shown in Section II-A-7.7.

When the PRM system is applied to BWR-6 with 132 LPRM signals, the following modifications from the hardware identified in Section II-A-4 are necessary

- Five LPRM modules, which are not used for BWR-6 application, in the LPRM unit used for APRM (A), (E), (C), and (G) channels are replaced with five BLANK modules.
- Six LPRM modules, which are not used for BWR-6 application, in the LPRM unit used for APRM (B), (F), (D), and (H) channels are replaced with six BLANK modules.

The modifications described above are minor changes from the hardware identified in Section II-A-4 of this guide and use hardware that has already been type tested and qualified, so additional qualification tests are not required for the modified BWR-6 PRM system.



* "(A)" in the figure denotes "A" channel. For example, APRM(A) means the APRM A channel.

Figure II-A-7-5 Typical PRM System Configuration for BWR-6 with 132 LPRM Signals

Table II-A-7-6 Applied Module for BWR-6 PRM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-5		Functional Description
		Total Number	Description Note: The system consists of 6 APRM channels (A through H) with 1 LPRM/APRM unit and 1 LPRM unit in each APRM channel, and 4 FLOW units. There are 8 APRM/LPRM units, 8 LPRM units and 4 FLOW units in the system accordingly.	
LPRM Module	HNS013	132	- 7 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM A, C, E and G channels. - 6 modules in an LPRM unit and 10 modules in an LPRM/APRM unit for APRM B, D, F and H channels	LPRM function
APRM Module	HNS020	8	- 1 module in an LPRM/APRM uni	APRM function
SQ-ROOT Module	HNS030	8	- 2 modules in a FLOW unit	Square root arithmetic function
FLOW Module	HNS040	4	- 1 module in a FLOW unit	Recirculation-flow calculation, trip and alarm functions
STATUS Module	HNS091	8	- 1 module in an LPRM/APRM unit	Data reception status, power supply voltage monitoring status indications
STATUS Module	HNS093	12	- 1 module in an LPRM unit - 1 module in a FLOW unit	Power supply voltage monitoring status indication
BLANK Module	HNS490	52	- 6 modules in an LPRM unit for APRM A, C, E and G channels - 7 modules in an LPRM unit for APRM B, D, F and H channels	Dummy LPRM module to fill open slots when the LPRM unit is not filled with 13 LPRM Modules.
LVPS Module	HNS500	40	- 2 modules in each unit in the system	+5V and ±15V power supply to each module
AO Module	HNS515	16	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit	Analog outputs to the Transient Monitor
AO Module	HNS516	12	- 1 module in an LPRM/APRM unit - 1 module in a FLOW unit	Analog outputs to recorders
AO Module	HNS517	4	- 1 module in a FLOW unit	Analog outputs to the Transient Monitor
AO Module	HNS518	20	- 1 module in each unit in the system	Analog outputs to the process computer
DIO Module	HNS520	20	- 1 modules in each unit in the system	Discrete signal input and output module
TRN Module	HNS0531	24	- 1 module in an LPRM/APRM unit - 1 module in an LPRM unit - 2 modules in a FLOW unit	Optical data transmission module
RCV Module	HNS0541	8	- 1 module in an LPRM/APRM unit	Optical data reception module

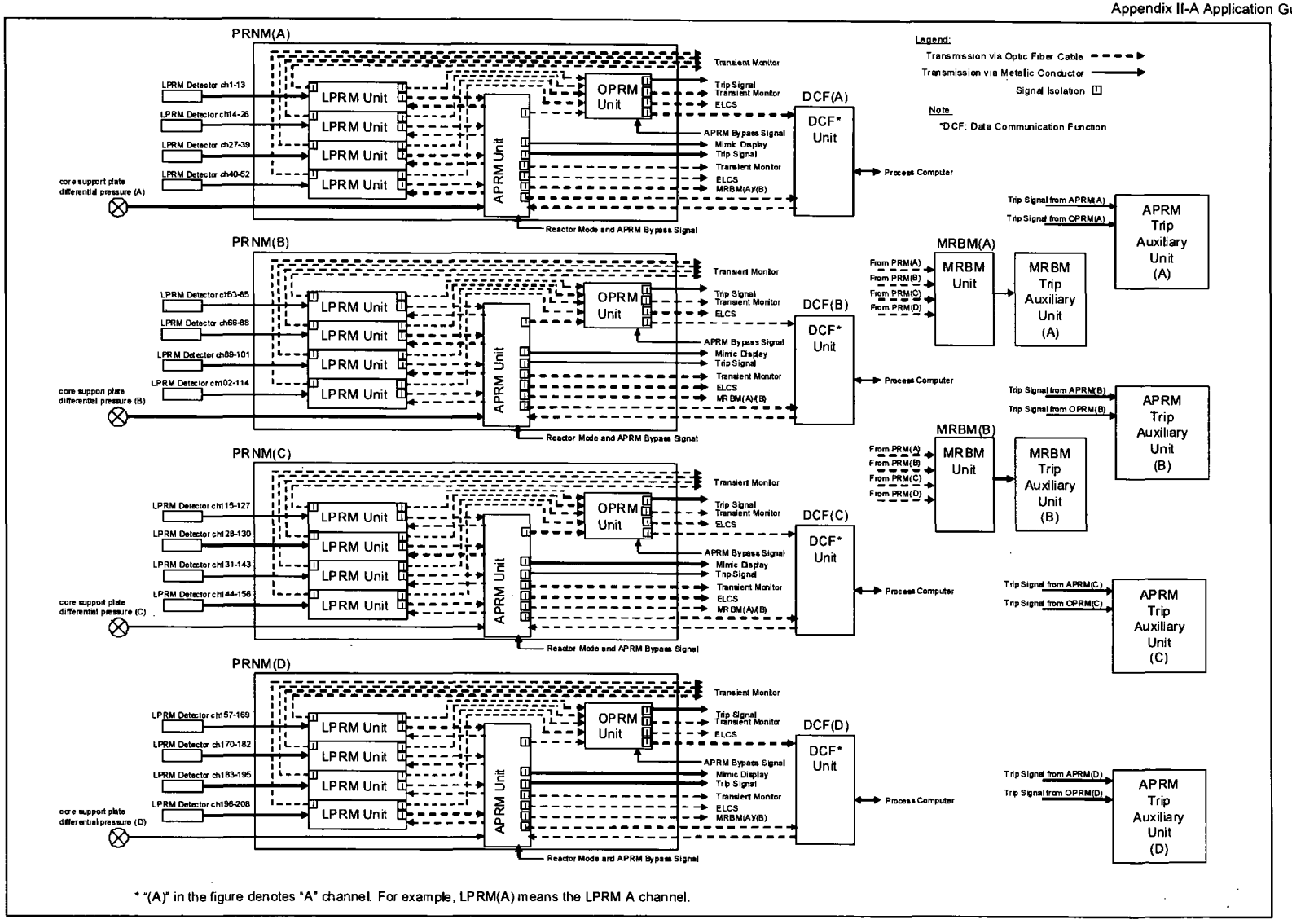
*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-7.6 Configuration for ABWR with 208 LPRM Signals

Typical PRNM system configuration for ABWR with 208 LPRM signals is shown in Figure **II-A-7-6**. The applied safety-related modules for this configuration are listed in Table II-A-7-7. The PRNM system includes OPRM.

When the PRNM system is applied to ABWR with 208 LPRM signals, the following new hardware will be applied as safety-related application, in addition to the hardware identified in Section II-A-4 of this guide:

- A module which calculates core flow from core support plate differential pressure.
- A module which transmits APRM data to the Multi-channel RBM (MRBM) and Process Computer using a TRN module that also indicates the unit status.
- A module which transmits LPRM data to the APRM unit and OPRM unit using a TRN module that also indicates the unit status.
- Chassis of APRM unit, which is designed based on the design of LPRM/APRM unit.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-6 Typical PRNM System Configuration for ABWR with 208 LPRM Signals

Table II-A-7-7 Applied Module for ABWR PRNM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-7-6		Functional Description
		Total Number	Description Note: The system consists of 4 divisions with 1 APRM unit, 4 LPRM units and 1 OPRM unit in each division.	
LPRM Module	HNS0302	208	- 13 modules in a LPRM unit	LPRM function
APRM Module	HNS0311	4	- 1 module in an APRM unit	APRM function
FLOW Module	HNS0321	4	- 1 module in an APRM unit	Core-flow calculation, trip and alarm functions
CAL/ST Module	HNS0330	16	- 1 module in an LPRM unit	Power status and Input status indications. LPRM calibration currents are calculated and provided to LPRM modules.
GAF/ST Module	HNS0341	4	- 1 module in an APRM unit	Power status and Input status indications. Gain Adjustment Factor (GAF) download and output to LPRM units
CELL Module	HNS0400	4	- 1 module in an OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410	4	- 1 module in an OPRM unit	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420	4	- 1 module in an OPRM unit	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.
PBD Module	HNS0430	4	- 1 module in an OPRM unit	Period-based Detection Algorithm judgment is performed.
LVPS Module	HNS0500	48	- 2 modules in each unit	+5V and ±15V power supply to each module
AO Module	HNS0515	20	- 1 module in LPRM unit - 1 module in APRM unit	Analog outputs to the mimic display on the main control panel and the Transient Monitor
DIO Module	HNS0520	24	- 1 module in a LPRM unit - 1 module in a APRM unit - 1 module in a OPRM unit	Discrete signal input and output module
TRN Module	HNS0531	36	- 1 module in a LPRM unit - 3 modules in a APRM unit - 2 modules in a OPRM unit	Optical data transmission module
RCV Module	HNS0541	32	- 1 module in a LPRM unit - 2 modules in a APRM unit - 2 modules in a OPRM unit	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

The OPRM unit configuration for ABWR is shown in Figure II-A-7-7 and described in Table II-A-7-8.

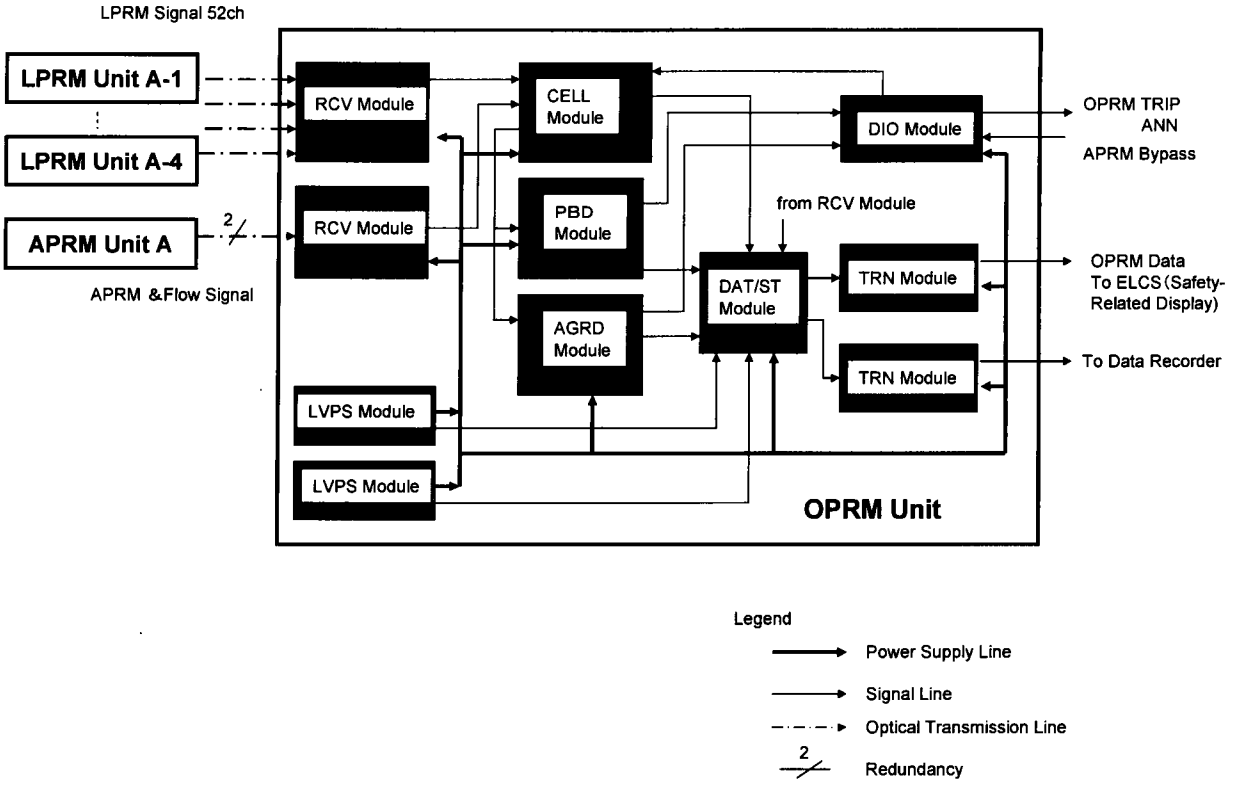


Figure II-A-7-7 Unit/Module Configuration for OPRM for ABWR

Table II-A-7-8 Unit/Module Configuration for OPRM for ABWR

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-A-7-7		Functional Description
		Total number	Description Note: The system has 4 divisions with 1 OPRM unit in each division.	
CELL Module	HNS0400	4	- 1 module in each OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410	4	- 1 module in each OPRM unit	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420	4	- 1 module in each OPRM unit	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.
PBD Module	HNS0430	4	- 1 module in each OPRM unit	Period-based Detection Algorithm judgment is performed.
LVPS Module	HNS0500	8	- 2 modules in each OPRM unit	+5V and ±15V power supply to each module
DIO Module	HNS0520	4	- 1 module in each OPRM unit	Discrete signal input and output module
TRN Module	HNS0531	8	- 2 modules in each OPRM unit	Optical data transmission module
RCV Module	HNS0541	8	- 2 modules in each OPRM unit	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

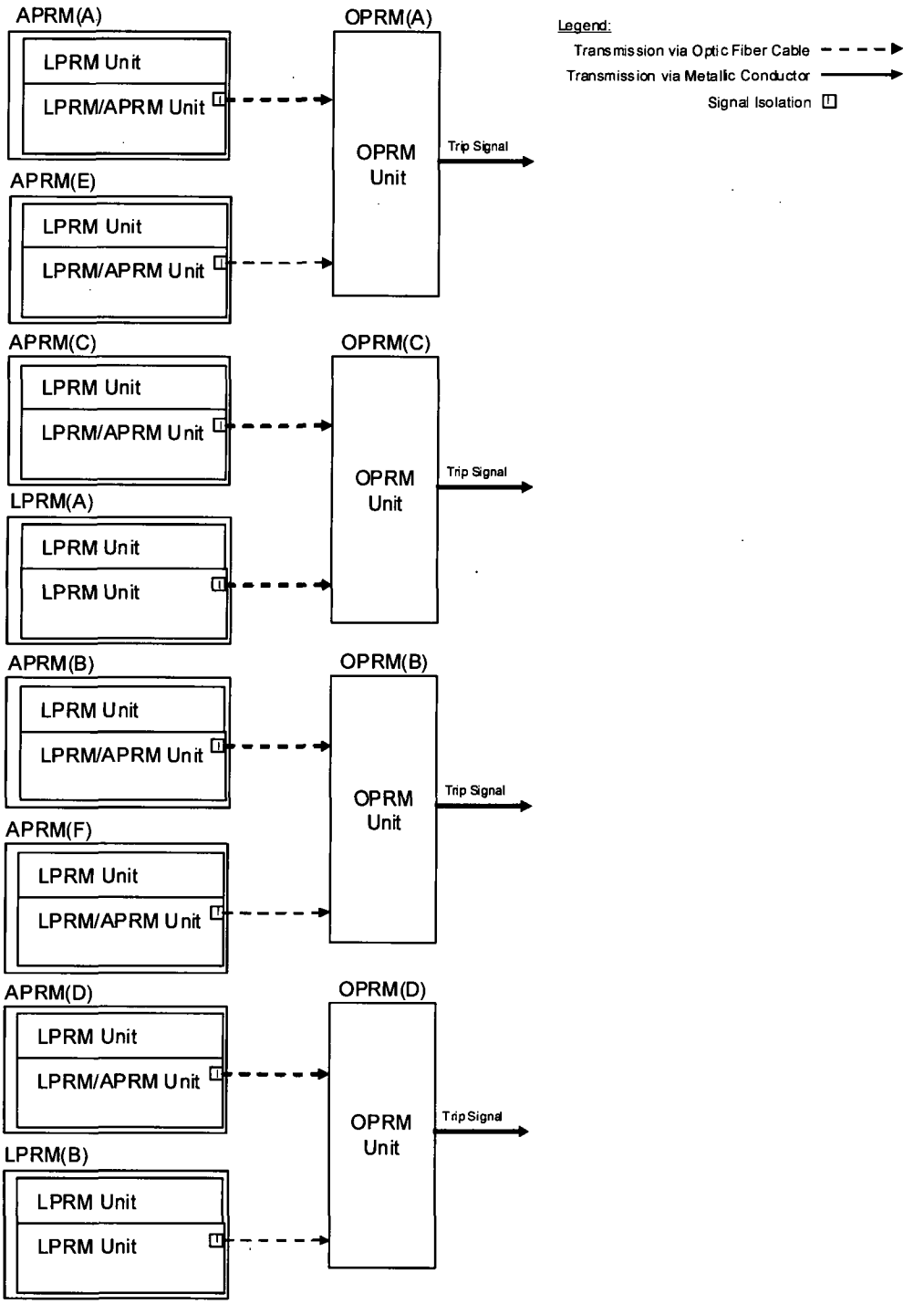
Since the PRNM system for ABWR includes the above new hardware in addition to the hardware identified in Section II-A-4 of this guide, the ABWR PRNM and OPRM will be type tested.

II-A-7.7 Interface Configuration between PRM and OPRM for Large Core BWR

Typical interface configuration between PRM and OPRM for BWR with 120 or more LPRM signals (large core) is shown in Figure II-A-7-8 and another configuration for BWR-6 is shown in Figure II-A-7-9. The applied safety-related modules for OPRM in these configurations are listed in Table II-A-7-9. APRM and OPRM connections for an ABWR are shown in Figure II-A-7-6. Same fiber optic communication boards are used although the connections are different between the large core application and the small core application

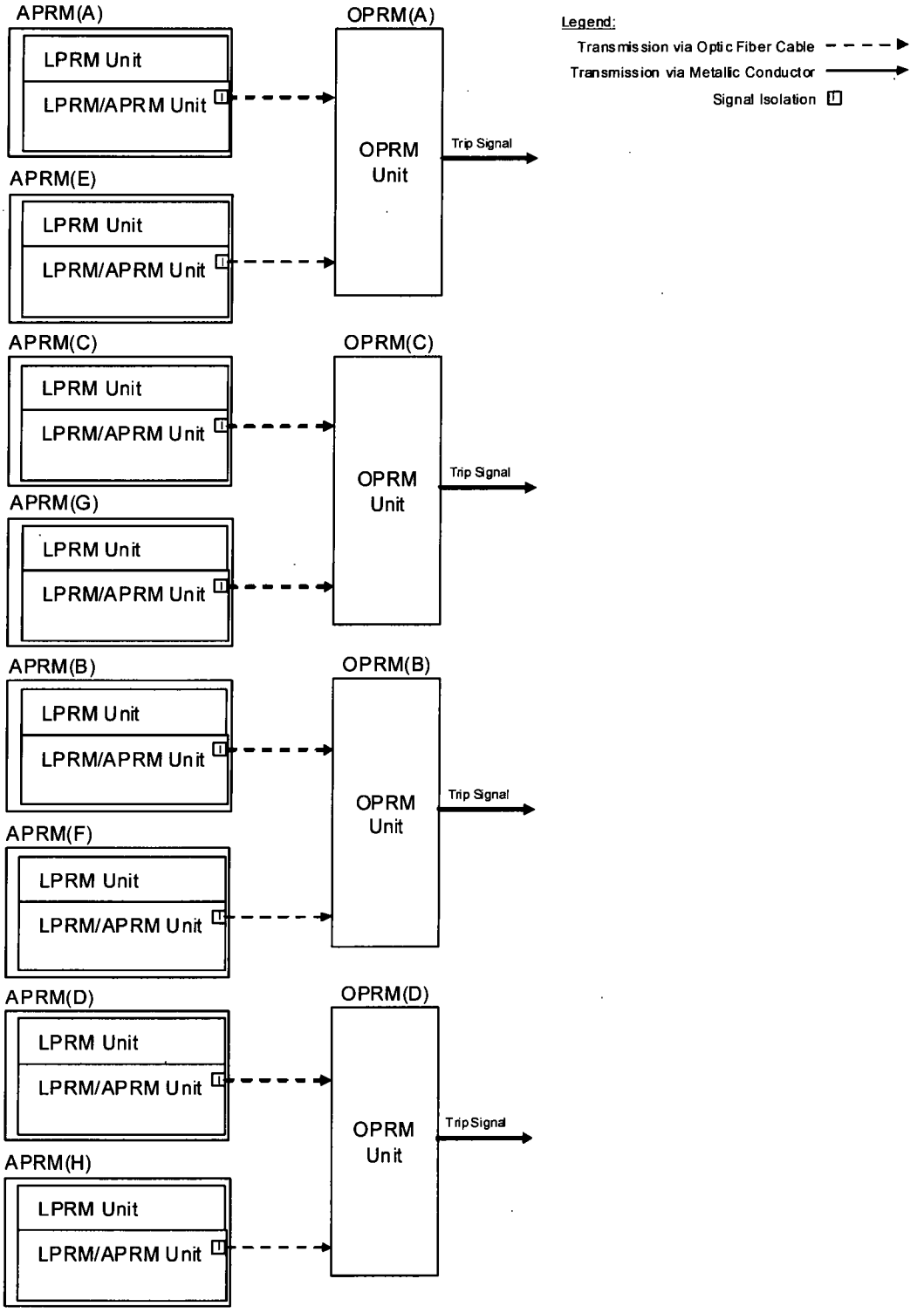
LPRM units transmit their LPRM data to the OPRM units. LPRM/APRM units transmit their LPRM data, APRM data, and FLOW data to the OPRM units.

The interface configuration provided in this guide provides separation and isolation between electrical divisions and channels, based on the existing plant requirements.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-8 Typical Interface Configuration between PRM and OPRM for Large Core BWR except BWR-6



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-9 Typical Interface Configuration between PRM and OPRM for BWR-6

Table II-A-7-9 Applied Module for Large Core OPRM

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-A-7-8 and Figure II-A-7-9		Functional Description
		Total number	Description Note: The system has 4 OPRM units.	
CELL Module	HNS0400	4	- 1 module in each OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410	4	- 1 module in each OPRM unit s	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420	4	- 1 module in each OPRM unit	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.
PBD Module	HNS0430	4	- 1 module in each OPRM unit	Period-based Detection Algorithm judgment is performed.
LVPS Module	HNS0500	8	- 2 modules in each OPRM unit	+5V and ±15V power supply to each module
DIO Module	HNS0520	4	- 1 module in each OPRM unit	Discrete signal input and output module
TRN Module	HNS0531	8	- 2 modules in each OPRM unit	Optical data transmission module
RCV Module	HNS0541	8	- 2 modules in each OPRM unit	Optical data reception module

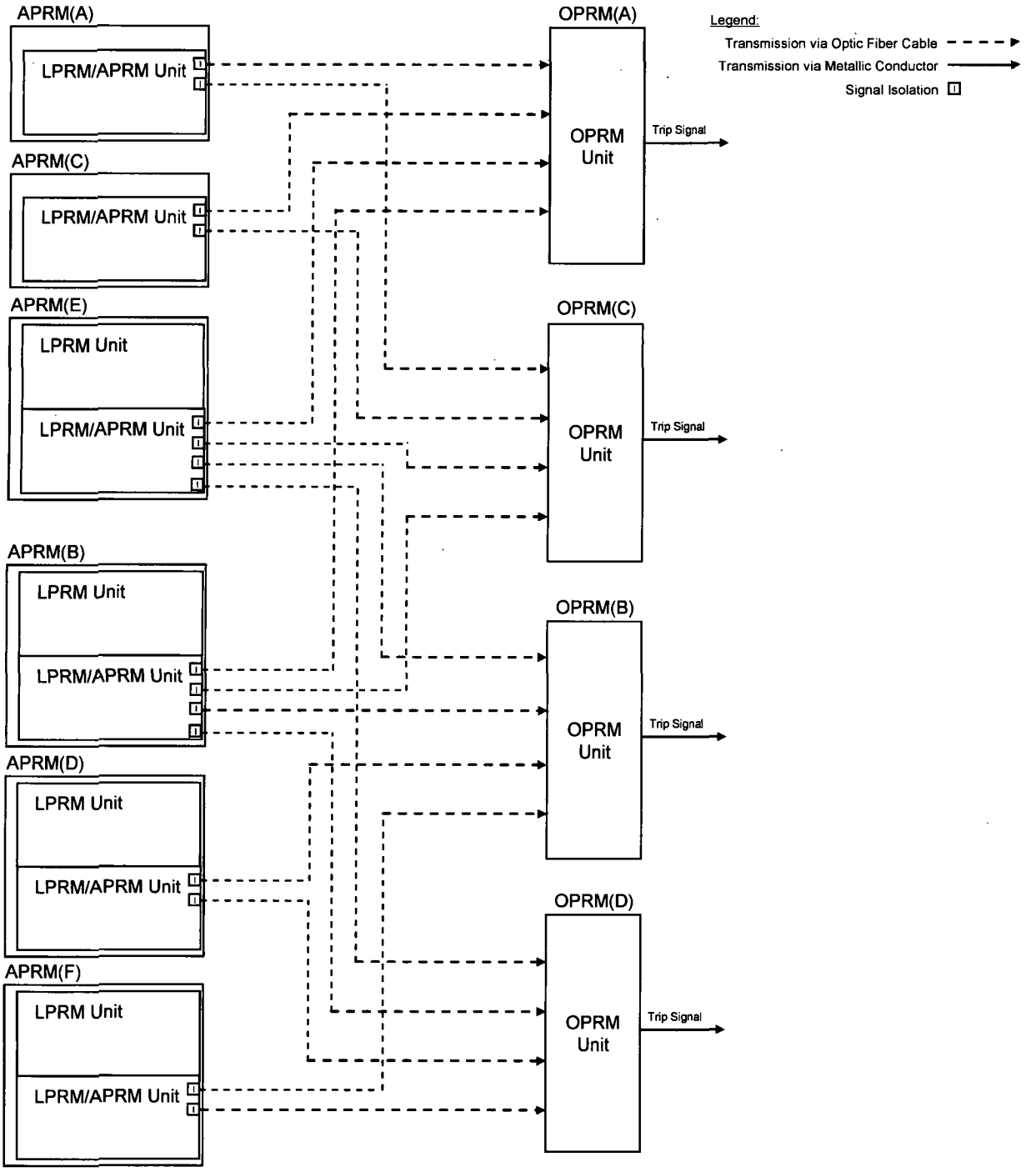
**1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-7.8 Interface Configuration between PRM and OPRM for Small Core BWR

Typical interface configuration between PRM and OPRM for BWR with less than 120 LPRM signals (small core) is shown in Figure II-A-7-10. The applied safety-related modules for OPRM in this configuration are listed in Table II-A-7-10.

LPRM units transmit their LPRM data to the OPRM units. LPRM/APRM units transmit their LPRM data, APRM data, and FLOW data to the OPRM units.

The interface configuration provided in this guide provides separation and isolation between electrical divisions and channels, based on the existing plant requirements.



* "(A)" in the figure denotes "A" channel. For example, LPRM(A) means the LPRM A channel.

Figure II-A-7-10 Typical Interface Configuration between PRM and OPRM for Small Core BWR

Table II-A-7-10 Applied Module for Small Core OPRM

Module Name	Module Model Number*1	Number of Applied Module for OPRM System Configuration shown in Figure II-A-7-10		Functional Description
		Total number	Description Note: The system has 4 OPRM units.	
CELL Module	HNS0400	4	1 module in each OPRM unit	LPRM Levels are converted to Normalized Oscillation Signal
DAT/ST Module	HNS0410	4	1 module in each OPRM unit s	Power status and Input status indications OPRM data are multiplexed
AGRD Module	HNS0420	4	1 module in each OPRM unit	Amplitude-Based Detection Algorithm judgment is performed. Growth Rate-Based Detection Algorithm judgment is performed.
PBD Module	HNS0430	4	1 module in each OPRM unit	Period-based Detection Algorithm judgment is performed.
LVPS Module	HNS0500	8	2 modules in each OPRM unit	+5V and ±15V power supply to each module
DIO Module	HNS0520	4	1 module in each OPRM unit	Discrete signal input and output module
TRN Module	HNS0531	8	2 modules in each OPRM unit	Optical data transmission module
RCV Module	HNS0541	8	2 modules in each OPRM unit	Optical data reception module

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-8 SRNM System Configuration for BWRs (BWR-2, BWR-3, BWR-4, BWR-5, BWR-6) and ABWR

The number of Startup Range Neutron Monitor (SRNM) units which would be used for other BWR designs will vary. This section provides a comparison between the SRNM system units that would be used for the various types of BWRs and ABWR. The SRNM modules and units are identical, with the number of units the only difference between the BWR models.

II-A-8.1 System Configuration for ABWR with 10 SRNM signals

A typical SRNM system configuration for an ABWR with 10 SRNM signals is shown in Figure II-A-8-1. The applied modules for this configuration are listed in Table II-A-8-1. In Figure II-A-8-1, only the SRNM units are FPGA-based safety-related equipment.

Since the SRNM system for ABWR includes SRNM specific hardware, additional qualification type tests are required for the specific hardware.

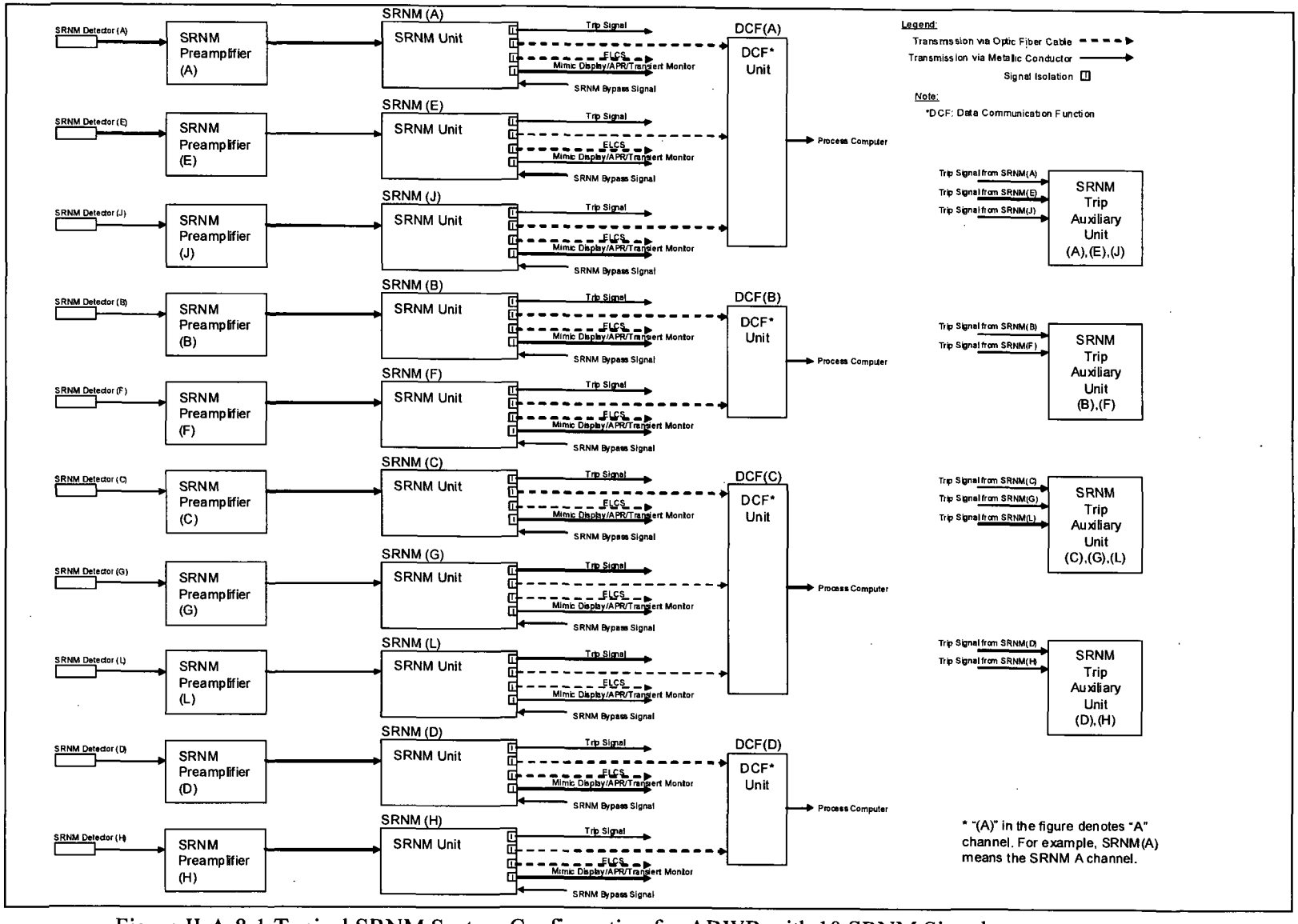


Figure II-A-8-1 Typical SRNM System Configuration for ABWR with 10 SRNM Signals

Table II-A-8-1 Applied Module for ABWR SRNM system

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-8-1		Functional Description
		Total Number	Description Note: The system has 10 channels with 1 SRNM unit in each channel.	
SRNM Module	HNS0101	10	- 1 module in a SRNM unit	SRNM signal processing function. Count rate, neutron flux, logarithmic % power, and linear % power are calculated from the neutron flux signal and are displayed them.
TRIP Module	HNS0117	10	- 1 module in a SRNM unit	Changing and display of trip setpoints and Trip judgment
PARAMETER Module	HNS0121	10	- 1 module in a SRNM unit	Display and changing of setpoints and parameter
ST/MON Module	HNS0131	10	- 1 module in a SRNM unit	Error diagnosis. Power voltage monitor display
ANALYZER Module	HNS0141	10	- 1 module in a SRNM unit	Transmission function with inspection tool for Plateau and/or Discrimination characteristics measurement
TEST Module	HNS0151	10	- 1 module in a SRNM unit	Trip and alarm test function
LVPS Module	HNS0500	20	- 2 modules in a SRNM unit	+5V and ±15V power supply to each module
AO Module	HNS0515	20	- 2 modules in a SRNM unit	Analog outputs to the mimic display on the main control panel, Automatic Power Regulator (APR) and the Transient Monitor (+1 to +5V)
DIO Module	HNS0520	10	- 1 module in a SRNM unit	Discrete signal input and output module
TRN Module	HNS0531	10	- 1 module in a SRNM unit	Optical data transmission module
RM Module	HNS0550	10	- 1 module in a SRNM unit	SRNM Range number and Mode signal output
PA Module	HNS0560	10	- 1 PA module supplies the power to a SRNM Preamplifier	High Voltage and Low Voltage power supply are supplied to SRNM preamplifier.

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-8.2 System Configuration for BWR with 6 SRNM signals

A typical SRNM system configuration for a BWR with 6 SRNM signals is shown in Figure II-A-8-2. The applied modules for this configuration are listed in Table II-A-8-2. This configuration is applied to a BWR in which the existing Intermediate Range Monitor (IRM) system consists of six channels. In Figure II-A-8-2., only the SRNM units are FPGA-based safety-related equipment.

The SRNM unit for this BWR is modified from the SRNM unit for the ABWR as follows:

- TRN module for communicating to plant computer is removed, and AO module is used for providing analog signals to plant computer instead. Optionally, the TRN module can be retained and the plant computer enhanced to support receiving data over a fiber optic communication link using Toshiba's existing protocol.

The modification described above is minor changes from the hardware of SRNM unit for ABWR. No new hardware from the hardware for ABWR would be required. The change in weight is less than 10%, and thus would not require seismic qualification. Since existing modules are used with the possibility of changing the FPGA programmable logic, then would not be required.

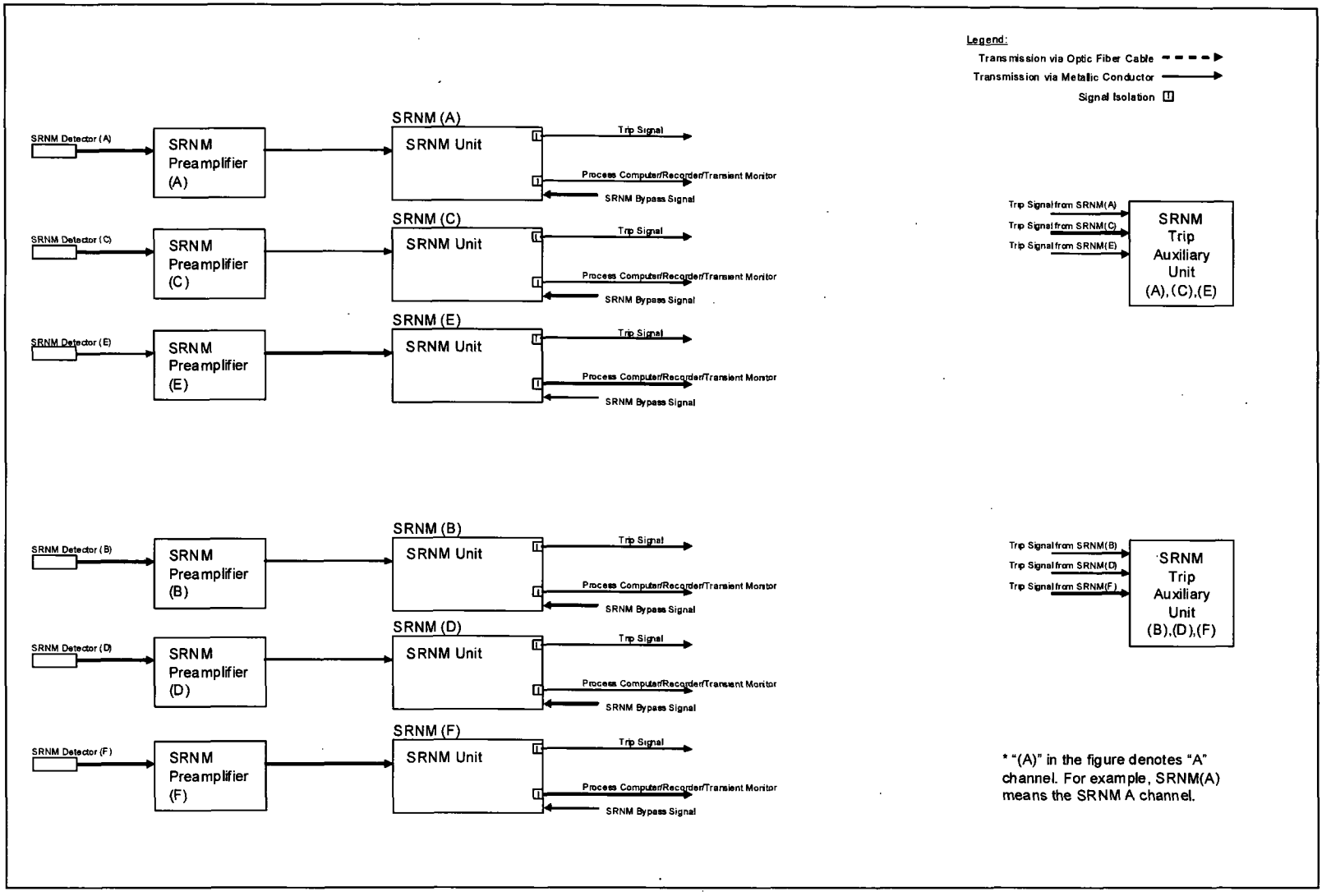


Figure II-A-8-2 Typical SRNM System Configuration for BWR with 6 SRNM Signals

Table II-A-8-2 Applied Module for SRNM system with 6 SRNM Signals

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-8-2		Functional Description
		Total Number	Description Note: The system has 6 channels with 1 SRNM unit in each channel.	
SRNM Module	HNS0101	6	- 1 module in a SRNM unit	SRNM signal processing function. Count rate, neutron flux, logarithmic % power, and linear % power are calculated from the neutron flux signal and are displayed them.
TRIP Module	HNS0117	6	- 1 module in a SRNM unit	Changing and display of trip setpoints and Trip judgment
PARAMETER Module	HNS0121	6	- 1 module in a SRNM unit	Display and changing of setpoints and parameter
ST/MON Module	HNS0131	6	- 1 module in a SRNM Uni.	Error diagnosis. Power voltage monitor display
ANALYZER Module	HNS0141	6	- 1 module in a SRNM unit	Transmission function with inspection tool for Plateau and/or Discrimination characteristics measurement
TEST Module	HNS0151	6	- 1 module in a SRNM unit	Trip and alarm test function
LVPS Module	HNS505	12	- 2 modules in a SRNM unit	+5V and ±15V power supply to each module Power Input 48VDC Type
AO Module	HNS0516	6	- 1 module in a SRNM unit	Analog outputs to the indicator and recorder on the main control panel
AO Module	HNS0518	6	- 1 module in a SRNM unit	Analog outputs to the process computer
DIO Module	HNS0520	6	- 1 module in a SRNM unit	Discrete signal input and output module
TRN Module	HNS0531	6	- 1 module in a SRNM unit	Optical data transmission module
RM Module	HNS0550	6	- 1 module in a SRNM unit	SRNM Range number and Mode signal output
PA Module	HNS0560	6	- 1 PA module supplies the power to a SRNM Preamplifier	High Voltage and Low Voltage power supply are supplied to SRNM preamplifier.

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-8.3 System Configuration for BWR with 8 SRNM signals

Typical SRNM system configuration for BWR with 8 SRNM signals is shown in Figure II-A-8-3. The applied modules for this configuration are listed in Table II-A-8-3. This configuration is applied to BWR in which the existing IRM system consists of eight channels. In Figure II-A-8-3, only SRNM units are FPGA-based safety-related equipment.

The SRNM unit for this BWR is modified from the SRNM unit for the ABWR as follows:

- TRN module for communicating to plant computer is removed, and AO module is used for providing analog signals to plant computer instead. Optionally, the TRN module can be retained and the plant computer enhanced to support receiving data over a fiber optic communication link using Toshiba's existing protocol.

The modification described above is minor changes from the hardware of SRNM unit for ABWR. No new hardware from the hardware for ABWR would be required. The change in weight is less than 10%, and thus would not require seismic qualification. Since existing modules are used with the possibility of changing the FPGA programmable logic, then would not be required.

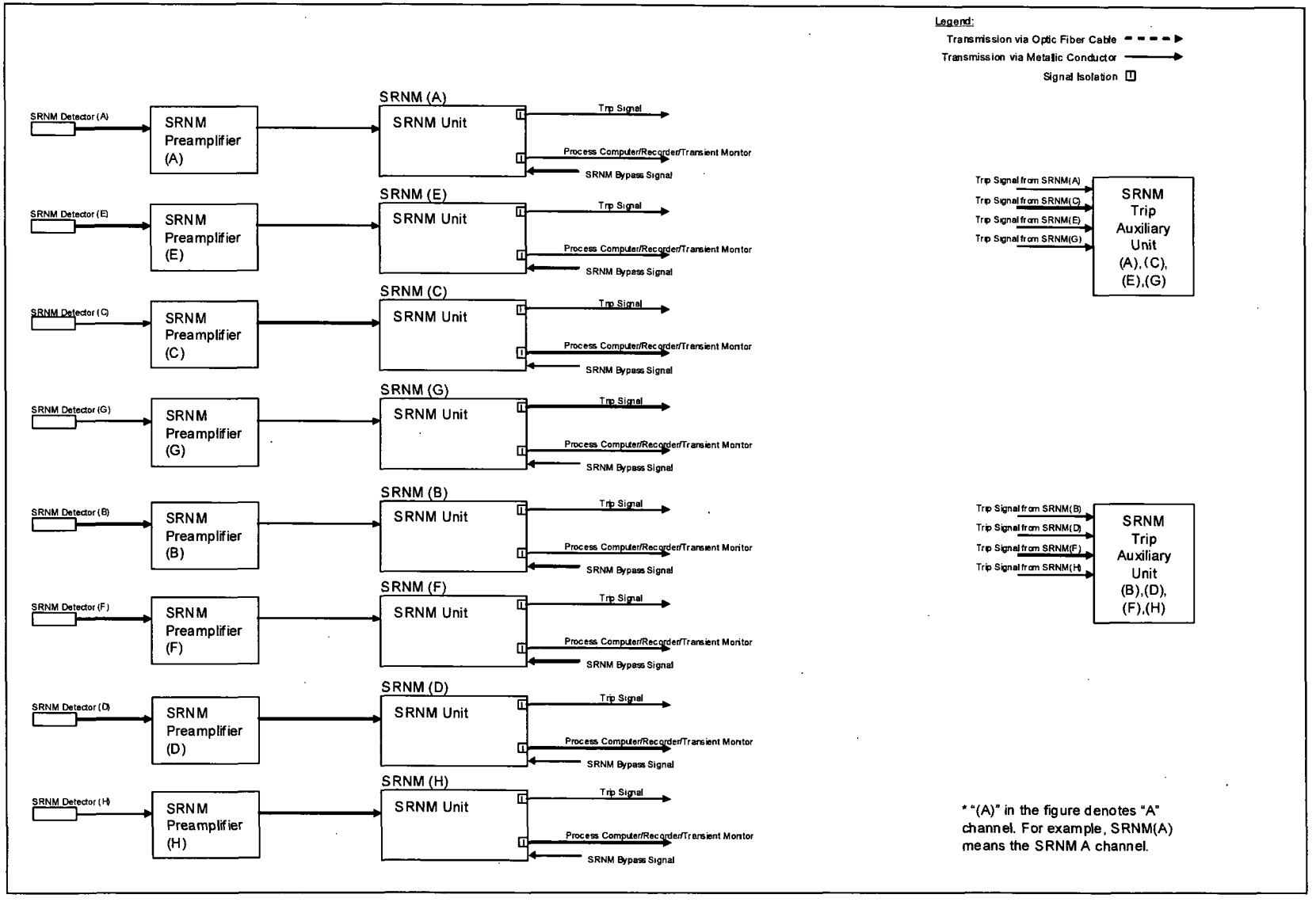


Figure II-A-8-3 Typical SRNM System Configuration for BWR with 8 SRNM Signals

Table II-A-8-3 Applied Module for SRNM system with 8 SRNM Signals

Module Name	Module Model Number*1	Number of Applied Module for System Configuration shown in Figure II-A-8-3		Functional Description
		Total Number	Description Note: The system has 8 channels with 1 SRNM unit in each channel.	
SRNM Module	HNS0101	8	- 1 module in a SRNM unit	SRNM signal processing function. Count rate, neutron flux, logarithmic % power, and linear % power are calculated from the neutron flux signal and are displayed them.
TRIP Module	HNS0117	8	- 1 module in a SRNM unit	Changing and display of trip setpoints and Trip judgment
PARAMETER Module	HNS0121	8	- 1 module in a SRNM unit	Display and changing of setpoints and parameter
ST/MON Module	HNS0131	8	- 1 module in a SRNM unit	Error diagnosis. Power voltage monitor display
ANALYZER Module	HNS0141	8	- 1 module in a SRNM unit	Transmission function with inspection tool for Plateau and/or Discrimination characteristics measurement
TEST Module	HNS0151	8	- 1 module in a SRNM unit	Trip and alarm test function
LVPS Module	HNS505	16	- 2 modules in a SRNM unit.	+5V and ±15V power supply to each module Power Input 48VDC Type
AO Module	HNS0516	8	- 1 module in a SRNM unit	Analog outputs to the indicator and recorder on the main control panel
AO Module	HNS0518	8	- 1 module in a SRNM unit	Analog outputs to the process computer
DIO Module	HNS0520	8	- 1 module in a SRNM unit	Discrete signal input and output module
TRN Module	HNS0531	8	- 1 module in a SRNM unit	Optical data transmission module
RM Module	HNS0550	8	- 1 module in a SRNM unit	SRNM Range number and Mode signal output
PA Module	HNS0560	8	- 1 PA module supplies the power to a SRNM Preamplifier	High Voltage and Low Voltage power supply are supplied to SRNM preamplifier.

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

II-A-9 RTIS System Configuration for ABWR

This section provides the Reactor Trip and Isolation System (RTIS) system configuration for an ABWR. The RTIS system for an ABWR consists of four divisions. Typical configuration of one division is shown in Figure II-A-9-1. The applied modules for all of four divisions are listed in Table II-A-9-1.

In Figure II-A-9-1, the following units are FPGA-based safety-related equipment.

- Digital Trip Function-Reactor Protection System (DTF-RPS) unit
- Trip Logic Function-Reactor Protection System (TLF-RPS) unit
- DTF-MSIV unit
- DTF-MSIV-Sub (DTF-MSIV-S) unit
- TLF-MSIV unit
- Suppression Pool Temperature Monitoring (SPTM) unit
- SPTM-Sub (SPTM-S) unit

The Reactor Protection System (RPS) function consists of one DTF-RPS unit, one TLF-RPS unit, one OLU-RPS unit, and eight LD-RPS units for one division.

The Main Steam Isolation Valve (MSIV) closure function consists of one DTF-MSIV unit, one DTF-MSIV-S unit, one TLF-MSIV unit, one OLU-MSIV unit, and ten LD-MSIV units for one division. The DTF-MSIV-S unit is a sub unit of the DTF-MSIV unit.

The SPTM function consists of one SPTM unit and two SPTM-S units for one division. The SPTM-S unit is a sub unit of the SPTM unit that performs suppression pool temperature monitoring function.

Since the RTIS system for ABWR includes new hardware in addition to the hardware identified in Section II-A-4 of this guide, additional qualification type tests will be required.

For applying the RTIS to BWR-2, -3, -4, -5, and -6, hardware and programmable logic would be removed and changed. The same hardware from the ABWR would be required. The change in weight would likely require seismic qualification. If only existing modules are used, then other type tests might be eliminated. This would need to be evaluated based on the magnitude of the changes required.

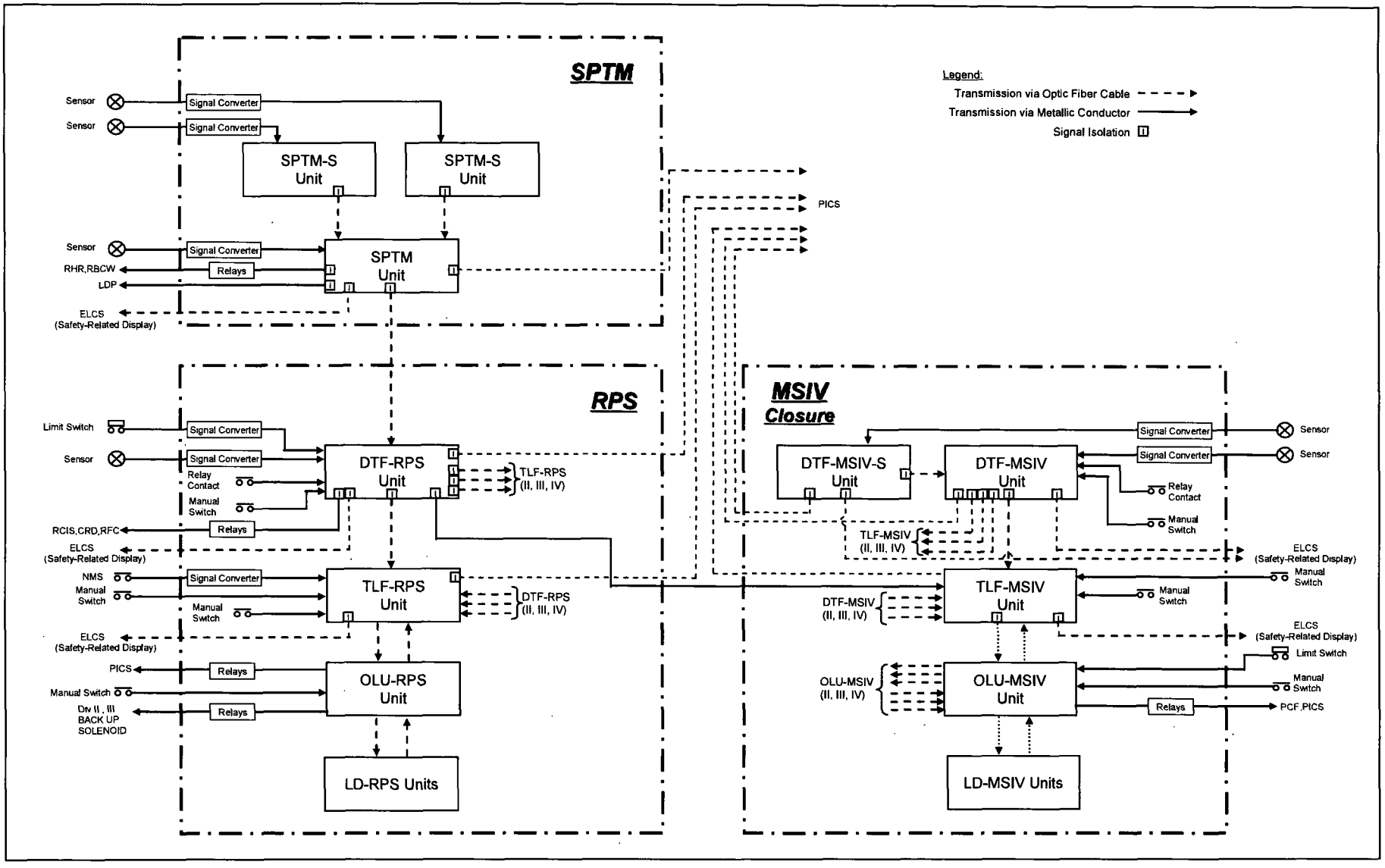


Figure II-A-9-1 RTIS System Configuration for ABWR (One Division)

Table II-A-9-1 Applied Module for ABWR RTIS system

Module Name	Module Model Number*1	Number of Applied Module for 4 divisions of RTIS		Functional Description
		Total Number	Description Note: The system consists of 4 RPS divisions and 4 MSIV divisions.	
AITRIP1 Module	HNS1100	192	- 8 modules in a SPTM unit - 8 modules in each unit of 2 SPTM-S units - 7 modules in a DTF-RPS unit (in each RPS Division) - 8 modules in a DTF-MSIV unit - 9 modules in a DTF-MSIV-S unit (in each MSIV Division)	Analog voltage signal processing and Trip Decision
SPTAVE1 Module	HNS1110	4	- 1 module in a SPTM unit (in each RPS Division)	Sensor signal average calculation and transfer data to AITRIP1 Module for Trip decision
SPTSEL1 Module	HNS1120	4	- 1 module in a SPTM unit (in each RPS Division)	Sensor signal Select and other data multiplexing
MLTPL1 Module	HNS1130	8	- 1 module in each unit of 2 SPTM-S units (in each RPS Division)	Serial Data Packet Conversion
DTUCA1 Module	HNS1141	4	- 1 module in a DTF-RPS unit (in each RPS Division)	Test Logic and Transfer Data multiplexing
DTUCA2 Module	HNS1142	4	- 1 module in a DTF-MSIV unit (in each MSIV Division)	Test Logic and Transfer Data multiplexing
TLUCA1 Module	HNS1151	4	- 1 module in a TLF-RPS unit (in each RPS Division)	4 division DTF signals input and 2 out of 4 Trip or 2 out of 3 Logic Decision
TLUCA2 Module	HNS1152	4	- 1 module in a TLF-MSIV unit (in each MSIV Division)	4 division DTF-MSIV signals input and 2 out of 4 Trip or 2 out of 3 Logic Decision
STR1 Module	HNS1161	4	- 1 module in a SPTM unit (in each RPS Division)	unit error diagnosis data display
STR1 Module	HNS1162	8	- 1 module in each unit of 2 SPTM-S units (in each RPS Division)	unit error diagnosis data display
STR1 Module	HNS1163	4	- 1 module in a DTF-RPS unit (in each RPS Division)	unit error diagnosis data display
STR1 Module	HNS1164	4	- 1 module in a DTF-MSIV unit (in each MSIV Division)	unit error diagnosis data display
STR1 Module	HNS1165	4	- 1 module in a TLF-RPS unit (in each RPS Division)	unit error diagnosis data display
STR1 Module	HNS1166	4	- 1 module in a TLF-MSIV unit (in each MSIV Division)	unit error diagnosis data display
STR1 Module	HNS1167	4	- 1 module in a DTF-MSIV-S unit (in each MSIV Division)	unit error diagnosis data display

Module Name	Module Model Number*1	Number of Applied Module for 4 divisions of RTIS		Functional Description
		Total Number	Description Note: The system consists of 4 RPS divisions and 4 MSIV divisions.	
MLTPL2 Module	HNS1170	4	- 1 module in a DTF-MSIV-S unit (in each MSIV Division)	Serial Data Packet Conversion
TLUBF1 Module	HNS1180	4	- 1 module in a TLF-RPS unit (in each RPS Division)	OLU data buffering and data multiplexing
LVPS Module	HNS0500	64	- 2 modules in a SPTM unit - 2 modules in each unit of 2 SPTM-S units - 2 modules in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 2 modules in a DTF-MSIV unit - 2 modules in a DTF-MSIV-S unit - 2 modules in a TLF-MSIV unit (in each MSIV Division)	+5V and ±15V power supply to each module
AO Module	HNS0515	4	- 1 module in a SPTM unit (in each RPS Division)	Analog outputs to the mimic display on the main control panel and the Transient Monitor (+1 to +5V)
TRN Module	HNS0531	64	- 2 modules in a SPTM unit - 1 module in each unit of 2 SPTM-S units - 3 modules in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 3 modules in a DTF-MSIV unit - 2 modules in a DTF-MSIV-S unit - 2 modules in a TLF-MSIV unit (in each MSIV Division)	Optical data transmission module
RCV Module	HNS0541	28	- 1 module in a SPTM unit - 1 module in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 1 module in a DTF-MSIV unit - 2 modules in a TLF-MSIV unit (in each MSIV Division)	Optical data reception module
DIC1 Module	HNS0730	32	- 3 modules in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 2 modules in a DTF-MSIV unit - 1 module in a TLF-MSIV unit (in each MSIV Division)	Discrete signal input
DOC1 Module	HNS0740	28	- 1 module in a SPTM unit - 1 module in a DTF-RPS unit - 2 modules in a TLF-RPS unit (in each RPS Division) - 1 module in a DTF-MSIV unit - 2 modules in a TLF-MSIV unit (in each MSIV Division)	Discrete signal output

Module Name	Module Model Number*1	Number of Applied Module for 4 divisions of RTIS		Functional Description
		Total Number	Description Note: The system consists of 4 RPS divisions and 4 MSIV divisions.	
LOM2_1 Module	HNS1201	4	- 1 module in a OLU-MSIV unit (in each MSIV Division)	Optical Transmission data received from TLF unit and sequential signal processing
LOM2_2 Module	HNS1202	4	- 1 module in a OLU-RPS unit (in each RPS Division)	Optical Transmission data received from TLF unit and sequential signal processing
LOI1 Module	HNS1211	28	- 2 modules in a OLU-RPS unit (in each RPS Division) - 5 modules in a OLU-MSIV unit (in each MSIV Division)	Optical Transfer to Load Drivers
LOI1 Module	HNS1212	4	- 1 module in a OLU-MSIV unit (in each MSIV Division)	Optical Transfer to other division OLU
LLN1 Module	HNS1220	8	- 1 module in a OLU-RPS unit (in each RPS Division) - 1 module in a OLU-MSIV unit (in each MSIV Division)	Discrete signal input (DC24V)
LHI1 Module	HNS1230	4	- 1 module in a OLU-RPS unit (in each RPS Division)	Discrete signal input (DC110V)
LHO1 Module	HNS1240	8	- 1 module in a OLU-RPS unit (in each RPS Division) - 1 module in a OLU-MSIV unit (in each MSIV Division)	Discrete signal output (AC/DC110V)
LDC1 Module	HNS1250	112	- 1 module in each RPS LD unit (32 RPS LD units in the system) - 2 modules in each MSIV LD unit (40 MSIV LD units in the system)	LD control module
LDD1 Module	HNS1261	80	- 2 modules in each MSIV LD unit (in each MSIV Division)	LD driver module for MSIV
LDD1 Module	HNS1262	32	- 1 module in each RPS LD unit (32 RPS LD units in the system)	LD driver module for RPS
LDB1 Module	HNS1270	32	- 1 module in each RPS LD unit (32 RPS LD units in the system)	LD booster module for RPS
SLD1 Module	-	120	- 1 module in OLU-RPS unit - (in each RPS Division) - 1 module in OLU-MSIV unit - (in each MSIV Division) - 1 module in each RPS LD unit - (32 RPS LD units in the system) - 2 modules in each MSIV LD unit - (40 MSIV LD units in the system)	Shield(blank) Panel

*1: Each Module has Type number for configuration control. When a module design is changed, a type number of each module shall be changed to a new revised type number which shall be different from the previous module type number.

Appendix II-B. Module Summary Description

II-B-1 Introduction

This appendix includes the Module Summary Descriptions (MSD)s for the modules listed in Table II-B-1. The MSDs are complied in Attachment of this Appendix.

Table II-B-1 includes the page number of each MSD in Attachment for reference.

Table II-B-1 Module Summary Description List

Document Number	Module Name	Type Number	Has FPGA Module?	System used	Unit used	Page on Attachment (bottom right)
MEM-JHS-000108	LPRM	HNS013	yes	PRM(BWR-2,3,4,5,6)	LPRM, LPRM/APRM, FLOW, SRNM	1
MEM-JHS-000109	LPRM	HNS0302	yes	PRM for ABWR	LPRM(ABWR)	5
MEM-JHS-000110	APRM	HNS020	yes	PRM(BWR-2,3,4,5,6)	LPRM/APRM	9
MEM-JHS-000111	APRM	HNS0311	yes	PRM for ABWR	APRM(ABWR)	14
MEM-JHS-000112	SQ-ROOT	HNS030	yes	PRM(BWR-2,3,4,5,6)	FLOW	19
MEM-JHS-000113	FLOW	HNS040	yes	PRM(BWR-2,3,4,5,6)	FLOW	23
MEM-JHS-000114	FLOW	HNS0321	yes	PRM for ABWR	APRM(ABWR)	28
MEM-JHS-000115	STATUS	HNS091	yes	PRM(BWR-2,3,4,5,6)	LPRM/APRM	32
MEM-JHS-000116	STATUS	HNS093	yes	PRM(BWR-2,3,4,5,6)	LPRM, FLOW	35
MEM-JHS-000117	MUX	HNS260	yes	PRM(BWR-2,3,4,5)	LPRM	38
MEM-JHS-000118	CAL/ST	HNS0330	yes	PRM for ABWR	LPRM(ABWR)	41
MEM-JHS-000119	GAF/ST	HNS0341	yes	PRM for ABWR	APRM(ABWR)	45
MEM-JHS-000104	TRN	HNS530	yes	PRM(BWR-2,3,4,5,6)	LPRM, LPRM/APRM, FLOW	49
MEM-JHS-000105	TRN	HNS0531	yes	OPRM, PRM(BWR-2,3,4,5,6), PRM for ABWR, SRNM, RTIS, SPTM	OPRM, LPRM, LPRM/APRM, FLOW, LPRM(ABWR), APRM(ABWR), SRNM, DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S	54
MEM-JHS-000106	RCV	HNS540	yes	PRM(BWR-2,3,4,5,6)	LPRM, LPRM/APRM	59

Document Number	Module Name	Type Number	Has FPGA Module?	System used	Unit used	Page on Attachment (bottom right)
MEM-JHS-000107	RCV	HNS0541	yes	OPRM, PRM(BWR-2,3,4,5,6), PRM for ABWR, RTIS, SPTM	OPRM, LPRM, LPRM/APRM, LPRM(ABWR), APRM(ABWR), DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, SPTM	63
MEM-JHS-000100	LVPS	HNS500	no	PRM, PRM for ABWR, OPRM, SRNM, RTIS, SPTM	LPRM, LPRM/APRM, FLOW, LPRM(ABWR), APRM(ABWR), OPRM, SRNM, DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S	67
MEM-JHS-000102	AO	HNS515, 516, 517, 518	no	PRM(BWR-2,3,4,5,6), PRM for ABWR	LPRM, LPRM/APRM, LPRM(ABWR), APRM(ABWR), FLOW, SRNM, SPTM	70
MEM-JHS-000103	DIO	HNS520	no	PRM(BWR-2,3,4,5,6), PRM for ABWR, OPRM, SRNM	LPRM, LPRM/APRM, FLOW, LPRM(ABWR), APRM(ABWR), OPRM, SRNM	72
MEM-JHS-000120	BLANK	HNS490	no	PRM(BWR-2,3,4,5,6)	LPRM	74
MEM-JHS-000121	CELL	HNS0400	yes	OPRM	OPRM	76
MEM-JHS-000122	DAT/ST	HNS0410	yes	OPRM	OPRM	81
MEM-JHS-000123	AGRD	HNS0420	yes	OPRM	OPRM	85
MEM-JHS-000124	PBD	HNS0430	yes	OPRM	OPRM	90
MEM-JHS-000125	SRNM	HNS0101	yes	SRNM	SRNM	95
MEM-JHS-000126	TRIP	HNS0117	yes	SRNM	SRNM	100
MEM-JHS-000127	PARAMETER	HNS0121	yes	SRNM	SRNM	105
MEM-JHS-000128	ST/MON	HNS0131	yes	SRNM	SRNM	110
MEM-JHS-000129	ANALYZER	HNS0141	yes	SRNM	SRNM	115
MEM-JHS-000130	TEST	HNS0151	yes	SRNM	SRNM	120
MEM-JHS-000101	LVPS	HNS505	no	SRNM	SRNM	124
MEM-JHS-000131	RM	HNS0550	no	SRNM	SRNM	127
MEM-JHS-000132	PA	HNS0560	no	SRNM	SRNM	129

Document Number	Module Name	Type Number	Has FPGA Module?	System used	Unit used	Page on Attachment (bottom right)
MEM-JHS-000135	AITRIP1	HNS1100	yes	RTIS, SPTM	DTF-RPS, DTF-MSIV, DTF-MSIV-S, SPTM, SPTM-S	132
MEM-JHS-000136	SPTAVE 1	HNS1110	yes	SPTM	SPTM	137
MEM-JHS-000137	SPTSEL1	HNS1120	yes	SPTM	SPTM	141
MEM-JHS-000138	MLTPL1	HNS1130	yes	SPTM	SPTM-S	146
MEM-JHS-000139	DTUCA1	HNS1141	yes	RTIS	DTF-RPS	150
MEM-JHS-000140	DTUCA2	HNS1142	yes	RTIS	DTF-MSIV	155
MEM-JHS-000141	TLUCA1	HNS1151	yes	RTIS	TLF-RPS	160
MEM-JHS-000142	TLUCA2	HNS1152	yes	RTIS	TLF-MSIV	165
MEM-JHS-000143	STR1	HNS1161, 1162, 1163, 1164, 1165, 1166, 1167	no	SPTM, RTIS	SPTM, SPTM-S, DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, DTF-MSIV-S	170
MEM-JHS-000144	MLTPL2	HNS1170	yes	RTIS	DTF-MSIV-S	173
MEM-JHS-000145	TLUBF1	HNS1180	yes	RTIS	TLF-RPS	177
MEM-JHS-000146	LOM2_1	HNS1201	yes	RTIS	OLU-MSIV	182
MEM-JHS-000147	LOM2_2	HNS1202	yes	RTIS	OLU-RPS	187
MEM-JHS-000152	LOM2_1	HNS1203	yes	RTIS	OLU-MSIV	192
MEM-JHS-000153	LOM2_2	HNS1204	yes	RTIS	OLU-RPS	197
MEM-JHS-000133	DIC1	HNS0730	no	RTIS	DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV	202
MEM-JHS-000134	DOC1	HNS0740	no	RTIS	DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, SPTM	204
MEM-JHS-000148	LOI1	HNS1211, 1212	no	RTIS	OLU-RPS, OLU-MSIV	206
MEM-JHS-000149	LLN1	HNS1220	no	RTIS	OLU-RPS, OLU-MSIV	209
MEM-JHS-000150	LHI1	HNS1230	no	RTIS	OLU-RPS	211
MEM-JHS-000151	LHO1	HNS1240	no	RTIS	OLU-RPS, OLU-MSIV	213

APPENDIX II-B Attachment

LPRM Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LPRM module

(2) Module Number: HNS013

(3) Unit and application to be used
LPRM/APRM, LPRM Units for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: Four

2 Functional Summary

The LPRM module controls the bias voltage applied to the in-core neutron detector, receives the current representing the LPRM power from the LPRM detector in the reactor core, converts the LPRM signal to a digital percent power value called the LPRM level, and provides that power to the APRM and OPRM for further processing.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the LPRM module.

3.2 Inputs and Outputs

The LPRM module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules

[ ] a,c

3.2.2 Outputs

(1) Output signals via process input and output modules a,c

[ ]

(2) Output signals via communication modules

[ ] a,c

a,c

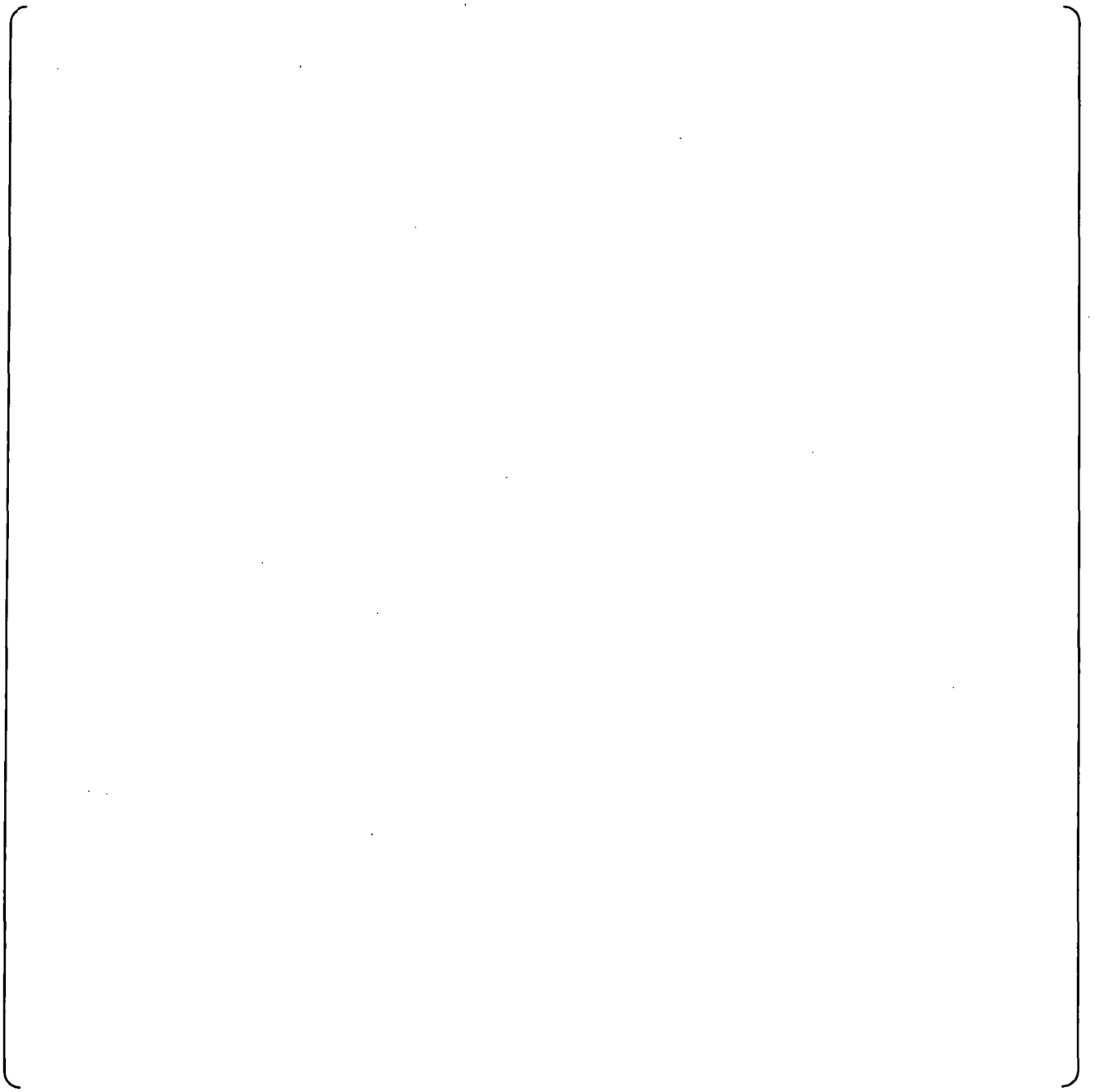


Figure 1 The front panel of the LPRM module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the LPRM module. Table 1 provides functions of each FPGA.

[ ] a,c

Figure 2 Functional Block Diagram of LPRM module

Table 1 FPGA functions in the LPRM module

FPGA	Description
[ ]	[ ]

a,c

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

[ ] a,c

3.4.2 Inoperable Trip

[ ] a,c

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変更記号 REV.MARK 変更発行日 REV.ISSUED	ページ PAGE	変更箇所・変更内容 CHANGED PLACE AND CONTENTS	承認 APPROVED BY	調査 REVIEWED BY	担当 PREPARED BY	保管 REGISTERED
⓪ Feb.8, 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15, 2013	1 2 3	Descriptions in Section 2 and 3 were improved Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Description of self diagnosis was improved.	K.Wakita Feb.15, 2013	T. Tarumi Feb. 15, 2013	H. Ito Feb. 15, 2013	H. Ito Feb. 15, 2013

LPRM Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LPRM module

(2) Module Number: HNS0302

(3) Unit and application to be used
LPRM Unit for ABWR Application

(4) Number of FPGA on the module: Four

2 Functional Summary

The LPRM module controls the bias voltage applied to the in-core neutron detector, receives the current representing the LPRM power from the LPRM detector in the reactor core, converts the LPRM signal to a digital percent power value called the LPRM level, and provides that power to the APRM and OPRM for further processing.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the LPRM module.

3.2 Inputs and Outputs

The LPRM module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

3.2.2 Outputs

(1) Output signals via process input and output modules a,c

[ ]

(2) Output signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

[ ] a,c

Figure 1 The front panel of the LPRM module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the LPRM module. Table 1 provides functions of each FPGA. a,c

Figure 2 Functional Block Diagram of LPRM module

Table 1 FPGA functions in the LPRM module

FPGA	Description

a,c

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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⓪ Feb.8. 2013	–	First issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb.15.2013	1 2 3	Summary description was improved. Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Description of self diagnosis was improved.	K.Wakita Feb.15.2013	T.Tarumi Feb.15.2013	H.Ito Feb.15.2013	H.Ito Feb.15.2013

APRM Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: APRM module

(2) Module Number: HNS020

(3) Unit and application to be used
LPRM/APRM Unit for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: Eleven

2 Functional Summary

The APRM module collects the LPRM levels from the individual LPRM modules, calculates an APRM level and a Simulated Thermal Power level. If the APRM level or the Simulated Thermal Power level exceeds one or more setpoints, the APRM module generates a trip signal for the reactor trip system to process. The APRM module uses the Flow values collected from the FLOW module to calculate setpoints for the APRM level and the Simulated Thermal Power level.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the APRM module.

3.2 Inputs and Outputs

The APRM module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[ ] a,c

(2) Input signals via communication modules

[ ] a,c

a,c

a, c

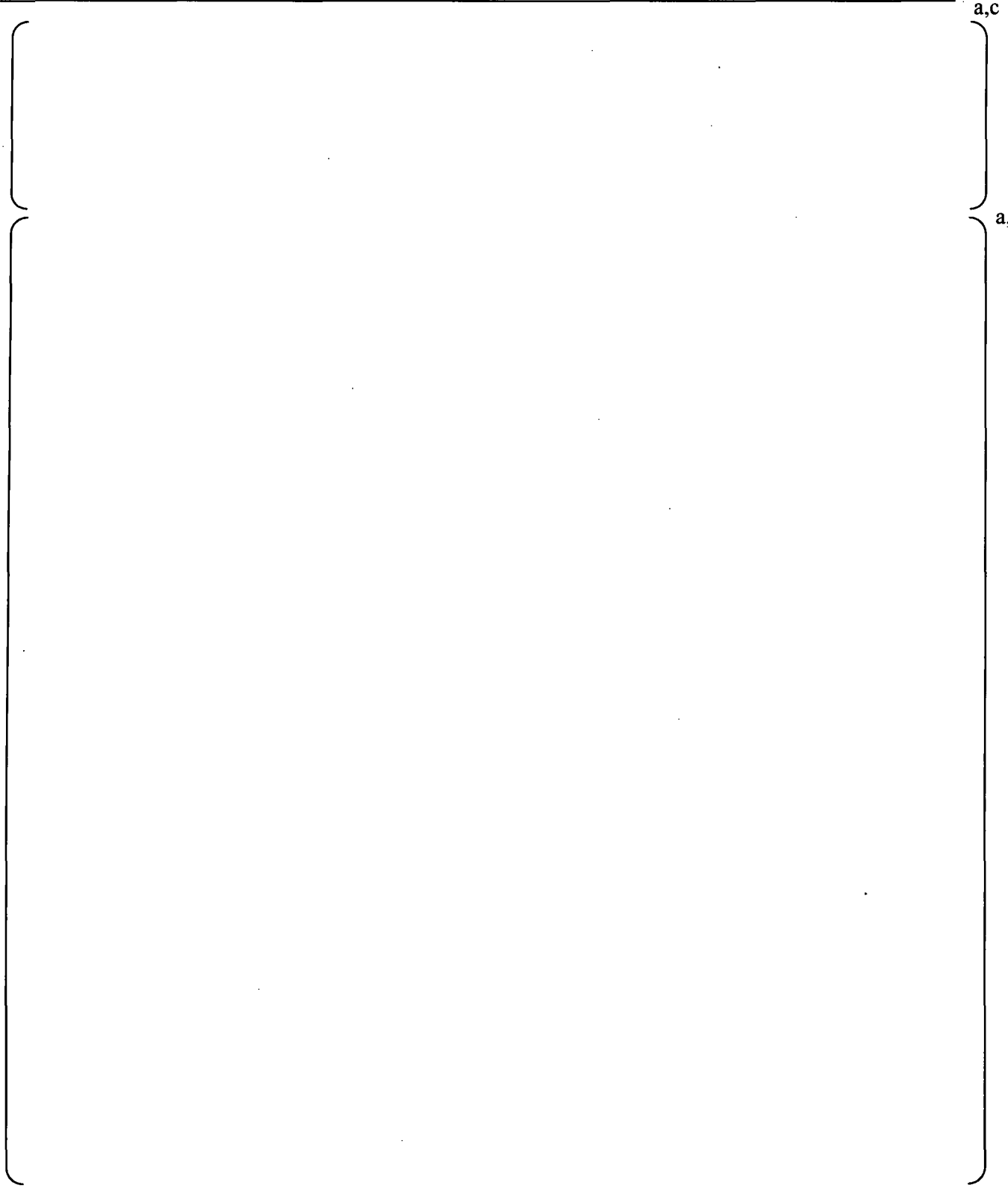

Figure 1 The front panel of the APRM module

3.2.2 Outputs

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication modules

a,c

(3) Others to be noted

a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the APRM module where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of APRM module

Table 1 FPGA functions in the APRM module

FPGA	Description

a,c

3.4 Self Diagnosis

The APRM module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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⓪ Feb.5. 2013	–	First issue	K.Wakita Feb.5,2013	T.Tarumi Feb.5,2013	H.Ito Feb.5,2013	H.Ito Feb.5,2013
① Feb.15.2013	1,2 3 3 3 3,4 4	Figure number 3-1 was changed to 1 Inputs and outputs descriptions were revised that "(3) Others to be noted" was added and contents were clarified. Figure number 3-2 was changed to 2. Figure 2 was detailed to clarify. Table number 3-1 was changed to 1. Description on self diagnosis was detailed to clarify.	K.Wakita Feb.15,2013	T.Tarumi Feb.15.2013	H.Ito Feb.15.2013	H.Ito Feb.15.2013

APRM Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: APRM module

(2) Module Number: HNS0311

(3) Unit and application to be used
APRM Unit for ABWR application

(4) Number of FPGA on the module: Ten

2 Functional Summary

The APRM module collects the LPRM levels from the individual LPRM modules, calculates an APRM level and a Simulated Thermal Power level. If the APRM level or the Simulated Thermal Power level exceeds one or more setpoints, the APRM module generates a trip signal for the reactor trip system to process. The APRM module uses the Flow values collected from the FLOW module to calculate setpoints for the APRM level and the Simulated Thermal Power level.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the APRM module.

3.2 Inputs and Outputs

The APRM module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

a,c

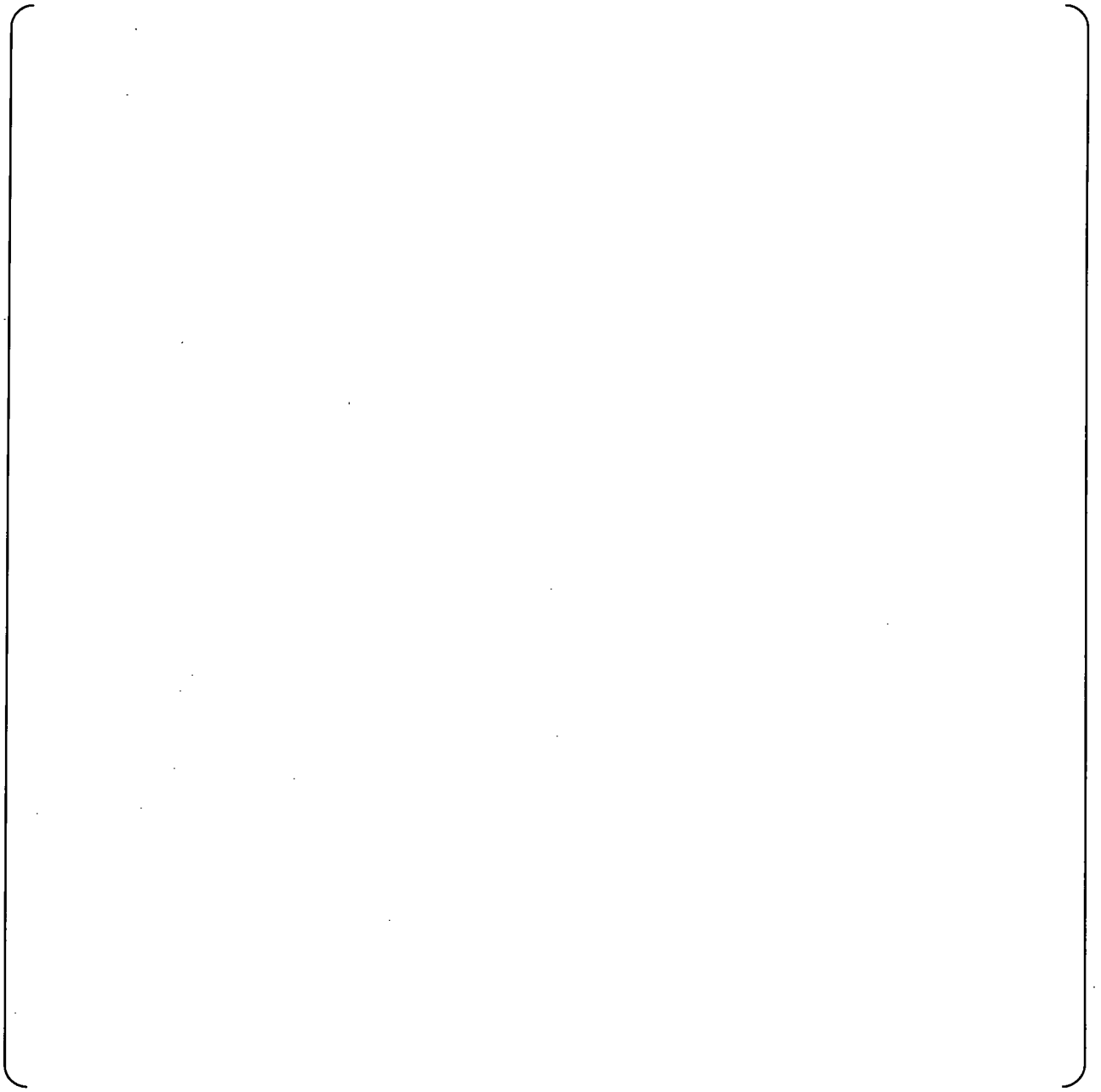

Figure 1 The front panel of the APRM module

3.2.2 Outputs

(1) Output signals via process input and output modules a,c

a,c

(2) Output signals via communication modules

a,c

(3) Others to be noted

a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the APRM module used for ABWR where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of APRM module

Table 1 FPGA functions in the APRM module

a,c

FPGA	Description

[a,c]

3.4 Self Diagnosis

The APRM module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

[a,c]

3.4.2 Inoperable Trip

[a,c]

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⓪ Feb.8, 2013	-	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15, 2013	1 3 4	Figure number was changed from 3-1 to 1. Figure number was changed from 3-2 to 2. Table number was changed from 3-1 to 1. Descriptions on self diagnosis were improved.	K.Wakita Feb.15,2013	T.Tarumi Feb.15,2013	H.Ito Feb.15,2013	H.Ito Feb.15,2013

SQ-ROOT Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: SQ-ROOT module

(2) Module Number: HNS030

(3) Unit and application to be used
FLOW Unit for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: Five

2 Functional Summary

The SQ-ROOT module receives a 4-20 mA current loop input from the differential pressure transmitter attached to one of the two recirculation loop, converts the current loop input to a digital value, and calculates a square root of the digital value to obtain a flow value.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the SQ-ROOT module.

3.2 Inputs and Outputs

The SQ-ROOT module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

(2) Input signals via communication modules a,c

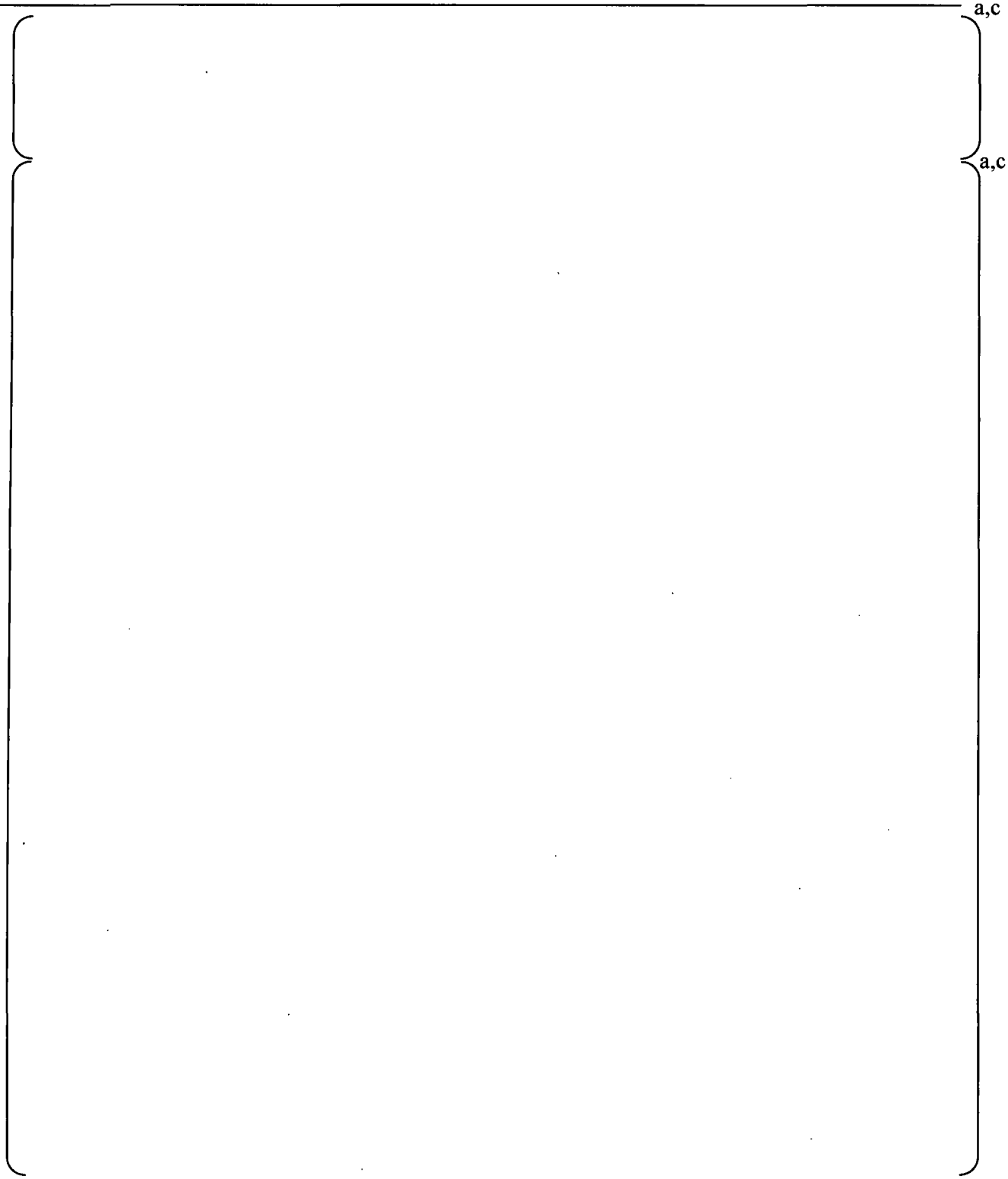
3.2.2 Outputs

(1) Output signals via process input and output modules a,c

(2) Output signals via communication modules a,c

(3) Others to be noted

a,c



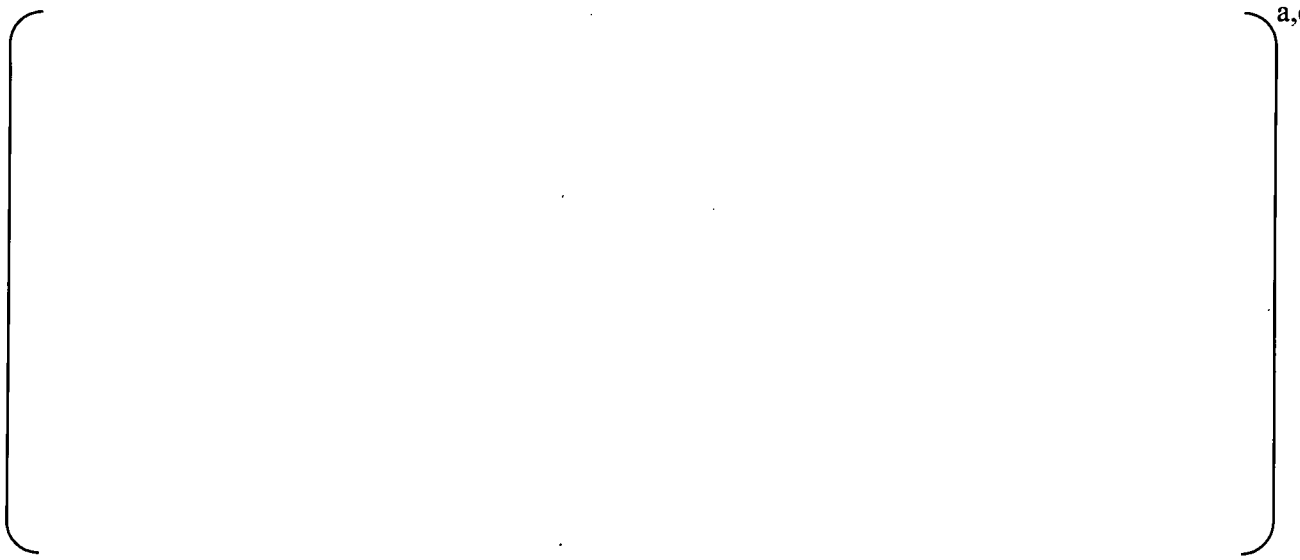
a,c

Figure 1 The front panel of the SQ-ROOT module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the SQ-ROOT module. Table 1 provides functions

of each FPGA.



a,c

Figure 2 Functional Block Diagram of SQ-ROOT module

Table 1 FPGA functions in the SQ-ROOT module

FPGA	Description

a,c

3.4 Self Diagnosis

The SQ-ROOT module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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⓪ Feb.8, 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb.15,2013	1 2 3	Description on inputs was improved. Figure number 3-1 was changed to 1 Figure number 3-2 was changed to 2, and the figure was corrected Table number 3-1 was changed to 1 Descriptions on self diagnosis were improved.	K.Wakita Feb.15, 2013	T.Tarumi Feb.15,2013	H.Ito Feb.15,2013	H.Ito Feb.15,2013

FLOW Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: FLOW module

(2) Module Number: HNS040

(3) Unit and application to be used

FLOW Unit for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: Four

2 Functional Summary

The FLOW module receives two raw Flow values from the SQ-ROOT module mounted in the same FLOW unit, and calculates a normalized Flow value by taking a sum of the two raw Flow values, and applying a gain value.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the FLOW module.

3.2 Inputs and Outputs

The FLOW module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication modules

[ ]a,c

(3) Others to be noted

[ ]a,c

3.2.2 Outputs

(1) Output signals via process input and output modules

[ ] a,c

(2) Output signals via communication modules

[ ] a,c

[ ] a,c

Figure 1 The front panel of the FLOW module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the FLOW module where each block shows an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of FLOW module

Table 1 FPGA functions in the FLOW module

a,c

FPGA	Description

3.4 Self Diagnosis

The FLOW module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

[ ]a,c

3.4.2 Inoperable Trip

[ ]a,c

through which the frame pulse is relayed from the first FPGA to the last FPGA.

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⓪ Feb.8, 2013	—	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15. 2013	1 3 4	Descriptions in Section 2 and 3 were improved adding information on communication Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Description of self diagnosis was improved.	K.Wakita Feb 15. 2013	T.Tarumi Feb. 15. 2013	H. Ito Feb. 15. 2013	H. Ito Feb. 15. 2013

FLOW Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: FLOW module

(2) Module Number: HNS0321

(3) Unit and application to be used: APRM Unit for ABWR Application

(4) Number of FPGA on the module: Eight

2 Functional Summary

The FLOW module receives a 4-20 mA current input from the differential pressure transmitter attached to the core support plate, and generates a differential pressure value. The FLOW module calculates one core flow value from the differential pressure value and a simulated thermal power level from the APRM module using a proprietary equation. If the FLOW module detects rapid coastdown of core flow, the FLOW module generates a trip signal to the reactor trip system.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the FLOW module.

3.2 Inputs and Outputs

The FLOW module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication modules

[ ]a,c

(3) Others to be noted

[ ]a,c

3.2.2 Outputs

(1) Output signals via process input and output modules

[ ]a,c

(2) Output signals via communication modules

[ ]a,c

(3) Others to be noted

[ ]a,c

[ ]a,c

Figure 1 The front panel of the FLOW module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the FLOW module used for ABWR where each block is an FPGA. Table 1 provides the functions of each FPGA.

[a,c

] a,c

Figure 2 Functional Block Diagram of FLOW module

Table 1 FPGA functions in the FLOW module

[a,c

FPGA	Description

] a,c

3.4 Self Diagnosis

The FLOW module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

[a,c

] a,c

3.4.2 Inoperable Trip

[a,c

] a,c

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⓪ Feb.8, 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15, 2013	1 2 3	Descriptions in Section 2 and 3 were improved adding information on current condition and communication Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Description of self diagnosis was improved.	K. Wakita Feb 15, 2013	T. Tarumi Feb. 15, 2013	H. Ito Feb. 15, 2013	H. Ito Feb. 15, 2013

STATUS Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: STATUS module

(2) Module Number: HNS091

(3) Unit and application to be used

LPRM/APRM Unit for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: One

2 Functional Summary

The STATUS module receives discrete alarm signals from the LVPS and APRM modules in the same unit, and shows the alarm on the module front panel.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the STATUS module.

3.2 Inputs and Outputs

The STATUS module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication modules

[ ]a,c

(3) Others to be noted

[ ]a,c

3.2.2 Outputs

(1) Output signals via process input and output modules

[ ]a,c

Figure 1 The front panel of the STATUS module

a,c

[

]

(2) Output signals via communication modules a,c

[

]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the STATUS module. Table 1 provides functions of each FPGA. a,c

[

]

Figure 2 Functional Block Diagram of STATUS module

Table 1 FPGA functions in the STATUS module

FPGA	Description

a,c

[

]

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

a,c

[

]

3.4.2 Inoperable Trip

a,c

[

]

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0 Feb.8. 2013	--	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
1 Feb. 15. 2013	1 2 3	Descriptions in Section 2 and 3 were improved. Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Descriptions of self diagnosis were corrected.	K Wakita Feb.15. 2013	T. Tarumi Feb. 15, 2013	H. Ito Feb. 15. 2013	H. Ito Feb 15. 2013

STATUS Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: STATUS module

(2) Module Number: HNS093

(3) Unit and application to be used
LPRM and FLOW Units for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: One

2 Functional Summary

The STATUS module receives discrete alarm signals from the LVPS modules in the same unit, and shows the alarm on the module front panel.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the STATUS module.

3.2 Inputs and Outputs

The STATUS module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication modules

[ ]a,c

(3) Others to be noted

[ ]a,c

3.2.2 Outputs

(1) Output signals via process input and output modules

[ ]a,c

Figure 1 The front panel of the STATUS module

a,c

[ ]

(2) Output signals via communication modules

a,c

[ ]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the STATUS module. Table 1 provides functions of each FPGA.

a,c

[ ]

Figure 2 Functional Block Diagram of STATUS module

Table 1 FPGA functions in the STATUS module

a,c

FPGA	Description
[ ]	

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

a,c

[ ]

3.4.2 Inoperable Trip

a,c

[ ]

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変更記録 REVISIONS						
⓪ Feb.8. 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15.2013	1 2 3	Descriptions in Section 2 and 3 were improved. Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Descriptions of self diagnosis were corrected.	K. Wakita Feb 15, 2013	T. Tarumi Feb.15,2013	H. Ito Feb.15.2013	H. Ito Feb. 15. 2013

MUX Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: MUX module

(2) Module Number: HNS260

(3) Unit and application to be used

LPRM Unit for BWR-2, 3, 4 and 5 application

(4) Number of FPGA on the module: Four

2 Functional Summary

The MUX module collects the LPRM levels from the individual LPRM modules in the same LPRM unit, multiplexes the LPRM levels in a data frame, and sends the data frame to external equipment.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the MUX module.

3.2 Inputs and Outputs

The MUX module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication modules

[ ]a,c

3.2.2 Outputs

(1) Output signals via process input and output modules

[ ]a,c

(2) Output signals via communication modules

[ ]a,c

[ ]a,c

Figure 1 The front panel of the MUX module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the MUX module where each block is an FPGA.

Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of MUX module

Table 1 FPGA functions in the MUX module

a,c

FPGA	Description

3.4 Self Diagnosis

The MUX module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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⓪ Feb.8, 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb.15,2013	1 2 3	Figure number was changed from 3-1 to 1 Figure number was changed from 3-2 to 2 Table number was changed from 3-1 to 1 Descriptions of self diagnosis were corrected.	K.Wakita Feb.15, 2013	T.Tarumi Feb.15,2013	H. Ito Feb.15.2013	H. Ito Feb.15.2013

CAL/ST Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: CAL/ST module

(2) Module Number: HNS0330

(3) Unit and application to be used: LPRM Unit for ABWR Application

(4) Number of FPGA on the module: Two

2 Functional Summary

The CAL/ST module has three functions:

(1) Collects the LPRM levels and status from the individual LPRM modules in the same LPRM unit, multiplexes the LPRM levels and status in a data frame, and sends the data frame to external equipment.

(2) Calculates and provides an Ical calibration value for each LPRM module mounted in the same LPRM unit. Each Ical calibration value is calculated comparing the current LPRM level from the LPRM module and, the Gain Adjustment Factor (GAF) downloaded from the process computer via the GAF/ST module in the APRM unit.

(3) Provides the status of the communication line status from the LPRM modules, and the LVPS modules on the front panel.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the CAL/ST module.

3.2 Inputs and Outputs

The CAL/ST module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

a.c

a.c

Figure 1 The front panel of the CAL/ST module

(2) Input signals via communication modules

[redacted] a.c

(3) Others to be noted

[redacted] a.c

3.2.2 Outputs

(1) Output signals via process input and output modules

[redacted] a.c

(2) Output signals via communication modules

[redacted] a,c

(3) Others to be noted

[redacted] a.c

3.3 FPGA functions

Figure 2 shows the Functional Block Diagram of the CAL/ST module used for ABWR. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of CAL/ST module

Table 1 FPGA functions in the CAL/ST module

FPGA	Description

a.c

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

a.c

3.4.2 Inoperable Trip

a,c

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0 Feb.8, 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tsurumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
1 Feb.15,2013	1 2 3	Summary description was corrected Figure number 3-1 was changed to 1. "Others to be noted" as added to the outputs Figure number 3-2 was changed to 2 Figure 2 was corrected. Table number 3-1 was changed to 1 Description on self diagnosis was improved.	K.Wakita Feb 15, 2013	T.Tsurumi Feb. 15, 2013	H.Ito Feb.8,2013	H.Ito Feb. 15, 2013

GAF/ST Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: GAF/ST module

(2) Module Number: HNS0341

(3) Unit and application to be used: APRM Unit for ABWR Application

(4) Number of FPGA on the module: Two

2 Functional Summary

The GAF/ST module has three functions:

(1) Collects the LPRM data and APRM data from the APRM module and the FLOW data from the FLOW module in the same APRM unit, multiplexes the data in a data frame, and sends the data frame to external equipment.

(2) Downloads Gain Adjustment Factors (GAFs) from the process computer for the LPRM modules in this division, and provides the GAFs to the LPRM modules via the CAL/ST modules. The GAF download is performed manually, setting the operation mode to ENB (enable) and pushing the GAF Req. (Request) button.

(3) Indicates the alarms of communication line status between the LPRM units and the APRM module, and the alarms of the LVPS modules.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the GAF/ST module.

3.2 Inputs and Outputs

The GAF/ST module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[a,c]

Figure 1 The front panel of the GAF/ST module

(2) Input signals via communication modules

[redacted] a,c

(3) Others to be noted

[redacted] a,c

3.2.2 Outputs

(1) Output signals via process input and output modules

[redacted] a,c

(2) Output signals via communication modules

[redacted] a,c

3.3 FPGA functions

Figure 2 shows the Functional Block Diagram of the GAF/ST module used for ABWR. Table 1 provides functions of each FPGA.

[redacted] a,c

Figure 2 Functional Block Diagram of GAF/ST module

Table 1 FPGA functions in the GAF/ST module

FPGA	Description
[	] a,c

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

[ ] a,c

3.4.2 Inoperable Trip

[ ] a,c

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⓪ Feb.8, 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15, 2013	1 2 	Summary description was corrected Figure number 3-1 was changed to 1. Inputs and outputs descriptions were improved Figure number 3-2 was changed to 2 Table number 3-1 was changed to 1 Description on self diagnosis was improved.	K. Wakita Feb.15, 2013	T. Tarumi Feb. 15. 2013	H. Ito Feb. 15. 2013	H. Ito Feb. 15. 2013

TRN Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: TRN module

(2) Module Number: HNS530

(3) Unit and application to be used

LPRM/APRM, LPRM, FLOW, SRNM Units for BWR-2,3,4,5 and 6 Application

LPRM, APRM, SRNM, DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S Units for ABWR Application

(4) Number of FPGA on the module: Six

2 Functional Summary

The TRN module has two data processing trains that collect data from other modules mounted in the same unit, generate a data frame in a fixed format by multiplexing the collected data, and transmit the data frame to external over fiber optic links and to other modules in the same unit. When installed in the LPRM/APRM unit, the TRN module receives the data frame from the APRM module in the same unit, and transmits the data frame over fiber optic links instead of the data frame generated in the TRN module.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the TRN module.

3.2 Inputs and Outputs

The TRN module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

[ ] a,c

3.2.2 Outputs

(1) Output signals via process input and output modules

[ ] a,c

(2) Outputs via communication modules

[ ] a,c

(3) Others to be noted

[ ] a,c

a,c

Figure 1 The front panel of the TRN module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the TRN module. Table 1 provides functions of each FPGA.

a,c

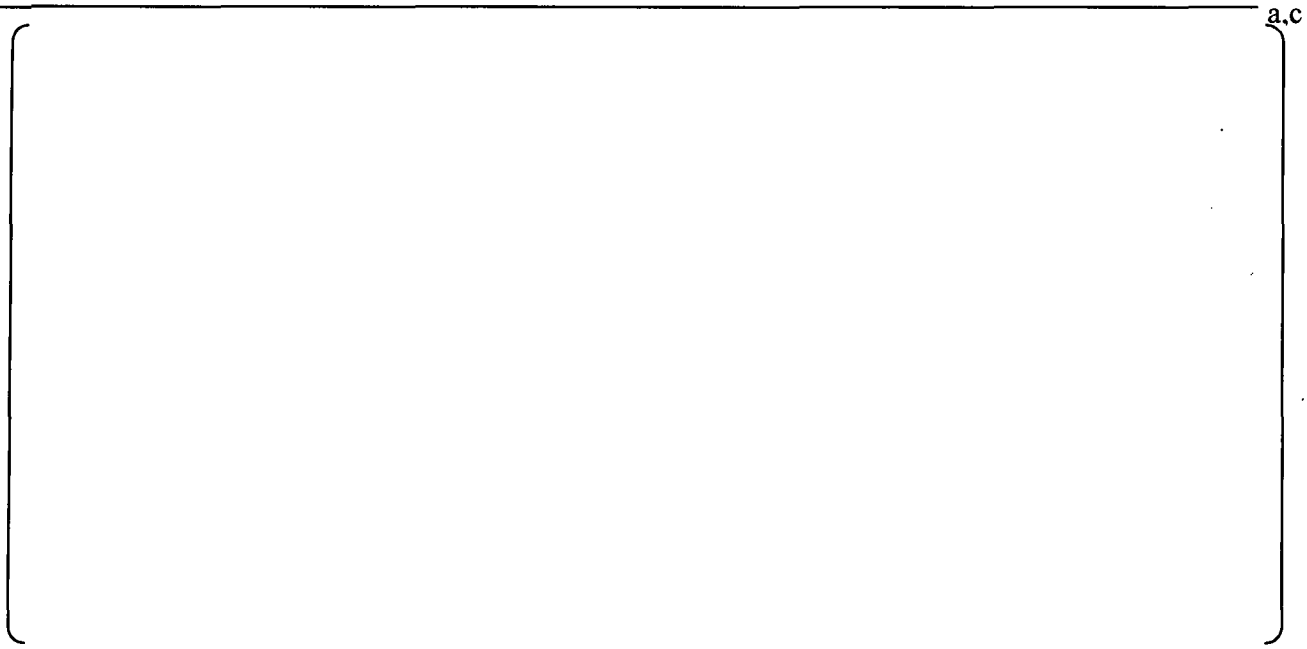

Figure 2 Functional Block Diagram of TRN module

Table 1 FPGA functions in the TRN module

a,c

FPGA	Description

3.4 Self Diagnosis

a,c

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⓪ Feb.5, 2013	–	First Issue	K.Wakita Feb.5,2013	T.Tarumi Feb.5,2013	H.Ito Feb.5,2013	H.Ito Feb.5,2013
① Feb. 15. 2013	1 3	Descriptions on communication were improved. Figure number was changed from 3-1 to 1. Figure number was changed from 3-2 to 2. Table number was changed from 3-1 to 1.	K. Wakita Feb 15. 2013	T. Tarumi Feb. 15, 2013	H. Ito Feb. 15 2013	H. Ito Feb. 15. 2013

TRN Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: TRN module

(2) Module Number: HNS0531

(3) Unit and application to be used

LPRM/APRM, LPRM, FLOW, SRNM Units for BWR-2, 3, 4, 5 and 6 Application

OPRM, LPRM, APRM, SRNM, DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S Units for ABWR Application

(4) Number of FPGA on the module: Six

2 Functional Summary

The TRN module has two data processing trains that collect data from other modules mounted in the same unit, generate a data frame in a fixed format by multiplexing the collected data, and transmit the data frame to external over fiber optic links and to other modules in the same unit. When installed in the LPRM/APRM unit, the TRN module receives the data frame from the APRM module in the same unit, and transmits the data frame over fiber optic links instead of the data frame generated in the TRN module.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the TRN module.

3.2 Inputs and Outputs

The TRN module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

a,c

[

]

3.2.2 Outputs

(1) Output signals via process input and output modules

a,c

[

]

(2) Outputs via communication modules

a,c

[

]

(3)Others to be noted

a,c

[

]

a,c

Figure 1 The front panel of the TRN module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the TRN module. Table 1 provides functions of each FPGA.

a,c

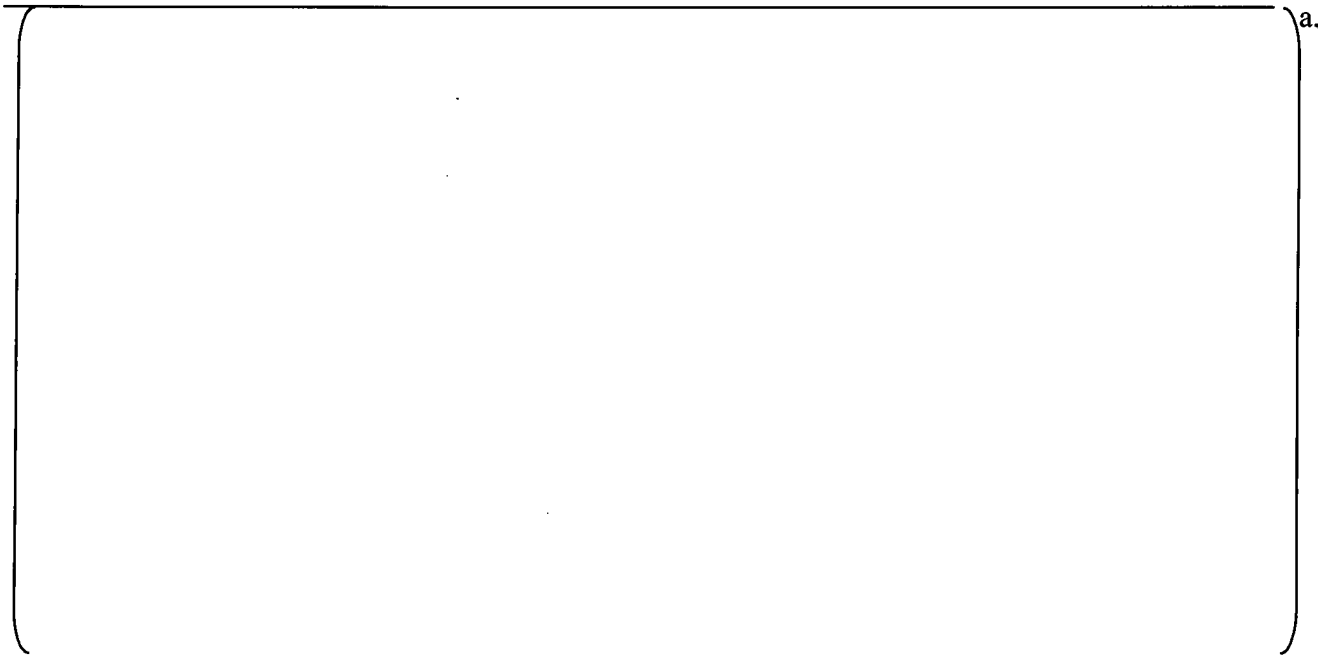

Figure 2 Functional Block Diagram of TRN module

Table 1 FPGA functions in the TRN module

FPGA	Description

a,c

3.4 Self Diagnosis

a,c

Watchdog timers in each data processing trains monitors operation of FPGAs. The TRN module shows the results of the monitoring on the front panel.

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⓪ Feb.13, 2013	–	First Issue	K.Wakita Feb.13,2013	T.Tarumi Feb.13,2013	H.Ito Feb.13,2013	H.Ito Feb.13,2013
① Feb.15,2013	1 3	Descriptions on communication were improved. Figure number was changed from 3-1 to 1. Figure number was changed from 3-2 to 2. Table number was changed from 3-1 to 1.	K.Wakita Feb.15,2013	T.Tarumi Feb.15,2013	H.Ito Feb.15,2013	H.Ito Feb.15,2013

RCV Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: RCV module

(2) Module Number: HNS540

(3) Unit and application to be used

LPRM/APRM Unit for BWR-2, 3, 4, 5 and 6 Application

LPRM, APRM, DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, SPTM for ABWR Application

(4) Number of FPGA on the module: Eight

2 Functional Summary

The RCV module has four independent data processing trains that receive optical signals containing a fixed format data frame from external, and transmits the data frame to other modules mounted in the same unit through point-to-point serial communication links.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the RCV module.

3.2 Inputs and Outputs

The RCV module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

3.2.2 Outputs

(1) Output signals via process input and output modules a,c

[ ]

(2) Outputs via communication modules a,c

[ ]

(3) Others to be noted

a,c

a,c

Figure 1 The front panel of the RCV module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the RCV module. Table 1 provides functions of each FPGA.

a,c

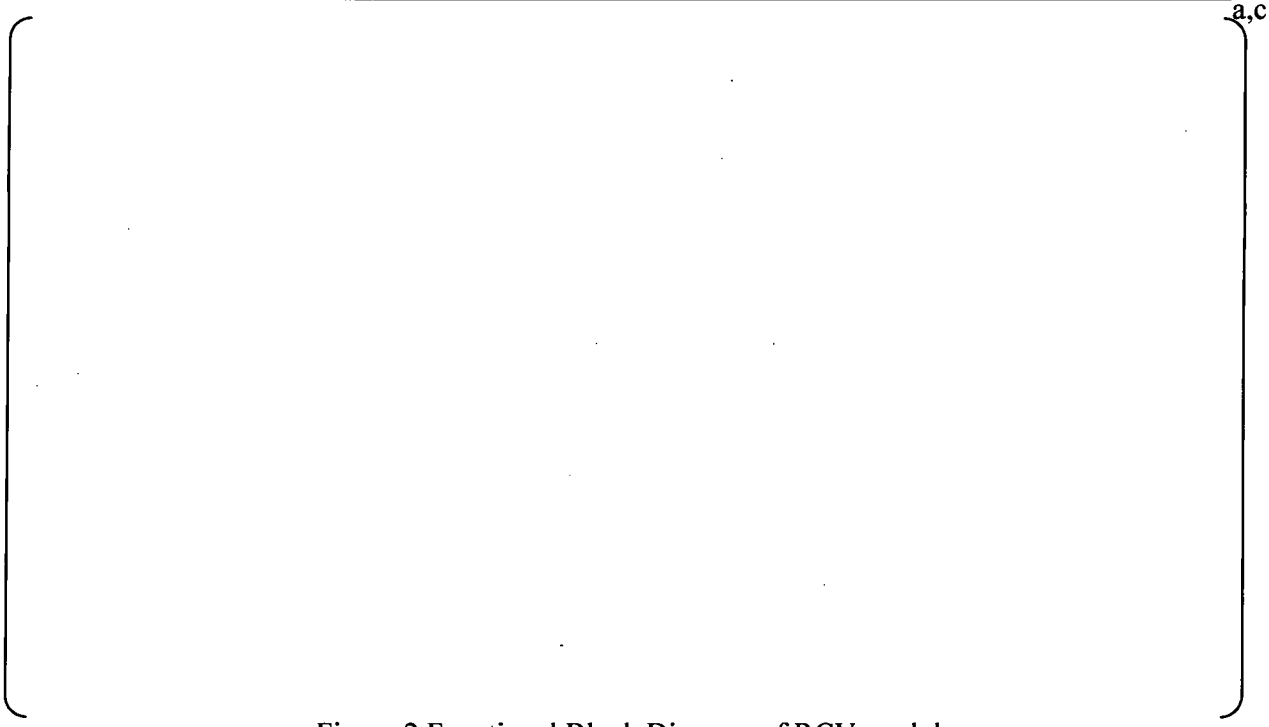

Figure 2 Functional Block Diagram of RCV module

Table 1 FPGA functions in the RCV module

FPGA	Description

a,c

3.4 Self Diagnosis

a,c

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⓪ Feb.5. 2013	–	First Issue	K.Wakita Feb.5,2013	T.Tanimi Feb.5,2013	H.Ito Feb.5,2013	H.Ito Feb.5,2013
① Feb. 15 2013	1 2 3	Descriptions on communication were improved. Figure number was changed from 3-1 to 1. Figure number was changed from 3-2 to 2. Table number was changed from 3-1 to 1. Description on self diagnosis was improved.	K.Wakita Feb 15.2013	T. Tanimi Feb. 15, 2013	H. Ito Feb. 15. 2013	H. Ito Feb. 15. 2013

RCV Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: RCV module

(2) Module Number: HNS0541

(3) Unit and application to be used

LPRM, LPRM/APRM Unit for BWR-2, 3, 4, 5 and 6 Application

OPRM, LPRM, APRM, DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, SPTM for ABWR Application

(4) Number of FPGA on the module: Eight

2 Functional Summary

The RCV module has four independent data processing trains that receive optical signals containing a fixed format data frame from external, and transmits the data frame to other modules mounted in the same unit through point-to-point serial communication links.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the RCV module.

3.2 Inputs and Outputs

The RCV module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[N/A]a,c

(2) Input signals via communication modules

[ ]a,c

3.2.2 Outputs

(1) Output signals via process input and output modules

[N/A]a,c

(2) Outputs via communication modules

[N/A]a,c

(3) Others to be noted

[ ]a,c

[ ]a,c

Figure 1 The front panel of the RCV module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the RCV module. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of RCV module

Table 1 FPGA functions in the RCV module

FPGA	Description

a,c

3.4 Self Diagnosis

a,c

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変更記録 REVISIONS						
(0) Feb.13. 2013	–	First Issue	K.Wakita Feb.13,2013	T.Tarumi Feb.13,2013	H.Ito Feb.13,2013	H.Ito Feb.13,2013
(1) Feb. 15. 2013	1 2 3	Descriptions on communication were improved. Figure number was changed from 3-1 to 1. Figure number was changed from 3-2 to 2. Table number was changed from 3-1 to 1. Description on self diagnosis was improved.	K. Wakita Feb 15. 2013	T. Tarumi Feb.15,2013	H. Ito Feb. 15. 2013	H. Ito Feb 15. 2013

LVPS Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LVPS module

(2) Module Number: HNS500

(3) Unit and application to be used

LPRM/APRM, LPRM, FLOW, OPRM, SRNM Units for BWR-2, 3, 4, 5 and 6 Application

LPRM, APRM, OPRM, SRNM, DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S Units for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The LVPS module is a plug-in type direct current (DC) power supply mounted in a unit and supplies DC power to other modules in the same unit through the backplane. Toshiba FPGA-based unit mount two redundant LVPSs, and either alone provide sufficient power to operate the unit. The LVPS module monitors the output voltage inside the power supply, and generates an alarm signal in case of failure.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the LVPS module.

3.2 Inputs and Outputs

The LVPS module has the following inputs and outputs.

3.2.1 Inputs

[N/A] a,c

3.2.2 Outputs

[The LVPS module provides a discrete module which has a function of status indicator in the same unit through the backplane] a,c

a,c

Figure 1 The front panel of the LVPS module

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⓪ Feb.8. 2013	-	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb. 15, 2013	1	Improve description in Section 2 and 3. Figure number was changed from 3-1 to 1	K.Wakita Feb 15, 2013	T.Tarumi Feb. 15, 2013	H. Ito Feb. 15, 2013	H. Ito Feb. 15, 2013

AO Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: AO module

(2) Module Numbers: HNS515, HNS516, HNS517, HNS518

(3) Unit and application to be used

LPRM/APRM, LPRM, FLOW, SRNM Units for BWR-2, 3, 4, 5 and 6 Application

LPRM, APRM, SRNM, SPTM Units for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The AO module provides sixteen 12-bit analog outputs to external equipment. The AO module receives individual digital values from other modules in the same unit through point-to-point copper serial communication links on the backplane. The AO module converts each output's digital data into an analog output value. The model number specifies the output signal voltage range for all of the digital-to-analog converters.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the AO module.

3.2 Inputs and Outputs

The AO module has the following inputs and outputs.

3.2.1 Inputs

3.2.2 Outputs

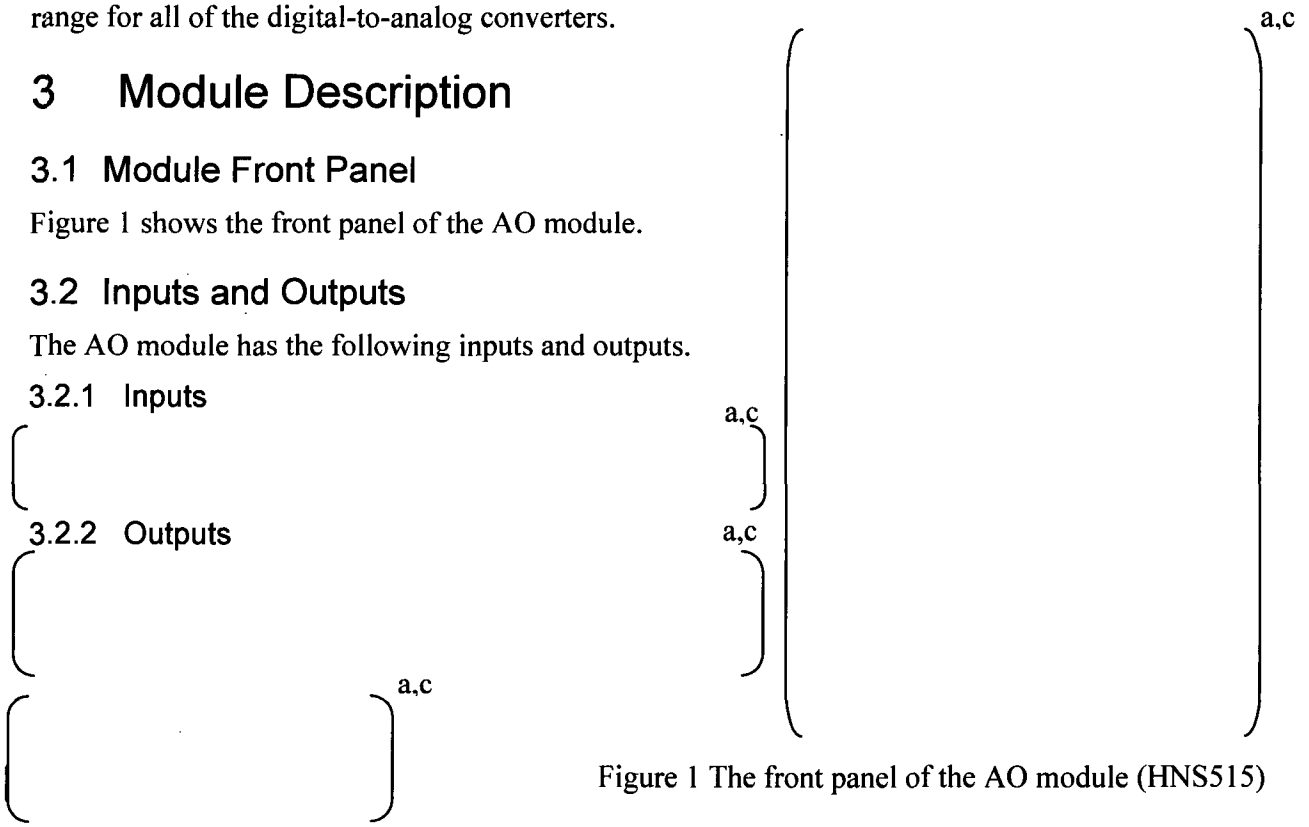

Figure 1 The front panel of the AO module (HNS515)

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変更記録 REVISIONS						
0 Feb.8, 2013	–	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
1 Feb. 15, 2013	1	Descriptions in Section 2 and 3 were improved. Added information on the communication.	K.Wakita Feb.15, 2013	T.Tarumi Feb.15,2013	H. Ito Feb.15.2013	H. Ito Feb.15.2013

DIO Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: DIO module

(2) Module Number: HNS520

(3) Unit and application to be used

LPRM/APRM, LPRM, FLOW, SRNM Units for BWR-2, 3, 4, 5 and 6 Application

LPRM, APRM, OPRM, SRNM Units for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The DIO module provides for sampling four discrete inputs from external equipment, and 16 discrete outputs to external equipment. The received signals are sent to other modules in the same unit. The output signals are provided from other modules in the same unit. The inputs and outputs are provided to the DIO module through the backplane (which Toshiba refers to as a middle plane) on copper point-to-point discrete wiring.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the DIO module.

3.2 Inputs and Outputs

The DIO module has the following inputs and outputs.

3.2.1 Inputs

a,c

3.2.2 Outputs

a,c

a,c

Figure 1 The front panel of the DIO module

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⓪ Feb.5. 2013	–	First Issue	K.Wakita Feb.5,2013	T.Tarumi Feb.5,2013	H.Ito Feb.5,2013	H.Ito Feb.5,2013
① Feb. 15. 2013	1	Descriptions in Section 2 and 3 were improved Figure number was changed from 3-1 to 1.	K. Wakita Feb 15. 2013	T. Tarumi Feb. 15. 2013	N. Ito Feb. 15. 2013	H. Ito Feb. 15. 2013

BLANK Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: BLANK module

(2) Module Number: HNS490

(3) Unit and application to be used
LPRM/APRM, LPRM Units for BWR-2, 3, 4, 5 and 6 Application

(4) Number of FPGA on the module: None

2 Functional Summary

The BLANK module fills a unit slot instead of an LPRM module. The BLANK module bypasses alarm signal lines that take OR (logical disjunction) of each LPRM module alarm.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the BLANK module.

3.2 Inputs and Outputs

The BLANK module has the following inputs and outputs through the backplane.

3.2.1 Inputs

a,c

[ ]

3.2.2 Outputs

a,c

[ ]

a,c

[ ]

Figure 1 The front panel of the BLANK module

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⓪ Feb.8. 2013	-	First Issue	K.Wakita Feb.8,2013	T.Tarumi Feb.8,2013	H.Ito Feb.8,2013	H.Ito Feb.8,2013
① Feb.15.2013	1	Figure number 3-1 was changed to 1.	K.Wakita Feb.15.2013	T.Tarumi Feb.15.2013	H.Ito Feb.15.2013	H.Ito Feb.15.2013

CELL Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: CELL module

(2) Module Number: HNS0400

(3) Unit and application to be used
OPRM Unit for ABWR Application

(4) Number of FPGA on the module: Eleven

2 Functional Summary

The CELL module converts LPRM levels to normalized oscillation levels, and provides the data to AGRD and PBD module for trip determinations.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the CELL module**Figure** .

3.2 Inputs and Outputs

The CELL module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

a,c

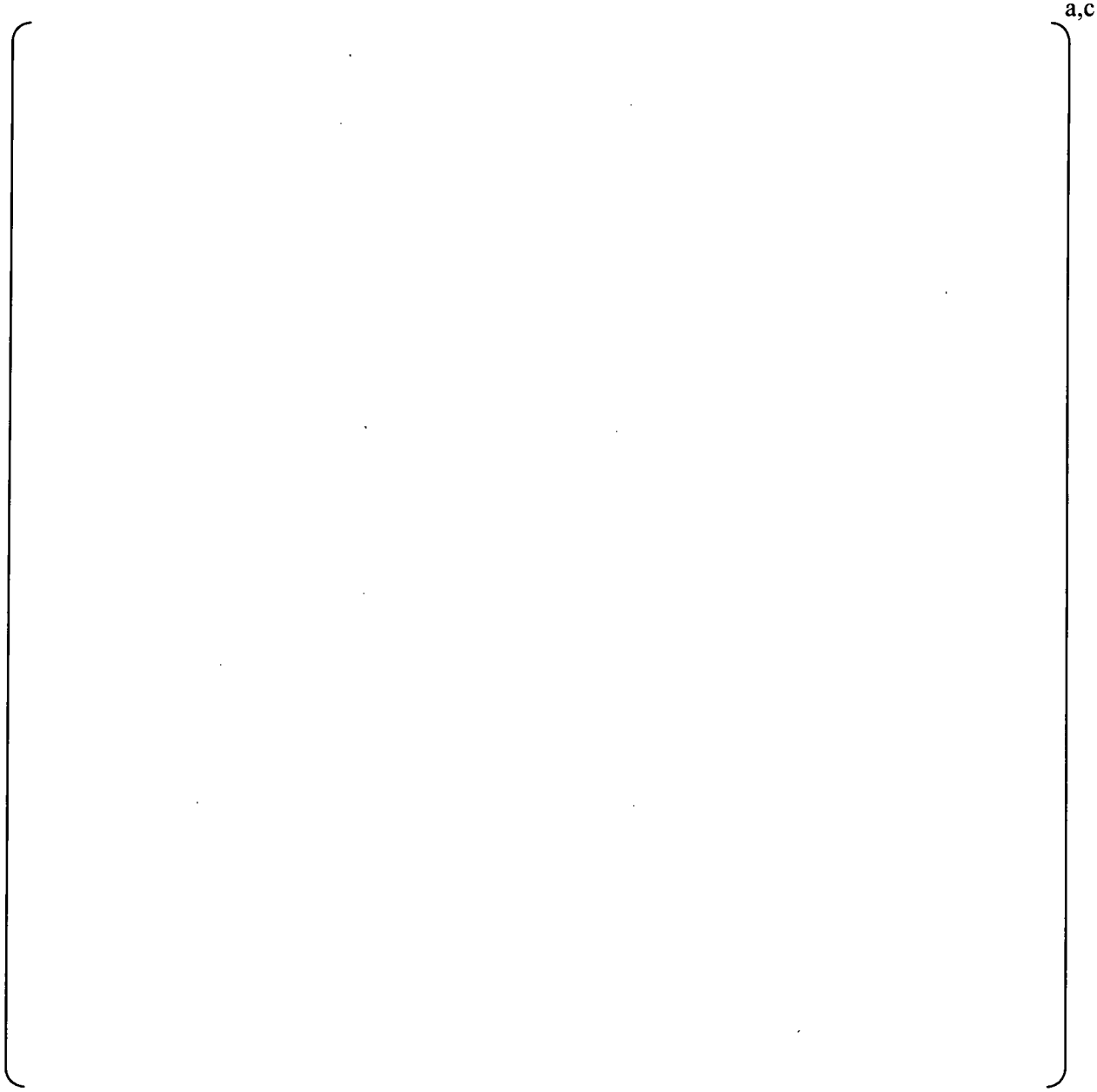

Figure 1 The front panel of the CELL module

3.2.2 Outputs

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication modules

a,c

3.3 FPGA functions

Figure 2**Figure** shows Functional Block Diagram of the CELL module where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of CELL module

Table 1 FPGA functions in the CELL module

a,c

FPGA	Description

[ ] a,c

3.4 Self Diagnosis

The CELL module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

[ ] a,c

3.4.2 Inoperable Trip

[ ] a,c

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⓪ Feb 25,2013	–	First Issue	K. Wakita Feb 25,2013	T. Tarumi Feb 25,2013	H. Ito Feb 25,2013	H. Ito Feb 25,2013
① Mar. 11, 2013	1	Editorial error correction.	K. Wakita Mar 11, 2013	T. Tarumi Mar. 11, 2013	H. Ito Mar. 11, 2013	H. Ito Mar. 11, 2013

DAT/ST Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: DAT/ST module

(2) Module Number: HNS0410

(3) Unit and application to be used
OPRM Unit for ABWR Application

(4) Number of FPGA on the module: Two

2 Functional Summary

The DAT/ST module receives data from CELL module, AGRD module, PBD module and LVPS module, multiplexes these data, and outputs them to the TRN module.

The DAT/ST module also displays input and power status on the front panel.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the DAT/ST module.

3.2 Inputs and Outputs

The DAT/ST module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

a,c

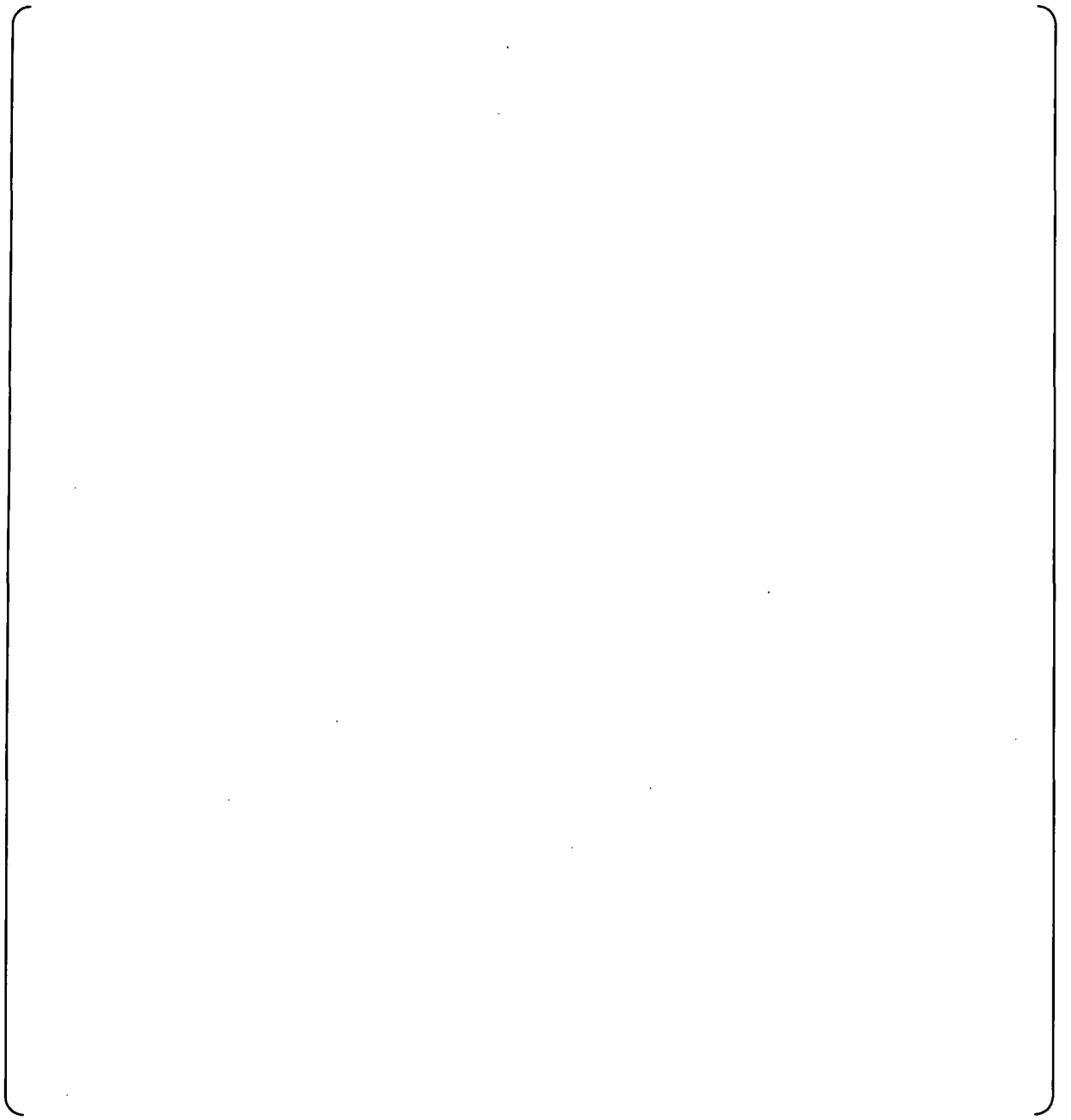

Figure 1 The front panel of the DAT/ST module

3.2.2 Outputs

(1) Output signals via process input and output modules a,c

(2) Output signals via communication modules

a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the DAT/ST module where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of DAT/ST module

Table 1 FPGA functions in the DAT/ST module

a,c

FPGA	Description

3.4 Self Diagnosis

The DAT/ST module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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① Mar. 11, 2013	1,2	Editorial error correction	K. Wakita Mar 11, 2013	T. Tarumi Mar. 11, 2013	H. Ito Mar. 11, 2013	H. Ito Mar. 11, 2013

AGRD Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: AGRD module

(2) Module Number: HNS0420

(3) Unit and application to be used
OPRM Unit for ABWR Application

(4) Number of FPGA on the module: Eight

2 Functional Summary

The AGRD module receives OPRM cell data from the CELL module, monitors power oscillation for each cell using the Amplitude-Based Algorithm (ABA) and Growth Rate-based detection Algorithm (GRA). When the power oscillation is detected by ABA or GRA, the AGRD module generates a trip signal to DIO module. The AGRD module transmits AGRD calculation data to the DAT/ST module.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the AGRD module.

3.2 Inputs and Outputs

The AGRD module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

a,c

Figure 1 The front panel of the AGRD module

3.2.2 Outputs

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication modules

a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the AGRD module where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of AGRD module

Table 1 FPGA functions in the AGRD module

a,c

FPGA	Description

a,c

[ ]

3.4 Self Diagnosis

The AGRD module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

[ ]

3.4.2 Inoperable Trip

a,c

[ ]

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⓪ Feb 25,2013	-	First Issue	K. Wakita Feb 25,2013	T. Tarumi Feb 25,2013	H. Ito Feb 25,2013	H. Ito Feb 25,2013
① Mar. 11. 2013	1,3	Editorial error correction.	K. Wakita Mar 11. 2013	T. Tarumi Mar. 11, 2013	H. Ito Mar. 11. 2013	H. Ito Mar. 11. 2013

PBD Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: PBD module

(2) Module Number: HNS0430

(3) Unit and application to be used
OPRM Unit for ABWR Application

(4) Number of FPGA on the module: Seven

2 Functional Summary

The PBD module receives OPRM cell data from the CELL module, monitors power oscillation for each cell using the Period-Based Detection Algorithm (PBDA). When the power oscillation is detected by PBDA, the PBD module generates a trip signal to DIO module. The PBD module transmits PBDA calculation data to the DAT/ST module.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the PBD module**Figure** .

3.2 Inputs and Outputs

The PBD module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

a,c

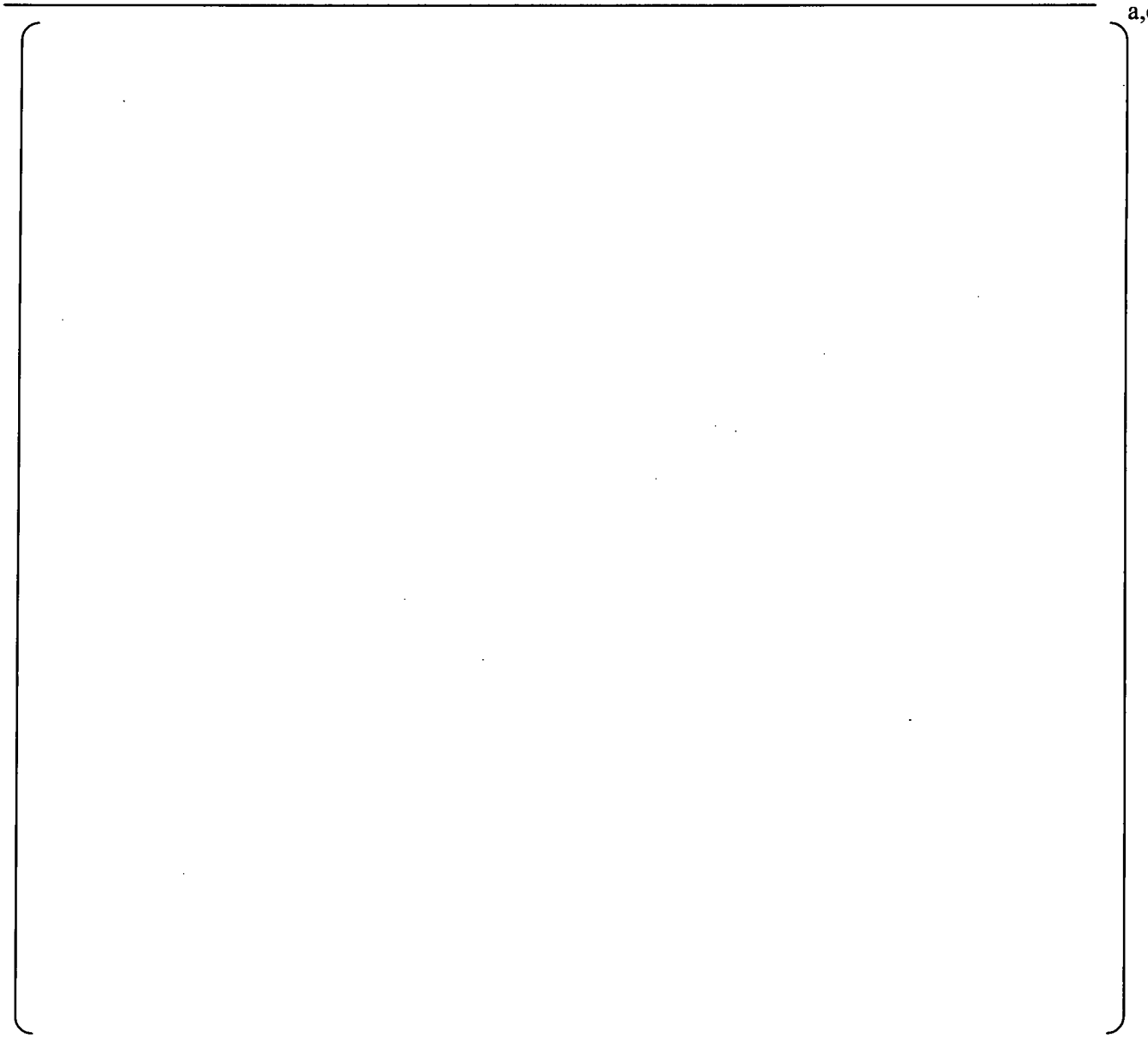

Figure 1 The front panel of the AGRD module

3.2.2 Outputs

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication modules

a,c

3.3 FPGA functions

Figure 2**Figure** shows Functional Block Diagram of the PBD module where each block is an FPGA. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of PBD module

Table 1 FPGA functions in the PBD module

a,c

FPGA	Description

3.4 Self Diagnosis

The PBD module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

[

]

3.4.2 Inoperable Trip

a,c

[

]

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① Mar. 11, 2013	1	Editorial error correction.	K. Wakita Mar. 11, 2013	T. Tarumi Mar. 11, 2013	H. Ito Mar. 11, 2013	H. Ito Mar. 11, 2013

SRNM Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: SRNM module

(2) Module Number: HNS0101

(3) Unit and application to be used
SRNM Unit for BWR-2, 3, 4, 5, 6 and ABWR Application

(4) Number of FPGA on the module: Twenty

2 Functional Summary

The SRNM module calculates the count-rate-based neutron flux and Mean Square Voltage (MSV) based neutron flux from the SRNM detector signal. In addition, the SRNM module calculates the SRNM neutron flux and period from the count-rate-based neutron flux and the MSV based neutron flux.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the SRNM module.

3.2 Inputs and Outputs

The SRNM module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[a,c]

(2) Input signals via communication modules

[a,c]

a,c

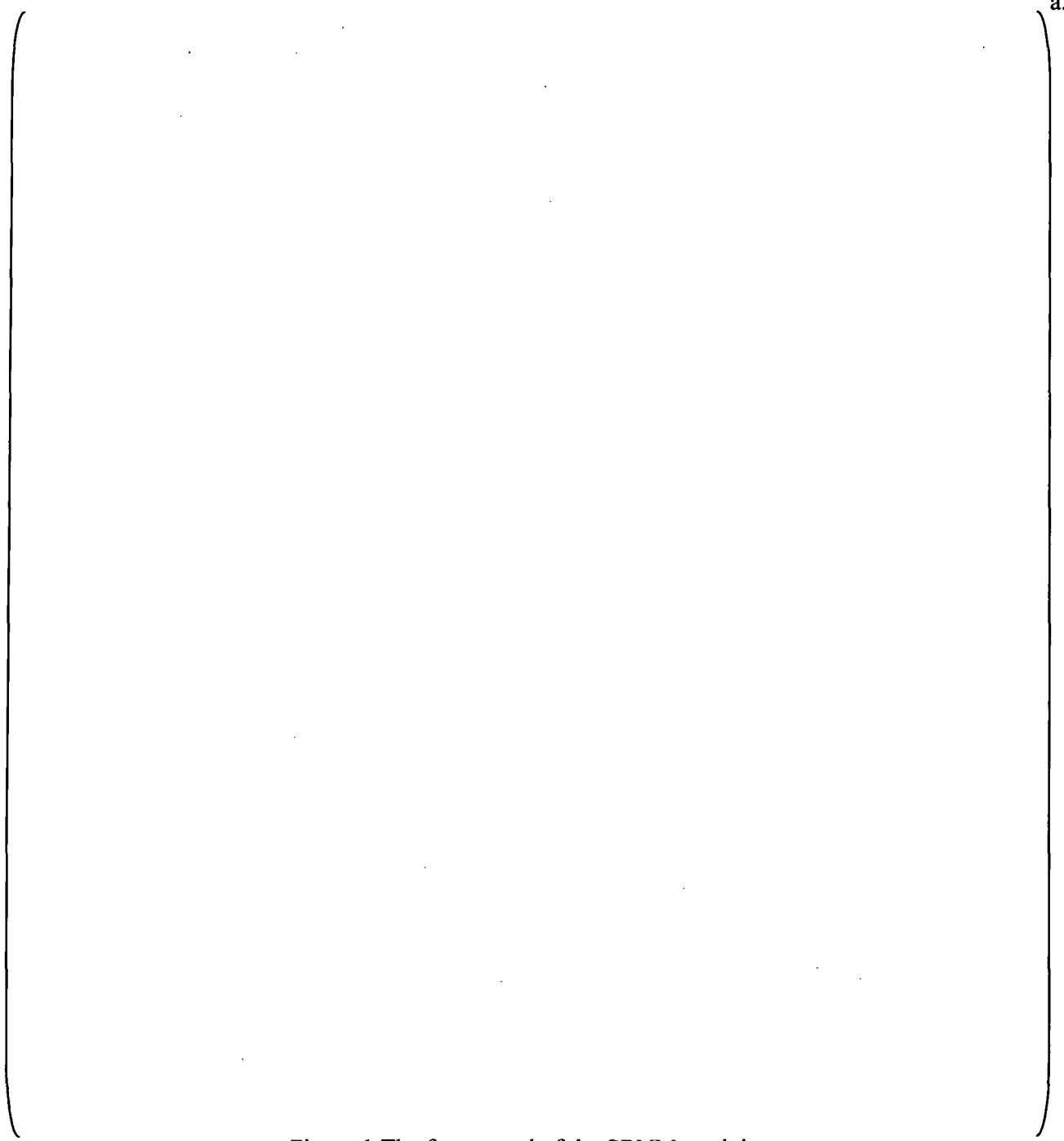

Figure 1 The front panel of the SRNM module

3.2.2 Outputs

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication modules

[ ] a,c

(3) Others to be noted

[through point-to-point copper serial communication links on the backplane in the SRNM unit.] a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the SRNM module. Table 1 provides functions of each FPGA.

[ ] a,c

Figure 2 Functional Block Diagram of SRNM module

Table 1 FPGA functions in the SRNM module

FPGA	Description
[ ]	

a,c

a,c

3.4 Self Diagnosis

The SRNM module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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⓪ Feb.25,2013	–	First Issue	K.Wakita Feb.25,2013	K.Wakita Feb.25,2013	T.Tanumi Feb.25,2013	H.Ito Feb.25,2013
① Mar. 11. 2013	1 3	3.2.1 "(10)" was deleted. 3.2.2.(3) Output Description was detailed to clarify.	K. Wakita Mar. 11. 2013	K. Wakita Mar. 11, 2013	T. Tanumi Mar. 11, 2013	H. Ito Mar. 11, 2013

TRIP Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: TRIP module

(2) Module Number: HNS0117

(3) Unit and application to be used
SRNM Unit for BWR-2, 3, 4, 5, 6 and ABWR Application

(4) Number of FPGA on the module: Four

2 Functional Summary

The TRIP module outputs trip and alarm signals to DIO module and shows the alarm on the module front panel when SRNM levels (SRNM Count Rate, SRNM %Power level, SRNM period,) exceeds their setpoints. The SRNM Inoperable trip is outputted not from the TRIP module but from ST/MON module. Also, the TRIP module converts measurement data as analog data and outputs to AO module.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the TRIP module.

3.2 Inputs and Outputs

The TRIP module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

a,c

Figure 1 The front panel of the TRIP module

3.2.2 Outputs

(1) Output signals via process input and output modules

a,c

[ ] a,c

(2) Outputs signal via communication modules

[ ] a,c

(3) Other to be noted

[ ] a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the TRIP module. Table 1 provides functions of each FPGA.

[ ] a,c

Figure 2 Functional Block Diagram of TRIP module

Table 1 FPGA functions in the TRIP module

FPGA	Description
[ ]	[ ]

a,c

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

[ ]a,c

3.4.2 Inoperable Trip

[ ]a,c

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⓪ Feb.25.2013	–	First Issue	K.Wakita Feb.25.2013	K.Wakita Feb.25.2013	T.Tarumi Feb.25.2013	H.Ito Feb.25.2013
① Mar.11.2013	2 3	Fig1 : Descriptions of select push button 1 and 2 were detailed to clarify. 3.3 Module name was corrected.	K.Wakita Mar.11.2013	K.Wakita Mar.11.2013	T.Tarumi Mar.11,2013	H.Ito Mar.11.2013

PARAMETER Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: PARAMETER module

(2) Module Number: HNS0121

(3) Unit and application to be used
SRNM Unit for BWR-2, 3, 4, 5, 6 and ABWR Application

(4) Number of FPGA on the module: Two

2 Functional Summary

The PARAMETER module displays SRNM parameters value received from the SRNM module and monitor data received from ST/MON. Input data are shown in 3.2.1.(3). The parameters can be changed on the module front panel in CAL mode and the PARAMETER module outputs the changed data and the change request signal shown in 3.2.2.(3) to the SRNM module and the data and the change request signal shown in 3.2.2.(3) to the ST/MON module. The PARAMETER module receives high voltage and discrimination valtage from the ANALYZER module and changes them when the SRNM unit performs discrimination characteristic measurement and plateau characteristic measurement in STANDBY mode. All the parameter setpoints are sent to the TRN module via the ANALYZER module.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the PARAMETER module.

3.2 Inputs and Outputs

The PARAMETER module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

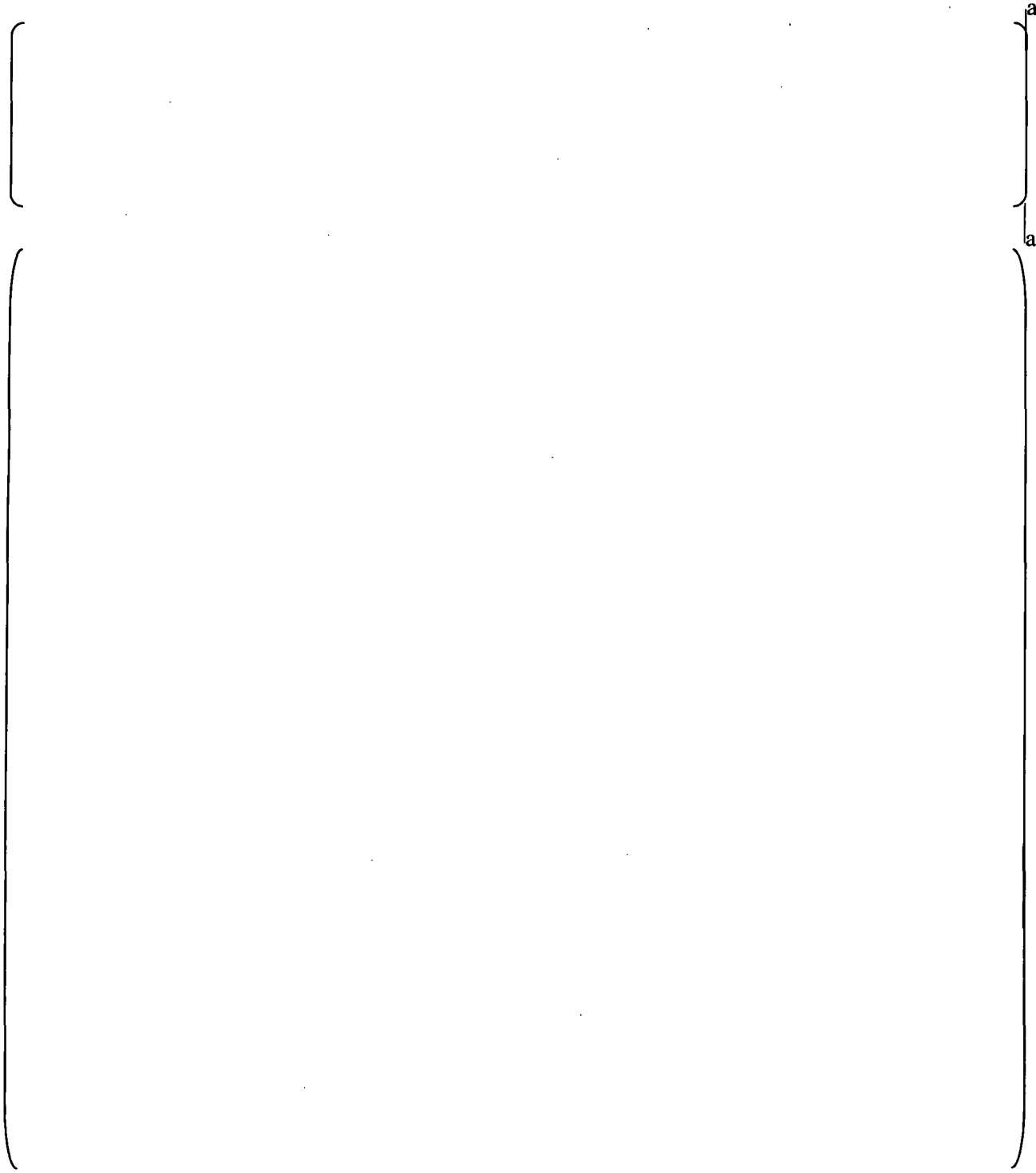
[ ]

(3) Other the note a,c

[ ]

. T

a,c



a,c

Figure 1 The front panel of the PARAMETER module

3.2.2 Outputs

(1) Output signals via process input and output module

[ ]a,c

(2) Output signals via communication module

[ ]a,c

(3) Other the note

(a,c)

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the PARAMETER module. Table 1 provides functions of each FPGA.

(a,c)

Figure 2 Functional Block Diagram of PARAMETER module

Table 1 FPGA functions in the PARAMETER module

FPGA	Description

a,c

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

[

a,c]

3.4.2 Inoperable Trip

[

a,c]

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⓪ Feb.25.2013	–	First Issue	K.Wakita Feb.25.2013	K.Wakita Feb.25.2013	T.Tarumi Feb.25.2013	H.Ito Feb.25.2013
① Mar. 11.2013	1 2 3	Summary description was correct words. Inputs descriptions were detailed to clarify. Figure 2 was correct.	K.Wakita Mar.11.2013	K.Wakita Mar.11.2013	T.Tarumi Mar.11, 2013	H.Ito Mar.11, 2013

ST/MON Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: ST/MON module

(2) Module Number: HNS0131

(3) Unit and application to be used
SRNM Unit for BWR-2, 3, 4, 5, 6 and ABWR Application

(4) Number of FPGA on the module: Four

2 Functional Summary

The ST/MON module is used to display inoperative and minor failure within the SRNM unit. The ST/MON module also monitors the power supply voltages..

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the ST/MON module.

3.2 Inputs and Outputs

The ST/MON module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

a,c

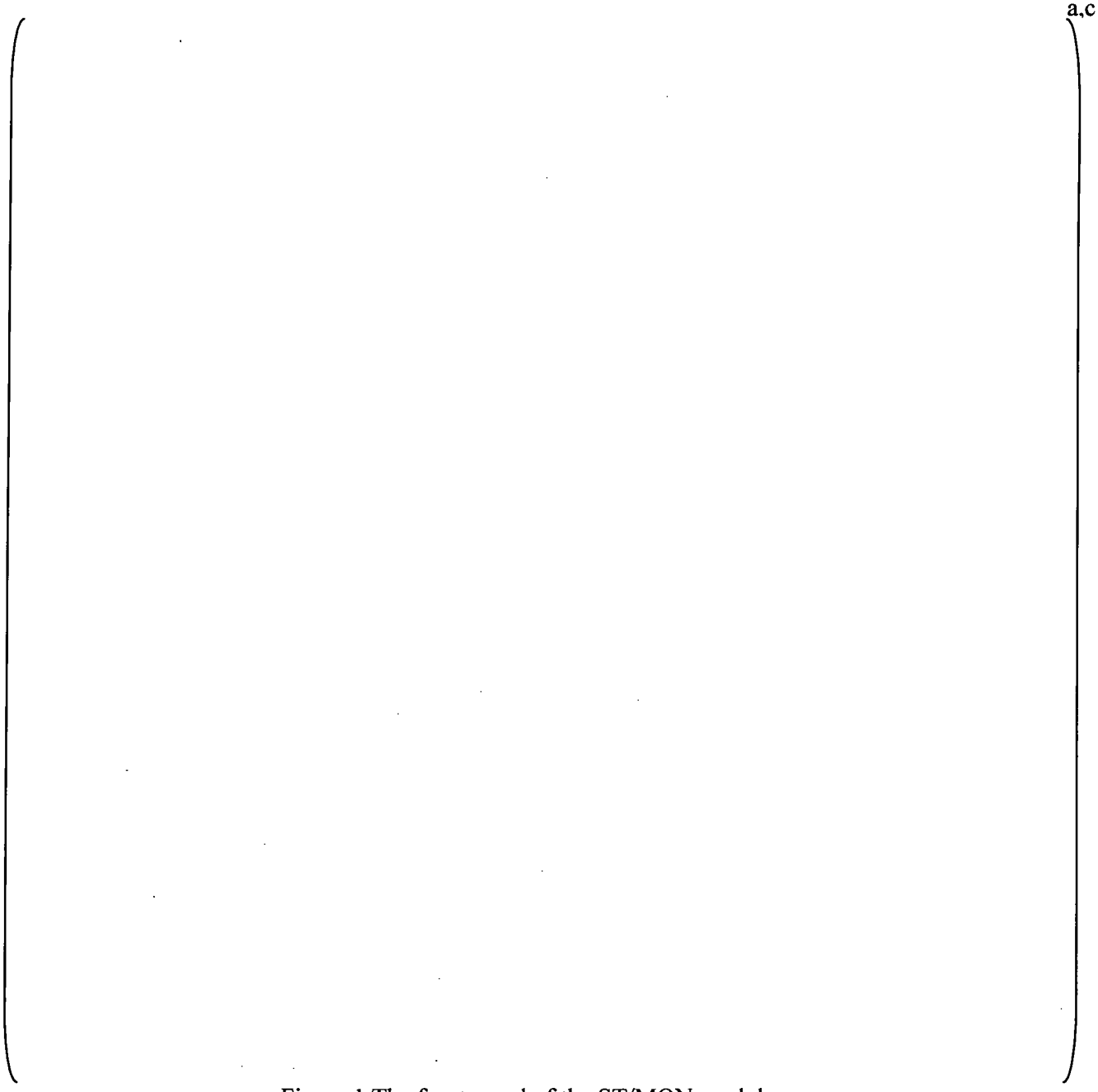

Figure 1 The front panel of the ST/MON module

3.2.2 Outputs

(1) Output signals via process input and output modules

a,c

[ ] a,c

(2) Output signals via communication modules

[ ] a,c

(3) Other to be noted

[ ] a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the ST/MON module. Table 1 provides functions of each FPGA.

[ ] a,c

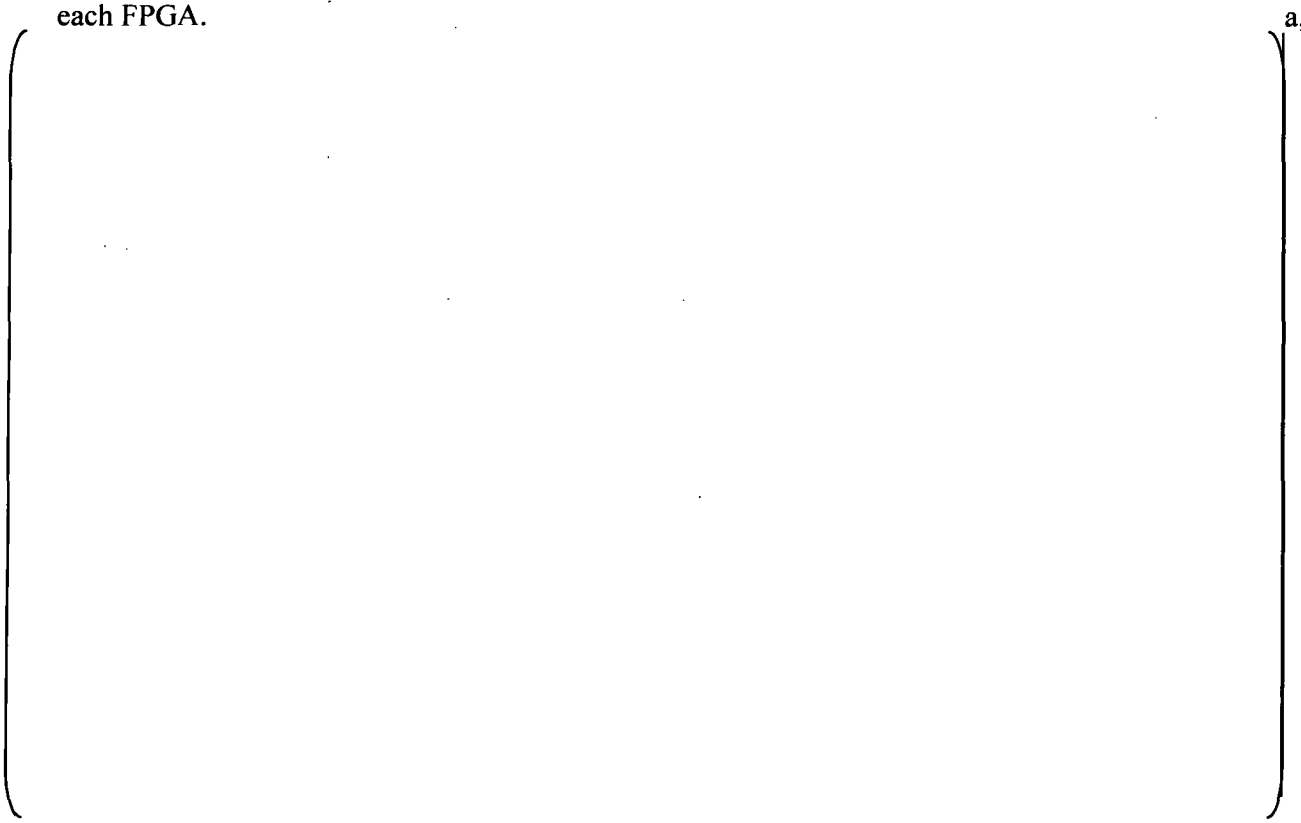

Figure 2 Functional Block Diagram of ST/MON module

Table 1 FPGA functions in the ST/MON module

FPGA	Description
[ ]	[ ]

a,c

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

[a,c]

3.4.2 Inoperable Trip

[a,c]

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① Mar.11.2013	1 1 2,3	2.Function Summary : Description was detailed to clarify. 3.2.1(3): Input Descriptions were detailed to clarify. 3.2.2 :Output descriptions were detailed to clarify.	K.Wakita Mar.11.2013	K.Wakita Mar.11.2013	T.Tarumi Mar.11.2013	H.Ito Mar.11.2013

ANALYZER Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: ANALYZER module

(2) Module Number: HNS0141

(3) Unit and application to be used
SRNM Unit for BWR-2, 3, 4, 5 , 6 and ABWR Application

(4) Number of FPGA on the module: Seven

2 Functional Summary

The ANALYZER module performs the Discrimination characteristics measurement and the Plateau characteristics measurement in STANDBY mode in the SRNM unit. In the Discrimination characteristic measurement, the ANALYZER module corrects the count values from the SRNM module when the Discrimination voltage is changed based on the starting voltage, the end voltage, the step voltage and the step time which are set on the module front panel of the ANALYZER module. In the Plateau characteristics measurement, the ANALYZER module corrects the Campbell values (MSV values) from the SRNM module when the High voltage is changed based on the starting high voltage, the end high voltage, the step voltage, and the step time which are set on the module front panel of the ANALYZER module. These measurement results are shown on the module front panel of the SRNM module via the TEST module.

Also, the ANALYZER module collects the data shown in the 3.2.2.(2) from the SRNM module, the TRIP module, the PARAMETER module and the ST/MON module and output them to the TRN module.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the ANALYZER module.

3.2 Inputs and Outputs

The STATUS module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication modules

a,c

[ ]

(3) Others to be noted

a,c

a,c

Figure 1 The front panel of the ANALYZER module

3.2.2 Outputs

(1) Output signals via process input and output module

[a,c]

(2) Output signals via communication module

[a,c]

(3) Others to be noted

[a,c]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the ANALYZER module. Table 1 provides functions of each FPGA.

[a,c]

Figure 2 Functional Block Diagram of ANALYZER module

Table 1 FPGA functions in the ANALYZER module

FPGA	Description

a,c

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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① Mar. 11. 2013	2,3 4	3.2.1 Input and 3.2.2 Output Discriptions were detailed to clarify. Table 1 ANADD description was detailed to clarify.	K.Wakita Mar. 11. 2013	K.Wakita Mar. 11. 2013	T. Tanami Mar. 11, 2013	H. Ito Mar. 11. 2013

TEST Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: TEST module

(2) Module Number: HNS0151

(3) Unit and application to be used
SRNM Unit for BWR-2, 3, 4, 5, 6 and ABWR Application

(4) Number of FPGA on the module: One

2 Functional Summary

The TEST module provides SRNM trip and alarm test to check trip and alarm determination function by changing the selected SRNM data (SRNM Count Rate, SRNM % Power Level (linear), SRNM Period, SRNM Neutron Flux value, and SRNM Preamplifier input conversion RMS voltage (MSV)) in CAL mode. The TEST module generates the selected SRNM data and test requirement signal to the SRNM module after the SRNM data are set on the TEST module front panel. The SRNM module receives these data and signal and performs the SRNM trip and alarm test function. In operation mode, trip and alarm test function is not performed. Also, the TEST module receives the Discrimination characteristics measurement data or the Plateau characteristics measurement data and sends that data to the SRNM module in STANDBY mode.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the TEST module.

3.2 Inputs and Outputs

The TEST module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules

[ ] a,c

(2) Input signals via communication modules

[ ] a,c

3.2.2 Outputs

(1) Output signals via process input and output modules

[ ] a,c

(2) Output signals via communication modules

[ ] a,c

(3) Others to be noted

[ ] a,c

[ ] a,c

Figure 1 The front panel of the TEST module

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the TEST module. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of TEST module

Table 1 FPGA functions in the TEST module

a,c

FPGA	Description

3.4 Self Diagnosis

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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⓪ Feb.25.2013	–	First Issue	K.Wakita Feb.25.2013	K.Wakita Feb.25.2013	T.Tarumi Feb.25.2013	H.Ito Feb.25.2013
① Mar.11.2013	2 2	3.2.(3) Output Description was detailed to clarify. Fig.1 each descriptions were detailed to clarify.	K.Wakita Mar.11.2013	K.Wakita Mar.11.2013	T.Tarumi Mar.11.2013	H.Ito Mar.11.2013

LVPS Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LVPS module

(2) Module Number: HNS505

(3) Unit and application to be used

SRNM Unit for BWR-2, 3, 4, 5, 6 and ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The LVPS module is a plug-in type direct current (DC) power supply mounted in a unit and supplies DC power to other modules in the same unit through the backplane. Toshiba FPGA-based unit mount two redundant LVPSs, and either alone provide sufficient power to operate the unit. The LVPS module monitors the output voltage inside the power supply, and generates an alarm signal in case of failure.

2.1 Module Front Panel

Figure 1 shows the front panel of the LVPS module

2.2 Inputs and Outputs

The LVPS module has the following inputs and outputs.

2.2.1 Inputs

[ ]a,c

2.2.2 Outputs

[ ]a,c

a,c

Figure 1 The front panel of the LVPS module

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⓪ Feb. 25. 2013	-	First Issue	K. Wakita Feb. 25, 2013	K Wakita Feb. 25. 2013	T. Tsuruno Feb. 25, 2013	M. Ito Feb. 25. 2013

RM Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: RM module

(2) Module Number: HNS0550

(3) Unit and application to be used
SRNM Unit for BWR2, 3, 4, 5, 6 and ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The RM module provides SRNM Range number and SRNM mode for SRNM range and mode display which is installed on the Main Control Panel or Large Display Panel.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the RM module.

3.2 Inputs and Outputs

The RM module has the following inputs and outputs.

3.2.1 Inputs

a,c

a,c

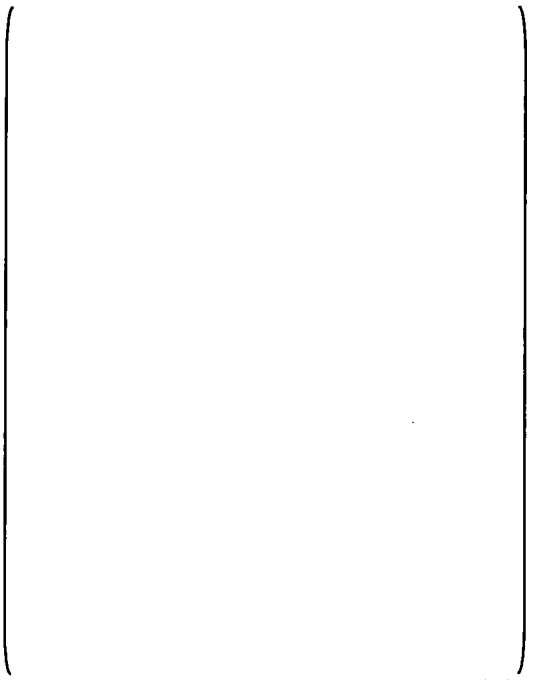

Figure 1 the front panel of the RM module

3.2.2 Outputs

a,c

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変更記号 REV.MARK 変更発行日 REV.ISSUED		変更箇所・変更内容 CHANGED PLACE AND CONTENTS	承認 APPROVED BY	調査 REVIEWED BY	担当 PREPARED BY	保管 REGISTERED
⓪ Feb.25, 2013	–	First Issue	K.Wakita Feb.25.2013	K.Wakita Feb.25.2013	T.Tarumi Feb.25.2013	H.Ito Feb.25.2013
① Mar.11, 2013	1 1	3.2.1 Input Description was detailed to clarify. 3.2.2 Onput Description was detailed to clarify.	K.Wakita Mar.11 2013	K.Wakita Mar.11 2013	T.Tarumi Mar.11, 2013	H Ito Mar.11, 2013

PA Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: PA module

(2) Module Number: HNS0560

(3) Unit and application to be used

SRNM Unit for BWR-2, 3, 4, 5, 6 and ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The PA module is a plug-in type unit power supply that supplies the low voltage (+15VDC, -15VDC) to the SRNM Preamplifier and high voltage (0V to 500VDC) to the SRNM detector via the SRNM Preamplifier. The high voltage output and its current limit output are controlled by analog outputs from the ST/MON module over point copper signals on the backplane.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the PA module

3.2 Inputs and Outputs

The PA module has the following inputs and outputs.

3.2.1 Inputs

a,c

[ ]

3.2.2 Outputs

a,c

[ ]

a,c

a,c

Figure 1 the front panel of the PA module

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⓪ Feb.25.2013	–	First Issue	K.Wakita Feb.25.2013	K.Wakita Feb.25.2013	T.Tarumi Feb.25.2013	H.Ito Feb.25.2013
① Mar.11.2013	1 1 1,2	2.Function Summary Discription was detailed to clarify. 3.2.1 Input Discription wasa detailed to clarify. 3.2.2.Output Description was detailed to clarify.	K.Wakita Mar.11.2013	K.Wakita Mar.11.2013	T.Tarumi Mar.11,2013	H.Ito Mar.11.2013

AITRIP1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: AITRIP1 module

(2) Module Number: HNS1100

(3) Unit and application to be used
DTF-RPS Unit, DTF-MSIV Unit, DTF-MSIV-S Unit, SPTM Unit, SPTM-S Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Four

2 Functional Summary

The AITRIP1 module samples analog data from a field sensor in the same division as the module, and compare the data with the setpoint to determine if the trip condition for the sensor is met. The AITRIP1 module outputs the discrete trip status via IO modules such as TRN module and DOC1 module. The AITRIP1 module also has the capability to accept the sampled signal from other module to determine the associated trip status.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the AITRIP1 module.

3.2 Input and Output

The AITRIP1 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication module

[ ]a,c

a,c

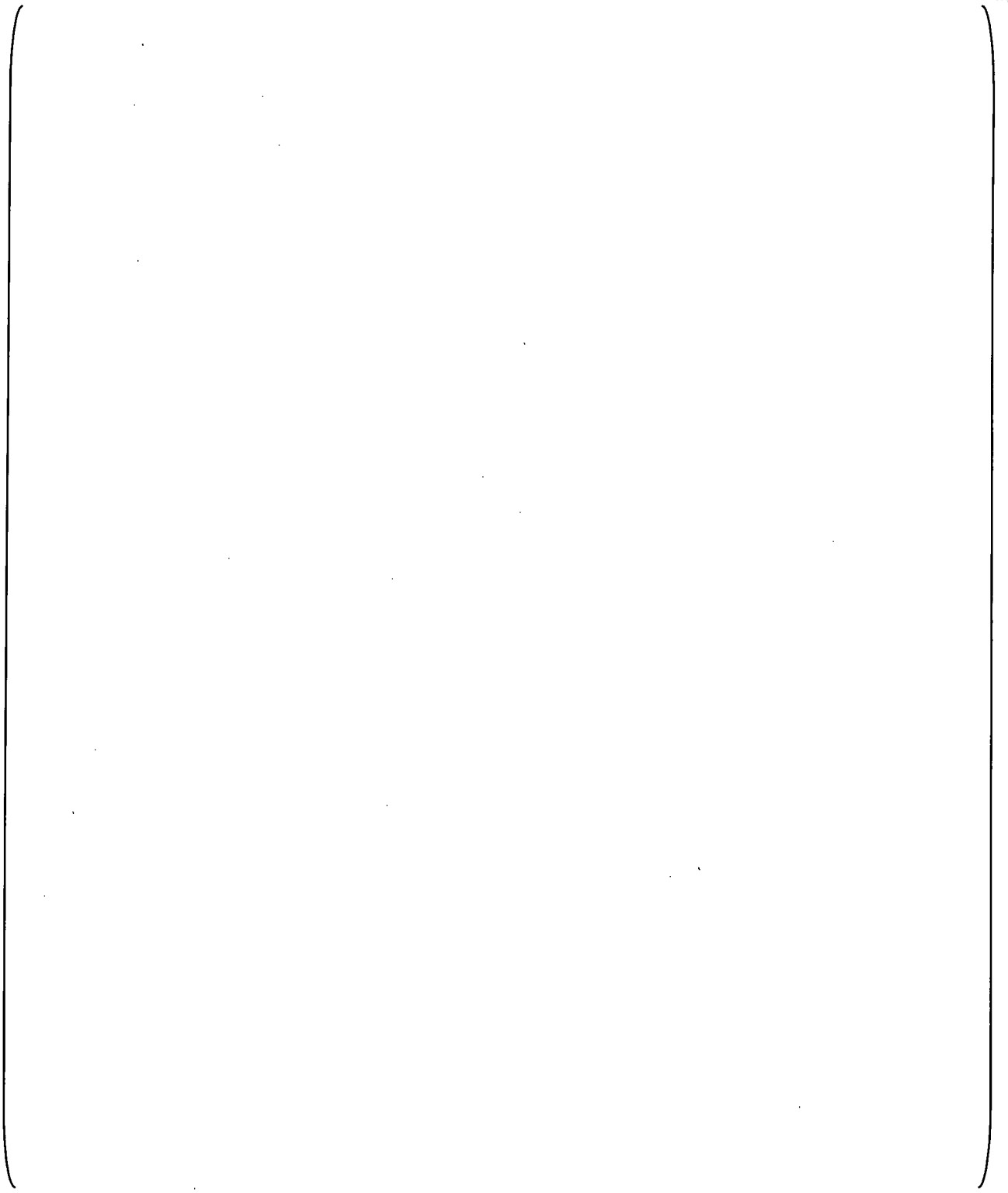

Figure 1 The front panel of the AITRIP1 module

3.2.2 Output Signals

(1) Output signals via process input and output modules a,c

[ ]

(2) Output signals via communication module a,c

[ ]

(3) Others to be noted a,c

[ ]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the AITRIP1 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA.

a,c

( )

Figure 2 Functional Block Diagram of AITRIP1 module

Table 1 FPGA functions in the AITRIP1 module

FPGA	Description

a,c

3.4 Self Diagnosis

The AITRIP1 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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⓪ Feb 18, 2013	—	First Issue	K. Wakita Feb 18,2013	K. Wakita Feb 18,2013	T. Joji Feb 18,2013	T. Joji Feb 18,2013
① Mar. 11, 2013	1	Description of the division sensor assigned was added.	K. Wakita Mar-11.2013	K. Wakita Mar-11.2013	T. Joji Mar. 8, 2013	T. Joji Mar. 11, 2013

SPTAVE1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: SPTAVE1 module

(2) Module Number: HNS1110

(3) Unit and application to be used: SPTM Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Two

2 Functional Summary

The SPTAVE1 module collects 16 suppression pool temperature data from the SPTSEL1 module and performs average calculation. The SPTAVE1 module outputs the average value of the 16 suppression temperature values to the AITRIP1 module.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the SPTAVE1 module.

3.2 Input and Output

The SPTAVE1 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication module a,c

[ ]

(3) Others to be noted a,c

[ ]

a,c

Figure 1 The front panel of the SPTAVE1 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

a,c

[ ]

(2) Output signals via communication module

a,c

[ ]

(3) Others to be noted

a,c

[by point-to-point serial communication links]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the SPTAVE1 module used for RTIS where each block is an FPGA if it is not noted otherwise. Table 1 provides functions of each FPGA.

a,c

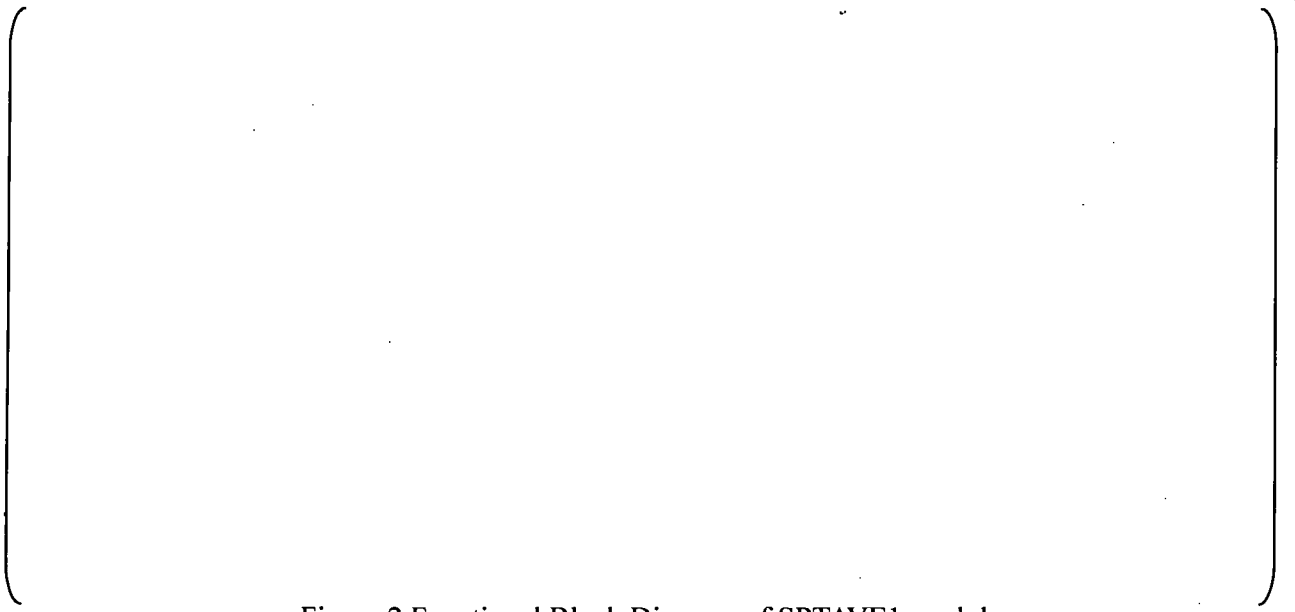

Figure 2 Functional Block Diagram of SPTAVE1 module

Table 1 FPGA functions in the SPTAVE1 module

FPGA	Description

a,c

3.4 Self Diagnosis

The SPTAVE1 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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0 Feb 19, 2013	–	First Issue	K. Wakita Feb 19,2013	K. Wakita Feb 19,2013	T. Joji Feb 18,2013	T. Joji Feb 19,2013
1 Mar. 11, 2013	1, 2	Description of the data communication was detailed to clarify.	K. Wakita Mar. 11, 2013	K. Wakita Mar. 11, 2013	T. Joji Mar. 8, 2013	Mar. 11, 2013

SPTSEL1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: SPTSEL1 module

(2) Module Number: HNS1120

(3) Unit and application to be used: SPTM Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Four

2 Functional Summary

The SPTSEL1 module collects suppression pool temperature data over communication link from two SPTM-S units each of which accepts eight suppression pool temperature inputs from eight AITRIP1 modules. The SPTSEL1 module collects a wide range suppression pool water level and four associated setpoints status via four AITRIP1 modules in the SPTM unit. The SPTSEL1 module also collects a narrow range suppression pool water level and an associated setpoint status via an AITRIP1 module. The SPTSEL1 module multiplexes all above mentioned data and sends them to the SPTAVE1 module which performs the averaging calculation.

The SPTSEL1 module also inputs the trip status information from the three AITRIP1 modules that determines the trip status regarding the average suppression pool temperature, and transfers them to the TRN module which transmits the data to external equipment.

The SPTAVE1 module outputs the narrow range suppression pool level and the trip status information to external equipment via process output modules.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the SPTSEL1 module.

3.2 Input and Output

The SPTSEL1 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules

a,c

[ ]

a,c

Figure 1 The front panel of the SPTSEL1 module

(2) Input signals via communication module

a,c

(3) Others to be noted

a,c

3.2.2 Output Signals

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication module

a,c

(3) Others to be noted

a,c

[redacted]

3.3 FPGA functions

Figure shows Functional Block Diagram of the SPTSEL1 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA.

a,c

[redacted]

Figure 2 Functional Block Diagram of SPTSEL1 module

Table 1 FPGA functions in the SPTSEL1 module

FPGA	Description

a,c

3.4 Self Diagnosis

The SPTSEL1 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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⓪ Feb.19, 2013	–	First Issue	K. Wakita Feb 19, 2013	K. Wakita Feb 19 2013	T. Toji Feb 18, 2013	T. Toji Feb. 19, 2013

MLTPL1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: MLTPL1 module

(2) Module Number: HNS1130

(3) Unit and application to be used: SPTM-S Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Two

2 Functional Summary

The MLTPL1 module collects eight suppression pool temperature data from eight AITRIP1 modules in the SPTM-S unit and multiplexes them as one transmission data frame and sends the data frame to the TRN module that transmits the data frame to the RCV module in SPTM unit.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the MLTPL1 module.

3.2 Input and Output

The MLTPL1 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication module

[ ]a,c

a,c

Figure 1 The front panel of the MLTPL1 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication module

a,c

(3) Others to be noted

a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the MLTPL1 module used for RTIS where each block is an FPGA if it is noted otherwise.

provides functions of each FPGA.

[ ] a,c

Figure 2 Functional Block Diagram of MLTPL1 module

Table 1 FPGA functions in the MLTPL1 module

FPGA	Description
[ ] a,c	

3.4 Self Diagnosis

The MLTPL1 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

[ ] a,c

3.4.2 Inoperable Trip

[ ] a,c

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⓪ Feb.19, 2013	–	First Issue	K. Wakita Feb.19.2013	K. Wakita Feb.19.2013	T. Toji Feb.18,2013	T. Toji Feb.19, 2013

DTUCA1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: DTUCA1 module

(2) Module Number: HNS1141

(3) Unit and application to be used: DTF-RPS Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Three

2 Functional Summary

The DTUCA1 module collects the trip states, present values and setpoint values of five analog trip parameters, and trip bypass states, present values and setpoint values of two trip bypass parameters from the AITRIP1 modules. The DTUCA1 module collects trip states of five discrete trip parameters and the trip test switch positions from the DIC1 module. The DTUCA1 module also receives trip states, present values and setpoints values of suppression pool temperature via the RCV module.

The DTUCA1 module determines the trip states of each trip function to be sent to external equipment, based on the trip states of individual trip parameters, trip bypass states of trip bypass parameters and trip test switch positions.

The DTUCA1 module sends the above mentioned trip states and other collected information to external equipment via the DOC1 and TRN modules.

The external equipment includes TLF-RPS units, TLF-MSIV units, other safety systems and non-safety systems.

3 Module Description

3.1 User Interfaces

Figure shows the front panel of the DTUCA1 module.

3.2 Input and Output

The DTUCA1 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules a,c

[redacted]

(2) Input signals via communication module

[a,c]

[a,c]

Figure 1 The front panel of the DTUCA1 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

[a,c]

(2) Output signals via communication module

[a,c]

(3) Others to be noted

[a,c]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the DTUCA1 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA.

Figure 2 Functional Block Diagram of DTUCA1 module

Table 1 FPGA functions in the DTUCA1 module

FPGA	Description

a,c

3.4 Self Diagnosis

The DTUCA1 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

[ ]a,c

3.4.2 Inoperable Trip

[ ]a,c

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0 Feb 18, 2013	–	First Issue	K. Wakita Feb 18,2013	K. Wakita Feb 18,2013	T. Joji Feb 18,2013	T. Joji Feb 19,2013
1 Mar. 11, 2013	1 2	Description was appropriately-modified. Descriptions of output signals were detailed to clarify.	K. Wakita Mar. 11, 2013	K. Wakita Mar. 11, 2013	T. Joji Mar. 8, 2013	N. Ito Mar. 11, 2013

DTUCA2 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: DTUCA2 module

(2) Module Number: HNS1142

(3) Unit and application to be used: DTF-MSIV Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Three

2 Functional Summary

The DTUCA2 module collects the trip states, present values and setpoint values of the eight analog trip parameters from AITRIP1 modules. The DTUCA2 module collects trip state of nine discrete trip parameters from the RCV module and the trip test switch positions from the DIC1 module.

The DTUCA2 module determines the trip states of each trip function to be sent to external equipment, based on the trip states of individual trip parameters and the trip test switch positions.

The DTUCA2 module sends the above mentioned trip states and other collected information to external equipment via the DOC1 and TRN modules.

The external equipment includes the TLF-MSIV units, other safety systems and non-safety systems.

3 Module Description

3.1 User Interfaces

Figure shows the front panel of the DTUCA2 module.

3.2 Input and Output

The DTUCA2 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication module a,c

[ ]

a,c

Figure 1 The front panel of the DTUCA2 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication module

a,c

in all divisions

(3) Others to be noted

a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the DTUCA2 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of DTUCA2 module

Table 1 FPGA functions in the DTUCA2 module

FPGA	Description

a,c

3.4 Self Diagnosis

The DTUCA2 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

[ ]

3.4.2 Inoperable Trip

a,c

[ ]

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⓪ Feb 18, 2013	–	First Issue	K. Wakita Feb 18,2013	K. Wakita Feb 18,2013	T. Joji Feb 18,2013	T. Joji Feb 19,2013
① Mar 11, 2013	1 2	Description was appropriately-modified. Description of output signals was detailed to clarify.	K. Wakita Mar. 11, 2013	K. Wakita Mar. 11, 2013	T. Joji Mar. 8, 2013	H. Ito Mar 11, 2013

TLUCA1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: TLUCA1 module

(2) Module Number: HNS1151

(3) Unit and application to be used: TLF-RPS Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: One

2 Functional Summary

The TLUCA1 module performs two out of four logic calculation to determine the divisional trip.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the TLUCA1 module.

3.2 Input and Output

The TLUCA1 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication module

[ ]a,c

[redacted] a,c

Figure 1 The front panel of the TLUCA1 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

[redacted] a,c

(2) Output signals via communication module

[redacted] a,c

(3) Others to be noted

[redacted] a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the TLUCA1 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA.

a,c

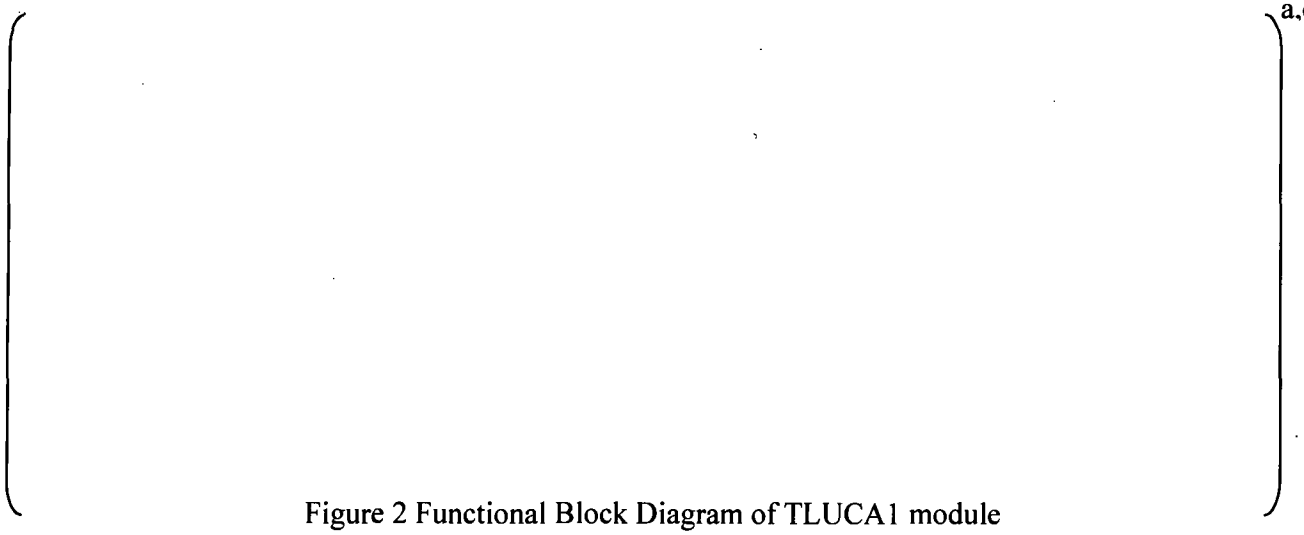

Figure 2 Functional Block Diagram of TLUCA1 module

Table 1 FPGA functions in the TLUCA1 module

a,c

FPGA	Description

3.4 Self Diagnosis

The TLUCA1 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

[ ]a,c

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⓪ Feb.19,2013	-	First issue	K. Ueki Feb.19.2013	K. Ueki Feb.19.2013	T. Joji Feb.18.2013	T. Joji Feb.19,2013

TLUCA2 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: TLUCA2 module

(2) Module Number: HNS1152

(3) Unit and application to be used: TLF-MSIV Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Two

2 Functional Summary

The TLUCA2 module performs two out of four logic calculation to determine the divisional trip.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the TLUCA2 module.

3.2 Input and Output

The TLUCA2 module has the following inputs and outputs.

3.2.1 Input Signals

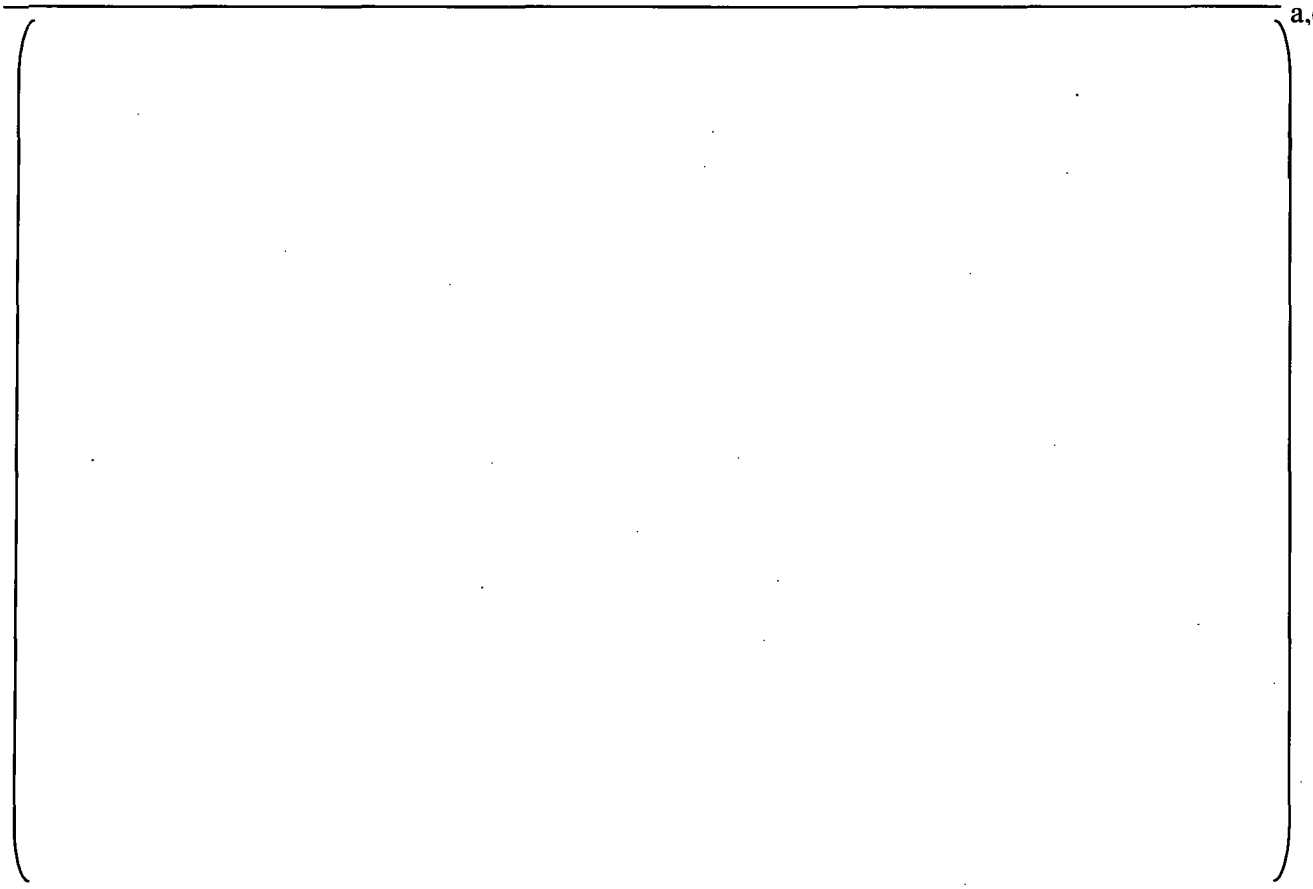
(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication module

[ ]a,c

[a,c



] a,c

Figure 1 The front panel of the TLUCA2 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

[a,c

] a,c

(2) Output signals via communication module

[a,c

] a,c

(3) Others to be noted

[a,c

] a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the TLUCA2 module used for RTIS where each block is an FPGA if it is not noted otherwise. Table 1 provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of TLUCA2 module

Table 1 FPGA functions in the TLUCA2 module

a,c

FPGA	Description

3.4 Self Diagnosis

The TLUCA2 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

[ ]a,c

3.4.2 Inoperable Trip

[ ]a,c

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⓪ Feb.19, 2013	–	First Issue	K.Wakita Feb.19, 2013	K.Wakita Feb.19, 2013	T.Joji Feb.18, 2013	T.Joji Feb.19, 2013

STR1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: STR1 module

(2) Module Number:

HNS1161, HNS1162, HNS1163, HNS1164, HNS1165, HNS1166, HNS1167

(3) Unit and application to be used

DTF-RPS, DTF-MSIV, DTF-MSIV-S, TLF-RPS, TLF-MSIV, SPTM, SPTM-S Units in RTIS for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The STR1 module receives discrete alarm signals from the LVPS modules and other modules in the same unit, and shows the alarm on the module front panel. The model number specifies the alarms corresponding to the location of modules in each unit.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the STR1 module.

3.2 Inputs and Outputs

The STR1 module has the following inputs and outputs.

3.2.1 Inputs

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication modules a,c

[ ]

(3) Others to be noted a,c

[ ]

3.2.2 Outputs a,c

[ ]

a,c

Figure 1 The front panel of the STR1 module (HNS1161)

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⓪ Feb 19, 2013	–	First Issue	K. Wakita Feb 19,2013	K. Wakita Feb 19,2013	T. Joji Feb 18,2013	T. Joji Feb 19,2013
① Mar. 11, 2013	2	Figure 1 was detailed to clarify.	K. Wakita Mar. 11. 2013	K. Wakita Mar. 11. 2013	T. Joji Mar. 8, 2013	H. Ito Mar. 11. 2013

MLTPL2 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name : MLTPL2 module

(2) Module Number: HNS1170

(3) Unit and application to be used: DTF-MSIV-S Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Two

2 Functional Summary

The MLTPL2 module collects nine main steam tunnel temperature data from nine AITRIP1 modules in the DTF-MSIV-S unit and multiplexes them as one transmission data frame and sends the data frame to the TRN module that transmits the data frame to the RCV module in the DTF-MSIV unit.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the MLTPL2 module.

3.2 Input and Output

The MLTPL2 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules a,c

[ ]

(2) Input signals via communication module a,c

[ ]

a,c

Figure 1 The front panel of the MLTPL2 module

3.2.2 Output Signals

(1) Output signals via process input and output modules a,c

(2) Output signals via communication module a,c

(3) Others to be noted a,c

3.3 FPGA functions

Figure shows Functional Block Diagram of the MLTPL2 module used for RTIS where each block is an FPGA if it is noted otherwise. Table provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of MLTPL2 module

Table 1 FPGA functions in the MLTPL2 module

a,c

FPGA	Description

3.4 Self Diagnosis

The MLTPL2 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

a,c

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⓪ Feb.19,2013	–	First Issue	K.Akikita Feb.19.2013	K.Akikita Feb.19.2013	T. Joji Feb.19, 2013	T. Joji Feb.19, 2013

TLUBF1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: TLUBF1 module

(2) Module Number: HNS1180

(3) Unit and application to be used: TLF-RPS Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: One

2 Functional Summary

The TLUBF1 module collects two out of four logic states from the TLUCA1 module and load driver status from the RCV module and transfers them to the TRN and DOC1 module to be sent to external equipment.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the TLUBF1 module.

3.2 Input and Output

The TLUBF1 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules

[ ]a,c

(2) Input signals via communication module

[ ]a,c

(3) Others to be noted

[ ]a,c

a,c

Figure 1 The front panel of the TLUBF1 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication module

a,c

(3) Others to be noted

a,c

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the TLUBF1 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA.

a,c

Figure 2 Functional Block Diagram of TLUBF1 module

Table 1 FPGA functions in the TLUBF1 module

a,c

FPGA	Description

3.4 Self Diagnosis

The TLUBF1 module generates the following self diagnosis signals.

3.4.1 Minor Failure Alarm

a,c

3.4.2 Inoperable Trip

[ ]a,c

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⓪ Feb 19, 2013	–	First Issue	K. Wakita Feb 19,2013	K. Wakita Feb 19,2013	T. Joji Feb 18,2013	T. Joji Feb 19,2013
① Mar. 11, 2013	2	Description of output signals was appropriately modified.	K. Wakita Mar. 11, 2013	K. Wakita Mar. 11, 2013	T. Joji Mar. 8, 2013	M. Ito Mar. 11, 2013

LOM2_1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LOM2_1 module

(2) Module Number: HNS1201

(3) Unit and application to be used: OLU-MSIV Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Five

2 Functional Summary

The LOM2_1 module receives trip output from TLF-MSIV unit. The LOM2_1 module collects switch positions that include LD testing, TLF bypass, trip reset etc. from LLN1 module. The LOM2_1 module determines the output state of the trip signal for the load drivers (LDs) by ROM Logic, using LUT (Look-up-table), based on the collected data mentioned above. The LOM2_1 outputs the determined trip signal to the LD units, and the OLU-MSIV units in other divisions via LOI1 modules. The LOM2_1 module receives trip outputs from the OLU-MSIV units in other divisions via the LOI1 module. The LOM2_1 module also outputs the determined trip state and manual trip state to external equipment via LHO1 module. The LOM2_1 module sends the status of the modules in the OLU-MSIV and the LD units to the TLF-MSIV unit.

Note: ROM Logic means the logic using the LUT stored in the ROM.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the LOM2_1 module.

3.2 Input and Output

The LOM2_1 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules

a,c

[redacted]

(2) Input signals via communication module

a,c

[redacted]

a,c

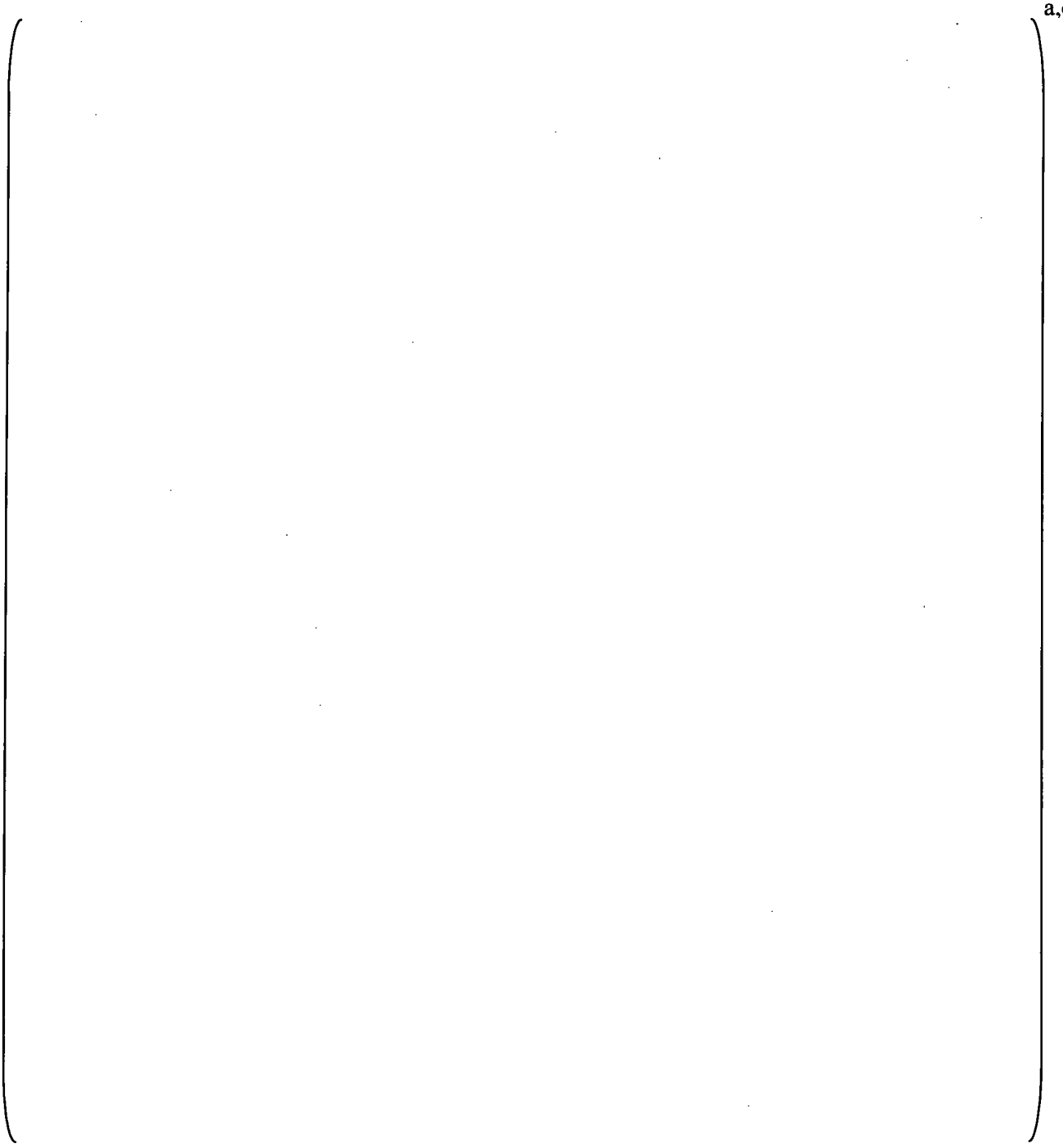

Figure 1 The front panel of the LOM2_1 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication module

a,c

[

]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the LOM2_1 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA. The only difference between LOM2_1 module and LOM2_2 is ROM Logic mounted on the sub board 1. Same main board, same FPGAs and same sub board 2 are commonly used in LOM2_1 module and LOM2_2 module.

a,c

(

)

Figure 2 Functional Block Diagram of LOM2_1 module

Table 1 FPGA functions in the LOM2_1 module

FPGA	Description

a,c

3.4 Self Diagnosis

The LOM2_1 module generates the following self diagnosis signals.

3.4.1 Error indication

a,c

3.4.2 Errors with fail safe action

a,c

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⓪ Feb 18, 2013	–	First Issue	K. Wakita Feb 18,2013	K. Wakita Feb 18,2013	T. Joji Feb 18,2013	T. Joji Feb 18,2013
① Mar. 11, 2013	1	Editorial error correction.	K. Wakita Mar. 11, 2013	K. Wakita Mar. 11, 2013	T. Joji Mar. 8, 2013	Mar. 11, 2013

LOM2_2 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LOM2_2 module

(2) Module Number: HNS1202

(3) Unit and application to be used: OLU-RPS Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Five

2 Functional Summary

The LOM2_2 module receives trip output from TLF-RPS unit. The LOM2_2 module collects switch positions that include manual scram, scram reset, TLF bypass and parallel LD test from the LLN1 module. The LOM2_2 module also collects reset permissive discrete signal from LHI1 module. The LOM2_2 module determines the output state of the trip signal for the load drivers (LDs) by ROM Logic, using LUT (Look-up-table), based on the collected data mentioned above. The LOM2_2 outputs the determined trip signal to the LD units via LOI1 modules and to scram backup circuit via LHO1 module. The LOM2_2 module also outputs the determined trip state and manual scram state to external equipment via the LHO1 module. The LOM2_2 module sends the status of the modules in the OLU-RPS and the LD units to the TLF-RPS unit.

Note: ROM Logic means the logic using the LUT stored in the ROM.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the LOM2_2 module**Figure** .

3.2 Input and Output

The LOM2_2 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules

a,c

[ ]

(2) Input signals via communication module

a,c

[2]

a,c

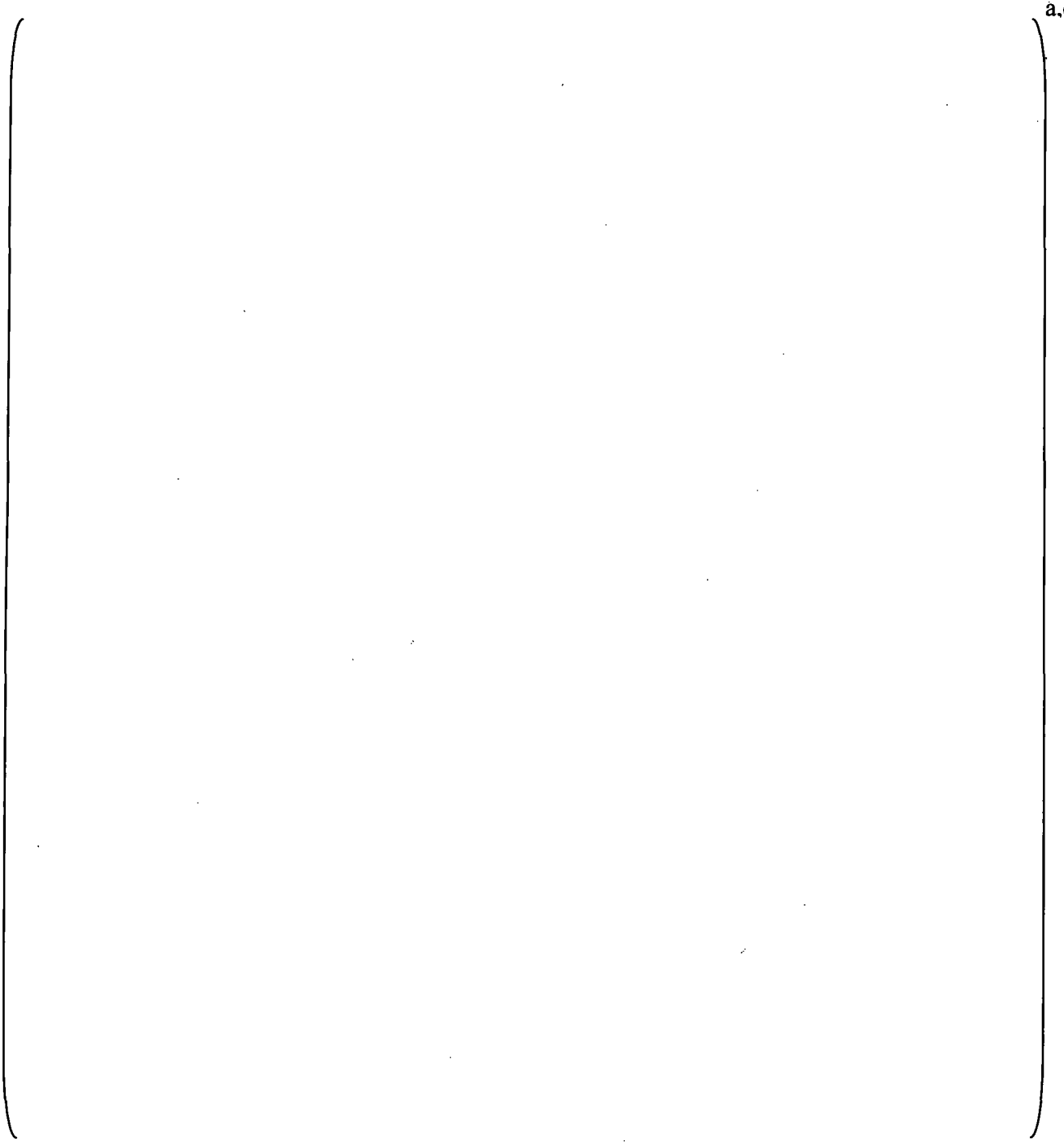

Figure 1 The front panel of the LOM2_2 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication module a,c

[ ]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the LOM2_2 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA. The only difference between LOM2_1 module and LOM2_2 is ROM Logic mounted on the sub board 1. Same main board, same FPGAs and same sub board 2 are commonly used in LOM2_1 module and LOM2_2 module.

( ) a,c

Figure 2 Functional Block Diagram of LOM2_2 module

Table 1 FPGA functions in the LOM2_2 module

FPGA	Description

a,c

3.4 Self Diagnosis

The LOM2_2 module generates the following self diagnosis signals.

3.4.1 Error indication

a,c

3.4.2 Errors with fail safe action

a,c

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① Mar. 11, 2013	1	Editorial error correction.	K. Wakita Mar. 11, 2013	K. Wakita Mar. 11, 2013	T. Joji Mar. 8, 2013	H. Ito Mar. 11, 2013

LOM2_1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LOM2_1 module

(2) Module Number: HNS1203

(3) Unit and application to be used: OLU-MSIV Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Five

2 Functional Summary

The LOM2_1 module receives trip output from TLF-MSIV unit. The LOM2_1 module collects switch positions that include LD testing, TLF bypass, trip reset etc. from the LLN1 module. The LOM2_1 module determines the output state of the trip signal for the load drivers (LDs) by ROM Logic, using LUT (Look-up-table), based on the collected data mentioned above. The LOM2_1 outputs the determined trip signal to the LD units, and the OLU-MSIV units in other divisions via LOI1 modules. The LOM2_1 module receives trip outputs from the OLU-MSIV units in other divisions via the LOI1 module. The LOM2_1 module also outputs the determined trip state and manual trip state to external equipment via LHO1 module. The LOM2_1 module sends the status of the modules in the OLU-MSIV and the LD units to the TLF-MSIV unit.

Note: ROM Logic means the logic using the LUT stored in the ROM.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the LOM2_1 module.

3.2 Input and Output

The LOM2_1 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules

a,c

[ ]

a,c

(2) Input signals via communication module

[ ]

a,c

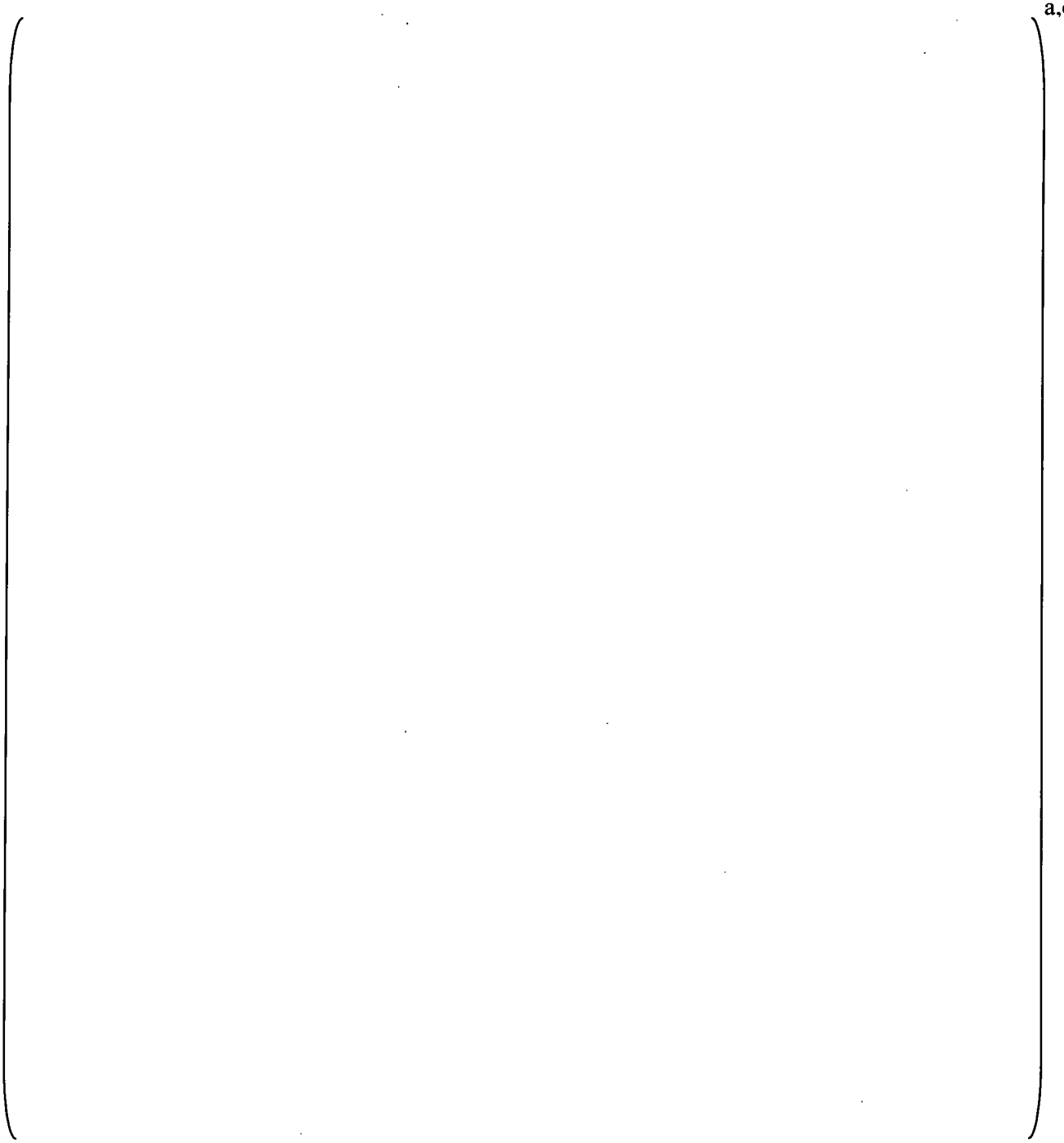

Figure 1 The front panel of the LOM2_1 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication module a,c

[ ]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the LOM2_1 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA. The only difference between LOM2_1 module and LOM2_2 is ROM Logic mounted on the sub board 1. Same main board, same FPGAs and same sub board 2 are commonly used in LOM2_1 module and LOM2_2 module. a,c

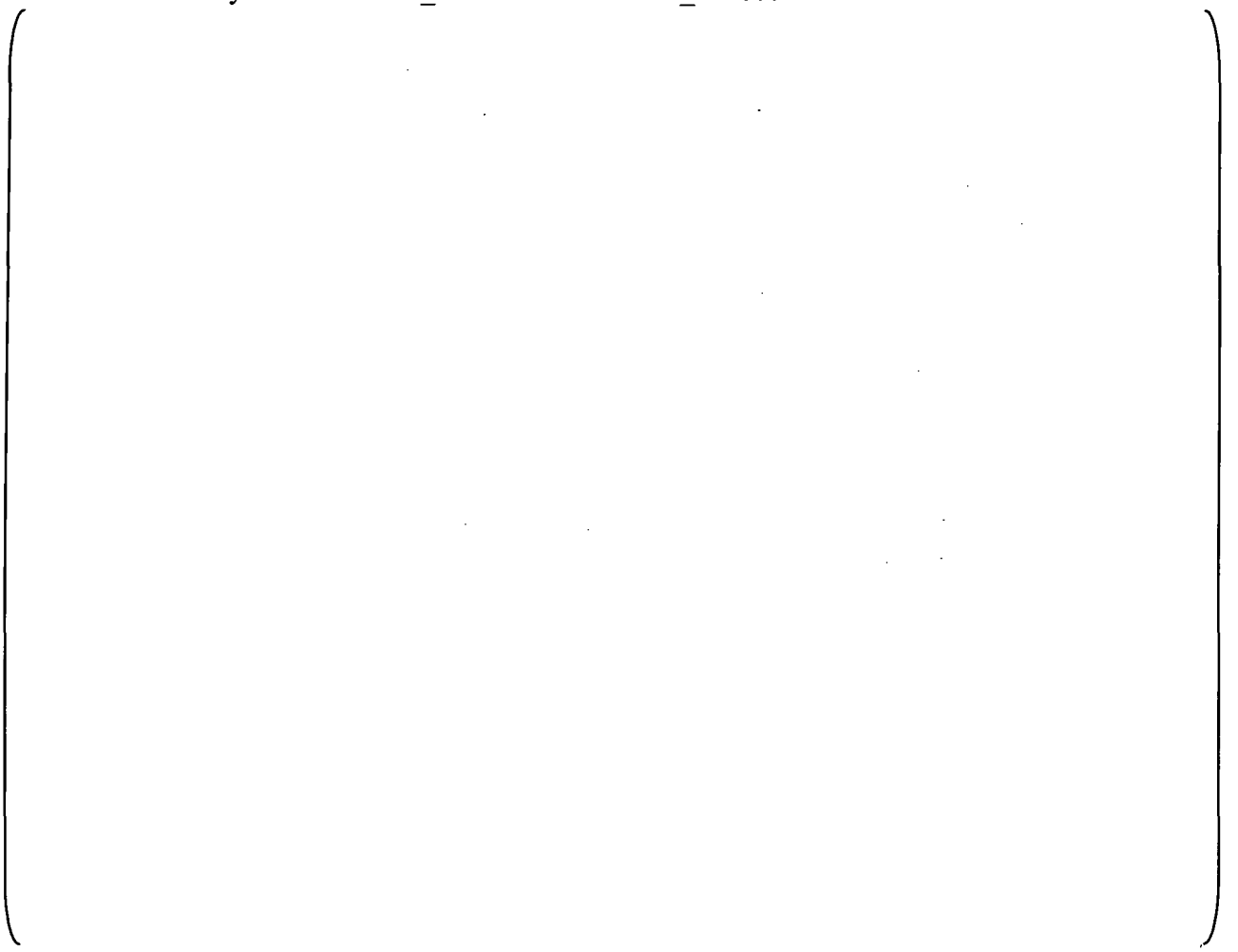

Figure 2 Functional Block Diagram of LOM2_1 module

Table 1 FPGA functions in the LOM2_1 module

FPGA	Description

a,c

3.4 Self Diagnosis

The LOM2_1 module generates the following self diagnosis signals.

3.4.1 Error indication

a,c

3.4.2 Errors with fail safe action

a,c

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① Mar. 11, 2013	1	Editorial error correction.	K. Wakita Mar. 11, 2013	K. Wakita Mar. 11, 2013	T. Joji Mar. 8, 2013	[illegible] Mar. 11, 2013

LOM2_2 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LOM2_2 module

(2) Module Number: HNS1204

(3) Unit and application to be used: OLU-RPS Unit in RTIS for ABWR Application

(4) Number of FPGA on the Module: Five

2 Functional Summary

The LOM2_2 module receives trip output from TLF-RPS unit. The LOM2_2 module collects switch positions that include manual scram, scram reset, TLF bypass and parallel LD test from the LLN1 module. The LOM2_2 module also collects reset permissive discrete signal from LHI1 module. The LOM2_2 module determines the output state of the trip signal for the load drivers (LDs) by ROM Logic, using LUT (Look-up-table), based on the collected data mentioned above. The LOM2_2 outputs the determined trip signal to the LD units via LOI1 modules and to scram backup circuit via LHO1 module. The LOM2_2 module also outputs the determined trip state and manual scram state to external equipment via the LHO1 module. The LOM2_2 module sends the status of the modules in the OLU-RPS and the LD units to the TLF-RPS unit.

Note: ROM Logic means the logic using the LUT stored in the ROM.

3 Module Description

3.1 User Interfaces

Figure 1 shows the front panel of the LOM2_2 module.

3.2 Input and Output

The LOM2_2 module has the following inputs and outputs.

3.2.1 Input Signals

(1) Input signals via process input and output modules

a,c

[ ]

a,c

(2) Input signals via communication module

[ ]

a,c

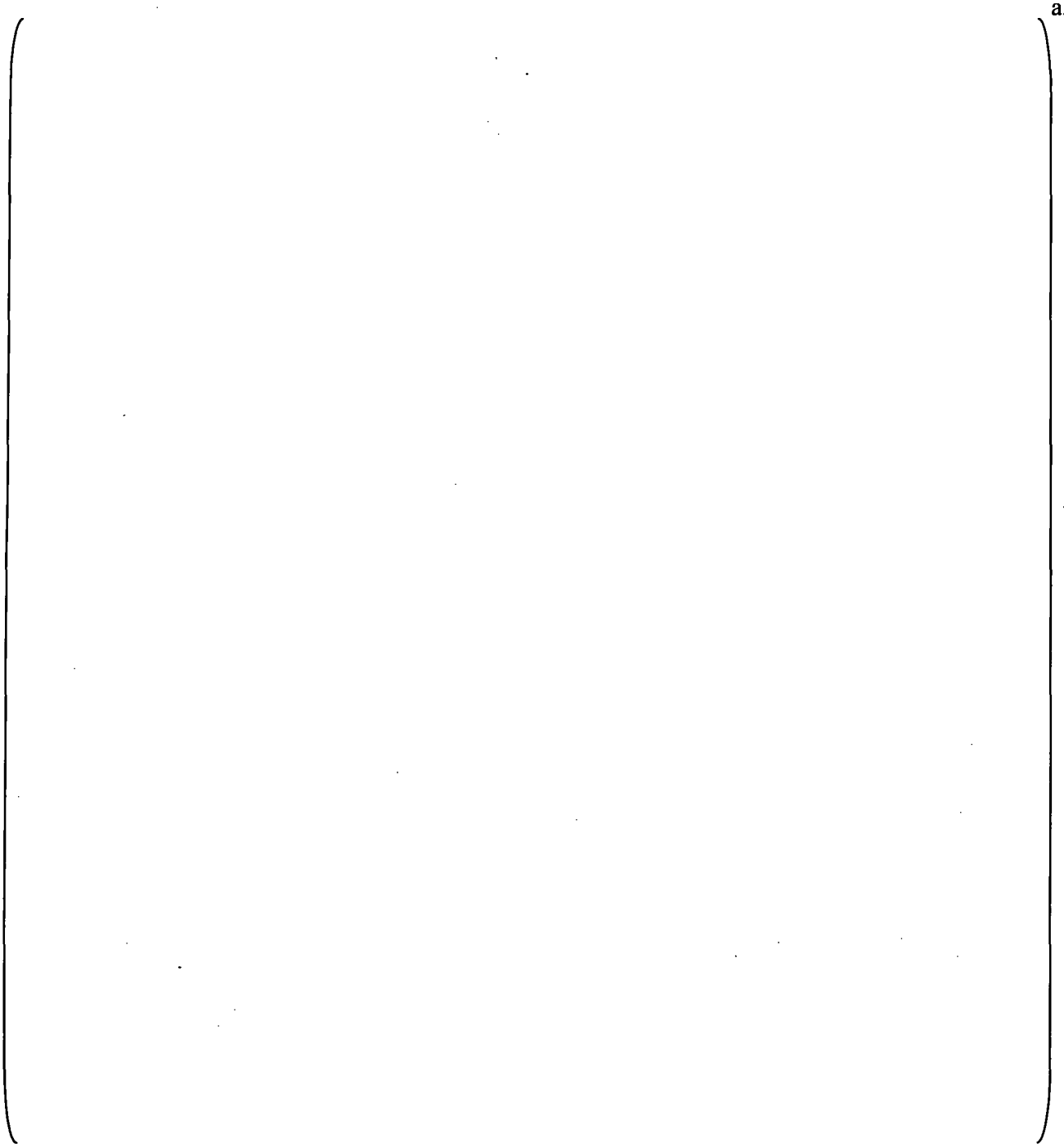

Figure 1 The front panel of the LOM2_2 module

3.2.2 Output Signals

(1) Output signals via process input and output modules

a,c

(2) Output signals via communication module a,c

[ ]

3.3 FPGA functions

Figure 2 shows Functional Block Diagram of the LOM2_2 module used for RTIS where each block is an FPGA if it is not noted otherwise.

provides functions of each FPGA. The only difference between LOM2_1 module and LOM2_2 is ROM Logic mounted on the sub board 1. Same main board, same FPGAs and same sub board 2 are commonly used in LOM2_1 module and LOM2_2 module.

Figure 2 Functional Block Diagram of LOM2_2 module

Table 1 FPGA functions in the LOM2_2 module

FPGA	Description

a,c

3.4 Self Diagnosis

The LOM2_2 module generates the following self diagnosis signals.

3.4.1 Error indication

a,c

3.4.2 Errors with fail safe action

a,c

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① Mar. 11, 2013	1	Editorial error correction.	K.Wakita Mar.11.2013	K.Wakita Mar. 11. 2013	T. Joji Mar. 8, 2013	H. Ito Mar. 11. 2013

DIC1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: DIC1 module

(2) Module Number: HNS0730

(3) Unit and application to be used

DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV Units in RTIS for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The DIC1 module provides for sampling sixteen discrete inputs from external equipment. The received signals are sent to other modules in the same unit through the backplane (which Toshiba refers to as a middle plane) on copper point-to-point discrete wiring.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the DIC1 module.

3.2 Inputs and Outputs

The DIC1 module has the following inputs and outputs.

3.2.1 Inputs

a,c

3.2.2 Outputs

a,c

a,c

Figure 1 The front panel of the DIC1 module

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⓪ Feb. 18 2013	–	First Issue	K. Wakita Feb. 18. 2013	K. Wakita Feb. 18, 2013	T. Joji Feb. 18, 2013	T. Joji Feb. 18, 2013

DOC1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: DOC1 module

(2) Module Number: HNS0740

(3) Unit and application to be used
DTF-RPS, DTF-MSIV, TLF-RPS, TLF-MSIV, SPTM Units in RTIS for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The DOC1 module provides sixteen discrete outputs to external equipment. The output signals are provided from other modules in the same unit through the backplane (which Toshiba refers to as a middle plane) on copper point-to-point discrete wiring.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the DOC1 module.

3.2 Inputs and Outputs

The DOC1 module has the following inputs and outputs.

3.2.1 Inputs

a,c

( )

3.2.2 Outputs

a,c

( )

a,c

( )

Figure 1 The front panel of the DOC1 module

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⓪ Feb.19, 2013	–	First Issue	K.Wakita Feb.19.2013	K.Wakita Feb.19.2013	T.Joji Feb.18,2013	T.Joji Feb.18,2013

LOI1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LOI1 module

(2) Module Number: HNS1211, HNS1212

(3) Unit and application to be used
OLU-RPS, OLU-MSIV Units in RTIS for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The LOI module is a fiber optical interface which connects the OLU unit and load driver (LD) units, or connects the OLU-MSIV units in different divisions.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the LOI1 module.

3.2 Inputs and Outputs

The LOI1 module has the following inputs and outputs.

3.2.1 Inputs

a,c

[ ]

3.2.2 Outputs

a,c

[ ]

a,c

Figure 1 The front panel of the LOI1 module (HNS1211)

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⓪ Feb.19, 2013	–	First Issue	K. Wakita Feb.19.2013	K. Wakita Feb.19.2013	T. Joji Feb.18.2013	T. Joji Feb.19, 2013

LLN1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LLN1 module

(2) Module Number: HNS1220

(3) Unit and application to be used
OLU-RPS, OLU-MSIV Units in RTIS for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The LLN1 module provides for sampling 32 discrete inputs from external equipment. The received signals are sent to the LOM2 module in the same unit through the backplane on copper point-to-point discrete wiring.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the LLN1 module.

3.2 Inputs and Outputs

The LLN1 module has the following inputs and outputs.

3.2.1 Inputs

[-] a,c

3.2.2 Outputs

[ ] a,c

[ ] a,c

Figure 1 The front panel of the LLN1 module

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⓪ Feb 19, 2013	–	First Issue	K. Wakita Feb 19,2013	K. Wakita Feb 19,2013	T. Joji Feb 18,2013	T. Joji Feb 19,2013
① Mar. 11, 2013	1	Editorial error correction.	K. Wakita Mar. 11. 2013	K. Wakita March. 2013	T. Joji Mar. 8, 2013	M. Ito Mar. 11, 2013

LHI1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LHI1 module

(2) Module Number: HNS1230

Unit and application to be used: OLU-RPS Unit in RTIS for ABWR Application

(3) Number of FPGA on the module: None

2 Functional Summary

The LHI1 module provides for sampling eight discrete inputs from external equipment. The received signals are sent to the LOM2 module in the same unit through the backplane on copper point-to-point discrete wiring.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the LHI1 module.

3.2 Inputs and Outputs

The LHI1 module has the following inputs and outputs.

3.2.1 Inputs

a,c

[ ]

3.2.2 Outputs

a,c

[ ]

a,c

[ ]

Figure 1 The front panel of the LHI1 module

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⓪ Feb. 19, 2013	–	First issue	K. Wakita Feb. 19, 2013	K. Wakita Feb 19, 2013	T. Joji Feb 18, 2013	T. Joji Feb 19, 2013

LHO1 Module Summary Description

1 Introduction

This document provides the module description for the following module.

(1) Module Name: LHO1 module

(2) Module Number: HNS1240

(3) Unit and application to be used
OLU-RPS, OLU-MSIV Units in RTIS for ABWR Application

(4) Number of FPGA on the module: None

2 Functional Summary

The LHO1 module provides eight discrete outputs to external equipment. The output signals are provided from the LOM2 module in the same unit through the backplane on copper point-to-point discrete wiring.

3 Module Description

3.1 Module Front Panel

Figure 1 shows the front panel of the LHO1 module.

3.2 Inputs and Outputs

The LHO1 module has the following inputs and outputs.

3.2.1 Inputs

a,c

3.2.2 Outputs

a,c

a,c

Figure 1 The front panel of the LHO1 module

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