5.0 ACCEPTANCE CRITERIA

The acceptance criteria for the operability tests are defined by EPRI TR-107330 and also based on the HFC specifications for the HFC-6000 product line. A preliminary set of results obtained during the prequalification phase of testing will establish baseline performance characteristics for the Test Specimen and TSAP. Subsequent performance of the operability tests during the qualification tests will disclose any deterioration from the baseline performance caused by the environmental stress conditions. The followings describe the specific acceptance criteria for individual tests.

5.1 ACCURACY TEST ACCEPTANCE CRITERIA

4- to 20-mA AI Channels

HFC Design Specification	15 bit AI image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.35% of span over the entire range.

4- to 20-mA AO Channels

HFC Design Specification	12 bit AO image Accuracy within ±0.1% of span over the entire range
During qualification test	Accuracy within ±0.32% of span over the entire range.

100-ohm RTD Input Channels

HFC Design Specification	15 bit AI image 0 deg to 700 deg C design operating range Accuracy within ±0.1% of range over the entire range
During qualification test	Accuracy within ±2 deg C (3.6 deg F) over entire range

Type E Thermocouple Input Channels

HFC Design Specification	15 bit AI image -50 deg to 600 deg C design operating range Accuracy within ±0.1% of range over the entire range
During qualification test	Accuracy within ±3 deg C (5.4 deg F) over entire range

Pulse Input Channels, AI4K

Rate Mode	12-bit count value image within 1 bit accuracy 512 Hz minimum input pulse rate (12-bit image)
Accumulate mode	24-bit count image within 1 bit accuracy
During qualification test	Accuracy within 1 bit

Pulse Input Channels, AI4K2

Pulse Measurement	4-byte count image within ± 1ms (1000 count) accuracy
During qualification test	Accuracy within ± 1ms (1000 count) accuracy

5.2 RESPONSE TIME ACCEPTANCE CRITERIA

a. Response time from activation of the trip condition to output of the trip signal for digital signal shall be less than 100ms and for analog signal shall be less than 300ms.

b. The measured response time shall not vary by more than ±10% from measured baseline value.

5.3 DISCRETE INPUT/OUTPUT OPERABILITY ACCEPTANCE CRITERIA

Discrete Input Operability

DI set voltage level	Guaranteed DI set level is 12 to 15 v at 25 deg C
DI dropout voltage	Guaranteed DI dropout level is 12 to 15 v at 25 deg C
Maximum input voltage	Maximum input voltage is 53 v at 25 deg C

Discrete Output Operability

Relay DO channels	5 A at 30 v for resistive load
Solid State DO Channels	Correct digital output state
120 vac output channels	90 to 130 vac at 47 to 63 Hz minimum range 2 A minimum in-rush capacity Up to 0.5 A steady state current 2 vac maximum on state voltage drop at 0.5 A Supplies off state leakage current for coil continuity monitoring function without energizing the relay.
125 vdc output channels	90 to 140 vdc 2 A minimum in-rush capacity Up to 0.5 A steady state current 2 vdc maximum on state voltage drop at 0.5 A Supplies off state leakage current for coil continuity monitoring function without energizing relay.

5.4 COMMUNICATION OPERABILITY ACCEPTANCE CRITERIA

C-Link Overall system operation continues in the presence of noise interference.

ICL I/O scanning continues in the presence of noise interference.

5.5 TIMER TEST ACCEPTANCE CRITERIA

Timer accuracy shall vary by no more than ±1% of preset value or ±3 scan cycles.

5.6 FAILOVER TEST ACCEPTANCE CRITERIA

(EPRI TR 107330 4.3.4.7 A & D)

a. Transfer to secondary controller shall trigger an alarm.

b. Secondary controller shall continue to run in normal operation mode.

c. The transfer shall ensure the followings:

   i. Shall occur with 200 ms (2 main processor scan cycle times)

   ii. Shall not cause I/O modules to have more than an 0.5% transient shift in the final output signal

   iii. Shall not cause a change in the I/O signal that persists for more than 5 ms for DC signals or 1 cycle for AC signals.

   iv. Shall not cause pulse input modules to lose signal.

   v. Shall not cause digital I/O to change state for more than 2 ms, and analog I/O signals to change by more than 5%.

5.7 POWER QUALITY ACCEPTANCE CRITERIA

Loss of Power Test

All output channels return to the deenergized state on loss of power.

All output channels remain in a failsafe state defined for the control circuit until the operator initiates operation.

Power Interruption Test

None of the processors reset

No static DO channels change state

None of the static AO channels change their output signal by more than 5%.

Logged parameters of all automated tests remain within tolerance.

Power Quality Tolerance Test

While source power is between 90 to 150 vac and 57 to 63 Hz, the output voltage level produced by the power supply remains within ±1% of its setpoint level.

No power supply dropout alarm occurs while source power is within the above specified range.

Undervoltage protection trips the power supply output; the power supply produces a system status alarm.

Overvoltage protection trips the power supply output; the power supply produces a system status alarm.

The power supply recovers from overvoltage and undervoltage conditions automatically.

5.8 FAILURE TO COMPLETE SCAN TEST ACCEPTANCE CRITERIA

a. When an input triggers a logic which execution time is over 100ms, the system fails over from the main controller to the secondary controller. And the system continues to operate.
b. The failover event is logged.
c. A power reset will bring the system back to redundant configuration.
d. SOE log indicates the failure to complete scan detected within 200 ± 100ms.

6.0 QA RECORDS

All data generated by execution of the tests covered by this procedure will become QA records. [Test data generated during manual execution of the Operability tests will be recorded on the appended Test Data Record sheets. Results for the automated portions of the Operability tests will be recorded in a set of SOE and HAS report files. All test data records during the qualification phase of testing will be filed in accordance with the QPP 17.1, "Quality Records".

7.0 ATTACHEMENTS

Attachment 7.1 – Test Equipment Log
Attachment 7.2 – 4- to 20- mA AI Channel Accuracy Test Record
Attachment 7.3 – 4- to 20- mA AO Channel Accuracy Test Record
Attachment 7.4 – Type E Thermocouple Card Accuracy Test Record
Attachment 7.5 – Type 100 ohm Card Accuracy Test Record
Attachment 7.6 – Pulse Input Card AI4K Accuracy Test Record
Attachment 7.7 – Pulse Input Card AI4K Test Record During Qualification Test
Attachment 7.8 – Response Time Test Record
Attachment 7.9 – Discrete Input Operability Test Record
Attachment 7.10 – Discrete Output Operability Test Record
Attachment 7.11 – Communication, Timer, Failover Test Record
Attachment 7.12 – Power Quality Test Record
Attachment 7.13 – SOE and HAS Test Records

Attachment 7.1 – Test Equipment Log

Test Equipment	Instrument ID	Calibration Due Date

Test Reviewer/Date

Attachment 7.2 – 4- to 20-mA AI Channel Accuracy Test Record

Card Type_____

HPAT Test Signal	HPAT AO Image (Count Value)	AO Test Signal (mA)	TSAP AI Image (Count Value)
10%			
30%			
50%			
70%			
90%			

Card Type_____

HPAT Test Signal	HPAT AO Image (Count Value)	AO Test Signal (mA)	TSAP AI Image (Count Value)
10%			
30%			
50%			
70%			
90%			

_____

Test Reviewer/Date

Attachment 7.2 4- to 20-mA AI Channel Accuracy Test Record (Continued)

Card Type_____

HPAT Test Signal	HPAT AO Image (Count Value)	AO Test Signal (mA)	TSAP AI Image (Count Value)
10%			
30%			
50%			
70%			
90%			

_____

Test Reviewer/Date

Attachment 7.3 – 4- to 20-mA AO Channel Accuracy Test Record

Card Type_____

TSAP Test Signal	TSAP AO Image (Count Value)	TSAP AO signal (mA)	HPAT AI Image (Count Value)
10%			
30%			
50%			
70%			
90%			

Card Type_____

TSAP Test Signal	TSAP AO Image (Count Value)	TSAP AO signal (mA)	HPAT AI Image (Count Value)
10%			
30%			
50%			
70%			
90%			

_____

Test Reviewer/Date

Attachment 7.4 – Type E Thermocouple Card Accuracy Test Record

Card Type HFC-AI8L

Input (deg C)	Expected Count	AI Image			
		CH1	CH2	CH3	CH4
0.0	2521 ($09D9_H$)				
130.0	9074 (2372_H)				
260.0	15627 ($3D0B_H$)				
390.0	22181 ($56A5_H$)				
520.0	28734 ($703E_H$)				

Input (deg C)	Expected Count	AI Image			
		CH5	CH6	CH7	CH8
0.0	2521 ($09D9_H$)				
130.0	9074 (2372_H)				
260.0	15627 ($3D0B_H$)				
390.0	22181 ($56A5_H$)				
520.0	28734 ($703E_H$)				

Test Engineer _____ **Date** _____

Attachment 7.5 – Type 100 Ohm RTD Card Accuracy Test Record

Card Type HFC-AI8M

120 ohm resister input image			
CH1 _____	CH2 _____	CH3 _____	CH4 _____
CH5 _____	CH6 _____	CH7 _____	CH8 _____

Input (ohm)	**Expected Count**	**AI Image**			
		CH1	**CH2**	**CH3**	**CH4**
100	0				
166.62	8192				
229.72	16384				
289.27	24574				
345.28	32767				

Input (ohm)	**Expected Count**	**AI Image**			
		CH5	**CH6**	**CH7**	**CH8**
100	0				
166.62	8192				
229.72	16384				
289.27	24574				
345.28	32767				

Test Engineer _____ **Date** _____

Attachment 7.6 – Pulse Input Card Accuracy Test Record

Card Type: AI4K

General Performance Parameters

Minimum input pulse amplitude _____
Maximum input pulse amplitude measured _____
Minimum input pulse width _____
Maximum input pulse duty cycle _____
Rate mode minimum input frequency _____ (12-bit mode)
Accumulate maximum count (24-bits) _____

Rate Mode

Input Signal		Indicated Rate
Nominal	Measured Frequency	Channel 1 (12-bit)
50 Hz		
600 Hz		
5 kHz		
10 kHz		
15 kHz		
19.5 kHz		

Accumulate Mode (300-second time interval)

Input Signal		Accumulated Count over 300 Seconds
Nominal	Measured Frequency	Channel 3(prescaler value = 10)
50 Hz		Starting Count _____ Final Count _____
5 kHz		Starting Count _____ Final Count _____
10 kHz		Starting Count _____ Final Count _____
15 kHz		Starting Count _____ Final Count _____
19.5 kHz		Starting Count _____ Final Count _____

Pulse Input Card Accuracy, HFC-AI4K2

Acquired pulse width count

Frequency\Channel	Ch0	Ch2
22.12 Hz		
10.00 Hz		
4.90 Hz		

Test Engineer _____ **Date** _____

Attachment 7.7 – Pulse Card Test Record During Qualification Tests

Cart Type: AI4K

Input Signal			
Nominal	**Measured Frequency**	**Channel 1 (Rate Mode)**	**Channel 3 (Accumulate mode)**
1 kHz		Resolution _____ Indicated Rate _____	Prescaler Value _____ Time Period 60 seconds Starting Count _____ Final Count _____

Cart Type: AI4K2

Input Frequency	**Channel 0 Count**	**Channel 2 Count**
10.0 Hz		

Test Engineer _____ **Date** _____

Attachment 7.8 – Response Time Test Record

Analog Response Time	**Measurement**		
	1	**2**	**3**
Leading edge transfer delay	_____	_____	_____
Trailing edge transfer delay	_____	_____	_____
SOE Report Files	_____	_____	_____
	4	**5**	**6**
Leading edge transfer delay	_____	_____	_____
Trailing edge transfer delay	_____	_____	_____
SOE Report Files	_____	_____	_____

Digital Response Time	**Measurement**		
	1	**2**	**3**
TRUE period of 1,DO,668	_____	_____	_____
FALSE period of 1,DO,668	_____	_____	_____
Leading edge response time	_____	_____	_____
Trailing edge response time	_____	_____	_____
SOE Report Files	_____	_____	_____

Test Engineer _____ **Date** _____

Attachment 7.9 – Discrete Input Operability Test Record

Card Type Under Test __DI16I_			
Input Channel Rating _____			
Set Voltage Threshold (3 cycles minimum)	_____	_____	_____
Maximum Input Voltage (3 cycles minimum)	_____	_____	_____
Dropout Voltage (3 cycles minimum)	_____	_____	_____
Card Type Under Test __DC33_			
Input Channel Rating _____			
Set Voltage Threshold (3 cycles minimum)	_____	_____	_____
Maximum Input Voltage (3 cycles minimum)	_____	_____	_____
Dropout Voltage (3 cycles minimum)	_____	_____	_____
Card Type Under Test __DC34_			
Input Channel Rating _____			
Set Voltage Threshold (3 cycles minimum)	_____	_____	_____
Maximum Input Voltage (3 cycles minimum)	_____	_____	_____
Dropout Voltage (3 cycles minimum)	_____	_____	_____
Card Type Under Test __DC35_			
Input Channel Rating _____			
Set Voltage Threshold (3 cycles minimum)	_____	_____	_____
Maximum Input Voltage (3 cycles minimum)	_____	_____	_____
Dropout Voltage (3 cycles minimum)	_____	_____	_____

Test Engineer _____ **Date** _____

Attachment 7.10 – Discrete Output Operability Test Record

Card Type Under Test: HFC-DO8J Contact Resistance (Average of 8 channels) _____ Test Load Applied _____ Each Channel Switches Under Load _____
Card Type Under Test: HFC-DO16J Contact Resistance (Average of 16 channels) _____ Test Load Applied _____ Each Channel Switches Under Load _____
Card Type Under Test: HFC-DO16C DO Status "ON" verified _____ DO Status "OFF" verified _____

Test Engineer _____ **Date** _____

Attachment 7.10 Discrete Output Operability Test Record (Continued)

Card Type Under Test: HFC-DC33

Solenoid Coil Resistance Set Coil_____ Reset Coil_____
90.0 ± 0.5 vac, 47 Hz responses Peak off-on response _____
Steady-state output _____
Peak reverse EMF _____
Off-state leakage _____
130.0 ± 0.5 vac, 63 Hz responses Peak off-on response _____
Steady-state output _____
Peak reverse EMF _____
Off-state leakage _____

Card Type Under Test: HFC-DC34

Solenoid Coil Resistance Set Coil_____ Reset Coil_____
90.0 ± 0.5 vdc responses Peak off-on response _____
Steady-state output _____
Peak reverse EMF _____
Off-state leakage _____

140.0 ± 0.5 vdc responses Peak off-on response _____
Steady-state output _____
Peak reverse EMF _____
Off-state leakage _____

Card Type Under Test: HFC-DC35

Solenoid Coil Resistance Set Coil_____
90.0 ± 0.5 vac responses Peak off-on response _____
Steady-state output _____
Peak reverse EMF _____
Off-state leakage _____

130.0 ± 0.5 vac responses Peak off-on response _____
Steady-state output _____
Peak reverse EMF _____
Off-state leakage _____

CR10 is energized by setting 1,DO,1041 to TRUE. _____

CR10 is denergized by setting 1,DO,1041 to FALSE. _____

Test Engineer _____ **Date** _____

Attachment 7.11 – Communication, Timer, Failover Test Record

Communication Operability Test

(Append Memory Editor screen captures)

ICL Errors	
Error count at start	
Final error count	
Duration of test	

(Append Database Editor screen captures)

C-Link Errors			
Channel 0 (1,CO,10)		Channel 1 (1,CO,11)	
Error count at start		Error count at start	
Final error count		Final error count	
Duration of test		Duration of test	

Timer Operability Test

Timer	Average Over 10 Periods Minimum	
	Period	Jitter
1 Sec		
5 Sec		

Failover Operability Test

Processor Cycle Time Measurement

1,CO,50 value at start of interval _____

1,CO,50 value at end of interval _____

Total period of measurement _____

Average processor cycle time _____

Failover Transfer Time Measurement

Delay from trailing edge of SANE_A/ to leading edge of PRI_B/ _____

Analog Loop Disruption

Magnitude of disruption for stable analog values _____

PV Settling time for 20% increase in SP value without failover _____

PV Settling time for 20% increase in SP value with failover _____

Magnitude of disruption for analog values in transition _____

Digital Loop Disruption

Duration of disruption for stable DI and DO channels _____

Duration of disruption for DI and DO channels in transition _____

Test Engineer _____ **Date** _____

Attachment 7.12 – Power Quality Test Record

Power Loss Test

On loss of power:

All AO channels are open (0 mA output signal.) _____

All power (120 vac and 125 vdc) output channels are open. _____

All solid state relay DO channels are open (no continuity) _____

All mechanical relay DO channels are deenergized (NO contacts open, NC contacts closed) _____

On restoration of power:

All output channels remain disabled while powerup initialization remains in progress. _____

Automated test functions controlled from the HPAT resume without user intervention. _____

Simulated control loops remain in default states. _____

Power Interruption Test (Append HAS and SOE reports for logged points.)

Neither primary nor secondary controller reset due to the power interruption. _____

None of the I/O card processors reset due to the power interruption. _____

None of the static DO channels change state during the power interruption. _____

None of the static AO channels change by more than 5% during the power interruption. _____

Measured parameters of the automated tests remain within tolerance during and following the power interruption. _____

Test Engineer _____ **Date** _____

Attachment 7.12 Power Quality Test Record (Continued)

Power Quality Tolerance Test (Append HAS and SOE reports for logged points.)

Test Setup:

All automated Operability tests configured for dynamic operation. _____

All simulated analog loops set to Auto mode with the SP at mid range. _____

All simulated digital loops have alarm status cleared and are set to simulate operating status (run/open status). _____

SOE and HAS loggers configured to record dynamic operating status. _____

All automated Operability tests enabled. _____

Record Power supply Output Voltage Levels

Power Feed	Power Module A		Power Module B	
	24-vdc	48 vdc	24 vdc	48 vdc
120 vac 60 Hz				
90 vac 57 Hz				
90 vac 63 Hz				
< 60 vac				
120 vac 60 Hz				
150 vac 57 Hz				
150 vac 63 Hz				
> 270 vac				
120 vac 60 Hz				

Test Engineer _____ **Date** _____

Attachment 7.13 – SOE and HAS Test Records

Record the file name, date and time for each test run.

Test Conducted	File Name	Date and Time Created
4- to 20-mA AI Accuracy		
4- to 20-mA AO Accuracy		
TC AI Accuracy		
RTD AI Accuracy		
Digital Response Time		
Analog Response Time		
Timer Test		
Communication Test		

Test Engineer _____ **Date** _____

Attachment 7.13 – SOE and HAS Test Records (Continued)

Test Conducted	File Name	Date and Time Created
Failover Operability Test		
Loss of Power Test		
Power Interrupt Test		
Power Quality Tolerance Test		
Failure to Complete Scan Test		

Test Engineer _____ **Date** _____

HF Controls

HF CONTROLS

HFC-6000 Control System

ERD111 – Control System Qualification Project

Prudency Test Procedure

TP0403 Rev G

Effective Date: 4/6/2010

Author: Ivan Chow

Reviewer: Charles McKinney

Approval: Ed Herchenrader

[XXXXXX]

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Revision History

Date	Revision	Author	Changes
4/15/02	0	J Taylor	Preliminary Draft
7/18/03	A	J Taylor	Initial Release
8/7/03	B	J Taylor	Reference to Figure 1 omitted; reference to QIO changed to ICL.
1/26/04	C	J Taylor	Document updated to reflect final design.
06/04	D	B Han	Red line changes
8/13/04	E	J Taylor	CR 2004-0155 Update prior to repetition of selected qualification tests.
9/8/04	F	J Taylor	CR2004-0170, SCR 926
3/8/10	G	I. Chow	Updated to current ERD111 configuration SCR 2670

Table of Contents

Paragraph	Title	Page
1.0	PURPOSE AND SCOPE	4
2.0	REFERENCES	4
2.1	INDUSTRY STANDARDS	4
2.2	RELATED PLANS AND PROCEDURES	5
2.3	SUPPORT DOCUMENTATION	5
2.4	HFC INTERNAL STANDARDS AND PROCEDURES	5
2.5	SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS	5
3.0	PREREQUISITES	6
3.1	EQUIPMENT REQUIRED	6
3.2	ENVIRONMENTAL CONDITIONS	7
3.3	TEST PERSONNEL	7
3.4	PRECAUTIONS	7
3.5	RED-LINE POLICY	7
3.6	EQUIPMENT SETUP	7
4.0	TEST PROCEDURE	8
4.1	BURST OF EVENTS TEST	8
4.1.1	BOE SETUP REQUIREMENTS	9
4.1.2	BOE TEST EXECUTION	11
4.1.3	CORRECTION FACTORS FOR ANALOG BOE CHANNELS	12

4.2 SERIAL PORT FAILURE TESTS 13
4.2.1 FAILURE TEST 14
4.2.2 FAILURE TEST 16
4.2.3 LINK FAILURE TEST 17
4.3 SERIAL PORT NOISE TEST 20
4.3.1 TEST SETUP 20
4.3.2 SERIAL LINK NOISE TEST 21
4.3.3 FAULT SIMULATION TEST 23
5.0 ACCEPTANCE CRITERIA 23
5.1 BURST OF EVENTS (BOE) TEST 23
5.2 C-LINK TEST 24
5.3 ICL TEST 24
5.4 PCC06 TEST 24
5.5 SERIAL PORT TEST 24
6.0 QA RECORDS 25
7.0 ATTACHEMENTS 25
Attachment 7.1 – Test Equipment Log 26
Attachment 7.2 – Prudency Test File Records 27

List of Figures

Number **Title** **Page**

Figure 1 – Algorithm for Analog BOE Test 12
Figure 2 – Noise Signal Waveform 21

List of Tables

Number **Title** **Page**

Table 1 – TSAP and HPAT Points Configured for Burst of Events Testing 10
Table 2 – BOE AO Channel Current Levels 13

1.0 PURPOSE AND SCOPE

In ERD111 project, a HFC-6000 control system, Test Specimen, is configured for generic qualification as a commercially available control system for safety-related applications in nuclear power plants. The following set of Prudency tests will be performed following completion of system integration and burn-in:

- **Burst of Events Test** - This test will consist of the simultaneous activation of a significant proportion of input and output channels in accordance [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XX]

- **Serial Port Failure Test**

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX] this test will impose three simulated failures on one cable at a time: link open, transmit line shorted to ground, and transmit line shorted to receive line. XXXXXXXXXXXXXXXXXXXXXXX

- **Serial Port Noise Test** - This test will introduce a white noise signal on each of the serial links one port at a time. XXXXXXXXXXXXXXXXXXXXXXXXXX

- **Fault Simulation Test** – This test covers introduction of a simulated failure condition to trigger failover from the primary to the secondary controller. The intent of this test is covered by the Failover Operability test (TP0402) and will not be duplicated in this test procedure.

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

This test procedure constitutes part of the pre-qualification testing for the HFC-6000 control system. These tests have been developed to document the baseline performance of the control system Test Specimen prior to the start of qualification stress testing.

2.2 [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXX]RELATED PLANS AND PROCEDURES

BOE	Burst of Events
CPC	Communication Protocol Controller
CSM	Control Switch Module
HAS	Historical Archiving System
HPAT	HFC Plant Automated Tester
FOT	Fiber-Optics Transmitter
M/A	Manual/Automatic
PCC	Peripheral Communication Controller
SOE	Sequence of Events
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test Specimen Application Program

3.0 PREREQUISITES

The following paragraphs identify the test equipment, test environment, and setup requirements for running each of the Prudency tests. Individual Prudency tests may be running concurrently with the Operability tests [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

3.1 EQUIPMENT REQUIRED

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

The following equipment and facilities will be required during performance of this test. Test personnel shall verify that all test and measuring equipment are capable of producing the level of accuracy required by the specific test being performed and that the calibration for the M&T to be used is current.

3.2 ENVIRONMENTAL CONDITIONS

This test will be conducted under various conditions of temperature and humidity. [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

Temperature	50 deg F to 104 deg F
Relative Humidity	7% to 90% non-condensing

3.3 TEST PERSONNEL

The set of Prudency tests will be conducted at the in-house test facility of HFC as part of the final acceptance testing of the Test Specimen and at the test facilities of qualification test laboratories during qualification testing. Qualified HFC test engineers will be responsible for conducting all Prudency tests both at the HFC facility and at qualification test laboratories.

3.4 PRECAUTIONS

WARNING

Certain I/O circuits are energized with high voltages and may carry potentially hazardous current loads. Exercise caution whenever working around exposed terminals or circuitry.

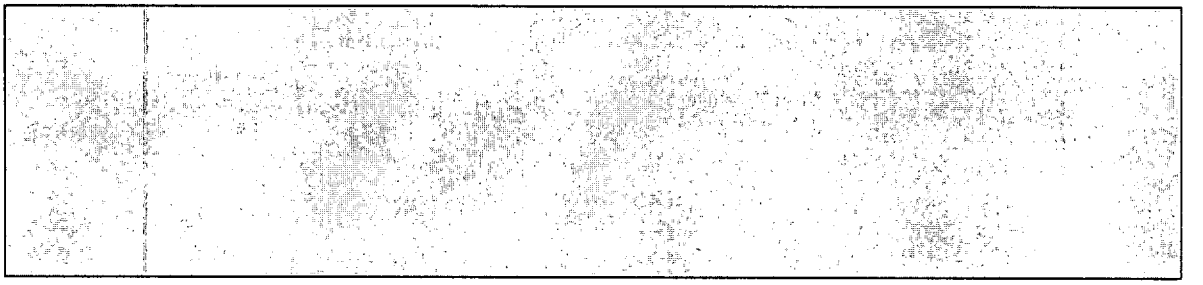
3.5 RED-LINE POLICY

The HFC policy for entering red-line corrections into a test procedure are presented in paragraph XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.6 EQUIPMENT SETUP

Prerequisites for beginning the Prudency test are as follows:

[illegible]



Validation that equipment setup is complete: _____
Name/Date

4.0 TEST PROCEDURE

Each of the Prudency tests provides a separate evaluation for a specific aspect of the Test Specimen performance and operation. Except as noted in a particular test procedure, no fixed sequence of execution is assumed or implied by the order of specific tests in this document.

Before executing the test, mark the test condition for this operability test to be executed in the following:

Test Condition

☐ Pre-Qualification / Baseline

☐ Environment ☐ High Temp/RH ☐ Low Temp/RH ☐ Post Stress

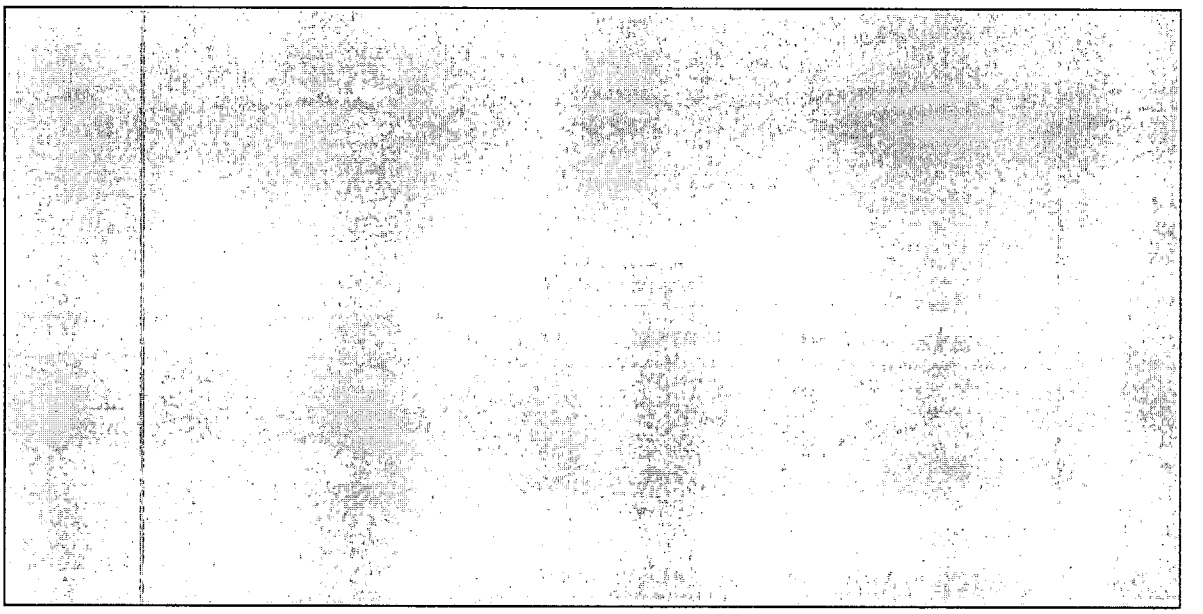
☐ Seismic ☐ During ☐ Post

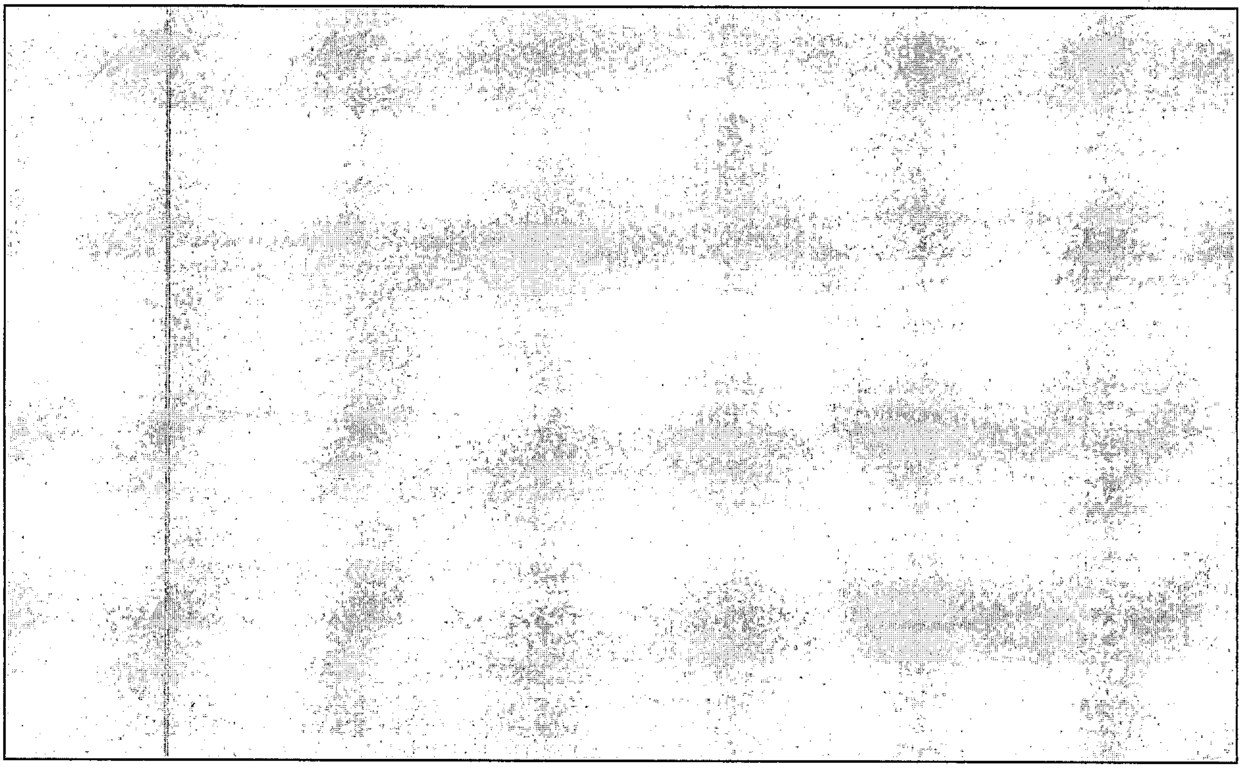
☐ EMI/RFI

☐ Post ESD

☐ Other _____

4.1 BURST OF EVENTS TEST





4.1.1 <u>BOE Setup Requirements</u>

The BOE test will be controlled by logic of the TSAP and the application programs running in the HPAT. [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

4.1.1.1 Automated Logging Utilities

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

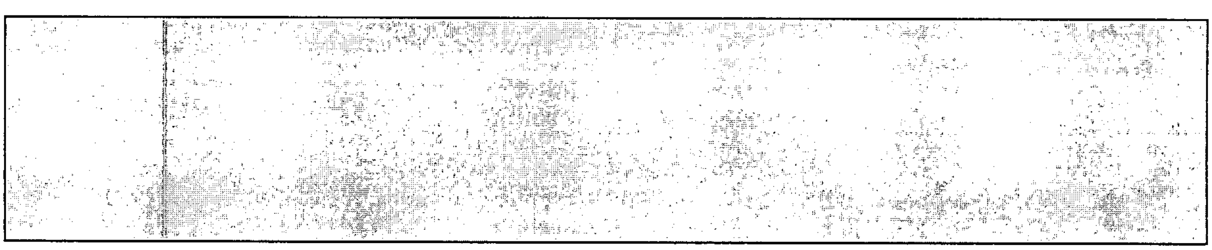
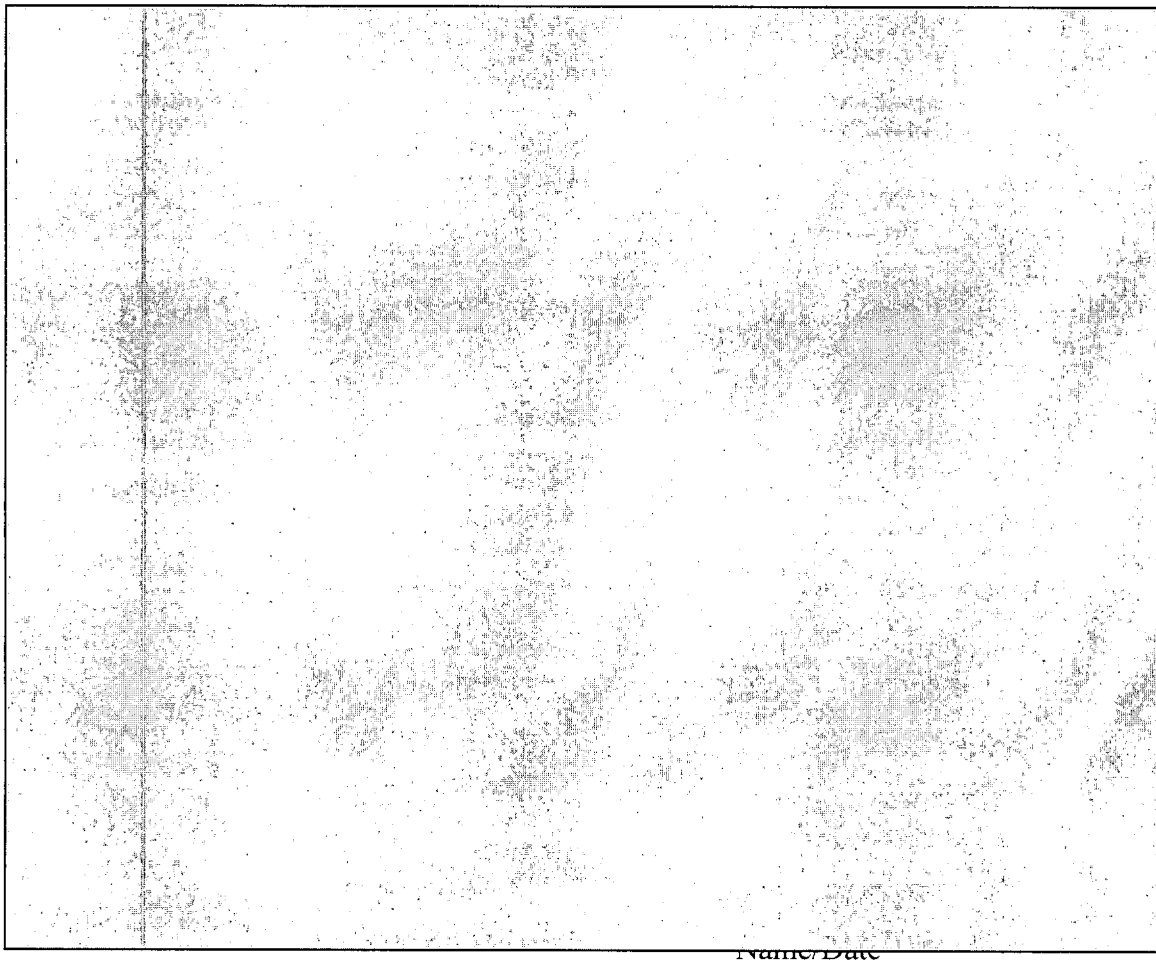


Table 1 – TSAP and HPAT Points Configured for Burst of Events Testing

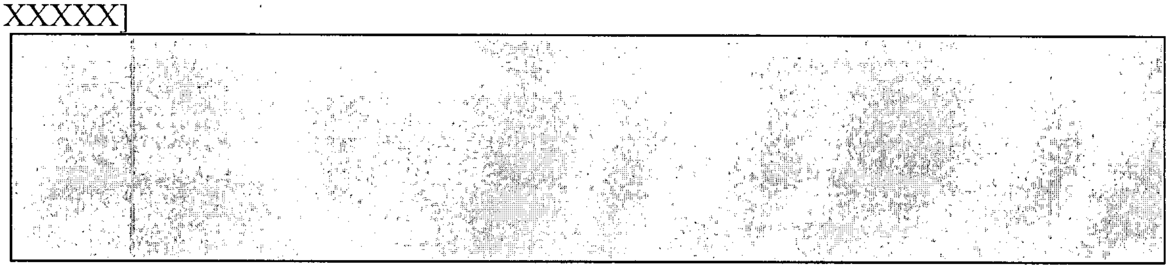
4.1.1.2 BOE Graphic Interface

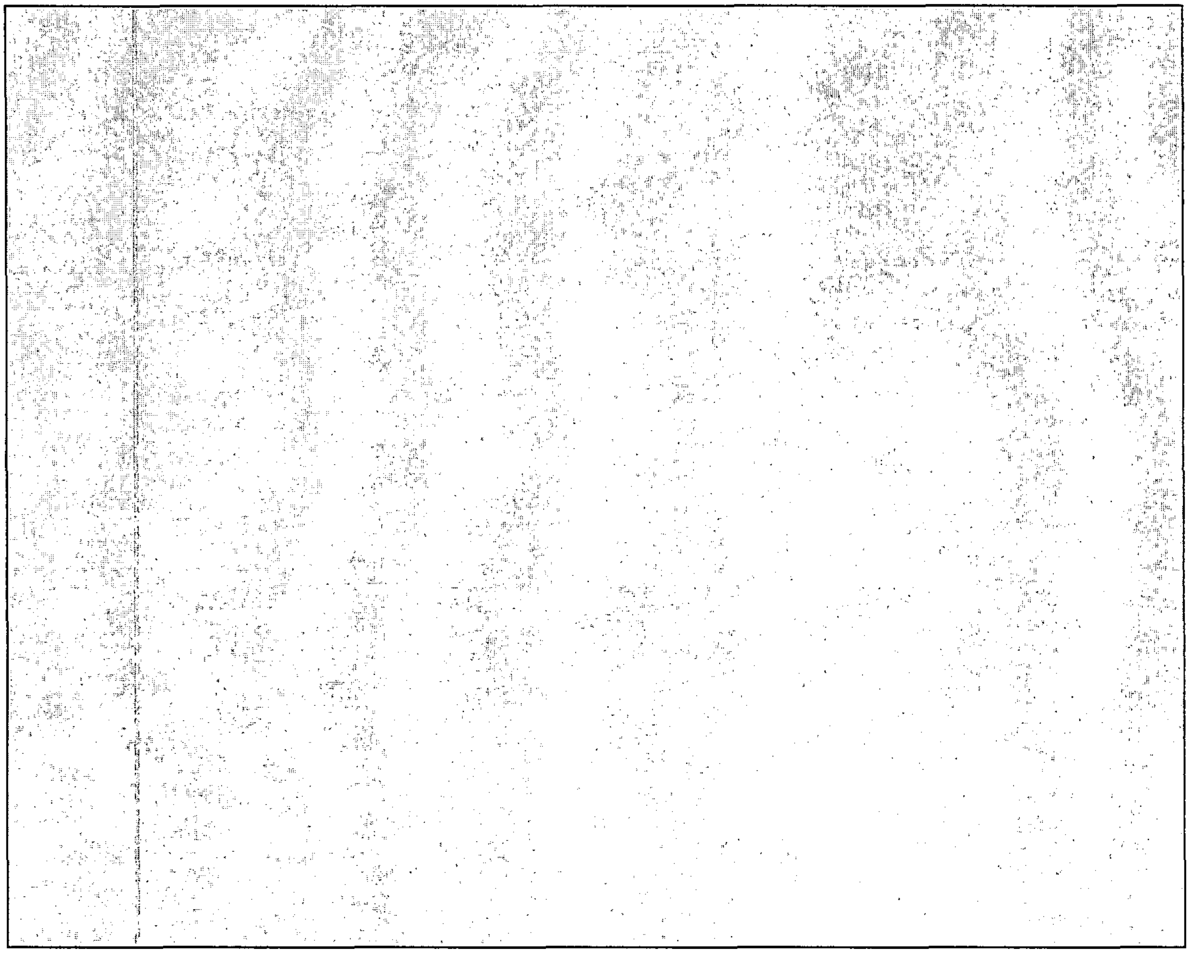
The BOE graphic interface is a display page for the MCRT that permits on/off control of the overall test and visual status monitoring of test operation. As a minimum, configure the BOE graphic interface as follows.



4.1.2 BOE Test Execution

After initial configuration requirements for the BOE test is complete[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXX]





4.2 SERIAL PORT FAILURE TESTS

The Test Specimen includes three different types of serial communication ports:

- [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XX]
- [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXX]
- [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

Each of these serial communication links will be subjected to a Serial Port Failure test. [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

4.2.1 XXXXX Failure Test

4.2.2 XXXXX Failure Test

[illegible]

4.2.3 <u>XXXXXXX Failure Test</u>

4.2.3.1 [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXX]Test Setup

[illegible]

4.3 SERIAL PORT NOISE TEST

[XXXXXXXXXXX] The serial port noise test will superimpose a XXXXXXXXXXX noise signal on the transmit and receive signal lines of each serial port. [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

4.3.1 <u>Test Setup</u>

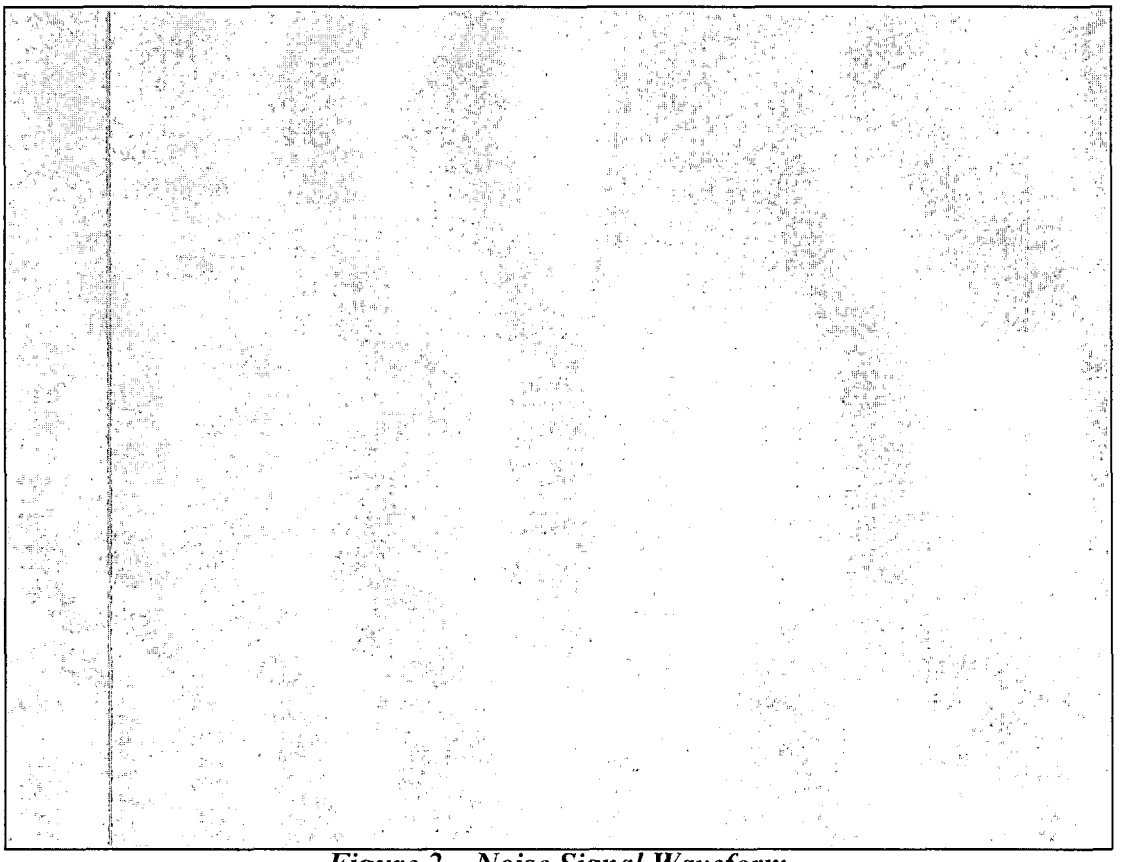
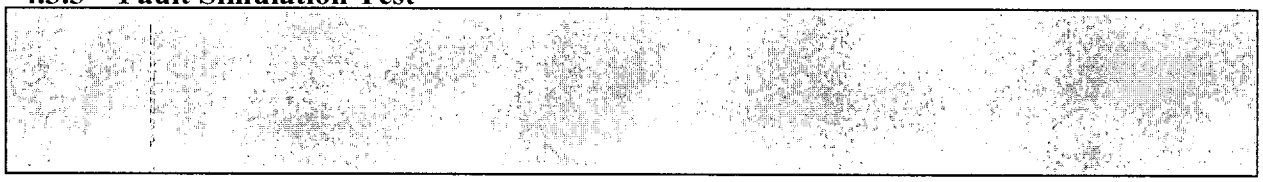


Figure 2 – Noise Signal Waveform

Validation that serial link noise test setup is complete: _____

Name/Date

4.3.3 Fault Simulation Test



5.0 ACCEPTANCE CRITERIA

5.1 BURST OF EVENTS (BOE) TEST

Acceptance criteria for the digital and analog points used in this test are as follows:

TSAP DI (TSAP memory image)	Every transition is detected. No link alarm condition is detected for DI cards in the Test Specimen. Each transition occurs within 1.0 ± 0.15 sec.
TSAP DO (HPAT memory image)	Every transition is detected. No link alarm condition is detected for DO cards in the Test Specimen. Each transition occurs within 1.0 ± 0.15 sec.
TSAP AI (TSAP memory image)	Each transition is detected and present in the resulting image signal. Averaged TSAP AI image accuracy at each level remains within ±0.32% of source signal (based on full span of 100%).
TSAP AO (HPAT memory image)	Each transition in the AI image is duplicated in the corresponding AO image. TSAP AO image duplicates source TSAP AI image. Averaged TSAP AO signal accuracy at each level remains within ±0.3% of source signal (based on full span of 100%).

5.2 C-LINK TEST

The test data records system response for two normal conditions (steps *2* and *13* in 4.2.1.2) and three abnormal (failure) conditions. Acceptance criteria for the XXXX port failure test are as follows:

> Response time characteristics of the test signal with the fault conditions imposed on the serial port do not deviate by more than ±10% from those with no fault condition.

5.3 ICL TEST

The test data records system response for two normal conditions (steps *2* and *13* in 4.2.2.2) and three abnormal (failure) conditions. Acceptance criteria for the XXXX-Link port failure test are as follows:

> Response time characteristics of the test signal with the fault conditions imposed do not deviate by more than ±10% from those with no fault condition.

5.4 PCC06 TEST

The test data records system response for two normal conditions (steps *2* and *23* in 4.2.3.2) and three abnormal (failure) conditions for each link. Acceptance criteria for the control module link failure are as follows:

> Response time characteristics of the test signal with the fault conditions imposed do not deviate by more than ±10% from those with no fault condition. (Failure to communicate over the link while a fault condition is imposed does not constitute a failure of the test.)

5.5 SERIAL PORT TEST

The test data records system response for normal conditions in step *13* in 4.3.2; each of the other test conditions includes injection of a noise signal on one of the system serial links. Acceptance criteria for the control module link failure are as follows:

> Response time characteristics of the test signal with the fault conditions imposed do not deviate by more than ±10% from those with no fault condition. (Loss of communication over the serial channel while the noise signal is being applied does not constitute a failure of the test.)

6.0 QA RECORDS

All data generated by execution of the tests covered by this procedure will become QA records and will be filed in accordance with QPP 17.1 "Quality Records". The test data will be recorded in SOE circular memory buffers and in an HAS database while the tests are being run. Following completion of each test, SOE and HAS report files must be generated to ensure reliable recovery of the test results.

The following sequence of steps outlines the procedure for generating SOE and HAS report files after completion of any particular test.

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7.0 ATTACHEMENTS

The following forms are attached to this document:

Attachment 7.1 – Test Equipment Log
Attachment 7.2 – Prudency Test File Records

Attachment 7.1 – Test Equipment Log

Test Equipment	Instrument ID	Calibration Due Date

Test Reviewer/Date

Attachment 7.2 – Prudency Test Data File Records

All test results will be recorded automatically in SOE and HAS logger files. Record the file name, date and time for each test run.

Test Conducted	File Name	Date and Time Created
Burst of Events Test		
C-Link Failure Tests		
ICL-Link Failure Tests		
Control Module Interface Failure Tests		

Test Engineer _____ **Date** _____

Attachment 7.2 – Prudency Test Data File Records (continued)

Test Conducted	File Name	Date and Time Created
C-Link Noise Test		
ICL-Link Noise Tests		
Control Module Noise Failure Tests		

Test Engineer _____ **Date** _____

HF Controls

HFC-6000 Control System

EPRI TR 107330 Qualification Program

Pre-Qualification Test Procedures

TP901-200-00 Rev B

Effective Date 8/3/2011

Author Ivan Chow

Reviewer Charles McKinney

Approval Ed Herchenrader

[XXXXXX]

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Revision History

Date	Revision	Author	Changes
1/26/2010	A	I. Chow	Initial Revision
8/01/2011	B	I. Chow	Inclusion of ERD1192

Table of Contents

1.0 PURPOSE AND SCOPE **3**

2.0 ORGANIZATIONAL RESPONSIBILITIES **3**

3.0 REFERENCES **3**

3.1 Industrial Standards and HFC Quality Procedures 3
3.2 Special Terms, Abbreviations, and Acronyms 4

4.0 TEST SPECIMEN SPECIFIC DOCUMENTS **4**

5.0 TEST PREREQUISITES **5**

5.1 Equipment Required 5
5.2 Equipment to be Tested 5
5.3 Environmental Conditions 5
5.4 Test Personnel 5
5.5 Equipment Setup 5

6.0 PRE-QUALIFICATION TEST SEQUENCE **5**

7.0 ACCEPTANCE CRITERIA **8**

8.0 QA RECORDS **8**

9.0 ATTACHMENTS **8**

1.0 Purpose and Scope

Components from the HFC-6000 product line will be assembled for a specific Test Specimen to be qualified. Before the assembly, the PLC/PCB components will be verified for valid calibrations. When assembly of the Test Specimen hardware is complete, the TSAP will be installed in the controllers and validated as part of the overall integration process. Integration testing will verify the following:

- The Test Specimen has been assembled in accordance with applicable engineering drawings.
- Hardware and software configuration is correct and accurately documented in the MCL.
- The controller communicates with all configured I/O channels and supporting equipment.
- The controller broadcasts all system status data to the C-Link.
- Software and hardware for logging status data are verified and validated to be functional so that the automated data can be captured.
- The HPAT is configured to control automatic testing of the Test Specimen.

Once overall configuration of the hardware and software has been verified, the first execution of the Operability and Prudency tests will begin.

2.0 Organizational Responsibilities

QPP 1.2 "Organizational Responsibilities" shall be followed for V&V / Testing activities.

V&V Team Manager is responsible for updating this document.

3.0 References

3.1 *Industrial Standards and HFC Quality Procedures*

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3.2 *Special Terms, Abbreviations, and Acronyms*

HAS	Historic Archive System
HPAT	HFC Plant Automated Tester
MCL	Master Configuration List
PCB	Printed Circuit Board
PLC	Programmable Logic Controller
SOE	Sequence of Events

4.0 Test Specimen Specific Documents

Use attachment 7.1 of this procedure to verify the documents required for this test procedure for a system/project. Completed attachment 7.1 shall be approved by the Director of Quality/Designee. The required documents for the system/project are:

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5.0 Test Prerequisites

The following paragraphs define the conditions that must be established and maintained throughout the duration of pre-qualification tests.

5.1 *Equipment Required*

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

5.2 *Equipment to be Tested*

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

5.3 *Environmental Conditions*

The test will be conducted in a mild environment without temperature or humidity stress conditions being imposed. The normal operating environment for the Test Specimen shall be as follows:

Temperature	60° to 104° F
Relative Humidity	40% to 95%

Test engineers shall verify that the temperature and relative humidity stay within the above indicated range throughout the operation.

5.4 *Test Personnel*

The pre-qualification tests will be conducted at the in-house test facility of HFC. All testing and monitoring functions will be conducted by HFC test engineers.

5.5 *Equipment Setup*

Equipment or system setup is project-specific to the test specimen. The test engineer shall make sure the test system setup complies with the "Test System Setup" document in the approved completed attachment 7.1 for the specific project.

6.0 Pre-Qualification Test Sequence

The Test Specimen will be subjected to a series of acceptance tests to verify that the hardware, firmware, and TSAP all operate as intended and to provide a performance baseline for the system. The overall sequence of testing during the pre-qualification phase will be as follows:

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The response of the Test Specimen during this phase of pre-qualification testing period will be recorded in a HAS archive database and will be used to produce a baseline performance profile. The SOE data will also be logged. Specified portions of the Operability and Prudency tests will be run during and after specified stress tests during the qualification test sequence. Comparison of the baseline performance profile with performance profiles recorded during and following each stress condition will provide the objective basis for acceptance of system performance. Any changes during the test execution shall comply with [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

7.0 Acceptance Criteria

Specific acceptance criteria for each test are presented in detail by the individual test procedures. These acceptance criteria are specific requirements listed in the EPRI standard as follows:

- Application Object Testing – 5.2.A, 5.6
- Initial Calibration – 5.2.D
- System Integration Tests, TSAP Validation Tests – 5.2.C
- Operability Tests – 4.2.3.7.B, 5.2.D, 5.3
- Prudency Tests – 5.2.E, 5.4
- Burn-In Test – 5.2.F

8.0 QA Records

Completed and approved attachment 7.1 of this procedure shall be kept in accordance with QPP 17.1 "Quality Record".

9.0 Attachments

7.1 Test Procedures Verification Form for Pre-Qualification Tests

Attachment 7.1
Test Procedures Verification Form for Pre-Qualification Tests

System/Project Name:_____ Contact Person:_____

Document Required

Document Description	Document Number	Rev	Verified
Application Object Test Procedures			_____ Initial/Date
System Integration Test			_____ Initial/Date
TSAP Validation Test			_____ Initial/Date
Operability Test			_____ Initial/Date
Prudency Test			_____ Initial/Date

_____
Test Engineer Signature/Date

_____
Reviewed/Approved by Director of Quality/Designee

HF Controls

HFC-6000 Control System

EPRI TR 107330 Qualification Program

Burn-In Test Procedures

TP901-200-01

Rev B

Effective Date	3/5/2010
Author	Ivan Chow
Reviewer	Charles McKinney
Approval	Ed Herchenrader

[XXXXXXXXXX]

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Revision History

Date	Revision	Author	Changes
1/19/2010	A	I. Chow	Initial Revision
3/4/2010	B	I. Chow	Revised red-line procedures to allow extension to burn-in log without initiating CR to address CR 2010-0043

Table of Contents

1.0 Purpose and Scope **3**

2.0 References **3**
2.1 Test Specimen Specific Documents 3
2.2 Industrial Standards and HFC Quality Procedures 3
2.3 Special Terms, Abbreviations, and Acronyms 3

3.0 Test Prerequisites **4**
3.1 Equipment Required 4
3.2 Equipment to be Tested 4
3.3 Environmental Conditions 4
3.4 Test Personnel 4
3.5 Equipment Setup 4

4.0 Burn-in Test Sequence **4**

5.0 Acceptance Criteria **6**

6.0 QA Records **6**

7.0 Attachments **7**

1.0 Purpose and Scope

The components for a HFC-6000 control system (Test Specimen) will be run in a normal operating environment for a minimum period of 352 hours prior to system qualification acceptance testing. The purpose of this test is to detect any early-life failures of PLC/PCB and other components. In addition to the required list of components of a test specimen, the scope of test will include spare parts which can be used to replace for any PCB that fails during subsequent qualification tests.

This test procedure is written in accordance with section XXXXXX. And it is written so that it can apply to test specimen for specific system setup.

To execute this test, a working copy of this procedure shall be obtained from document control.

2.0 References

2.1 *Test Specimen Specific Documents*

Use attachment 7.1 of this procedure to verify the documents required for this test of a specific system/project. Completed attachment 7.1 shall be approved by the Director of Quality/Designee. The required documents for the system/project are:

2.2 *Industrial Standards and HFC Quality Procedures*

EPRI TR-107330-1996	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants
QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-815	"Red-line" Procedure

2.3 *Special Terms, Abbreviations, and Acronyms*

MCL	Master Configuration List
PCB	Printed Circuit Board
PLC	Programmable Logic Controller
RH	Relative Humidity

PLC and PCB are interchangeable throughout this document.

3.0 Test Prerequisites

The following paragraphs define the conditions that must be established and maintained throughout the duration of the burn-in test.

3.1 *Equipment Required*

The burn-in test can be conducted in any system or test set as long as the operation of the PCB and related components can be verified. Power Distribution and Test System Setup documents only serve as references for validating the test specimen operation status.

3.2 *Equipment to be Tested*

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX1 shall contain the list of equipment to be tested.

3.3 *Environmental Conditions*

The test will be conducted in a mild environment without temperature or humidity stress conditions being imposed. The normal operating environment for the Test Specimen shall be as follows:

Temperature	50° to 104° F
Relative Humidity	7% to 90% Non-condensing

The information shall be logged using attachment 7.2 of this procedure for each component.

3.4 *Test Personnel*

The burn-in test will be conducted at the in-house test facility of HFC. All testing and monitoring functions will be conducted by HFC test engineers.

3.5 *Equipment Setup*

Equipment or system setup is project-specific to the test specimen. Test engineer shall make sure the test system setup complies with the "Test System Setup" document in the approved completed attachment 7.1 for the specific project.

4.0 Burn-in Test Sequence

The burn-in test requires a minimum period of 352 hours of operation. During that period, all cards/PCBs under test must remain in a normal operating state. These PCBs under test are those identified in the MCL or the spare part lists. Only those PCBs that complete the burn-in test satisfactorily will be available for subsequent use as part of the HFC-6000 test specimen.

Any changes during the test execution shall comply with XXXXXXXXXXXX Procedure except extending burn-in log for additional days incurred during the test.

The test engineer shall maintain a separate test record for each component being tested. The test record shall include the following information:

- Component name, part number, serial number, and software ID, revision
- PCB/Component rack and slot designation (if applicable) for burn-in test.
- Date and time burn-in test started.
- Date and time when burn-in test ended.
- Date and time when PCB was removed from the burn-in test.
- Description of equipment failure (if any) (Ref. CR number written for failure.)

NOTE:

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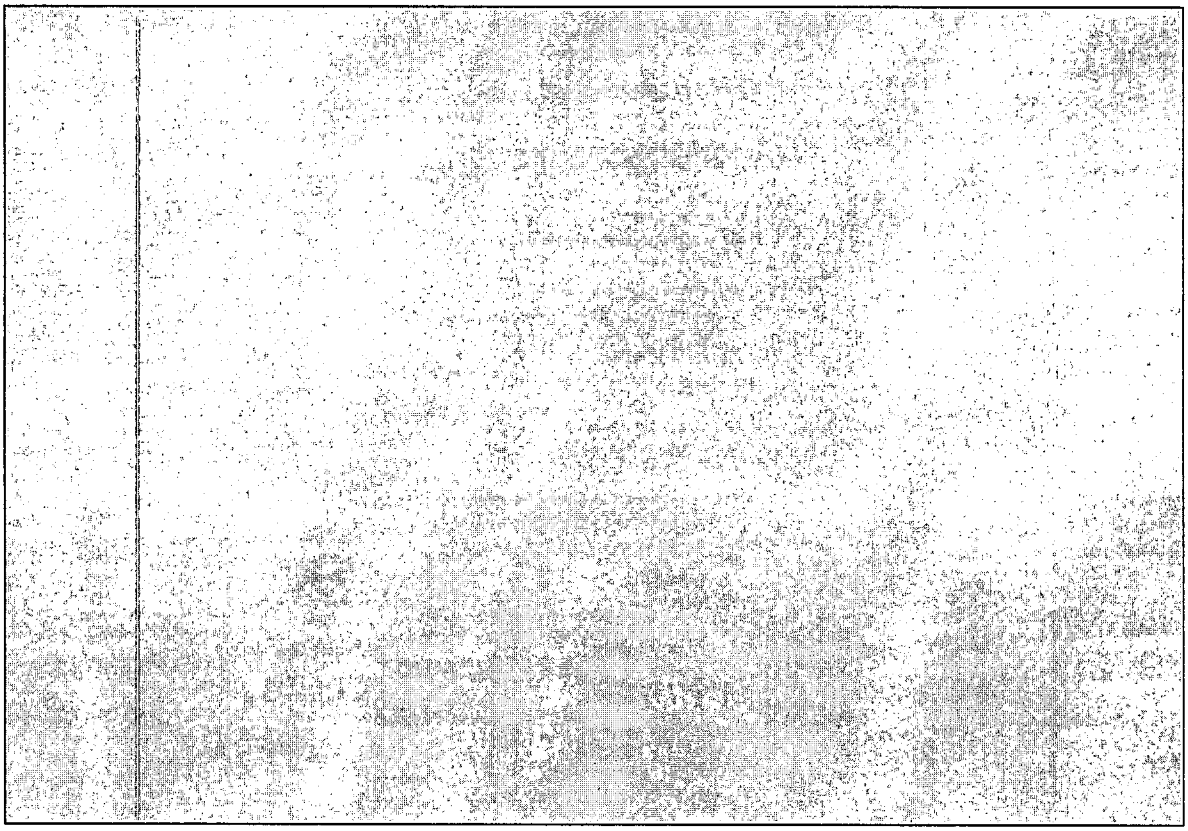

5.0 Acceptance Criteria

Acceptance criteria for successful completion of the burn-in test are as follows:

- For PCB,
  - Its edge LEDs under test indicates normal operation throughout the entire test interval.
  - DMT LED is on constantly.
  - TX and RX LEDs flash rapidly to indicate active communication.
- For other components such as power supply, computers or networking equipments, they shall be operating throughout the entire test period.

6.0 QA Records

The following QA records shall be generated during this test:

- [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

7.0 Attachments

7.1 Test Specimen Document Verification Form for Burn-in Tests

7.2 Burn-In Test Results Record

Attachment 7.1
Test Specimen Document Verification Form for Burn-in Tests

System/Project Name:_____ Contact Person:_____

Document Required

Document Description	Document Number	Rev	Verified
Master Configuration List (MCL)			_____ Initial/Date
Power Distribution Document			_____ Initial/Date
Test System Setup			_____ Initial/Date

_____
Test Engineer Signature/Date

_____
Reviewed/Approved by Director of Quality/Designee

Attachment 7.2
Burn-in Test Results Record

Master Configuration List: _____
PCB Name _____
Part No._____ Rev _____ Serial No. _____
Test System Rack and Slot _____

Test Summary

Item	Description	Signoff
1	Record date and time burn-in test period started and Temperature: _____ Relative Humidity : _____	_____ Date/Time
2	Record date and time burn-in test period will end successfully.	_____ Date/Time
3	Burn-in test period aborted due to component failure. Failed component identified and rejected. CR Number: _____	_____ Test Engineer/date
4	Record date and time burn-in test stopped either following complete 352-hour period was completed or following component failure.	_____ Date/Time

Burn-in Test Log

Day	Description Record date and time that normal operation is verified during burn-in test period	Signoff
1		_____ Date/Time
2		_____ Date/Time
3		_____ Date/Time
4		_____ Date/Time
5		_____ Date/Time
6		_____ Date/Time
7		_____ Date/Time

Attachment 7.2

Burn-in Test Log (Continued)

Day	Description Record date and time that normal operation is verified during burn-in test period	Signoff
8		_____ Date/Time
9		_____ Date/Time
10		_____ Date/Time
11		_____ Date/Time
12		_____ Date/Time
13		_____ Date/Time
14		_____ Date/Time
15		_____ Date/Time
16		_____ Date/Time
17		_____ Date/Time
18		_____ Date/Time

_____
Test Reviewer/Date

HF Controls

Qualification Test Procedure

Environmental Stress Tests

TP901-200-02 Rev D

Effective Date 9/13/2010

Author/Title Nathan Reid

Reviewer/Title Charles McKinney

Approval/Title Ivan Chow

[XXXXXXXXX]

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Revision History

Date	Revision	Author	Changes
3/16/10	A	I. Chow	Initial Release
5/27/10	B	R. McClanahan	Include TUV QP130066 Revision 0
6/29/10	C	I. Chow	Revised to make consistent format across different qualification test procedures and specify the acceptable test execution order.
8/30/10	D	N. Reid	CR 2010-0187 red-line changes.

Table of Contents

Section **Page**

1. 0 PURPOSE AND SCOPE 3

2. 0 ORGANIZATIONAL RESPONSIBILITIES 4

3. 0 REFERENCES 4

3.1. Test Specimen Specific Documents 4
3.2. Documentation 4
3.3. Special Terms, Abbreviations, and Acronyms 5

4. 0 QUALIFICATION TEST PREREQUISITIES 5

4.1. Test Personnel 5
4.2. Red-line Policy 5
4.3. Precautions 5
4.4. Test Setup 5

5. 0 TEST EXECUTION 6

5.1. Test Procedure 6
5.1.1. Test Environment 6
5.1.2. System Operation 6
5.1.3. Testing Location 6
5.1.4. Test Steps 7
5.1.5. Alarms, Failures and Environmental Conditions 24
5.2. Acceptance Criteria 24

6. 0 TEST RECORDS 25

7. 0 ATTACHMENTS 25

Attachment 7.1 Test Equipment Log 26
Attachment 7.2 Test Specimen Specific Documents 27
Attachment 7.3 Test Event Record 28

List of Figures and Tables

Number **Title** **Page**

Figure 1. Environmental Qualification Temperature and Humidity Profile 8
Table 1 Environmental Qualification Temperature and Humidity Profile Data 9

1.0 PURPOSE AND SCOPE

An environmental stress qualification test is one of a battery of tests mandated by EPRI TR-107330, Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, to qualify a commercially available PLC for safety-related applications in a nuclear power plant. This test exposes a control system executing a test application (hereafter referred to as the Test Specimen) to extremes of temperature and humidity in order to induce accelerated aging of functional components. This test also meets the TUV Climatic Test Requirements described in QP130066 Revision 0.

Testing will be accomplished by enclosing the Test Specimen in an environmental test chamber. There are test periods of operation (power on) and test periods of no operation (power off). During the operation periods, the Test Specimen will execute a Test System Application Program (TSAP) throughout the test period, and its operation will be monitored continuously by an automated test controller located outside the test chamber. In addition, comprehensive functional tests will be conducted at specified points during testing. The results of these tests will be used to identify any deterioration in the functional performance of the Test Specimen due to environmental stress.

The scope of this document covers any Test Specimen undergoing EPRI TR-107330 environmental qualification testing and TUV Climatic testing described in QP130066. Section 3.2 of this document contains references to the types of documents required for environmental qualification testing.

Attachment 7.2 shall be populated with the actual document numbers and revisions corresponding to the document types referenced for the specific qualification project. The list shall be approved by Director of Quality / Designee.

The following from document EPRI TR-107330 define the content and scope for environmental qualification testing:

- Sections 4.3.6, 4.6.1.1, 5.5, 6.2.1.1 item B, 6.3.1, 6.3.3 and 6.4.3
- Figure 4-4
- Table 5-1

Additionally, the following from document TUV QP130066 are included in the scope for environmental qualification testing:

- Page 2 Climatic Tests C-1, C-2, C-3, C-4, and C-5

To execute this test, a control copy of this procedure shall be obtained from document control. Test engineer shall record the Test Specimen(s) for this test shown below:

Test Specimen(s) for the Environmental Stress Test

_____

_____

_____

_____

2.0 ORGANIZATIONAL RESPONSIBILITIES

Director of Quality is responsible for maintaining this test procedure.

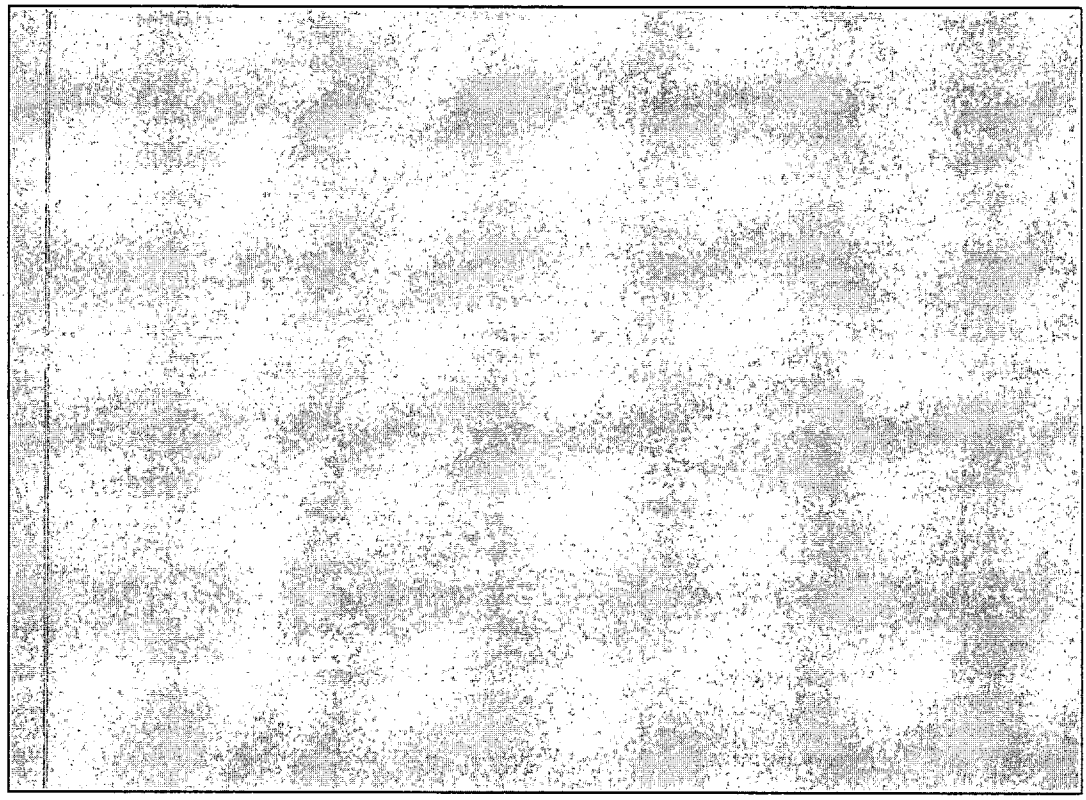
QA Manager is responsible for validating the test records.

V&V Manager is responsible for executing this test procedure with the assistance from Department of Engineering and Department of Operations for providing engineering personnel and technicians.

3.0 REFERENCES

3.1. Test Specimen Specific Documents

The following is a list of documents required to conduct EPRI TR-107330 environmental qualification testing on a particular Test Specimen. Attachment 7.2 contains the actual document numbers and revisions for the Test Specimen.



3.2. Documentation

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996
TUV QP130066	Basic requirements on environmental tests for functional safety type approval.
WI-ENG-815	"Red-line" Procedure
QPP 2.1	Quality Plans

3.3. Special Terms, Abbreviations, and Acronyms

HAS	Historical Archiving System
PLC	Programmable Logic Controller
RH	Relative Humidity
SOE	Sequence of Events
Test Specimen	A specific combination of control system hardware and software components to be subjected to specified test conditions. This may include power supplies, cabinets and mounting chassis
TSAP	Test Specimen Application Program – a synthetic application used to verify PLC functionality

4.0 QUALIFICATION TEST PREREQUISITIES

4.1. Test Personnel

A qualified test engineer from HFC will oversee setup of the Test Specimen, conduct all functional tests, and certify all test records produced during the test period.

4.2. Red-line Policy

The HFC policy for entering red-line corrections into a test procedure are specified in WI-ENG-815. Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

4.3. Precautions

The environmental test chamber will be maintained at an elevated temperature for several periods of time. During these periods, access to the interior of the test chamber should be avoided to ensure safety of personnel and to prevent invalidation of test results. To this end remote power switching is required.

4.4. Test Setup

Use attachment 7.1 to record test equipment used for the tests.

Use attachment 7.2 to record the required documents and the equipment list per test specimen.

Use attachment 7.3 to record the test events.

5.0 TEST EXECUTION

5.1. Test Procedure

Before executing the test, ensure all the required documents of the latest versions on the approved attachment 7.2 are available.

5.1.1. Test Environment

Environmental qualification testing shall be conducted with the Test Specimen located inside a temperature chamber.
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5.1.2. System Operation

Section 6.3.3 of EPRI TR-107330 requires the Test Specimen to be energized with the TSAP running during environmental qualification testing and loaded as follows:

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
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5.1.3. Testing Location

Execution for this test is expected to be done at a qualified laboratory outside HFC facility. Use attachment 7.3 to record the actual testing site and events for the actual test execution.

5.1.4. Test Steps

Figure 1 and Table 1 show the steps of the tests to be run using this procedure. Two environment stress tests are covered by this test procedure[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
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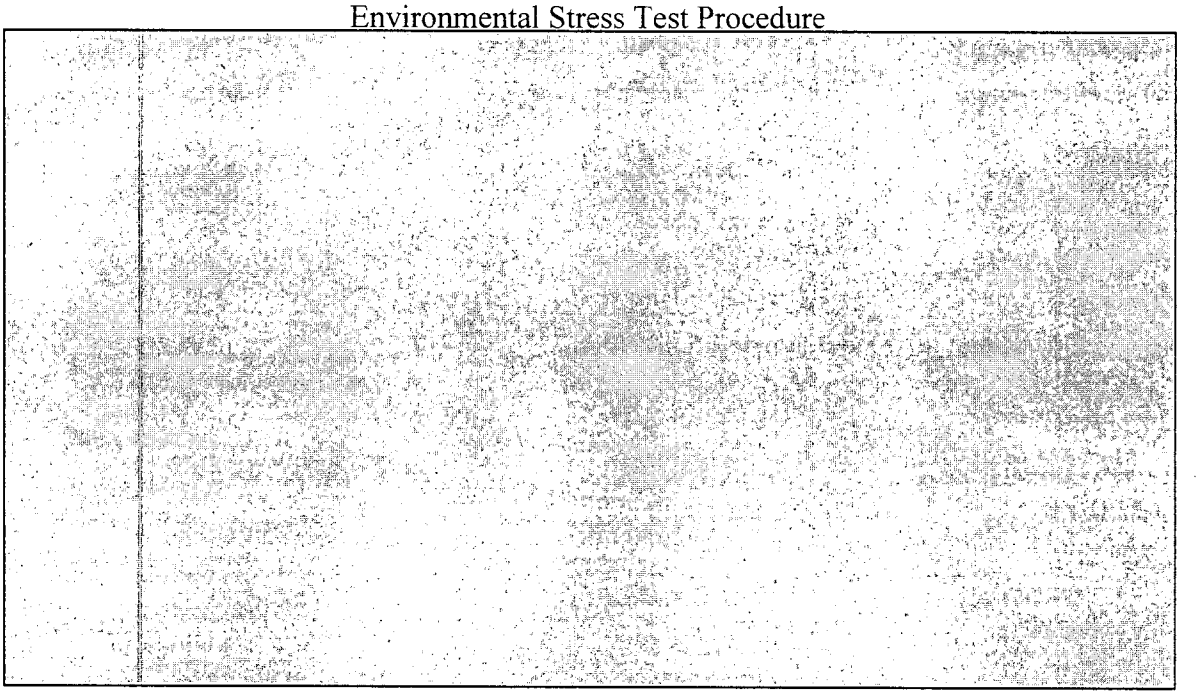
- Figure 1 and Table 1 below show the overall testing period with details.

Figure 1. Environmental Qualification Temperature and Humidity Profile

Use the following to record the actual test steps. The steps are designated to their specific tests.



Test Reviewer/Date

5.1.5. Alarms, Failures and Environmental Conditions

If any alarm condition is detected, the alarm state shall not affect overall functional operation of the Test Specimen or TSAP.

A random failure of any module will not be considered a failure of the overall environmental qualification test if the control system continues overall functional operation. A failed module may be replaced with a spare module without impacting the integrity of the test[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

5.2. Acceptance Criteria

The same Operability and Prudency tests performed during pre-qualification acceptance testing to establish baseline performance are also performed one or more times during environmental qualification testing. Acceptance criteria are as follows:

- Operability test results shall remain within tolerance limits of baseline values established during pre-qualification acceptance testing. Any deviation from baseline results exceeding specified tolerances shall be identified and recorded
- Prudency test results shall remain within tolerance limits of baseline values established during pre-qualification acceptance testing. Any deviation from baseline results exceeding specified tolerances shall be identified and recorded

The following shall also be included as part of the acceptance criteria:

- Static DO channels – no relay channels, energized or de-energized, shall exhibit any spurious transitions during testing. Any deviations shall be identified and recorded
- Static AO channels – an AO channel shall not deviate by more than 0.05% from its original set value throughout the test period. Any deviations shall be identified and recorded

6.0 TEST RECORDS

All test data generated during environmental stress qualification testing will become QA records. Test data will either be recorded on test data sheets appended to this document or in a set of HAS and SOE electronic files. The file names for each report and the date that the test was conducted will be recorded on test data sheets.

The following documentation shall be generated during the environmental test:

- [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

7.0 ATTACHMENTS

Attachment 7.1 – Test Equipment Log
Attachment 7.2 – Test Specimen Specific Documents
Attachment 7.3 – Test Event Log

Attachment 7.1 Test Equipment Log

Test Equipment	Instrument ID	Cal Due Date

_____
Test Engineer/Date

Attachment 7.2 Test Specimen Specific Documents

Test Specimen: _____

Equipment List

Quantity	Modular Type	Description	Cabinet Location

Setup Validation

TSAP Validation Test Procedure	Validation Completion Date

Required Documents

Operability Test Procedure	Prudency Test Procedure

_____
Test Engineer/Date

_____
Director of Quality or Designee / Date

Attachment 7.3 Test Event Record

Address of Test Facility:
Test start date:
Test end date:
List of electronic media storing test data:

HF Controls

HFC-6000 Control System

Qualification Program

ESD Test Procedures

TP901-200-03 Rev C

Effective Date 7/23/2010

Author Ivan Chow

Reviewer Charles McKinney

Approval Ed Herchenrader

[XXXXXXXX]

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Revision History

Date	Revision	Author	Changes
6/2/2010	A	I. Chow	Initial Revision
6/29/10	B	I. Chow	Revised to make consistent format across different qualification test procedures.
7/23/10	C	I. Chow	Revised the Equipment Setup section to use Pre-Test procedures

Table of Contents

Section **Title** **Page**

1.0 PURPOSE AND SCOPE **3**

2.0 REFERENCES **3**
2.1 INDUSTRIAL STANDARD 3
2.2 HFC QUALITY PROCEDURES 3
2.3 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS 4

3.0 TEST PREREQUISITES **4**
3.1 TEST EQUIPMENT REQUIRED 4
3.2 ENVIRONMENTAL CONDITIONS 4
3.3 TEST PERSONNEL 4
3.4 RED-LINE POLICY 4
3.5 TEST SPECIMEN SETUP 4
3.6 TEST SPECIMEN SPECIFIC TEST PROCEDURE 5
3.7 ESD TEST POINTS 5

4.0 ESD TEST SEQUENCE **6**
4.1 PRE-TEST 6
4.2 TEST EXECUTION 7
4.2.1 General Criteria 7
4.2.2 HFC Test Procedure 8
4.3 POST TEST 9

5.0 ACCEPTANCE CRITERIA **10**

6.0 QA RECORDS **11**

7.0 ATTACHMENTS **11**

Attachment 7.1– ESD Test Equipment Log 12
Attachment 7.2 – ESD Test Points 13
Attachment 7.3 – ESD Pre-Test Record 15
Attachment 7.4 – ESD Test Record 16
Attachment 7.5 – ESD Post-Test Record 17

1.0 Purpose and Scope

Electrostatic Discharge (ESD) is the abrupt release of charge from one object (often a person) to another. Such a discharge can permanently damage or otherwise upset the function of sensitive electronic circuits.

Electronic products are tested for ESD immunity to insure their continued reliable operation if subjected to realistic levels of ESD after being placed in service. Standard EPRI TR 107330 describes the specifics for acceptable ESD level of immunity in a nuclear safety operation environment. The test procedures described in this document are established for testing HFC-6000 control system in accordance with EPRI TR 107330, 1996.

The following references in the XXXX standard define the scope and content for this procedure: 4.3.8, Table 5-1, 6.3.1.B, 6.4.2

The level of ESD immunity required is defined in XXXX Appendix B Paragraph 3.5. ESD testing will be conducted by a qualified laboratory in accordance with international standard IEC 61000-4-2.

To execute this test, a control copy of this procedure shall be obtained from document control.

Test engineer shall record the Test Specimen(s) for this test shown below:

Test Specimen(s) for the ESD Test

_____

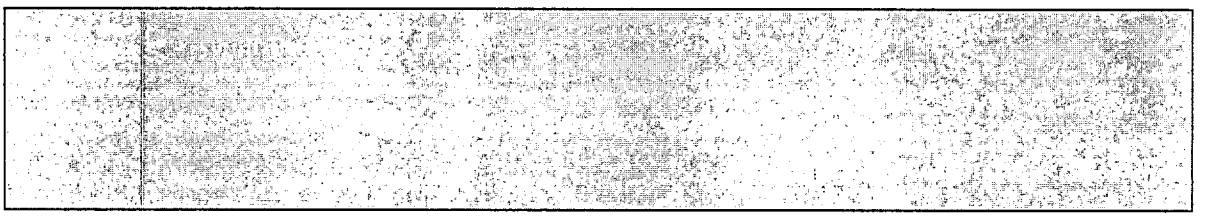
_____

_____

_____

2.0 References

2.1 *Industrial Standard*



2.2 *HFC Quality Procedures*

QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-815	"Red-Line" Procedure

2.3 *Special Terms, Abbreviations, and Acronyms*

EPRI	Electrical Power Research Institute
ESD	Electro-Static Discharge
HFC	Doosan HF Controls/HF Controls
PLC	Programmable Logic Controller

3.0 Test Prerequisites

The following paragraphs define the conditions required to begin ESD test.

3.1 *Test Equipment Required*

Test equipment required to generating the discharge will be provided by the laboratory. [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

The actual multimeter and other test equipment used shall be logged in attachment 7.1.

3.2 *Environmental Conditions*

The test will be conducted in a mild environment without temperature or humidity stress conditions being imposed. The normal operating environment for the Test Specimen shall be as follows:

Temperature	50° to 104° F
Relative Humidity	7% to 90% Non-condensing

3.3 *Test Personnel*

The ESD test will be conducted at a certified laboratory. Test personnel at the certified laboratory will conduct the tests and HFC test engineers will monitor the system and record the test results.

3.4 *Red-Line Policy*

Entering red-line corrections into a test procedure shall be done in accordance with [XXXXXXXXXXXXXXX] Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.5 *Test Specimen Setup*

Equipment or system setup is project-specific to the test specimen. Test engineer shall execute the Pre-Test test procedure in section 4.1 for validating the setup of the test specimen.

3.6 *Test Specimen Specific Test Procedure*

The test engineer shall request the Operability Test Procedure and Prudency Test Procedure for the Test Specimen(s) from Document Control and ensure the revision is the latest from the Quality Department. Complete attachment 7.2 for the required operability and prudency test procedures for the test specimen.

3.7 *ESD Test Points*

The ESD test points are also project-specific to the test specimen. The test engineer shall use attachment 7.2 to get the ESD test points from Engineering Department and approved by the Quality Department for the test specimen before executing this test. Make copies if necessary for each Test Specimen.

4.0 ESD Test Sequence

Test Specimen(s): _____

4.1 *Pre-Test*

After completing equipment setup, the following pre test shall be conducted to verify that the equipment is fully operational.

Pre-Test is completed successfully: _____

Test Engineer/Date

4.2 *Test Execution*

4.2.1 General Criteria

The following items summarize the general methods for test pulse application listed in XXXXX Paragraph 8.3.1:

4.2.2 HFC Test Procedure

HFC personnel shall perform the following steps for each Test Specimen while the ESD test is in progress.

[redacted]

4.3 *Post Test*

After applying discharges to all required ESD test points, for each Test Specimen, run the post test as follows.

[redacted]

5.0 Acceptance Criteria

Overall acceptance criteria for each component subjected to the ESD waveform shall be as follows:

- Application of the ESD test waveform does not disrupt normal operation of the Test Specimen or result in invalid transitions of any I/O channel, as indicated by the static point test log and the communication error counters.

- Failure of one controller will not be considered as a failure condition if the secondary controller takes over primary operation for the redundant pair.

- The Test Specimen performance remains within tolerance limits after exposure to the ESD test waveforms, and indicated by the pre test and post test Operability test results.

Each test record shall distinguish between four different categories of response:

- **Normal performance**. The equipment displays no degradation or deviation from the performance observed before the start of ESD testing.

- **Temporary degradation**. The equipment displays some deviation from performance observed before the start of testing but returns to normal operation without operator intervention.

- **Temporary loss of function**. The equipment displays deviation from performance observed before the start of testing but returns to normal operation following operator intervention or system reset.

- **Permanent degradation**. The system displays loss of function that cannot be restored due to component damage, damage to program software, or loss of data.

6.0 QA Records

The following documentation shall be generated during the ESD test. These documents will be considered QA records in accordance with QPP 17.1, "Quality Records".

- Pre-Test Results Records:
  - TSAP Validation (Functional) Test Record
  - SOE files and HAS data for the automated tests.
- Completed test procedure signoffs in each of the test procedure documents.
- Completed test result records appended to this document.
- SOE and HAS files covering the period during the ESD test
- Alarm log file for the period during the ESD test
- Post-Test Results Records:
  - SOE files and HAS data for the automated tests.

7.0 Attachments

7.1 Test Equipment Log

7.2 ESD Test Points

7.3 ESD Pre-Test Record

7.4 ESD Test Record

7.5 ESD Post-Test Record

Attachment 7.1– ESD Test Equipment Log

Test Equipment	Instrument ID	Calibration Due Date

Test Engineer/Date

Attachment 7.2 – Test Specimen Validation and ESD Test Points

Test Specimen: _____

Equipment List

Quantity	Modular Type	Description	Cabinet Location

Required Documents

Operability Test Procedure	Prudency Test Procedure

_____
Test Engineer (Engineering)/Date

_____
Approval (Quality)/Date

Attachment 7.2 – Test Specimen Validation and ESD Test Points (Continued)

Component (Chassis)	**Location**	**Discharge Type**
Power Supply		
Controller, I/O		

Author (Engineering)/Date

Approval (Quality)/Date

Attachment 7.3 – ESD Pre-Test Record

Test Specimen: _____

Item	Description	Initial
1	Power Supply Modules Records:	

Type	Measured Output

_____

2 Communication link error count record

ICL error count: _____

C-Link error count: _____

_____

3 Alarms which cannot be cleared:

_____

_____

_____

_____

SOE, HAS Files for Automated Operability and Prudency Test:

_____

_____

_____

_____
Test Engineer/Date

Attachment 7.4 – ESD Test Record

Test Specimen: _____

ESD Test Point: _____

Item	Description	Initial
1	Processing disruption (alarm/static data/communication Errors):	
	_____ _____ Time: _____	
	_____ _____ Time: _____	
	_____ _____ Time: _____	
	_____ _____ Time: _____	_____
2	Describe type of disruption: (1) Temporary Degradation, (2) Temporary loss of function, (3) Permanent Degradation. Record the maximum pulse withstood.	
	_____ _____ Max pulse: _____	
	_____ _____ Max pulse: _____	
	_____ _____ Max pulse: _____	
	_____ _____ Max pulse: _____	_____

SOE, HAS Files : _____

_____

_____

_____

Test Engineer/Date

Attachment 7.5 – ESD Post-Test Record

Test Specimen: _____

Item	Description	Initial
1	Power Supply Modules Records:	

Type	Measured Output

_____

2 Communication link error count record

ICL error count: _____

C-Link error count: _____

_____

3 Alarms which cannot be cleared:

_____

_____

_____

_____

SOE, HAS Files for Automated Operability and Prudency Test:

_____

_____

_____

_____
Test Engineer/Date

HF Controls

HFC-6000 Control System

EMI/RFI Qualification Test Procedure

TP901-200-05 Rev C

Effective Date 7/23//2010

Author Richard McClanahan

Reviewer Ivan Chow

Approval Ed Herchenrader

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Revision History

Date	Revision	Author	Changes
6/25/10	A	I. Chow	Initial Revision
6/29/10	B	I. Chow	Revised to have consistent format across different qualification test procedures.
7/20/10	C	R. McClanahan	Update attachments' layouts

Table of Contents

Paragraph	Title	Page
1.0	PURPOSE AND SCOPE	3
2.0	REFERENCES, ABBREVIATIONS, AND ACRONYMS	5
2.1	REFERENCES	5
2.2	ABBREVIATIONS, AND ACRONYMS	5
3.0	TEST PREREQUISITES	5
3.1	TEST EQUIPMENT REQUIRED	6
3.2	TEST ENVIRONMENT	6
3.3	TEST PERSONNEL	6
3.4	RED-LINE POLICY	6
3.5	SAFETY PRECAUTIONS	6
3.6	TEST SPECIMEN SPECIFIC TEST PROCEDURE	6
3.7	EQUIPMENT TO BE TESTED, EMI/RFI TEST POINTS	6
4.0	TEST SEQUENCE	8
4.1	PRE TEST	8
4.2	EMI/RFI TESTS	9
4.2.1	EMISSIONS TESTS	9
4.2.2	SUSCEPTIBILITY TESTS	11
5.0	ACCEPTANCE CRITERIA	14
6.0	QA RECORDS	15
7.0	ATTACHMENTS	15

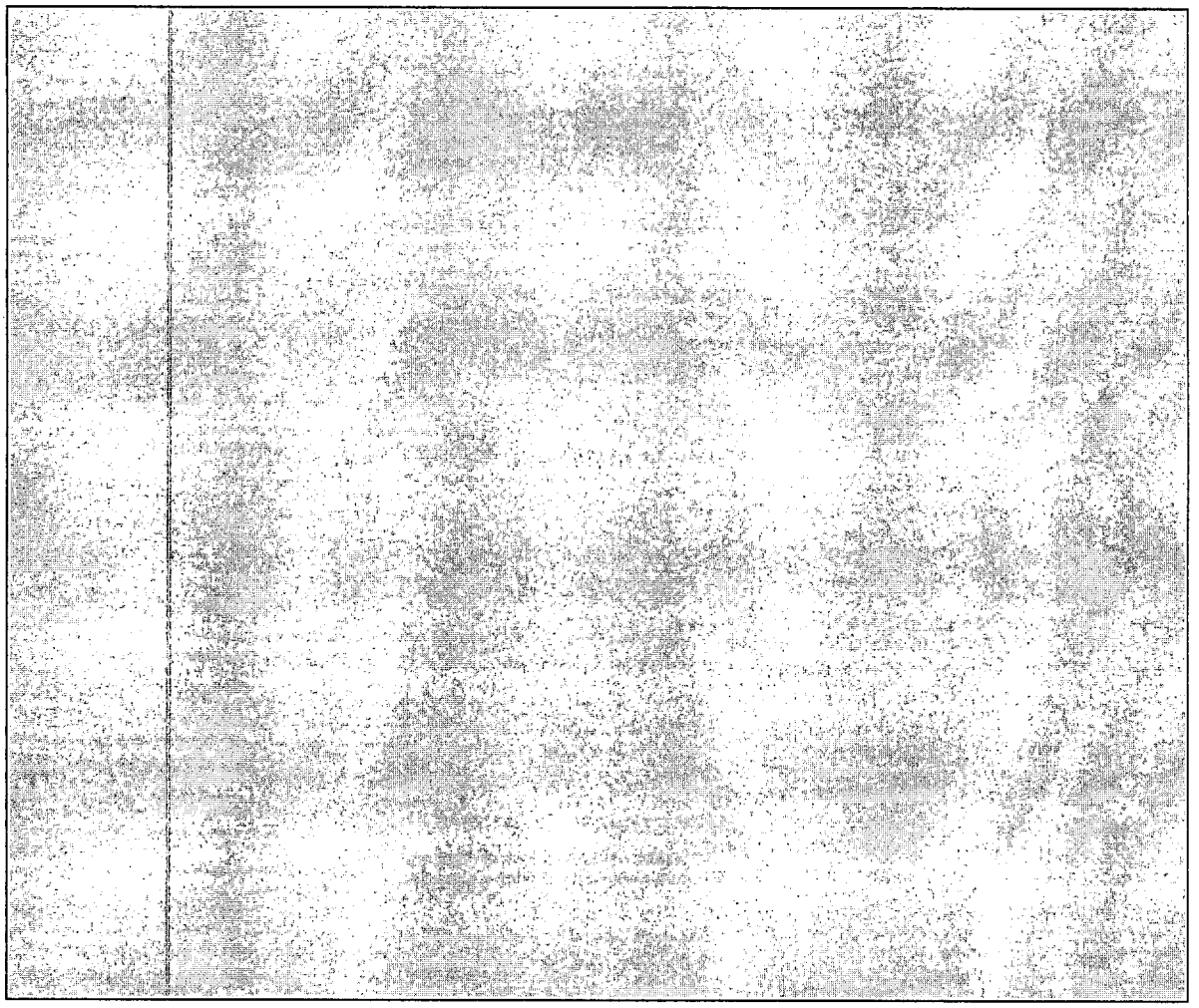
List of Tables and Figures

Number	Title	Page
Table 1 – Baseline Emission Tests		3
Table 2 – Baseline Susceptibility Tests		4
Figure 1 – Baseline Emission Tests		3
Figure 2 – Baseline Susceptibility Tests		4

1.0 PURPOSE AND SCOPE

This test procedure is designed to provide data to qualify a HFC-6000 Safety Control System to be operated in a nuclear power plant. The test procedure is written to follow the guidance of NRC Regulatory Guide 1.180 2003 Revision 1. Separate test procedures for both emission detection and radiation susceptibility are included. All tests will be conducted at a ISO/IEC 17025 certified laboratory. This document provides the overall procedures for performing the EMI/RFI tests in a certified laboratory. It applies to all HFC-6000 test specimens. Specifics of a particular test specimen shall be filled out using attachment 7.2 for approval before going to a certified laboratory for the tests. These specifics include detail equipment list and test points for the EMI/RFI tests.

According to the RG 1.180 2003 R1, section 3.6 EMI/RFI Emissions Test Summary, the required baseline emissions tests are:



For radiation susceptibility, the required baseline tests are listed in the following table:

Table 2 – Baseline Susceptibility Tests

Figure 2 – Baseline Susceptibility Tests

These test methods from MIL-STD- 461E are acceptable to the NRC staff for accomplishing EMI/RFI susceptibility testing for safety-related I&C systems intended for installation in nuclear power plants.

In this document, the specific test steps for performing these baseline tests are described.

To execute this test, a control copy of this procedure shall be obtained from document control. Test engineer shall record the Test Specimen(s) for this test shown below:

Test Specimen(s) for the EMI/RFI Test

_____

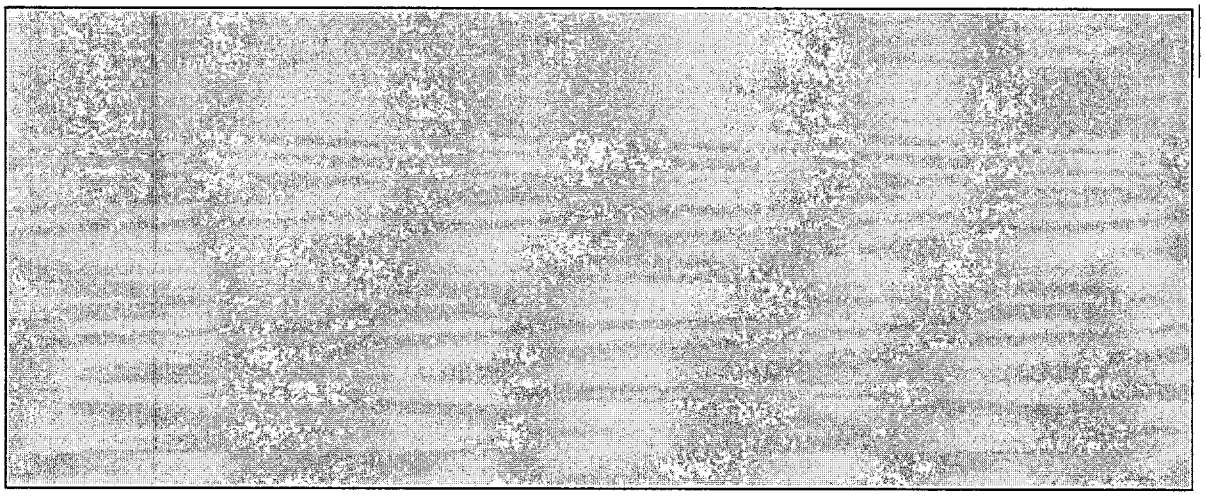
_____

_____

_____

2.0 REFERENCES, ABBREVIATIONS, AND ACRONYMS

2.1 *References*



2.2 *Abbreviations, and Acronyms*

BOE	Burst of Events
EMI	Electromagnetic Interference
MCL	Master Configuration List
RFI	Radio Frequency Interference
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test System Application Program

3.0 TEST PREREQUISITES

The following paragraphs provide detailed requirements for setup and performance of the EMI/RFI test. Certified test personnel from the laboratory will be responsible for installing the Test Specimen in the test chamber and for providing the equipment necessary to generate/measure EMI/RFI signals during the test. HFC test personnel will be responsible for controlling and monitoring functional operation of the Test Specimen.

3.1 *Test Equipment Required*

Use attachment 7.1 of this document to record test equipment used. The corresponding operability and prudency test procedures for the test specimen list the test equipment required, which are provided by HFC. The laboratory will supply their equipment as listed in their test plan.

3.2 *Test Environment*

The test will be conducted in a mild environment without temperature or humidity stress conditions being imposed. The normal operating environment for the Test Specimen shall be set as ambient conditions: room temperature and relative humidity.

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

3.3 *Test Personnel*

The EMI/RFI tests will be conducted at a certified laboratory. One or more qualified test engineers supplied by the laboratory will mount the Test Sample in the test chamber, control generation of the EMI/RFI test waveforms, and record EMI/RFI radiation levels. A qualified test engineer from HFC will oversee setup of the Test Specimen, conduct all functional tests, and certify all test records produced during each test.

3.4 *Red-Line Policy*

HFC quality work instruction [XXXXXXXXXXXXXXXXXXXXXXX]" shall be used for governing all red line changes.

3.5 *Safety Precautions*

EMI/RFI testing involves high frequency, large amplitude electromagnetic signals. Exposure to this radiation can damage electronic equipment and cause injury to personnel. Ensure that all applicable safety precautions are observed while test signals are being generated.

Do not view the equipment directly while the test waveforms are being applied to the Test Specimen.

3.6 *Test Specimen Specific Test Procedure*

The test engineer shall request the XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

3.7 *Equipment to be Tested, EMI/RFI Test Points*

Equipment to be tested and the EMI/RFI test points are also project-specific to the test

specimen[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXX]

4.0 TEST SEQUENCE

4.2 *EMI/RFI Tests*

There are no specific requirements for the order for performing these tests. The only requirement is to perform these tests according to the order set forth by the laboratory.

4.2.1 <u>Emissions Tests</u>

The emission tests are designed to detect if radiated or conducted emissions of the test specimen, while operating under normal conditions, are under the threshold given in the guiding standards.
[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

4.2.1.1 Conducted Emissions Test (CE 101, CE 102)

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

4.2.1.2 Radiated Emissions Test (RE 101, RE 102)

The RE101 test measures radiated magnetic field emissions in the frequency
[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

4.2.2 <u>Susceptibility Tests</u>

The susceptibility test consists of exposing the Test Sample to a radiated or conducted electronic noise signal and monitoring functional operation of the control logic for failure or invalid transitions. [XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

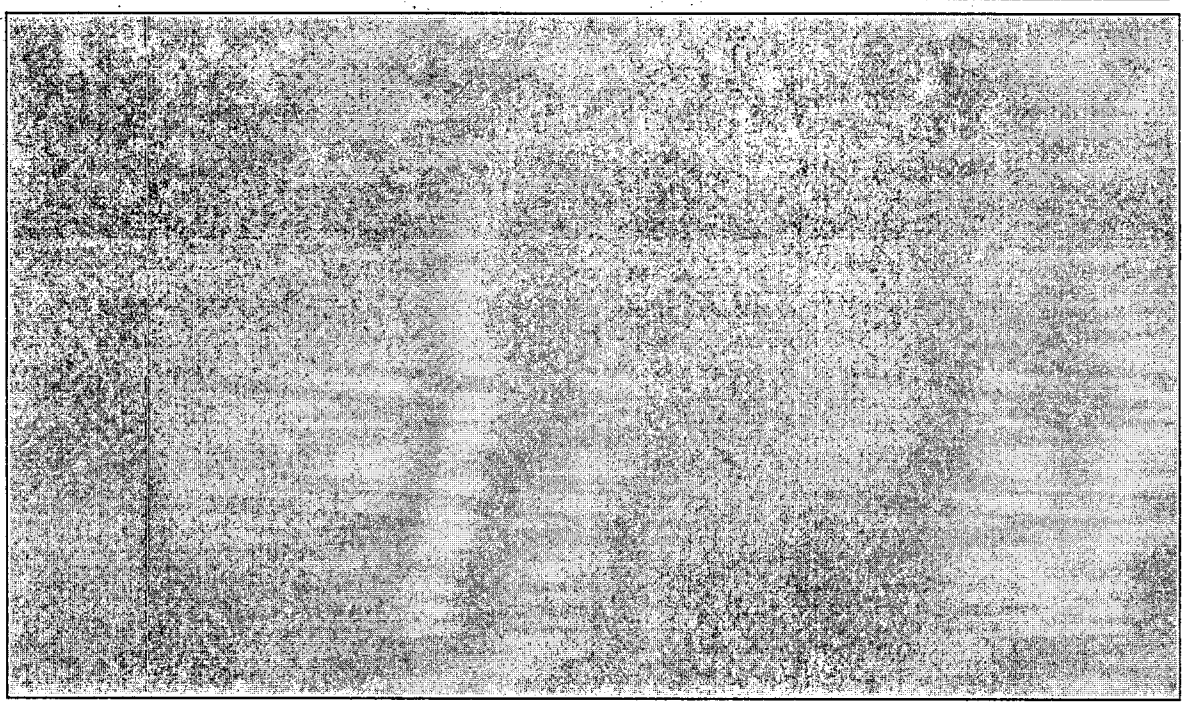
4.2.2.1 Conducted Susceptibility Test (CS 101, CS114, CS 115, CS 116)

[XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX]

4.2.2.2 Radiated Susceptibility Test (RS 101, RS 103)

The RS101 test ensures that equipment and subsystems are not susceptible to radiated magnetic fields [XXXXXXXXXXXXXXXXXX]

The RS103 test ensures that equipment and subsystems are not susceptible to radiated electric fields [XXXXXXXXXXXXXXXXXXXXX]



5.0 ACCEPTANCE CRITERIA

The EMI/RFI testing will be conducted in three phases. Overall acceptance criteria for each phase are as follows:

1. Operability and Prudency tests results during susceptibility tests shall remain within the tolerance limits listed in documents the corresponding Operability and Prudency test procedures for the test specimens. Any deviation from baseline results established during qualification testing shall be identified and recorded.

2. NRC RG 1.180 figure 3.1 3.2, 3.3, 3.4 indicates the maximum acceptable equipment emissions profile for each frequency range of each emission test.

3. Each subspecialty test will be run at 25%, 50%, 75% and 100% of the indicated maximum signal field strength listed in accordance with NRC RG 1.180. Insusceptible to signal provided is demonstrated by the following acceptance criteria:

   - All Test Specimen microprocessors continue to function normally.
   - Transfer of I/O data over serial links is not disrupted.
   - Serial communication links exhibit no increase in communication error rates.
   - Discrete I/O channels exhibit no spurious transitions.
   - Analog I/O channels do not change by more than 3% while the EMI/RFI signal is being applied.

   Signal level at which a susceptibility condition is detected shall be identified and recorded.

Attachment 7.1 – Test Equipment Log

Test Equipment	Instrument ID	Cal Due Date

_____
Test Reviewer/Date

Attachment 7.2 – Equipment Under Test List and EMI/RFI Test Points

Test Specimen: _____

Section A: Test Specimen Setup

Equipment List

Quantity	Modular Type	Description	Cabinet Location

Required Documents

Operability Test Procedure	Prudency Test Procedure

_____

Test Engineer (Engineering)/Date

_____

Approval (Quality)/Date

Attachment 7.2 – Equipment List and EMI/RFI Test Points (Continued)

Test Specimen: _____

Section B: EMI/RFI Emission Test Points/Cases

MIL-STD-461E	Test Cases	Description
CE 101		
CE 102		
RE 101		
RE 102		

_____

Test Engineer (Engineering)/Date

_____

Approval (Quality)/Date

Attachment 7.2 – EMI/RFI Test Points (Continued)

Test Specimen: _____

Section C: EMI/RFI Susceptibility Test Points/Cases

MIL-STD-461E	Test Cases	Description
CS 101		
CS 114		
CS 115		
CS 116		
RS 101		
RS 103		

_____

Test Engineer (Engineering)/Date

_____

Approval (Quality)/Date

Attachment 7.3 – EMI/RFI Pre-Test Record

Test Specimen: _____

Item	**Description**	**Initial**
1	Power Supply Modules Records:	

Type	Measured Output

_____

2 Communication link error count record

ICL error count: _____

C-Link error count: _____

_____

3 Alarms which cannot be cleared:

_____

_____

_____

_____

SOE, HAS Files for Automated Operability and Prudency Test:

_____

_____

_____

_____

Test Engineer/Date

Attachment 7.4 – CE 101

Low Frequency Conducted Emission Test

Test Specimen: _____

Test Case and Description: _____

Reference operating envelop shown as Fig. 5.2 Cabinet Doors: ☐ Closed ☐ Open

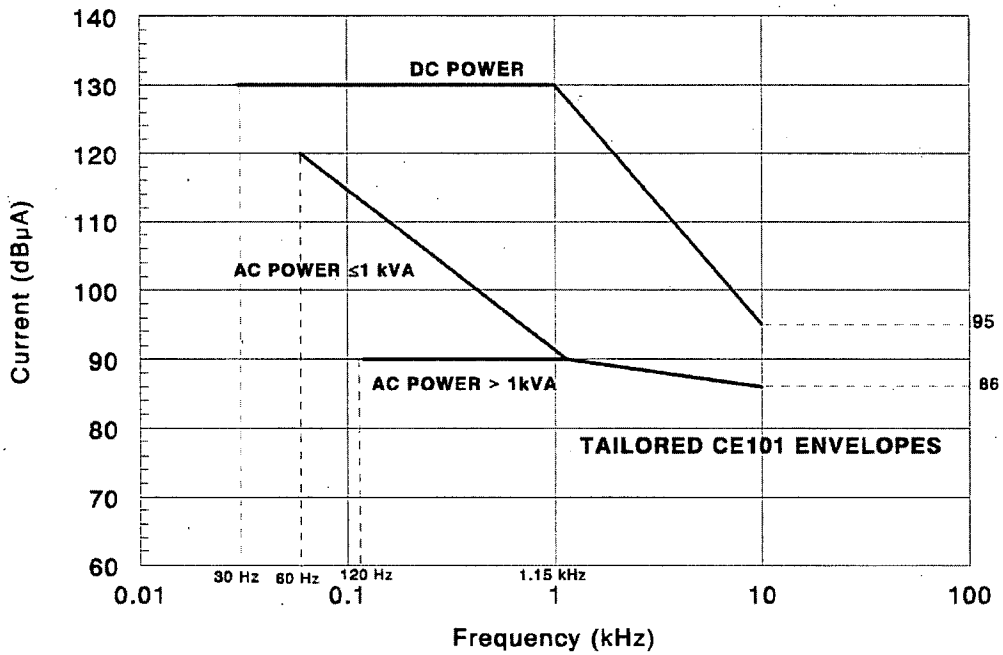


Fig. 5.2. CE101 operating envelopes.

Item	Description	Initial
1	Start time of test: _____	_____
2	End time of test: _____	_____
3	Test Data file (by lab): _____	_____

_____

Test Engineer/Date

Attachment 7.5 – CE 102

High Frequency Conducted Emission Test

Test Specimen: _____

Test Case: _____

Reference operating envelop shown as Fig. 5.5 Cabinet Doors: ☐ Closed ☐ Open

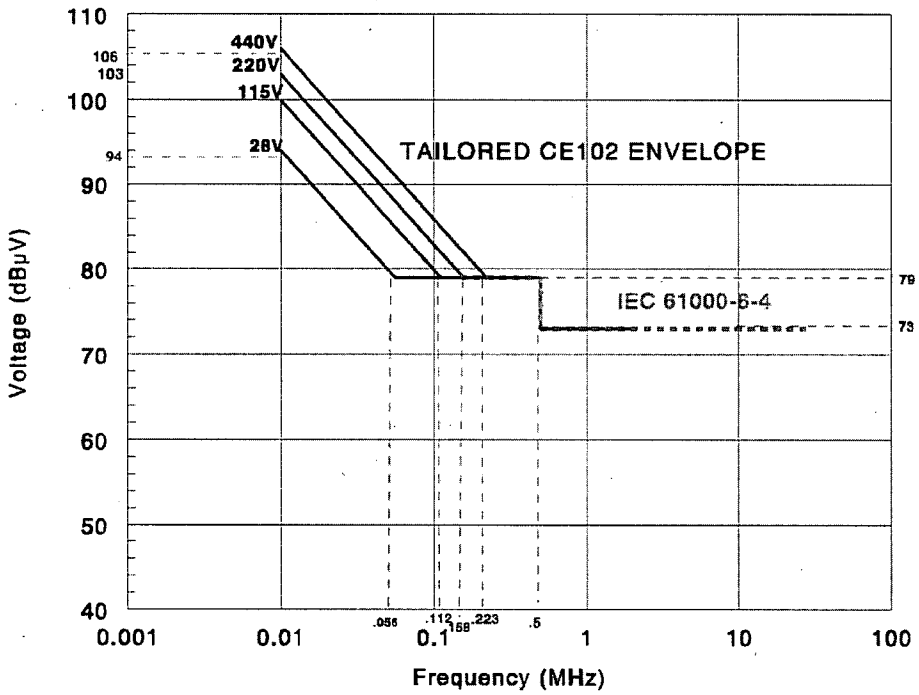


Fig. 5.5. CE102 operating envelope.

Item	Description	Initial
1	Start time of test: _____	_____
2	End time of test: _____	_____
3	Test Data file (by lab): _____	_____

_____

Test Engineer/Date

Attachment 7.6 – RE 101

Low Frequency Radiation Emission Test

Test Specimen: _____

Test Case: _____

Reference operating envelop shown as Fig. 5.3 Cabinet Doors: ☐ Closed ☐ Open

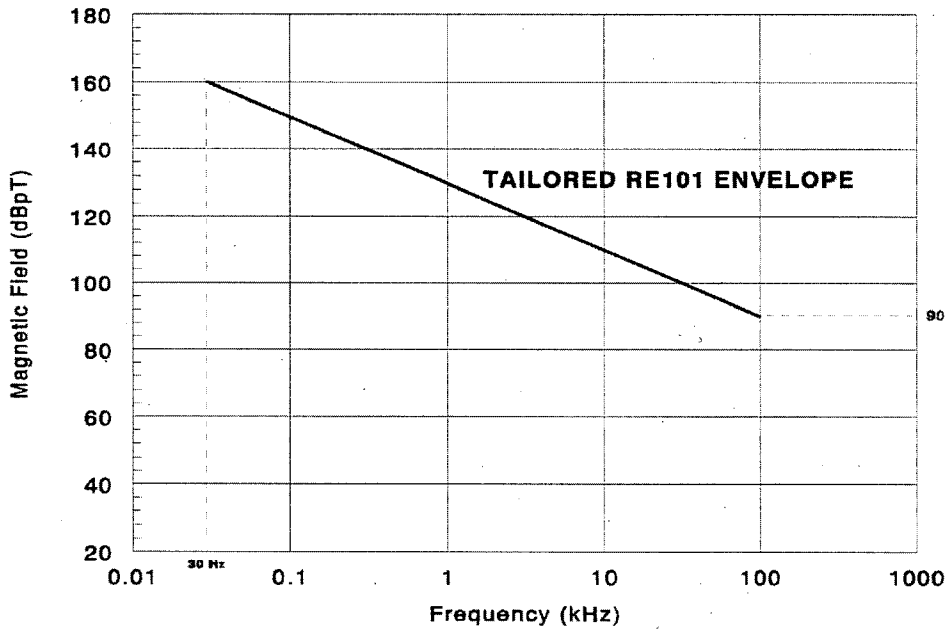


Fig. 5.3. RE101 operating envelope.

Item	Description	Initial
1	Start time of test: _____	_____
2	End time of test: _____	_____
3	Test Data file (by lab): _____	_____

_____

Test Engineer/Date

Attachment 7.7 – RE 102

High Frequency Radiation Emission Test

Test Specimen: _____

Test Case: _____

Reference operating envelop shown as Fig. 6.1 Cabinet Doors: ☐ Closed ☐ Open

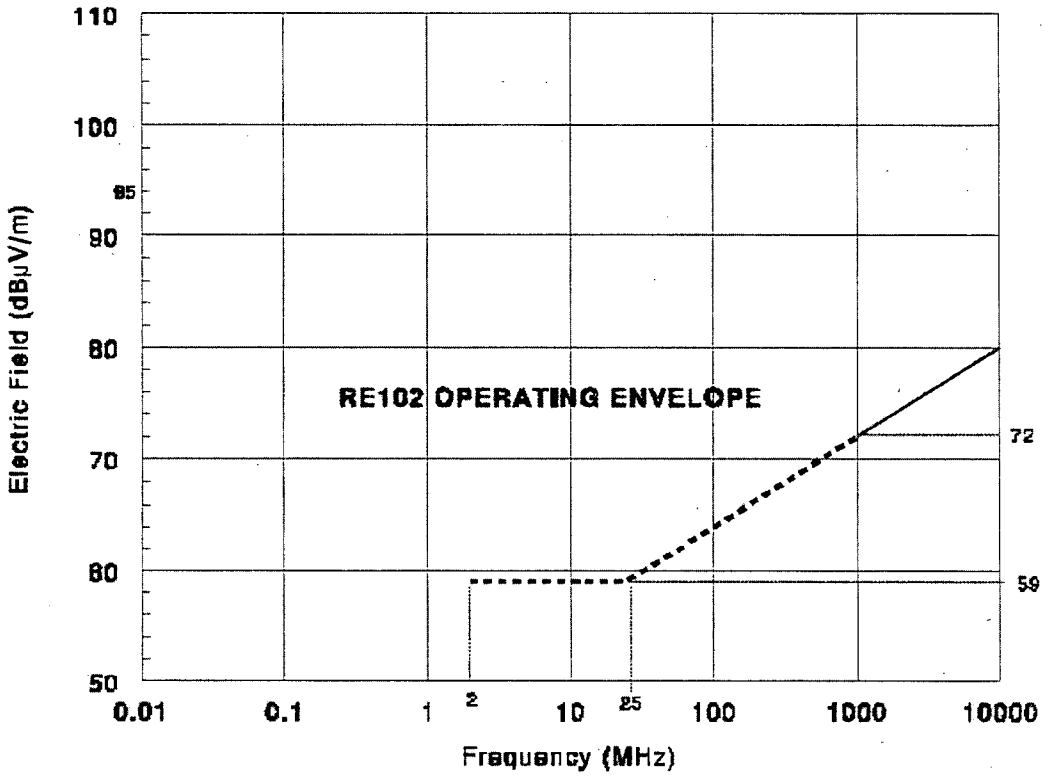


Figure 6.1 Electric-Field Radiated Emissions Envelope Above 1 GHz

Item	Description	Initial
1	Start time of test: _____	_____
2	End time of test: _____	_____
3	Test Data file (by lab): _____	_____

_____

Test Engineer/Date

Attachment 7.8 – CS 101

Low Frequency Conducted Susceptibility Test, Power Leads

Test Specimen: _____

Test Case and Description: _____

Reference operating envelop shown as Fig. 6.3 Cabinet Doors: ☐ Closed ☐ Open

Item	Description	Initial
1	% field strength required for the test: _____	_____
2	Start time: _____	_____
3	Stop time: _____	_____
4	SOE, HAS files: _____	_____
5	Test Data file (by lab): _____	_____
6	Susceptibility: ☐ Pass ☐ Not Pass Describe susceptibility condition detected (if any): _____ _____ at _____ frequency at _____ frequency at _____ frequency at _____ frequency	_____

_____

Test Engineer/Date

Attachment 7.9 – CS 114

High Frequency Conducted Susceptibility Test, Power and Signal Leads

Test Specimen: _____

Test Case and Description: _____

Reference operating envelop shown as Fig. 6.6 Cabinet Doors: ☐ Closed ☐ Open

Item	Description	Initial
1	% field strength required for the test: _____	_____
2	Start time: _____	_____
3	Stop time: _____	_____
4	SOE, HAS files: _____	_____
5	Test Data file (by lab): _____	_____
6	Susceptibility: ☐ Pass ☐ Not Pass Describe susceptibility condition detected (if any): _____ _____ at _____ frequency at _____ frequency at _____ frequency at _____ frequency	_____

_____

Test Engineer/Date

Attachment 7.10 – CS 115

Bulk Injection Conducted Susceptibility Test, Power and Signal Leads

Test Specimen: _____

Test Case and Description: _____

Reference test signal 6.7 Cabinet Doors: ☐ Closed ☐ Open

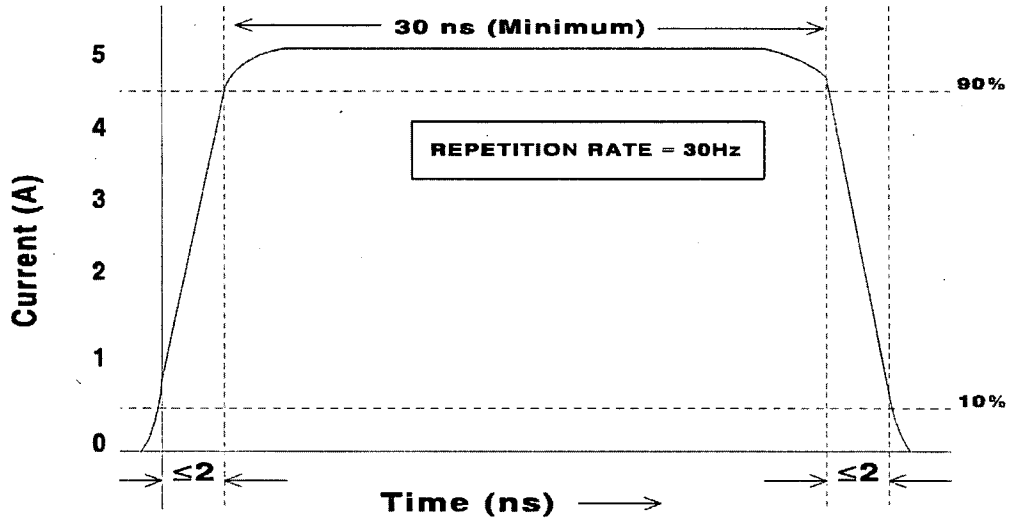


Fig. 6.7. CS115 test signal.

Item	Description	Initial
1	% field strength required for the test: _____	_____
2	Start time: _____	_____
3	Stop time: _____	_____
4	SOE, HAS files: _____	_____
5	Test Data file (by lab): _____	_____
6	Susceptibility: ☐ Pass ☐ Not Pass Describe susceptibility condition detected (if any): _____ _____	_____

_____

Test Engineer/Date

Attachment 7.11 – CS 116

Damped Sinusoidal Transients Conducted Susceptibility Test, Power and Signal Leads

Test Specimen: _____

Test Case and Description: _____

Reference operating envelop shown as Fig. 6.14 Cabinet Doors: ☐ Closed ☐ Open

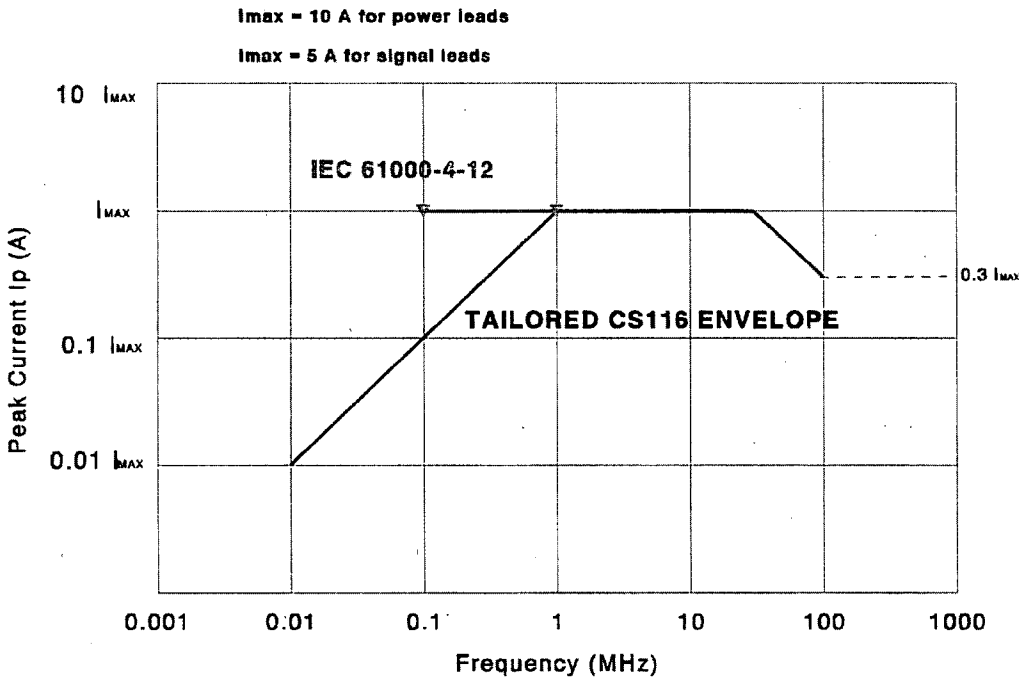


Fig. 6.14. Damped sinusoid conducted susceptibility operating envelopes.

Item	Description	Initial
1	% field strength required for the test: _____	_____
2	Start time: _____	_____
3	Stop time: _____	_____
4	SOE, HAS files: _____	_____
5	Test Data file (by lab): _____	_____
6	Susceptibility: ☐ Pass ☐ Not Pass Describe susceptibility condition detected (if any): _____ _____ at _____ frequency at _____ frequency at _____ frequency at _____ frequency	_____

_____

Test Engineer/Date

Attachment 7.12 – RS 101

Low Frequency Radiated Susceptibility Test

Test Specimen: _____

Test Case and Description: _____

Reference operating envelop shown as Fig. 7.2 Cabinet Doors: ☐ Closed ☐ Open

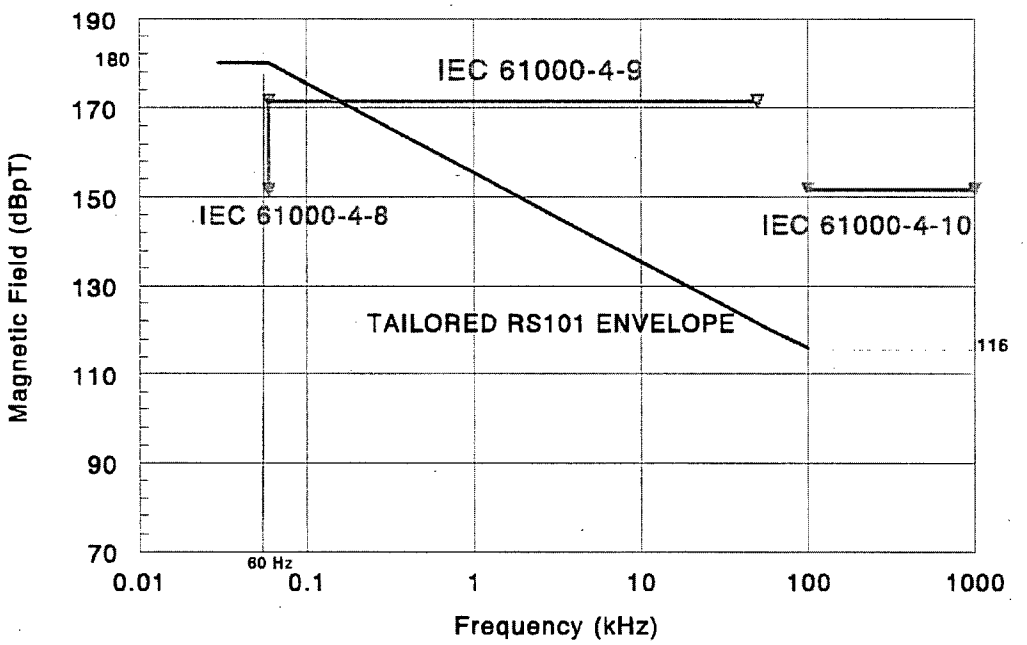


Fig. 7.2. Low-frequency radiated susceptibility operating envelopes.

Item	Description	Initial
1	% field strength required for the test: _____	_____
2	Start time: _____	_____
3	Stop time: _____	_____
4	SOE, HAS files: _____	_____
5	Test Data file (by lab): _____	_____
6	Susceptibility: ☐ Pass ☐ Not Pass Describe susceptibility condition detected (if any): _____ _____ at _____ frequency at _____ frequency at _____ frequency at _____ frequency	_____

_____

Test Engineer/Date

Attachment 7.13 – RS 103

High Frequency Radiated Susceptibility Test

Test Specimen: _____

Test Case and Description: _____

Reference operating envelop shown as Table 7.5 Cabinet Doors: ☐ Closed ☐ Open

Table 7.5. Comparison of high-frequency radiated susceptibility tests

Parameter	RS103	IEC 61000-4-3
Application	Equipment enclosures	Equipment enclosures
Frequency coverage	10 kHz to 1 GHz	26 MHz to 1 GHz
Methodology:		
Similarities	– Exposure to electric fields	– Exposure to electric fields
Differences	– Shielded or partially anechoic room – EUT exposure monitored by field probes – EUT grounded and bonded as in typical use – No circularly polarized fields – Square wave modulation – Variable sweep rate through frequency bands	– Anechoic room – Exposure levels determined with sensor grid without EUT – EUT isolated from ground plane and grounded only through safety ground wire – Circularly polarized fields allowed – Sine wave modulation – Fixed sweep rate over entire frequency range
Operating envelopes	10 V/m	Level 3–10 V/m

Item	Description	Initial
1	% field strength required for the test: _____	_____
2	Start time: _____	_____
3	Stop time: _____	_____
4	SOE, HAS files: _____	_____
5	Test Data file (by lab): _____	_____
6	Susceptibility: ☐ Pass ☐ Not Pass Describe susceptibility condition detected (if any): _____ _____ at _____ frequency at _____ frequency at _____ frequency at _____ frequency	_____

_____

Test Engineer/Date

HF Controls

HFC-6000 Control System

Qualification Program

Surge Withstand Test Procedures

TP901-200-06 Rev D

Effective Date 12/31/2010

Author Nathan Reid

Reviewer Ivan Chow

Approval Charles McKinney

[XXXXX]

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Revision History

Date	Revision	Author	Changes
5/18/2010	A	I. Chow	Initial Revision
6/29/10	B	I. Chow	Revised to make consistent format across different qualification test procedures
7/23/10	C	I. Chow	Revised to use Pre-Test test procedure for validating the system setup.
8/26/10	D	N. Reid	CR 2010-0244 1) Removed EFT wave from data line test points. 2) Revised test procedure for better channel monitoring.

Table of Contents

Section **Title** **Page**

1.0 PURPOSE AND SCOPE **4**

2.0 REFERENCES **4**
2.1 Industrial Standard 4
2.2 HFC Quality Procedures 5
2.3 Definitions, Abbreviations, and Acronyms 5

3.0 TEST PREREQUISITES **5**
3.1 Test Equipment Required 5
3.2 Test Waveform Requirements 6
3.3 Environmental Conditions 6
3.4 Test Personnel 6
3.5 Red-Line Policy 7
3.6 Test Specimen Setup 7
3.7 Test Specimen Specific Test Procedure 7
3.8 Surge Withstand Test Points 7

4.0 SURGE WITHSTAND TEST SEQUENCE **8**
4.1 Pre-Test 8
4.2 Test Points 9
4.3 Test Execution 10

5.0 ACCEPTANCE CRITERIA **21**

6.0 QA RECORDS **21**

7.0 ATTACHMENTS **22**
Attachment 7.1– Surge Withstand Test Equipment Log 23
Attachment 7.2 – Surge Withstand Test Points 24
Attachment 7.3 – ESD Pre-Test Record 27
Attachment 7.4 – Power Supply Test Results 28
Attachment 7.5 – DO Channels Test Results 30
Attachment 7.6 – DI Channel Test Results 34
Attachment 7.7 – AI/AO 4- to 20-mA Common Terminal Test Results 36

Attachment 7.8 – AI Input 0- to 5-vdc Common Terminal Test Results 38
Attachment 7.9 – RTD Common Terminal Test Results..... 40
Attachment 7.10 – TC Common Terminal Test Results..... 42
Attachment 7.11 – Pulse Card Common Terminal Test Results 44

1.0 Purpose and Scope

The HFC-6000 control system (Test Specimen) is designed to operate in a wide variety of industrial applications. The control system hardware may be installed both in an electrical equipment room and at various other locations near the equipment under control. In either environment, power, electrical I/O signal lines, and hardwired communication cables may be exposed to high amplitude transient signals. The test covered by this document injects a large amplitude surge waveform at specified points of the Test Specimen. The purpose of this test is to demonstrate that Test Specimen performance characteristics remain within acceptable limits during and after exposure to such discharges.

The test procedures are written to follow the guidelines set forth by NRC RG 1.180 on power surge tests. In addition, the scope of this test procedure will cover requirements in EPRI TR 107330-1996 section: 4.3.4.4.F, 4.6.2, 4.6.8, 6.3.1.E, 6.3.5, 8.6.1.C.

Test engineer shall record the Test Specimen for this test shown below:

Test Specimen(s) for the Surge Withstand Test

_____

_____

_____

_____

2.0 References

[redacted]

2.2 *HFC Quality Procedures*

QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-815	"Red-Line" Procedure

2.3 *Definitions, Abbreviations, and Acronyms*

2.3.1 Definitions

Coupling network - Electrical circuit for transferring energy from one circuit to another.

Test Specimen – HFC-6000 control system components configured for NRC qualification tests

2.3.2 Abbreviations and Acronyms

HFC	Doosan HF Controls/HF Controls
NRC	Nuclear Regulatory Commission
RTD	Resistance-Temperature Detector
TC	Thermocouple
TSAP	Test Specimen Application Program

3.0 Test Prerequisites

3.1 *Test Equipment Required*

In addition to the test equipment supplied by the laboratory, the following equipment will be required by HFC personnel to perform this test:

- [redacted]
-
-
-

Use attachment 7.1 to log the actual test equipment used for this test.

3.2 *Test Waveform Requirements*

The power surge waveform for the tests defined in the following table:

Table 1. Power Surge Waveforms

The waveforms described in table 1 are from NRC RG 1.180 which are typical environmental conditions for power surges in a nuclear power plant. IEEE Std C62.45-1992 describes the associated test methods and equipment to be employed when performing the surge tests.

IEEE Std C62.41-1991 describes location categories and exposure levels that define applicable amplitudes for the surge waveforms that should provide an appropriate degree of SWC. This test procedure uses Category B as described in IEEE Std C62.41-1991. See the following table:

Table 2. Surge Withstand Levels

Test personnel shall allow 30 seconds to 120 seconds pause in applying successive pulses.

3.3 *Environmental Conditions*

The test will be conducted in a mild environment without temperature or humidity stress conditions being imposed. The normal operating environment for the Test Specimen shall be in ambient conditions.

3.4 *Test Personnel*

The Surge Withstand tests will be conducted at a certified laboratory. Test personnel at the certified laboratory will conduct the tests and HFC test engineers will monitor the system and record the test results.

3.5 *Red-Line Policy*

Entering red-line corrections into a test procedure shall be done in accordance with WI-ENG-815 "Red-Line Procedure".Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.6 *Test Specimen Setup*

Equipment or system setup is project-specific to the test specimen. Test engineer shall execute the Pre-Test test procedure in section 4.1 for validating the setup of the test specimen.

3.7 *Test Specimen Specific Test Procedure*

The test engineer shall request the Operability Test Procedure and Prudency Test Procedure for the Test Specimen(s) from Document Control and ensure the revision is the latest from the Quality Department. Complete attachment 7.2 for the required test procedures for the test specimen.

3.8 *Surge Withstand Test Points*

The Surge Withstand test points are also project-specific to the test specimen. The test engineer shall use attachment 7.2 to get the Surge Withstand test points from Engineering Department and approved by the Quality Department for the test specimen before executing this test.

4.0 Surge Withstand Test Sequence

Test Specimen(s): _____

4.2 *Test Points*

Test points for the Test Specimen(s) for this test shall include the minimum of the following points (EPRI 107330 section 4.6.2) provided that the test specimen has the available test points:

4.3 *Test Execution*

The test engineer at the laboratory will apply the surge waveforms described in section 3.2 across each test point listed in attachment 7.2. The HFC test engineer will verify and certify setup for each test case. Following application of each test waveform, the HFC test engineer will examine performance of the Test Specimen(s) to identify the scope and nature of any component failures. The following tests apply only if the associated I/O cards are available for the Test Specimen.

4.3.1 Power Supply Test

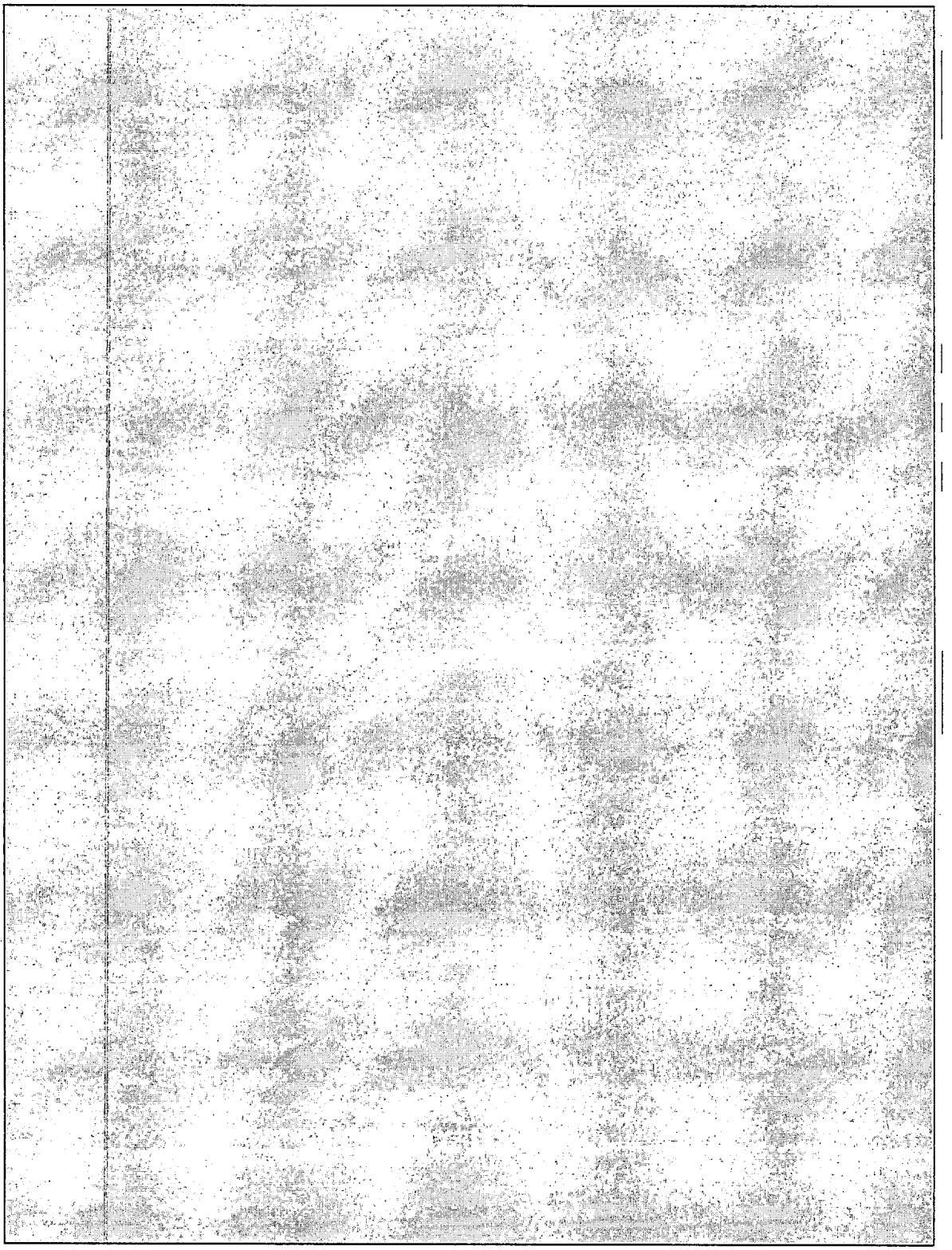
4.3.2.2 DO Solid State Channels

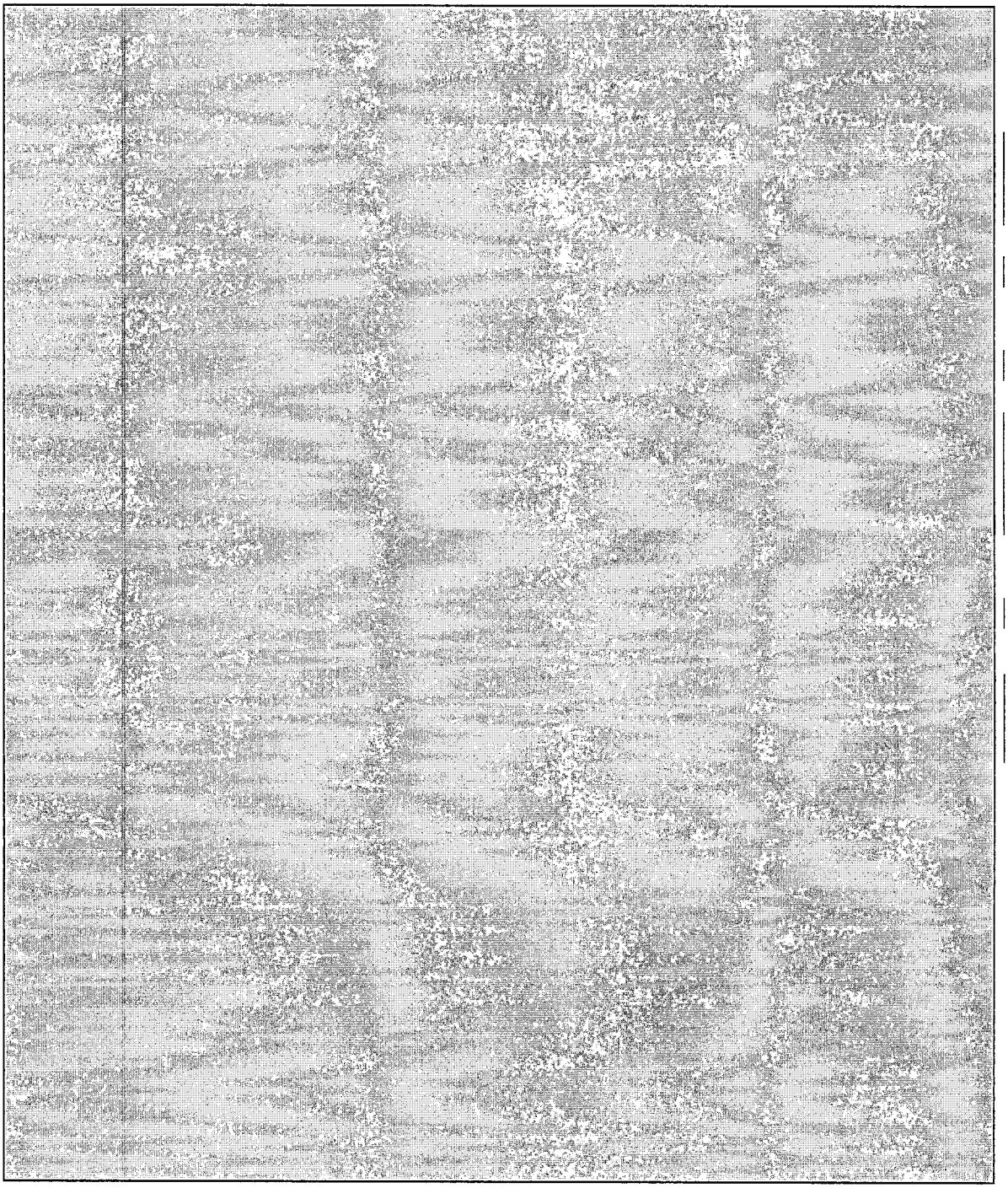
4.3.3 DI Common Terminals

4.3.3.2 One DI Common and Power Supply Ground

4.3.4 Analog Common Terminals

4.3.4.2 AI 0- to 5- vdc Common Terminal





5.0 Acceptance Criteria

The test waveforms are described in section 3.2. General acceptance criteria are the Test Specimen shall continue operating satisfactorily during and after application of the test waveforms without disruption of backplane signals or other data that could disable the capability of generating a trip. Specific acceptance criteria for each component subjected to the surge waveform shall be as follows:

- Application of surge waveform shall not damage any other, component, or channel other than those specific modules or circuits under test.

- Channels or modules other than the one under test continue to operate within normal accuracy limits for those modules during and after application of the test waveform.

- Failure of a single controller of the redundant pair will not be considered a failure condition if the backup controller assumes normal operation for the Test Specimen.

- Failure of the particular channel or circuit under test will not be considered a failure of the Test Specimen if the circuit (e.g., power module) is redundant, if the failure does not disrupt overall operation of the Test Specimen, or the failure does not propagate to other channels or circuits.

Application of the test waveforms may cause one or more modules, components, or individual I/O channels to fail. The HFC test engineer shall make detailed records of each failure and evaluate the consequences of that failure as follows:

6.0 QA Records

The following documentation shall be generated during the environmental test. These documents will be considered QA records in accordance with QPP 17.1, "Quality Records".

- Pre-Test Results Records:
    - TSAP Validation (Functional) Test Record
    - SOE files and HAS data for the automated tests.
- All completed attachments of this procedure, including all approved list of test points
- Completed test procedure signoffs in each of the test procedure documents.
- Completed test result records appended to this document.
- Alarm log file from the remotes folder

7.0 Attachments

7.1 Test Equipment Log

7.2 Surge Withstand Test Points

7.3 Pre-Test Test Record

7.4 Power Supply Test Results

7.5 DO Channels Test Results

7.6 DI Channels Test Results

7.7 AI Input 4- to 20-mA Common Terminal Test Results

7.8 AI Input 0- to 5- vdc Common Terminal Test Results

7.9 RTD Common Terminal Test Results

7.10 TC Common Terminal Test Results

7.11 Pulse Card Common Terminal Test Results

Attachment 7.1– Surge Withstand Test Equipment Log

Test Equipment	Instrument ID	Calibration Due Date

Test Engineer/Date

Attachment 7.2 – Surge Withstand Test Points

Test Specimen: _____

Equipment List

Quantity	Modular Type	Description	Cabinet Location

Required Documents

Operability Test Procedure	Prudency Test Procedure

_____
Test Engineer/Date

_____
Director of Quality or Designee / Date

Attachment 7.2 – Surge Withstand Test Points (Continued)

Section A – Power Supply Test Points

Test Points
Power Lines

Section B – DO Channel Points

1. **DO Relay Channels**

DO Test Points

2. **DO Solid State Channels**

DO Test Points

Section C – DI Channel Points

1. **Two DI Common Terminals**

DI Test Points	

2. **DI Common and Power Supply Ground**

DI Test Points

_____

Test Engineer/Date

_____

Approval/Date

Attachment 7.2 – Surge Withstand Test Points (Continued)

Test Specimen: _____

Section D – AI/AO 4- to 20-mA Common Channels

AI Test Points		

Section E – AI 0- to 5- vdc Common Channels

0- to 5- vdc AI Test Points		

Section F – RTD Channels

RTD AI Test Points							

Section G – TC Channels

TC AI Test Points							

Section H – Pulse Card Channels

1. **AI4K**

AI4K Test Points	

2. **AI4K2**

AI4K Test Points	

_____

Test Engineer/Date

_____

Approval/Date

Attachment 7.3 – Pre-Test Record

Test Specimen: _____

Item	Description	Initial
1	Power Supply Modules Records:	

Type	Measured Output

_____

2 Communication link error count record

ICL error count: _____

C-Link error count: _____

_____

3 Alarms which cannot be cleared:

_____

_____

_____

_____

SOE, HAS Files for Automated Operability and Prudency Test:

_____

_____

_____

_____

Test Engineer/Date

Attachment 7.4 – Power Supply Test Results

Test Specimen: _____ **Power Supply Module:** _____

Power supply output voltage before surge test: _____

Item	Description	Initial
1	Ring Wave at 2kV • Power supply output voltages after surge test: _____ • Alarm condition triggered by surge test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	_____
	Ring Wave at 4kV • Power supply output voltages after surge test: _____ • Alarm condition triggered by surge test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	
2	Combination Wave at 2kV • Power supply output voltages after surge test: _____ • Alarm condition triggered by surge test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	_____
	Combination Wave at 4kV • Power supply output voltages after surge test: _____ • Alarm condition triggered by surge test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	

Describe any failures noted: _____

_____

_____
Test Engineer/Date

Attachment 7.4 – Power Supply Test Results (Continued)

Test Specimen: _____ **Power Supply Module:** _____

Item	Description	Initial
3	EFT at 2kV • Power supply output voltages after surge test: _____ • Alarm condition triggered by surge test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	_____
	EFT at 4kV • Power supply output voltages after surge test: _____ • Alarm condition triggered by surge test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	_____

Describe any failures noted: _____

_____

_____

_____
Test Engineer/Date

Attachment 7.5 – DO Channels Test Results

Test Specimen: _____ **DO Relay Channel: DO,** _____

Item	**Description**	**Initial**
1	Ring wave with relay deenergized	_____

Test signal at 2kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

2 Ring wave with relay energized _____

Test signal at 2kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

SOE files: _____

Describe any failures noted: _____

_____

_____
Test Engineer/Date

Attachment 7.5 – DO Channels Test Results (Continued)

Test Specimen: _____ DO Relay Channel: DO, _____

Item	Description	Initial
3	Combination wave with relay deenergized	_____

Test signal at 2kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

4 Combination with relay energized _____

Test signal at 2kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

SOE files: _____

Describe any failures noted: _____
_____

_____
Test Engineer/Date

Attachment 7.5 – DO Channel Test Results (Continued)

Test Specimen: _____ DO Solid State Channel: DO, _____

Item	Description	Initial
1	Ring wave – TRUE status	_____

Test signal at 2kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

2 Ring wave – FALSE status _____

Test signal at 2kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

SOE files: _____

Describe any failures noted:

_____

_____
Test Engineer/Date

Attachment 7.5 – DO Channel Test Results (Continued)

Test Specimen: _____ DO Solid State Channel: DO, _____

Item	Description	Initial
3	Combination wave – TRUE status	_____

Test signal at 2kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

4 Combination wave – FALSE status _____

Test signal at 2kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

SOE files: _____

Describe any failures noted:

_____

_____
Test Engineer/Date

Attachment 7.6 – DI Channel Test Results

Test Specimen: _____

Two DI Common Terminals

Item	Description	Initial
1	Ring wave: DI, _____ to DI, _____ Test signal at 2kV • Alarm condition triggered by test signal? _____ • Other channel affected by test? _____ • Other module affected by test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____ Test signal at 4kV • Alarm condition triggered by test signal? _____ • Other channel affected by test? _____ • Other module affected by test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	_____
2	Combination wave: _____ to _____ Test signal at 2kV • Alarm condition triggered by test signal? _____ • Other channel affected by test? _____ • Other module affected by test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____ Test signal at 4kV • Alarm condition triggered by test signal? _____ • Other channel affected by test? _____ • Other module affected by test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	_____

SOE files: _____

Describe any failures noted: _____

_____
Test Engineer/Date

Attachment 7.6 – DI Channel Test Results (Continued)

Test Specimen: _____

Power Supply Ground to DI Common

Item	Description	Initial
1	Ring wave: DI, _____ Test signal at 2kV • Alarm condition triggered by test signal? _____ • Other channel affected by test? _____ • Other module affected by test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____ Test signal at 4kV • Alarm condition triggered by test signal? _____ • Other channel affected by test? _____ • Other module affected by test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	_____
2	Combination wave: DI, _____ Test signal at 2kV • Alarm condition triggered by test signal? _____ • Other channel affected by test? _____ • Other module affected by test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____ Test signal at 4kV • Alarm condition triggered by test signal? _____ • Other channel affected by test? _____ • Other module affected by test? _____ • Alarm condition cleared after surge test? _____ • Time of test _____	_____

SOE files: _____

Describe any failures noted: _____

_____
Test Engineer/Date

Attachment 7.7 – AI/AO 4- to 20-mA Common Terminal Test Results

Test Specimen: _____

Power Supply Ground to the indicated AI Channel

Item	Description	Initial
1	Ring wave test signal – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

SOE, HAS files: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.7 – AI/AO 4- to 20-mA Common Terminal Test Results (Continued)

Test Specimen: _____

Power Supply Ground to the indicated AI Channel

Item	**Description**	**Initial**
2	Combination wave – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

SOE, HAS files: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.8 – AI Input 0- to 5-vdc Common Terminal Test Results

Test Specimen: _____

Power Supply Ground to the indicated AI Channel

Item	Description	Initial
1	Ring wave – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

SOE files: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.8 – AI Input 0- to 5-vdc Common Terminal Test Results (Continued)

Test Specimen: _____

Power Supply Ground to the indicated AI Channel

Item	**Description**	**Initial**
2	Combination wave – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

SOE files: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.9 – RTD Common Terminal Test Results

Test Specimen: _____

Power Supply Ground to the indicated RTD AI Channel Common

Item	Description	Initial
1	Ring wave – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

HAS files: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.9 – RTD Common Terminal Test Results (Continued)

Test Specimen: _____

Power Supply Ground to the indicated RTD AI Channel Common

Item	Description	Initial
2	Combination wave – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Record time during which test was run: _____

HAS files: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.10 – TC Common Terminal Test Results

Test Specimen: _____

Power Supply Ground to the indicated TC AI Channel Common

Item	Description	Initial
1	Ring wave – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Record time during which test was run: _____

HAS files: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.10 – TC Common Terminal Test Results (Continued)

Test Specimen: _____

Power Supply Ground to the indicated TC AI Channel Common

Item	Description	Initial
2	Combination wave – AI, _____	_____

Test signal at 2kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV
- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Record time during which test was run: _____

HAS files: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.11 – Pulse Card Common Terminal Test Results

Test Specimen: _____

Power Supply Ground to the indicated AI4K Channel Common

Item	Description	Initial
1	Ring wave – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.11 – Pulse Card Common Terminal Test Results (Continued)

Test Specimen: _____

Power Supply Ground to the indicated AI4K Channel Common

Item	Description	Initial
2	Combination wave – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Record time during which test was run: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.11 Pulse Card Common Terminal Test Results (Continued)

Test Specimen: _____

Power Supply Ground to the indicated AI4K2 Channel Common

Item	Description	Initial
1	Ring wave test signal – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Record time during which test was run: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

Attachment 7.11 Pulse Card Common Terminal Test Results (Continued)

Test Specimen: _____

Power Supply Ground to the indicated AI4K2 Channel Common

Item	Description	Initial
2	Combination wave – AI, _____	_____

Test signal at 2kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Test signal at 4kV

- Alarm condition triggered by test signal? _____
- Other channel affected by test? _____
- Other module affected by test? _____
- Alarm condition cleared after surge test? _____
- Time of test _____

Record time during which test was run: _____

Describe any failures noted:

_____

_____

_____
Test Engineer/Date

HF Controls

HFC-6000 Control System

EPRI TR 107330 Qualification Program

Class 1E Isolation Test Procedures

TP901-200-07 Rev D

Effective Date 3/23/2011

Author Yang Lu

Reviewer Ivan Chow

Approval Charles McKinney

[XXXXXXX]

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Revision History

Date	Revision	Author	Changes
6/25/2010	A	I. Chow	Initial Revision
6/29/10	B	I. Chow	Revised to make consistent format across different qualification test procedures.
7/23/10	C	I. Chow	Revised to use Pre-Test for validating the system setup.
3/22/11	D	Y. Lu	Changes made per red-line mark-up. Refer to CR 2010-0259

Table of Contents

Section **Title** **Page**

1.0 PURPOSE AND SCOPE **3**

2.0 REFERENCES **3**
2.1 Industrial Standards 3
2.2 HFC Quality Procedures 3
2.3 Definitions, Abbreviations, and Acronyms 4

3.0 TEST PREREQUISITES **4**
3.1 Test Equipment Required 4
3.2 Test Personnel 5
3.3 Red-Line Policy 5
3.4 Channel-To-Channel Isolation 5
3.5 Test Specimen Setup 6
3.6 Precautions 6
3.7 Test Specimen Specific Test Procedure 6
3.8 Equipment to be Tested/Isolation Test Points 6

4.0 ISOLATION TEST SEQUENCES **9**
4.1 Pre Test 9
4.2 Test Execution 10

5.0 ACCEPTANCE CRITERIA **13**

6.0 QA RECORDS **15**

7.0 ATTACHMENTS **15**
Attachment 7.1 – Isolation Test Equipment Log 16
Attachment 7.2 – Equipment List and Isolation Test Points 17
Attachment 7.3 – Isolation Pre-Test Record 21
Attachment 7.4 – Isolation Test Results 22

1.0 PURPOSE AND SCOPE

The HFC-6000 control system (Test Specimen) is designed to operate in a wide variety of industrial applications. The control system hardware may be installed both in an electrical equipment room and at various other locations near the equipment under control. When I/O chassis are physically located in a remote location with respect to the controller hardware, they will be connected to the controller by means of a dedicated fiber-optic communication link. This link will provide the mechanism for ensuring physical and electrical isolation between a Class 1E controller and all non-Class 1E equipment in an installation. This document covers specific testing to demonstrate two categories of isolation:

- Channel-to-channel isolation of I/O ports under ordinary operation
- Class 1E to non-Class 1E isolation.

The following references in the EPRI TR-107330 standard define the content and scope for this test procedure: 4.3.2, 4.3.3, 4.3.4.3.E, 4.3.4.4.E, 4.6.4, 4.6.8, 6.3.6, 8.6.1.C.

The procedures listed in this document describe the steps of performing the isolation tests for a qualifying test specimen.

To execute this test, a control copy of this procedure shall be obtained from document control.

Test engineer shall record the Test Specimen for this test shown below:

Test Specimen(s) for the Isolation Test

_____

_____

_____

_____

2.0 REFERENCES

2.1 *Industrial Standards*

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996
IEEE 384	Standard Criteria for Independence of Class 1E Equipment and Circuits, 1981

2.2 *HFC Quality Procedures*

QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-815	"Red-line" Procedure

2.3 *Definitions, Abbreviations, and Acronyms*

2.3.1 Definitions

Coupling network - A set of input channels that share a common ground. A group may consist of a single channel or any subset of the total number of channels on a particular input card.

Test Specimen – HFC-6000 control system components configured for NRC qualification tests.

2.3.2 Abbreviations and Acronyms

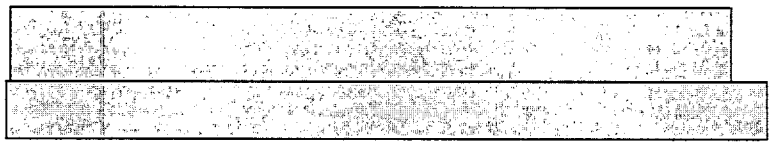
AI	Analog Input
AO	Analog Output
CSM	Control Switch Module
DI	Digital Input
DO	Digital Output
HAS	Historical Archiving System
HPAT	HFC Plant Automated Tester
I/O	Input/Output
LAN	Local Area Network
LED	Light Emitting Diode
M/A	Manual/Automatic
MCL	Master Configuration List
RTD	Resistance Thermal Detector
TC	Thermocouple
TSAP	Test System Application Program

3.0 TEST PREREQUISITES

The following paragraphs define the conditions required to begin the isolation tests. These tests will be conducted at a certified laboratory. Test personnel at the laboratory will apply the test waveforms and HFC personnel will monitor the functional operations of the Test Specimen and look for any deviations during the test.

3.1 *Test Equipment Required*

Test equipment required to generating the discharge will be provided by the laboratory. Specific test requirement needed for the test specimen are listed in the corresponding Operability Test Procedure for the test specimen. In addition, the following equipment is required:



The actual test equipments used shall be logged in attachment 7.1.

3.2 *Test Personnel*

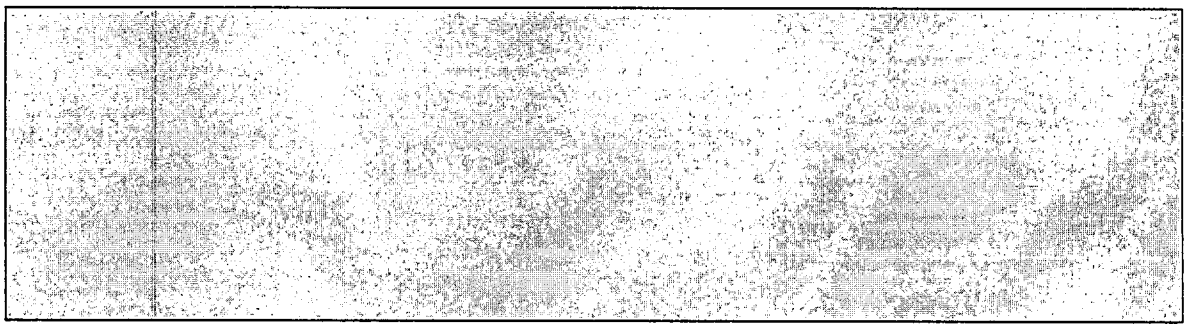
Isolation testing will be at a certified laboratory. The laboratory test personnel will conduct all functional tests, and certify all test records produced during the test period. HFC test personnel will certify the test execution done with this test procedure.

3.3 *Red-Line Policy*

Entering red-line corrections into a test procedure shall be done in accordance with WI-ENG-815 "Red-Line Procedure". Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.4 *Channel-To-Channel Isolation*

The following tests cover channel-to-channel isolation tests applicable to each of the individual I/O card types. The primary purpose of these tests is to demonstrate immunity to channel-to-channel interference during a design basis event. The test signals will be applied to I/O channels both in the Class 1E portion of the Test Specimen and to I/O channels in the expansion rack. The general approach to testing will consist of two phases:



3.4.1 Normal Channel-to-Channel Isolation Test Signal

The minimum acceptable level of channel-to-channel isolation for normal operation differs for each card type. The following list presents the minimum acceptable level of according to EPRI TR 107330 isolation on a channel-to-channel or group-to-group basis.

- ±30 v peak for AI channels on a group basis
- 40 v peak for 24-vdc discrete inputs on a group basis
- 40-vdc for pulse input channels on a group basis
- 600 v peak applied for 30 seconds for 120-vac discrete output channels on a group basis
- Twice the nominal output voltage for discrete output channels and serial I/O channels on a group basis.

3.4.2 Class 1E Isolation Test Signal

This isolation test refers to demonstration of electrical isolation of class 1E control equipment from non-class 1E equipment as well as isolation between different Class 1E channels. The minimum signal levels specified by EPRI TR 107330 for this test will be as follows:

- 600 vac applied for 30 seconds
- 250 vdc applied for 30 seconds

3.5 *Test Specimen Setup*

Equipment or system setup is project-specific to the test specimen. Test engineer shall execute the Pre-Test test procedure in section 4.1 for validating the setup of the test specimen.

3.6 *Precautions*

Surge testing involves large amplitude voltage and current transient signals that can pose significant risk to personnel and equipment. The following precautions shall be observed throughout execution of the test sequence to avoid injury to personnel and unnecessary damage to equipment.

- Voltage levels used for Class 1E isolation testing are potentially lethal. Only qualified personnel should perform such tests with all applicable safety precautions enforced.
- Catastrophic failure of equipment under test can result in explosion or fire. The test area should be equipped with fire protection equipment as well as hand-held fire extinguishers.
- Test personnel should not monitor the Test Specimen directly while the test signals are being applied.

3.7 *Test Specimen Specific Test Procedure*

The test engineer shall request the Operability Test Procedure and Prudency Test Procedure for the Test Specimen(s) from Document Control and ensure the revision is the latest from the Quality Department. Complete attachment 7.2 for the required operability and prudency test procedures for the test specimen.

3.8 *Equipment to be Tested/Isolation Test Points*

Equipment to be tested and the isolation test points are also project-specific to the test specimen. The test engineer shall use attachment 7.2 to get equipment list and the isolation test points from the Engineering Department and approved by the Quality Department for the test specimen before executing this test.

3.8.1 Channel-to Channel (Non-Class 1E) Isolation

The following test cases list the minimum channel-to-channel isolation requirement for each type of I/O card as specified in EPRI TR-107330.

ISO1. For current input (4 to 20 mA) and voltage input (0 to 5 v) AI modules, group-to-group isolation shall be at least ±30 v peak.

ISO2. For RTD input channels, group-to-group isolation shall be at least ±30 v peak.

ISO3. For thermocouple input channels, group-to-group isolation shall be at least ±30 v peak.

ISO4. For 120-vac discrete input channels, group-to-group isolation shall be at least 600v peak.

ISO5. For 125-vdc discrete input channels, group-to-group isolation shall be at least 600v peak.

ISO6. For 48-vdc discrete input channels, group-to-group isolation shall be at least 100vdc.

ISO7. For pulse input channels, group-to-group isolation shall be at least 40 vdc.

ISO8. For analog output channels, group-to-group. Module-to-module, and module-to-backplane isolation shall be a minimum of 600 vac and 250 vdc applied for 30 seconds.

ISO9. For solid-state 120-ac discrete output channels, group-to-group isolation shall be at least 600 v peak.

ISO10. For solid-state 125-dc discrete output channels, group-to-group isolation shall be at least twice the nominal output voltage (250 vdc).

ISO11. For serial I/O channels, group-to-group isolation shall be at least 300 vdc applied for 30 seconds.

ISO12. For relay discrete output channels, group-to-group isolation shall be at least 600 v peak.

3.8.2 Class 1E Isolation

The following test cases list the Class 1E to non-Class 1E isolation requirements for each type of I/O channel specified in EPRI TR-107330. A representative channel from each type of I/O module in the Test Specimen will be exposed to the indicated level of test signal(s).

I/O modules having more than one type of channel on the same hardware assembly shall be subjected to the test signal for both channel types.

1E01. For current input (4 to 20 mA) and voltage input (0 to 5 v) AI modules, 600 vac and 250 vdc for 30 seconds each.

1E02. For RTD input channels, 600 vac and 250 vdc for 30 seconds each.

1E03. For thermocouple input channels, 600 vac and 250 vdc for 30 seconds each.

1E04. For 120-vac discrete input channels, 600 vac and 250 vdc for 30 seconds each.

1E05. For 125-vdc discrete input channels, 600 vac and 250 vdc for 30 seconds each.

1E06. For 48-vdc discrete input channels, 600 vac and 250 vdc for 30 seconds each.

1E07. For pulse input channels, 600 vac and 250 vdc for 30 seconds each.

1E08. For analog output channels, 600 vac and 250 vdc for 30 seconds each.

1E09. For solid-state ac discrete output channels, 600 vac and 250 vdc for 30 seconds each.

1E010. For solid-state dc discrete output channels, 600 vac and 250 vdc for 30 seconds each.

1E011. For serial I/O channels, 600 vac and 250 vdc for 30 seconds each.

1E012. For relay discrete output channels, 600 vac and 250 vdc for 30 seconds each.

4.0 ISOLATION TEST SEQUENCES

Test Specimen(s): _____

4.1 *Pre Test*

Pre-Test is completed successfully: _____

Test Engineer/Date

4.2 *Test Execution*

4.2.1 Test Preparation

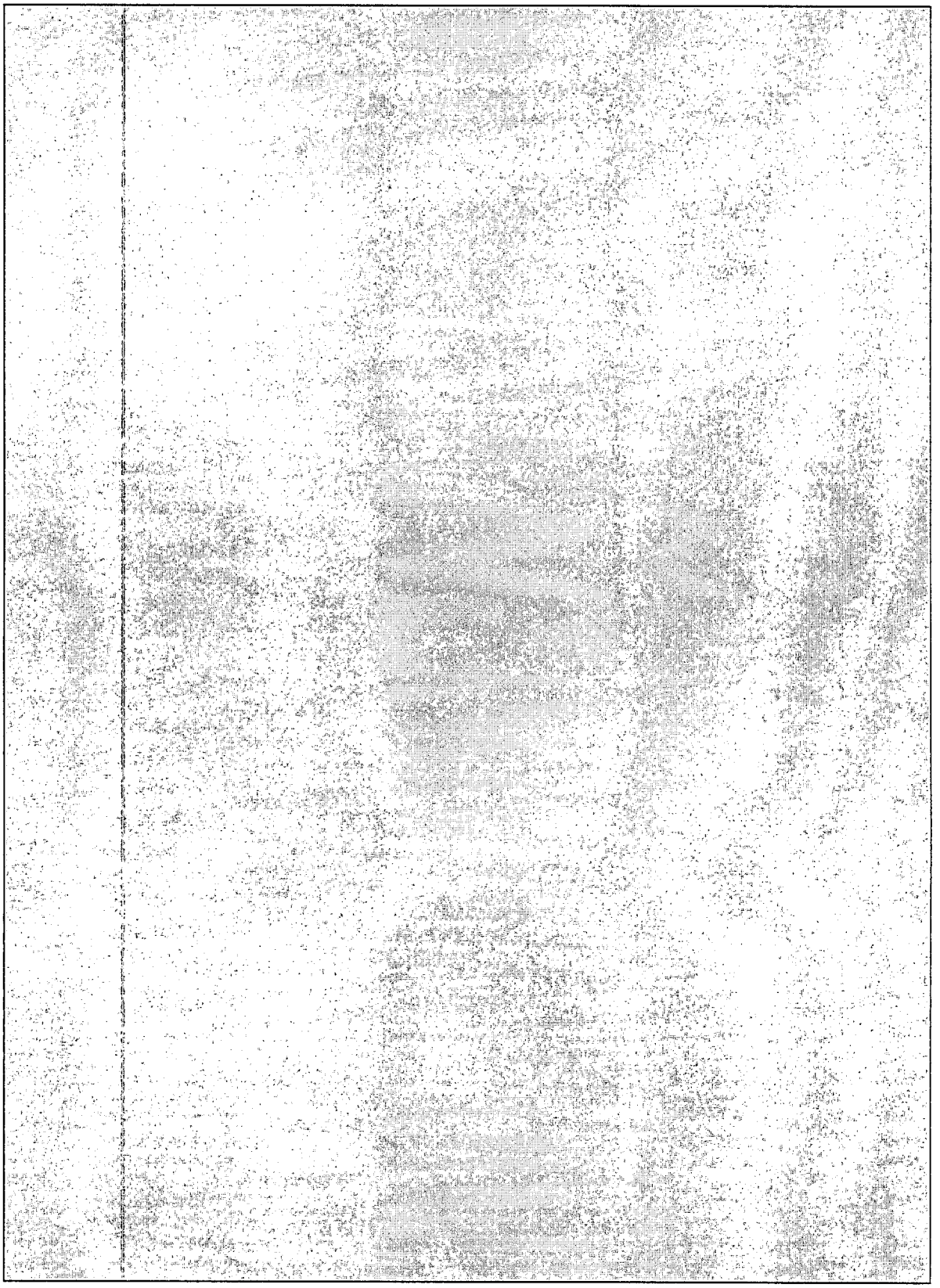
The automated Operability and Prudency tests will be set to be running during execution of the isolation test. In addition, the SOE and HAS loggers will be used to monitor static points, and the alarm process utility will be used to monitor system operation for failure conditions.

4.2.2 Test Execution

The purpose of this test is to determine the level of isolation provided by each I/O channel type in the Test Specimen. The approved representative I/O channels will be subjected to the Class 1E isolation test waveforms **first**. If a channel does not pass the test, then we will switch to the Channel-to-Channel Non Class 1E Isolation test. If the channel successfully passes the Channel-to-Channel Non-Class 1E Isolation test, the magnitude of the test signal will be increased by steps up to the minimum limits for the Non Class 1E isolation acceptance criteria. Passing of the minimum acceptance criteria of the Non Class 1E/Class 1E isolation test voltages will qualify that channel as a Non-Class 1E/Class 1E isolation protected channel.

CAUTION

When applying the test signal, ensure that all other disconnected wires in the harness are held away from the test signal leads. Arcing from the test leads to the I/O harness could result in damage to the external test



5.0 ACCEPTANCE CRITERIA

Acceptance criteria for each circuit type to be tested are listed in the following tables:

Table 1 – Class 1E Isolation

Test Case	Channel Type	Test Signal	Acceptance Criteria
1E01	4-20 mA AI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1E02	RTD AI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1E03	TC AI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1E04	120 vac DI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1E05	125 vdc DI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1E06	48 vdc DI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1E07	Pulse Input	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1E08	4-20 mA AO	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected No other channel on the module under test shall change by more than 0.05%.
1E09	Solid-state ac DO	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected
1E10	Solid-state dc DO	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected
1E11	Serial Channel	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected
1E12	Relay DO	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected

Table 2 – Normal Channel-to-Channel Isolation

Test Case	Channel Type	Test Signal	Acceptance Criteria
All			No disruption in operation for any other channel on the card or any other module in the chassis occurs.
ISO1	4-20 mA AI	±30 v peak group-to-group isolation	No channel other than the one under test changes by more than 0.05%.
ISO2	RTD AI	±30 v peak max group-to-group isolation	No channel other than the one under test changes by more than 0.05%.
ISO3	TC AI	±30 v peak max group-to-group isolation	No channel other than the one under test changes by more than a 0.54° F (0.3° C).
ISO4	120 vac DI	600 v peak group-to-group isolation	No channel on a different group other than the one under test exhibits invalid transitions.
ISO5	125 vdc DI	600 v peak group-to-group isolation	No channel on a different group other than the one under test exhibits invalid transitions
ISO6	48 vdc DI	100 vdc group-to-group isolation	No channel on a different group other than the one under test exhibits invalid transitions
ISO7	Pulse Input	40 vdc group-to-group isolation	No channel on a different group other than the one under test exhibits invalid transitions
ISO8	4-20mA AO	600 vac max for 30 sec 250 vdc max for 30 sec	No channel other than the one under test changes by more than 0.05% while the signal is applied.
ISO9	Solid-state ac DO	600 v peak group-to-group isolation	No disruption in operation for any other channel on the card occurs.
ISO10	Solid-state dc DO	Twice nominal output voltage group-to-group isolation	No disruption in operation for any other channel on the card occurs
ISO11	Serial channel	300 vdc peak max port-to-port isolation applied for 30 seconds	No disruption in operation for any other channel, the main processor, or any other module occurs
ISO12	Relay DO	600 v peak group-to-group isolation	No disruption in operation for any other channel on the card occurs

6.0 QA RECORDS

The following documentation shall be generated during the isolation test. These documents will be considered QA records in accordance with QPP 17.1, "Quality Records".

- Pre-Test Results Records:
  - TSAP Validation (Functional) Test Record
  - SOE files and HAS data for the automated tests.
- Completed test procedure signoffs in each of the test procedure documents.
- Completed test result records appended to this document.
- SOE and HAS files covering the period during the isolation test
- Alarm log file for the period during the isolation test
- Post-Test Results Records:
  - SOE files and HAS data for the automated tests.

7.0 ATTACHMENTS

Attachment 7.1 – Test Equipment Log
Attachment 7.2 – Isolation Test Points Form
Attachment 7.3 – Pre-Test Test Result Record
Attachment 7.4 – Isolation Test Result Record

Attachment 7.1 – Isolation Test Equipment Log

Test Equipment	Instrument ID	Calibration Due Date

_____

Test Engineer/Date

Attachment 7.2 – Equipment List and Isolation Test Points

Test Specimen: _____

Section A: Equipment List

Quantity	Modular Type	Description	Cabinet Location

Required Documents

Operability Test Procedure	Prudency Test Procedure

_____
Test Engineer (Engineering)/Date

_____
Approval (Quality)/Date

Attachment 7.2 – Equipment List and Isolation Test Points (Continued)

Assigned Channel Range

Card	Description	Assigned Channel Range

_____
Test Engineer (Engineering)/Date

_____
Approval (Quality)/Date

Attachment 7.2 – Equipment List and Isolation Test Points (Continued)

Section B: Isolation Test Points

(If a specific test case is not applicable, mark N/A for the channels for that test case.)

Test Case	Test Channel		Alternate Channel		Monitor Channel ID
	Channel ID	Cable Contacts	Channel ID	Cable Contacts	
1E01 ISO1					
1E02 ISO2					
1E03 ISO3					
1E04 ISO4					
1E05 ISO5					
1E06 ISO6					

Author (Engineering)/Date

Approval (Quality)/Date

Attachment 7.2 – Isolation Test Points (Continued)

Test Specimen: _____

(If a specific test case is not applicable, mark N/A for the channels for that test case.)

Test Case	Test Channel		Alternate Channel		Monitor Channel ID
	Channel ID	Cable Contacts	Channel ID	Cable Contacts	
1E07 ISO7					
1E08 ISO8					
1E09 ISO9					
1E010 ISO10					
1E011 ISO11					
1E012 ISO12					

_____
Author (Engineering)/Date

_____
Approval (Quality)/Date

Attachment 7.3 – Isolation Pre-Test Record

Test Specimen: _____

Item	Description	Initial
1	Power Supply Modules Records:	

Type	Measured Output

_____

2 Communication link error count record

ICL error count: _____

C-Link error count: _____

_____

3 Alarms which cannot be cleared:

_____

_____

_____

_____

SOE, HAS Files, and Alarm Logs for Automated Operability and Prudency Test:

_____

_____

_____

_____
Test Engineer/Date

Attachment 7.4 – Isolation Test Results

Isolation Test Case: _____

Channel Under Test: _____

Item	Description	Initial
1	Test signal passed (applied 30 secs):	_____

DC (V)		AC (V)	
30	☐	30	☐
130	☐	130	☐
250	☐	230	☐
		330	☐
		430	☐
		530	☐
		600	☐

2 Disruption happens at: _____ _____

Describe the disruption:

_____
_____
_____

6 Channel is destructed at: _____ _____
Describe:

_____
_____
_____
_____

7 Class 1E Isolation Test: _____

600 VAC 30 seconds; 250 VDC 30 seconds

Pass ☐ No Pass ☐ ; Maximum Isolation AC: _____
Maximum Isolation DC: _____

SOE, HAS Files, and Alarm Logs for Automated Operability and Prudency Test:

_____

_____

_____
Test Engineer/Date