HF Controls

HFC-6000 Qualifying System

ERD111

Environmental Stress Retest Detail Report

TR901-200-03 Rev. A

Effective Date: 6/28/2011

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[ ]

Revision History

Date	Revision	Author	Changes
6/24/11	A	I. Chow	Initial revision for detail environmental retest results at Environmental Testing Laboratory for ERD111 Test Specimen.

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1.0 Introduction

1.1 *Purpose*

An environment stress retest was performed for the ERD111 test specimen for resolving the open items listed in the safety evaluation report (SER) issued by US Nuclear Regulatory Commission (NRC) for Doosan HF Controls (HFC) HFC-6000 platform. This report contains an analysis of the Operability tests (TP0402) that were executed at various times during the environmental stress retest. The primary purpose for these tests was to provide objective evidence that the ERD111 test system continued to operate within specified limits before, during, and after being subjected to environmental stress conditions.

1.2 *Scope*

The focus of this report is to address the open environmental stress items listed in the SER for HFC-6000 platform. Although there was enhanced equipment installed in the ERD111 test specimen, the test results described in this document are limited to those equipments listed in the SER.

2.0 References and Acronyms

2.1 *Industry References*

EPRI TR 107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996

2.2 *HFC References*

50040801	ERD111/ERD921 Power Distribution System Cabinet, Rev. D
50040901	Loop Layout Table of PCB Assemblies ERD111/TÜV, Rev. B
QPP 17.1	Quality Process Procedures – Quality Record
TP0402	ERD111 Operability Test, Rev. L
TP0403	ERD111 Prudency Tests, Rev. G
TP901-200-02	EPRI TR 107330 Environmental Stress Test Procedure, Rev. D
VV0414	ERD111 Master Configuration List, Rev. E
VV901-300-01	ERD111/ERD921 Qualification Master Test Plan, Rev B

2.3 *Acronyms*

EPRI	Electrical Power Research Institute
ERD111	Engineering R&D Project 111
HFC	Doosan HF Controls/HF Controls
HPAT	HFC Plant Automated Tester
HAS	Historical Archiving System
I/O	Input/Output
NRC	Nuclear Regulatory Commission
PLC	Programmable Logic Controller
RTD	Resistive Temperature Detector
SER	Safety Evaluation Report
SLC	Single Loop Controller

3.0 Testing Information

3.1 *Venues*

The environmental stress tests were conducted at the Environmental Testing Laboratory, an ISO/IEC 17025 certified laboratory. The laboratory is located at 11034 Indian Trail, Dallas, Texas 75229-3513.

The testing period was from July 1st, 2010 until July 17th, 2010.

3.2 *Test Specimen Equipment List*

The HFC-6000 modules installed in the ERD111 test specimen are listed in the following table.

Table 1 – ERD111 Test Specimen HFC-6000 Modules

Quantity	Modular Type	Description
4	**PS, Jasper 24V**	**600W 24V Power Supply**
1	Rack, Jasper PS	8-slot Jasper PS Rack, 19"
2	HFC-FOT06	Fiber-Optic Transmitter
4	**HFC-ILR06**	**I/O Link Repeater/Terminator**
1	**HFC-BPC01-19**	**Controller Chassis backplane**
2	**HFC-BPE01-19**	**Expander Chassis backplane**
1	HFC-BPC03-08	3 Loop, 8 inch backplane
2	**HFC-SBC06**	**Main Controller**
1	**HFC-DPM06**	**Dual-Ported Memory**
2	HFC-SCG06	Communication Gateway
1	HFC-DPM06BP	Backplane Connected DPM06
1	HFC-DO16C	Solid State Output Card
2	**HFC-DC33**	**Special Function Card (120 vac output)**
4	**HFC-DC34**	**Special Function Card (125-vdc output)**
1	HFC-DC35	Special Function Card (120 vac output)
2	**HFC-AI4K**	**Pulse Input Card**
1	HFC-AI4K2	Pulse Input Card
1	**HFC-AI16F**	**Analog Input Card (4- to 20 mA)**
1	HFC-AI16FD	Analog Input Card (4- to 20 mA) (DSP)
2	**HFC-AO8F**	**Analog Output Card (4- to 20 mA)**
1	HFC-AI8LD	Thermocouple Input Card
1	**HFC-AI8M**	**RTD Input Card, 100 ohm**
4	HFC-AC36	Analog Input/Output Board
2	HFC-PCC06	Serial Channel Card
7	**HFC-DI16I**	**Digital Input Card with SOE**
1	**HFC-DO8J**	**Relay Output Card**
6	HFC-DO16J	Relay Output Card

(Note: Modules listed in bold-faced font indicate that they are listed in HFC-6000 SER.)

Figure 1 shows the layout of the modules inside the qualification cabinet. Only racks and locations marked with "ERD111" apply to the HFC-6000 SER listed equipment.

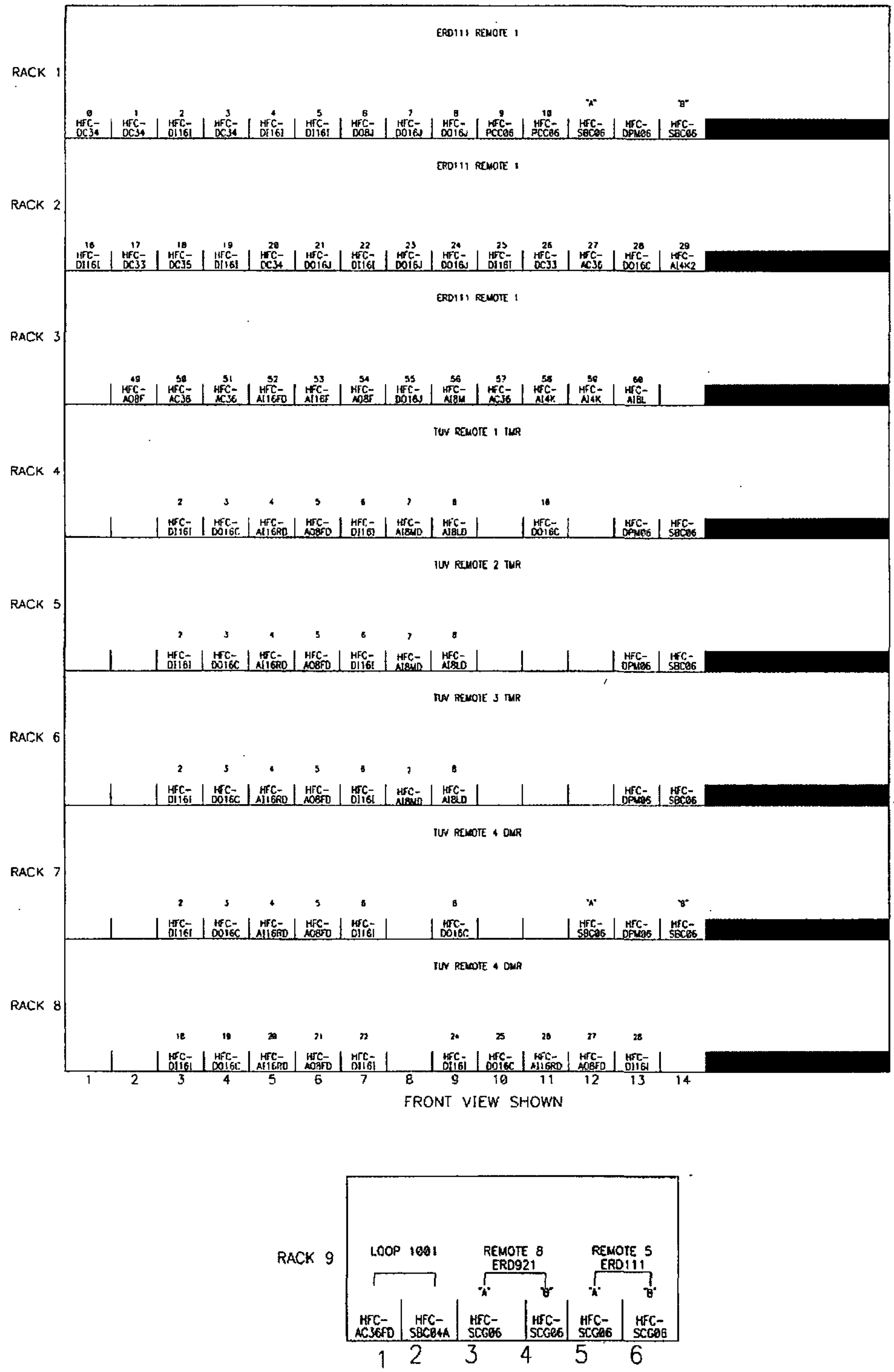

Figure 1 – Equipment Layout in the Cabinet

3.3 *Environmental Stress Validation Tests*

As specified in EPRI TR 107330-1996, operability checks or validation tests are required to ensure that the platform performs properly in various environment stress conditions as shown in Figure 2.

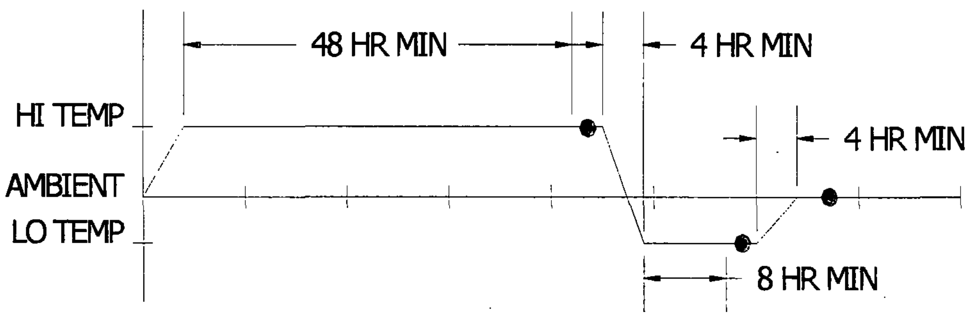

Figure 2 – Environmental Stress Test Profile

Note: The black dots on the graph designate the operability check points required by the standard.

High humidity ~90% during high temperature and low humidity ~5% during low temperature were maintained. In the rest of this report, the humidity conditions are implied by the temperature and will not be mentioned again.

These validation tests are grouped into operability and prudency tests in accordance with EPRI TR 107330. Refer to the standard for the details of these test descriptions.

3.3.1 Operability Tests

The following tests are required for the operability checks in accordance with EPRI TR 107330 as noted in Figure 2:

A. Accuracy

B. Response Time

C. Discrete Input and Output Operability

D. Communication Operability

E. Timer

F. Failure to complete scan detection

G. Failover Operability

H. Loss of Power

I. Power Interruption

J. Power Quality (Only performed after the end of high temperature testing period)

The required coprocessor operability tests were excluded because there is no coprocessor usage in HFC-6000 platform.

3.3.2 Prudency Tests

In addition to the operability tests, prudency tests are required only after the high temperature stress period in accordance with EPRI TR 107330-1996. The required burst of event tests (BOE) were divided into digital BOE and analog BOE tests. The digital BOE tests are also used for validating the discrete input/output operability of the test specimen. Detail test results and analyses are provided in the following section.

4.0 Test Results

During the environment stress retest, the time of exposure of the ERD111 test specimen to the high temperature/high humidity (HT/HH) was longer than 48 hours. The first set of operability tests not related to power supplies were performed after the initial exposure of 48 hours. In order not to disrupt the operations, operability tests related to power supplies and power quality were performed at the end of HT/HH exposure before ramping down to low temperature/low humidity. A set of prudency tests were also performed during the first operability checkpoint at the end of the initial 48 hours exposure of HT/HH. No anomalies for the ERD111 test specimen were found at any operability checkpoints. The stress profiles applied during the environmental tests are shown in the following figures.

Figure 3 – Profile of High Temperature Stress I during Operation

Figure 4 – Profile of High Temperature Stress II during Operation

Figure 5 – Profile of Low Temperature Stress during Operation

Note: After arriving to the Environmental Testing Laboratory (ETL), before starting the environmental stress tests, a pretest consisting of operability and prudency tests was performed. The purpose of the pretest was to validate the ERD111 test specimen was properly setup after it was disassembled at the HFC facility and shipped to the ETL. The pretest data were analyzed and were found satisfactory as compared to the baseline data collected at the HFC facility. Since the focus of this report is the performance data during the environmental stress periods, the pretest data and results are not presented.

As shown in the figures above, the complete ERD111 test specimen was subjected to an environmental stress profile more than the required stress profile shown in Figure 2. The period of stressing in the high elevated temperature of 60°C/140°F or higher was 218 hours instead of 48 hours. The period of stressing in low temperature of 4.4°C/40°F or lower was 10 hours instead of 8 hours. In addition, there were stress cycles before and after the high temperature and low temperature stresses. These additional stress cycles were performed for qualifying to a different standard.

The required operability and prudency tests at the end of high temperature stress in operation were performed after 48 hours of 60°C/140°F environmental stress on July 8. The extended high temperature stress period of 218 hours was related to a device which was not part of ERD111 test specimen. The low temperature stress exposure was conducted after 4 hours ramp down time after the 218 hours of the elevated high temperature. Operability tests were performed after an 8-hour of 4.4°C/40°F environment stress. After two stress cycles of 54°C and 4.4 °C, another operability check was performed at ambient temperature. The following sections provide the detail information of the test results performed during these periods.

4.1 *Operability Tests*

4.1.1 Accuracy

At least one channel of each analog device included in the ERD111 Test System was included in the analog accuracy tests. The specific channels and I/O cards covered are listed in Table 1.

Table 2 -- ERD111 Analog I/O Channels Covered by Accuracy Testing

Equipment Type	Channel Tested	Test Type
AI Accuracy Tests		
HFC-AI16F – 4 to 20 mA AI	[ ]	Manual and automated tests
HFC-AI8M – RTD Input	[ ]	Manual and automated tests
HFC-AI4K – Pulse Input	[ ]	Manual and automated tests
AO Accuracy Tests		
HFC-AO8F – 4 to 20 mA AO	[ ]	Automated test only
HFC-AO8F – 4 to 20 mA AO	[ ]	Manual and automated tests

All of the manual tests were executed during the Operability pre-qualification testing conducted at the HFC test facility before the test cabinet was placed in the environmental test chamber. The purpose of the manual tests was two fold:

- Demonstrate that the ERD111 analog hardware operated within specified calibration limits prior to the start of stress testing.

- Determine the magnitude of any systemic error introduced by the test hardware being used to control and log the automated test.

The automated tests were run during the pretest at HFC, prior to the start of the environmental stress test, and at various points during the environmental stress tests. Results from the automated tests were logged by an Historical Archiving System (HAS), which was running on a PC workstation that was external to the ERD111 test system.

The test configuration consists of a five-step algorithm running in both the HPAT and in the ERD111 TSAP. See Figure 6. The specific combination of hardware channels and software modules is illustrated in Figure 7. [

] The images of the AI channels were logged through HFC HAS server. The algorithm in the ERD111 test specimen drove AO channels to the HPAT whose values were logged through HFC HAS server.

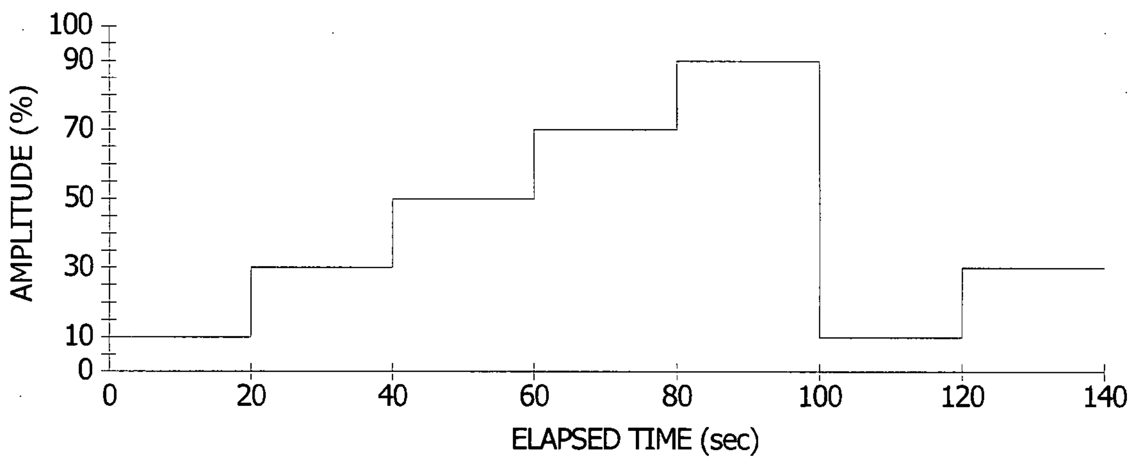

Figure 6 – Algorithm for 4- to 20mA Analog Channel Accuracy Test

Figure 7 – Automated AI/AO Test Arrangement

The bold BL points in these figures identify the point images that were logged while the test was running. Because of the additional hardware involved in the HPAT, correction factors need to be applied to the raw values of the analog channels. Based on the manual test results and indirect HPAT accuracy algorithm, the correction factors for the analog signals measured in the ERD111 test specimen is summarized in the following table.

Table 3 – Correction Factors for Analog Accuracy Tests

Interface Card:	**AI16F**	**AO8F**
Channel:	[ ]	[ ]
Analog Image:	[ ]	[ ]
10	[ ]	[ ]
30	[ ]	[ ]
50	[ ]	[ ]
70	[ ]	[ ]
90	[ ]	[ ]

The correction factor for AI16F was based on the results from the manual accuracy tests performed during the pre-qualification test phase. See pre-qualification test report for more details.

The automated analog accuracy I/O test was run before, during, and after environmental stress test. The following seven tables summarize the results obtained. The results shown in the table contain averaged values for each step level and include the appropriate correction factor from *Table 3*. Each step level of the algorithm lasted for 20 seconds, and each test run included from two to four repetitions of each level. Acceptance criteria for these channels as specified in TP0402 in accordance with EPRI TR 107330 are as follows:

4 to 20 mA AI Channels

During qualification test — Accuracy within ±0.35% of span over the entire range

4 to 20 mA AO Channels

During qualification test — Accuracy within ±0.32% of span over the entire range

4.1.1.1 AI16F

[ ] This log point was monitored throughout the operability tests performed at the end of the high temperature stress period, at the end of the low temperature stress period, and at the end of back to the ambient period.

The test data were analyzed and the accuracy results are listed in *Table 4*. In each step level of all testing periods, the accuracy of the AI16F measured was well within ±0.35% of span over the entire range. AI16F, therefore, meets the acceptance criteria of accuracy in an environmental stress profile in accordance with EPRI TR 107330.

Table 4 – HFC-AI16F [ ] Accuracy Test Results

Step Level	Raw Averaged Image	Corrected Average Value	% Accuracy
High Temperature Test Execution 1			
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]
High Temperature Test Execution 2			
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]
Low Temperature Test Execution 1			
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]
Low Temperature Test Execution 2			
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]
Return to Ambient Temperature Test Execution 1			
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]
Return to Ambient Temperature Test Execution 2			
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]

The following figure shows the input measurements of the AI16F continued to exhibit linearity in each environmental stress period

Figure 8 – AI16F Accuracy Data during the Environmental Stress Periods

During the temperature stress conditions, every channel under test exhibited some increase in error magnitude. The following results are notable:

- The HFC-AI16F channel generally remained within the ±0.35% accuracy limit during the high temperature phase, but exhibited its maximum error during the low temperature phase.

- The HFC-AI16F module exhibited accuracy range from 0.0889% to 0.157% during the environment stress periods.

4.1.1.2 AO8F

[

] This AO image was indirectly driven by an AO image from the HPAT. The log point was monitored throughout the operability tests performed at the end of the high temperature stress period, at the end of the low temperature stress period, and at the end of back to the ambient period.

The test data were analyzed and the accuracy results were listed in *Table 5*. In each step level of all testing periods, the accuracy of the AO8F measured was well within ±0.32% of span over the entire range. The AO8F, therefore, meets the acceptance criteria of accuracy in an environmental stress profile in accordance with EPRI TR 107330.

Table 5 – HFC-AO8F [ ] Accuracy Test Results

Average Source Value [ ]	Averaged Image [ ]	% Accuracy
High Temperature Test Execution 1		
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
High Temperature Test Execution 2		
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
Low Temperature Test Execution 1		
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
Low Temperature Test Execution 2		
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
Return to Ambient Temperature Test Execution 1		
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
Return to Ambient Temperature Test Execution 2		
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]

In addition, charting of the values at various environmental stress periods for the AO8F channel demonstrates that the card continued to exhibit linearity. See Figure 9.

Figure 9 – AO8F Accuracy Data during the Environmental Stress Periods

Accuracy of AO8F channels remained within the ±0.32% tolerance limit throughout the environmental stress tests.

4.1.1.3 AI8M

The ERD111 test system included one HFC-AI8M RTD input card that was calibrated to process input signals from 100-Ω platinum RTD. All eight channels were tested manually during the in-house execution of the pretest. [

] The following table summarizes the results of the automated test conducted during environmental stress testing.

Table 6 – Summary of HFC-AI8M Accuracy Results

Test Phase	Channel 1 ([ ])		Channel 2 ([ ])		Channel 8 ([ ])	
	Max.	Min.	Max.	Min.	Max.	Min.
High Temp 1	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
High Temp 2	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
Low Temp 1	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
Low Temp 2	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
Ambient 1	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]
Ambient 2	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]

Specified acceptance criteria for the RTD channels are as follows:

Qualification test limits ±2°C over entire range

Results during the environmental test are as follows:

[

]

The variations of the RTD input card were less than ±2°C from its measurement mean value. The AI8M has demonstrated it meets specified acceptance requirements for the range tested.

4.1.1.4 AI4K

The ERD111 test system included two HFC-AI4K pulse input cards that were calibrated to input pulse frequency up to 20 kHz. Channel 1 and channel 3 of one of these HFC-AI4K cards were tested manually during the in-house execution of the pre-qualification test. Due to the accessibility to the test chamber, a signal generator was used for providing a 200Hz test signal, 10% of the full range, to channel 1 of the HFC-AI4K card. [ ] The following test data shows that the environment stresses, high temperature or low temperature did not impact the performance of the pulse card. The accuracy of the pulse card remained < 0.1% meeting the acceptance criteria.

Table 7 – Summary of HFC-AI4K Accuracy Results

Test Phase	Channel 1 [ ]			
	Maximum	Minimum	Average	Accuracy
High Temp	[ ]	[ ]	[ ]	[ ]
Low Temp	[ ]	[ ]	[ ]	[ ]
Ambient 1	[ ]	[ ]	[ ]	[ ]

4.1.2 Response Time

The ERD111 test system was configured to run separate algorithms for digital and analog response time, which were run during each phase of the environmental test. The purpose of these tests was to provide objective evidence for the processing characteristics of the controller hardware during environmental stress conditions.

4.1.2.1 Digital Response Time

The automated digital response time test used two different algorithms. See *Figure 10.*

[

]

Acceptance criteria for digital response time are as follows:

- Response time from activation of a trip condition to output of a trip signal shall be 100 ms or less for digital signals.
- The measured response time shall not vary by more than ±10% from the measured baseline value.

Figure 10 – Timer Algorithm used in TSAP

Table 8 lists a summary of the digital response time data logged during the environmental stress test. [

]

Table 8 – Summary of Digital Response Time Test Results

SOE File	S1891921 – High Temp Test 1				
Algorithm	Log Point	Minimum	Average	Maximum	Avg/14
Free-Running	[ ]	[ ]	[ ]	[ ]	[ ]
Algorithm	[ ]	[ ]	[ ]	[ ]	[ ]
Trip Response	[ ]	[ ]	[ ]	[ ]	
SOE File	S1891934 – High Temp Test 2				
Algorithm	Log Point	Minimum	Average	Maximum	Avg/14
Free-Running	[ ]	[ ]	[ ]	[ ]	[ ]
Algorithm	[ ]	[ ]	[ ]	[ ]	[ ]
Trip Response	[ ]	[ ]	[ ]	[ ]	
SOE File	S1961058 – Low Temp Test 1				
Algorithm	Log Point	Minimum	Average	Maximum	Avg/14
Free-Running	[ ]	[ ]	[ ]	[ ]	[ ]
Algorithm	[ ]	[ ]	[ ]	[ ]	[ ]
Trip Response	[ ]	[ ]	[ ]	[ ]	
SOE File	S1961105 – Low Temp Test 2				
Algorithm	Log Point	Minimum	Average	Maximum	Avg/14
Free-Running	[ ]	[ ]	[ ]	[ ]	[ ]
Algorithm	[ ]	[ ]	[ ]	[ ]	[ ]
Trip Response	[ ]	[ ]	[ ]	[ ]	
SOE File	S1961644 – Ambient Test 1				
Algorithm	Log Point	Minimum	Average	Maximum	Avg/14
Free-Running	[ ]	[ ]	[ ]	[ ]	[ ]
Algorithm	[ ]	[ ]	[ ]	[ ]	[ ]
Trip Response	[ ]	[ ]	[ ]	[ ]	
SOE File	S1961648 – Ambient Test 2				
Algorithm	Log Point	Minimum	Average	Maximum	Avg/14
Free-Running	[ ]	[ ]	[ ]	[ ]	[ ]
Algorithm	[ ]	[ ]	[ ]	[ ]	[ ]
Trip Response	[ ]	[ ]	[ ]	[ ]	
Note: Data from **S1961648** exhibited two examples of contact bounce for 2.DI.145.					

The average response time is less than 100 ms as shown in Table 8. The results shown the digital response time meets the acceptance criteria in each environmental stress periods.

4.1.2.2 Analog Response Time

The algorithm used to test analog response time consists of a simulated analog trip signal from the HPAT and a DHA block configured to trip when its input reaches 50%. See Figure 11.

Figure 11 – Analog Response Time Test Algorithm.

Since the HAS logger is limited to a one-second update rate, the SOE logger was used to record the data for this test. In order to produce signals that could be detected by the SOE input card, an external module triggered a relay at the leading and trailing edge of the analog trip signal. Three signals were monitored for the test:

[

]

Acceptance criteria for the analog response time parameter are as follows:

- Response time from activation of a trip condition to output of a trip signal shall be 300ms.
- The measured response time shall not vary by more than ±10% from the measured baseline value.

Table 9 shows that the analog response time for the digital trip output signal is less than 300 ms for all phases of the test. All response time delays were within the range encompassed by the baseline test.

Table 9 – Analog Response Time Test

Response Delay	[	]	[	]
	Leading Edge	**Trailing Edge**	**Leading Edge**	**Trailing Edge**
High Temperature 1 - S1891921				
Average	[ ]	[ ]	[ ]	[ ]
Response Delay	[	]	[	]
	Leading Edge	**Trailing Edge**	**Leading Edge**	**Trailing Edge**
High Temperature 2 - S1891934				
Average	[ ]	[ ]	[ ]	[ ]
Response Delay	[	]	[	]
	Leading Edge	**Trailing Edge**	**Leading Edge**	**Trailing Edge**
Low Temperature 1 - S1961058				
Average	[ ]	[ ]	[ ]	[ ]
Response Delay	[	]	[	]
	Leading Edge	**Trailing Edge**	**Leading Edge**	**Trailing Edge**
Low Temperature 2 - S1961105				
Average	[ ]	[ ]	[ ]	[ ]
Response Delay	[	]	[	]
	Leading Edge	**Trailing Edge**	**Leading Edge**	**Trailing Edge**
Return to Ambient 1 - S1961644				
Average	[ ]	[ ]	[ ]	[ ]
Response Delay	[	]	[	]
	Leading Edge	**Trailing Edge**	**Leading Edge**	**Trailing Edge**
Return to Ambient 2 - S1961648				
Average	[ ]	[ ]	[ ]	[ ]

4.1.3 Discrete Input/Output Operability Tests

The discrete input operability test demonstrates the capability of each type of discrete input channel to detect a transition in the signal being monitored. The purpose of discrete output operability test was to demonstrate the capability of each type of discrete output channel to operate within its specified range of loading conditions.

During the environmental stress tests, due to the accessibility of the heat chamber, the manual testing of each of these discrete input or output channel were not feasible. Therefore, the prudency BOE test data were used for validating that these channels functioned normally during these stress conditions. See section 4.2 "Prudency Test Results" for detail analyses for the digital signals related to discreet input/output channel operability.

4.1.4 Communication Test

This test monitored the operation of the ICL and C-Link error counters during each phase of the environmental stress test.

Acceptance criteria for this test are that the system and both of its communication links continue operating without disruption before, during, and after application of the stress conditions. Nominal performance of the background tests indicate that the ERD111 test system continued operating reliably, and error logs indicate that no C-Link and no ICL errors were logged during the test.

Data collected from the prudency BOE tests during all environmental stress testing periods also verified that the communication links did not have errors. See section 4.2 "Prudency Test Results" for more information.

4.1.5 Timer Test

The ERD111 TSAP included two algorithms for testing the timer function consisting of four timers:

[

]

See the following figure for the algorithm.

Figure 12 – Timer Algorithm

The accumulated results are listed in Table 10.

Table 10 – Timer Test Results

S1892024	Averaged	[ ]		[ ]	
	Period	Ave Value	Accuracy	Avg Value	Accuracy
High Temp 1	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]
S1892029	Averaged	[ ]		[ ]	
	Period	Ave Value	Accuracy	Avg Value	Accuracy
High Temp 2	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]
S1961143	Averaged	[ ]		[ ]	
	Period	Ave Value	Accuracy	Avg Value	Accuracy
Low Temp 1	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]
S1961147	Averaged	[ ]		[ ]	
	Period	Ave Value	Accuracy	Avg Value	Accuracy
Low Temp 2	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]
S1961737	Averaged	[ ]		[ ]	
	Period	Ave Value	Accuracy	Avg Value	Accuracy
Return to Ambient 1	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]
S1961739	Averaged	[ ]		[ ]	
	Period	Ave Value	Accuracy	Avg Value	Accuracy
Return to Ambient 2	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]

The specified acceptance criterion for the timer function is that timer accuracy shall vary by no more than ±1% of the preset value or by more than ±3 scan cycles.

Table 10 shows that the averaged timer period meets the ±1% acceptance criterion in every case. The presence of environmental stress had no impact on the performance of the timer function.

4.1.6 Failure to Complete Scan Detection

The purpose of this test is to demonstrate that the ERD111 system will initiate failover if the controller fails to complete at least one execution of the application program within a context switch period. When the test is initiated, the algorithm forces the application program to enter an infinite loop. When the primary detects failure to complete scan status, it activates an alarm flag and forces failover to the secondary. When failover occurs, the test algorithm is automatically disabled to prevent failure of the secondary controller as well. [

]

4.1.7 Failover Test

The purpose of the failover operability test was to demonstrate that the ERD111 test system could transfer control from primary to secondary without disrupting the process under control. The complete test had several phases including a few manual steps for using oscilloscope connecting to specific hardware. Due to the accessibility of the heat chamber, however, only those tests that could be done outside the heat chamber were executed. This set of tests was performed at the end of high temperature stress, the end of low temperature stress. The following figures and tables show the test results.

Figure 13 – Analog Accuracy Data during Failover at High Temperature

Figure 14 – Analog Accuracy Data during Failover at Low Temperature

These tables and figures show there was no impact on stable analog values or analog values in transition during faillover at any environmental stress conditions.

For digital loops, timer function loops were used for validating the impact of failover. As shown in the following table, there was no impact for the digital loop during failover at any environmental stress conditions. Control transfer to the secondary processor during the failover event was also logged in the alarm file.

Table 11 – Timer Test Results through Failover at Environmental Stress Periods

SOE File S1951823	Averaged Period	[ ]		[ ]	
		Avg Value	Accuracy	Avg Value	Accuracy
High Temperature	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]
SOE File S1961308	Averaged Period	[ ]		[ ]	
		Avg Value	Accuracy	Avg Value	Accuracy
Low Temperature	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]

In addition to these measurements, processor cycle time were recorded for over a period of five minutes covering the failover event. The average processor cycle time measured during the environmental stress periods were summarized in the following table.

Table 12 – Process Cycle Time through Failover at Environmental Stress Period

Environmental Stress Period	Average Process Cycle Time
At the end of High Temperature	[ ]
At the end of Low Temperature	[ ]

No impact of the failover event was observed. By examining the above test results, it is concluded that the environment stress conditions, either high temperature stress or low temperature stress, do not have any impact on the failover function of the ERD111 test specimen.

4.1.8 Loss of Power Test

This test was run at the end of the high temperature and low temperature phases of the environmental stress test. The purpose of the test was to demonstrate that output channels went to their inactive levels when power was lost and that they remained in those states until the controller completed its internal initialization. Table 13 shows the test points validated for the output states during the environmental stress tests.

Table 13 – Loss of Power Verification Points

Verification Criteria	Points Tested
AO channels are open (0 mA output)	[ ]
Power Outputs are open (120 vac, 125 vdc)	[ ]
DO channels are de-energized	[ ]

4.1.8.1 At the End of High Temperature Stress

During the high temperature stress phase, the Loss of Power test was conducted on 7/14/2010 around 6:55pm. The figures below shows the system resumed operation without intervention after the power was restored.

Figure 15 – Analog Accuracy during Loss of Power Test at High Temperature

4.1.8.2 At the End of Low Temperature Stress

During the low temperature stress phase, the loss of power test was conducted on 7/15/2010 around 1:00pm. Similar to the high temperature case, the figure below shows the system resumed operation without intervention after the power was restored.

Figure 16 – Analog Accuracy Data during Power Loss at Low Temperature

The test results show that after the loss of power:

[

]

After the power was restored, all operations returned to normal without intervention. These test results show that the environmental stress conditions, high temperature or low temperature, do not have any negative impact to the ERD111 specimen recovering from loss of power.

4.1.9 Power Interruption

The power interruption test subjects the system to a 40 ms interruption in source AC power to demonstrate the capability of the system to continue functional operation during switchover to a backup power source. The test was conducted during the high temperature and low temperature phases of the environmental test with the following background conditions configured:

- Static points were configured to known states
- Automatic accuracy test, response time test, and timer test were running

The following acceptance criteria are specified for this test:

- No controller resets
- No static DO channel changes state
- No static AO point changes its value by more than 5%
- Logged parameters for all of the automated tests remain within tolerance

4.1.9.1 At the end of High Temperature

The following tables show the data collected during the high temperature execution.

Table 14 – HFC-AI16F [ ] Image – High Temperature Execution

Step Level	Raw Averaged Image	Corrected Average Value	Accuracy
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]

Table 15 – HFC-AO8F [ ] Image – High Temperature Execution

Average Source Value (HPAT Source Image)	Averaged Image [ ]	Accuracy
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]

Table 16 – HFC-AI8M AI Images – High Temperature Execution

Channel 1 [ ]		Channel 2 [ ]		Channel 8 [ ]		
Max.	Min.	Max.	Min.	Max.	Min.	Difference
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]

Table 17 – Digital Response Time Test – High Temperature Execution

SOE File	S1951903 – HI Temp				
Algorithm	Log Point	Minimum	Average	Maximum	Avg/14
Free-Running	[ ]	[ ]	[ ]	[ ]	[ ]
Algorithm	[ ]	[ ]	[ ]	[ ]	[ ]
Trip Response	[ ]	[ ]	[ ]	[ ]	

Table 18 – Analog Response Time Test at High Temperature

Response Delay	[ ]		[ ]	
	Leading Edge	Trailing Edge	Leading Edge	Trailing Edge
HI Temp - S1951903				
Average	[ ]	[ ]	[ ]	[ ]

Table 19 – Timer Test at High Temperature

SOE S1951903	Averaged Period	[ ]		[ ]	
		Avg Value	Accuracy	Avg Value	Accuracy
High Temp	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]

4.1.9.2 At the end of Low Temperature

The following tables show the data collected during the low temperature execution.

Table 20 – HFC-AI16F [ ] Image – Low Temperature Execution

Step Level	Raw Averaged Image	Corrected Average Value	Accuracy
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]

Table 21 – HFC-AO8F [ ] Image – Low Temperature Execution

Average Source Value (HPAT Source Image)	Averaged Image Value [ ]	Accuracy
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]

Table 22 – HFC-AI8M AI Images – Low Temperature Execution

Channel 1 [ ]		Channel 2 [ ]		Channel 8 [ ]		
Max.	Min.	Max.	Min.	Max.	Min.	Difference
[ ]	[ ]	[ ]	[ ]	[ ]	[ ]	[ ]

Table 23 – HFC-AI4K AI Image – Low Temperature Execution

Channel 1 [ ]			
Maximum	Minimum	Average	Accuracy
[ ]	[ ]	[ ]	-[ ]

Table 24 – Digital Response Time Test at Low Temperature

SOE File	**S1961320 – LO Temp**				
Algorithm	**Log Point**	**Minimum**	**Average**	**Maximum**	**Avg/14**
Free-Running	[ ]	0.9153	1.153084	1.3708	0.082363
Algorithm	[ ]	0.8698	1.152366	1.3251	0.082312
Trip Response	[ ]	0.0421	0.083581	0.1177	

Table 25 – Analog Response Time Test at Low Temperature

Response Delay	[ ]		[ ]	
	Leading Edge	**Trailing Edge**	**Leading Edge**	**Trailing Edge**
LO Temp – S1961320				
Average	[ ]	[ ]	[ ]	[ ]

Table 26 – Timer Test at Low Temperature

SOE S1961320	Averaged Period	[ ]		[ ]	
		Avg Value	Accuracy	Avg Value	Accuracy
Low Temp	On	[ ]	[ ]	[ ]	[ ]
	Off	[ ]	[ ]	[ ]	[ ]
	Total	[ ]	[ ]	[ ]	[ ]

All logs of digital data recorded during these tests indicate normal operation without any disruption.

- There was no indication of any disruption during either the high temperature or the low temperature execution of this test
- Values for both the averaged timer period and accuracy are comparable to those measured without the power interruption
- Values for the automated digital and analog response time are comparable to those measured without the power interruption

[

]

- Changes in values of static points did not occur.

4.1.10 Power Quality

The power quality tolerance test was executed once at the end of the high temperature period of the test. During this test the voltage and frequency of the primary source power were varied over the limits of the ERD111 test system power supplies, and system performance was monitored. The test was conducted on 7/8/2011 from 9:00 AM to 9:18 AM and included three phases:

- **Pretest**. Source power was set to the normal level of 120 vac at 60 Hz (9:00 to 9:03 AM). Automated accuracy, timer, and response time test were run, and selected static point values were monitored.

- **Low voltage limit**. Source power was set to 90 vac at 57 Hz and then to 90 vac and 63 Hz. Then the source voltage was reduced until the power supplies shut down. (9:08 to 9:11:19 AM) System shutdown occurred at 9:11:19 AM. Automated accuracy and BOE tests were run and selected static points were monitored.

- **High voltage**. Source power was set to 150 vac at 57 Hz, to 150 vac and 63 Hz, and then back to 120 vac at 60 Hz. (9:15 to 9:18 AM) Automated accuracy and BOE tests were run and selected static points were monitored.

The automated accuracy tests of the analog cards were running during each phase of this test to demonstrate system stability under varying states of supply power quality. Results for each phase of the test are summarized in the following tables.

Table 27 – HFC-AI16F [ ]

Step Level	Raw Averaged Image	Corrected Average Value	Accuracy
Pretest			
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]
Low Voltage Power			
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]
High Voltage Power			
10%	[ ]	[ ]	[ ]
30%	[ ]	[ ]	[ ]
50%	[ ]	[ ]	[ ]
70%	[ ]	[ ]	[ ]
90%	[ ]	[ ]	[ ]

Table 28 – HFC-AO8F [ ]

Average Source Value [ ]	Averaged Image Value [ ]	Accuracy
Low Voltage Power		
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
High Voltage Power		
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]

[

]

4.1.10.1 Miscellaneous Points

Various static points were monitored to detect spurious transitions. [

]

4.2 *Prudency Tests*

4.2.1 Digital Burst of Event Tests

The digital BOE test was executed before, during and after the environmental test conducted on the ERD111 test specimen. Table 29 through Table 34 present a summary of the test data preserved in the SOE reports during high temperature, low temperature and back to ambient. The tables are each divided into two sets of points. These two sets of points represent the different phase relationship between the BOE driving signals. [

] This asymmetry produced a small part of the reported deviation; the remainder was produced by the processing of the ERD111 Test Specimen and the TSAP logic. In each case, the signal source was connected to a DI channel of the ERD111 test specimen, and the resulting image drove a DO channel, which controlled the input to the SOE logger. Different paths through the TSAP produced different total transfer delays from input to output, but the delay from transition to transition was expected to be consistent with that of the signal source. As indicated in the tables, the averaged HI/LO interval was within tolerance for every test run. (Note: Entries with * indicate contact bounce detected for that run at that channel.)

Table 29 – *High Temperature Test 1 S1892049 – 7/8/2010 at 8:49 PM*

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 30 – High Temperature Test 2 **S1892051 – 7/8/2010 at 8:52 PM**

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 31 – Low Temperature Test 1 **S1961247 – 7/15/2010 at 12:47 PM**

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 32 – Low Temperature Test 2 **S1961251 – 7/15/2010 at 12:51 PM**

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 33 – Return to Ambient Test 1 **S1961800 – 7/15/2010 at 6:00 PM**

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

Table 34 – Return to Ambient Test 2 **S1961803 – 7/15/2010 at 6:03 PM**

Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
Signal Source	Point Logged	Time HI	Time LO
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]

[

]

4.2.2 Analog BOE data

[

]

Table 35 – AI16F to AO8F (Environmental Stress Test)

[ ]		[ ]			[ ]		
Time	**Value**	**Time**	**Value (Avg)**	**Δ**	**Time**	**Value (Avg)**	**Δ**
High Temp Test 1							
<49:02.0	10	<49:01.0	[ ]	[ ]	49:02.0	[ ]	[ ]
49:02.0	90	49:05.0	[ ]	[ ]	49:08.0	[ ]	[ ]
49:12.0	10	49:17.0	[ ]	[ ]	49:20.0	[ ]	[ ]
49:22.0	90	49:25.0	[ ]	[ ]	49:28.0	[ ]	[ ]
49:32.0	10	49:37.0	[ ]	[ ]	49:40.0	[ ]	[ ]
49:42.0	90	49:45.0	[ ]	[ ]	49:48.0	[ ]	[ ]
>49:52.0	10	49:58.0	[ ]	[ ]	50:00.0	[ ]	[ ]
High Temp Test 2							
<51:26	90	<51:24.0	[ ]	[ ]	<51:24.0	[ ]	[ ]
51:26.0	10	51:30.0	[ ]	[ ]	51:32.0	[ ]	[ ]
51:36.0	90	51:40.0	[ ]	[ ]	51:40.0	[ ]	[ ]
51:46.0	10	51:51.0	[ ]	[ ]	51:52.0	[ ]	[ ]
51:56.0	90	52:00.0	[ ]	[ ]	52:00.0	[ ]	[ ]
52:06.0	10	52:10.0	[ ]	[ ]	52:12.0	[ ]	[ ]
52:16.0	90	52:20.0	[ ]	[ ]	52:20.0	[ ]	[ ]
52:26.0	10	52:30.0	[ ]	[ ]	52:32.0	[ ]	[ ]
52:36.0	90	52:40.0	[ ]	[ ]	52:40.0	[ ]	[ ]
52:46.0	10	52:50.0	[ ]	[ ]	52:52.0	[ ]	[ ]
52:56.0	90	52:58.0	[ ]	[ ]	53:00.0	[ ]	[ ]
Low Temp Test 1							
45:00.0	90	45:04.0	[ ]	[ ]	45:04.0	[ ]	[ ]
45:10.0	10	45:15.0	[ ]	[ ]	45:16.0	[ ]	[ ]
45:20.0	90	45:24.0	[ ]	[ ]	45:24.0	[ ]	[ ]
45:30.0	10	45:35.0	[ ]	[ ]	45:36.0	[ ]	[ ]
45:40.0	90	45:44.0	[ ]	[ ]	45:44.0	[ ]	[ ]
45:50.0	10	45:55.0	[ ]	[ ]	45:56.0	[ ]	[ ]
[ ]		[ ]			[ ]		
Time	**Value**	**Time**	**Value (Avg)**	**Δ**	**Time**	**Value (Avg)**	**Δ**
Low Temp Test 2							
49:00.0	10	49:06.0	[ ]	[ ]	49:06.0	[ ]	[ ]
49:10.0	90	49:14.0	[ ]	[ ]	49:14.0	[ ]	[ ]
49:20.0	10	49:25.0	[ ]	[ ]	49:26.0	[ ]	[ ]
49:30.0	90	49:34.0	[ ]	[ ]	49:34.0	[ ]	[ ]
49:40.0	10	49:45.0	[ ]	[ ]	49:46.0	[ ]	[ ]
49:50.0	90	49:54.0	[ ]	[ ]	49:54.0	[ ]	[ ]
Averaged deviation during test				[ ]			[ ]

Table 36 – AI16F to AO8F (Return to Ambient)

[ ]		[ ]			[ ]		
Time	**Value**	**Time**	**Value (Avg)**	**Δ**	**Time**	**Value (Avg)**	**Δ**
<58:13.0	90	<58:13.0	[ ]	[ ]	<58:11.0	[ ]	[ ]
58:13.0	10	58:19.0	[ ]	[ ]	58:19.0	[ ]	[ ]
58:23.0	90	58:27.0	[ ]	[ ]	58:29.0	[ ]	[ ]
58:33.0	10	58:38.0	[ ]	[ ]	58:39.0	[ ]	[ ]
58:43.0	90	58:47.0	[ ]	[ ]	58:47.0	[ ]	[ ]
58:53.0	10	58:58.0	[ ]	[ ]	59:01.0	[ ]	[ ]
59:03.0	90	59:07.0	[ ]	[ ]	59:09.0	[ ]	[ ]
59:13.0	10	59:18.0	[ ]	[ ]	59:19.0	[ ]	[ ]
59:23.0	90	59:28.0	[ ]	[ ]	59:29.0	[ ]	[ ]
59:33.0	10	59:38.0	[ ]	[ ]	59:39.0	[ ]	[ ]
59:43.0	90	59:47.0	[ ]	[ ]	59:49.0	[ ]	[ ]
00:11.0	10	00:16.0	[ ]	[ ]	00:15.0	[ ]	[ ]
00:21.0	90	00:24.0	[ ]	[ ]	00:25.0	[ ]	[ ]
00:31.0	10	00:36.0	[ ]	[ ]	00:37.0	[ ]	[ ]
00:41.0	90	00:44.0	[ ]	[ ]	00:45.0	[ ]	[ ]
00:51.0	10	00:55.0	[ ]	[ ]	00:57.0	[ ]	[ ]
01:01.0	90	01:04.0	[ ]	[ ]	01:05.0	[ ]	[ ]
01:11.0	10	01:16.0	[ ]	[ ]	01:17.0	[ ]	[ ]
01:21.0	90	01:24.0	[ ]	[ ]	01:25.0	[ ]	[ ]
01:32.0	10	01:36.0	[ ]	[ ]	01:37.0	[ ]	[ ]
01:41.0	90	01:44.0	[ ]	[ ]	01:45.0	[ ]	[ ]
01:51.0	10	01:55.0	[ ]	[ ]	01:57.0	[ ]	[ ]
02:01.0	90	02:04.0	[ ]	[ ]	02:05.0	[ ]	[ ]
02:11.0	10	02:16.0	[ ]	[ ]	02:15.0	[ ]	[ ]
02:21.0	90	02:24.0	[ ]	[ ]	02:25.0	[ ]	[ ]
02:31.0	10	02:35.0	[ ]	[ ]	02:37.0	[ ]	[ ]
02:41.0	90	02:44.0	[ ]	[ ]	02:47.0	[ ]	[ ]
02:51.0	10	02:55.0	[ ]	[ ]	02:57.0	[ ]	[ ]
03:01.0	90	03:04.0	[ ]	[ ]	03:05.0	[ ]	[ ]
03:12.0	10	03:15.0	[ ]	[ ]	03:17.0	[ ]	[ ]
03:21.0	90	03:24.0	[ ]	[ ]	03:25.0	[ ]	[ ]
>03:33.0	90	>03:36.0	[ ]	[ ]	>03:37.0	[ ]	[ ]
Averaged deviation during test				[ ]			[ ]

Acceptance criteria for the analog BOE test are as follows:

AI Image — Each transition is present in the logged image data.

The averaged image at each level remains within ±0.35% of the source signal based on a full span of 100%.

AO Image — Each transition is present in the logged image data.

The averaged image at each level remains within ±0.32% of the source signal based on a full span of 100%.

Examination of the above tables indicates every transition was detected except at the end of the test run when the input channel failed to reach a stable value after the algorithm was halted. In addition, all of the stable levels were well within the specified tolerance. All results obtained were within the limits specified for acceptability and consistent with the results obtained during the baseline test.

4.3 *Anomalous Records*

4.3.1 Contact Bounce

[

] Standard HFC-6000 and ECS-1200 DI modules include a software algorithm that de-bounces data read from each input channel to eliminate nuisance pulses that are less than 10 ms in duration. However, when a DI module is configured for SOE logging, the de-bounce algorithm is bypassed, and every change to the input image triggers an interrupt to initiate an input scan cycle. Because the SOE clock has a time tick of 0.1 ms, SOE DI modules have the capability of detecting and logging any pulse with a pulse width of 0.1 ms or greater. Pulses shorter than 0.1 ms may be detected and logged, but their duration cannot be reported accurately. The SOE function of the EWS does include the capability of including a de-bounce filter, but this capability was not used.

The following tables show the distribution of the contact bounce events by channel, percentage and detail list of each event.

Table 37 – Distribution of Contact Bounce Events by Channel

DO Channel	Environmental Test	Baseline Test
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]
[ ]	[ ]	[ ]

Table 38 – Percentage of Contact Bounce Events by Test Phase

DO Channel	Percentage of Contact Bounce
High Temperature Test	[ ]
Low Temperature Test	[ ]
Back to Ambient Test	[ ]
Baseline Test	[ ]

Table 39 – Contact Bounce Events Recorded During BOE Testing

SOE Record	Point	Time Stamp	Pulse State	Pulse Duration
High Temperature Test				
[ ]	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
Low Temperature Test				
[ ]	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
Return to Ambient Test				
[ ]	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]
[ ]	[ ]	[ ]	[ ]	[ ]
		[ ]	[ ]	[ ]

In every instance the contact bounce event took place immediately after the relay energized, and there was no instance in which a transition failed to be logged. The difference in distribution of contact bounce records between the baseline test and the current test indicates that logging contact bounce events is essentially a random phenomenon. [

]

4.3.2 BOE Alarm Summary

Alarm files from the days during which the environmental tests were run indicates that no alarm was logged during any execution of the BOE test.

5.0 Conclusions

The retest of ERD111 test specimen in accordance with EPRI TR 107330-1996 environmental envelope demonstrated that the HFC-6000 platform remained fully operational at different environmental stress conditions: high temperature 60°C/140°F for at least 48 hours, low temperature 4°C/40°F for at least 8 hours, and back to ambient after the cycle of the stressed conditions.

6.0 QA Records

The test results recorded in the test documents during the tests (see section 2.2) shall be preserved in accordance with QPP 17.1 "Quality Records" as nuclear records.

7.0 Attachments

None.