

ArevaEPRDCPEm Resource

From: WILLIFORD Dennis (AREVA) [Dennis.Williford@areva.com]
Sent: Wednesday, May 25, 2011 3:16 PM
To: Tesfaye, Getachew
Cc: BENNETT Kathy (AREVA); DELANO Karen (AREVA); ROMINE Judy (AREVA); RYAN Tom (AREVA)
Subject: Response to U.S. EPR Design Certification Application RAI No. 485 (5743), FSAR Ch. 7
Attachments: RAI 485 Response US EPR DC.pdf

Getachew,

Attached please find AREVA NP Inc.'s response to the subject request for additional information (RAI). The attached file provides a schedule since a technically correct and complete response to the 2 questions cannot be provided at this time.

The following table indicates the respective pages in the response document, "RAI 485 Response US EPR DC.pdf," that contain AREVA NP's response to the subject questions.

Question #	Start Page	End Page
RAI 485 — 07.09-69	2	3
RAI 485 — 07.09-70	4	4

A complete answer is not provided for the 2 questions in RAI 485. The schedule for a technically correct and complete FINAL response to these questions is provided below.

Question #	Response Date
RAI 485 — 07.09-69	June 29, 2011
RAI 485 — 07.09-70	June 29, 2011

Sincerely,

Dennis Williford, P.E.
U.S. EPR Design Certification Licensing Manager
AREVA NP Inc.

7207 IBM Drive, Mail Code CLT 2B
Charlotte, NC 28262
Phone: 704-805-2223
Email: Dennis.Williford@areva.com

From: Tesfaye, Getachew [<mailto:Getachew.Tesfaye@nrc.gov>]
Sent: Monday, May 09, 2011 4:42 PM
To: ZZ-DL-A-USEPR-DL
Cc: Zhang, Deanna; Zhao, Jack; Spaulding, Deirdre; Jackson, Terry; Canova, Michael; Colaccino, Joseph; ArevaEPRDCPEm Resource
Subject: U.S. EPR Design Certification Application RAI No. 485 (5743), FSAR Ch. 7

Attached please find the subject requests for additional information (RAI). A draft of the RAI was provided to you on April 28, 2011, and discussed with your staff on May 2, 2011. Drat RAI Question 07.09-68 was deleted

and 07.09-70 was modified as a result of that discussion. The schedule we have established for review of your application assumes technically correct and complete responses within 30 days of receipt of RAIs. For any RAIs that cannot be answered within 30 days, it is expected that a date for receipt of this information will be provided to the staff within the 30 day period so that the staff can assess how this information will impact the published schedule.

Thanks,
Getachew Tesfaye
Sr. Project Manager
NRO/DNRL/NARP
(301) 415-3361

Hearing Identifier: AREVA_EPR_DC_RAIs
Email Number: 3020

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FSAR Ch. 7
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From: WILLIFORD Dennis (AREVA)

Created By: Dennis.Williford@areva.com

Recipients:

"BENNETT Kathy (AREVA)" <Kathy.Bennett@areva.com>
Tracking Status: None
"DELANO Karen (AREVA)" <Karen.Delano@areva.com>
Tracking Status: None
"ROMINE Judy (AREVA)" <Judy.Romine@areva.com>
Tracking Status: None
"RYAN Tom (AREVA)" <Tom.Ryan@areva.com>
Tracking Status: None
"Tesfaye, Getachew" <Getachew.Tesfaye@nrc.gov>
Tracking Status: None

Post Office: auscharm02.adom.ad.corp

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RAI 485 Response US EPR DC.pdf		67370

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Response to

Request for Additional Information No. 485(5743), Revision 0

5/09/2011

U. S. EPR Standard Design Certification

AREVA NP Inc.

Docket No. 52-020

SRP Section: 07.09 - Data Communication Systems

Application Section: 7.9

**QUESTIONS for Instrumentation, Controls and Electrical Engineering 1
(AP1000/EPR Projects) (ICE1)**

Question 07.09-69:

Demonstrate that during a design basis event, the vulnerabilities for a postulated software common-cause-failure (SCCF) of all protection system (PS) division's actuation logic units (ALUs) "no-go" test, which continuously blocks the output of all applicable priority modules (PACS), have been adequately addressed and the required protective functions can be accomplished, as required by 10 CFR Part 50, Appendix A, GDC 22.

10 CFR Part 50, Appendix A, General Design Criterion (GDC) 22, "Protection System Independence," requires, in part, that design techniques, such as functional diversity or diversity in component design and principles of operation, shall be used to the extent practical to prevent loss of the protection function. The staff requirements memorandum to SECY-93-087, "Policy, Technical, and Licensing Issues Pertaining to Evolutionary and Advanced Light-Water Reactor (ALWR) Designs," Item II.Q (ML003708056), Point 1, states that the applicant shall assess the defense-in-depth and diversity of the proposed instrumentation and control system to demonstrate that vulnerabilities to common-mode failures have adequately been addressed. Point 3 states that if a postulated common-mode failure could disable a safety function, then a diverse means, with a documented basis that the diverse means is unlikely to be subject to the same common-mode failure, shall be required to perform either the same function or a different function.

Each PS division contains four ALUs; two assigned to each subsystem. For engineered safety features actuation system (ESFAS) protective functions, the ALU logic performs voting, actuation logic (e.g., checking permissive conditions, sequencing), signal latching, and output of ESFAS actuation orders. Therefore, a postulated SCCF of the ALU logic could fail any one or all of these logic functions. Figure 2-5, "ESFAS "No-Go" Test Concept," in Technical Report ANP-10315, "U.S. EPR Protection System Surveillance Testing and TELEPERM XS Self-Monitoring Technical Report," Revision 0, shows that a SCCF of the ALU logic's no-go test blocking signal would block the ESFAS actuator initiation output signal of the PACS. The PACS collects the actuation signals from multiple I&C systems (both safety and non-safety related, including diverse actuation system,) and transfers the proper actuation order to the ESFAS actuator according to pre-defined priority assignments.

Technical Report ANP-10315, Section 2.2.5.1.1, states that the blocking signal lasts for 5 seconds and is overridden if, at any time during a 5-second period, a legitimate protection function is initiated. In addition, system-level manual ESFAS actuations initiated by the operator from the safety information and control system are sent to and combined with the ALU logic. It is the staff's understanding that the ALU performs both the blocking action and the release action for the PACS no-go test. According to NUREG/CR-6303, "Method for Performing Diversity and Defense-in-Depth Analyses of Reactor Protection Systems" (ML071790509), when postulating a system SCCF, it cannot be assumed that a failed PS component can produce incorrect and correct outputs. As stated in NUREG/CR-6303, Guideline 5, among other things, in blocks containing software, it is credible that outputs shall assume values irrespective of inputs because the only logic connecting inputs to outputs is software, and the effects of software failures on outputs are unpredictable.

As stated in NUREG/CR-6303, Guideline 6, analysis of defense-in-depth should be performed by postulating concurrent failures of the same block or identical blocks (as defined in Guideline 7) in all redundant divisions. Since several channels may pass through the same block or identical blocks, such common-mode failures have the potential to cause multiple channel

failures in a single division, with the same failure replicated across all (four) protection system divisions. The output signals of the blocks thus postulated to fail should do so in accordance with Guideline 5. In other words, signals entering failed blocks assume the most adverse credible values on output, essentially losing their protective function at that point. Subject to Guidelines 7, 8, and 9, concurrent failure of each set of identical blocks in all divisions should be postulated in turn (until the list of diverse blocks has been exhausted), and the result of the failure should be documented as a finding of the analysis.

Given that the ALUs perform both the block and release function for the PACS no-go test, describe how a SCCF of the ALU that blocks and fails to release the PACS outputs is addressed.

Response to Question 07.09-69:

A response to this question will be provided by June 29, 2011.

Question 07.09-70:

The staff requests the applicant provide additional detail on the implementation of the service unit (SU) in terms of design functionality and administrative controls for plant operations.

10 CFR 52.47(a)(2) requires, in part, that the design descriptions of systems, structures and components shall be sufficient to permit understanding of the system design and their relationship to the safety evaluations. The staff understands that the SU is a non-safety tool that was originally planned to be permanently connected to the safety-related PS and SAS. To address independence between the non-safety SU and the safety systems, the design was altered, as described in interim Revision 3 of the U.S. EPR Design Control Document, Tier 2, Section 7.1, to have the SU disconnected during plant operation. The staff recognizes that the SU would need to be connected to support surveillance testing and maintenance similar to other maintenance and test equipment. However, administrative controls would need to be in place to ensure the SU is not connected beyond these circumstances since the credited independence mechanism between the SU and the safety systems is physical disconnection. Within interim Revision 3 Section 7.1, the staff noted that for the various operating modes of the TELEPERM XS-based safety systems (PS and SAS), when the SU is connected, the processors would be considered inoperable per Technical Specifications except for the cyclic processing mode. Currently, the staff does not see sufficient administrative controls to limit connection of the SU when the processors are in the cyclic processing mode (i.e., SU could be connected indefinitely in this mode).

Given the above-mentioned concerns, the staff requests the following items be addressed:

- a. Provide sufficient criteria to limit SU connectivity to PS and SAS for the cyclic processing mode of the TELEPERM XS processors.
- b. Provide an estimate of the amount of time per week, and per shift, that the SU would need to be plugged into a PS or SAS division to perform tasks that support plant operations and maintenance or for any other reasons.
- c. Identify the Technical Specification Surveillances that would require using the SU, what type of function processor is impacted by the surveillance (APU, ALU, or CU in SAS), and match these tests to the various operating modes of the function processor in which the tests would be performed.
- d. Explicitly state that the SU can only perform the functions stated in the U.S. EPR FSAR, and while the SU is not in use, it will be fully disconnected from safety-related structures, systems and components (SSCs).
- e. Define in specific terms, what is meant when a function processor's outputs are disabled and differentiate in terms of divisional and system-level impact to both PS (APUs/ALUs) and SAS(CUs). Match this refined definition to specific tasks in which the SU will be performing (refer to item C).

Response to Question 07.09-70:

A response to this question will be provided by June 29, 2011.