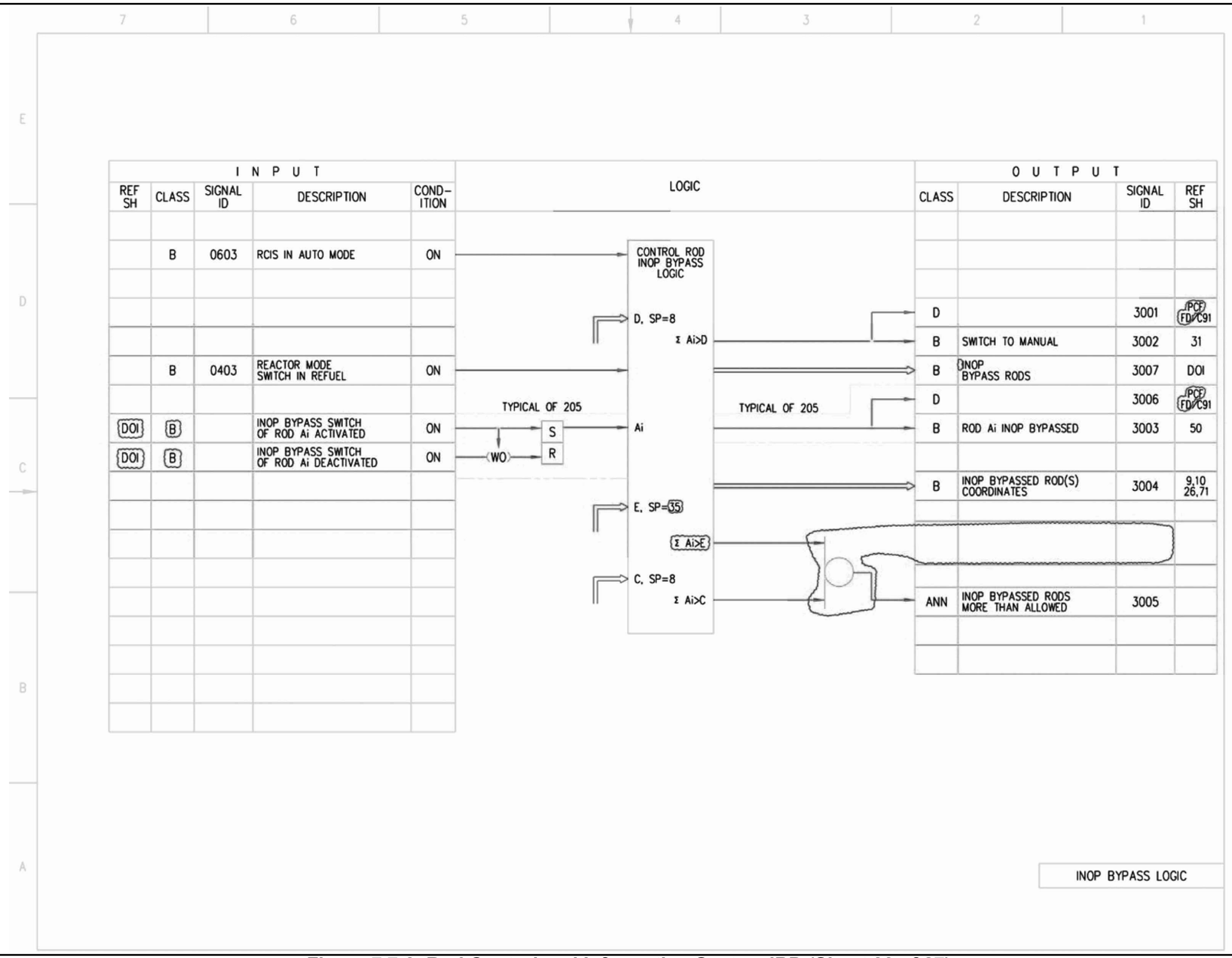


Figure 7.7-3 Rod Control and Information System IBD (Sheet 30 of 87)

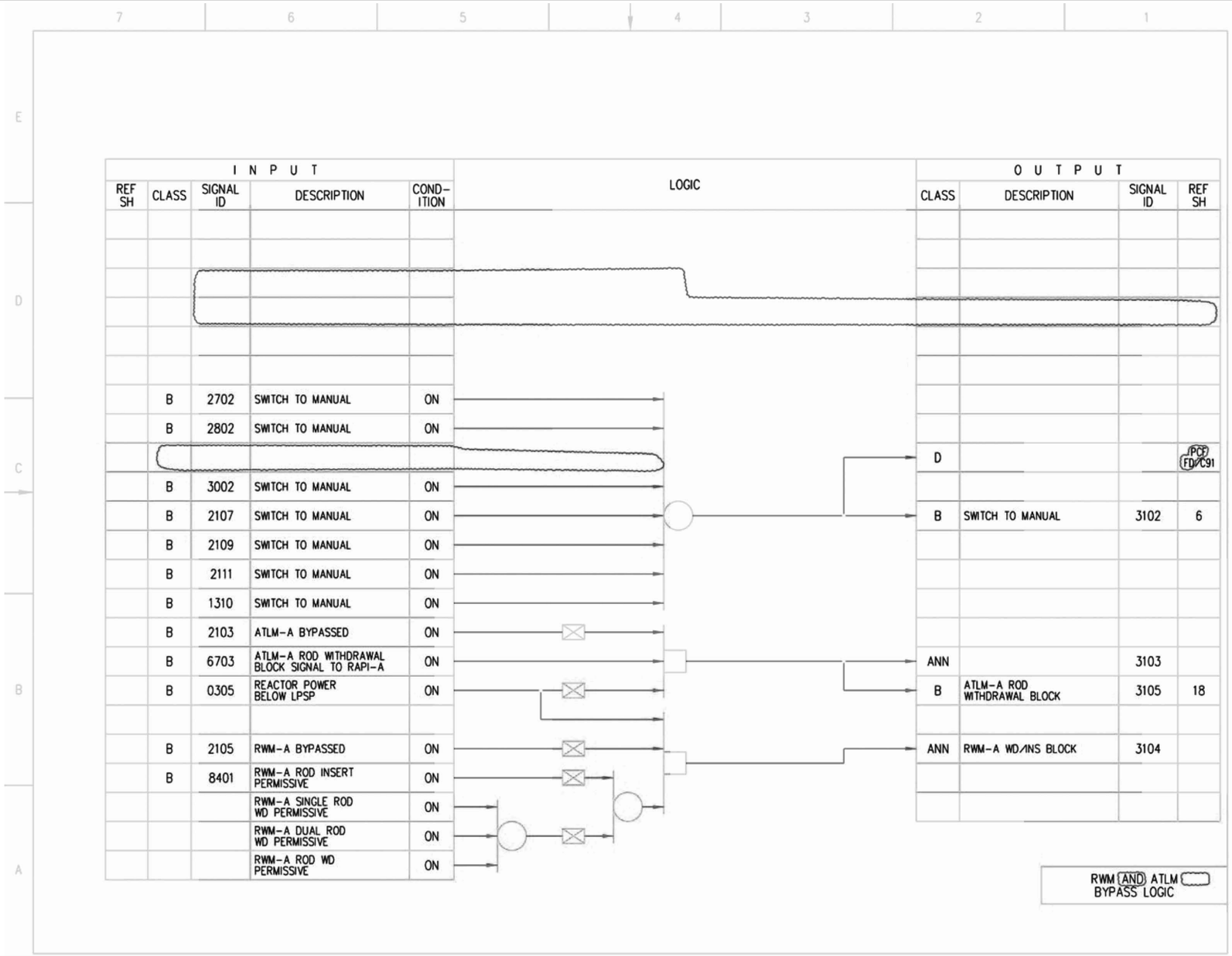


Figure 7.7-3 Rod Control and Information System IBD (Sheet 31 of 87)

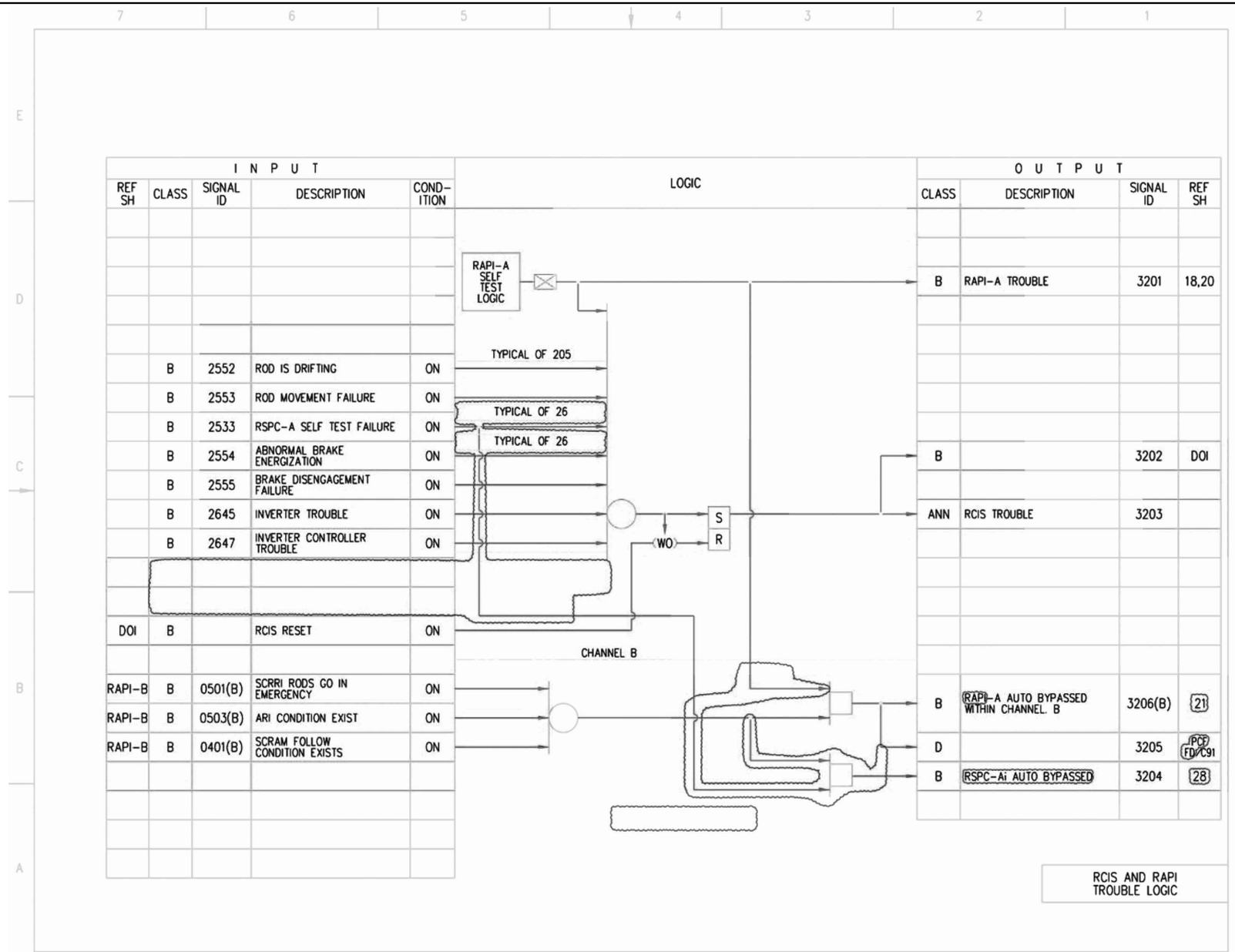


Figure 7.7-3 Rod Control and Information System IBD (Sheet 32 of 87)

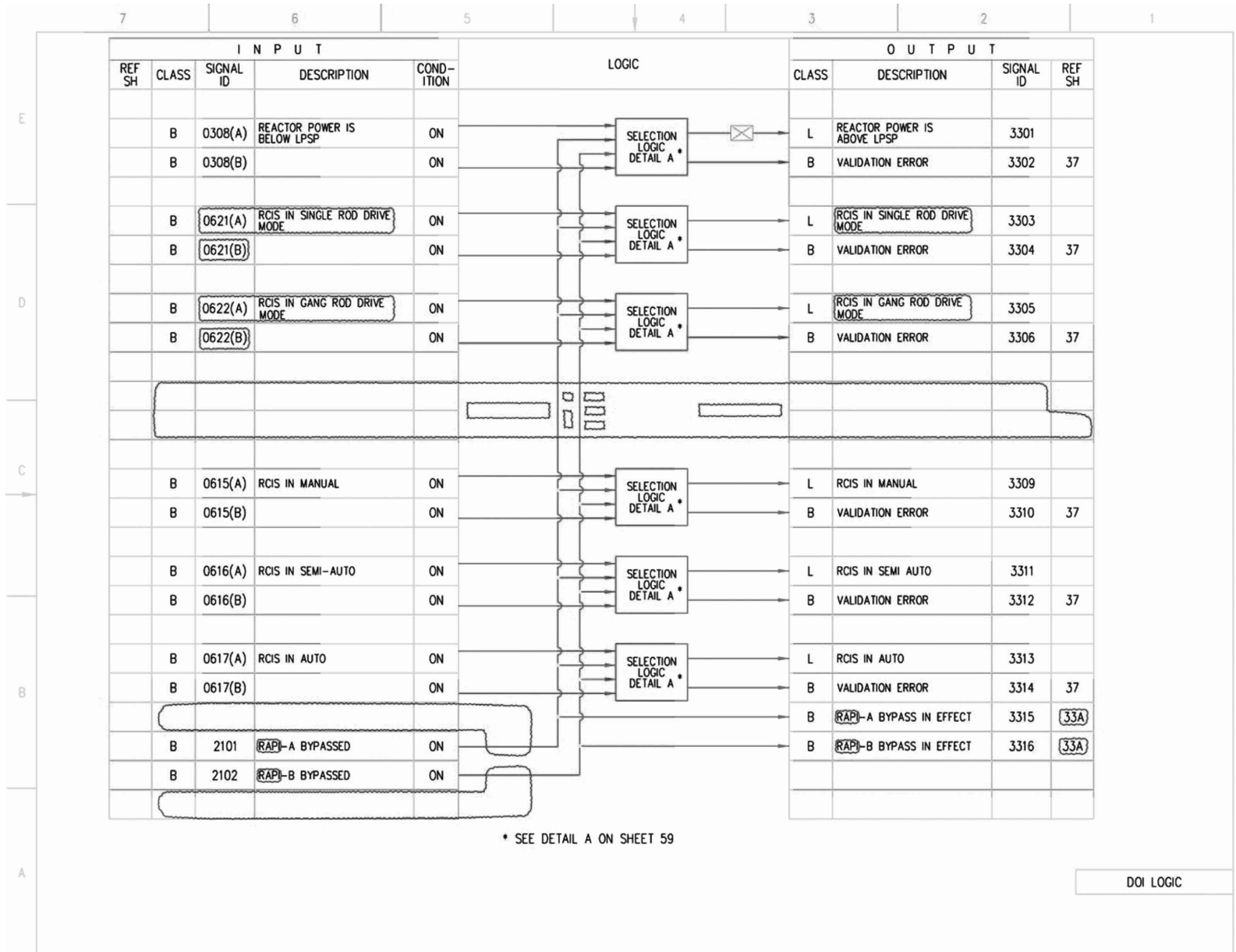


Figure 7.7-3 Rod Control and Information System IBD (Sheet 33 of 87)

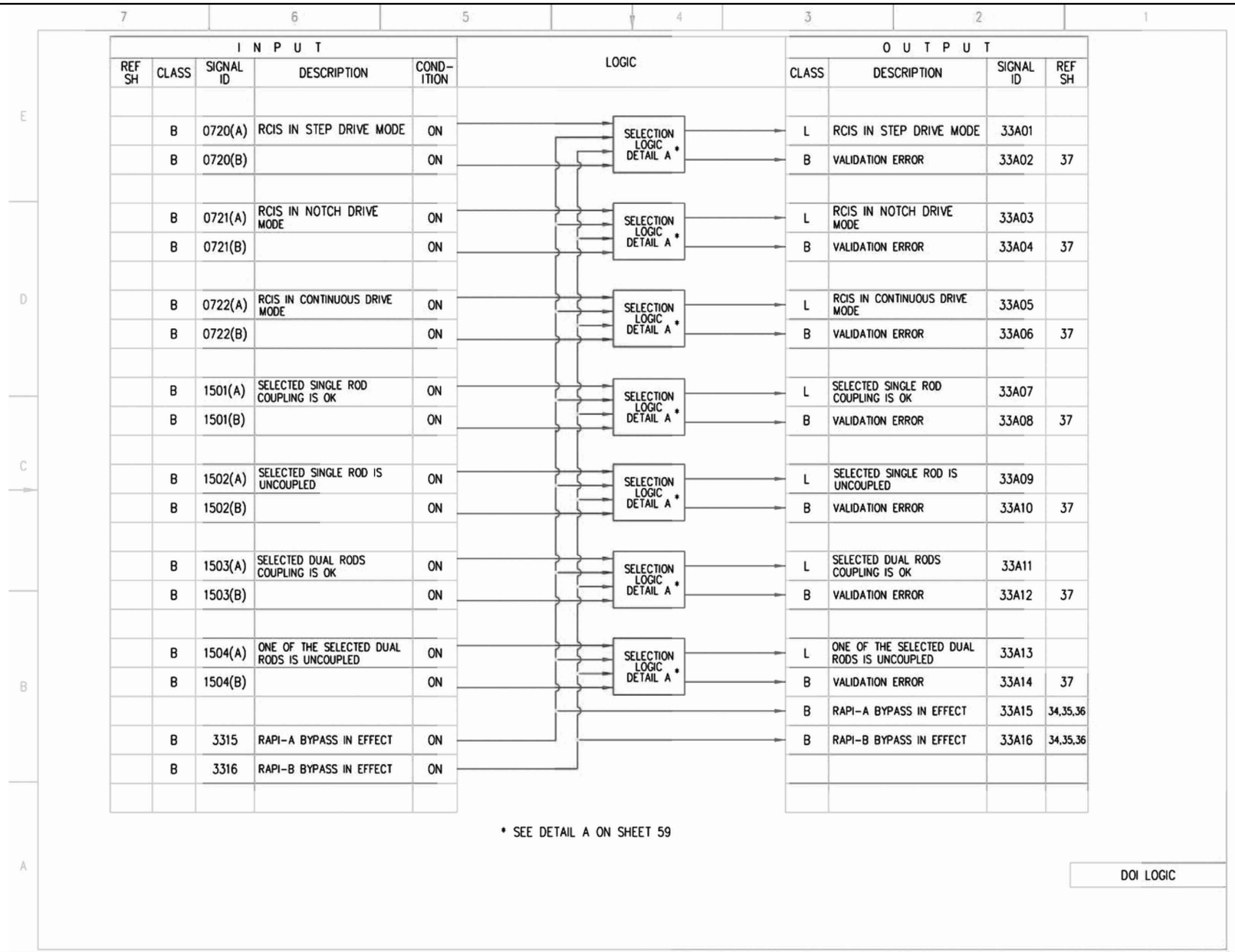


Figure 7.7-3 Rod Control and Information System IBD (Sheet 33a of 87)

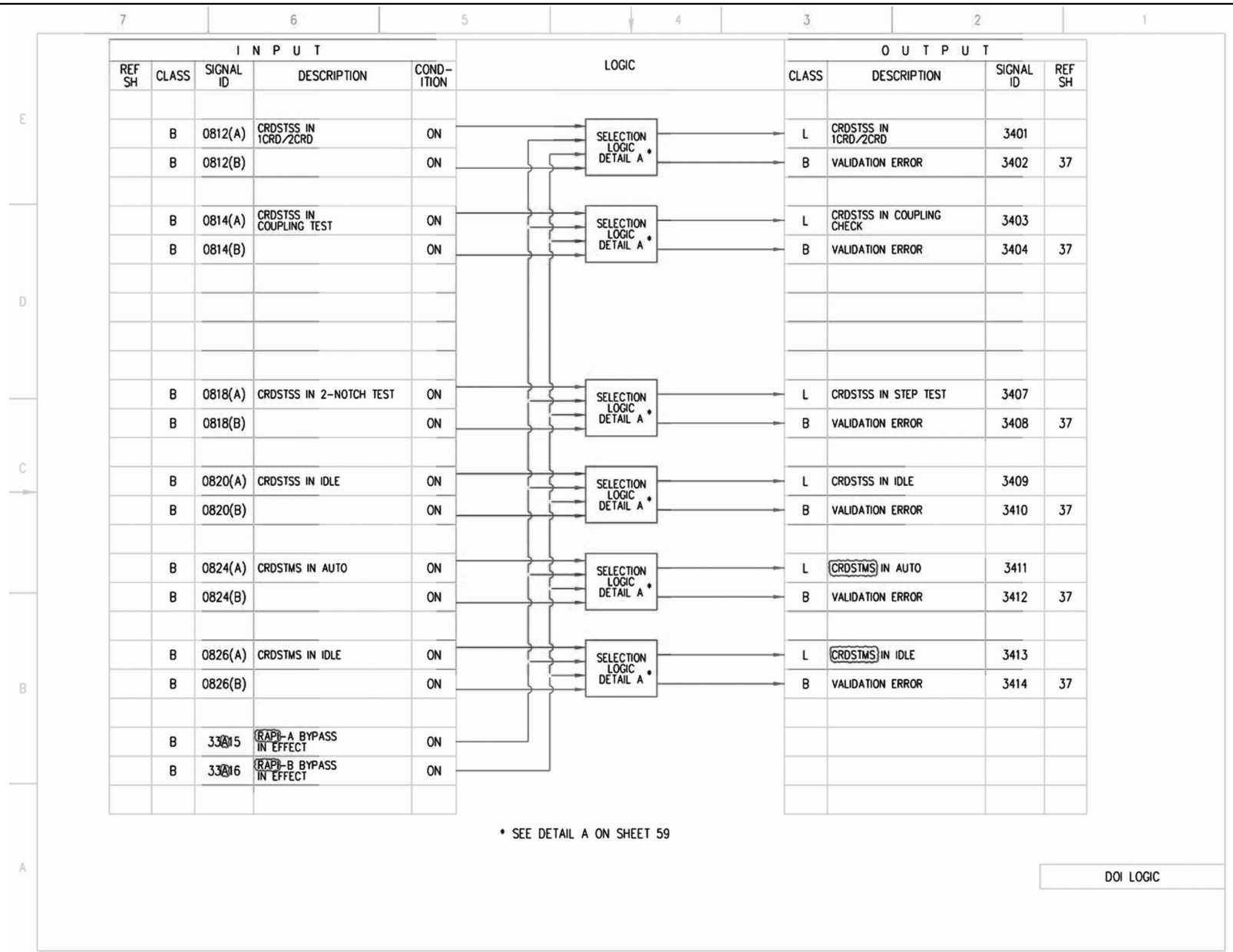


Figure 7.7-3 Rod Control and Information System IBD (Sheet 34 of 87)

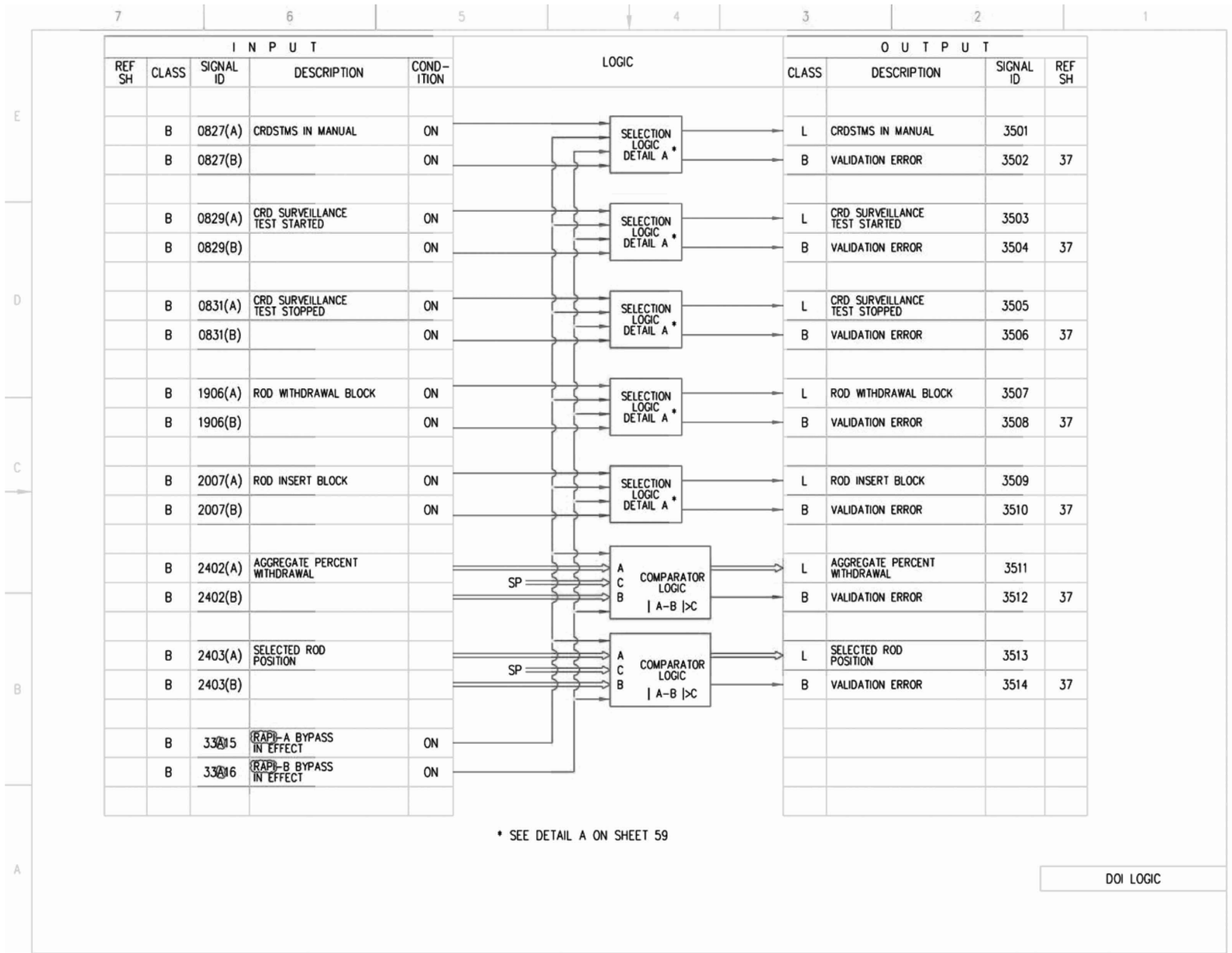


Figure 7.7-3 Rod Control and Information System IBD (Sheet 35 of 87)

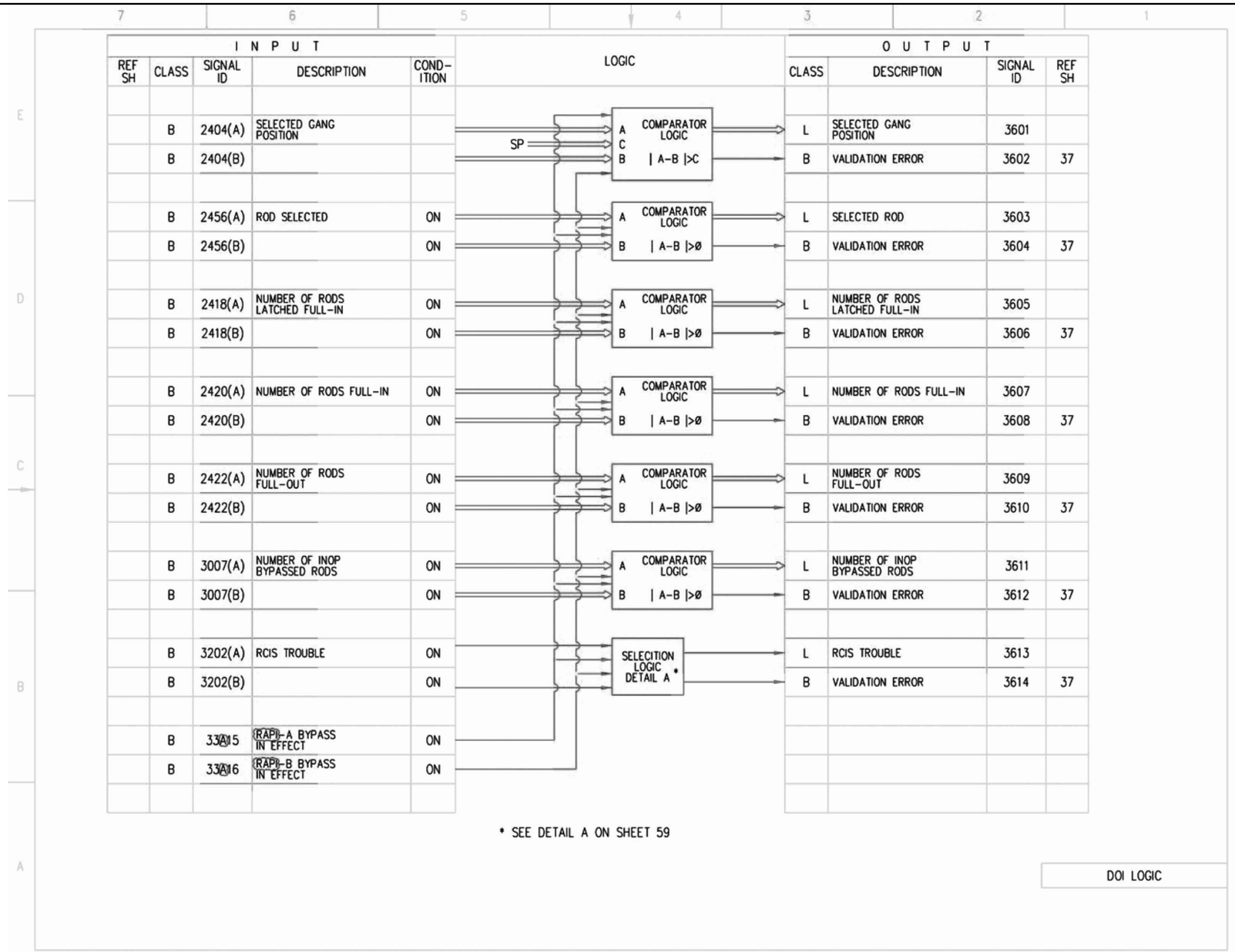


Figure 7.7-3 Rod Control and Information System IBD (Sheet 36 of 87)

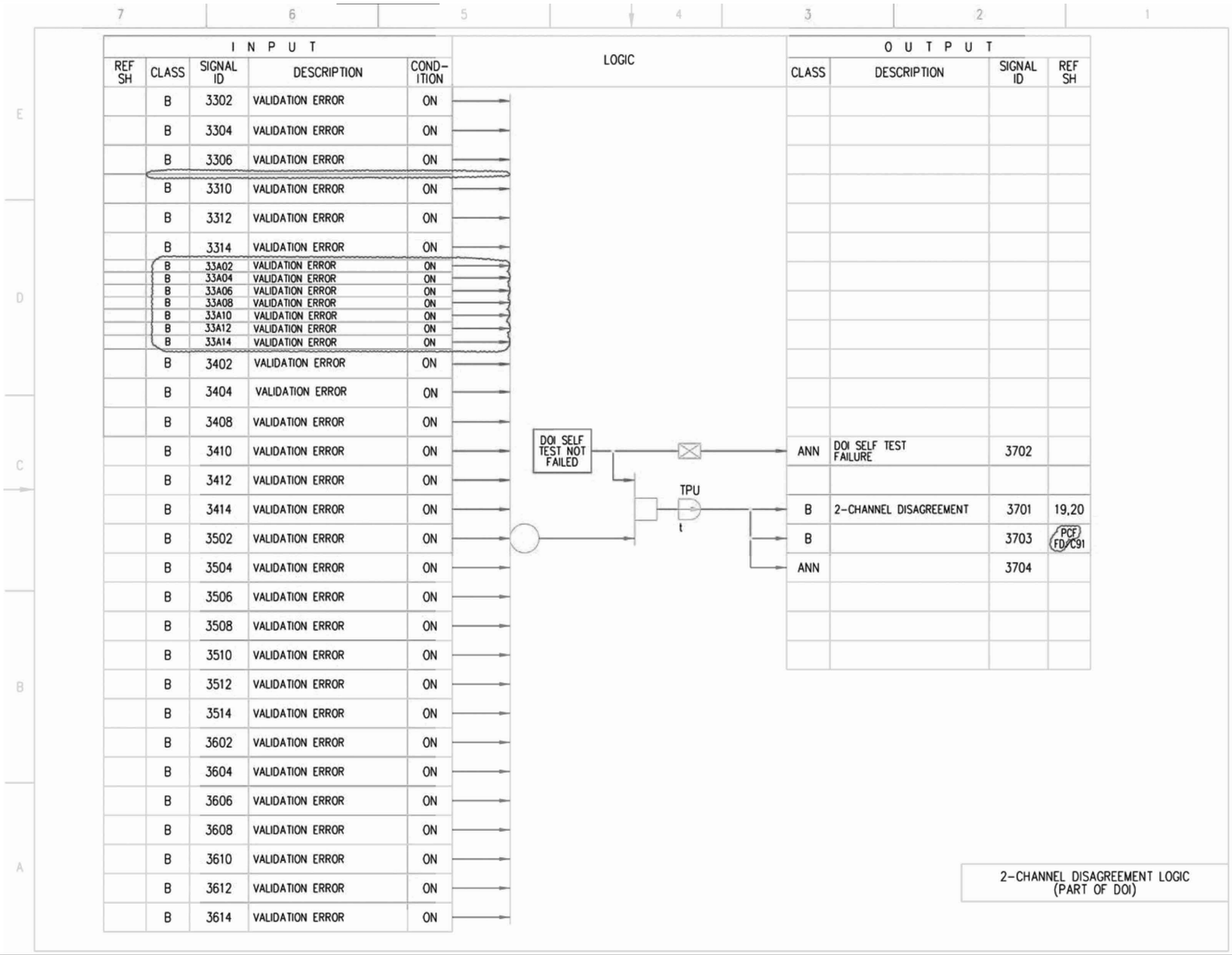


Figure 7.7-3 Rod Control and Information System IBD (Sheet 37 of 87)

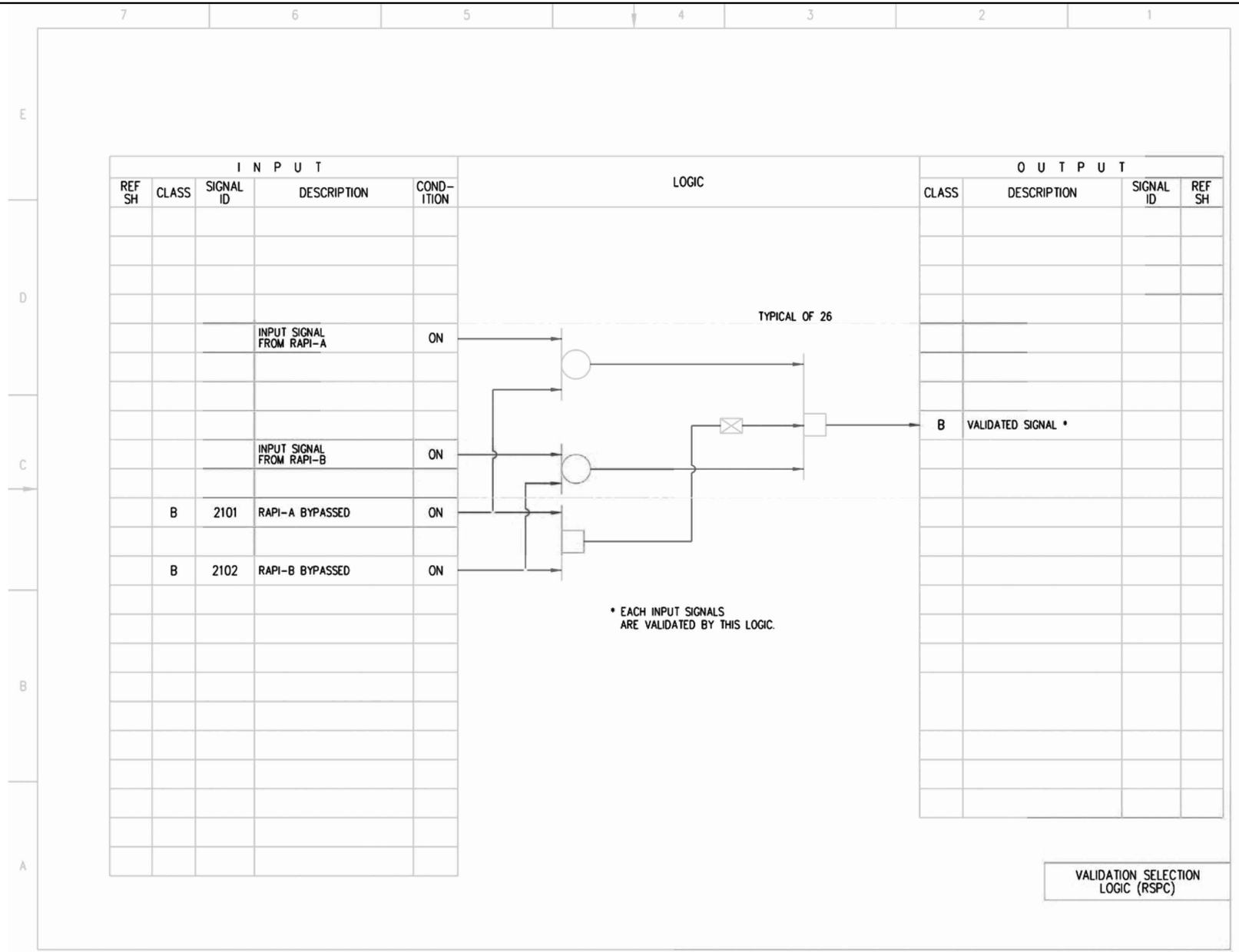


Figure 7.7-3 Rod Control and Information System IBD (Sheet 37a of 87)

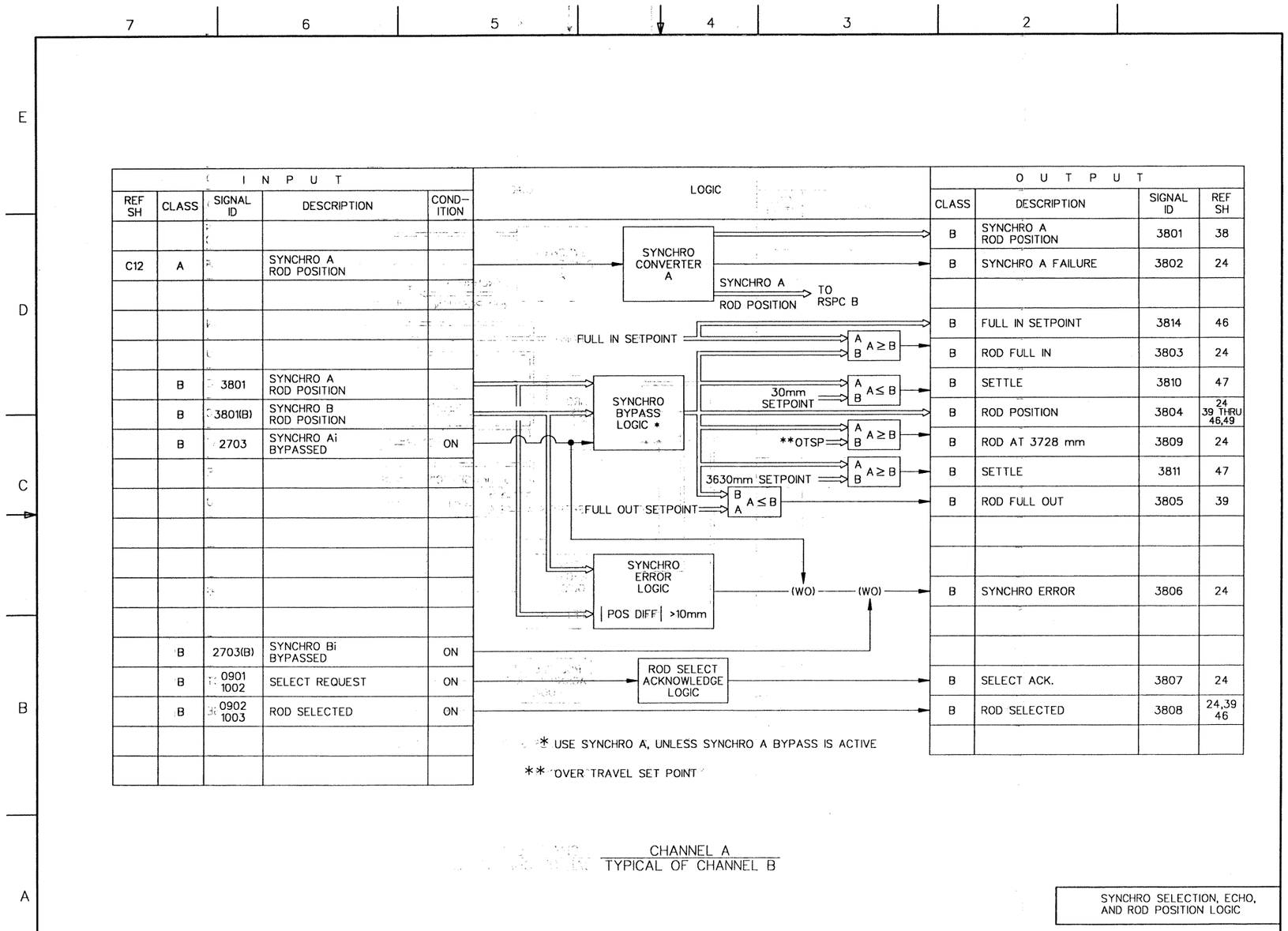


Figure 7.7-3 Rod Control and Information System IBD (Sheet 38 of 87)

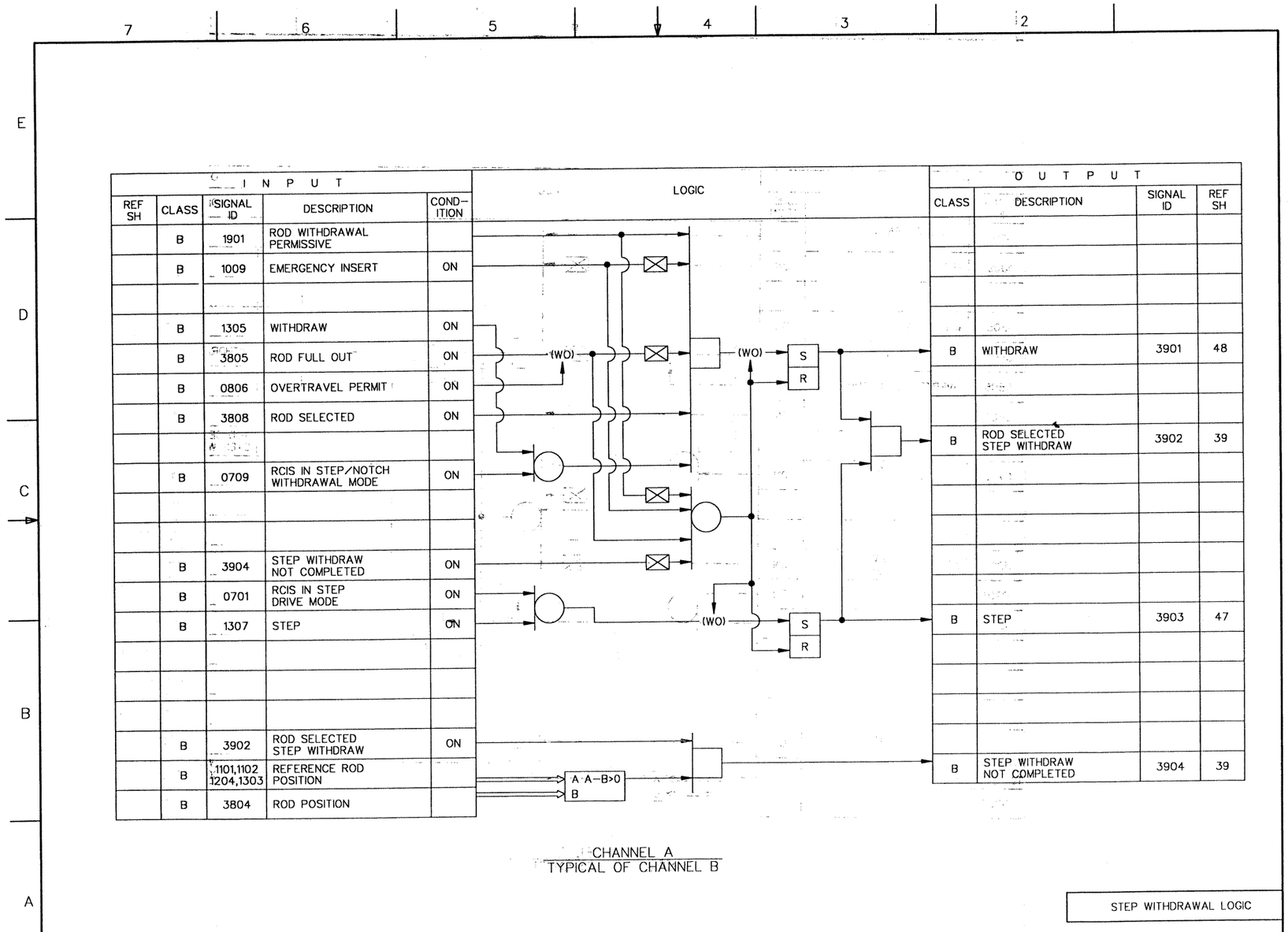


Figure 7.7-3 Rod Control and Information System IBD (Sheet 39 of 87)

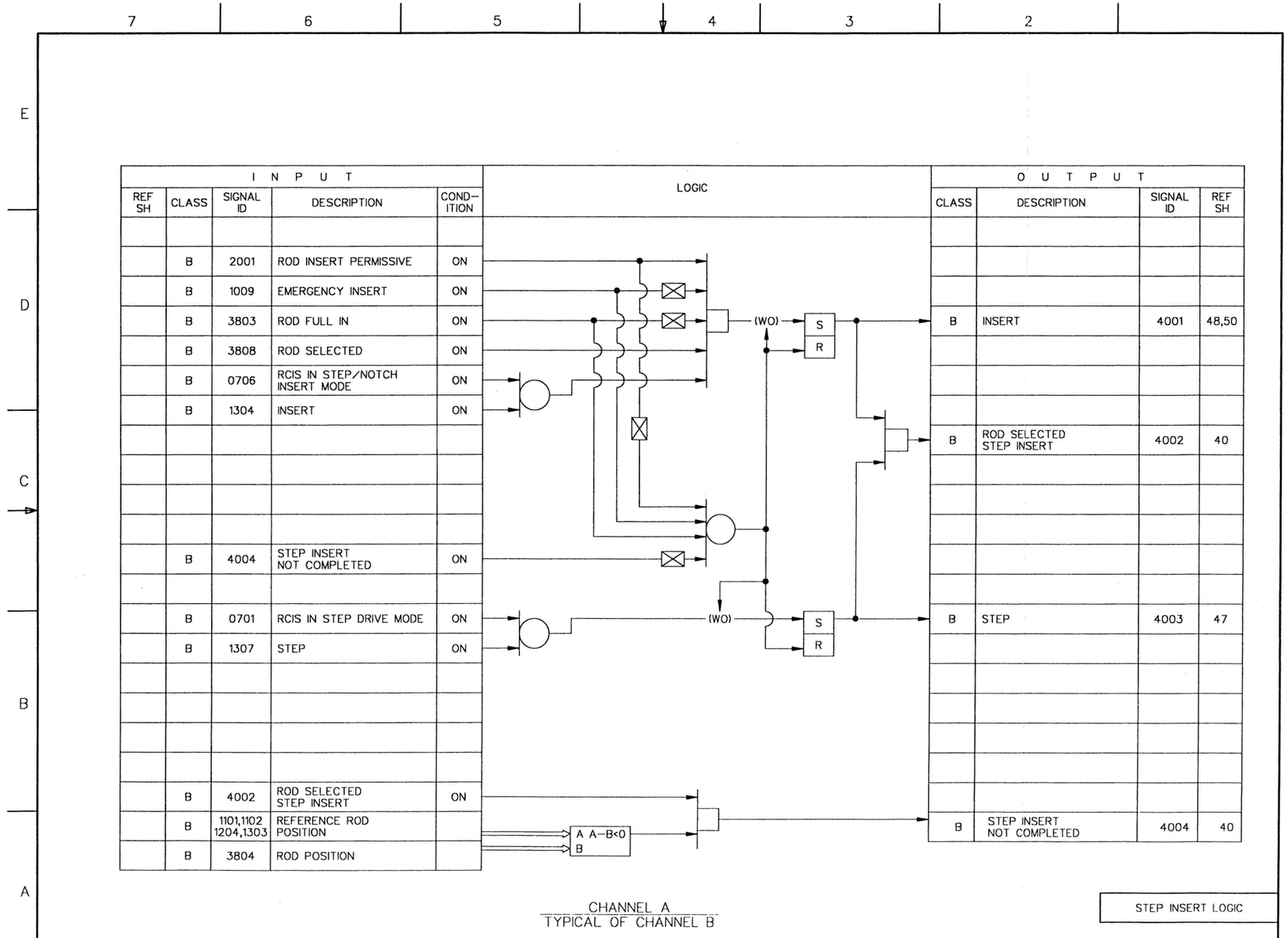


Figure 7.7-3 Rod Control and Information System IBD (Sheet 40 of 87)

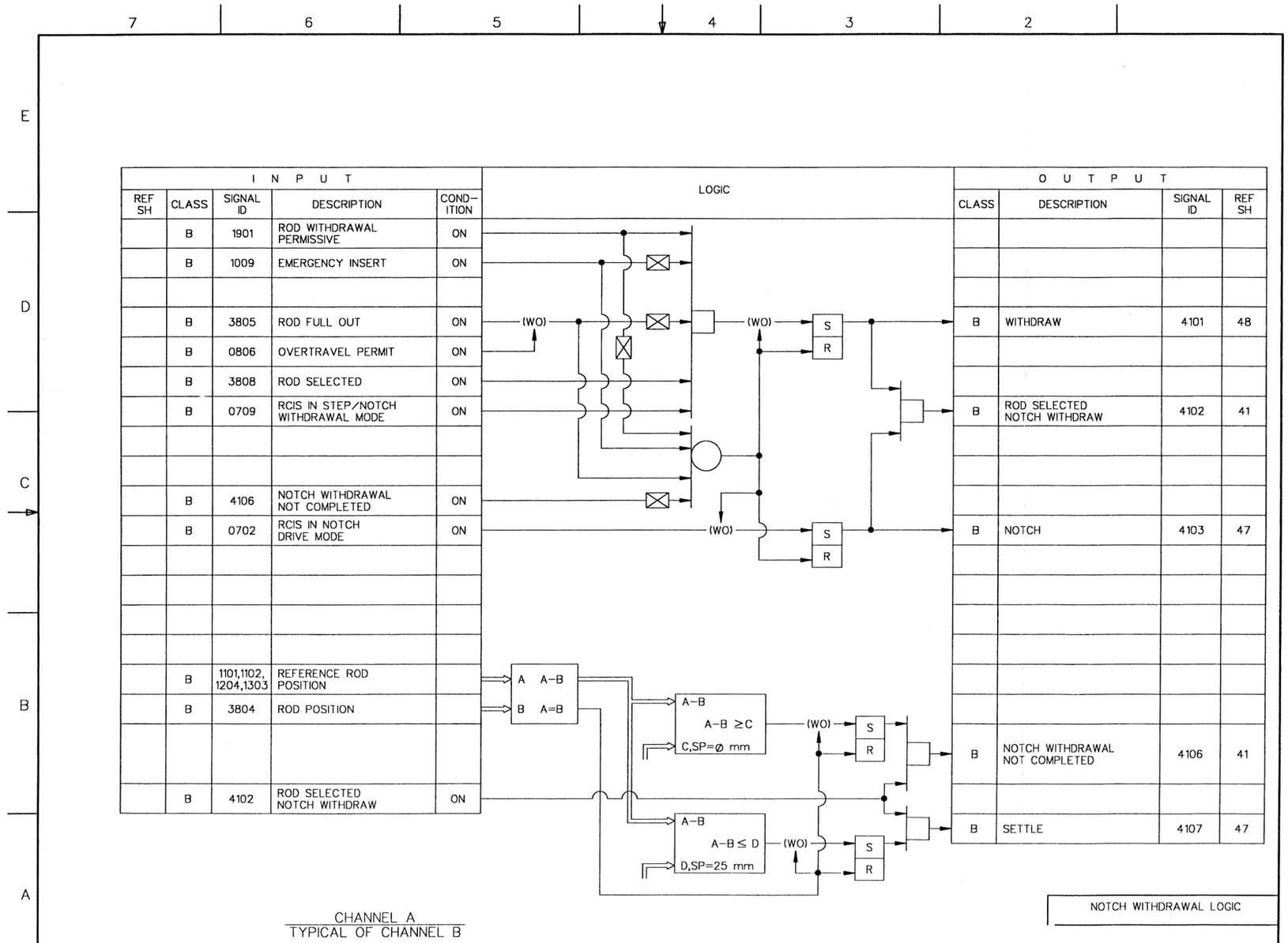


Figure 7.7-3 Rod Control and Information System IBD (Sheet 41 of 87)

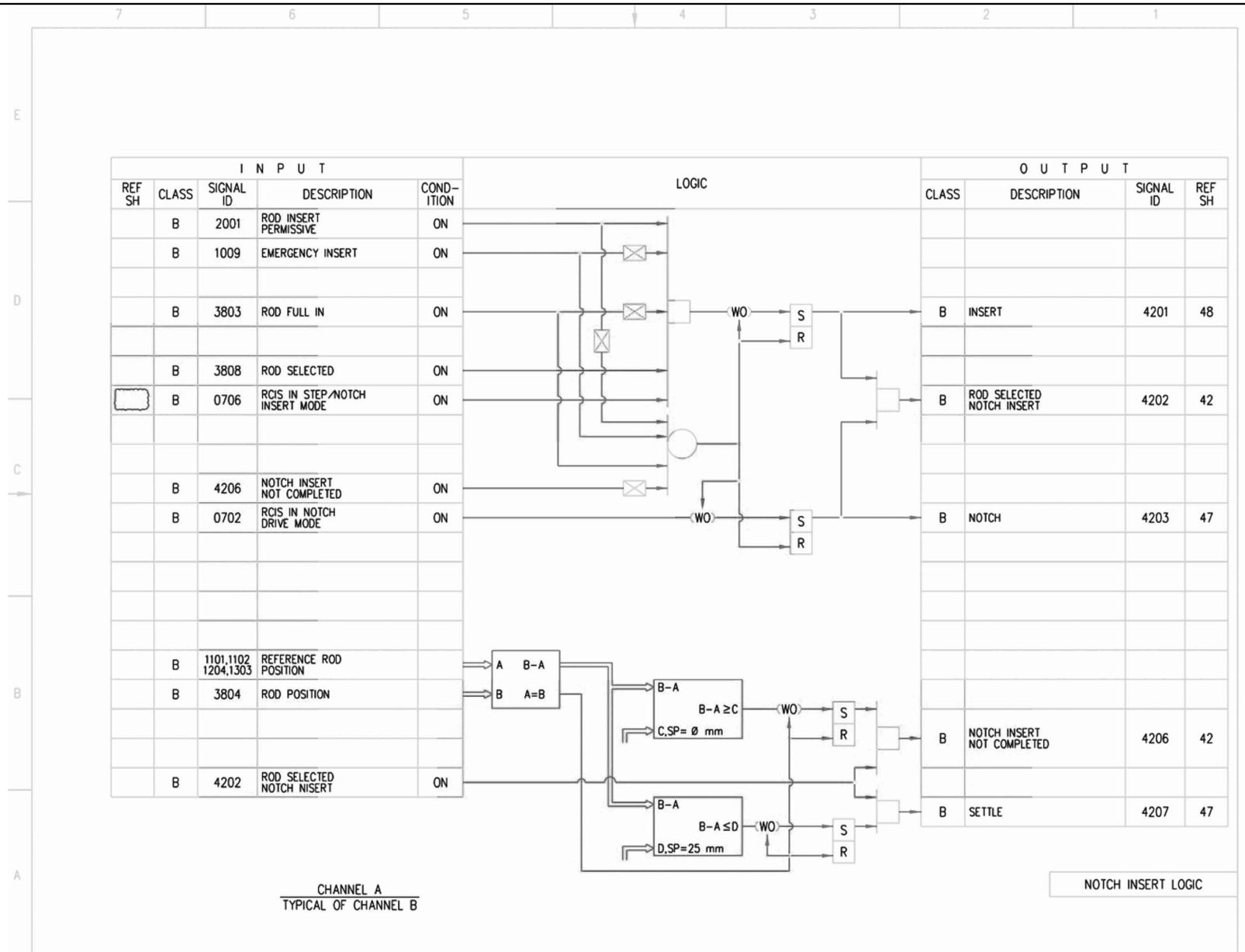


Figure 7.7-3 Rod Control and Information System IBD (Sheet 42 of 87)

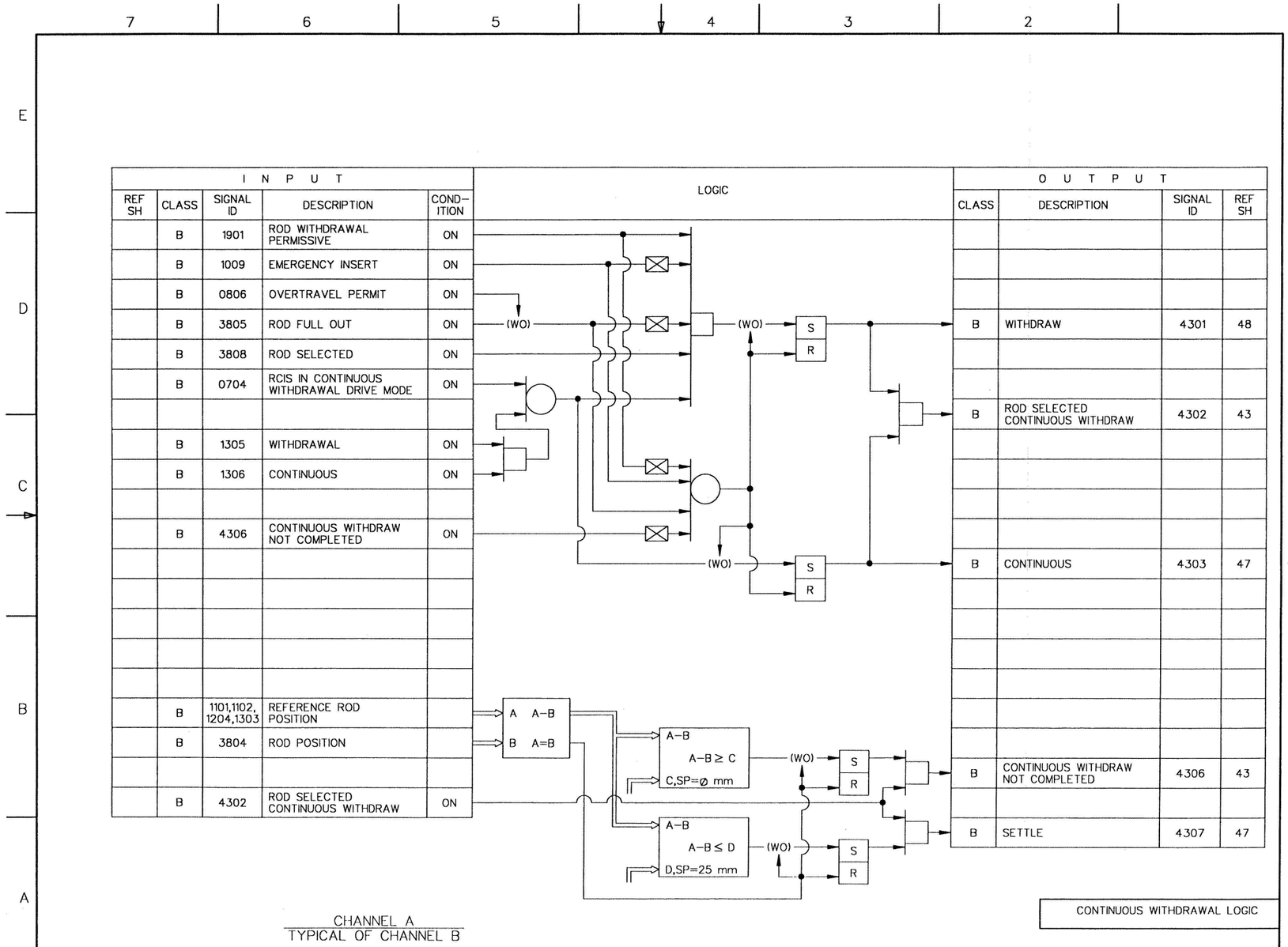


Figure 7.7-3 Rod Control and Information System IBD (Sheet 43 of 87)

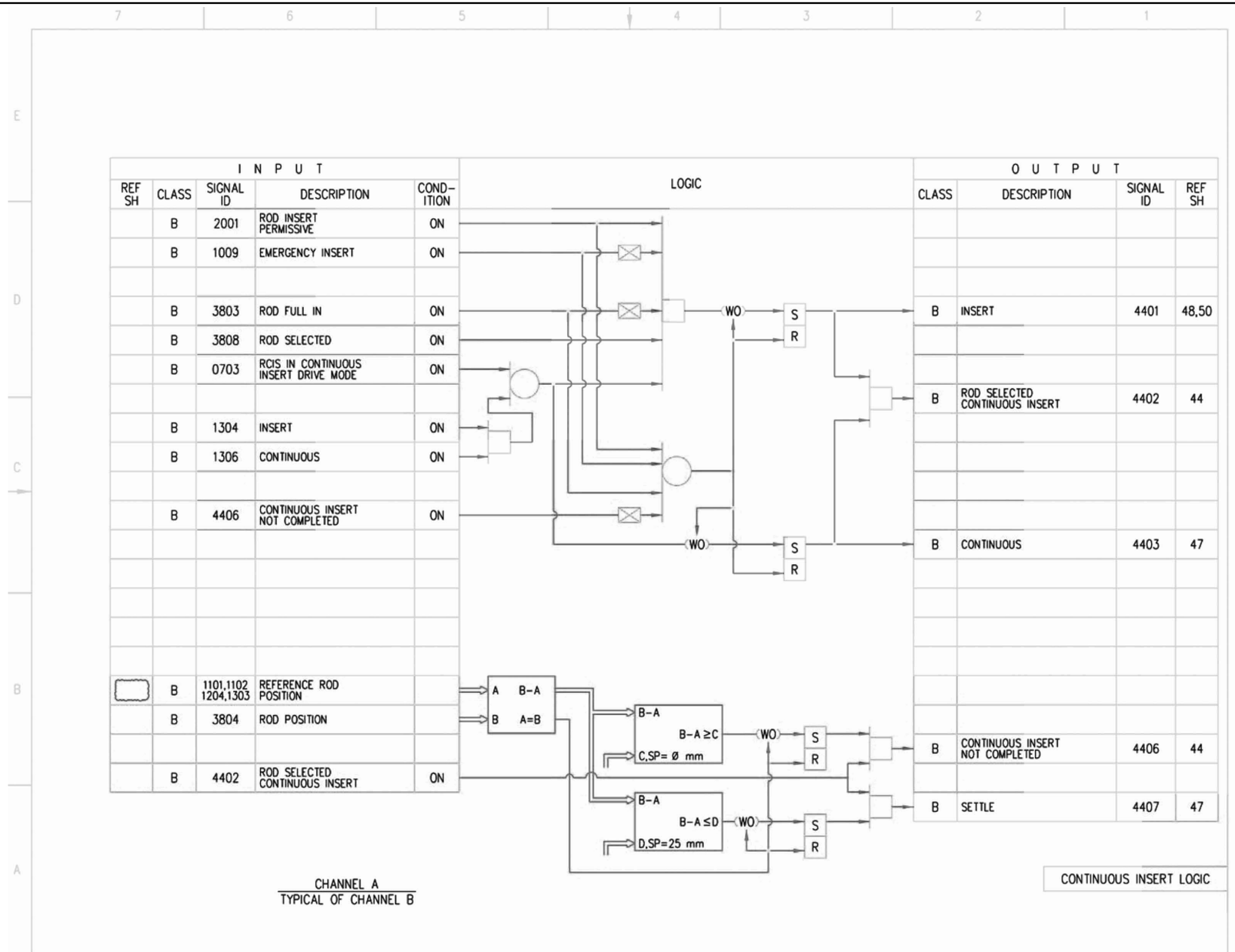


Figure 7.7-3 Rod Control and Information System IBD (Sheet 44 of 87)

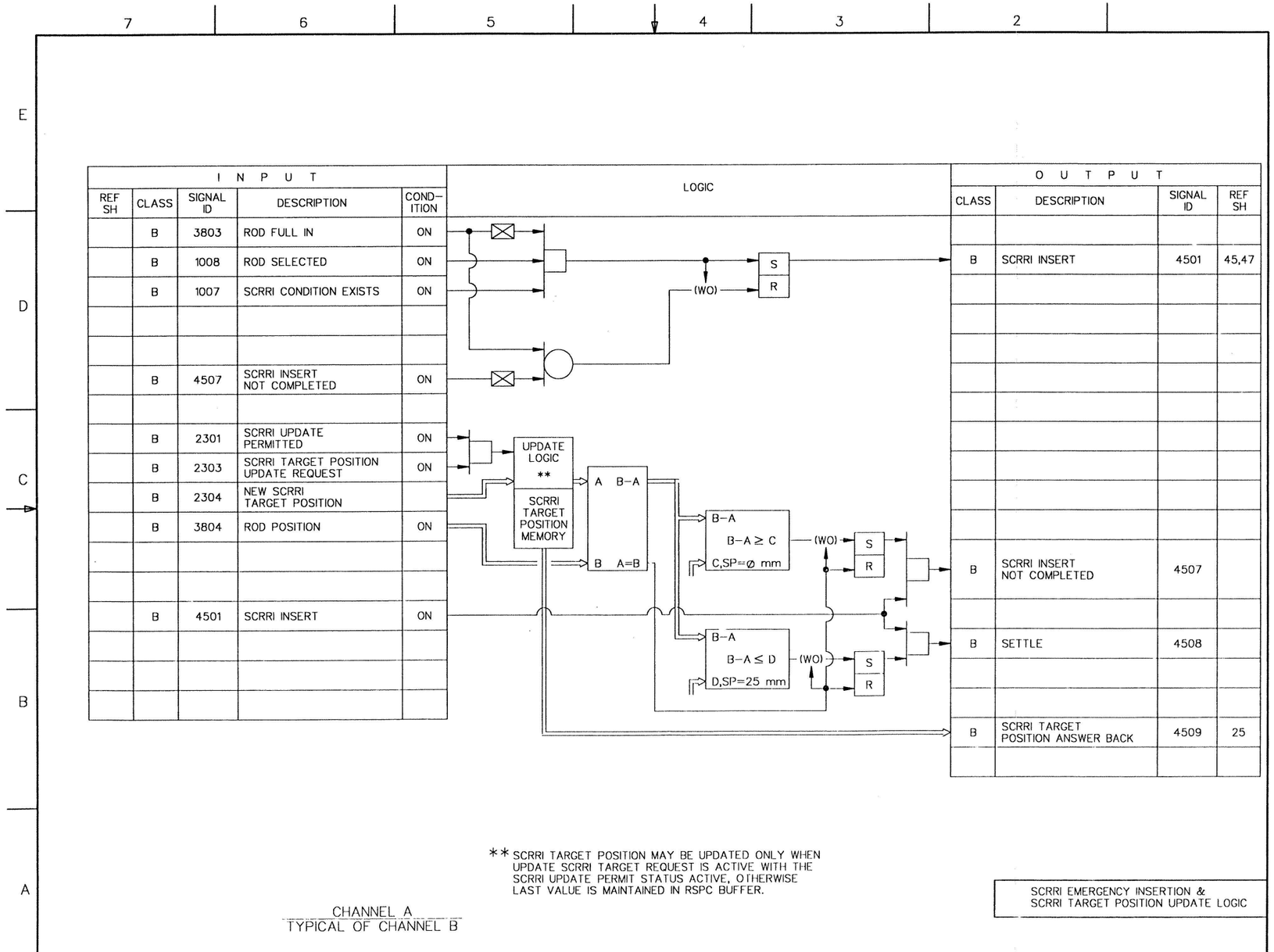


Figure 7.7-3 Rod Control and Information System IBD (Sheet 45 of 87)

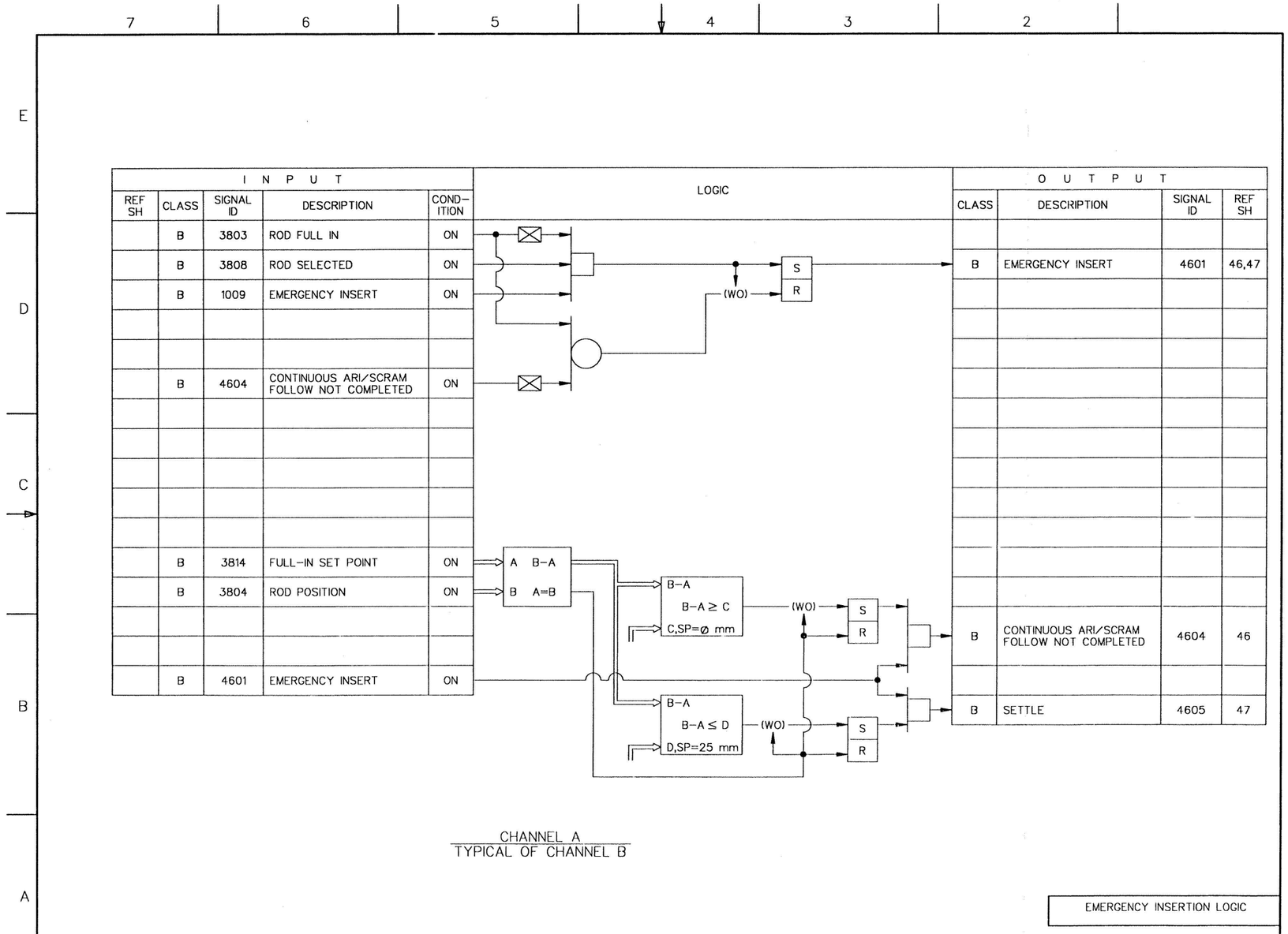
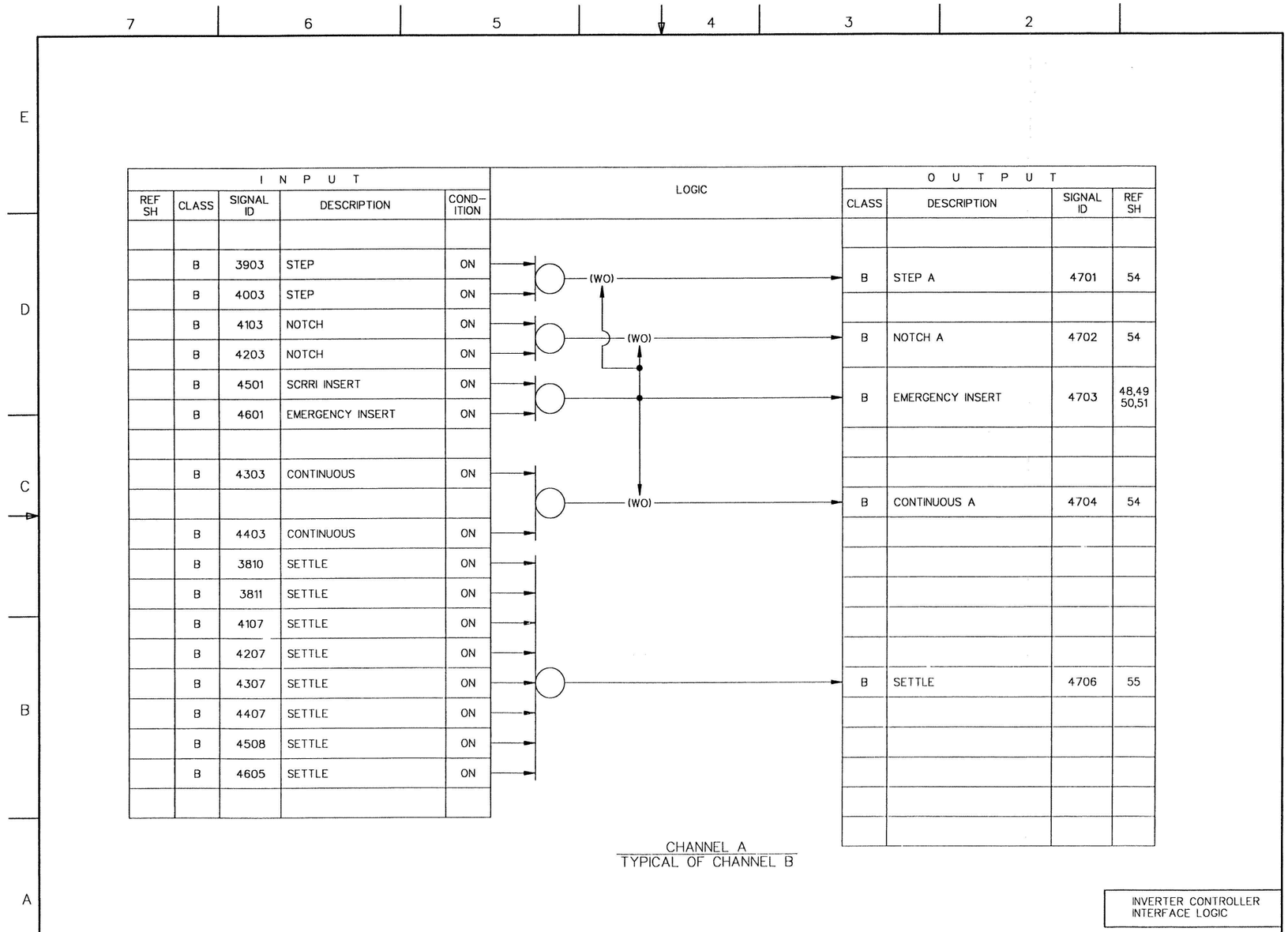


Figure 7.7-3 Rod Control and Information System IBD (Sheet 46 of 87)



INPUT					OUTPUT			
REF SH	CLASS	SIGNAL ID	DESCRIPTION	COND-ITION	CLASS	DESCRIPTION	SIGNAL ID	REF SH
	B	3903	STEP	ON	B	STEP A	4701	54
	B	4003	STEP	ON				
	B	4103	NOTCH	ON	B	NOTCH A	4702	54
	B	4203	NOTCH	ON				
	B	4501	SCRRI INSERT	ON	B	EMERGENCY INSERT	4703	48,49 50,51
	B	4601	EMERGENCY INSERT	ON				
	B	4303	CONTINUOUS	ON	B	CONTINUOUS A	4704	54
	B	4403	CONTINUOUS	ON				
	B	3810	SETTLE	ON				
	B	3811	SETTLE	ON				
	B	4107	SETTLE	ON				
	B	4207	SETTLE	ON				
	B	4307	SETTLE	ON	B	SETTLE	4706	55
	B	4407	SETTLE	ON				
	B	4508	SETTLE	ON				
	B	4605	SETTLE	ON				

Figure 7.7-3 Rod Control and Information System IBD (Sheet 47 of 87)

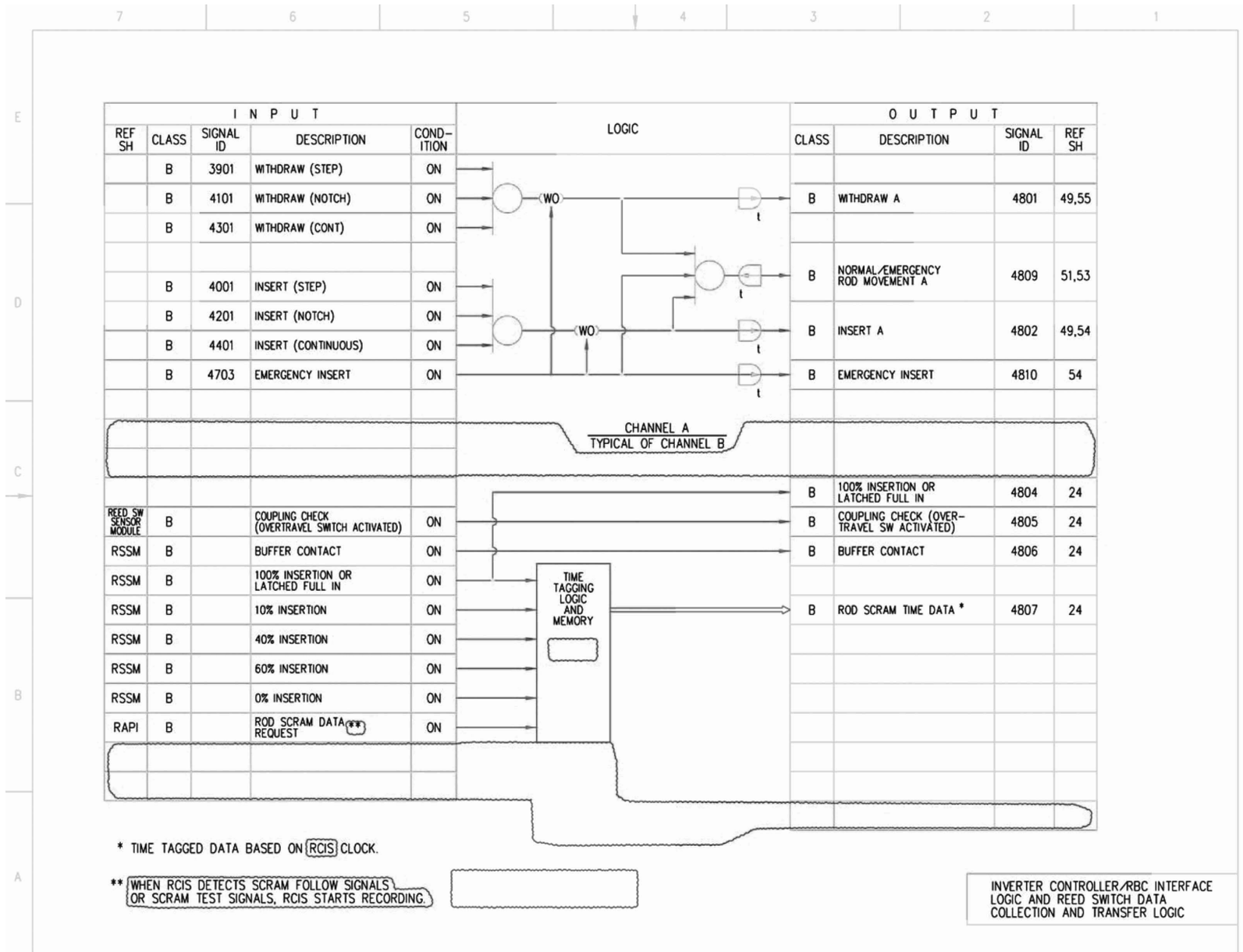
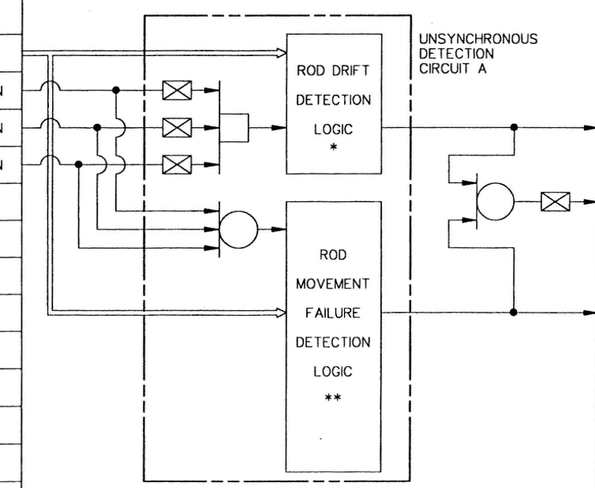


Figure 7.7-3 Rod Control and Information System IBD (Sheet 48 of 87)

INPUT					LOGIC	OUTPUT			
REF SH	CLASS	SIGNAL ID	DESCRIPTION	COND-ITION		CLASS	DESCRIPTION	SIGNAL ID	REF SH
	B	3804	ROD POSITION			B	DRIFT DETECTION	4901	24
	B	4703	EMERGENCY INSERT	ON		B	NO UNSYNCHRONOUS DETECTION	4902	54
	B	4801	WITHDRAW	ON		B	ROD MOVEMENT FAILURE	4903	24
	B	4802	INSERT	ON					



CHANNEL A
TYPICAL OF CHANNEL B

* DRIFT DETECTION OUTPUT BECOMES HIGH WHEN ROD POSITION CHANGES IN THE ABSENCE OF WITHDRAW/INSERT/EMERGENCY INSERT SIGNALS.

** ROD MOVEMENT FAILURE OUTPUT BECOMES HIGH WHEN ROD POSITION DOES NOT CHANGE WHILE ROD MOVEMENT COMMANDS ARE PRESENT.

UNSYNCHRONOUS DETECTION LOGIC

Figure 7.7-3 Rod Control and Information System IBD (Sheet 49 of 87)

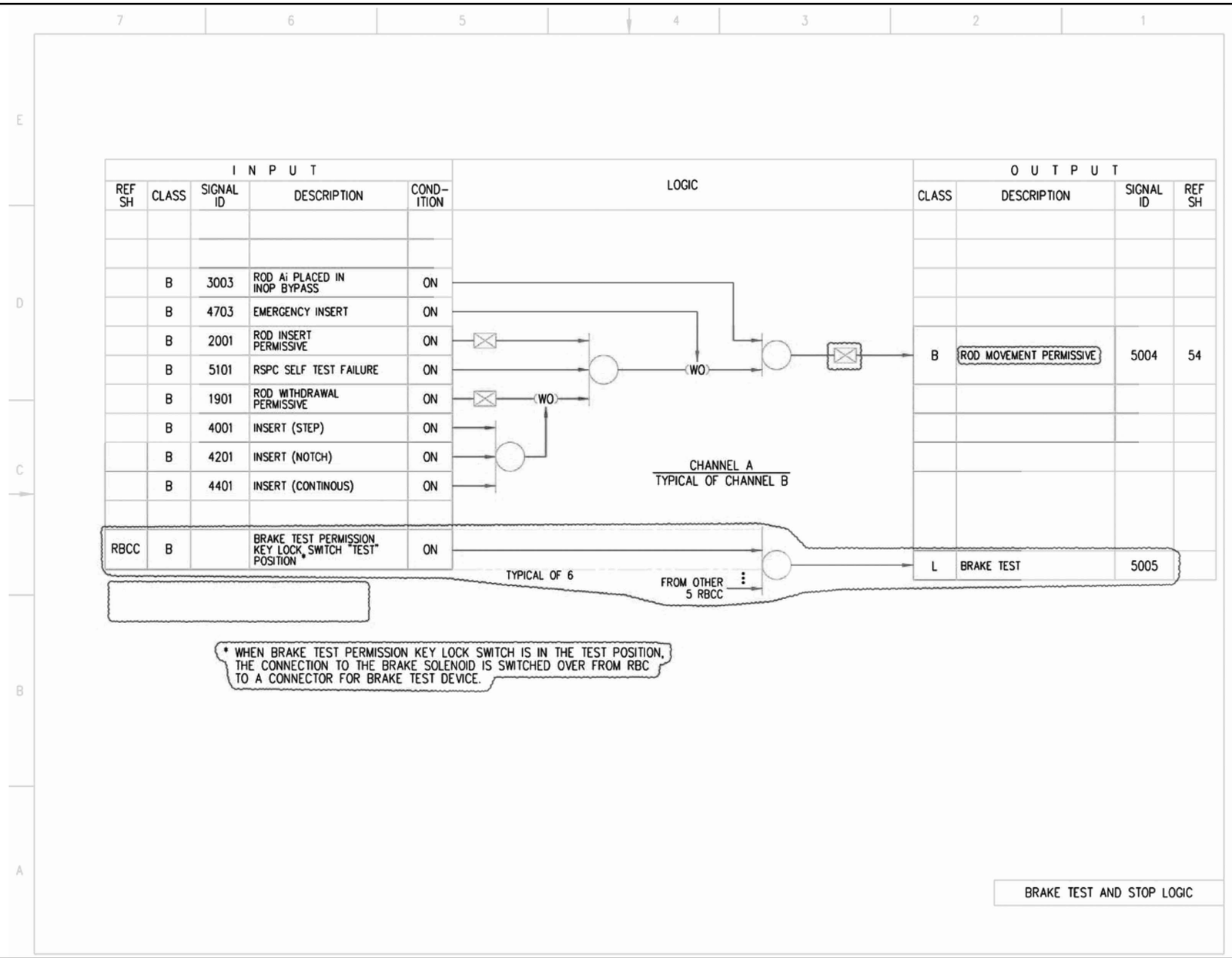
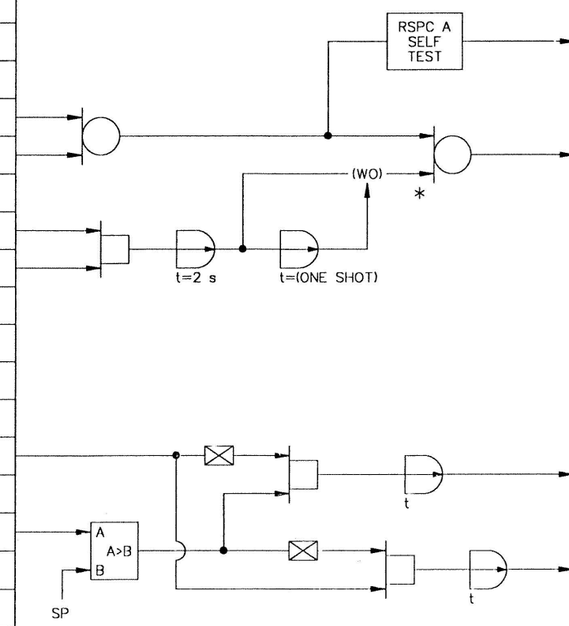


Figure 7.7-3 Rod Control and Information System IBD (Sheet 50 of 87)

INPUT					LOGIC	OUTPUT			
REF SH	CLASS	SIGNAL ID	DESCRIPTION	COND-ITION		CLASS	DESCRIPTION	SIGNAL ID	REF SH
						B	RSPC SELF TEST FAILURE	5101	24,50
RAPI	B		RESET A	ON					
RSPC A	B		LOCAL RESET	ON		D	RESET	5102	55
	B	5505	IC TROUBLE	ON					
	B	4703	EMERGENCY INSERT	ON					
	B	4809	NORMAL/EMERGENCY ROD MOVEMENT A	ON		D	ABNORMAL BRAKE SOLENOID ENERGIZATION	5103	24
	A	5302	BRAKE CURRENT SENSE SIGNAL			B	BRAKE DISENGAGEMENT FAILURE	5104	24



* THIS PROVIDES AUTOMATIC RESTART CAPABILITY IF EITHER ARI CONDITION/SCRAM FOLLOW CONDITION OR SCRRI EXIST.

CHANNEL A
TYPICAL OF CHANNEL B

DIAGNOSTICS AND RESTART LOGIC

Figure 7.7-3 Rod Control and Information System IBD (Sheet 51 of 87)

INPUT					LOGIC	OUTPUT			
REF SH	CLASS	SIGNAL ID	DESCRIPTION	COND-ITION		CLASS	DESCRIPTION	SIGNAL ID	REF SH
	B	5403	STEP	ON	→	B	STEP	5201	25
	B	5404	NOTCH	ON	→	B	NOTCH	5202	25
	B	5402	CONTINOUS	ON	→	B	CONTINOUS	5203	25
	B	5503	SETTLE	ON	→	B	SETTLE	5204	25
	B	5401	EMERGENCY INSERT	ON	→	B	EMERGENCY INSERT	5205	25
	B	5406	INSERT	ON	→	B	INSERT	5206	25
	B	5502	WITHDRAW	ON	→	B	WITHDRAW	5207	25
	B	5405	STOP	ON	→	B	STOP	5208	25
	B	5802	INVERTER TROUBLE	ON	→	B	INVERTER TROUBLE	5209	25
	B	5505	INVERTER CONTROLLER TROUBLE	ON	→	B	INVERTER CONTROLLER TROUBLE	5210	25

CHANNEL A
TYPICAL OF CHANNEL B

IC SIGNAL
TRANSFER TO RAPI

Figure 7.7-3 Rod Control and Information System IBD (Sheet 52 of 87)

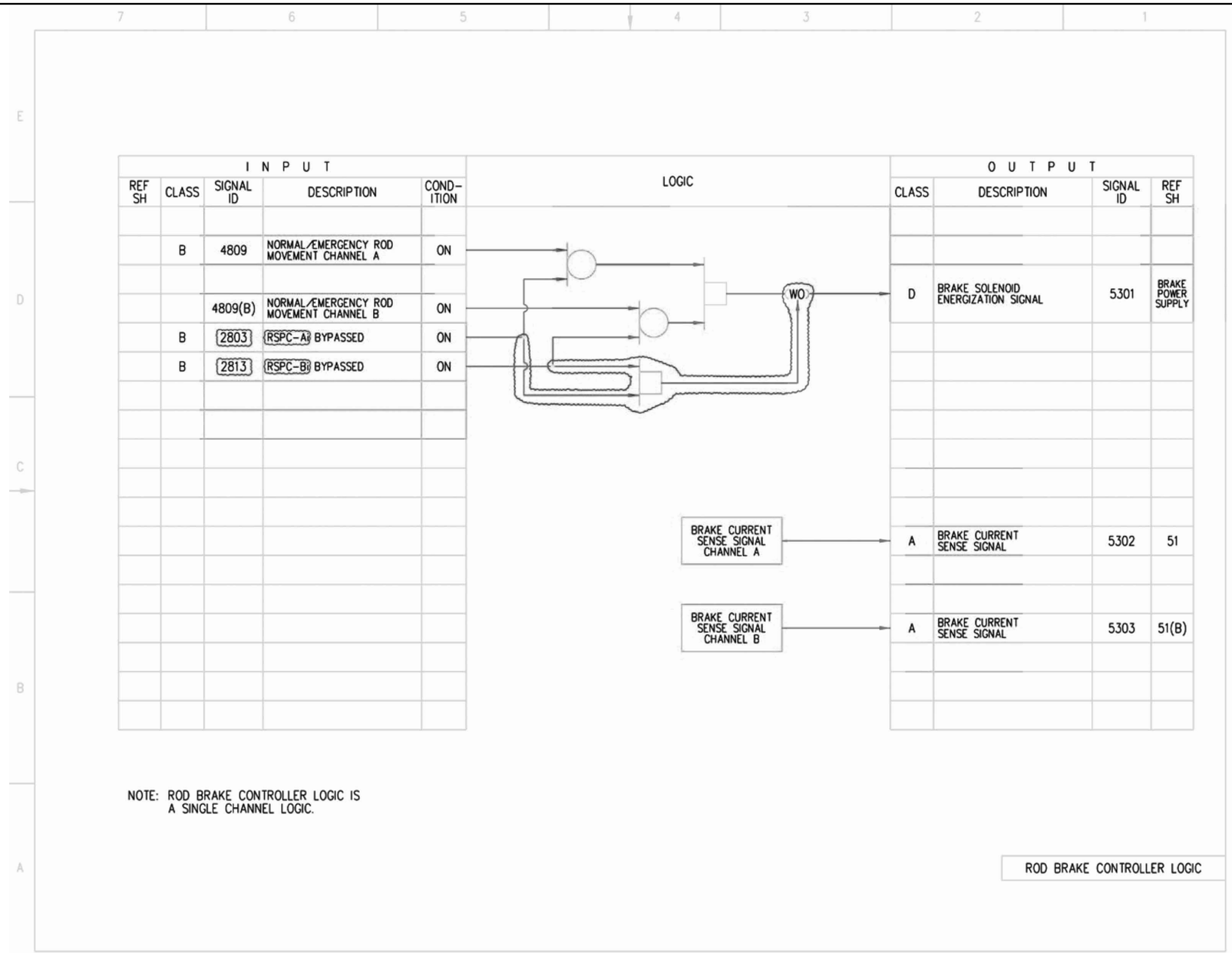


Figure 7.7-3 Rod Control and Information System IBD (Sheet 53 of 87)

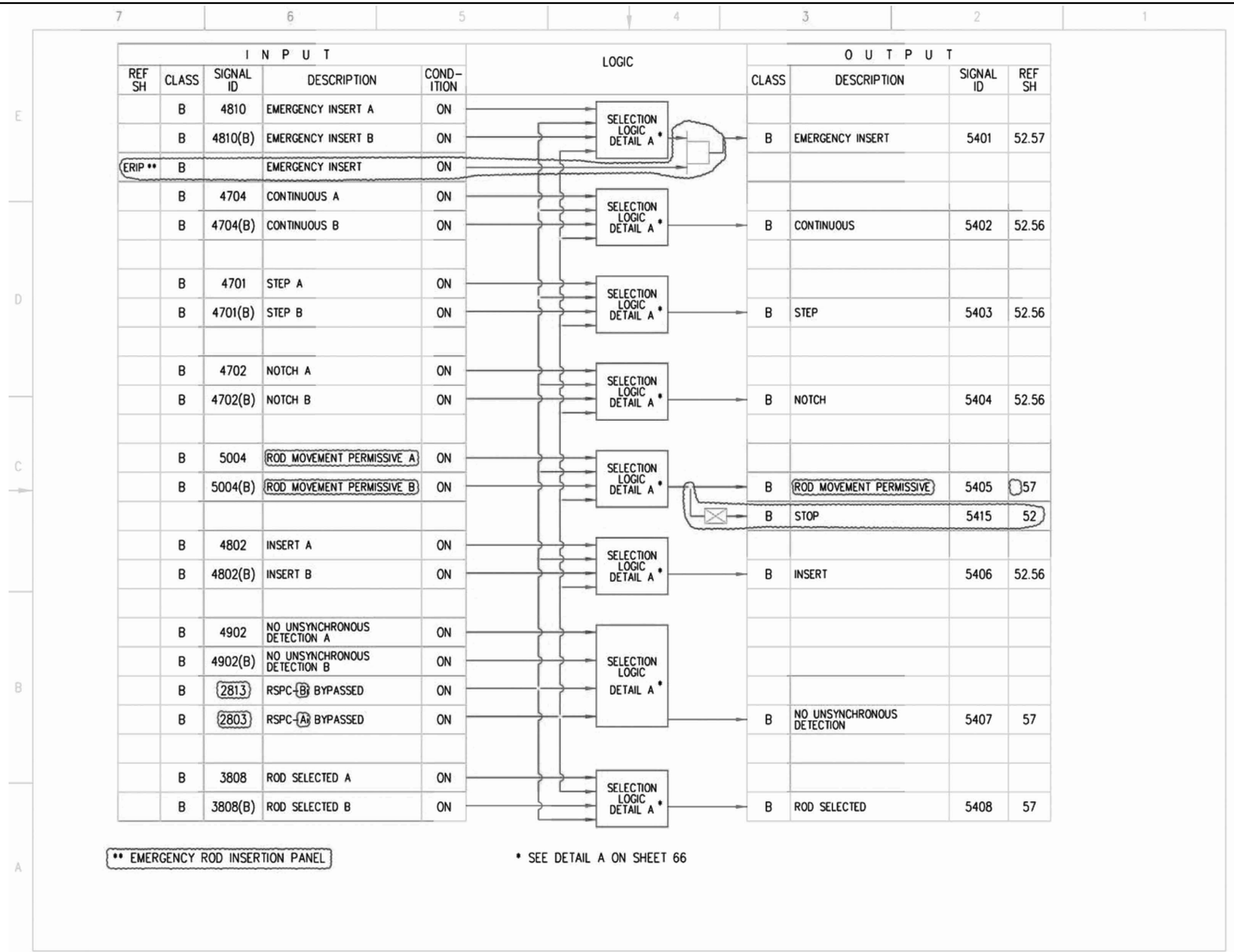


Figure 7.7-3 Rod Control and Information System IBD (Sheet 54 of 87)

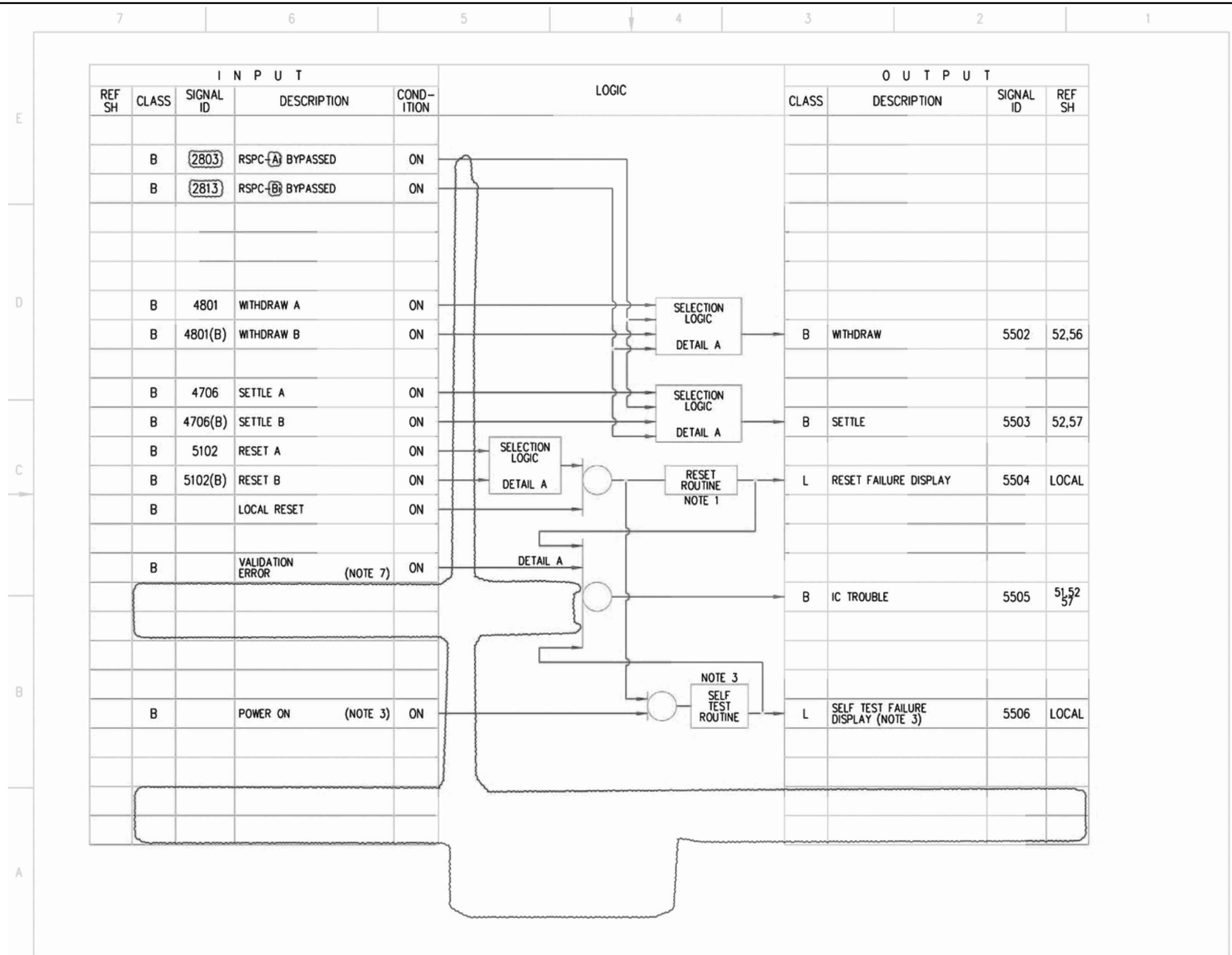
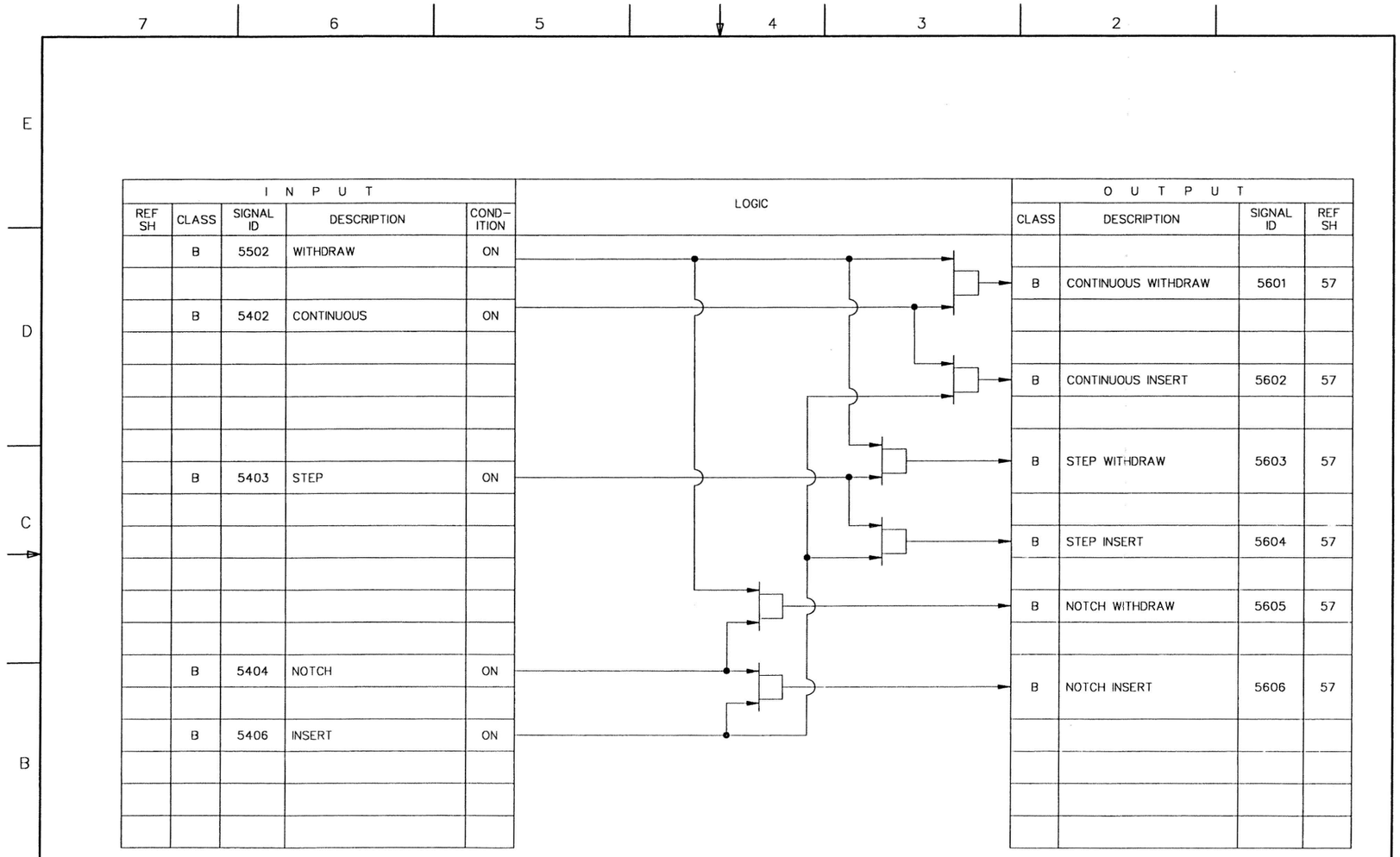


Figure 7.7-3 Rod Control and Information System IBD (Sheet 55 of 87)



INPUT					OUTPUT			
REF SH	CLASS	SIGNAL ID	DESCRIPTION	COND-ITION	CLASS	DESCRIPTION	SIGNAL ID	REF SH
	B	5502	WITHDRAW	ON				
					B	CONTINUOUS WITHDRAW	5601	57
	B	5402	CONTINUOUS	ON				
					B	CONTINUOUS INSERT	5602	57
					B	STEP WITHDRAW	5603	57
	B	5403	STEP	ON				
					B	STEP INSERT	5604	57
					B	NOTCH WITHDRAW	5605	57
	B	5404	NOTCH	ON	B	NOTCH INSERT	5606	57
	B	5406	INSERT	ON				

Figure 7.7-3 Rod Control and Information System IBD (Sheet 56 of 87)

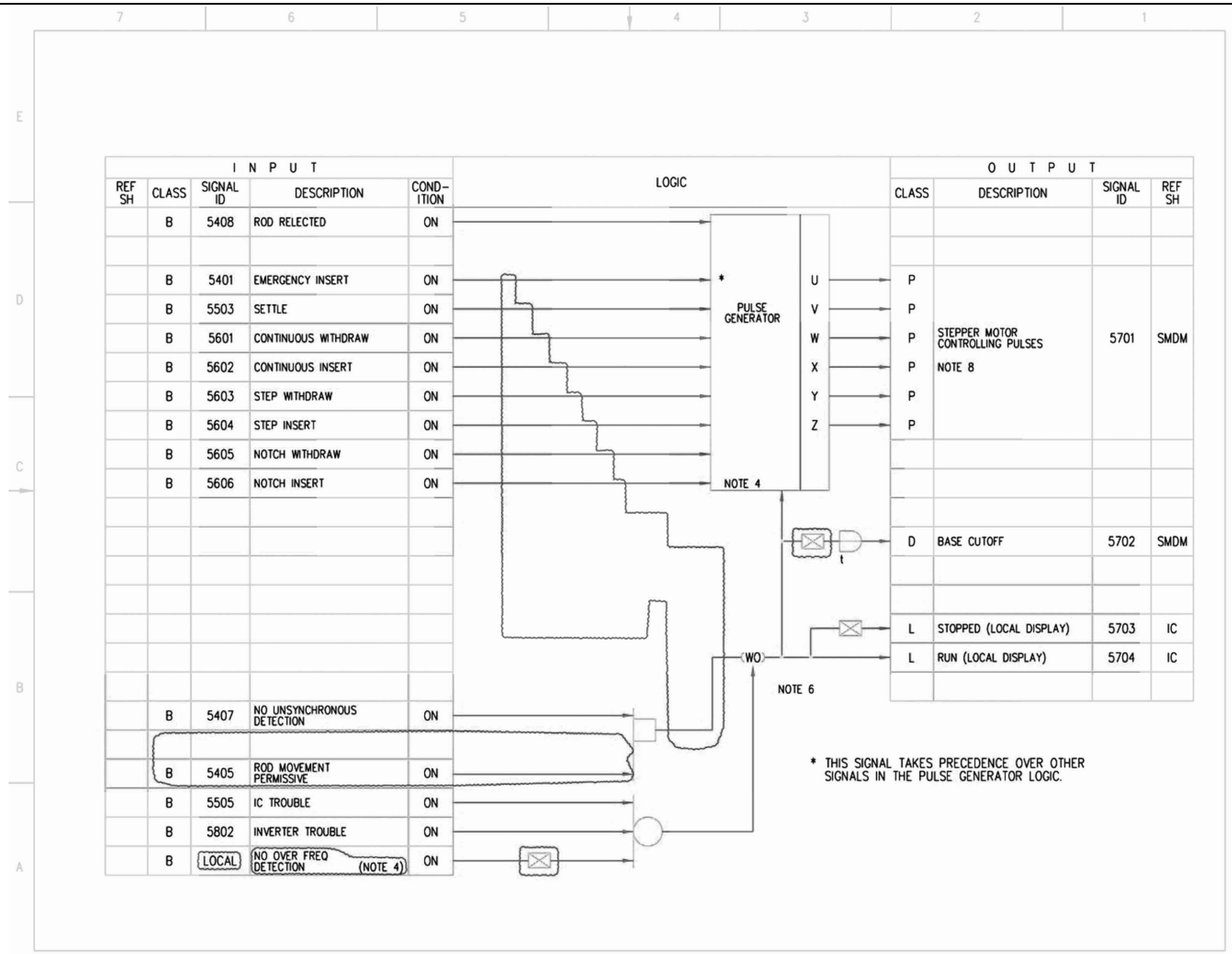
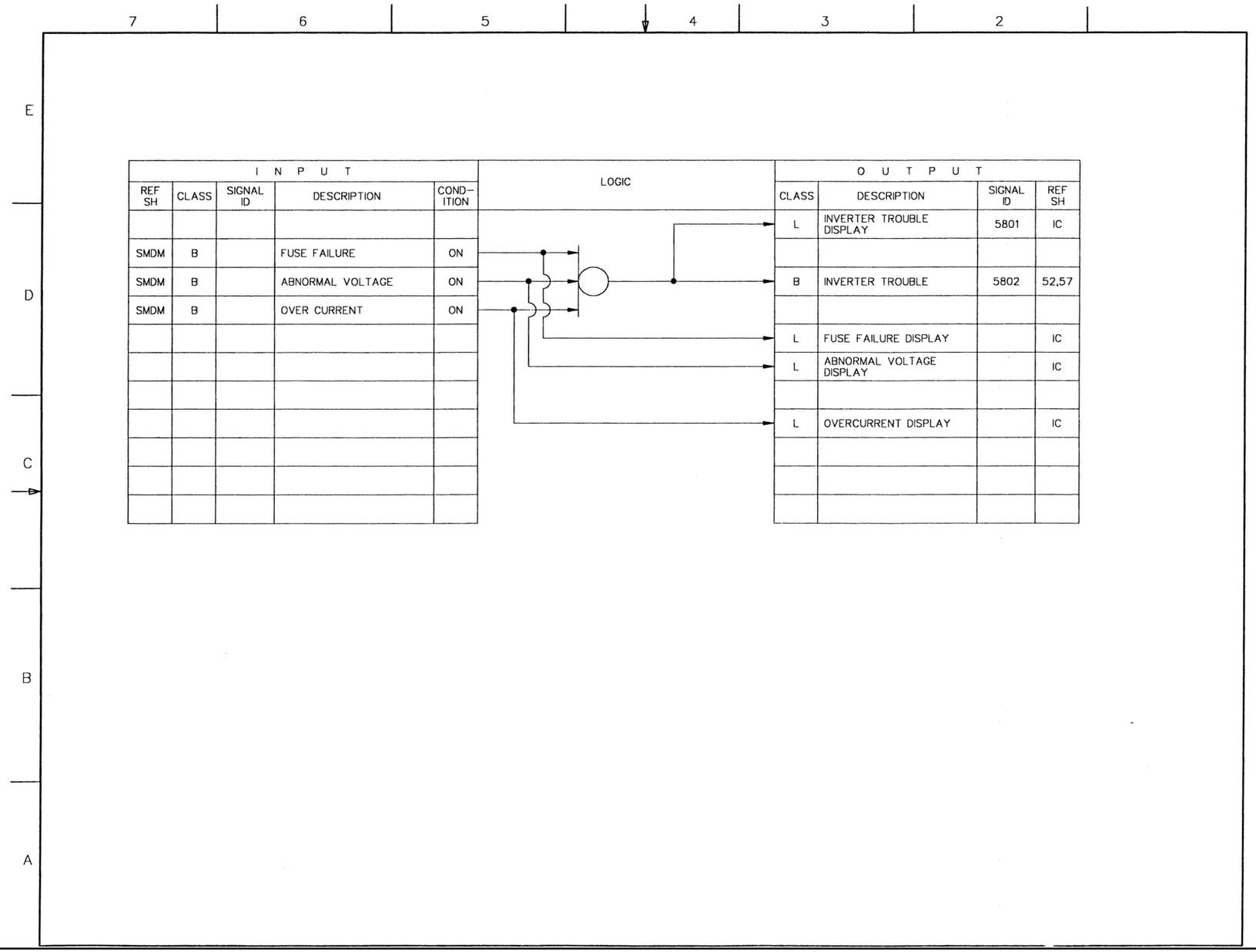


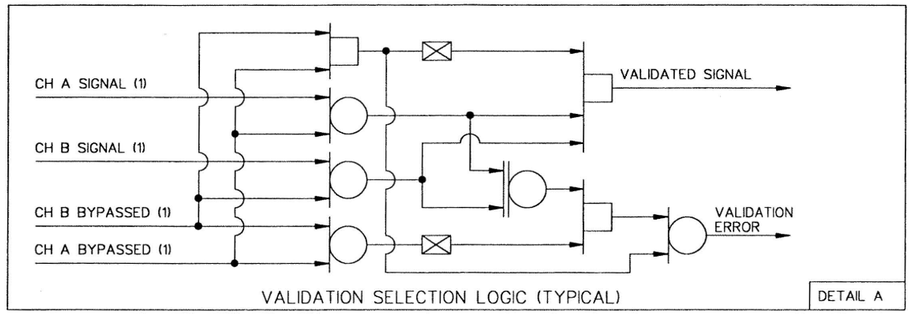
Figure 7.7-3 Rod Control and Information System IBD (Sheet 57 of 87)



INPUT				
REF SH	CLASS	SIGNAL ID	DESCRIPTION	COND-ITION
SMDM	B		FUSE FAILURE	ON
SMDM	B		ABNORMAL VOLTAGE	ON
SMDM	B		OVER CURRENT	ON

OUTPUT			
CLASS	DESCRIPTION	SIGNAL ID	REF SH
L	INVERTER TROUBLE DISPLAY	5801	IC
B	INVERTER TROUBLE	5802	52,57
L	FUSE FAILURE DISPLAY		IC
L	ABNORMAL VOLTAGE DISPLAY		IC
L	OVERCURRENT DISPLAY		IC

Figure 7.7-3 Rod Control and Information System IBD (Sheet 58 of 87)



NOTES:

1. RESET FAILURE SIGNAL IS ISSUED BY IC WHEN THE RESET ROUTINES TO BE COMPLETED BY THE MICROPROCESSOR ARE NOT SUCCESFULLY ACCOMPLISHED. GENERATION OF THIS SIGNAL SHALL BE AN INTEGRAL PART OF THE RESET ROUTINES OF THE HARDWARE. THE IC SHALL CONDUCT AUTOMATICALLY A RESET ROUTINE WHEN RECOVERING FROM A PRIOR FAILURE/TROUBLE CONDITION.

2. THE IC HARDWARE SHALL UTILIZE A WATCHDOG TIMER TO MONITOR THE UPDATES OF EACH SIGNAL FROM RSPC. THE TIMER SHALL COUNTDOWN FROM A PREDETERMINED AMOUNT OF TIME TO 0 AND RESET TO (TIME TO BE DETERMINED IN DETAILED DESIGN PHASE) ms AUTOMATICALLY ON EVERY UPDATE OF SIGNAL. WHEN TIMER COUNTS DOWN TO ZERO ON ANY INPUT SIGNAL FROM THE RSPC, IT SHALL PROVIDE A TIME OUT SIGNAL.

3. SELF TEST FEATURES SHALL INCLUDE THE ROUTINES OF CHECKING THE PROCESSOR RAM, ROM AND BUFFERS. WHEN THE SELF TEST IS NOT COMPLETED SUCCESFULLY, THE IC HARDWARE SHALL ISSUE A SELF TEST FAILURE SIGNAL. SELF TEST SHALL BE EXECUTED WHEN THE IC POWER IS TURNED ON. THE IC RECEIVES A RESET COMMAND FROM RSM, OR THE IC RECOVERS FROM A PRIOR FAILURE/TROUBLE, AND ON A CONTINUOUS BASIS FROM THEN ON.

4. PULSE GENERATOR COMPRISES OF FREQUENCY LIMITER, PULSE DISTRIBUTOR AND OTHER NECESSARY HARDWARE. IT GENERATES APPROPRIATE PULSES CORRESPONDING TO THE INPUT DRIVE COMMAND TO PRODUCE THE REQUIRED SPEED PATTERN OF THE STEPPING MOTOR (SM) TO MOVE THE ROD TO THE REQUIRED POSITION APPROPRIATELY. THE OUTPUT OF THE PULSE GENERATOR IS ENABLED BY ALLOWABLE CONDITIONS, AS SHOWN, TO DRIVE THE STEPPING MOTOR.

5. ALGORITHM FOR IDENTIFIED FUNCTIONS AND LOGICS ARE DESCRIBED IN C11-4020 AND SCRAM TIME DATA IN C11-4010.

6. DEDICATED DISPLAY INDICATION SHALL BE PROVIDED FOR RUN, STOPPED, IC TROUBLE, INVERTER TROUBLE AND RESET CONDITIONS. IN THE EVENT OF EITHER A IC TROUBLE OR INVERTER TROUBLE CONDITION, THE FAILURE CAUSING SUCH CONDITION SHALL BE DISPLAYED.

7. VALIDATION ERROR SIGNAL IS GENERATED WHEN CHANNEL A & B ARE NOT BYPASSED AND CHANNELS A & B SIGNALS DO NOT MATCH. TYPICAL OF THESE SIGNALS ARE "ORED" TO PRODUCE ONE VALIDATION ERROR SIGNAL TO INDICATE IC TROUBLE.

8. THE CHARACTERISTICS OF THE UVWXYZ PULSES ARE DETERMINED BY THE IC (PULSES GENERATOR) ARCHITECTURE, THE INVERTER DESIGN AND THE PERFORMANCE CHARACTERISTICS CURVES OF THE SM, TO ACCURATELY MOVE THE CONTROL ROD BY SPECIFIED DISTANCE AS DEFINED BY THE RC&IS DESIGN.

Figure 7.7-3 Rod Control and Information System IBD (Sheet 59 of 87)

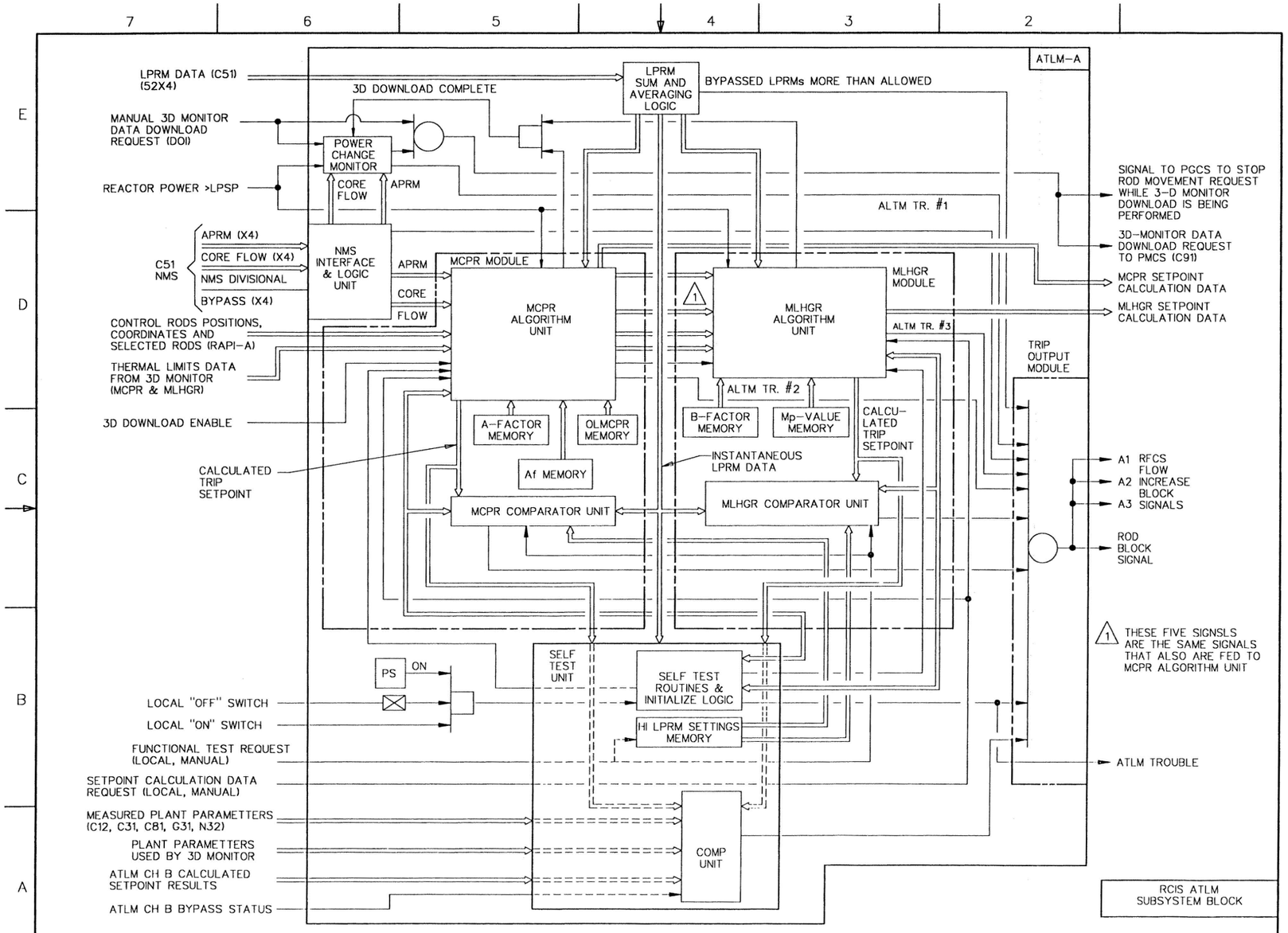


Figure 7.7-3 Rod Control and Information System IBD (Sheet 60 of 87)