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September 22nd, 2010

U.S. Nuclear Regulatory Commission
Office of Nuclear Reactor Regulation
Division of Policy and Rulemaking
11555 Rockville Pike,
Rockville, Maryland 20852

Subject: Supporting documents for Safety Evaluation Report of PP901-000-01, REVISION C, "HFC-6000 SAFETY SYSTEM"

Reference: HFC-6000 Safety System

Docket number: 000-00731

Enclosed is the document, RR901-000-44, "ERD111 Qualification Seismic Analysis Report", Rev A. which Doosan HF Controls (HFC) made available to the Commission.

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ERD111 Seismic Qualification Analysis Report

RR901-000-44

Rev A

Effective Date: 7/30/2010

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Reviewer: Ivan Chow

Approval: Charles McKinney

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Revision History

Date	Revision	Author	Changes
6/25/2010	A	J Taylor	

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1.0 GENERAL

This document covers an analysis for dynamic qualification of the ERD111 Test Specimen, which has been presented to the NRC for generic qualification for use in nuclear safety systems. The base control system hardware and its digital functions were subjected to seismic testing between 9/22/2004 and 9/23/2004. Although both analog and digital I/O modules were present at that time, detailed test data accumulated at that time did not establish all of the performance characteristics desired. The purpose of this report is to establish the basis for extending the performance envelope beyond that unambiguously established in previous reports.

1.1 REFERENCES

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants, 1996
TP0402	Operability Test Procedure, Rev F
TS901-000-29	Post Qualification Testing Summary Report, Rev B
TS901-000-34	Seismic Retest In-House Testing Summary Report, Rev B
TS901-000-35	Seismic Testing Summary Report, Rev B
TS901-000-39	AI Response Time Regression Test Report, Rev A
TN901-000-07	Addendum for TS901-000-34 Rev B, Rev A
TN901-000-08	Addendum for TS901-000-35 Rev B, Rev A
RR901-000-37	ERD111 Performance Envelope, Rev C

1.2 ABBREVIATIONS AND ACRONYMS

AI	Analog Input
AIC	Analog Input with Compensation (analog processing algorithm)
ANO	Analog Output (analog processing algorithm)
AO	Analog Output
C-Link	Communication Link
DHA	Digital High Alarm (analog processing algorithm)
DO	Digital (Discrete) Output
g	acceleration of gravity
HAS	Historical Archiving System
HFC	HF Controls
HPAT	HFC Plant Automated Tester
ICL	Intercommunications Link
I/O	Input/Output
ms	millisecond
OBE	Operating Basis Earthquake
s	second
SOE	Sequence of Events
SSE	Safety Shutdown Earthquake
TSAP	Test Specimen Application

2.0 SEISMIC QUALIFICATION PROGRAM

HFC conducted seismic stress testing for the ERD111 Test Specimen at Wyle Laboratories during September 2004. A comprehensive pre test was conducted at the HFC facilities before the Test Specimen was shipped to Wyle and following reassembly on the seismic simulation table. The following test runs were completed successfully:

- OBE1 through OBE5 were run in sequence.
- SSE was run after OBE5 was completed.

In addition to these test runs, OBE1 was run twice because a procedural error invalidated the results for the first execution. The SSE was run twice because a power cable to the Test Specimen became disconnected during the first test run. After completion of the second SSE, a post test was run to verify that the Test Specimen remained operational.

2.1 DYNAMIC STRESS LIMITS

The seismic spectrum specified by EPRI TR-107330 required a peak acceleration of 9.5 g for the OBE and 14 g for the SSE. The peak acceleration actually obtained was 10 g for both the OBE and the SSE. This constitutes the upper limit for the level of seismic stress actually demonstrated. The following anomalies were reported by Wyle as a direct result of the seismic stress conditions:

- Test Run 4 (OBE1 1st run) – (1) Two accelerometers came off the Test Specimen. (2) HFC personnel discovered that the voltage and frequency of the power feed to the equipment was incorrect.

- Test Run 5 (OBE1 2nd run) – Two accelerometers came off the equipment.

- Test Run 6 (OBE2) – Power supply modules partially ejected. A locking bar was mounted to hold the power supplies in place.

- Test Run 10 (SSE 1st run) Power supply cable to the main equipment rack became disconnected causing a partial loss of power. Chatter box channels 1, 2, 3, 4, and 7 indicated loss of power.

For test runs 4 and 10, the fault was corrected, and the test run was executed a second time. Following test run 6, a locking bar was mounted across the front of the power supply rack to prevent the power supply modules from being ejected during subsequent test runs.

2.2 ANALOG ACCURACY

2.2.1 4- to 20-MA AI Channel Accuracy

Two different waveforms were used to demonstrate accuracy and linearity: a 5-step (10%, 30%, 50%, 70% and 90%) waveform and a 10%-to 90% square wave signal. Both

waveforms were run before and during the seismic test runs. Averaged results for both waveforms are tabulated below.

Table 1. Five-Step Algorithm for AI Channel

Step Level	Averaged Percent Deviation				
	10%	30%	50%	70%	90%
Pre Test	-0.024	-0.007	-0.019	0.039	0.056
OBE3	0.036	0.053	0.041	0.089	0.066
OBE4	-0.024	0.003	-0.019	0.039	0.056
OBE5	0.046	0.293	0.301	0.039	0.056
SSE	0.036	0.303	0.291	0.039	0.076
Post Test	-0.014	0.013	-0.009	0.049	0.066
Reference: TS901-000-35 Tables A.2-1 through A.2-8					

Table 2. 10%/90% Algorithm for AI Channel

Step Level	Averaged Percent Deviation							
	Pre Test	OBE1	OBE2	OBE3	OBE4	OBE5	SSE	Post Test
10%	+0.0055	-0.039	-0.054	-0.036	-0.037	-0.029	-0.032	-0.049
90%	-0.075	-0.179	-0.134	-0.101	-0.106	-0.111	-0.108	-0.115
Reference: TS901-000-35 Tables 02-4, 012-4, 02-6, 02-8, 02-10, 02-12, 02-14, and 0-16								

The EPRI standard for accuracy and linearity of current-based AI channels is ±0.35%. The results of Table 1 indicate that the AI channels under test met the EPRI requirement for accuracy and linearity during all phases of the test except for OBE1 and OBE2, for which no data was preserved. However, Table 2 supplements the content of Table 1 to indicate that this requirement was met during all test runs.

2.2.2 4- to 20-MA AO Channel Accuracy

The same two waveforms were used to test AO channels during the seismic test runs. Averaged results for both waveforms are tabulated below. Data for the accuracy test is available for every seismic test run; data for the BOE test is available for every test run except OBE1.

Table 3. Five-Step Algorithm for AO Channel

Step Level	Averaged Percent Deviation				
	10%	30%	50%	70%	90%
Pre Test	-0.026	-0.017	-0.022	-0.011	-0.016
OBE1	-0.056	-0.057	-0.082	-0.061	-0.076
OBE2	-0.026	-0.057	-0.082	-0.061	-0.036
OBE3	-0.036	-0.027	-0.032	-0.011	0.014
OBE4	-0.036	-0.027	-0.042	-0.011	-0.026
OBE5	+0.004	+0.013	-0.002	-0.001	+0.004
SSE	-0.006	+0.003	-0.022	-0.011	-0.016
Post Test	-0.026	-0.037	-0.062	-0.021	-0.046
Reference: TS901-000-35 Tables A.3-1 through A.3-8					

Table 4. 10%/90% Algorithm for AO Channel

Step Level	Averaged Percent Deviation							
	Pre Test	OBE1	OBE2	OBE3	OBE4	OBE5	SSE	Post Test
10%	-0.069	-0.067	-0.067	-0.062	-0.107	-0.066	-0.064	-0.069
90%	-0.157	-0.161	-0.154	-0.139	-0.152	-0.153	-0.151	-0.136
Reference: TS901-000-35 Tables 02-5, 02-7, 02-9, 02-11, 02-13, 02-15, and 02-17								
* NOTE: Data listed was logged for the Single Loop Controller that was tested at the same time and included the same type of analog I/O module.								

Table 3 indicated that the AO accuracy remained within ±0.1% before during and after the seismic test runs. Data from Table 4 indicates that the AO channels remained within the ±0.3% tolerance limit for performance under stress.

2.2.3 RTD AI Channel Accuracy

The test specimen included one eight-channel RTD module. The module was subjected to a five-step linearity test before the seismic test, but during and after the seismic test runs, three channels (CH1, CH2, and CH8) were configured with fixed resistors to simulate an input having a fixed value. The results from these tests are tabulated below.

Table 5. Manual Pre-test Results for RTD Module

Simulated Input	Averaged Accuracy Per Channel							
	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
70° C	0.011%	-0.007%	-0.012%	-0.012%	-0.002%	0.003%	-0.006%	-0.007%
210° C	0.014%	-0.013%	-0.010%	-0.010%	-0.001%	0.004%	-0.003%	-0.007%
350° C	0.003%	-0.013%	-0.015%	-0.013%	-0.005%	-0.002%	-0.007%	-0.016%
490° C	-0.006%	-0.119%	-0.017%	-0.015%	-0.003%	-0.011%	-0.008%	-0.013%
630° C	-0.010%	-0.005%	-0.019%	-0.011%	0.003%	-0.008%	-0.006%	-0.017%
Average	**±0.009%**	**±0.032%**	**±0.015%**	**±0.012%**	**±0.003%**	**±0.006%**	**±0.006%**	**±0.012%**
Averaged accuracy for all channels over calibrated range: **±0.012% = ±0.08° C**								
Reference TS901-000-34 Table A.4-2. NOTE: The test report lists values for channels 1, 2, and 8 only, but values were recorded for all eight channels during the test. The averaged accuracy values were recalculated from the original test data.								

Table 6. Historical Archive Data for RTD Channels

Test Run	Averaged Deviation Per Channel			Average Deviation
	CH1	CH2	CH3	
Pre Test	-2.07° C	-0.76° C	-2.34° C	-1.72° C
OBE1	-2.07° C	-0.9° C	-2.47° C	-1.81° C
OBE2	-2.04° C	-0.77° C	-2.29° C	-1.7° C
OBE3	-2.05° C	-0.77° C	-2.32° C	-1.71° C
OBE4	-2.06° C	-0.78° C	-2.33° C	-1.72° C
OBE5	-2.06° C	-0.77° C	-2.33° C	-1.72° C
SSE	-2.07° C	-0.76° C	-2.34° C	-1.72° C
Post Test	-2.07° C	-0.78° C	-2.36° C	-1.74° C
Max Deviation From Pre Test	0.03° C	0.14° C	0.13° C	0.09° C
Reference: TS901-000-35 Tables A.4-1 through A.4-8				

Accuracy/linearity limits for RTD modules are ±2° C or ±3.6° F. Averaged results for the manual accuracy test (Table 5) indicate accuracy/linearity of ±0.08° C for all channels over the 700-degree range of the module. During the seismic test runs, three of the channels were configured with fixed resistors, and the resulting values were logged by a Historical Archiving System (HAS). The averaged value for all channels under test remained within the ±2° C accuracy limit for all seismic test runs, and no channel changed its indicated pre test value by more than ±0.14° C during the course of the seismic test runs. This indicates that the processing characteristics and reliability of the RTD module remained uniform before, during, and after all seismic test runs. The obvious difference between the manual test results and those during the seismic test were the result of contact resistances at the terminal board where the simulation resisters were installed. Because the contact resistance of a terminal may change by a few tenths of an ohm each time a wire is connected or disconnected, HFC has typically calibrated RTD modules in place following installation.

2.2.4 Pulse AI Channel Accuracy

The Test Specimen was equipped with two pulse card modules. Each module module provided both rate and accumulate modes of operation. When configured in rate mode, the module can produce either an 8-bit or a 12-bit image. When operating in accumulate mode, the module produces a 24-bit image. Functional capabilities of the module are summarized below.

Table 7. General Performance Characteristics

Property	Rate Mode		Accumulate Mode
	8 Bit	12 Bit	
Minimum Input Pulse Amplitude with 50% Duty Cycle (vpp)	22.6	24.4	
Maximum Input Pulse Amplitude (vpp)	32.0 (limit of signal generator)		
Minimum Duty Cycle (%)	26	10	
Maximum Duty Cycle (%)	75	90	
Minimum Rate Input Frequency (Hz)	20	70	
Maximum Rate Input Frequency (kHz)	10	20	
Maximum Accumulate Count Value	N/A		16,777,215

Table 8. Pulse Channel Accumulate Mode Accuracy Data - Pre Test

Input Frequency		Accumulate Mode Performance						Deviation (%)	
		Prescaler Value = 1			Prescaler Value = 100				
Nominal	Measured	Start Count	Final Count	Calculated Rate (Hz)	Start Count	Final Count	Calculated Rate (Hz)	Prescaler Value = 1	Prescaler Value = 100
50	49.8022	9220087	9235042	49.85	6509062	6509212	50	0.000	0.001
5000	4985.7	9332517	10826339	4979.407	6527330	6542300	4990	0.031	0.022
10000	10002.8	11347180	14341274	9980.313	6542545	6572574	10010	0.112	0.034
15000	14978.8	14916292	2629977	14969.67	6572574	6449699	14966	0.046	0.065
19500	19459.1	3820481	9644603	19413.74	6449840	6508237	19466	0.227	0.033
Note: Starting value is greater than final value because counter rolled over.									
Reference: TS901-000-29 Rev B Table PQ.A.5-1									

Table 9. Pulse Channel Rate Mode Accuracy Data - Pre Test

Input Frequency		Rate Mode – 8-Bit Image			Rate Mode – 12-Bit Image		
Nominal	**Measured**	**Count Value**	**Indicated Frequency**	**Deviation**	**Count Value**	**Indicated Frequency**	**Deviation**
50	49.752	16 - 32	39.06 - 78.13	In Range	11	53.72	0.0199%
600	594.454	256	585.94	3.0851%	122	595.85	0.0077%
5000	4978.5	2048	4960.94	2.3943%	1021	4986.57	0.0464%
10000	10003	4095	9958.50	-0.0557%	2050	10012.21	0.0583%
15000	14977.3	N/A	N/A	N/A	3068	14984.13	0.0524%
19500	19450.3	N/A	N/A	N/A	3985	19462.76	0.0861%

Reference: TS901-000-34 Rev B Table A.5-3.
NOTE: The values for frequency were recalculated based on an accumulation interval of 3 minutes.

During the seismic tests, two channels were configured with a constant input signal of 997.6 Hz to provide a basis for evaluating performance. One channel was configured for rate mode operation, and the other was configured for accumulate mode with a prescaler Value of 100. The results for both channels are listed below.

Rate Mode Channel Averaged error of ±0.007% during all phases of the seismic test (Reference TS901-000-35 Rev B paragraph A.5.1)

Accumulate mode Channel Error values for each seismic run are tabulated below (Reference TS901-000-35 Rev B Table A.5-1)

Table 10. Accumulate Mode Performance During Seismic Test

Test	Test Time	Start Reading	Start Time	Period (second)	End Time	Expected Reading	Actual End Reading	% Error
Pre Test	9:59 AM	0.09	9/22/04 9:37:51	2251	9/22/04 10:15:22	0.103382	0.1	-0.0034%
OBE1	4:11 PM	0.21	9/22/04 15:47:44	2343	9/22/04 16:26:47	0.223929	0.22	-0.0039%
OBE2	8:16 AM	0.25	9/23/04 7:52:51	1682	9/23/04 8:20:53	0.259999	0.26	0.00
OBE3	9:13 AM	0.27	9/23/04 8:48:58	1684	9/23/04 9:17:02	0.280011	0.28	0.00
OBE4	9:38 AM	0.28	9/23/04 9:17:02	1684	9/23/04 9:45:06	0.290011	0.29	0.00
OBE5	9:54 AM	0.29	9/23/04 9:45:06	1683	9/23/04 10:13:09	0.300005	0.3	0.00
SSE	10:27 AM	0.3	9/23/04 10:13:09	1684	9/23/04 10:41:13	0.310011	0.31	0.00
Post Test	12:17 PM	0.24	9/23/04 12:05:22	1684	9/23/04 12:33:26	0.250011	0.25	0.00

Reference: TS901-000-25 Table A.5-1

Accuracy/linearity requirements for the pulse input module is 0.1% for its operating range before, during, and after the imposed stress conditions.

When configured to produce an 8-bit rate mode image, the module cannot achieve an accuracy of ±0.1% except at the upper limit of its operating range due to the limitation of the 8-bit image, and it toggles between two values at the lowest end of its range. When configured to produce a 12-bit image in rate mode, the module is uniformly within the required accuracy/linearity tolerance.

Two configurations of the accumulate mode were tested: one with the prescaler set to 1 and the other with the prescaler set to 100. The both configurations produced results within the 0.1% tolerance limit.

The constant input during the seismic test runs indicates that the dynamic excitation had no impact on pulse card performance.

2.3 RESPONSE TIME

2.3.1 Digital Response Time

The digital response time test produced two parameters to indicate digital response characteristics of the Test Specimen. One consisted of seven cascaded signals configured to produce an in-out-in-out pattern. This algorithm produced a direct measurement of the application cycle time. The second consisted of a simulated fault signal that triggered a trip output on each low-to-high transition. Both algorithms were run during pre test, post test, and the seismic test runs. The results of these tests are summarized below.

Table 11. Automated Digital Response Time Test Results

In-House Pretest								
SOE Record File	**Equation Cycle Time (ms)**						**Response Time (ms)**	
	4,DI,2			**4,DI,3**			**4,DI,8 – 4,DI,9**	
	MIN	AVE	MAX	MIN	AVE	MAX	MIN	MAX
S2390200	68.40	84.05	90.61	76.41	84.05	91.06	37.8	134.9
S2441200	82.67	88.51	91.44	82.56	88.64	91.26	54.5	161.1
S2441209	82.94	88.68	93.94	82.87	88.69	96.61	22.1	161.4
Pretest at Wyle								
SOE Record File	**Equation Cycle Time (ms)**						**Response Time (ms)**	
	4,DI,2			**4,DI,3**			**4,DI,8 – 4,DI,9**	
	MIN	AVE	MAX	MIN	AVE	MAX	MIN	MAX
S2661002	55.98	88.60	90.03	44.64	88.25	92.31	41.4	176.55
S2661038	56.45	88.38	92.33	86.46	88.78	92.26	52.1	179.1
During OBE1								
SOE Record File	**Equation Cycle Time (ms)**						**Response Time (ms)**	
	4,DI,2			**4,DI,3**			**4,DI,8 – 4,DI,9**	
	MIN	AVE	MAX	MIN	AVE	MAX	MIN	MAX
S2661451	86.46	88.75	90.46	86.55	88.74	90.54	52.9	173.2
S2661610								
During OBE2								
SOE Record File	**Equation Cycle Time (ms)**						**Response Time (ms)**	
	4,DI,2			**4,DI,3**			**4,DI,8 – 4,DI,9**	
	MIN	AVE	MAX	MIN	AVE	MAX	MIN	MAX
S2670819	86.61	88.78	92.13	86.55	88.76	90.46	48.6	174.5

Table 11. Automated Digital Response Time Test Results (Cont)

During OBE3								
SOE Record File	**Equation Cycle Time (ms)**						**Response Time (ms)**	
	4,DI,2			**4,DI,3**			**4,DI,8 – 4,DI,9**	
	MIN	AVE	MAX	MIN	AVE	MAX	MIN	MAX
S2670918								
During OBE4								
SOE Record File	**Equation Cycle Time (ms)**						**Response Time (ms)**	
	4,DI,2			**4,DI,3**			**4,DI,8 – 4,DI,9**	
	MIN	AVE	MAX	MIN	AVE	MAX	MIN	MAX
S2670938	76.179	88.57	93.33	82.14	88.70	93.23	54.6	171.6
During OBE5								
SOE Record File	**Equation Cycle Time (ms)**						**Response Time (ms)**	
	4,DI,2			**4,DI,3**			**4,DI,8 – 4,DI,9**	
	MIN	AVE	MAX	MIN	AVE	MAX	MIN	MAX
S2670954	56.82	88.51	91.16	56.73	88.51	91.40	53.4	176
During SSE								
SOE Record File	**Equation Cycle Time (ms)**						**Response Time (ms)**	
	4,DI,2			**4,DI,3**			**4,DI,8 – 4,DI,9**	
	MIN	AVE	MAX	MIN	AVE	MAX	MIN	MAX
S2671028	75.95	85.958	92.89	70.9	85.85	93.18	28.6	159.9
Post Test								
SOE Record File	**Equation Cycle Time (ms)**						**Response Time (ms)**	
	4,DI,2			**4,DI,3**			**4,DI,8 – 4,DI,9**	
	MIN	AVE	MAX	MIN	AVE	MAX	MIN	MAX
S2671220	85.036	88.741	91.329	85.65	88.742	91.186	45.6	171.7
S2671435	73.47	88.64	93.0	50.87	88.49	95.86	56.4	174.6
Reference: TN901-000-08 Rev A Table A.13-1								

As indicated by the table, SOE records **S2661610** and **S2670918** did not preserve any data for the digital response time test. OBE1 was actually executed twice. The first time, the power feed had not been reduced to stress levels, so the data from that first run of OBE1 (SOE record **S2661451**) was not previously reported. OBE3 did not have a second SOE report, but two of the signals from the digital response time algorithm were logged by the Wyle chatter box strip chart. Qualitatively, the strip chart indicates that the digital response time algorithm was running with no disruption throughout the test run and that the equation cycle time was between 87.1 and 90 ms. In addition, the Burst of Events test was logged during OBE3 (Table 13). Although the simulated trip signal was not recorded on the strip chart, the BOE data does provide an indication of digital response time. And these data are in the same range as the data produced by the digital response time test.

As indicated in TN901-000-06 paragraph 3.3, the base line response time values are as follows:

Equation cycle time	48.557 ms to 99.871 ms
Digital response time	53.1 ms to 173.2 ms

Corresponding limits from the above table are:

Equation cycle time	44.64 ms to 96.61 ms
Digital response time	22.1 ms to 179.1 ms

The discussion of the results in TN901-000-04 asserted that worst case response time for this particular controller and application should be less than 180 ms as long as the transfer through the application code is not blocked. All of the results logged in the above records are within that worst case limit, indicating that the seismic stress had no impact on performance of digital processing functions.

2.3.2 Analog Response Time Test

The test algorithm originally developed for testing the analog response time was developed based on requirements of EPRI TR-107330. The TSAP included a test algorithm (Figure 1) composed of two blocks and a simulated trip memory. One block received an input from an AI channel, and the output of that block controlled the input to a DHA (digital high alarm) block. The DHA block was configured with an alarm setpoint of 50% and a deadband of 0.01%. The HPAT application included an algorithm consisting of a free-running analog square wave that switched between 45% and 55% of span with a period of 20 seconds (10 seconds high, 10 seconds low). This signal provided the input to an ANO block to produce a 4- to 20-mA AO signal that controlled the input to the Test Specimen. The analog system response time was measured from the point where the AI signal crosses the 50% level to the DO response.

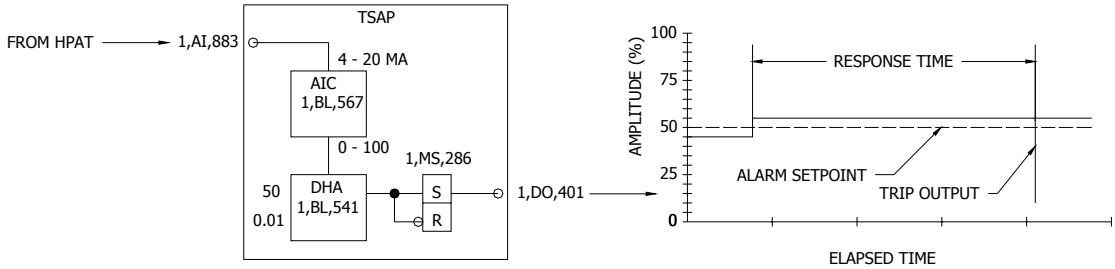

Figure 1 – TSAP Algorithm for Analog Response Testing

In order to automate data recovery, the DO signal was connected to an SOE logger, which was capable of logging the simulated trip signal with an accuracy of ±1 ms. The difference between the trip output signal and the trip trigger signal would then give accurate measurements for the system analog response time. Unfortunately, the analog trigger signal did not have sufficient amplitude to activate an SOE input, so the signal image was logged by an HAS. The two signals were logged, but the time stamps of the two loggers could not be synchronized with one another, so no definitive value for the analog response time could be established from the data archives.

2.3.2.1 Pretest Results

The complete set of Operability and Prudency tests were conducted in August of 2004 at the HFC facility prior to going to Wyle Labs. During that test, both the manual and the

automated analog response time test was run. The results of those tests were reported in TS901-000-34, Rev B and are summarized below.

Analog trigger signal period	20 sec
Trip output leading edge response time	4.145 ± 0.032 sec
Trip output trailing edge response time	3.303 ± 0.046 sec
Trip output True period (manual)	9.193 ± 0.117 sec
Trip output True period (SOE log)	9.19823 ± 0.059 sec
Trip output False period (SOE log)	10.80783 ± 0.064 sec

The attempt to associate data recovered from the HAS with that from the SOE proved unsuccessful. However, the records obtained from the SOE reports did provide two useful pieces of information:

- Because the trip output was triggered by the analog signal from the HPAT, the presence of trip signal in the SOE report indicates that the Test Specimen was receiving the input signal and executing the test algorithm.
- The presence of uniform ON/OFF periods of the trip signal implies that no disruption in operation was present.

2.3.2.2 Seismic Test Results

HFC conducted five OBE runs and one SSE run (up to 10 g acceleration) on the ERD111 Test Specimen in September of 2004. The analog response time algorithm was running during each test run. The results of the analog response time test were not discussed because the data were not adequate to establish a specific response time during seismic stress; a summary of the data for the trip signal is presented below.

Table 12. Averaged Trip Signal Periods

Report File	Test Run	Averaged TRUE Period	Averaged FALSE Period
S2441200	Pre Test	9.205 s	10.797 s
S2441209	Pre Test	9.198 s	10.808 s
S2661002	Pre Test	9.072 s	10.927 s
S2661038	Pre test	9.272 s	10.687 s
S2661451	OBE 1 (1st run)	9.271 s	10.735 s
S2670938	OBE 4	9.304 s	10.696 s
S2670954	OBE 5	9.283 s	10.723 s
S2671013	SSE (1st run)	9.322 s	10.69 s
S2671028	SSE	9.270 s	10.712 s
S2671435	Post Test	9.254 s	10.757 s

No data was logged during OBE1, OBE2, and OBE3 for the analog response time algorithm. Data in SOE report S2661451 was generated during the first execution of OBE1 before the power source was set to reduced voltage and frequency. Similarly, the data in S2671013 was taken from the first attempt at the SSE before the power cord pulled away from the Test Specimen. These data are being used to supplement the data from the regular test runs. The reason for the loss of data cannot now be determined for

certain; however, other data presented up to this point indicates that the application was running normally, and analog functions continued to operate. The uniformity of the data that has been preserved indicates that execution of the analog response time algorithm was not impacted by the seismic excitation.

2.3.2.3 Post Test Enhancement

HFC deemed the 4-sec analog response time obtained with the original ERD111 Test Specimen to be unacceptable. Consequently, additional tests were conducted after completion of the qualification tests to determine how to improve this result. TS901-000-39, AI Response Time Regression Test Report, Rev A, provides a detailed description of the tests conducted and the resulting improvement in response time. The primary investigation focused on the effect of two minor modifications to the original design:

- Modification of the software to reduce the processing algorithm from a 100-sample moving average to a 2-sample moving average. All other aspects of the software remain unchanged. Because program code is resident in PROM, this change will not affect the response of the assembly to seismic stress.

- Changing the input filter capacitors from two 10 μF capacitors to two 1 μF capacitors. This modification was intended to reduce the transfer time upstream from the Analog-to-Digital converter. Because the hardware change was limited to replacement of two capacitors for each AI channel, this modification also will not affect the overall response of the assembly to seismic stress.

This combination of hardware and software modifications reduced the analog response time from more than 4 seconds to 380 ms or less.

2.4 DISCRETE INPUT OPERABILITY

The purpose of the Discrete Input Operability test was to demonstrate the ability of the input channels to detect transitions in the field input signals. Results from the pre test execution of the Discrete Input Test are summarized below.

Average Set Voltage	15.13 V
Average Dropout Voltage	15.0 V
Maximum Voltage	50.19 V

This test was not run during or after the seismic test runs. However, the reliability and capability of input channels to detect and respond to changes to their input signal level is demonstrated by the digital BOE signals. All of these BOE signals originated in the HPAT external to the Test Specimen. The signals were hard-wired to DI channels of the Test Specimen, and then the resulting images were used to drive DO channels. The results of the BOE test runs are summarized below.

Table 13. BOE Transfer Delays

4,DI,28 (1,DO,648)	On Period (sec)	Off Period (sec)	Transfer Delay (ms)		
			Max	Ave	Min
HFC Pretest S21401316	1.007	0.992	136.6	78.563	27.4
Wyle Pretest S2661015	1.009	0.99	177.4	101.25	31.70
Wyle PretestS2661038	0.994	1.006	173.9	97.192	28.6
OBE1 S2661451 (1st run)	0.992	1.008	178.1	102.5	27.2
OBE1 S2661610	1.011	0.99	169.4	101.52	34.4
OBE2 S2670819	No BOE data collected during OBE2				
OBE3 S2670918	1.004	0.996	179.9	103.695	28.1
OBE4 S2670938	1.005	0.996	172.5	100.207	38.3
OBE5 S2670954	1.006	0.993	177.2	69.521	30.9
SSE S2671028	0.999	1.001	171.1	58.81	19.6
Post Test S2671435	1.01	0.99	169.4	99.977	40.6
4,DI,32 (1,DO,688)	**On Period (sec)**	**Off Period (sec)**	**Transfer Delay (ms)**		
			Max	**Ave**	**Min**
HFC Pretest S21401316	1.008	0.992	134.1	80.197	47.2
Wyle Pretest S2661015	1.007	0.99	**189.4**	101.687	43.2
Wyle PretestS2661038	1.02	0.981	172.9	102.649	53.0
OBE1 S2661451 (1st run)	1.1017	0.983	**190.4**	103.629	30.9
OBE1 S2661610	1.003	0.996	**180.9**	101.336	45.6
OBE2 S2670819	No BOE data collected during OBE2				
OBE3 S2670918	1.010	0.99	169.5	103.23	47.4
OBE4 S2670938	1.009	0.992	173.1	98.476	51.7
OBE5 S2670954	1.007	0.992	171.9	99.73	19.5
SSE S2671028	1.010	0.989	**180.6**	92.846	32.5
Post Test S2671435	1.004	0.996	173.8	104.658	37.8
4,DI,33 (1,DO,682)	**On Period (sec)**	**Off Period (sec)**	**Transfer Delay (ms)**		
			Max	**Ave**	**Min**
HFC Pretest S21401316	1.005	0.995	136.4	79.657	16.6
Wyle Pretest S2661015	1.008	0.992	178.6	100.454	25.2
Wyle PretestS2661038	0.996	1.004	177.5	102.59	47.5
OBE1 S2661451 (1st run)	0.997	1.003	175.7	102.943	29.5
OBE1 S2661610	1.004	0.995	170.3	100.815	**1.2**
OBE2 S2670819	No BOE data collected during OBE2				
OBE3 S2670918	1.005	0.996	174.4	100.404	24.9
OBE4 S2670938	0.99	1.010	173.1	97.487	20.5
OBE5 S2670954	1.001	0.998	173.5	103.271	30.5
SSE S2671028	1.002	0.997	178	89.87	19.6
Post Test S2671435	1.011	0.989	180	103.14	25.6
Reference: TN901-000-08 Paragraph 3.4					

The Burst of Events algorithm was run before, during, and after the seismic test runs, but no data was preserved for OBE2. Consequently, the test data was augmented by records from two additional pre tests and the first run of OBE1. All of the points monitored exhibited every transition of the signal source, and the averaged periods were all within

1.0±0.1 sec. There were four instances in which the maximum response time exceeded the theoretical maximum of 180 ms, and all of these instances occurred during the second run of OBE1.

2.5 DISCRETE OUTPUT OPERABILITY

The purpose of the discrete output operability test was to demonstrate that each type of output channel was capable of operating within specified voltages and currents under stress conditions. The test specimen included three different types of output channel:

- Mechanical relay output channels
- 120 vac output channels (solid state switch)
- 125 vdc output channels (solid state switch)

The discrete output test for these channels was conducted manually during the pre test executed at HFC but not as part of the tests conducted at Wyle.

2.5.1 Relay Channels

HFC-DO8 modules include a separate miniature ice cube relays on the board to control each channel. The circuit arrangement permits configuration for both normally closed and normally open channels. The results of the pretest execution of the DO operability test are summarized below.

Contact resistance	0.6Ω to 0.74 Ω
Maximum current load	> 9.4 A; switching under maximum load verified

The operability test for the relay output channels was not executed during the seismic test, but the digital response time, digital BOE, and timer tests all employed relay output channels, and these tests were running during the seismic test runs. In each case, those DO channels that were logged by the SOE were connected to a DI channel, and 48 vdc was used as the excitation voltage for these channels. The following characteristics were demonstrated by these tests:

No instance of contact bounce lasting longer that 1 ms was recorded by either the SOE or the chatter box strip chart during the seismic test runs.

All transitions of the digital response time, BOE, and timer tests were detected during the seismic test runs.

Applied excitation voltage	48 vdc
Peak switching current during test	10.9 mA
Steady state current during test	10.5 mA (approx)

2.5.2 120 VAC/125 VDC Output Channels

The HFC-DC33 module contained 12 DI channels and two 120 vac DO channels; the HFC-DC34 module contained 12 DI channels and two 125 VDC DO channels. The purpose of these modules is to have a single assembly provide the electrical interface needed by a field device having an AC or DC solenoid. The test setup consisted of circuit connections to either one- or two-coil solenoids configured with the HPAT. Manual execution of the operability test consisted of enabling/disabling the output channels and measuring the response of the external solenoid. The results of the manual test are as follows:

120 vac output channels	90 to 130 vac at 47 to 63 Hz range supported 2 A in-rush capacity supported 0.5 A steady state current supported Maximum on state voltage drop < 3vac at 0.5 A Supplies off state leakage current for coil continuity monitoring function without energizing the relay (Reference: TS901-000-34 Table A.10-1)
125 vdc output channels	90 to 140 vdc supported 2 A in-rush capacity supported 0.5 A steady state current supported 4 vdc maximum on state voltage drop at 0.5 A Supplies off state leakage current for coil continuity monitoring function without energizing relay (Reference: TS901-000-34 Table A.10-2)

The solenoids were not included as part of the Test Specimen. The purpose of the test was to demonstrate the capability of the onboard circuitry to supply the voltage/current levels necessary to control solenoid operation. The operability tests for these channels were not conducted during seismic test runs because the time required to perform the test exceeded the duration of any seismic test run. Two HFC-DC33 and two HFC-DC34 modules were configured as DO channels for the digital BOE test, which was run during each test run. The operation of the solenoids could be heard audibly during the test runs, but the high voltage output channels could not be logged directly, so there is no SOE record of their operation. Bases for acceptance of seismic qualification for these channels is as follows:

- Solid state switching ICs were used as the onboard control hardware for both the 120 VAC and the 125 VDC output channels. The internal circuitry of such devices is not subject to damage due to seismic stress. The only mechanism for circuit failure is failure of the solder joints securing the component to the surface of the circuit board.

- The ERD111 Test Specimen had already been subjected to seismic stress in April 2004, and the DO operability test had been accomplished as part of the post stress test and the pre test for the second seismic test. Both of these tests had indicated that the HFC-DC33 and HFC-DC34 modules had survived the seismic stress without failure.

- A second source of system failure during seismic stress is separation of cable/PCB connectors. For this system, all PCBs are secured to the chassis with thumb screws to prevent them from backing out of the edge connectors on the backplane. Similarly, the I/O cables each include a pair of jack screws to secure the connector body to its plug. There was no instance of any I/O cable becoming disconnected or loosened during the seismic test.

These considerations provide reasonable confidence that the high voltage output channels will remain operational as long as the high voltage source is available and the controller itself is running.

2.6 COMMUNICATION OPERABILITY

Two serial communication links were part of the ERD111 Test Specimen: the C-Link and the ICL. Because the communication links are not accessible during stress testing, the Communication Operability test was limited to logging the status of error counters before and after application of stress tests.

2.6.1 C-Link

Each controller includes two error counters – one for each channel controlled by the module. If the controller is operating normally, its error counters indicate the presence of any errors it detects on the link. If a remote on the C-Link exhibits failure on one or both of its channels, the error count data from other remotes on the link identify both the remote that is failing and the number of errors on the link. There were no C-Link communication errors reported during Pre Tests. During OBE tests and SSE test, only remote 4 showed errors. Remote 4 was connected to C-Link only while the SOE data was being retrieved. This indicates that operation of the C-Link was not impacted by the seismic stress conditions.

2.6.2 ICL

The ICL consists of redundant traces on the backplane of each equipment rack. When more than one equipment rack is present, physical cables link expansion racks to the controller rack in a daisy chain configuration. The ERD111 Test Specimen had four racks. The first three were connected with wire cables, and the fourth was connected with fiber-optic cables. The ICL Communication Operability test was run at the beginning and end of the seismic test runs, but much of the data for this test taken during September 2004 was lost.. Data from the first execution of the seismic test during April 2004 has been preserved. This data is presented in Tables 14 through 17 below.

Table 14. ICL Communication Operability Test Results During Pre Test

Station	Card Type	Start Count	End Count	Change	Start Time	Stop Time	Duration	Comments
0	KPD16	0	0	0	4/2/2004 9:32	4/2/2004 9:40	0:08:35	
1	KPD16	0	0	0	4/2/2004 9:32	4/2/2004 9:40	0:08:35	
3	KPD16	0	0	0	4/2/2004 9:32	4/2/2004 9:40	0:08:35	
5	KDI16	0	0	0	4/2/2004 9:32	4/2/2004 9:40	0:08:35	
6	KDO8	0	0	0	4/2/2004 9:32	4/2/2004 9:40	0:08:35	
7	KDO8	0	0	0	4/2/2004 9:32	4/2/2004 9:40	0:08:35	
9	PCC03	362C	690F	13027	4/2/2004 9:32	4/2/2004 9:40	0:08:35	PCC06
9	PCC03	362C	690F	13027	4/2/2004 9:32	4/2/2004 9:40	0:08:35	PCC06
10	PCC06	3813	6E20	13837	4/2/2004 9:32	4/2/2004 9:41	0:09:05	PCC06
10	PCC06	3813	6E20	13837	4/2/2004 9:32	4/2/2004 9:41	0:09:05	PCC06
16	KDI16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:05	Rack 2
17	KPD16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:05	Rack 2
19	KDI16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:05	Rack 2
20	KPD16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:05	Rack 2
22	KDI16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:05	Rack 2
23	KDO8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:05	Rack 2
24	KDO8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	Rack 2
25	KDI16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	Rack 2
26	KPD16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	Rack 2
36	KDI16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	
37	KDI16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	
38	KDO8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	
39	KDO8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	
40	KDO8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	
48	KAIO	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:04	
49	KAO8	4	4	0	4/2/2004 9:32	4/2/2004 9:41	0:09:04	
50	KAIO	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:04	
51	KAIO	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:04	
52	KAI16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:04	
53	KAI16	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:04	
54	KAO8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:04	
56	KAI8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:04	
57	KAIO	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	
58	KAI8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	AI4K
59	KAI8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	AI4K
60	KAI8	0	0	0	4/2/2004 9:32	4/2/2004 9:41	0:09:06	

Table 15. ICL Communication Operability Test Results During OBE5

Station	Card Type	Start Count	End Count	Change	Start Time	Stop Time	Duration	Comments
0	KPD16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:23	0:18:45	
1	KPD16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:23	0:18:45	
3	KPD16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:23	0:18:45	
5	KDI16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:23	0:18:45	
6	KDO8	000B	000B	0	4/2/2004 16:05	4/2/2004 16:23	0:18:45	
7	KDO8	000B	000B	0	4/2/2004 16:05	4/2/2004 16:23	0:18:45	
9	PCC03	7F6C	EEFA	29558	4/2/2004 16:05	4/2/2004 16:23	0:18:45	PCC06
9	PCC03	7F6C	EEFA	29558	4/2/2004 16:05	4/2/2004 16:23	0:18:45	PCC06
10	PCC06	8154	EFC7	28275	4/2/2004 16:05	4/2/2004 16:24	0:18:34	PCC06
10	PCC06	8154	EFC7	28275	4/2/2004 16:05	4/2/2004 16:24	0:18:34	PCC06
16	KDI16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:34	Rack 2
17	KPD16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:34	Rack 2
19	KDI16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:34	Rack 2
20	KPD16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:34	Rack 2
22	KDI16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:34	Rack 2
23	KDO8	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:34	Rack 2
24	KDO8	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:35	Rack 2
25	KDI16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:35	Rack 2
26	KPD16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:35	Rack 2
36	KDI16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:35	
37	KDI16	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:35	
38	KDO8	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:35	
39	KDO8	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:35	
40	KDO8	000B	000B	0	4/2/2004 16:05	4/2/2004 16:24	0:18:35	
48	KAIO	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:38	
49	KAO8	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:38	
50	KAIO	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:38	
51	KAIO	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:38	
52	KAI16	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:38	
53	KAI16	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:38	
54	KAO8	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:38	
56	KAI8	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:38	
57	KAIO	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:41	
58	KAI8	0928	0928	0	4/2/2004 16:05	4/2/2004 16:24	0:18:41	AI4K
59	KAI8	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:41	AI4K
60	KAI8	0	0	0	4/2/2004 16:05	4/2/2004 16:24	0:18:41	

Table 16. ICL Communication Operability Test Results During SSE

Station	Card Type	Start Count	End Count	Change	Start Time	Stop Time	Duration	Comments
0	KPD16	000B	000B	0	4/2/2004 16:23	4/2/2004 16:40	0:16:13	
1	KPD16	000B	000B	0	4/2/2004 16:23	4/2/2004 16:40	0:16:13	
3	KPD16	000B	000B	0	4/2/2004 16:23	4/2/2004 16:40	0:16:13	
5	KDI16	000B	000B	0	4/2/2004 16:23	4/2/2004 16:40	0:16:13	
6	KDO8	000B	000B	0	4/2/2004 16:23	4/2/2004 16:40	0:16:13	
7	KDO8	000B	000B	0	4/2/2004 16:23	4/2/2004 16:40	0:16:13	
9	PCC03	EEFA	4F3F	-41891	4/2/2004 16:23	4/2/2004 16:40	0:16:13	PCC06
9	PCC03	EEFA	4F3F	-41891	4/2/2004 16:23	4/2/2004 16:40	0:16:13	PCC06
10	PCC06	EFC7	5084	-40771	4/2/2004 16:24	4/2/2004 16:40	0:16:17	PCC06
10	PCC06	EFC7	5084	-40771	4/2/2004 16:24	4/2/2004 16:40	0:16:17	PCC06
16	KDI16	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:17	Rack 2
17	KPD16	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:17	Rack 2
19	KDI16	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:17	Rack 2
20	KPD16	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:17	Rack 2
22	KDI16	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:17	Rack 2
23	KDO8	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:17	Rack 2
24	KDO8	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:16	Rack 2
25	KDI16	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:16	Rack 2
26	KPD16	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:16	Rack 2
36	KDI16	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:16	
37	KDI16	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:16	
38	KDO8	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:16	
39	KDO8	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:16	
40	KDO8	000B	000B	0	4/2/2004 16:24	4/2/2004 16:40	0:16:16	
48	KAIO	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:15	
49	KAO8	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:15	
50	KAIO	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:15	
51	KAIO	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:15	
52	KAI16	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:15	
53	KAI16	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:15	
54	KAO8	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:15	
56	KAI8	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:15	
57	KAIO	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:14	
58	KAI8	0928	0928	0	4/2/2004 16:24	4/2/2004 16:40	0:16:14	AI4K
59	KAI8	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:14	AI4K
60	KAI8	0	0	0	4/2/2004 16:24	4/2/2004 16:40	0:16:14	

Table 17. ICL Communication Operability Test Results During Post Test

Station	Card Type	Start Count	End Count	Change	Start Time	Stop Time	Duration	Comments
0	KPD16	001C	001C	0	4/3/2004 6:24	4/3/2004 6:30	0:05:24	
1	KPD16	0	0	0	4/3/2004 6:24	4/3/2004 6:30	0:05:24	
3	KPD16	001A	001A	0	4/3/2004 6:24	4/3/2004 6:30	0:05:24	
5	KDI16	0019	0019	0	4/3/2004 6:24	4/3/2004 6:30	0:05:24	
6	KDO8	0	0	0	4/3/2004 6:24	4/3/2004 6:30	0:05:24	
7	KDO8	000A	000A	0	4/3/2004 6:24	4/3/2004 6:30	0:05:24	
9	PCC03	0167	87B9	0	4/3/2004 6:24	4/3/2004 6:30	0:05:24	PCC06
9	PCC03	0167	87B9	0	4/3/2004 6:24	4/3/2004 6:30	0:05:24	PCC06
10	PCC06	6885	89CC	8519	4/3/2004 6:24	4/3/2004 6:30	0:05:36	PCC06
10	PCC06	6885	89CC	8519	4/3/2004 6:24	4/3/2004 6:30	0:05:36	PCC06
16	KDI16	0	0	0	4/3/2004 6:24	4/3/2004 6:30	0:05:36	Rack 2
17	KPD16	0018	0018	0	4/3/2004 6:24	4/3/2004 6:30	0:05:36	Rack 2
19	KDI16	0	0	0	4/3/2004 6:24	4/3/2004 6:30	0:05:36	Rack 2
20	KPD16	0	0	0	4/3/2004 6:24	4/3/2004 6:30	0:05:36	Rack 2
22	KDI16	0	0	0	4/3/2004 6:24	4/3/2004 6:30	0:05:36	Rack 2
23	KDO8	000E	000E	0	4/3/2004 6:24	4/3/2004 6:30	0:05:36	Rack 2
24	KDO8	000F	000F	0	4/3/2004 6:24	4/3/2004 6:30	0:05:35	Rack 2
25	KDI16	0017	0017	0	4/3/2004 6:24	4/3/2004 6:30	0:05:35	Rack 2
26	KPD16	0017	0017	0	4/3/2004 6:24	4/3/2004 6:30	0:05:35	Rack 2
36	KDI16	0017	0017	0	4/3/2004 6:24	4/3/2004 6:30	0:05:35	
37	KDI16	0013	0013	0	4/3/2004 6:24	4/3/2004 6:30	0:05:35	
38	KDO8	3	3	0	4/3/2004 6:24	4/3/2004 6:30	0:05:35	
39	KDO8	3	3	0	4/3/2004 6:24	4/3/2004 6:30	0:05:35	
40	KDO8	2	2	0	4/3/2004 6:24	4/3/2004 6:30	0:05:35	
48	KAIO	0	0	0	4/3/2004 6:25	4/3/2004 6:30	0:05:36	
49	KAO8	0	0	0	4/3/2004 6:25	4/3/2004 6:30	0:05:36	
50	KAIO	5	5	0	4/3/2004 6:25	4/3/2004 6:30	0:05:36	
51	KAIO	5	5	0	4/3/2004 6:25	4/3/2004 6:30	0:05:36	
52	KAI16	0018	0018	0	4/3/2004 6:25	4/3/2004 6:30	0:05:36	
53	KAI16	001E	001E	0	4/3/2004 6:25	4/3/2004 6:30	0:05:36	
54	KAO8	0	0	0	4/3/2004 6:25	4/3/2004 6:30	0:05:36	
56	KAI8	0	0	0	4/3/2004 6:25	4/3/2004 6:30	0:05:36	
57	KAIO	0	0	0	4/3/2004 6:25	4/3/2004 6:30	0:05:37	
58	KAI8	14A8	14A8	0	4/3/2004 6:25	4/3/2004 6:30	0:05:37	AI4K
59	KAI8	001A	001A	0	4/3/2004 6:25	4/3/2004 6:30	0:05:37	AI4K
60	KAI8	0019	0019	0	4/3/2004 6:25	4/3/2004 6:30	0:05:37	

The ICL error counters for all I/O modules configured for the controller were read 9 times:

- Twice during the pre test (Table 14)

- Before OBE1 and OBE2. The original intention was to read the ICL error counters before and after each seismic test runs to detect any error generated during the test. However, the Test Specimen experienced a partial or total loss of power during OBE1 and OBE2. Because the ICL status data is reset during initialization, the loss of power renders the data from these tests invalid.

- Before OBE5, before SSE, and after SSE (Tables 15 and 16)

- Twice during the post test (Table 17)

Note that only the HFC-PCC06 modules logged any ICL errors during the test intervals reported. These modules did not have operational software installed during the test and so never responded to any ICL polls. The fact that a negative error count is recorded in Table 17 indicates that the error counters rolled over during the test interval. Also note that the starting count values in Tables 14, 15, and 17 differ from one another. This change was caused by the execution of the power interruption test, which caused some portions of the system to lose power.

As previously mentioned, the Communication Operability test was executed during the second seismic run, but the complete test data has not been preserved. However, the alarm status logs have been preserved for September 22 and 23 of 2004. The timeline for the overall test was as follows:

- The pre test was executed from 9:59 to 11:26 on 9-22-04, with the loss of power and power interruption test being executed between 10:55 and 11:26.

- The first run of OBE1 occurred from 2:47 to 2:54 PM on 9-22, and the second run of OBE1 occurred from 4:11 to 4:14.

- OBE2 was run between 8:16 and 8:21 AM of 2-23-04.

- OBE3 was run between 9:14 and 9:18 AM.

- OBE4 was run between 9:36 and 9:41 AM.

- OBE5 was run between 9:51 and 9:56 AM.

- The first run of the SSE occurred between 10:09 and 10:11 AM. The second run of the SSE occurred from 10:24 to 10:30 AM.

- The post test was conducted during the period from approximately 10:30 AM on.

The alarm log contains both ICL Link Alarms and Station Alarms for the individual I/O modules configured on the link. The controller generate a Station Alarm whenever a module fails to respond to an ICL poll; it generate a link alarm for all other types of ICL faults. Table 19 presents a summary of when the link and station failures occurred relative to the tests that were being conducted.

Table 18. Alarms During Seismic Testing

Test Conducted		Time	Link Alarm	Station Alarm
9-22-2004				
Pre Test		9:59 to 11:26	8:39	8:39 (station 58)
	Loss of Power	10:55 to 11:03	11:01 – 11:18	
	Power Interrupteion	11:11 to 11:26	11:01 – 11:18	11:12 – 11:14 (most)
OBE1	First Run	14:47 to 14:54	14:50	13:46 (station 60) 14:50 (station 52) 15:25 (station 52)
	Second Run	16:11 to 16:14	16:17	16:00 (station 58) 16:01 (station 58) 16:01 (station 59) 16:04 (station 58) 16:17 (station 49)
9-23-2004				
OBE2		8:16 -8:21	8:05 8:21	4:58 – (station 60)* 8:21 (station 49) 8:58 (station 52)
OBE3		9:14 - 9:18	9:16	9:16 (station 49)
OBE4		9:36 - 9:41		
OBE5		9:51 - 9:56		
SSE	First Run	10:09 - 10:11	10:19	10:19 (station 49)
	Second Run	10:24 to 10:30		
Post Test		10:30 - 14:37	14:55 After 15:00	After 15:00 (all)
Note: Station 60 started generating station alarms at 4:58 and continued doing so throughout the remainder of the test.				

Comparing the test time line with the alarm status file reveals the following:

1. An alarm was generated for Station 58 (one of the AI4K modules) during initial setup prior to the start of the pre test, and then no other ICL alarm occurred until the loss of power test.

2. Power was cut off from 10:55:53 to 11:01:12. No alarms were received from the Test Specimen until power was restored.

3. During the power interruption test, Station Alarms were generated for 21 out of 35 I/O modules during the period from 11:12:06 to 11:14:35.

4. During the first run of OBE1, data was logged from 14:47:59 to 14:51:56. An alarm was generated for Station 52 at 14:50:35, and an alarm for an out of range analog value. Station 52 was the AI16I module that received the analog accuracy, analog BOE, and analog response time inputs from the HPAT. There is no data for AI

accuracy during this period, but there is data for the analog BOE input signal. Evidently the AI16I module was operating, but the AI accuracy input signal was not.

5. The Test Specimen was powered down from 15:53:15 to 16:00:09 while the power feed was configured to produce a stress level input. The Station Alarms were generated from 16:00 to 16:04 when power was restored.

6. An alarm for Station 49 (AO8J module) was generated after the second run of OBE1 was completed. Station 49 (AO8J) was an operating spare that was configured but received no AO image.

7. According to the SOE record, data was logged for OBE2 from 8:15:14 to 8:18:54. Alarms for Station 60 (thermocouple input module) started at 4:58 AM and continued doing so throughout the day. An alarm for Station 49 was generated an alarm at 9:16 after completion of OBE2.

8. Data was logged for OBE3 from 9:14:00 to 9:18:07. An alarm for Station 49 was generated an alarm at 9:16.

9. No alarms were generated during OBE4 and OBE5 except those for station 60.

10. SOE records were logged for the first run of the SSE from 10:09:04 to 10:11:37. During this period, there was a partial loss of power, but the remote continued to operate. Multiple alarms were generated for station 60 but no other.

11. SOE records were logged for the second run of the SSE from 10:24:59 to 10:27:43. During this period, station 60 continued to generate alarms, but all other stations were operating normally.

12. The post test was run from 10:30 on with the power fault tests being run after 14:46. Except for station 60, there were no station or link alarms except for Station 60 until the start of the power fault tests.

These data indicate that both the C-Link and the ICL remained operational during all of the seismic test runs. The only disruption in their operation was cause by loss of power between seismic test runs. Evidently the thermocouple module (Station 60) failed after the first day, but that module was removed from consideration for qualification.

2.7 TIMER OPERABILITY

The ERD111 system includes a timer function that can be configured to operate over extended periods of time. The Test Specimen included 1-second and 5-second timers to permit accumulation of a reasonable amount of data within the limited periods of the seismic test runs. Results for each phase of the test are summarized in Table 19.

Table 19. Automated Timer Test Results

S1671050	Interval	4,DI,11		4,DI,12	
		Ave Value	Ave. % Deviation	Ave Value	Ave. % Deviation
Post Qualification Test	On Period	1.0006	0.06%	5.0022	0.044%
	Off Period	0.9985	0.15%	0.9961	0.39%
	Total Period	1.9997	0.015%	5.9993	0.038%
S2661002	**Interval**	**4,DI,11**		**4,DI,12**	
		Ave Value	**Ave. % Deviation**	**Ave Value**	**Ave. % Deviation**
Pretest At Wyle	On Period	1.0008	0.08%	5.0054	0.108%
	Off Period	0.9991	0.09%	0.9957	0.43%
	Total Period	1.9998	0.01%	5.9997	0.005%
S2661451	**Interval**	**4,DI,11**		**4,DI,12**	
		Ave Value	**Ave. % Deviation**	**Ave Value**	**Ave. % Deviation**
During OBE1 (1st run)	On Period	1.0041	0.41%	5.0050	0.1%
	Off Period	0.9960	0.4%	0.9950	0.5%
	Total Period	2.0001	0.0045%	6.0000	0.0%
S2670819	**Interval**	**4,DI,11**		**4,DI,12**	
		Ave Value	**Ave. % Deviation**	**Ave Value**	**Ave. % Deviation**
During OBE2	On Period	1.0029	0.29%	5.0046	0.092%
	Off Period	0.9976	0.24%	0.9954	0.46%
	Total Period	2.001	0.05%	5.9988	0.02%
S2670838	**Interval**	**4,DI,11**		**4,DI,12**	
		Ave Value	**Ave. % Deviation**	**Ave Value**	**Ave. % Deviation**
During OBE4	On Period	1.0008	0.08%	4.9973	0.054%
	Off Period	0.9987	0.13%	0.9998	0.02%
	Total Period	2.0003	0.015%	6.0007	0.012%
S2670954	**Interval**	**4,DI,11**		**4,DI,12**	
		Ave Value	**Ave. % Deviation**	**Ave Value**	**Ave. % Deviation**
During OBE5	On Period	1.0011	0.11%	4.9926	0.148%
	Off Period	0.9983	0.27%	1.0059	0.59%
	Total Period	2.0000	0.0%	5.9999	0.0017%
S2671013	**Interval**	**4,DI,11**		**4,DI,12**	
		Ave Value	**Ave. % Deviation**	**Ave Value**	**Ave. % Deviation**
During SSE (1st run)	On Period	0.9981	0.19%	5.0121	0.245%
	Off Period	0.9960	0.39%	0.9915	0.85%
	Total Period	1.9954	0.28%	6.0036	0.06%

Table 19. Automated Timer Test Results (Cont)

S2671028	Interval	4,DI,11		4,DI,12	
		Ave Value	Ave. % Deviation	Ave Value	Ave. % Deviation
During SSE	On Period	0.9998	0.02%	4.9978	0.044%
	Off Period	01.0006	0.06%	1.0028	0.28%
	Total Period	2.0002	0.01%	6.0005	0.0083%
S2671220	**Interval**	**4,DI,11**		**4,DI,12**	
		Ave Value	**Ave. % Deviation**	**Ave Value**	**Ave. % Deviation**
Post Test	On Period	1.0003	0.03%	5.0012	0.024%
	Off Period	1.0004	0.04%	0.9979	0.21%
	Total Period	1.9993	0.015%	5.9991	0.015%
Reference: TN901-000-08 Rev A Table A.7-1					

The SOE reports for OBE1 and OBE3 did not include any data for the timer test. The data from the first run of OBE1 and the SSE have been added to the table to supplement the data from the other seismic runs. In all, the test algorithm included four different time intervals: 1 sec, 2 sec, 5 sec, and 6 sec. Averaged values for each interval over the entire seismic test are as follows:

1 sec period	0.9990 sec (0.1% deviation)
2 sec period	1.9995 sec (0.025% deviation)
5 sec period	5.002 sec (0.04% deviation)
10 sec period	6.0002 sec (0.0033% deviation)

Averaged timer results met the ±0.1% tolerance for overall accuracy, and the deviation during seismic stress was below 1% for all test runs.

2.8 FAILURE TO COMPLETE SCAN DETECTION

The failure to complete scan function was not tested during seismic testing. This test was configured and executed at a later date to demonstrate that the equipment was capable of detecting and alarming the fault. Plans are currently in progress to execute additional environmental and EMI/RFI testing to demonstrate reliability of this function. However, the testing that has already been accomplished demonstrates that functional operation of the Test Specimen was not adversely impacted by seismic stress. Because detection of the failure to complete a scan of the application program is strictly internal to the controller, it also will not be susceptible to seismic stress.

2.9 FAILOVER OPERABILITY

The failover Operability test was run satisfactorily as part of the pre test for the ERD111 Test Specimen, but it was not run during or after the seismic stress test runs. The purpose of this test is to establish operability of the failover hardware for redundant devices. The following redundant elements are included in the ERD111 Test Specimen:

- Redundant controllers
- Redundant ICL
- Redundant C-Link
- Redundant power supplies and power distribution.

Of these, only the redundant controllers support automatic failover. The following hardware components required to support this failover function:

- ICs and a mechanical relay on each controller PCB
- The HFC-DPM06 PCB installed between the two controllers
- Signal traces on the backplane of the controller rack.

None of these elements were ejected from their normal position or experienced any mechanical damage during the seismic test. Consequently, functional operation of these components would have been available during and after application of the seismic stress. In addition, the failover operability test was successfully conducted during the post test after the first seismic test, indicating that the seismic stress did not impact their functional capability.

2.10 SERIAL LINK FAILURE TESTS

The Prudency test defined by EPRI TR-107330 define a set of failure tests to be conducted on the serial communication links associated with the Test Specimen and specified that these tests be conducted during the SSE. The tests were conducted during the pre test at HFC but not during the actual seismic tests. The reason for this omission is two-fold:

- The tests required installation of a breakout cable and direct access to the Test Specimen.
- Execution of the test required more time than any seismic test run.

Test results as reported in TS901-000-34, Rev B are satisfactory. Seismic stress does not affect electrical characteristics of a cable unless the connector pulls away from its socket. The CAT5 C-Link cables include a snap lock to secure the connector shell to its plug, and the ICL connector includes jack screws. Consequently, seismic stress will not have material impact on the results already observed.

2.11 LOSS OF POWER TEST

The purpose of this test was to demonstrate that all I/O channels of the Test Specimen move to power off default states while power is removed and that normal operation resumes following restoration of power. This test was conducted explicitly during the pre and post test phases of the seismic test but not during any seismic test run. Both the pre test and post test executions of the loss of power test produced satisfactory results, as reported in TS901-000-35 Rev B.

2.11.1 Digital Point Response

As previously mentioned, the loss of power test was not intentionally executed during the seismic test runs, because doing so would have invalidated the data being produced by the other test algorithms. However, one of the power connectors became disconnected during the first attempt of the SSE resulting in a partial loss of power to the Test Specimen. The data from SOE report S2671013 had not previously been analyzed because it was considered to have been invalidated by this loss of power. The log contains data for the following digital points:

- 4,DI,10 – analog response time trip signal.
- 4,DI,2, 4,DI,3, 4,DI,8, 4,DI,9 – digital response time signals
- 4,DI,11, 4,DI,12 – timer test signals
- 4,DI,28, 4,DI,32, 4,DI,33, 4,DI,34, 4,DI,35 – digital BOE signals

In addition, the Wyle chatterbox recorded five signals that exhibited dynamic operation during the test runs. Traces 1 and 2 are cascaded signals from the digital response test, and traces 3, 4, and 7 are digital BOE signals. Four additional traces on the chart were connected to static points that were being monitored to detect contact chatter. The last trace was connected to an accelerometer to indicate when the seismic test was active.

Although the SOE logger and the strip chart time stamp were not synchronized, both exhibit an abrupt halt in the Test Specimen operation. The five dynamic signals on the strip chart all drop to inactive levels (logic 0) approximately 7 seconds into the test run, which continued for another 20 seconds. (The complete SSE lasted approximately 30 seconds from beginning to end, not counting the initial resonance sweep.) Similarly, the SOE record for this test indicates that 9 out of the 12 signals all dropped to logic 0 at 10:11 AM. The three signals that continued running (4,DI,8, 4,DI,34, and 4,DI,35) were all generated by the HPAT, which was not affected by the loss of power. This is the required response to a low power/loss of power condition.

2.11.2 Analog Point Response

The analog accuracy, analog BOE, and static analog points from this test are not accessible. As indicated by the examination of the alarm file for 9/23/2004, the Remote 1 did not halt operation or stop broadcasting data to the C-Link. If the excitation power was lost from a chassis, all of the digital points in that chassis would have been affected. However, the analog I/O modules do not use the 48-vdc excitation power, so they would not have been affected. Loss of logic power causes both AO and AI channels to become immediately inactive, as indicated by the pre and post test execution of the loss of power test. Seismic stress might cause loss of power, but it could not prevent the AO channels from dropping to power off levels once power has been removed.

2.12 POWER INTERRUPTION TEST

The Test Specimen was configured with redundant power supplies, but they were connected to the same power feed in accordance with EPRI TR-107330 paragraph 6.4.3. The power interruption test was run before and after, but not during, the seismic test runs.

The purpose of this test was to demonstrate the capability of the power supplies to maintain output voltage levels during a 40 ms interruption in the power feed. In virtually every instance, functional operation of the Test Specimen was disrupted during the 40 ms interval. Consequently, a 40 ms holdup time for the output power rails was not demonstrated for a configuration with redundant power supplies connected to a single power source.

The redundant power supplies were sized so that one set of power modules were sufficient for both normal and stress operating conditions. The normal configuration for HFC control systems includes redundant power supplies with separate power sources. This configuration ensures adequate power to ensure holdup of the power rail during an interruption of power on one of the two power sources.

2.13 POWER QUALITY TOLERANCE

The EPRI specification (paragraph 6.4.3) required execution of a power quality tolerance test after completion of the seismic test runs. For the ERD111 Test Specimen, this consisted of setting the power source to supply primary power at 90 vac and 57 Hz (EPRI specification Paragraph 4.6.1.1.A). The EPRI specification (paragraph 5.4) required that the power source be set to this same level for performance of the Prudency tests.

Due to an oversight, the power source was not set to a reduced voltage and frequency prior to the first execution of OBE1. This procedural error was detected immediately after completion of OBE1 and corrected at that time. OBE1 was run a second time, and all successive test runs were conducted with the power source set to reduced voltage and frequency. Then the power quality tolerance test was executed after completion of the second SSE. Results of that test are tabulated below.

Table 20. Post Seismic Power Quality Tolerance Test

Power Feed	Power Module A				Power Module B			
	24-vdc	Deviation (%)	48 vdc	Deviation (%)	24 vdc	Deviation (%)	48 vdc	Deviation (%)
120 vac 60 Hz	24.07	0.29	48.03	0.06	24.02	0.08	47.99	-0.02
90 vac 57 Hz	24.07	0.29	48.03	0.06	24.02	0.08	47.99	-0.02
90 vac 63 Hz	24.07	0.29	48.03	0.06	24.02	0.08	47.99	-0.02
< 60 vac	Drop out at 77-76 vac							
120 vac 60 Hz	24.07	0.29	48.03	0.06	24.01	0.04	47.99	-0.02
150 vac 57 Hz	24.07	0.29	48.03	0.06	24.01	0.04	47.99	-0.02
150 vac 63 Hz	24.07	0.29	48.03	0.06	24.02	0.08	47.99	-0.02
> 270 vac (276 vac)	24.07	0.29	48.04	0.08	24.02	0.08	47.99	-0.02
Reference: TS901-000-34 Rev B Tasble 010-1								

As indicated, all power supply outputs remained within stipulated tolerance limits during this test. In addition, the power source was set at its low limit throughout the seismic test, indicating that dynamic stress had no impact on proper performance of the power supplies and power distribution within the Test Specimen.

3.0 SEISMIC QUALIFICATION

The ERD111 Test Specimen successfully passed a seismic test consisting of 5 successive OBE test runs and one SSE with a maximum acceleration of 10 g. The equipment was operational before, during and after each test run with the exception that a locking bar had to be installed across the power supply rack to prevent the power supply modules from being ejected. The detailed seismic qualification envelope is as follows:

Analog Accuracy/Linearity

4- to 20 mA AI Modules	Deviation within ±0.1% over entire span Deviation during seismic stress < ±0.35%
4- to 20 mA AO Modules	Deviation within ±0.1% over entire span Deviation during seismic stress < ±0.3%
100Ω Platinum RTD AI	Calibration within ±0.1% over 700° C span Averaged deviation < 2° C from starting value during seismic stress
Pulse input AI	Rate mode range 50 Hz to 20 KHz for 12-bit image with ±0.1% accuracy over entire range Range from 50 Hz to 10 KHz for 8-bit image Percent accuracy for 8-bit image varies with frequency due to the limited image size Averaged deviation from starting value during seismic test is within ±0.1% for 12-bit image Accumulate mode range 50 Hz to 20 KHz For prescaler =1, accuracy is within ±0.2% For prescaler = 100, accuracy is within ±0.1% Averaged deviation from starting value during seismic stress is within ±0.1%

Response Time

Digital Processing	Nominal response time from input to output transition ranged from 22 to 180 ms for the Test Specimen Seismic excitation had no impact on performance.
4- to 20 mA Analog Channels	Nominal response to AI step to trip output for the Test Specimen at the time of testing was approximately 4.1 s. Seismic excitation had no impact on performance. Post test modification to software and the input filter Circuit reduced response time to less than 380 ms.

Discrete Input Operability

Set voltage	15.13 v
Dropout Voltage	15.0 v
Maximum Input	50.19 v
Seismic Response	Seismic acceleration has no impact on performance

Discrete Output Operability

Relay Output Channels	Contact resistance: < 0.74Ω Maximum current load applied: 9.4 A Switching under maximum load verified Contact bounce period < 1 ms Seismic acceleration has no impact on performance
120 vac output channels	90 to 130 vac at 47 to 63 Hz 2 A in-rush capacity supported 0.5 A steady-state current supported Maximum on state voltage drop < 3vac at 0.5 A Supplies off state leakage current for coil continuity monitoring function without energizing the relay Seismic stress did not impact onboard DO circuitry
125 vdc output channels	90 to 140 vdc 2 A in-rush capacity supported 0.5 A steady-state current supported 4 vdc maximum on state voltage drop at 0.5 A Supplies off state leakage current for coil continuity monitoring function without energizing relay Seismic stress did not impact onboard DO circuitry

Communication Operability

C-Link	TC/IP communication link for transmitting system status to external portions of control system Link operation not impacted by seismic stress
ICL	Proprietary link to enable communication between controller and its configured I/O modules. Link operation not impacted by seismic stress

Application Functions

Timer Function	Configurable with a time base of 1 sec, 1 min, or 1 hour Timer preset range is from 0.1 to 5555.9 times the selected time base Averaged accuracy within ±0.1% Deviation under seismic stress within ±1%

Analog Processing	Application functions are constructed from a set of program algorithms operating within the controller. Seismic stress does not impact performance or accuracy.
Digital Processing	Application functions defined by Boolean-based equation statements. Seismic stress does not impact performance.
Failure to Complete Scan	Function not demonstrated during this test. It was configured, and the capability was demonstrated subsequently. This function is controlled by software within the controller and is not subject to interference by seismic stress.
Failover Operability	Function not specifically tested during the seismic test runs. The mechanical and electrical structures required to accomplish failover were tested after seismic testing, indicating that they were not impacted by the seismic stress.
Loss of Power Test	On loss of power, all relay DO points become de- energized. AO points drop to a 0 output level. System resumes normal operation on restoration of power. Seismic stress does not degrade functional characterisrtics.
Power Interruption Test	Power supplies used during the test did not provide a 40 ms holdup time during power interruption. 1) Normal system configuration includes redundant power supplies with separate power sources. 2) HFC has subsequently obtained a special power supply that does guarantee a 40 ms holdup time.
Power Quality Tolerance	Each power module maintained its output voltage level within tolerance for the following input voltage ranges: 90 vac at 57 to 63 Hz 150 vac at 57 to 63 Hz