

ENCLOSURE 4
(Non-Proprietary)

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WCAP-17226-NP R2)

“Assessment of Potential Interactions between the Core Exit Thermocouple Signals and the Self-Powered Detector Signals in the AP1000™ In-Core Instrumentation System”



Westinghouse Non-Proprietary Class 3

AP1000

Assessment of Potential Interactions between the Core Exit Thermocouple Signals and the Self-Powered Detector Signals in the AP1000TM In-core Instrumentation System

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SECTION 1 INTRODUCTION

The AP1000TM¹ In-core Instrumentation System (IIS) design contains hardware that places the Class 1E and non-Class 1E signal wires into very close proximity with each other. These two circuits are electrically separate, but are physically located in the same hardware components at the core end of the circuit. The Post-Accident Monitoring System (PAMS) Core Exit Thermocouple (CET) signals are Class 1E. The On-line Power Distribution Monitoring System (OPDMS) Self Powered Detector (SPD) signals are Non-Class 1E. Four of the CETs provide a signal to the Divers Actuation System (DAS). These four CETs are also Non-Class 1E. Each Incore Instrument Thimble Assembly (IITA), Quick Lock connector at the reactor vessel head penetration, and Mineral Insulated (MI) cable assembly contains both CET and SPD detectors and signal wires. (Note the MI cables discussed here only run from Reactor Vessel Head (RVH) penetration Quick Lock connector to the Refueling Disconnect Panel (RDP) on the Containment Building Refueling Deck.) The separation distance between the 1E and Non-1E portions of the circuits within the IITAs, Quick Lock connectors, and MI cables does not meet the prescribed separation distances between Safety and Non-Safety signals per the dictums in IEEE-384 (1981). Therefore, an analysis or testing of the potential interactions between the Safety and Non-Safety signals is required to demonstrate that credible faults in the Non-Safety signals will not cause a loss of the required safety functions. This report describes how the AP1000 IIS design satisfies the requirements of IEEE-384 (1981) such that any credible single fault in the Non-Class 1E SPD signals or Non-Class 1E CET signals will not reduce the number of valid Class 1E CET inputs to the PAMS below the required minimum number (i.e. – 3 operable CET per core quadrant).

¹ AP1000 is a trademark of the Westinghouse Electric Company LLC.

SECTION 2 ANALYSIS DESCRIPTION

The AP1000 IIS and the PAMS both use signals output from the IITA. The AP1000 IITA contain metal sheathed Class 1E grounded junction Type-K CET used by the PAMS and Non-Class 1E metal sheathed Vanadium SPD elements used by the OPDMS feature of the IIS. Inside the IITA the Class 1E CET elements and the SPD elements are electrically isolated from each other by placing the active portions of the elements inside individual steel outer sheaths that share a common ground. The IITA are connected to Class 1E design and post-accident environmentally qualified MI cables that are used to route the CET and SPD signals from the RVH to the RDP that also electrically isolate the SPD and CET signals using steel outer sheaths with a common ground. The presence of two commonly grounded metallic barriers within the IITA probe assembly and in the MI cables makes it incredible for an SPD emitter signal to short directly to the CET element signal leads. Figure 1 presents the layout of an AP1000 IITA.

The CET signals and SPD signals share common Class 1E design and post-accident environmentally qualified MI cable assemblies from the Quickloc flanges on the Reactor Vessel Head until a location just beyond the cable RDP is reached. [

]a,c Figure 2 provides a representation of the cable and cable sub-assembly components. The CET signals used by the PAMS are then split into two Divisions and routed to Class 1E Containment Penetrations via Class 1E design and post-accident environmentally qualified cables. The SPD signals are also split into two corresponding Trains at the CET Division split location and routed separately from the RDP area to the two SPS cabinets located inside the Containment Building via MI cables that also meet the 1E design and post-accident environmental qualification requirements. The analog SPD currents are digitized inside the SPS cabinets and conditioned for transmission out of the containment via fiber-optic cables. The 4 CET signals used by the DAS are routed to Non-Class 1E penetrations via long Class 1E design and post-accident environmentally qualified MI cables. The SPD signals are split between the SPS cabinets such that all of the SPD signals input to one cabinet are associated with one Division of PAMS CET signals. The IITA containing CET that provide inputs to the DAS are divided evenly between the two SPS cabinets. Figure 3 provides a schematic representation the CET and SPD signal routing.

Since the SPD signals are not used for any Reactor Protection System functions, and the SPD signals are not required for post-accident use, the original input power supply scheme for the SPS Cabinets had each cabinet being supplied with redundant sources of Non-Class 1E power. During the Preliminary SPS Cabinet Design Review, the issue of compliance with IEEE-384 (1981) requirements related to isolation of Class 1E and Non-Class 1E circuits within the IIS was discussed. Specific questions on the consequences of a potential unbounded power supply surge or over-voltage input to the SPS cabinets during LOCA or other harsh post-accident conditions on the operability of the PAMS CET signal inputs to the PAMS were raised.

Since the SPD signals have no direct Reactor Protection applications, the SPS cabinets are not specifically designed to operate in a post-accident environment. If it is assumed that none of the Non-Class 1E

qualified and non-post accident environment qualified over-voltage or surge protection contained in the SPS cabinet electronics operates as designed (due perhaps to harsh environmental conditions in containment in the post-accident environment), and an over-voltage or surge voltage from the electrical power source providing input to the SPS cabinets is able to propagate backwards to the SPD input signals through the SPS circuitry without attenuation or shorting to ground, it is considered credible that a sufficiently large over-voltage or a voltage surge at the SPS cabinet power supply inputs could cause at least a momentary loss of all Class 1E CET signals associated with the affected SPS cabinet via shorting between the SPD and CET wires in the backshell of the IITA or MI cable electrical connectors. If the over-voltage or transient surge condition were to occur on both SPS cabinets, then the result could be that all of the CET signals needed by the PAMS become inoperable. Figure 4 provides the IIS design configuration established to prevent these potentially adverse consequences. Details of the analysis performed to evaluate the design relative to the requirements of IEEE-384 (1981) are provided below.

AP1000 requires that low voltage systems be installed in a separate raceway system from medium voltage systems. As such, the maximum credible sustained over-voltage condition which can occur in a low voltage power or control circuit routed in this (these) low voltage raceway system(s) can be determined conservatively by considering nominal system operating voltages and maximum preferred system voltage range as defined in ANSI C84.1-2006. The system voltage at the low voltage system will remain balanced when the medium voltage system is supplied from normal or reserved source of power during the normal plant operation. During the abnormal plant operation when the normal and reserve sources of power are not available, the low voltage system will continue to function by receiving power from the standby diesel generators. The system voltage will also remain balanced even when the medium voltage continues to operate in the presence of a single line to ground fault indefinitely.

As the neutral of the load center transformers secondary windings are solidly (or effectively) grounded there will be no increase in the maximum credible sustained over-voltage of the low voltage system whether a ground fault is present at the medium voltage system or not. [

]a,c The high voltage taps of the load center transformer is set such that the maximum allowable voltage at the terminals of the loads and the secondary winding of the load center transformers is not exceeded.

[

]a,c

The Design Requirements for the MI Cable and IITA electrical connector hardware identified through Reference 1 require that manufacturing or proof testing be performed to demonstrate compliance with the []a,c requirement. This hardware testing requirement satisfies the requirements for testing or

analysis of Associated Circuit interactions with Class 1E circuits contained in IEEE-384 (1981) for over-voltage conditions.

In order to mitigate the possibility of a transient surge voltage condition in the SPS cabinet's input power supply disabling both Divisions of the CET signals used by the PAMS, the AP1000 IIS design outlined in Figure 4 supplies different Divisions of Safety Power to the IIS SPS cabinets with the power cables routed in separate shielded conduits to the SPS cabinets. Assigning each SPS cabinet and its corresponding PAMS Division to a different Class 1E power bus ensures that any credible fault on the SPS cabinets input power supplies will only occur on one SPS cabinet and can therefore only disable one Division of the CET signals used by PAMS. Since the PAMS is still operable with only one operable Division of CET signals, the potential for a loss of the minimum required PAMS functionality due to any single SPS cabinet input power issue is not credible. Figure 4 illustrates the power supply scheme to the SPS cabinets to be used that is consistent with the configuration of Associated Circuit item 2 in Figure 1 of IEEE 384 (1981).

Additionally, four of the 42 AP1000 IITA contain CET that produce signals which are routed to the DAS. The DAS is a Non-Class 1E system. These signals represent another potential path for surge or continuous over-voltage faults to enter the IIS from the DAS that could affect PAMS CET signal availability. The peak credible surge voltage generated by the DAS per USNRC Reg. Guide 1.180 Rev. 1 is the same as the IIS IITA and CET cable and electrical connector hardware voltage environmental and electromagnetic interference qualification limit requirements contained in Tier 2, Appendix Section 3D.4.1.2 of Revision 17 of the AP1000 Design Control Document (DCD). The DCD hardware requirements specifically require that the IIS IITA and associated cables be qualified to meet Reg. Guide 1.180 peak surge voltage pulse levels. The required compliance with Reg. Guide 1.180, Rev. 1 signal lead and power cable surge characteristics ensures that if there is a voltage surge from DAS that propagates down through the DAS CET signal leads to the associated SPD cables, there will be no credible, systematic shorting of DAS CET signals to the associated SPD signal leads. Therefore there is no credible mechanism to cause loss of the minimum required amount PAMS CET coverage.

Reference 1 identifies the analysis performed for the IIS for a nominal, un-faulted input power supply condition needed to address IEEE 384 (1981) Section 5.6 item 4 which states that Non-Class 1E circuits "are not required to be physically separated or electrically isolated from associated circuits provided that ... the Non-Class 1E circuits are analyzed to demonstrate that Class 1E circuits are not degraded below an acceptable level." The analysis that supports the Non-Class 1E Circuit analysis required by IEEE 384 (1981) for the IIS with a nominal input power supply condition called out in Reference 1 includes the IITA and MI cable and connector design requirement that the integrity of the IITA and MI cable and connectors are fully demonstrated at or above the maximum surge or over-voltage that could be generated in the IIS with nominal external power supply conditions and also addresses the following:

1. Ensure that no fault originating within the SPS cabinets can result in fault voltages at the reactor vessel head or refueling disconnect panel connectors greater than the maximum credible surge or continuous over-voltage values between the connector pins.

2. Ensure that inadvertent disconnection or failures of any IITA emitter wire or wires either at the SPS cabinet, or anywhere in the cabling between the IITA and the SPS cabinet will not cause voltage charge-up on the SPD emitter wire exceeding the maximum credible surge or continuous over-voltage values during normal plant operation, thus preventing a fault voltage from affecting the associated CET.

The analysis contained in Reference 1 concludes that there is no credible fault originating in the IIS SPS cabinets or cables with nominal input electrical power that could credibly cause the loss of the CET required for PAMS operability. Figure 4 provides a schematic representation of the 1E/Non-1E boundaries contained within the AP1000 IIS.

SECTION 3
ANALYSIS CONCLUSION

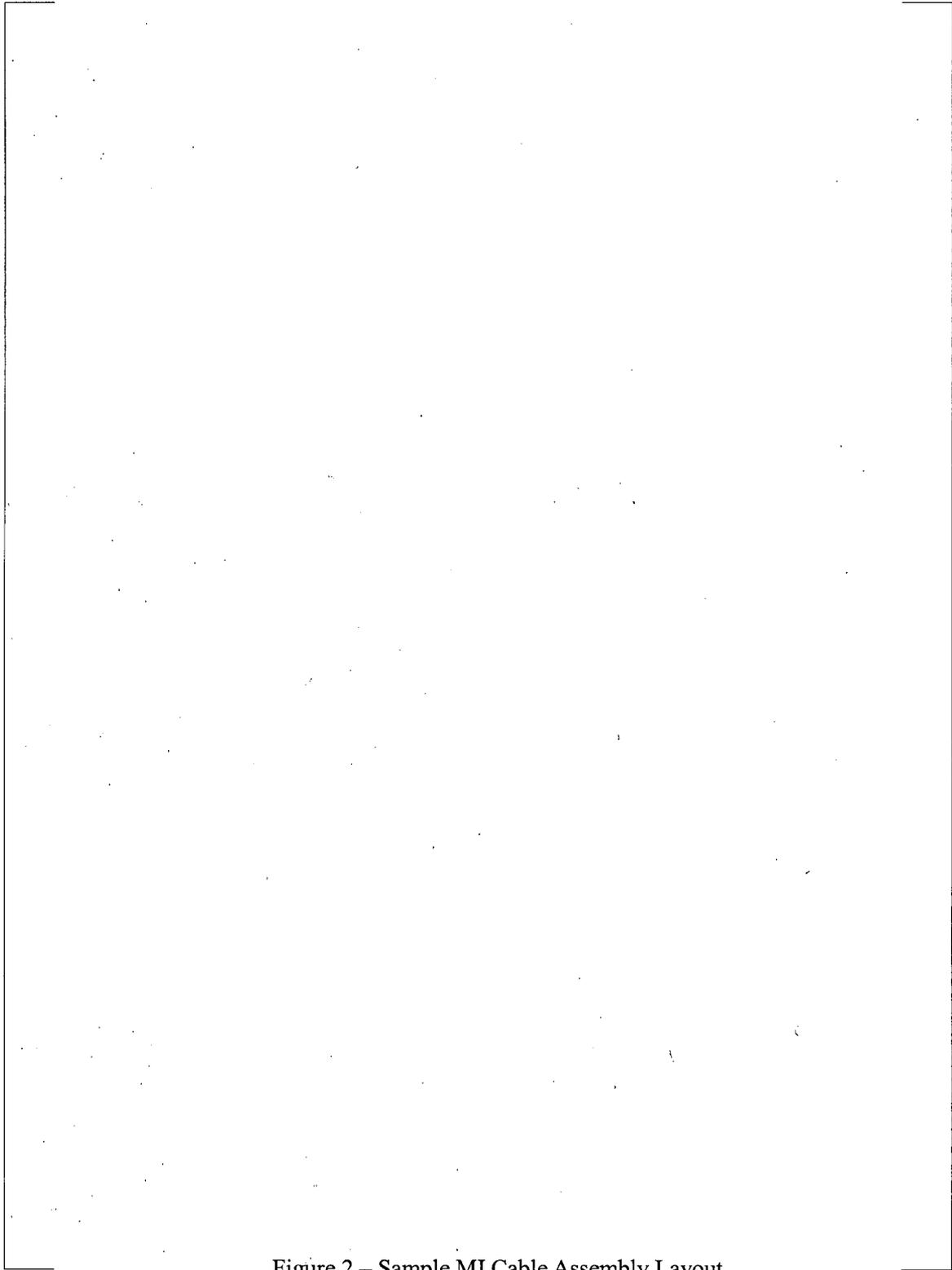
The use of different Divisions of Safety Power to power the IIS SPS cabinets, design compliance with the signal lead and power cable voltage surge withstand requirements in Reg. Guide 1.180 Rev. 1, and design compliance with the maximum credible continuous over-voltage and the DAS CET interaction potential analysis described above demonstrates that the Non-Class 1E Circuits in the IIS will not interfere with the safety functions of the Class 1E CET under any credible operating conditions.

**SECTION 4
REFERENCES**

1. APP-IIS-J7C-001 Rev. A, "AP1000 Incore Instrumentation System (IIS) Signal Processing System (SPS) Isolation Requirements," Westinghouse Electric Company LLC.

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Figure 1 – IITA Layout Drawing



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Figure 2 – Sample MI Cable Assembly Layout

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Figure 3 – AP1000 IIS Sensor Configuration Schematic



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Figure 4 – AP1000 IIS IITA and SPS Cabinet Interface Schematic