

MELTAC Platform FPGA V&V Final Report

Non Proprietary Version

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1. Outline

This is a Final Report of software V&V activity about the FPGAs of Safety System Digital Platform MELTAC NplusS.

This Software V&V activity was performed in accordance with MELTAC NplusS FPGA Software V&V SVVP(JEXU-1025-0002). This additional independent V&V activity was conducted for MELTAC NplusS FPGA, because it was previously determined that the original development of this FPGA did not follow all requirements applicable to US Nuclear Safety Systems, but this FPGA was not included in the original US Conformance Program (UCP).

2. Reference

Reference documents are shown in Table 2-1. For documents generated through V&V activity such as Task Report and Review Report, see "4.7 **Document List**".

Table 2-1 Reference

Document Number	Title
JEXU-1024-0002	Safety System Platform MELTAC NplusS FPGA Re-evaluation Project Plan
JEXU-1025-0002	Safety System Platform MELTAC NplusS FPGA Software V&V SVVP (Software V&V Plan)

3. Evaluation

Evaluation details of V&V activity are described in this chapter.

3.1. Evaluation Criteria and Evaluation Results

Evaluation criteria and evaluation results of V&V activity are shown in Table 3-1. See “3.2 Evaluation of V&V Activity” for more details.

Table 3-1 Evaluation Criteria and Evaluation Summaries

	Evaluation Criteria		Evaluation Summary	Result	
1	Was V&V performed according to SVVP for all required objects?	V&V organization	V&V was performed in proper organization according to SVVP. (Qualification Certificate shows V&V Team members had enough skills. In addition, V&V team is independent of software design organization, including personnel, management and budget.)	Good	—
		Scope of V&V	V&V was performed for all V&V object FPGA of the Module List attached to SVVP.	Good	—
		V&V report	All required documents were prepared as report documents. See Chapter 4.	Good	Table 4-2 to Table 4-6
2	Is there any problem (NG items) in the results of V&V activities? (For results of V&V reviews and tests.)		All V&V results are “Good”.	Good	Table 3-2
3	Is there any anomaly report still pending?		There is no pending.	Good	Table 4-2 to Table 4-6

V&V activities were performed according to SVVP as shown in Table 3-1 and were completed without pending item. In addition, V&V findings were corrected completely.

Therefore, all the activities planned in SVVP have completed. And all V&V results have turned out to be acceptable after evaluation.

3.2. Evaluation of V&V Activity

This section shows validity of V&V results.

Evaluation was performed for all V&V results including corrective actions to Anomaly Report and conclusions of Review Report.

For individual V&V object documents and source codes, they are described in Chapter 4. This section describes only a summary of V&V results and evaluations.

Table 3-2 V&V Result and Evaluation for Each Phase (1/3)

Table 3-2 V&V Result and Evaluation for Each Phase (2/3)

Table 3-2 V&V Result and Evaluation for Each Phase (3/3)

4. Appendix

4.1. V&V Implementation States and Results

This chapter describes the process of V&V activities. Also V&V results for every document and source code, and Document List are shown here.

Structure of this chapter is shown in Table 4-1.

Table 4-1 Structure of Chapter 4 (1/4)

Table 4-1 Structure of Chapter 4 (2/4)

Table 4-1 Structure of Chapter 4 (3/4)

Table 4-1 Structure of Chapter 4 (4/4)

4.2. System Specification V&V

Table 4-2 Result of System Specification V&V

4.3. Hardware Specification V&V

Table 4-3 Result of Hardware Specification V&V (1/4)

Table 4-3 Result of Hardware Specification V&V (2/4)

Table 4-3 Result of Hardware Specification V&V (3/4)

Table 4-3 Result of Hardware Specification V&V (4/4)

4.4. FPGA Specification V&V

Table 4-4 Result of FPGA Specification V&V (1/10)

Table 4-4 Result of FPGA Specification V&V (2/10)

Table 4-4 Result of FPGA Specification V&V (3/10)

Table 4-4 Result of FPGA Specification V&V (4/10)

Table 4-4 Result of FPGA Specification V&V (5/10)

Table 4-4 Result of FPGA Specification V&V (6/10)

Table 4-4 Result of FPGA Specification V&V (7/10)

Table 4-4 Result of FPGA Specification V&V (8/10)

Table 4-4 Result of FPGA Specification V&V (9/10)

Table 4-4 Result of FPGA Specification V&V (10/10)

Table 4-5 Result of Source Code V&V (1/12)

Table 4-5 Result of Source Code V&V (2/12)

Table 4-5 Result of Source Code V&V (3/12)

Table 4-5 Result of Source Code V&V (4/12)

Table 4-5 Result of Source Code V&V (5/12)

Table 4-5 Result of Source Code V&V (6/12)

Table 4-5 Result of Source Code V&V (7/12)

Table 4-5 Result of Source Code V&V (8/12)

Table 4-5 Result of Source Code V&V (9/12)

Table 4-5 Result of Source Code V&V (10/12)

Table 4-5 Result of Source Code V&V (11/12)

Table 4-5 Result of Source Code V&V (12/12)

4.6. FPGA Unit Test V&V

Table 4-6 Result of FPGA Unit Test V&V (1/12)

Table 4-6 Result of FPGA Unit Test V&V (3/12)

Table 4-6 Result of FPGA Unit Test V&V (4/12)

Table 4-6 Result of FPGA Unit Test V&V (5/12)

Table 4-6 Result of FPGA Unit Test V&V (6/12)

Table 4-6 Result of FPGA Unit Test V&V (7/12)

Table 4-6 Result of FPGA Unit Test V&V (8/12)

Table 4-6 Result of FPGA Unit Test V&V (9/12)

Table 4-6 Result of FPGA Unit Test V&V (10/12)

Table 4-6 Result of FPGA Unit Test V&V (11/12)

Table 4-6 Result of FPGA Unit Test V&V (12/12)

4.7. Document List

Table 4-7 Output Documents of the V&V Activities1 (1/12)

Table 4-7 Output Documents of the V&V Activities (2/12)

Table 4-7 Output Documents of the V&V Activities (3/12)

Table 4-7 Output Documents of the V&V Activities (4/12)

Table 4-7 Output Documents of the V&V Activities (5/12)

Table 4-7 Output Documents of the V&V Activities (6/12)

Table 4-7 Output Documents of the V&V Activities (7/12)

Table 4-7 Output Documents of the V&V Activities (8/12)

Table 4-7 Output Documents of the V&V Activities (9/12)

Table 4-7 Output Documents of the V&V Activities (10/12)

Table 4-7 Output Documents of the V&V Activities (11/12)

Table 4-7 Output Documents of the V&V Activities (12/12)