

**Attachment 2**

**NLI Report VVR-042181-1, Revision 8 Verification and Validation Report for Square  
D Masterpact Circuit Breaker (Including the Micrologic Trip Unit)**



**VERIFICATION AND VALIDATION REPORT  
FOR  
SQUARE D MASTERPACT CIRCUIT BREAKER  
(INCLUDING THE MICROLOGIC TRIP UNIT)**

NLI Report VVR-042181-1  
Revision 8  
June 2009

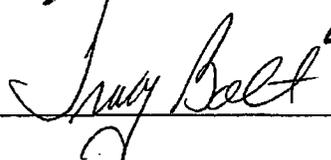
**APPROVAL**  
**VERIFICATION AND VALIDATION REPORT**  
**FOR**  
**SQUARE D MASTERPACT CIRCUIT BREAKER**  
**(INCLUDING THE MICROLOGIC TRIP UNIT)**

This report has been prepared in accordance with the NLI Quality Assurance Program.

The document was originally approved on 6/11/2009, as a NLI proprietary report. It is resigned as a non-proprietary version. There are no changes to the content of this document.

Prepared by:  date 8/16/09

Verified by:  date 8/17/09

Approved by:  date 8/17/09

## REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Date</u>
0	Original Issue	05/7/04
1	Added clarifications.	6/2/04
2	Incorporated neutral current transformer configuration and QR-042181-1-SUPP1.	10/13/05
3	Updated information and address client comments	9/12/2008
4	Correct typographical error	11/07/2008
5	Add firmware revisions (section 2.2)	2/6/2009
6	Add details on P and H series trip unit HC16 microcontroller and address client comments	3/26/2009
7	Add data on shunt trip, UV (undervoltage), and close coils.	4/22/2009
8	Address client comments.	6/11/2009

## TABLE OF CONTENTS

- 1.0 SUMMARY OF RESULTS
  - 1.1 Scope
  - 1.2 Limitations
  - 1.3 Project Specific Activities
  - 1.4 Codes and Standards
  - 1.5 Conclusion
  
- 2.0 EQUIPMENT IDENTIFICATION
  - 2.1 Safety Function
  - 2.2 Equipment Configuration
  - 2.3 Human Machine Interface
  - 2.4 Test Devices
  - 2.5 Cyber Security
  - 2.6 Traceability of the Test Specimen to the Production Units
  
- 3.0 SOFTWARE QUALITY ASSURANCE AND LIFECYCLE MANAGEMENT
  - 3.1 Software Quality Assurance Plan
  - 3.2 Software Lifecycle Management Plan
  
- 4.0 ABNORMAL CONDITIONS AND EVENTS
  - 4.1 Environmental Service Conditions
  - 4.2 Seismic Service Conditions
  - 4.3 Electromagnetic Interference/Radio Frequency Interference (EMI/RFI)
  - 4.4 Voltage Range
  - 4.5 Infant Mortality of Electronic Components
  - 4.6 Fault in Non Safety Plant System
  - 4.7 Hardware/Software Faults
  - 4.8 Loss of Power
  - 4.9 Overcurrent Condition
  
- 5.0 FAILURE MODES AND EQUIPMENT RELIABILITY
  - 5.1 Hardware Failure Modes and Effects Analysis
  - 5.2 Hardware Reliability
  - 5.3 Firmware Reliability
  
- 6.0 REQUIRED SYSTEM CHARACTERISTICS
  - 6.1 Verification of Required System Characteristics
  - 6.2 Separation Criteria
  - 6.3 Common Mode Failure Evaluation
  
- 7.0 IMPLEMENTATION OF REQUIRED CHARACTERISTICS
  - 7.1 Commercial Grade Audit of Schneider/Square D
  - 7.2 NLI Testing

- 7.2.1 Qualification Testing
- 7.2.2 Dedication/Factory Acceptance Testing (FAT)
- 7.2.3 Validation Testing
- 7.2.4 Failure Modes & Effects Testing
- 7.2.5 ANSI Design Testing
- 7.3 Operating History
- 7.4 Users Manuals
  
- 8.0 CONFIGURATION MANAGEMENT PLAN
  - 8.1 Schneider Firmware Configuration Control and Error Reporting
  - 8.2 NLI Configuration Control
  - 8.3 Plant Lifetime Configuration Control
  
- 9.0 QUALITY ASSURANCE
  
- 10.0 MEASUREMENT & TEST EQUIPMENT
  
- 11.0 REFERENCES
  
- ATTACHMENT A: Trip Unit Configurations and NLI Audit of Schneider/Square D
- ATTACHMENT B: NLI Validation Test Plan VVTP-042181-1 with test data
- ATTACHMENT C: Failure Modes & Effects Analysis
- ATTACHMENT D: NLI V&V Plan VVP-042181-1
- ATTACHMENT E: NLI Validation Test Plan VVTP-042181-2, rev. 2 with test data

## 1.0 SUMMARY OF RESULTS

### 1.1 Scope

This Verification & Validation (V&V) program was performed to demonstrate the acceptability of Square D Micrologic trip units to meet the requirements for the use of digital components in safety related applications in nuclear power plants. The Micrologic devices will be referred to as a "trip unit" or "trip device" in this report.

This report also addresses the shunt trip device, UV (undervoltage) trip device, and close coil in the Masterpact circuit breakers (referred to in the report as "coils"). These coils contain microcontrollers with firmware. There are no user configurable setpoints or field modifications.

Rev. 8

The circuit breakers are supplied with and without the Micrologic trip devices. For those breakers supplied with the Micrologic trip devices, all of this report is applicable. For those breakers supplied without the Micrologic trip devices, only the sections of this report that refer to "coils" are applicable.

Rev. 8

The Micrologic trip units are used in the Masterpact AC low voltage switchgear breakers (up to 600 vac nominal). The trip units are the digital devices that provide the protective function of the switchgear breaker and trip the breaker when an overcurrent condition is detected. The coils provide the close, shunt trip and UV functions on the breaker.

The typical application for the Masterpact breakers at nuclear plants in the United States is as part of a replacement breaker to replace existing low voltage breakers. A summary of this application is as follows:

- The Masterpact breaker with Micrologic trip unit is manufactured by Schneider/Square D. Square D is the company that supplies the Masterpact breakers with trip units in the United States. Schneider is the parent company located in France. A summary of the Schneider/Square D activities and locations is presented in section 7.1 of this report.
- The Masterpact breaker is converted by Square D Services in West Chester, Ohio to the specific replacement breaker configuration. This involves the design and manufacture of the electrical and mechanical interfaces to the existing switchgear. Square D Services is a long term NLI partner.
- The Masterpact circuit breakers are also supplied in new Square D switchgear.
- Square D Services performs the ANSI design testing required in accordance with ANSI C37.59 and other applicable ANSI standards.
- NLI performs the required dedication activities:
  - Production controls and Quality Control oversight of Square D activities.
  - Dedication of materials.
  - Dedication/Factory Acceptance Testing (FAT) of the replacement breakers.
- NLI performs the required qualification activities, including the following:
  - Seismic qualification.
  - EMI/RFI qualification.
  - V&V as documented in this report.
  - Mild or harsh environment qualification.

Safety related breakers are supplied to nuclear plants in accordance with the NLI Nuclear Quality Assurance Program which meets the requirements of 10CFR50 Appendix B, 10CFR21, and ASME NQA-1.

The trip units use Application Specific Integrated Circuit (ASIC) and microcontroller technologies. The coils use microcontroller technology. This report documents the results of the V&V of the software/hardware used in the trip devices and coils.

### **Trip Unit Configuration**

The specific range of equipment and parameters that are addressed by this V&V report are as follows:

- Standard, Ammeter, Power, and Harmonic models of the Micrologic trip device (3.0, 5.0, 3.0A, 5.0A, 6.0A, 5.0P, 6.0P, 5.0H, and 6.0H).
- All protective functions (L, S, I, G) including 4-wire neutral protection.
  - L: Long time delay.
  - S: Short time delay.
  - I: Instantaneous.
  - G: Ground fault protection.
- The safety function of the trip device is:
  - Maintain low voltage power circuits during normal conditions, including no spurious tripping.
  - Interrupt low voltage circuits in overcurrent conditions.
  - Modify the trip settings using the Incremental Fine Tuning (IFT) function on the H and P series trip units. This is performed using the touchpad on the front of the trip unit.
- The non-safety related features (communications, etc.) cannot interfere with the proper operation of the trip unit.
- All other functions of the trip device are considered non-safety related:
  - External communications, interlocking, etc. are considered to not be safety related functions. The history storage and recall functions are non-safety related.
  - This V&V program verified that these functions will not impact the safety related function of the trip unit.
  - The basis for this is as follows:
    - Based on NLI experience, most plants will not require these options. V&V of these options would be on a case by case basis, depending on plant specific requirements.
    - V&V of these features, especially the communication feature, would be significantly more complicated and would involve 50.59 issues that would be very plant specific.
    - The Schneider/Square D design documents identify that the communications features, metering, indicator lights, and history information files are outside the ASIC core protection design and are not required for protective functions.

The excerpt from the Masterpact catalog in Attachment A identifies features for each model of trip unit.

### **Coil Configuration**

The components addressed in the V&V report are the UV, shunt trip, and close coils for the Masterpact NT and NW circuit breakers:

- Shunt trip and close coil (nominal rating of 125vdc/120vac):
  - NW breaker: Square D p/n S33812.
  - NT breaker: Square D p/n S48493.
- Undervoltage trip (nominal rating of 125vdc/120vac):
  - NW breaker: Square D p/n S33821.
  - NT breaker: Square D p/n S48503.

### **Report Summary**

This V&V report provides the following detailed information:

- Section 1.2: Limitations of this V&V program.
- Section 1.3: Activities that will be performed by NLI for each individual project where the components are supplied.
- Section 1.4: Summary of the codes and standards that are met by this V&V program. The detailed evaluation of the applicable standards is contained in the V&V Plan in Attachment D.
- Section 1.5: Report conclusion.
- Section 2.0: Detailed summary of the equipment configuration.
- Section 3.0: Summary of the Software Quality Assurance Plan. The detailed plan is contained in the V&V Plan in Attachment D. Summary of the Software Lifecycle Management Plan.
- Section 4.0: Identification and evaluation of the Abnormal Conditions and Events (ACE's).
- Section 5.1: Summary of the Failure Modes and Effects Analysis.
- Section 5.2 and 5.3: Equipment reliability information.
- Table 6.1: Identification of the applicable critical characteristics, the acceptance criteria for each critical characteristic, the methods used to verify the critical characteristics, and the results.
- Section 6.2: Evaluation of separation criteria.
- Section 6.3: Evaluation of common mode failure.
- Section 7.1: Summary of the Schneider/Square D audits.
- Section 7.2: Summary of the NLI V&V activities.
- Section 7.3: Summary of the product operating history, including nuclear plant operating experience.
- Sections 8.1 and 8.2: Schneider/Square D and NLI configuration control activities.
- Section 8.3: Required plant configuration control activities.

Attachment A contains the NLI audit report of Schneider/Square D and supporting Schneider documents. The supporting documents are proprietary and are not included in the versions of this report that are released. These documents are available for review at the NLI facility.

## 1.2 Limitations

The following limitations are applicable to this V&V program;

- The following configurations were not addressed in this V&V program. The trip unit is not considered qualified in these configurations:
  - The trip unit is not qualified with any permanent communications features connected, such as Modbus communications.
  - The trip unit is not qualified with an external power supply connected.
- The xx.P and xx.H series trip units allow fine tuning of the trip curve using the Incremental Fine Tuning (IFT) function. Use of the IFT for fine tuning the trip current thresholds is evaluated in this report and is acceptable.
  - Use of the IFT function to fine tune other functions is not evaluated in this report and is not a qualified configuration.
- The xx.P and xx.H series trip unit have the capability for external communications to perform the Incremental Fine Tuning functions. Use of this function has not been evaluated and should not be used. The touchscreen on the front of the trip unit should be used to perform this function.
- The Square D Full Function Test Kit (FFTK) is used to test the trip unit and collect data from the trip unit. Per the Square D manual, the FFTK can be connected to the breaker with the breaker installed and operating. This configuration has not been evaluated by NLI. The breaker is considered inoperable with the test kit connected to the trip unit. See the additional information on the FFTK in section 2.4 of this report.
- The following functions are included on some of the Micrologic trip unit models. These functions are not included in the trip unit V&V (see details in references [20, 30]):
  - Advanced Protection
    - Alarms.
    - Minimum (Under) and Maximum (Over) Demand Current and Voltage Protection.
    - Current or Voltage Unbalance Protection.
    - Reverse Power Protection (rPmax).
    - Minimum (Under) and Maximum (Over) Frequency Protection.
    - Load Shedding.
    - Phase Rotation Protection.
  - M2C and M6C Programmable Contact Kits
  - Zone-selective Interlocking.
  - Metering.
  - Graphic Display Screen.
    - Non-safety related on the base and xx.A units.
    - Safety related on the xx.P and xx.H units.
  - Contact Wear Indicator.
  - Trip Unit History.

These features are considered non-safety related. The V&V activities have verified that these non-safety related functions will not impact the safety related trip function of the trip unit.

**Coils:** The following coil configurations are not addressed in this V&V program. The coils are not considered qualified in these configurations:

- The coils can be configured for external communications. This is not a qualified configuration.

Installation of this equipment must be evaluated on a plant specific basis in accordance with the plant procedures for 10CFR50.59 evaluations.

### 1.3 Project Specific Activities

This V&V report documents the activities that were performed for the V&V of the Micrologic trip units and coils for safety related applications. The following activities are performed for each specific project to verify the applicability of this report and dedicate and qualify the supplied trip units:

- Hardware and software configuration review to verify applicability of this report.
- NLI FAT/dedication testing on 100% of the supplied equipment. The FAT/dedication testing will include the following trip unit specific critical characteristics:
  - Record the trip unit configuration data (part number, serial number, code and revision).
  - Primary injection testing on the supplied circuit breaker.
    - Verify a sample of the trip curve points for each active function (L, S, I, G).
    - Verify proper operation of the trip unit with the CT's, ratings plug, and actuator.
  - Circuit breaker at degraded and over voltage conditions to verify proper operation of the trip unit across the primary voltage range (the trip unit is powered from the CT's on the primary bus).
  - Test the circuit breaker across the plant specified range of control voltages. This includes operation of all of the coils.
  - Note: The dedication plan for each replacement breaker type will include additional critical characteristics that verify the proper operation of the entire breaker assembly.
- Verify that the plant specific ACE's and ACE levels are enveloped by this report and supporting documentation or testing is performed per the client specific requirements.
  - Seismic qualification: Seismic qualification is plant specific and specific to the configuration of the replacement breaker.
  - EMI/RFI.
  - Environmental service conditions.
  - Voltage range.
  - Additional ACE's as defined by the plant.
- ANSI design testing: The ANSI design testing is a function of the trip unit and the replacement breaker. It is required for each replacement breaker design and is performed for each breaker design in accordance with IEEE C37.59-2002 [18].

In addition to this report, the following documents will be prepared for each plant/breaker configuration (including the trip unit and the coils), as applicable:

- Seismic qualification report.
- EMI/RFI qualification report.
- Design drawings.
- Instruction manual.
- ANSI design report.
- NLI Factory Acceptance Testing (FAT)/Dedication Test plan and report.

#### **1.4 Codes and Standards**

The firmware for the trip unit and coils was developed under the controls of the Schneider/Square D ISO 9001-2000 quality assurance program. The hardware and firmware are being dedicated for safety related applications by NLI under the controls of the NLI Nuclear Quality Assurance Program [19]. The applicable codes and standards are identified in the NLI V&V Plan [23] in Attachment D of this report. These codes and standards form the basis for the V&V activities and this V&V report.

Note: Most of the codes and standards referenced in the V&V Plan are for controls of the entire software lifecycle. Many of the codes and standards are very prescriptive concerning the required activities and documentation. Since this project is the dedication of existing commercial software, only certain requirements of these standards are applicable.

The V&V plan [23] documents the method used to meet the applicable requirements of the applicable codes and standards. The V&V plan is contained in Attachment D of this report.

Section 3.0 of this report contains a summary of the key software documents.

#### **1.5 Conclusion**

This V&V program was performed in accordance with the guidelines of EPRI-TR-102348 [4] and EPRI TR-106439 [5]. The dedication program was performed in accordance with the NLI Nuclear Quality Assurance Program and it includes all of the provisions of EPRI-TR-106439. The dedication program was based on commercial grade audits of the Schneider facility and testing by NLI. The activities that were performed are summarized below.

- The trip unit and coil requirements are documented in this report.
- The trip unit and coil design was performed by Schneider/Square D. The trip unit and coil design is documented in the Schneider/Square D documents that were reviewed by NLI during the audits.
- Detailed hardware Failure Modes and Effects Analyses (FMEA's) were performed by Schneider/Square D [21] and supplemental black box FMEA testing was performed by NLI [23].
- The ACE's were identified and addressed by testing or analysis (see section 4.0 of this report).

- The trip unit and coil critical characteristics (electrical, mechanical, firmware, process, dependability) were identified by NLI based on the function of the equipment. The trip unit and coil critical characteristics were verified based on audits of Schneider, testing at NLI, and evaluation of the operating history. The critical characteristics were found to
- meet the acceptance criteria.
- Table 6.1 identifies the critical characteristics of the trip unit and coil, including the digital system.
- Lifetime configuration control of the components is as specified in section 8.0 of this report.
- Nuclear plant operating experience was reviewed and evaluated.

These activities ensure that the acceptance features in Figure 3-2 of EPRI TR-106439 were followed for the firmware dedication process. There was an acceptable blend of the NLI dedication efforts, product operating experience, and the vendor efforts to demonstrate that the components are acceptable for this safety related application. NLI has provided an acceptable level of control over the development, installation, testing, and maintenance of the firmware under the control of the NLI Nuclear Quality Assurance Program. The firmware are within the bounds of the dedication and all critical characteristics have been successfully verified by audits, tests, and inspections. The operating history of the trip unit shows very good performance with no software problems in approximately 50,000 installed units. The operating history of the coils shows very good performance with no firmware problems in well over 100,000 installed units. There have been no revisions to the trip unit software since it was issued in 1998. There have been no revisions to the coil firmware since it was issued in 2002. The manufacturer, Schneider, has an excellent record for support and addressing past problems. Our review of the trip unit's and coils' overall architecture, hardware, and firmware design shows a high quality design without any weaknesses. This includes the failure analysis which was performed that shows that all failures are adequately addressed in the equipment design. All of these activities provide reasonable assurance that the trip unit and coils will perform their safety-related functions. The quality of the trip unit and coils, both hardware and firmware, is equivalent to equipment that is developed under the controls of a Nuclear Quality Assurance Program.

## 2.0 EQUIPMENT IDENTIFICATION

### 2.1 Safety Function

The safety functions of the trip devices are:

- Maintain low voltage power circuits during normal conditions, including no spurious tripping.
- Interrupt low voltage circuits in overcurrent and ground fault conditions.
- The non-safety related features (external communications, etc.) cannot interfere with the proper operation of the trip unit.
- Modify the trip settings using the Incremental Fine Tuning (IFT) function on the H and P series trip units. This is performed using the touchpad on the front of the trip unit.

Rev. 8

The communications, interlocking, historical data storage and other functions not associated with breaker tripping are considered to be non-safety related functions and are addressed as follows:

- The trip units are not qualified with any communications features operational or connected.
- The internal communication firmware and hardware are demonstrated to not impact the operation of the safety related function of circuit protection.

The safety functions of the coils are:

- UV: Allow the breaker to close during a normal voltage condition (coil energized). Trip the breaker in an undervoltage condition (coil de-energized, spring return). Not inadvertently trip the breaker.
- Shunt trip: Allow the breaker to close with no control voltage applied (coil d-energized). Trip the breaker with control voltage applied (coil energized). Not inadvertently trip the breaker.
- Close coil: Close the breaker with voltage applied (coil energized).

See the additional information is section 2.2.1 on the operation of the coils.

### 2.2 Equipment Configuration

The trip unit is available in a number of configurations, as follows:

- Standard, Ammeter, Power, and Harmonic models of the Micrologic trip device (3.0, 5.0, 3.0A, 5.0A, 6.0A, 5.0P, 6.0P, 5.0H, and 6.0H).
- All available functions (L, S, I, G).
- The equipment data sheets in the V&V Plan in Attachment D provide details on the equipment configurations.
- Incremental Fine Tuning (IFT) of the trip settings is part of the design of the x.xH and x.xP trip units.

The current revisions of the firmware are:

- ASIC: version 2.7.
- HC11 Microcontroller (used in all xx.A trip units): Version 1.027.
- HC16 Microcontroller (used in xx.P and xx.H trip units units): Plogic-2005.AF.

See additional details below.

### **2.2.1 Trip Unit and Coil Models**

#### **Trip Units**

This V&V program addresses the model 3.0, 5.0, 3.0A, 5.0A, 6.0A, 5.0P, 6.0P, 5.0H, and 6.0H Micrologic trip devices.

The part number designations are as follows:

- Trip unit functions:
  - Model 3.0: LI functions.
  - Model 5.0: Selective LSI functions.
  - Model 6.0: Selective LSIG functions.
- Advanced functions:
  - Suffix x.xA: Ammeter measurements.
  - Suffix x.xP: Power measurements.
  - Suffix x.xH: Harmonic metering.

All of the models use the same ASIC for the protective functions. Different microcontrollers are used in the different series trip units. The two microcontrollers are discussed in sections 2.2.2.15 and 2.2.2.16.

Incremental Fine Tuning (IFT) of the trip settings is only available on the x.xH and x.xP units.

#### **Coils**

The components addressed in the V&V report are the UV and shunt trips for the Masterpact NT and NW circuit breakers:

- Shunt trip and close coil (nominal rating of 125vdc/120vac):
  - NW breaker: Square D p/n S33812.
  - NT breaker: Square D p/n S48493.
- Undervoltage trip (nominal rating of 125vdc/120vac):
  - NW breaker: Square D p/n S33821.
  - NT breaker: Square D p/n S48503.

The identifier and current revision of the firmware is:

- Hardware part number: 51005451AA, revision B.
- Firmware revision: V15.

The configuration of the coils are as follows:

- The package, mounting, circuit board and configuration of the coils are all the same, except as evaluated below:

- NW vs. NT part numbers: The wiring and connectors are different to mate with the electrical components in the breakers.
- Operation of the shunt trip, close coil, and UV are the same, except as follows:
  - Shunt trip: The shunt trip is normally de-energized with the plunger retracted. The coil is energized for a short duration to extend the plunger. The plunger impacts the trip latch and trips the breaker. When the coil is de-energized, the spring returns the plunger to the retracted position.
  - Close coil (same part number as the shunt trip): The close coil is normally de-energized with the plunger retracted. The coil is energized for a short duration to extend the plunger. The plunger impacts the close latch and trips the breaker. When the coil is de-energized, the spring returns the plunger to the retracted position.
  - UV: With the coil de-energized, the plunger is extended and the breaker cannot be closed. The coil is energized to retract the plunger. This allows the breaker to be closed. When the voltage is lowered below the setpoint or removed, the coil is de-energized and the spring returns the plunger to the extended position. The extended plunger hits the trip latch and trips the breaker.

### **2.2.2 Equipment Configuration**

The equipment configuration is provided in the following sections:

- Circuit breaker: sections 2.2.2.1.
- Trip unit: sections 2.2.2.2 - 2.2.2.16.
- Coils: section 2.2.2.17.

Additional details are provided in the NLI audit report and Schneider/Square D documents in Attachment A.

#### **2.2.2.1 Breaker Configuration**

The overall configuration of the circuit breaker is as follows:

- The low voltage power circuit breaker is installed in the low voltage switchgear. Each circuit breaker is in an isolated cubicle.
- The trip unit is mounted on the circuit breaker. There is one trip unit per circuit breaker.
- Each circuit breaker contains 3 current transformers (CTs). The 3 CT's power the trip unit. There are no other power sources for the trip unit. Some circuit breakers may be supplied with an external neutral CT.
- Operation of the trip function is as follows;
  - During an overcurrent or ground fault event, the CT's send a signal (current) to the trip unit that is proportional to the primary current through the circuit breaker or neutral CT.
  - The trip unit compares the signal from the CT's to the settings. The settings are made in the field by mechanical switches on the front of the trip unit, except for the neutral protection setting. The neutral protection setting is set via the

- electronic menu (lcd).
  - Incremental fine tuning of the trip units can be made in the field using the touchpad on the front of the trip unit.
- If the current to the trip unit exceeds the setting for the required time delay, the trip unit sends a signal to the actuator.
- The actuator trips the breaker. The actuator will fire and trip the breaker each time it receives a signal. There is no signal processing by the actuator.
- The trip unit external interfaces are as follows:
  - Power and current signal from the CT's.
  - Output signal to the actuator.
  - There are no other input/output (I/O) signals.
- The operation of the coils is as follows:
  - All of the coils are installed in the breaker.
    - The unextended UV and shunt trip coil plungers are in close proximity (approximately ¼") to the trip latch. Extension of the coil plunger hits the trip latch and trips the breaker.
    - The unextended close coil plunger is in close proximity (approximately ¼") of the close latch. Application of control voltage extends the plunger, hitting the latch and closing the breaker.
  - UV coil: The coil is energized with control voltage to retract the plunger. This allows the breaker to be closed. When the control voltage is removed or reduced below the dropout voltage of the coil, the spring return extends the plunger. The plunger hits the trip latch and trips the breaker.
  - Shunt trip coil: The coil plunger is normally retraced and the breaker can be closed. Application of control voltage extends the plunger, hitting the trip latch and tripping the breaker.

#### 2.2.2.2 Trip Unit Performance Specifications

The performance characteristics of the trip devices are as follows:

- Accuracy (% of input):
  - Trip Unit Performance:
    - Long-time pickup ( $I_r$ ) + 1.05%, + 20%
    - Long-time delay ( $t_r$ ) +0% -20%
    - Short-time pickup ( $I_{sd}$ )  $\pm$  10%
    - Short-time delay ( $t_{sd}$ ) for 5.0A trip units, accuracy is per Square D Catalog 0613CT0001R4/08, page 24, Table 24. For all H trip units, accuracy is per Square D Catalog 48049-330-01, page 13, Table 3, and for all P trip units, accuracy is per Square D Catalog 48049-137-04, page 12, Table 3.(2.0A and 3.0A have no short time delay)
    - Instantaneous ( $I_i$ )  $\pm$  10%

This accuracy is for the entire trip system (trip device + CT's).

- Linearity (% of input): The device is linear  $\pm 0.001\%$  throughout the range. The air core CT is considered completely linear. The linearity deviation is due to the inherent characteristics of the A/D converters.
- Drift: Total drift over 10 years is  $<1\%$ . The drift is due to design characteristics of the CT, RC coupling effects of the CT and small changes in the ADC reference voltage. The drift characteristics are based upon accelerated life testing of Masterpact and Micrologic production units.
- Temperature affect: No known temperature affect on accuracy, linearity, or drift throughout the operating temperature range of  $-22^{\circ}\text{F}$  to  $140^{\circ}\text{F}$  have been identified.
- Response Time from input to output with change of state:
  - Digital: 544  $\mu\text{seconds}$  + user selected trip delay time + 20 milli-seconds.
  - Analog: 1  $\mu\text{second}$  + 20 milli-seconds.
  - Note: Change of state is defined to be the total time from current detection to when the breaker contacts transition from fully closed to contacts fully open.

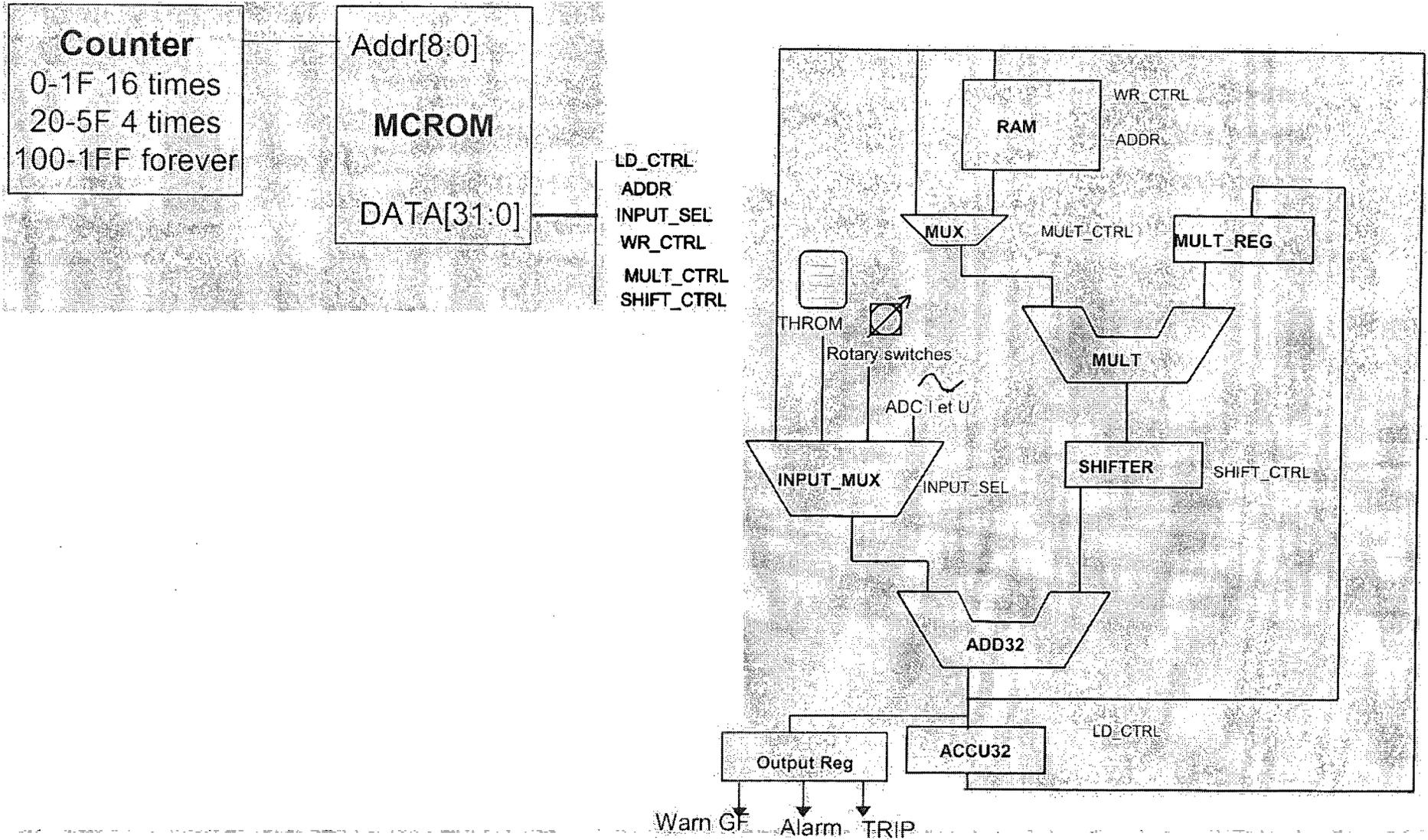
### 2.2.2.3 Trip Unit Architecture

The trip units consists of the following digital devices:

- ASIC: The ASIC performs the safety related trip functions.
- Microcontroller:
  - Base trip units (xx series) do not contain a microcontroller.
  - HC11 Microcontroller (used in all xx.A trip units): This microcontroller performs no safety related functions and is isolated from the ASIC. See additional details in section 2.2.2.15.
  - HC16 Microcontroller (used in xx.P and xx.H trip units): This microcontroller is not isolated from the ASIC and can be used to fine tune the trip settings. See additional details in section 2.2.2.16.

### 2.2.2.4 Trip Unit ASIC

The schematic of the ASIC portion of the trip unit is contained on the following page.



The Application Specific Integrated Circuit (ASIC) provides core protection functions using both digital and analog circuitry. Both the digital and analog circuitry are contained on the ASIC. These core ASIC functions are safety related.

Rev. 8

- The digital portion of the ASIC supports user selectable safety-related circuit breaker protection functions. The user selectable functions are made with the mechanical switches on the front of the trip unit. The hardware and firmware provides True RMS Current Sensing.
- The incremental fine tuning is implemented by the microcontroller in the x.xP and x.xH units. Details are contained in section 2.2.2.16.
- The analog portion of the ASIC provides over temperature thermal imaging protection and instantaneous high current protection. This provides redundant, safety related backup to the digital portion of the ASIC. These analog protection functions provide additional breaker/circuit protection and are not incorporated into the trip curve.
  - Thermal imaging: Thermal imaging is similar to the thermal memory of the thermal element in a thermal-magnetic molded case circuit breaker. The thermal imaging algorithm reflects the actual heating and cooling characteristics of the conductors and accurately monitors the thermal condition of the conductors. The thermal imaging provides protection from a sequence of intermittent faults that are below the trip unit settings. This allows the normal cycling of loads without nuisance tripping. The thermal imaging is not included in the trip unit curves. The breaker will trip per the trip curve, unless there have been recent intermittent faults that have heated the conductors. A note is included on the trip curves to provide additional information.
  - Instantaneous high current protection: Faults at or above the instantaneous override value are cleared in 25 msec or less.
  - Note: Failure of the digital portion of the ASIC will result in loss of breaker coordination and ground fault protection. The backup analog portion of the ASIC provides basic protective functions only.

The digital portion of the ASIC is a hard-coded, deterministic, continuous loop over-current protection device. The design is very simplistic in nature and has been designed for high reliability. Decisions are made by hard-logic methodology. No conditional instructions, jumps, calls, or interrupt functions are used. The digital portions of the ASIC are designated as follows:

- Microcode is contained in the MCROM, which provides instructions for the sequencing of trip unit activities and arithmetic manipulation of measured current data and user selected protection variables.
- The THROM provides the constants and thresholds, which are used during the manipulation of the measured current data. Decisions are made by hard-logic methodology.

MCROM and THROM are the Schneider/Square D internal designations.

The following additional information is provided on the ASIC architecture:

- The MCROM is a masked program device. It controls the sequence of activity in the safety-related digital portion of the ASIC. The MCROM microcode is contained in an Alcatel CMOS07 masked ROM library.

- The ASIC architecture is deterministic. The continuous loop process completes each cycle every 544  $\mu$ seconds. Instructions are located in the MCROM, which contains 2 Kbytes of microcode for the main program and two start up programs. There are no interrupt driven tasks.
- The MCROM instructions of the digital portion of the ASIC are implemented through one Reduced Instruction Set Computer (RISC) device. Implementation of instructions does not use a compiler or assembler because all instructions are hard coded into the MCROM. The instructions are in the form of 32-bit microcode. The instructions are supplied directly to the RISC device without decoding or sequencing. The operating frequency is 2.0 MHz.
- The ASIC digital protection design has no operating system, multitasking, self-diagnostics, or interrupt usage. All register addresses are singularly unique and are addressed and accessed by hard-coded instructions. The digital portion of the ASIC contains the following components:
  - 6583 logic ports (and-or gates).
  - One RAM 256x32.
  - One ROM 512x32.
  - One ROM 2048x16.
  - One 32x16 Multiplier.
- There are no safety-related communications or handshaking. The ASIC is a hardware device, whose digital protection feature uses hard-wired arithmetic calculator capabilities in order to complete protection algorithms. As configured for safety related applications, the microprocessor's trip unit has no external communication capabilities.
- The THROM contains all thresholds and constants for the calculation of the trip unit protection values. The THROM contains 4 Kbytes of 16 bit digital words. The MCROM contains the microcode which sequences the digital portion of the ASIC's trip unit's execution of the overload protection activities. The MCROM contains 2 Kbytes of 32-bit machine language code.
- The trip unit contains no PROM or external memory. Field programming is not available.
- When the digital portion of the ASIC's protection functions are lost, all user selectable protection functions are lost; however, basic protection functions are retained. The basic protection functions that are retained are detection of a high temperature condition and detection of current in excess of the circuit breaker's interrupt rating.
- There are no hardware or software watchdog timers in the digital portion of the ASIC.

The architecture information above is valid for all Micrologic trip units. The incremental fine tuning (IFT) in the x.xH and x.xP units is implemented by overwriting the rotary switch trip

settings with the IFT settings in the ASIC RAM (EEPROM). Additional information is provided in section 2.2.2.16 of this report.

### **ASIC Operation**

Operation of the ASIC is summarized below. The NLI audit report and Schneider/Square D design data provides additional information.

- A 2.0 MHz clock drives the ASIC microprocessor. A crystal oscillator controls the clock frequency. The sequence of events performed by the microprocessor is dictated by the masked code set located in the MCROM.
- The ASIC startup or restart sequence completes 384 microseconds after the trip unit is powered. During the 384 microseconds start sequence the digital words created by the interface of the rotary switch positions or IFT and the state of the and-or gates are restored. All other information to perform the safety-related function of the ASIC is contained in the MCROM and THROM.
- A complete protection cycle occurs every 544 microseconds. Poles are evaluated in the sequence: O, A, B, C. The logic for each pole is processed in 128 microseconds and the decision to trip or not trip is processed in 32 microseconds. The L, S, G, and I for each pole are calculated separately every 544 microseconds, as applicable. The NLI audit report in Attachment A contains a table which depicts the sequencing of the digital portion of the ASIC after completion of the start up sequence.
  - Each pole (A, B, C) is calculated separately.
  - Each function (L, S, I, G) is calculated separately.
- User selectable trip functions (L, S, I, and G with time delays) are chosen by rotary switch position selection. The rotary switch position configures its portion of the hard-wired decision logic by means of and-or gates. Regardless of model, each rotary switch has its own and-or gate matrix. Each matrix is independent but all are contained in the same silicon device. Each function (L, S, I, G) is logically independent, except as follows:
  - Long time pickup and long time delay are dependant.
  - Short time pickup and short time delay are dependant.
  - Ground fault pickup and ground fault delay are dependant.
- The neutral protection setting is chosen thru the electronic menu.

#### **2.2.2.5 Trip Unit Non-Safety Functions**

The trip unit non-safety related functions are identified below:

- All functions on the HC11 microprocessor are non-safety related (metering, trip indication, communication, display). The HC11 microprocessor is isolated from the ASIC and is considered non-safety related. Details are provided in the following sections.
- The HC16-series microprocessor is safety related. The details are provided in the following sections:
  - The touchscreen can be used for incremental fine tuning, a safety related function.

- The metering, trip indication, and communications functions are non-safety related.

Details of the HC11 and HC16 microprocessors are contained in sections 2.2.2.15 and 2.2.2.16 of this report.

### **2.2.2.6 Trip Unit Input/Output and Signal Conditioning**

#### **Inputs**

The inputs to the ASIC are:

- Up to four (3 primary bus + neutral bus) analog current measurements from air-core CTs are converted through by A-to-D converters into digital words and placed into dedicated registers.
- Up to seven user selectable current and time-delay settings in the form of digital words, which are selected by adjustment of break-before-make rotary switch positions. This provides the user adjustable L (long time), S (short time), I (instantaneous), and G (ground) functions.
  - Series x.xP and x.xH trip units: The user selectable settings can also be input using the incremental fine tuning function. Details are provided in section 2.2.2.16.
- Constants and thresholds contained in the THROM, which are used for calculation of protection values, are compared with the user selected current and time-delay settings.
- The power to the trip device is from the current transformers that are powered from the load side of the breaker primary power.

There is no input range checking provision. The current from the CT is input directly to the A-to-D. The A-to-D digital word is stored in a dedicated register. The word is manipulated by instructions from the MCROM. The result is compared against the user selected protection parameters. If the measured current exceeds the user selected parameters or the instantaneous current rating to the circuit breaker, the trip unit initiates a trip command, which trips the circuit breaker and opens the contacts.

Signal conditioning in the ASIC is limited to analog to digital conversion of AC voltage and current values from the CT's. Analog voltage values are determined by the use of a fixed value resistance bridge located in the ASIC. Analog current values are determined from current transformers. The analog values are converted to digital words by a silicon-based A-to-D converter.

There is no process noise filtering, except as summarized below. It is not required due to the quality of the signal from the CT's. The following additional information is provided:

- A filter capacitor has been installed on the input to the Micrologic due to inadvertent Ap trips due the surges during breaker closure in some applications (see additional details in Section 7.3).
- Air-core current transformers and appropriate analog circuits convert the current input to voltage input for the A-D converter. Resistive voltage dividers and their related analog circuits scale the voltage inputs to the A-D converters. The ASIC is built in a 0.7 micron

process which provides sufficient ruggedness for the current values encountered during 5 volt DC operation. Based on the design, it is not possible for the A to D range to be exceeded.

There is no field calibration of the input signals. There is no digital to analog conversion.

### **Outputs**

The trip unit output (external communications) is summarized as follows:

- There is one safety-related output, the breaker trip command, which is a hard logic decision via AND and OR gates. These are switched by 5 volt (binary one) and 0 volt (binary zero) inputs that result from the user selectable current, time-delay settings, and the arithmetic functions performed in the ASIC. The use of 5 volt logic, rather than 3.3 volt logic, significantly reduces 'half-state' logic errors should there be an unlikely failure in a AND or OR gate p-n junction.
- The trip units have provisions for external communications, such as Modbus. Use of this feature is not a qualified configuration.
- There are no D-to-A converters.
- The status of the circuit breaker's main contacts (OPEN or CLOSED) is communicated by an analog signal sent via auxiliary switch contacts on the circuit breaker itself. These are electrically and physically independent of the trip unit.

#### **2.2.2.7 Trip Unit Alarms and Diagnostics**

There is one failure alarm, Ap, which is an LED display on the trip unit itself. The trip unit designers consider this display as a non-critical for information only output. This is a deliberate design consideration that provides the operator an opportunity to make the decision as to the appropriateness of interrupting power by opening the circuit breaker. The failure alarm light is activated by a hard-logic decision matrix, which is implemented through an AND/OR gate which creates a digital word that is read by the non-safety related microcontroller. The microcontroller subsequently activates the Ap LED in accordance with its programmed instructions.

There is no input range checking provision or data validity checks during operation. During the start sequence diagnostics activities are limited to verification that the user configurable L, S, I, G are restored to the appropriate RAM addresses. During the run sequence the availability of voltage and current data at the appropriate RAM addresses is confirmed. If there is an absence of voltage and current data at the required RAM addresses, the ASIC will detect a failure condition and activate the failure alarm, Ap.

This failure alarm will not trip the breaker.

Other "Advanced Protection, Ap" features are discussed in section 2.2.2.14.

There are no safety-related digital communications outside the trip unit associated with the trip function.

- The status of the circuit breaker's contacts (OPEN or CLOSED) is communicated by an analog signal sent via auxiliary switch contacts on the circuit breaker. These contacts are electrically and physically independent from the trip unit.
- The IR trip indicator LED, Isd/Ii trip indicator LED, and Ap indicator LED are considered as non-critical, for information only outputs by the trip unit designers.

The reset of the indicator LED's is as follows:

- The IR trip indicator LED and Isd/Ii trip indicator LED are reset by depressing the reset button on the face of the trip unit.
- If the Ap fault clears, the Micrologic will operate per design, and the Ap indicator LED will remain on. The Ap indicator LED is reset manually.

### **2.2.2.8 Trip Unit Failure State and Trip Function Diversity**

If the trip unit fails, the breaker will stay in the existing state (opened or closed), as follows:

- If the breaker is open, the trip device is unpowered. The breaker will stay in the open position. The breaker can be manually closed.
- If the breaker is closed, the breaker will stay closed. The backup analog circuits in the trip device would provide thermal and overcurrent protection (see details below). The breaker can be manually opened.
- The failed state is not selectable.
- In case of clock (gate) failure, the ASIC ceases to perform its digital protection functions in accordance with user selected trip parameters and leaves the breaker in the closed position. The Ap indicator LED is lighted to alert operator or maintenance personnel.
- Diverse overcurrent protection is provided by the analog portion of the ASIC as follows:
  - Thermal protection that is measured by a positive temperature coefficient thermistor. When the thermistor reaches 115-125°C, the breaker will trip.
  - Instantaneous overcurrent protection is provided when the current exceeds the circuit breaker's instantaneous overload trip interrupt (DIN) rating.
  - In either condition, the circuit breaker contacts will open within 20 milliseconds.
  - Both of these diverse trip functions are operational following failure of the digital portion of the ASIC or clock (gate) failure.
- In all cases, remote indication of the breaker position and interlocks are through the mechanical auxiliary switches and would not be impacted by the failure of the trip unit.

Note that loss of the digital portion of the trip unit would remove the breaker coordination with upstream and downstream breakers. The purpose of the diverse analog protection is to provide ultimate protection to the breaker and power system. The digital portion of the trip unit (hardware and software) is demonstrated to be highly reliable (see section 5.0) and use of the analog protection is a very low probability event.

#### **2.2.2.9 Trip Unit Internal Power Supply**

The internal power supply in the trip unit is a very simple device, as follows:

- Power is derived from the 3 primary CT's.
- The internal power supply consists of a four-diode bridge rectifier, filter, and regulating circuit. All components are board mounted and are designed for high reliability.
- There is a filter network on the output of the internal power supply.

#### **2.2.2.10 Trip Unit Battery**

Some of the trip unit models contain a battery. The purpose of the battery is to power the memory and external communication features. These features are considered non-safety related. The trip unit protective functions are powered by the breaker CT's and the battery is not required for these functions.

The NLI validation testing verified that the trip unit protective functions operated properly with no battery installed and with a dead battery installed (see the test data in Attachment B).

The battery is not required to maintain the IFT trip settings. See the additional details in section 2.2.2.16.

#### **2.2.2.11 Trip Unit Computer System Redundancy and Diversity**

The trip unit contains no internal redundancy. Nuclear plant system redundancy is discussed in section 6.2 of this report.

The trip unit does contain diverse thermal and instantaneous trip functions that operate in the event of a failure of the digital system. Section 2.2.2.7 of this report provides additional details on the diverse thermal and instantaneous trip functions.

#### **2.2.2.12 Trip Unit Computer System Testability**

The computer system is highly testable as follows:

- Primary injection testing of the breaker is used to confirm operation per the trip curve.
- Secondary injection testing of the trip unit is used to confirm operation per the trip curve.

This testing is performed with the circuit breaker and trip unit out of service.

There is no in-service testing available.

#### **2.2.2.13 Trip Unit Unused Software Function Blocks**

There are no unused software function blocks.

#### **2.2.2.14 Trip Unit Advanced Protection (Ap) Functions**

The advanced protection (Ap) functions are summarized below.

- The Schneider Micrologic manual [33] identifies the Ap functions that are accessible to the user. These functions can provide additional protection and alarms, if configured by the user.

The inadvertent Ap trips that have been documented are the result of protection features that are build into the trip unit. These functions are described in detail in section 7.3.

#### **2.2.2.15 Trip Unit HC11 Microcontroller (used in all xx.A trip units)**

Non-safety related functions, including metering, display, trip indication, and ASIC failure indication, are accomplished with the HC11series microcontroller controlled circuitry. The details are as follows:

- No safety related functions are performed on the microcontroller.
- The microcontroller cannot be used to modify any of the ASIC settings.
- The ASIC communicates with the microcontroller using a closed serial interface through an optical coupler. The ASIC provides metering and indication information to the microcontroller.
- The optical coupler provides electrical isolation between the ASIC and the microcontroller.
- The ASIC will perform all protection functions with the non-safety related microprocessor removed from the trip unit. This is evident because the most basic of the Micrologic trip units, the 3.0 and 5.0, perform all of the core protection functions without any on-board microprocessor.
- No failure modes of the microcontroller have been identified that would disable the ASIC safety related functions.

The trip sequence of operation of the ASIC is as follows. The microcontroller is not involved in the trip sequence.

- The rotary switch positions are converted to 4-bit words by GRAYBIN and sent via the MUX to the ROM (Read-Only-Memory) stack.
- The ROM stack sends the switch settings to the RAM stack which looks-up the THROM table equivalent switch values and inserts those values into the ASIC protection calculation loop.
- If the switch setting protection thresholds are exceeded, a trip command is issued by the ASIC.

There is also a provision for the addition of external communications capabilities to the trip units; however, this option is not addressed in this V&V report. Connection of the external communications is not considered a qualified configuration.

#### **2.2.2.16 Trip Unit HC16 Microcontroller (used in xx.P and xx.H trip units units)**

The HC16 microcontroller performs non-safety related functions, including metering, trip indication, and ASIC failure indication.

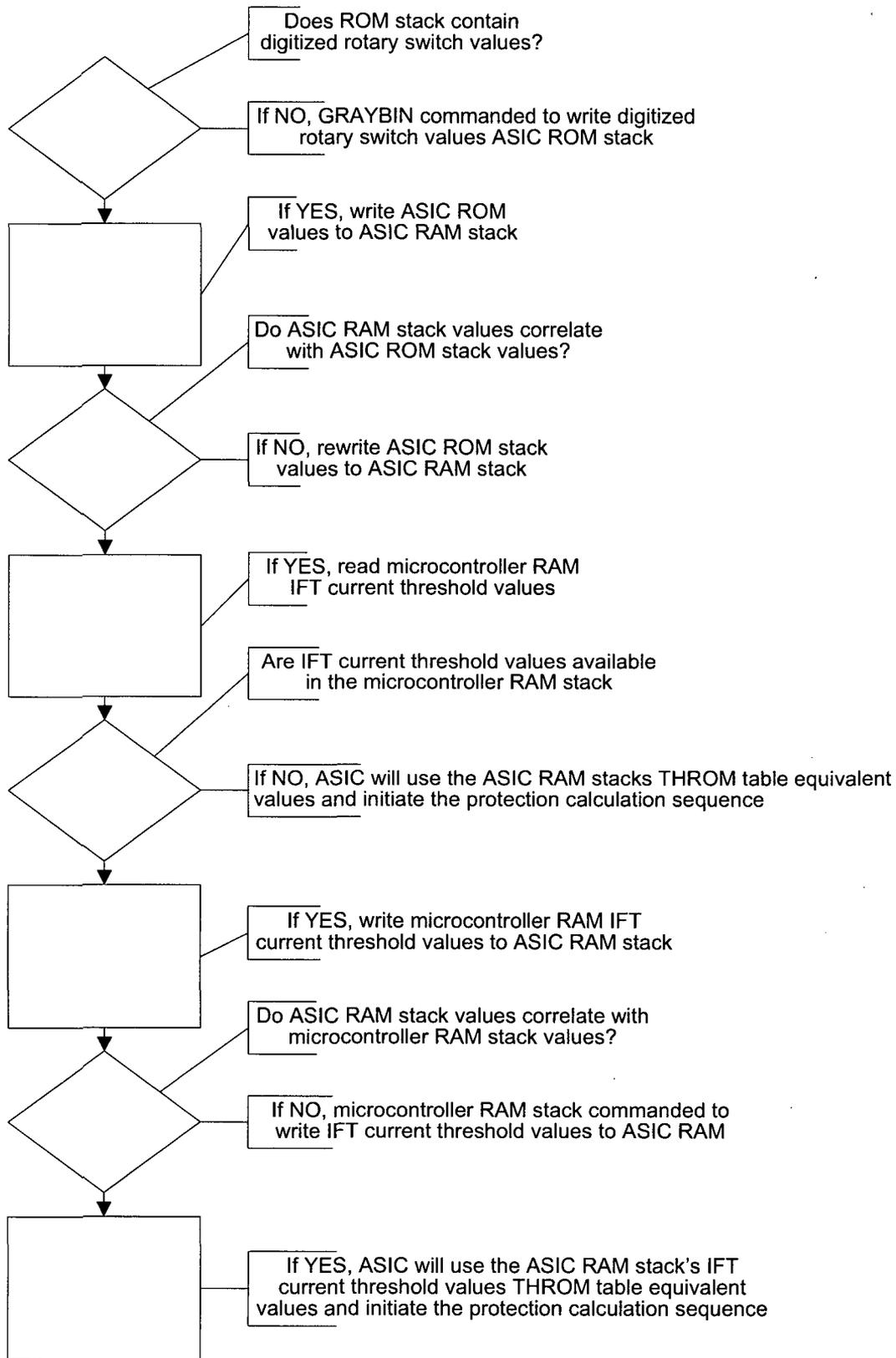
The HC16 microcontroller is also used to perform Incremental Fine Tuning (IFT) of the trip current settings. The IFT of the trip current settings is a safety related function. This is achieved as follows:

- The user selected IFT currents are input using the touchpad on the trip unit. The ITF program instructions cannot be modified.
- The ASIC program instructions cannot be modified. The trip values selected by the rotary switches are stored in the ASIC RAM (EEPROM). These values are replaced with the IFT values in the ASIC RAM. The ASIC RAM stored trip values are implemented by the ASIC using the ASIC on-board THROM stored protection algorithms.

Input of the IFT trip current values are limited as follows:

- The IFT values can only be input to be less than the current rotary switch value. Therefore, the IFT values will always be between the rotary switch value and the next lowest rotary switch setting.
- The IFT cannot be set lower than the rotary switch setting below the current setting.

The following flowchart identifies the IFT sequence to fine tune the trip current settings:



The HC16 microcontroller also allows Incremental Fine Tuning (IFT) of other functions. At no time should any other functions be changed using the IFT function. These functions are implemented by the microcontroller. This is not a qualified condition.

Potential failure modes of the HC16 microcontroller are evaluated as follows:

- Battery failure: Battery failure does not impact the IFT settings.
  - The EEPROM does not require electrical power to maintain the settings. Once the IFT settings are programmed into the EEPROM, loss of the battery will not impact the settings.
  - If the battery fails, the IFT settings cannot be programmed from the touchpad.
- Voltage power supply: An additional voltage power supply is installed in these trip units to power the microcontroller and the larger LCD display. Failure of this power supply will cause the microcontroller to fail. This will cause the trip unit to default to the rotary switch protection settings. This would result in a partial loss of breaker coordination, however, the protective functions will be maintained.
  - The MPE (enable microprocessor) function controls the ability of the microcontroller to input to the ASIC.
    - HIGH (+5 volts): Values of the rotary switch may be overridden by the microcontroller, using the IFT function.
    - LOW (0 volts): Values of the rotary switch may not be overridden by the microcontroller. If the microcontroller is not in service due to a loss of power supply voltage, defective watchdog timer, or a microcontroller hardware failure, a hard-logic latch takes the MPE to LOW.
      - Note: The MPE is held LOW by a hard wired connection in the xx.A series trip units.

Firmware failures of the microcontroller are not considered credible, based on the rigorous Schneider programming and testing regime and the operating history of the trip unit.

No potential failure modes of the HC16 microcontroller are identified that would prevent the ASIC portion of the trip unit to perform the trip function. Failure of the microcontroller would cause the trip unit to revert to the rotary switch settings. This would cause a slight change in the breaker coordination, however, the breaker would still perform the required trip functions.

#### **2.2.2.17 Coil Architecture**

##### **2.2.2.17.1 Summary of Operation.**

**MN: Undervoltage release (UVR).** This release instantaneously opens the circuit breaker when its supply voltage drops to a value between 35 and 70% of its rated voltage. Any attempt to close the circuit breaker equipped with an MN (VR) release when its supply voltage is less than 85% of the rated voltage inhibits closing of the main contacts.

**MX: Shunt trip release (SHT).** This release instantaneously opens the circuit breaker whenever its supply voltage is 50% over its rated supply voltage. This release may have a continuous or transient supply.

**XF: Shunt close (SHCL).** This electromagnet closes the circuit breaker whenever its supply voltage is more than 50% of its rated supply voltage.

#### 2.2.2.17.2 Architecture

The architecture of the coils is as follows:

- (1) The only difference between MX/XF actuators and MN actuator is mechanical. They have the same electrical characteristics (same microcontroller and coils).
- (2) Microcontroller : 8 bit MOTOROLA 68HC805P18
- (3) There have been no firmware revisions since 2002.
- (4) There is no communication in NLI supplied equipment with the trip unit (ASIC or its companion microcontroller).
- (5) Programming language – assembler.
- (6) There are no unused software blocks or complied code.
- (7) All measured parameters are stored in direct addressed RAM.
- (8) Program values are stored in an EEPROM and are read-into the microcontroller ROM during initialization.
- (9) The microcontroller initialization sequence verifies hardware and firmware operation.
- (10) The total code consists of the following eight code modules
  - a. RESS.ASM
  - b. RAM.ASM
  - c. T\_CARRE.ASM
  - d. T\_U.ASM
  - e. T\_IAPP.ASM
  - f. T\_IMAI.ASM
  - g. T\_BOB.ASM
  - h. CONST.ASM
- (11) There are no internal diagnostics other than a time-out watch dog during main loop program operation.
- (12) Power to the coils is from the plant control power. A 5 volt power supply is used to power the electronics. The FMEA did not identify the power supply as a critical part in the design life/mean time to failure (MTTF) of the coils (see section 5.1.3).
- (13) There is no battery used.
- (14) The hardware/firmware system is testable. The NLI dedication/FAT testing tests the system on 100% of the supplied breakers.

(15) The common mode failure evaluation is contained in section 6.3.

### **2.2.2.17.3 Firmware Operating Sequence**

The firmware operating sequence is as summarized below:

#### **Measurement phase**

- Regulation of the maintain current:
  - Maintain current measurement
    - Activate the maintain transistor. Wait 34 $\mu$ s
    - Put CDE\_I=1 during 10 $\mu$ s
    - Input the maintain current measurement
  - Comparison of the maintain current measurement with the previous measurement.
  - Management of transient failures
  - Actuate or inhibit of the maintain transistor.
- Management of BP and COM (if COM module installed) functions:
  - Read the input BP and management of the function BP
  - Management of the function COM.

- Network voltage
  - Read the network voltage
  - FIR filter, which gives an output value each 8 cycles
- Determination of the next condition
  - Functions BP and COM
  - If the output data of the FIR filter is higher than the first threshold, go to the activation phase.

#### Activation phase

- Regulation of activate current:
  - Initiation of the activate current measurement
    - Put  $G\_activate = 1$
    - Input the activate current measurement
  - Comparison of the activate current measurement with the previous measurement.
  - Initiate or inhibit of the activation transistor.
- Network voltage – is there a measured network voltage value or FIR value
- Determination of next condition
  - The firmware remains in the activation phase for 80ms
  - Go to the delay phase

#### Delay phase

- Regulation of maintain current :
  - Maintain the current measurement
    - Activate the maintain transistor. Wait  $34\mu s$
    - Put  $CDE\_I=1$  during  $10\mu s$
    - Input the maintain current measurement
  - Comparison of the maintain current measurement with the previous measurement.
  - Initiate or inhibit of the maintain transistor.
- Network voltage
  - Read the network voltage
  - FIR filter, which gives an output value each 8 cycles
- Determination of next condition
  - The firmware will stay in idle period phase for 30ms
  - Go to the maintain phase.

## 2.3 Human Machine Interface

**Trip Unit:** The Human/Machine Interfaces are as follows:

- All trip units: Rotary switches on the front of the trip unit.
- Series x.xH and x.xP trip units: The touchpad on the front of the trip unit can be used to make the IFT adjustments.

Except for the IFT adjustments, no field programming can be performed on the trip unit. There are no field configurable tuning constants, scaling factors, or other user programming.

**Coils:** There are no human-machine interfaces.

## 2.4 Breaker Test Kits

Schneider/Square D supplies a Full Function Test Kit (FFTK) to test the breaker and collect data from the trip unit. This test kit is summarized as follows:

- The FFTK communicates with the trip unit digitally.
- Operation of the FFTK with the breaker operating is as follows:
  - The FFTK can be connected to a breaker when the breaker is on-line.
  - The FFTK can be used to change/modify the protective settings with the breaker on-line.
  - NLI has not evaluated to condition of the FFTK being connected to a breaker that is installed and operating. The breaker is considered inoperable with the test kit connected to the trip unit.
- The test kits are used to test the trip unit on the bench (secondary injection). The test kit can be used to override some of the trip unit functions when connected to the trip unit (thermal imaging, ground fault).
- When disconnected, the FFTK does not impact the trip unit settings. The trip unit settings are made using the mechanical switches on the front of the unit.
- The FFTK has a RS232 serial port that supports communications with a computer. If this feature is used, the plant must implement the proper cyber security for the connected computer.

Schneider/Square D supplies a Hand Held Test Kit to test the breaker.

- The test kit communicates with the trip unit digitally.
- The test kit cannot be connected to the breaker while the breaker is in operation.
- The test kit is used to test the breaker on the bench. The test kit can be used during testing of the breaker to defeat ground fault and thermal imaging.
- The test kit has no ports to connect to a computer.

## 2.5 Cyber Security

### 2.5.1 Micrologic Trip Unit

Cyber security for the Micrologic trip units is addressed as follows:

- The trip units have the capability for permanently installed communications, such as Modbus. This configuration has not been evaluated by NLI and is not a qualified configuration.
- The ASIC logic gates are analog devices that are not susceptible to viruses or bugs. The logic resides on a ROM (read only memory).
- The trip units can interface digitally with the Schneider/Square D test kits. See the information below on these kits.
- The xx.P and xx.H series trip unit have the capability for performing the IFT functions. The following information is provided:
  - The IFT functions can be programmed from the touchpad on the front of the trip unit. There is no security on this function and it must be controlled procedurally by the plant. Only the trip current IFT function is addressed in this report.
  - Fine tuning of functions other than the trip currents is not addressed in this report. This is an unqualified condition and must be controlled procedurally.
  - Section 1.2 identifies the limitations of this V&V effort. The features that are not addressed in the V&V report should not be used. The non-safety related information must be controlled procedurally.
  - The IFT functions can be programmed using a computer. This is an unqualified condition and must be controlled procedurally.

## 2.5.2 Test Kits

### Full Function Test Kit (FFTK)

Cyber security for the FFTK is addressed as follows:

- Schneider/Square D implement appropriate cyber security measures to verify that the FFTK is supplied virus free.
- The FFTK can be used to change the protective features/functions on the trip unit. The appropriate plant procedures should be implemented to control this activity.
- The FFTK has an RS232 serial port for communications with a computer. If this feature is used, the plant must implement the proper cyber security for the connected computer.

### Hand Held Test Kit

Cyber security for the Hand Held Test Kit is addressed as follows:

- Schneider/Square D implement appropriate cyber security measures to verify that the test kit is supplied virus free.
- The test kit can be used to defeat certain features during breaker testing. It cannot be used to change the protective features/functions on the trip unit. The appropriate plant procedures should be implemented to control this activity.

The test kit does not have ports to connect to a computer.

## 2.5.3 Coils

The coils are hard coded microcontrollers that cannot be field modified. The microcontroller is mounted on a circuit board inside of the coil sealed plastic housing. Opening the plastic housing would damage the coil. No cyber security requirements are applicable.

## **2.6 Traceability of the Test Specimens to the Production Units**

Traceability of the test specimens to the supplied trip units is documented for each project. The following methodology is used to document the traceability:

- The test specimens and the production units will be shown to have the same hardware and software configuration:
  - Trip unit physical configuration.
  - Trip unit part number, revision level, and serial number. (Note: The circuit boards and digital chips in the trip units are not accessible to record the part number and revision level).
- There are no field configurable circuit board settings (DIP switches, jumpers, etc.).
- The functional testing of the test specimen and the dedication testing of the production units will provide added assurance that the production units were manufactured to the same design standards and perform in an equivalent manner to the test specimen.

## **3.0 SOFTWARE QUALITY ASSURANCE AND LIFECYCLE MANAGEMENT**

### **3.1 Software Quality Assurance Plan**

Project activities were performed in accordance with the NLI Nuclear Quality Assurance Program [19], which meets the requirements of 10CFR50 Appendix B, 10CFR21, and ASME NQA-1. The software quality assurance plan for this project is contained in the V&V Plan in Attachment D of this report.

The firmware was developed under the controls of the Schneider ISO9001-2000 quality assurance program. A Software Quality Assurance Plan was developed and implemented for this firmware by Schneider. Additional details are presented in section 7.1.3 of this report and the source inspection of the Schneider facility that is contained in Attachment A.

The dedication, configuration review, and other activities that are performed for each circuit breaker, as identified in section 1.3, are performed in accordance with the NLI Nuclear Quality Assurance Program.

### **3.2 Software Lifecycle Management Plan**

The methods that are used to control the lifecycle of the software is presented in this section. The lifecycle model presented in IEEE 1012 was used to identify the relevant lifecycle steps. The software was developed as commercial grade software and is being dedicated for safety related applications. As such, the explicit documentation requirements in IEEE 1012 are not met.

The Software Lifecycle Management Plan addresses the following:

- NLI Lifecycle Activities: The lifecycle management of the computer system that was previously developed under the controls of the Schneider commercial quality assurance program.
- Plant Specific Activities: The plant specific activities that are performed.

Lifecycle Step	NLI Lifecycle Activities	Plant Lifecycle Activities
Concept	None. This activity was performed by Schneider. It is not relevant to the V&V program being performed by NLI.	Not applicable.
Requirements	NLI audited Schneider. The audits verified that Schneider has a detailed specification for the equipment.	The requirements are documented in the plant specification.
Design	NLI audited Schneider. The audits verified that Schneider used a controlled process for the design of the equipment. See the specific critical characteristics in section 6.0 of this report.	Not applicable.
Implementation	NLI audited Schneider. The audits verified that Schneider used a controlled process for the implementation of the equipment design. See the specific critical characteristics in section 6.0 of this report.	The implementation is documented in the plant specific modification package.
Component Testing	NLI audited Schneider. The audits verified that Schneider used a controlled process for the component testing. See the specific critical characteristics in section 6.0 of this report.	Not applicable.
Integration Testing	NLI audited Schneider. The audits verified that Schneider used a controlled process for the integration testing. See the specific critical characteristics in section 6.0 of this report.	Not applicable.

System Testing	<p>NLI audited Schneider. The audits verified that Schneider used a controlled process for the testing of the trip units. NLI performed independent validation testing of the programmer.</p> <p>NLI performs dedication testing of all supplied equipment.</p> <p>See the specific critical characteristics in section 6.0 of this report.</p>	Not applicable.
Acceptance Testing	Not applicable.	The plant performs acceptance testing prior to installation in accordance with plant procedures.
Installation and Checkout	Not applicable.	The plant performs installation and checkout in accordance with plant procedures.
Operation and Maintenance	NLI supplies plant specific Users Manuals.	The plant performs operation and maintenance in accordance with plant procedures.
Configuration Management	NLI audited Schneider. The audit verified that Schneider has a controlled process for documentation and reporting problems. See section 8.0 of this report for details.	<p>The firmware cannot be field modified.</p> <p>The breaker settings made using mechanical switches. The plant documents and controls the breaker settings in accordance with plant procedures.</p> <p>If the plant uses IFT, the settings must be documented in accordance with the plant procedures.</p>

#### 4.0 ABNORMAL CONDITIONS AND EVENTS (ACE's)

The guidance provided in Annex F of IEEE Standard 7-4.3.2-1993 [1] was used to identify the various ACEs that could impact the capability of the components to perform the intended safety functions. The Abnormal Conditions and Events (ACEs) that could impact the proper operation are identified in this section. The methods which are used to evaluate each of the ACE's are also presented.

**Note: The ACE's and the ACE levels specified below are expected to envelope most of the Class 1E applications in nuclear power plants. Plant specific levels that are not enveloped will be evaluated and tested on a plant specific basis as specified in section 1.3 of this report.**

#### 4.1 Environmental Service Conditions

The following service conditions are defined:

- Operating time: continuous
- Temperature range: 40-104°F (note 1)
- Relative Humidity: 98% (non-condensing) maximum
- Radiation: 5E3 rad gamma

Notes:

1. The maximum temperature of 104°F is the maximum ambient temperature. The components are demonstrated to be acceptable for a total temperature of 121°F (104°F ambient + 17°F in-switchgear temperature rise).

The mild environment qualification is in accordance with IEEE 323-1974/1983 [2], IEEE C37.81-1989 [12], and IEEE C37.82-1987 [13].

Environmental qualification is performed on a plant specific basis, as required to meet the plant specifications.

#### 4.2 Seismic Service Conditions

Seismic qualification of the components on the breaker is performed for each specific breaker configuration. The seismic qualification includes the following:

- Seismic qualification is by testing in accordance with IEEE 344-1975/1987 [3], IEEE 323-1974/1983 [2], IEEE C37.81-1989 [12], and IEEE C37.82-1987 [13]. The test plan provides detailed acceptance criteria for the seismic testing.
- The test specimen includes the replacement breaker with the components installed.
- The TRS envelopes the plant specific RRS. The breaker is qualified to the amplified in-switchgear RRS.
- Note that the trip unit is solid state and is seismically rugged. However, the seismic qualification of the breaker in the switchgear must be demonstrated.

The seismic service conditions are met by testing of the components on the breaker for each breaker configuration.

#### **4.3 Electromagnetic Interference/Radio Frequency Interference (EMI/RFI)**

EMI/RFI emissions and susceptibility requirements are defined for the trip unit based on EPRI TR-102323, revision 1 [6]. The trip unit will be qualified by testing as specified in the project specific qualification plan [29]. The test plan provides detailed acceptance criteria for the EMI/RFI testing.

The EMI/RFI qualification will be met by testing of the trip unit on a representative breaker. This testing is independent of the replacement breaker configuration so only one test will be performed, as follows:

- All replacement breaker configurations use the Masterpact NT or NW breakers. Power to the trip unit is from the CT's on the breaker.
- The only wiring to the trip unit are the wiring from the CT's and the wiring to the actuator. This wiring is self contained and not connected to any plant wiring. Therefore, the breaker wiring does not impact the conducted susceptibility or emissions of the trip unit.
- The trip unit is open at the front of the breaker on all of the replacement breaker configurations. Therefore, the radiated emissions and susceptibility would be the same for all breaker configurations.

The EMI/RFI service conditions will be met by testing of the trip unit on a breaker, for one representative breaker configuration.

In mid-2005, inadvertent Ap tripping was identified in two nuclear plants in the U.S. where replacement Masterpact breakers were installed. Testing by NLI and Square D determined that the tripping was due to high voltage surges. A modification was made to the breakers to eliminate this susceptibility. The issue and testing are fully addressed in NLI qualification report QR-042181-1-SUPP1 [32].

**Coils:** Supplemental EMI/RFI qualification testing was performed on the coils in accordance with EPRI TR-102323, revision 3, as documented in reference [33].

#### **4.4 Voltage Range**

The trip units are powered by current transformers (CT's) on the main bus. The equipment is required to operate across the plant specified voltage range for the AC bus. The standard voltage conditions are specified as follows:

- Typical nominal plant voltages are 480vac and 575vac.
- Minimum voltage will be 480vac (75%) = 360vac.
- Maximum voltage will be 575vac (110%) = 635vac.

The following testing is performed to verify proper operation of the trip units across the voltage

range:

- The NLI Validation Testing verified proper operation at 360vac and 635vac. The test data is contained in Attachment B.
- The dedication testing for each project will include testing across the client specified voltage range.

Note: The purpose of the testing was only to verify the proper operation of the trip unit across any expected voltage range. The actual operating and interrupt rating of the circuit breakers is not addressed by this testing and is in accordance with the Schneider/Square D literature.

Note: The secondary control voltages at the plants are typically 125vdc, 120vac, and 250vdc. The secondary power is not used to power the trip unit. The dedication testing of the circuit breakers with trip units includes testing across the secondary voltage range for breaker trip, close, and charge.

**Coils:** Dedication/FAT testing is performed on 100% of the supplied breakers. The testing include operation of the coils across the plant specific control voltage range. This demonstrates proper operation for the plant specific requirements.

#### **4.5 Infant Mortality of Electronic Components**

##### **Micrologic Trip Unit:**

NLI's previous practice was to burn in the Micrologic trip devices for at least 48 hours during the dedication testing. This was determined to not be necessary and was discontinued. The following information is provided:

- The electronics are burned in by Schneider/Square D during manufacture. The burn-in for the Micrologic trip unit was witnessed by the NLI auditor during the audit, with a burn-in time of approximately 8 hours (overnight).
- NLI's experience with the burn-in of approximately 250 trip units identified no infant failures.
- There has only been one field failure reported to NLI due to failure of electronics. The failure was attributed to the failure of an electronic component. This was identified as an isolated case.
- The NLI dedication testing includes primary injection testing. This exercises the trip unit and verifies proper operation.

Rev. 8

##### **Coils:**

NLI does not have information that the coils are burned-in at Schneider. A burn-in is not considered required as follows:

- The electrical circuit in the coils is a simple circuit.
- The coils are exercised during the dedication testing of the breakers. There have been no failures of the coils during the dedication testing.
- There have been no coils failures reported to NLI from installed breakers.

Rev. 8

#### **4.6 Fault in Non Safety Plant System**

The Class 1E trip units do not interface with the non-safety plant equipment. The trip unit is self contained within the breaker as follows:

- The trip unit receives power from the CT's on the breaker's primary circuit.
- The trip unit sends the trip signal to the actuator in the breaker.

The coils receive safety related control power, so it is electrically isolated from non-safety plant systems.

The EMI/RFI qualification [29, 33] verifies that EMI/RFI emissions from non-safety plant equipment do not impact the operation of the trip units or coils.

Since the trip devices and coils are physically and electrically separated from non-safety related plant systems, faults in these systems will not impact these components.

#### **4.7 Hardware/Software Faults**

Potential faults in the hardware or firmware were evaluated by vendor audit and NLI testing. The fault areas that were evaluated include programming or logic errors, problems with hardware/software integration, potential for unintended functions, potential for data handling problems, and hardware defects. Table 6.1 of this plan identifies the faults that were addressed.

Credible faults in the HC16 microcontroller in the x.xH and x.xP trip units are identified and evaluated in 2.2.2.16. There are no identified faults that are unacceptable.

There are no unacceptable software/hardware faults identified.

#### **4.8 Loss of Power**

By design and construction, the trip units and coils are designed to be unpowered for an indefinite amount of time.

NLI testing verified that the trip units and coils operate properly following loss of power with no loss of programming. The following testing is performed:

- The Validation Testing verified proper operation of the trip units following loss of power. The test data is contained in Attachment B.
- The dedication testing of 100% of the supplied trip units includes primary and secondary injection testing and other functional tests. The supplied trip units and coils will have been unpowered from the time they were tested in the factory until tested by NLI. It is estimated that this is 1 month to 1 year. This will verify proper operation following an extended time unpowered.

As discussed in section 2.2.2.16, the IFT function writes to the EEPROM. Therefore, indefinite

loss of primary or battery power will not result in the loss of these settings.

By design and NLI testing, the trip unit is acceptable for loss of power conditions.

#### **4.9 Overcurrent Condition**

One of the safety functions of the trip unit is to trip the breaker in an overcurrent event in accordance with the published trip curves. The following activities are performed to verify this attribute:

- ANSI design testing is performed as follows.
  - This testing has been performed by Square D on the Masterpact breaker with Micrologic trip unit.
  - Additional ANSI design testing is required for each replacement breaker configuration. This testing will be performed on a plant/replacement breaker specific basis and submitted to the client as part of the design testing.
- The NLI audit of Schneider verified proper programming of the trip curves.
- NLI validation testing verified proper programming of the trip curves.
- NLI dedication testing will verify proper programming of the trip curve for a sample of the trip points on 100% of the shipped trip units.

The V&V, ANSI design testing, and dedication activities document the acceptability of the trip unit to operate in overcurrent conditions.

**Coils:** The coils operate on the control voltage, which is protected from overcurrent conditions by fusing or circuit breakers, in accordance with plant design requirements.

## **5.0 FAILURE MODES AND EQUIPMENT RELIABILITY**

### **5.1 Hardware Failure Modes and Effects Analysis (FMEA)**

#### **5.1.1 FMEA Methodology**

Schneider performed detailed hardware FMEA's which were reviewed by NLI (see reference [33] in Attachment C for the trip unit and section 7.1.8 for the coils). A summary of the FMEA methodology is as follows:

- An external functional analysis was performed. This methodology shows the ties between the studied item and its environment in order to determine a failure relationship. The methodology used is M.I.S.M.E (method of systematic inventory of the surrounding environment). Note: This technique was used as part of the functional and safety requirements analysis performed by the European Organization for Nuclear Research for the CERN Safety Alarm Monitoring System.
- An internal functional analysis by functional block diagram was performed in accordance with MIL-HDBK-217F.
- A dysfunctional analysis was performed showing the consequences of a failure on the operability of the trip unit.
- Reliability calculations were performed in accordance with MIL-HDBK-217F. The results are summarized in section 5.2 of this report.
- An A.M.D.E.C. quantified for a temperature of 40°C in a stationary environment. Note: AMDEC is a technique used for the development of products and processes in order to reduce the risk of failures and to document the actions undertaken. It is part of the QS 9000 'whole quality system' methodology.

#### **5.1.2 Trip Unit FMEA**

##### **5.1.2.1 Summary of Schneider FMEA Results**

Based on data from Schneider, there are two credible failure modes that could impact ASIC operation. These failure modes are identified and evaluated below:

- Loss of clock (gate pulse).
  - This postulated failure results in a loss of the ASIC's digital protection functions. The diverse analog instantaneous and thermal imaging functions are maintained.
  - This failure mode is considered a low probability event based on the simplicity of the design and reliability of the parts used. The equipment reliability documented in section 5.2 includes clock failures.
- Loss of 24 volt DC power.
  - This postulated failure results in a loss of all ASIC protection functions, including the diverse analog instantaneous and thermal trip functions.

- This failure mode is considered a low probability event based on the simplicity of the design and reliability of the parts used. The equipment reliability documented in section 5.2 includes loss of the internal power supply.
- Note: Loss of power will result in loss of the ASIC analog protection functions. The power is required to generate the logic state to initiate the trip command.

Both of these failures are acceptable as follows:

- These are hardware failures in the system and are not a function of the firmware. The hardware is manufactured with a minimum number of components and is highly reliable (see section 5.2).
- Hardware failure of a proven production like the Micrologic trip device is a random event. Common cause failure of this type of hardware is not credible.
- The operating experience for the Micrologic trip devices demonstrates a robust, reliable design. No failures of the clock or power supply have been documented.

The potential failure modes of the HC16 microcontroller and the impact on the trip function are identified and evaluated in section 2.2.2.16 of this report. This data was collected during an audit at Schneider/Square D. No unacceptable failure modes were identified.

#### **5.1.2.2 NLI FMEA Testing**

NLI performed supplemental FMEA testing. The FMEA testing is included with the Validation testing in Attachment B. The following potential failure modes were tested by NLI:

- Remote communications, alarms, and interlocks do not impact operation of the trip unit. Note that these functions are not electrically connected.
- Trip unit operates properly with battery removed or a dead battery.

The trip unit responded as specified in the Schneider design documents during the FMEA testing. No additional failure modes were identified.

#### **5.1.3 Coil FMEA**

The results of the Schneider FMEA for the coils is summarized as follows:

- Function of coil to actuate: The critical parts are the integrated circuit, regulator, comparator, transistors and varistors. The calculated reliability is presented in section 5.2.2.
- Function of energized coil to not inadvertently release (UV release and trip breaker): The critical parts are the transistors and regulator. The calculated reliability is presented in section 5.2.2.
- The microcontroller and the power supply are not identified as limiting parts.
- The reliability of the hardware is identified in section 5.2. The reliability of the hardware is based on the individual components. No especially sensitive components were identified.

NLI performed supplemental testing. Radiation exposure was used to disable the microcontroller. Note that this is a microcontroller hardware failure, not a firmware failure. The results were as follows:

- With the microcontroller disabled, the coils will not respond to the applied and will spring return to the de-energized position:
  - UV coil:
    - If the coil is de-energized, it cannot be energized and the breaker cannot be closed.
    - If the coil is energized, it will spring return the plunger to the extended position and trip the breaker.
  - Shunt trip coil will not pick up.
  - Close coil will not close the breaker.
- This failure mechanism is equivalent to an electrical failure of the same components in the original breakers (spring return to the de-energized position). The microcontroller failure does not introduce an additional breaker failure mechanism.

As identified above, the Schneider FMEA identified that the microcontroller was not one of the components that limits the reliability of the circuit.

#### **5.1.4 Conclusions**

The Schneider/Square D FMEA's were performed in a rigorous manner and addresses the relevant potential failure modes. The FMEA identified two hardware failure modes that could impact the trip unit operation. These failure modes were determined to be acceptable, as identified above.

The NLI testing did not identify any additional unacceptable failure modes.

No potential failure modes have been identified that have unacceptable consequences.

## **5.2 Hardware Reliability**

### **5.2.1 Micrologic Trip Unit**

A hardware reliability simulation was performed by Schneider Electronics in accordance with MIL-HDBK-217F. The calculated failure rates were as follows for ground fixed applications:

- $3.11 \text{ E-6 h}^{-1} @ 40^{\circ}\text{C}$ .
- $5.64 \text{ E-6 h}^{-1} @ 100^{\circ}\text{C}$ .

The design of the trip unit ASIC is based on the previous generation of the Masterpact ASIC design (NSF and NSJ series circuit breakers). The core protection functions in these older generation trip units were accomplished through the use of 350 components. The current Micrologic ASIC design performs the same core protection functions using 53 components. The smaller number of components significantly increases the reliability of the system.

All of the microcode for the present ASIC digital protection is new, though the function of the trip unit is conceptually very similar to the previous design.

Due to the reduced number of components, architectural design, and small amount of microcode, the trip unit is more reliable than any previous analog or digital overload protection model designs.

### 5.2.2 Coils

A hardware reliability simulation was performed by Schneider Electronics in accordance with MIL-HDBK-217F (see the report number identified in section 7.1.8). The calculated hardware failure rates are as follows:

- Failure rate at 105°C:
  - Coil does not energize:  $4.61 \text{ E-6 h}^{-1}$
  - Coil inadvertently releases:  $1.28 \text{ E-6 h}^{-1}$
- Failure rate at 40°C:
  - Coil does not energize:  $1.27 \text{ E-6 h}^{-1}$
  - Coil inadvertently releases:  $3.7 \text{ E-6 h}^{-1}$

The coils have a small number of components, a simple architectural design, and a small amount of microcode. The hardware failure rates of the coils are low.

### 5.3 Firmware Reliability

A software failure modes and effects analysis was not performed. NLI concludes that the firmware is highly reliable. No software flaws or software coding flaws have been identified. The following information is provided:

- A highly controlled process was used to develop and test the software and the software/hardware system (see the details in section 7.1.3 of this report).
- A highly controlled process is used during production of the trip units and coils. (see the details in section 7.1 of this report).
- The logic gates in the trip unit are analog devices that are custom manufactured for the Micrologic design. Since the ASIC protection scheme was designed as a hardware process, there is no firmware in the traditional sense. Program instructions are incorporated into a read only memory (ROM) by layering die-cut metal oxide mask layers during manufacture. This process insures that there is no possibility of the wrong program being loaded or external memory address or data lines to fail.
- Schneider emulation and black-box testing sufficiently verify compliance with design requirements. White-box testing for this type of device is inappropriate because exogenous stimulus to create an out-of-design event is not considered a viable failure mechanism.
- The operating history identifies a highly reliable design (see details in section 7.3 of this report).

- No firmware failures have been identified during NLI testing. No trip units or coils have been returned to NLI with failures due to the firmware.

## **6.0 REQUIRED SYSTEM CHARACTERISTICS**

### **6.1 Verification of Required System Characteristics**

The required system characteristics that the hardware/software systems must possess are identified in Table 6.1. The following information is presented for each critical characteristic:

- Acceptance criteria.
- Results of the V&V activities.
- Reference documents.

Section 7 of this report provides the details on the activities that were performed to verify that the exciter system possesses the required attributes.

Note: During the audit of Schneider and the NLI Validation Testing, critical characteristics were identified that were not included in the V&V Plan [23]. These are included in Table 6.1.

**TRIP UNIT SOFTWARE V&V CRITICAL CHARACTERISTICS**

**TABLE 6.1**

“Ref” documents are the plans that will be used to verify the critical characteristic, as follows:

- VVTP-042181-1 [26]: NLI validation test plan to verify the software/hardware design of the trip unit. These are design tests and will be performed on one of the trip units.
- (Project specific dedication plan) [25]: These production tests and inspections will be performed on 100% of the supplied trip units.
- SVR-042181-1 [21]: NLI audit report of the Schneider Micrologic trip unit facilities which is contained in Attachment A of this report.
- VVR-042181-1: This V&V report.
  - Note: The V&V audit report contained in Appendix A was supplemented by another audit in 12/2008 to collect additional information on the HC16 microcontroller. This data is contained in the body of this report.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
<b><u>Quality Assurance Program</u></b>			
Quality Assurance Program that controlled the development of the software/hardware.	The software and hardware were developed under the controls of the Schneider ISO 9001-2000 quality program.	Verified during the audit of Schneider/Square D. See the summary in section 7.1.3 of this report. Acceptable.	SVR-042181-1
Industry standards used to control the development and testing of the software.	The software is developed and tested in accordance with industry recognized codes and standards.	Verified during the audit of Schneider/Square D. See the summary in section 7.1.3 of this report.  See section 7.1.8 for the data on the coils. Acceptable.	
<b><u>Software Lifecycle</u></b>			
Software specification/software requirements.	Software specification documents the detailed software requirements.	Verified during the audit of Schneider/Square D. See the summary in section 7.1.3 of this report.  See section 7.1.8 for the data on the coils. Acceptable.	SVR-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Procedural controls used during software development.	Software development controlled by Schneider procedures. Document the procedures used and evaluate process.	Verified during the audit of Schneider/Square D. See the summary in section 7.1.3 of this report.  See section 7.1.8 for the data on the coils. Acceptable.	SVR-042181-1
Failure Modes & Effects Analysis	Failure Modes & Effects Analysis performed and used during software development.	Verified during the audit of Schneider and review of the FMEA by NLI. NLI performed supplemental FMEA testing. See details in section 5.1 of this report. Acceptable.	SVR-042181-1 VVTP-042181-1
Development and testing approach.	Schneider developed and tested the software in small function based blocks of code. Development and testing documented.	See the summary in section 7.1.3 of this report. Acceptable.	SVR-042181-1
Independence of software development and testing.	Independent personnel used.	See the summary in section 7.1.3 of this report. Acceptable.	SVR-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Integrated hardware/software testing.	Integrated testing of the hardware/software system was performed.	See the summary of Schneider activities in sections 7.1.3 and 7.1.4 of this report.	SVR-042181-1
		See section 7.1.8 for the data on the coils.	
		NLI performed validation testing of the hardware/software system (see section 7.2 of this report).	VVTP-042181-1
		NLI performs dedication testing on 100% of the supplied equipment (see section 7.2 of this report).	(project specific dedication plan)
		Acceptable.	
Product operating history.	Installed units operating properly. Specify number of operating units, time in service, and number and types of identified problems.	See the summary in section 7.3 of this report.	SVR-042181-1
		Acceptable.	

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Error handling.	1. Code errors are identified, documented, evaluated, and reported in a controlled manner by Schneider. 2. Mechanism for reporting and evaluating user reported problems.	The audit of Schneider verified a controlled program to identify, evaluate, and report errors and changes.	SVR-042181-1
		NLI configuration control activities meet the requirements for safety related equipment.  See the details in Section 8.0 of this report.  Acceptable.	VVR-042181-1
Problem reporting to plant.	Identified problems are evaluated and reported to the client.	The audit of Schneider verified a controlled program to identify, evaluate, and report errors and changes.	SVR-042181-1
		NLI configuration control activities meet the requirements for safety related equipment.  See the details in Section 8.0 of this report.  Acceptable.	VVR-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Software updates and service bulletins.	Schneider has a formal process to alert customers concerning software updates and provides service bulletins.	<p>The audit of Schneider verified a controlled program to identify, evaluate, and report errors and changes.</p> <p>Section 8.0 of this plan identifies the Schneider and NLI actions.</p> <p>Acceptable.</p>	SVR-042181-1
<b><u>Configuration Control</u></b>			
Revision control.	Revision control used on code, chips, and boards.	<p>The audit of Schneider verified a controlled program for revision control.</p> <p>NLI configuration control activities meet the requirements for safety related equipment.</p> <p>See the details in Section 8.0 of this report.</p> <p>Acceptable.</p>	SVR-042181-1 VVR-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Hardware configuration.	Hardware per Schneider and NLI design documentation and drawings.	<p>The audit of Schneider verified the required production controls.</p> <p>NLI dedication testing verifies proper operation and configuration.</p> <p>Acceptable.</p>	<p>SVR-042181-1</p> <p>(Project specific dedication plan)</p>
Electrical interfaces including wire, terminations, and grounding.	Per Schneider/Square D and NLI design drawings.	<p>The audit of Schneider verified the required production controls.</p> <p>NLI dedication testing verifies proper operation and configuration.</p> <p>Acceptable.</p>	<p>SVR-042181-1</p> <p>(Project specific dedication plan)</p>
Manufacturing controls of code.	<p>Controls to assure correct code installed on each unit.</p> <p>Traceability between development and production code is documented.</p>	<p>The audit of Schneider verified proper revision control. See sections 7.1.4 and 7.1.8 of this report for a summary of the production controls.</p> <p>NLI configuration control activities are per section 8.0 of this report.</p> <p>Acceptable.</p>	<p>SVR-042181-1</p> <p>VVR-042181-1</p>

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Regression testing or evaluations.	Regression testing or evaluations performed when code is revised.	<p>The audit of Schneider documented that regression testing has not been required since there have been no changes to the code.</p> <p>NLI dedication testing of replacement parts will document compatibility with the original configuration.</p> <p>Acceptable.</p>	<p>SVR-042181-1</p> <p>Dedication plan for each project.</p>
<p><u>Software/Hardware Critical Characteristics-Trip Unit</u></p> <p>Data storage.</p>	Per Schneider design specifications.	<p>The audit of Schneider verified per the Schneider design documents.</p> <p>Acceptable.</p>	SVR-042181-1
Signal conditioning and logic functions	Per Schneider design specifications.	<p>The audit of Schneider verified per the Schneider design documents.</p> <p>Acceptable.</p>	SVR-042181-1
System response time.	Per Schneider design specifications.	<p>The audit of Schneider verified per the Schneider design documents.</p> <p>Acceptable.</p>	SVR-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Remote alarms and indications.	The communication features are not considered safety related and will not be connected in the plant.	The audit of Schneider verified per the Schneider design documents.	SVR-042181-1
	Local indication is considered non-safety related.	NLI validation testing did not identify potential problems caused by the non-safety indication.	VVTP-042181-1
	The V&V program verified that the non-safety related communication and local indication features will not impact the safety related functions of the trip unit.	Acceptable.	
Watchdog timer.	Per Schneider design.	The ASIC is deterministic and no watchdog timer is in the circuit.	SVR-042181-1
		Acceptable.	
Timing and clock control.	Per Schneider design.	The audit of Schneider verified per the Schneider design documents.	SVR-042181-1
		Acceptable.	

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Output alarms.	Non-safety related. See above.	The audit of Schneider verified per the Schneider design documents.  NLI validation testing did not identify potential problems caused by the non-safety indication.  Acceptable.	SVR-042181-1  VVTP-042181-1
Features which could impact operation.	No features which could interrupt operation (interruptions, diagnostics, manual inputs, non-essential application programs, unauthorized programs or data modifications).	The audit of Schneider verified per the Schneider design documents.  NLI validation testing did not identify features that could impact the trip unit operation.  Acceptable.	SVR-042181-1  VVTP-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Security.	<p>The base program is on the ASIC chip and cannot be field modified. The trip current can be field modified using the IFT function on the x.xH and x.xP units.</p> <p>The trip unit does not contain security. The trip settings can be changed from the front of the trip unit. This must be procedurally controlled by the plant. Note that this is no change from solid state trip units currently used in safety related applications.</p>	<p>Plant configuration control per section 8.3 of this report. Cyber security requirements are per section 2.5 of this report.</p>	VVP-042181-1
Year 2000 compliance.	<p>Units recognize dates beyond 12/31/99 correctly.</p>	<p>N/A. The digital system does not use time sensitive functions.</p> <p>Acceptable.</p>	SVR-042181-1
Processor restart and initialization.	<p>Following removal of power, the trip unit maintains the settings.</p>	<p>By design and Schneider testing, the trip unit maintains all settings during an indefinite removal of power.</p> <p>NLI validation testing verified proper operation following removal of power.</p> <p>IFT settings are also maintained upon loss of power (see section 2.2.2.16).</p> <p>Acceptable.</p>	SVR-042181-1 VVTP-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Data validity checks.	The system contains logic to perform checks of the validity of intermediate results.	<ul style="list-style-type: none"><li>• There are no input range checking provisions or data validity checks during operation. They are not required due to the deterministic operation.</li><li>• During the start sequence, diagnostics verify that the user selected L, S, I, G settings are restored to the correct RAM addresses.</li><li>• The digital system is deterministic and there are no intermediate results.</li></ul> <p>Acceptable.</p>	SVR-042181-1
User configurable input values.	All trip units: The user inputs are hard wired switches. x.xP and x.xH trip units: The IFT function provides user configurable trip current settings.	Use of the hard wired switches to set the trip currents is acceptable. Use of the IFT function to fine tune the trip current settings is acceptable (see section 2.2.2.16). Use of the touchpad to change fine tune other parameters is not acceptable and must be controlled procedurally (see sections 1.2 and 2.5.1).  Acceptable.	This report.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Loss of input instruments.	Trip unit responds to loss of CT signal per Schneider design.	A winding short in a CT would be detected as an overcurrent condition. An open CT would be sensed in the x.0H series trip unit only. Failure of the CT's is not considered a credible failure mechanism due to the design and construction of the CT's.  Acceptable.	SVR-042181-1
Diagnostics.	Not applicable. The programming is deterministic and diagnostics are not required.	Not applicable.	Not applicable.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
<b><u>Software/Hardware Critical Characteristics-Coils</u></b>			
Data storage.	Per Schneider design specifications.	See the data in section 2.2.2.17 Acceptable.	This report.
Signal conditioning and logic functions	Per Schneider design specifications.	See the data in section 2.2.2.17  Acceptable.	This report.
System response time.	Per Schneider design specifications.	See the data in section 2.2.2.17.  Acceptable.	This report.
Remote alarms and indications.	None used in the safety related configuration.	None. The communications features are not connected in the safety related configuration.  Acceptable.	This report.
Watchdog timer.	Per Schneider design.	Timeout watchdog during the main loop program operation. See section 2.2.2.17 of this report.  Acceptable.	This report.
Timing and clock control.	Per Schneider design.	See the data in section 2.2.2.17.  Acceptable.	This report.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Output alarms.	None used in the safety related configuration.	None. The communications features are not connected in the safety related configuration.  Acceptable.	This report.
Features which could impact operation.	No features which could interrupt operation (interruptions, diagnostics, manual inputs, non-essential application programs, unauthorized programs or data modifications).	The audit of Schneider, review of Schneider documents and NLI testing did not identify any features that could interrupt operation.  Acceptable.	This report.
Security.	The firmware is coded on the microcontroller and cannot be field modified.	The firmware is coded on the microcontroller and cannot be field modified (see section 2.2.2.17).  Acceptable.	This report.
Year 2000 compliance.	Units recognize dates beyond 12/31/99 correctly.	N/A. The digital system does not use time sensitive functions.  Acceptable.	This report

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Processor restart and initialization.	Following removal of power, the microcontroller maintains the code.	<p>By design and Schneider testing, hard coding is used. The initialization sequence verifies hardware and firmware operation (see section 2.2.2.17 of this report).</p> <p>NLI dedication testing verifies proper operation following extended duration with no power.</p> <p>Acceptable.</p>	This report.
Data validity checks.	Per Schneider design documents.	<ul style="list-style-type: none"><li>• There are no input range checking provisions or data validity checks during operation. They are not required due to the deterministic operation.</li><li>• The microcontroller initialization sequence verifies that there no hardware or firmware problems.</li><li>• There are no intermediate results.</li></ul> <p>Acceptable.</p>	This report.
User configurable input values.	There are no user configurable input values.	<p>There are no user configurable input values (see section 2.2.2.17 of this report).</p> <p>Acceptable.</p>	This report.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Loss of input instruments.	There are no input instruments.	There are no input instruments (see section 2.2.2.17 of this report).  Acceptable.	This report.
Diagnostics.	Not applicable. The programming is deterministic and diagnostics are not required.	Not applicable (see section 2.2.2.17 of this report).	This report.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
<u>Human Interface Critical Characteristics-Trip Unit</u> Switch settings.	The rotary switches used to set the trip settings operate per the Schneider design.	The Schneider design was verified during the audit.	SVR-042181-1
		NLI validation testing included primary injection testing to validate 100% of the trip settings.	VVTP-042181-1
		NLI dedication testing includes primary and secondary injection testing to verify a sample of the trip settings.	(Project specific dedication plan).
Operation of touchpad or computer.	x.xP and x.xH trip units: The touchpad can be used to change the trip settings.	Acceptable.	
		Use of the IFT function to fine tune the trip current settings is acceptable (see section 2.2.2.16). Use of the touchpad to change fine tune other parameters is not acceptable and must be controlled procedurally (see sections 1.2 and 2.5.1).	This report.
Setting switch security.	Security as specified above.	Acceptable.	
		Per plant configuration control as specified in section 8.3 of this plan.	VVR-042181-1
<u>Human Interface Critical Characteristics-Coils</u>	There are no human-machine interfaces for the coils.	Not applicable (see section 2.2.2.17 of this report).	This report.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
<b><u>Trip unit specific hardware/software critical characteristics</u></b>			
Trip unit operation on Masterpact NT and NW breakers.	Trip unit mounts and interfaces properly with the Masterpact NT and NW breakers, including physical mounting, wiring, CT interface, ratings plug interface, and flux shifter interface.	The audit of Schneider verified the trip unit is for use on the NW and NT Masterpact breakers.	SVR-042181-1
		Validation testing by NLI documented operation on the NW breaker.	VVTP-042181-1
		Dedication testing by NLI on 100% of the supplied breakers will verify proper operation.  Acceptable.	(Project specific dedication plan).
Trip unit interfaces properly with ratings plug.	Trip unit + ratings plug provide trip settings per the Square D published trip curves.	The audit of Schneider verified the trip unit is for use on the NW and NT Masterpact breakers.	SVR-042181-1
		Validation testing by NLI documented operation on the NW breaker.	VVTP-042181-1
		Dedication testing by NLI on 100% of the supplied breakers will verify proper operation.  Acceptable.	Project specific dedication plan.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Trip settings.	Verify that the trip settings are per the Square D curves.	The audit of Schneider verified this critical characteristic.	SVR-042181-1
		Validation testing by NLI tested 100% of the switch settings by primary injection testing.	VVTP-042181-1
		Dedication testing by NLI (test representative settings).  Acceptable.	(Project specific dedication plan).
Function defeats operate properly.	The function is defeated.  Defeat of the function does not impact operation of the active functions.	The audit of Schneider verified this critical characteristic.	SVR-042181-1
		Acceptable.	VVTP-042181-1
		Validation testing by NLI verified this critical characteristic.  Acceptable.	

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
No spurious tripping.	There is no spurious tripping outside the active trip functions and the trip curve.	The audit of Schneider verified this critical characteristic.	SVR-042181-1
		Validation testing by NLI verified this critical characteristic.	VVTP-042181-1
		See additional information in Section 7.3.  Acceptable.	
Non safety functions do not interfere with safety related trip function.	External communications functions are non-safety related. The communication feature will not be connected in the plant.	The audit of Schneider verified this critical characteristic.	SVR-042181-1
	Verify that the communication functions will not interfere with the trip function.	Validation testing by NLI verified this critical characteristic.  Acceptable.	VVTP-042181-1
Breaker position on ASIC failure.	The breaker will remain in the current position upon ASIC failure.	The audit of Schneider verified this critical characteristic.	SVR-042181-1
		Validation testing by NLI verified this critical characteristic.  Acceptable.	VVTP-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Indication on ASIC failure.	If the ASIC fails, and LED on the front of the trip unit will light.	The audit of Schneider verified this critical characteristic.  Acceptable.	SVR-042181-1
Short circuit protection on digital failure.	If the digital portion of the ASIC fails, the trip unit will still provide short circuit protection. See additional details in section 2.2.2.3.	The audit of Schneider verified this critical characteristic.  Acceptable.	SVR-042181-1
Thermal protection on digital failure.	If the digital portion of ASIC fails, the trip unit will still provide overcurrent protection.	The audit of Schneider verified this critical characteristic.  Validation testing by NLI verified this critical characteristic.  Acceptable.	SVR-042181-1 VVTP-042181-1
Battery function.	The battery is not required for the safety related trip function. The trip operates per the trip curve with the battery removed or a dead battery.	The audit of Schneider verified this critical characteristic.  Validation testing by NLI verified this critical characteristic.  Note: The IFT settings are copied to an EEPROM and battery power is not required to maintain these settings (see section 2.2.2.16).  Acceptable.	SVR-042181-1 VVTP-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Trip unit performance upon loss of clock (gate pulse).	The digital protective function is lost. The analog instantaneous and thermal trip functions are maintained.	The audit of Schneider verified this critical characteristic.  Acceptable.	SVR-042181-1
Trip unit performance upon loss of internal power supply.	All trip functions are lost (digital and analog).	The audit of Schneider verified trip unit operation. See the additional data is section 2.1.2.8 of this report.  Acceptable.	SVR-042181-1

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
<u>Coil specific hardware/firmware critical characteristics</u>			
Coils operation on Masterpact NT and NW breakers across voltage range.	Coils mount and interfaces properly with the Masterpact NT and NW breakers, including physical mounting, wiring, and latch interface.	Dedication testing by NLI on 100% of the supplied breakers verifies proper operation. Testing is performed across the plant specific control voltage range (see section 7.2.2 of this report).  Acceptable.	This report.  (Project specific dedication plan).
Coil settings.	There are no coil settings.	Not applicable (see section 2.2.2.17 of this report).  Acceptable.	This report.
No spurious tripping.	There is no spurious operation of the coils (energization or de-energization as applicable).	No spurious operation has been documented by Schneider or during NLI testing. EMI/RFI testing identified no spurious operation. The FMEA addressed the hardware failure rate for spurious operation.  Acceptable.	This report.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
Non safety functions do not interfere with safety related trip function.	Connection of the communication features is not a safety related configuration.	Not applicable (see section 2.2.2.17 of this report).  Acceptable.	This report.
Position upon loss of control power.	Per Schneider design documents.	Spring return of the plunger retracted (shunt trip and close coils) or plunger extended (UV) verified during NLI dedication testing. See section 7.2.2 of this report.  Acceptable.	This report.
Battery function.	No batteries are used.	There is no battery installed (see section 2.2.2.17 of this report).  Acceptable.	This report.
Coil performance upon loss of microcontroller.	Per Schneider design documents.	The coil returns to the spring return position. Per the Schneider FMEA, microcontroller failure is not a significant reliability issue. No impact on the trip function of the breaker.  Acceptable.	This report.

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Results</u>	<u>Reference</u>
<u>ACE's Critical Characteristics</u> The following ACE's are identified: <ul style="list-style-type: none"><li>• Environmental service conditions.</li><li>• Seismic service conditions.</li><li>• EMI/RFI.</li><li>• Voltage range (undervoltage to overvoltage).</li><li>• Infant mortality of electronics.</li><li>• Fault in non-safety plant system.</li><li>• Hardware/software faults.</li><li>• Loss of power.</li></ul>	Components operate properly when exposed to the identified ACE's.	NLI testing and analysis.  The evaluation of each ACE is documented in section 4.0 of this report.  Acceptable.	Section 4.0 of this report.

## 6.2 Separation Criteria

### 6.2.1 Micrologic Trip Unit

The following information on the Micrologic trip units that is related to separation criteria is presented:

- The Micrologic trip units are self-contained on each circuit breaker. They are located within the switchgear cubicle for each breaker, as are the currently installed trip units. Installation of the replacement breaker with the trip units does not change the physical location or separation of the breakers or trip units.
- The electrical interfaces to and from the trip units are fully contained on each breaker.
  - The trip units are powered from the CT's on the breakers, which are powered from the primary bus. Note that the CT's are not directly connected electrically to the primary bus.
  - The trip units receive their input signal from the CT's.
  - The trip units send their output signal to the actuator on the breaker.
  - In the qualified configuration, the trip units do not communicate with any other devices in the plant.
  - The electrical interfaces of the Micrologic trip units are the same as the currently installed solid state trip units.
- If the Micrologic trip units are replacing electromechanical trip units, there are no CT's and wiring. The separation of the Micrologic trip units is still maintained from this configuration, because the trip units are self-contained within each switchgear cubicle.

Installation of the Micrologic trip units maintains the same level of physical and electrical separation as the existing trip units on the low voltage switchgear breakers.

### 6.2.2 Coils

The following information on the Masterpact shunt trip, close coil, and UV trip that is related to separation criteria is presented:

- The coils are self-contained on each circuit breaker. They are located within the switchgear cubicle for each breaker, as are the currently installed devices. Installation of the replacement breaker with the coils installed does not change the physical location or separation of the breakers or the coils.
- The electrical interfaces to and from the coils are fully contained on each breaker.
  - Each coil in a breaker is electrically and physically independent.
  - The coils are powered from external control power.
  - The coils receive their signals from the plant logic outside the switchgear.
  - The output of the coils is a mechanical function (plunger actuation). There is no electrical or digital output.
  - In the qualified configuration, the coils do not communicate with any other devices in the plant.
  - The electrical interfaces of the coils are the same as the currently installed coils.

Installation of the Masterpact coils maintain the same level of physical and electrical separation as the existing trip units and coils on the low voltage switchgear breakers.

### 6.3 Common Mode Failure Evaluation

The following activities were performed by Schneider/Square D and NLI to verify that the components operate as intended:

- **Trip units:** The equipment architecture is robust by design and manufacture.
  - The trip unit is a simple ASIC architecture. It is deterministic with all commands executed sequentially in every cycle without interrupts or jumps.
  - By design, the number of components was minimized. This resulted in a highly reliable system with a very low failure rate.
  - Potential failures of the microcontrollers have been evaluated as follows:
    - X.x.A trip units: The safety related trip function on the ASIC is isolated from the HC11 microcontroller. The microcontroller does not perform safety related functions.
    - X.xP and x.xH trip units: The safety related HC16 microcontroller interfaces with the safety related ASIC. The HC16 microcontroller can be used for IFT of the trip currents. This V&V report documents the acceptability of the microcontroller. No firmware failure modes were identified. Credible hardware failure modes were evaluated and determined to be acceptable (see section 2.2.2.16).
  - The breaker + trip unit maintain instantaneous and thermal protection in the event of failure of the ASIC.
  - With an installed base of over 50,000 trip units, there have been no reported software related failures. The software has not been revised since it was released in 1998.
  - The detailed FMEA by Schneider/Square D and FMEA testing by NLI did not identify any unacceptable failure modes. The two credible failure modes that were identified (see section 5.1) are hardware failures. The robust Schneider design of the trip units eliminate these hardware failures as potential common mode failure mechanisms.
- **Coils:** The equipment architecture is robust by design and manufacture.
  - The components use simple microcontroller architecture. It is deterministic with all commands executed sequentially in every cycle without interrupts.
  - By design, the number of components was minimized. This resulted in a highly reliable system with a very low failure rate.
  - With an installed base of over 100,000 coils, there have been no reported firmware related failures. The firmware has not been revised since 2002.
- The component's design and development was performed in a rigorous manner and is well documented.
- Rigorous production controls are used by Schneider/Square D to assure that 100% of the supplied trip units meet the design requirements.
- Extensive production testing is performed, including the following:

- Schneider tests each algorithm on 100% of the supplied trip units during the production testing. The testing verifies 100% of the functions sequenced by the MCROM instructions, approximately 40% of trip decision calculations supported by THROM data, and approximately 25% of each rotary switch and-or gate logic matrix.
- Schneider tests the supplied coils.
- NLI performs dedication testing on 100% of the supplied breakers, with the trip units and coils installed, as applicable.
- Detailed quality assurance/quality control processes and procedures are implemented throughout the lifecycle of the trip units, by both Schneider/Square D and NLI.
  - Activities performed by Schneider/Square D are controlled by their ISO 9001 quality assurance program. Based on the NLI audit, Schneider/Square D has a comprehensive program for the control of the trip unit design, development, testing, and manufacture.
  - Activities performed by NLI are performed under the controls of the NLI Nuclear Quality Assurance Program.
- The applicable ACE's have been identified and addressed by testing or analysis. Based on these activities, no ACE's have been identified that would prevent operation of the devices.
- Each trip unit and each coil are electrically and physically isolated from the other trip units and coils on the breaker and in the plant. The different coils in the breaker (UV, shunt, close) are electrically isolated from each other.
  - Known ACE's have been identified and addressed by testing or analysis. Some of these ACE's could impact multiple trip devices. Based on these activities, ACE's are not credible failure mechanisms for the trip units.
  - There are no credible single events that could cause failure of multiple trip units.
- Trip units only: The identified plant issues have been addressed with hardware modifications (see section 7.3 for details).

Based on the extensive design, development and testing performed by Schneider/Square D and NLI and the equipment configuration in the nuclear plant, common mode failure of the Micrologic trip units and coils is not considered credible.

## 7.0 IMPLEMENTATION OF REQUIRED CHARACTERISTICS

The activities identified in this section are performed to verify that the components possess the required characteristics identified in section Table 6.1.

### 7.1 Commercial Grade Audit of Square D/Schneider

Audits were performed at the Schneider/Square D facilities that are involved in the design, manufacture, and testing of the Micrologic trip unit. The audit report is contained in Attachment A of this report.

The audits verified implementation of the critical characteristics specified in Table 6.1. The audit demonstrated that the Schneider technical, management, and quality assurance program controlled the applicable critical characteristics as identified in Table 6.1.

A summary of the audit activities and results are presented in this section. The detailed audit results are contained in Attachment A.

A supplemental audit of the Schneider/Square D facilities was performed in December 2008 at the design and engineering facility in Grenoble, France to collect additional information on the HC16 microcontroller. The audit was performed by Archie Bell, who performed the original audit. This information is included in the body of this report.

#### 7.1.1 Summary of Audited Facilities

The firmware was developed by Square D/Schneider under the controls of their commercial ISO 9001-2000 quality assurance program. NLI performed commercial grade audits of the Schneider design and manufacturing facility. The following Schneider/Square D facilities are involved in the design and manufacture of the components and breakers:

Schneider facilities in France that were audited by NLI:

- Grenoble, France: Trip unit design and engineering.
- Montmelian, France: Trip unit manufacture.
- Moirans, France: Manufacture, assembly and testing of the Masterpact breaker modules. The Masterpact breaker is a modular breaker with bolts and screws used to assemble the modules. The various modules include the 3 contact modules, trip unit module, mechanism module, etc. All of the modules are manufactured and tested in fixtures at the Schneider facility in Moirans, France.
- The Square D test facility in Cedar Rapids, Iowa was audited. Some of the design and development testing was performed at this facility. This facility also assembles the Masterpact modules and tests the completed breakers.
- The Square D Services in West Chester, Ohio was audited. This facility receives the assembled and tested Masterpact breakers (with trip units) and assembles them into the replacement breakers with carriages.

- The Square D assembly facility in Columbia, SC was not audited. Some of the Masterpact modules are assembled and tested in this facility. An audit of this facility is not required for the V&V based on the following:
  - No design or manufacturing of the components occurs in this facility. The trip unit and coils are modules that are attached to the breaker.
  - NLI dedication/FAT testing is performed on 100% of the supplied breakers and confirms that the trip devices and coils operate per design.

### 7.1.2 Summary of Audit Activities

The following activities were performed during the audit:

1. Face-to-face interviews with engineering personnel, reviews of testing documents, and analysis of the Micrologic trip unit design documents at Square D's engineering and test facilities in Cedar Rapids, IA.
2. Reviews of the Micrologic design documents with the Schneider's Micrologic design team and quality assurance representatives, inspection of test facilities, verification of measurement and test equipment calibration, reviews of trip unit design methodology, development documentation, control and testing requirements, and analysis of test results and documentation at Schneider Electric's design and testing facilities in Grenoble, France. Additional information was collected during teleconference calls.
3. Interviews with production and quality control personnel, inspection of trip unit production, testing, and packaging operations, and analysis of assemble methods, test equipment certification, and test reports at Schneider Electric's Micrologic production facilities in Montmelian, France. This is the only facility in the world that assembles the Micrologic trip unit.
4. Interviews with production and quality control personnel, inspection of circuit breaker production, testing, and packaging operations, analysis of receipt, in-process and post-production inspection and test methods, test equipment certification, and documentation of test results at Schneider Electric's Masterpact production facilities in Moirans, France.
5. Additional information was transmitted electronically to NLI, to support the V&V activities.

A second audit of the Schneider design and engineering facilities in Grenoble, France was performed in December 2008 to collect additional information on the x.xP and x.xH trip units with the HC16 microcontroller. This data is included in this report.

### 7.1.3 Design and Development Controls (Trip Unit)

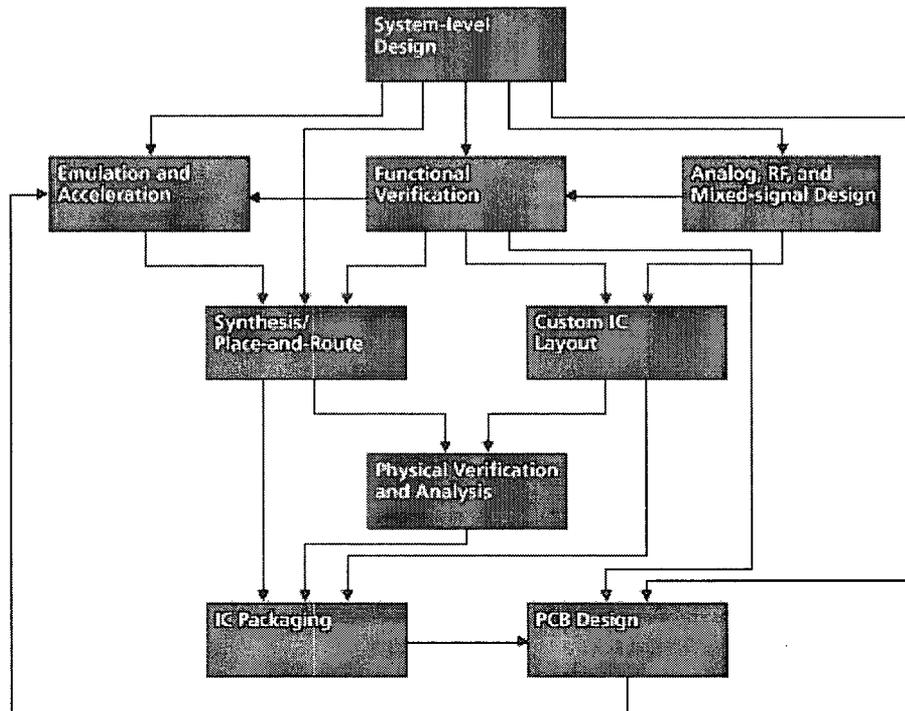
A summary of the design and development controls used by Schneider for the Micrologic trip unit is presented:

- Schneider Electric managed the digital design and microcode development and testing as a hardware project, which is consistent with the design and validation toolsets provided by ASIC manufacturing houses such as AMI Semiconductor (AMIS). The Micrologic design team management and quality assurance activities comply with the intent, where applicable, of the following IEC documents: 1131-1-1992; 1131-2-1992; 1131-3-1992;

and 1131-4-1995 for microcontrollers, which correlate, where applicable, to the requirements of IEEE Standards 830-93, 603-91, 828-90, 1042-87, 1008-87, and 1042-87. The titles and content follow European format and in some cases requirements are combined in a single document.

- Verification and validation of new designs falls under ‘qualification activities’ and are controlled by Schneider Electric Procedure PCO 09. During the design phase, the calculation constants and formulas were determined by simulation. The final versions of the masked program device code (located in the MCROM) and the constants and thresholds (located in the THROM) were finalized based on testing, which was performed and documented in accordance with controlled procedures and plans.
- Extracts of the design documents have been obtained and are in NLI’s possession. Complete versions of the design documents are available for review at the Square D facility in Cedar Rapids, IA. Test plans and reports, quality manuals and procedures, generic ASIC design methodology and implementation methods and techniques, and Micrologic production and testing documentation were reviewed and are available for review at NLI’s facility.
- Good software coding practices were used during the development of the software. The ASIC design requirements were documented using Verilog simulation toolsets specifically designed by Cadence and AMIS for ASIC applications. The good software practices included the following:
  - Data flow was written in a modular, overlay fashion.
  - Design notes are included with the data flow to allow review by a cognizant peer.
  - Design requirements are safeguarded with a tool similar to source safe, which date stamps the file each time that it is saved/closed.
- During prototype coding, the designer performed simulations. All integrated testing was performed by second party or peer reviewers. This approach is consistent with the intent of IEEE Standards 1008-1987 and 829-1983.

- The flowchart below identifies the high-level design flow:



- The software testing and integrated software/hardware testing that was performed is summarized below. This testing was performed during the development and prototype portion of the project.
  - The threshold and constant data contained in the THROM was developed in Grenoble; France using a “C” language program that generated theoretically ideal data, which was documented on a Microsoft Excel spreadsheet.
  - The THROM data was validated by testing in Cedar Rapids, IA.
  - Correction (tuning) of the code was performed in Grenoble, France and implemented through a THROM revision.
  - The MCROM machine level code was written in Grenoble, France and tested in Cedar Rapids, IA to verify that the deterministic instruction loop correctly sequenced the THROM data and the user input digital words.
  - This iterative process continued until the design requirements were met.
- Black box (input/output) testing only was performed during development due to the simplistic nature of the ASIC architecture.
- The following Schneider/Square D controlling procedures were used to control the design process:
  - *Requirements Definition.*
  - *Subcontracting Design Requirements.*

- *Validation of Technical or Design Requirements.*
  - *Project Startup and Progress Tracking (Form).*
  - *Software Quality Assurance.*
  - *Qualification of Products and Systems.*
  - *Storage and Distribution of Quality Document.*
  - *Software Quality Reviews.*
- The following reports document the development testing that was performed by Schneider/Square D:
    - *Test Report – Validation of Micrologic 5.0A Current Measurements.*
    - *Test Report – Aging Tests Applicable to Micrologic 2.0A, 3.0A, 5.0A, and 6.0A.*
    - *Test Report – ASIC Developmental Testing.*
    - *Test Report – Micrologic 5.0A Post Production Testing.*
    - *Test Report -- EMC per ANSI/IEEE C37.90, Test Report – Multiple Power Circuit Breaker Frames per UL 1066, ANSI C37.50 and C37.13, EMC per IEC 60947-2 Annex F.*
    - *Test Plan – Post Production Testing.*
    - *Test Report – Post Production Automated Testers.*

#### 7.1.4 Production Controls and Testing (Trip Unit)

The following summary of the production controls used during the manufacture and testing of the trip devices is presented:

- After production release, engineering oversight was transferred to the sustaining/product improvement organization.
  - This transfer of responsibility was accomplished in accordance with procedure *Transfer of Technical Management after Product Release.*
  - Activities after product release are performed in accordance with procedure *Project Activities after Product Release.*
- The following Schneider/Square D procedures control the production processes:
  - The requirements for procurement are identified in procedure *Purchasing of Inventory Items.* Items are purchased from two levels of approved suppliers. Certified supplier's products are accepted without additional testing based upon a defined grading system. Products from uncertified suppliers are subject to acceptance testing, which are performed in accordance with documented plans. Incoming certified products are differentiated from non-certified products by a two-alpha prefix on the item's part number.
  - Production planning and control is accomplished in accordance with the following procedures:
    - *Design Review and Production Startup (Form).*
    - *Production Planning.*
    - *Modification of Production Plans.*
    - *Distribution and Modification of the Production Plan.*
- A summary of the production process is as follows:

- The overall architecture and design, MCROM and THROM microcode and data, functional and environmental testing against IEC standards, and test design was performed at Schneider in Grenoble, France.
- Alcatel (Belgium), now AMI Semiconductor, <http://www.amis.com>, performed the analog design, mechanical layout, and manufactures the ASIC semiconductor device, which includes masking the code for the MCROM and THROM devices.
- AMIS provides the completed, tested silicon devices to Solectron Corporation, <http://www.solectron.com>, where the Micrologic printed wire boards are manufactured.
- Solectron Corporation provides the manufactured and tested printed wire board assemblies to Schneider Electric's assembly plant in Montmelian, France where the Micrologic trip units are fully assembled and tested.
- AMI Semiconductor and Solectron Alcatel both have ISO 9001-2000 compliant quality assurance programs and are certified suppliers of Schneider Electric.

A high level of control and quality is maintained by Schneider/Square D throughout the production process.

- A summary of the production testing performed by Schneider prior to shipment is as follows:
  - After assembly, the Micrologic trip units are functionally tested to verify compliance with the design requirements at Schneider Electric's production facilities in Montmelian, France. The testing verifies 100-percent of the functions sequenced by the MCROM instructions, approximately 40-percent of trip decision calculations supported by THROM data, and approximately 25-percent of each rotary switch and-or gate logic matrix.
  - The production testing is performed by automated means using a robotic test bed and automatic test equipment. Automated testing of the completed trip unit assembly verifies the correct hardware and software configuration of the assembly. Automated testing is performed in accordance with Schneider Electric document "*Plan for the Four Function Testers PROXIMA*", Revision T, dated 2/19/2002. The automated testing is performed using software controlled M&TE. The verification and validation activities for the testing software is documented in Schneider Electric document "*Qualification of the Four Function Testers PROXIMA*", dated 2/5/2003.

The production testing performed by Schneider provides a very high level of confidence that the supplied trip devices are in accordance with the design documents.

### **7.1.5 Product Support**

The long term product support that will be provided by NLI and Schneider is summarized in section 8.0 of this report.

### 7.1.6 Audit Documents

Extracts of the design, testing, and production documents have been obtained and are in NLI's possession. Complete versions of the design documents are available for review at the Square D facility in Cedar Rapids, IA. Test plans and reports, quality manuals and procedures, generic ASIC design methodology and implementation methods and techniques, and Micrologic production and testing documentation are available at NLI's facility in Fort Worth, TX.

The Schneider documents which were made available to NLI are maintained in accordance with the NLI Quality Assurance Program. Some Schneider documents are proprietary to Schneider and were reviewed during the audit but will not be released to NLI.

### 7.1.7 Trip Unit Microcontrollers

The requirements for the ELU and ELH microcontroller software (firmware) are documented in Schneider Electric design specification PROA\_NAA, Version 1.1, dated 4/23/2002. The design concept was further amplified in Schneider Electric specification, Conception des Protections Avancées ELU/H, dated 5/13/2004. Coding was performed in accordance with Schneider Electric coding specification N° 5100511735, Version 4, dated 9/14/2001. The code consists of 41 modules. Only 9 modules instruct management of IFT current threshold data, main program loop and related interrupts, and ASIC communications. The majority of the remaining modules implement the remaining IFT and display functions. The program uses a RTXC operating system and is coded in C and assembler. The operating system was exhaustively tested by Schneider Electric prior to its selection for use for controlling the ELU and ELH advanced protection and display functions. Integrated hardware/software testing is documented in Schneider Electric report GT040349, Declencheur PROXIMA Micrologic 5.0P 6.0H, dated 6/28/2004.

### 7.1.8 Coil Documentation

The lifecycle of the coils is controlled under the same ISO 9000 quality assurance program and implementing procedures as the trip units. The controls and higher level procedures identified above are applicable to the coils.

The following specifications and procedures are applicable to the coils. These documents were reviewed and the applicable information was included in this report.

- **Technical Design Requirements:** Schneider Electric document 5100512854, Revision B, PROXIMA Auxiliary Design File, (English Translation), dated 3/11/2005.
- **PROXIMA Auxiliaries Relay Software Specification:** Schneider Electric document 5100512993, Revision B, Description of PROXIMA Auxiliary Software (English Translation), dated 12/12/2005.
- **Coding Specification:** Schneider Electric document 5100511735, Revision 4, Manual for the Development of Program Code, dated 9/14/2001.
- **Acceptance Test Requirements:** Schneider Electric document 5100561500, Revision A1, Functional Test Specification for PROXIMA Auxiliaries, undated.

- **FEMA Documents:** Schneider Electric document 51311620, Revision B, Study of Reliable Function of PROXIMA Auxiliaries, dated 1/20/2003 (references MIL-HDBK-217) – firmware not considered.

## 7.2 NLI Testing

Testing and analysis is performed by NLI to fully document the V&V of the components. The testing and analysis address the critical characteristics identified in Table 6.1, as applicable.

### 7.2.1 Qualification Testing

Qualification testing and analysis will be performed in accordance with the requirements for each utility. The testing will be performed on a single test specimen which is the same configuration as the production units which are being delivered. This testing will include the following:

- EMI/RFI testing.
- Seismic testing.
- Mild environment analysis.

Sections 4.1-4.3 provide details on the qualification testing.

The qualification reports are separate documents.

### 7.2.2 Dedication Testing

100% of the production units will be dedicated to verify the functional requirements of the computer based systems are met. The dedication will be based on testing 100% of the supplied units as identified in section 1.3 of this plan. The testing specified in the dedication plan will be performed at the NLI facility and/or the Square D facility with NLI personnel witnessing the testing. The dedication testing will include the applicable ANSI Production Tests.

The characteristics that will be verified by dedication testing are identified in Table 6.1.

The dedication plans and dedication reports are separate documents.

**Coils:** The dedication testing includes testing across the plant specific control voltage range, including undervoltage and overvoltage conditions. This testing is performed on 100% of the supplied circuit breakers.

### 7.2.3 Validation Testing

NLI has performed validation testing [13] to verify that the trip units meet the Schneider design specifications. This testing supplements the data collected during the audit of Schneider.

The characteristics that were verified by the validation testing are identified in Table 6.1. The validation test plan and test data sheets are contained in Attachment B. The basis for the validation test plan sample size is documented in the test plan.

The trip unit responded as specified in the Schneider design documents during the Validation testing.

Based on the information supplied by Schneider, it was determined that no additional validation testing was required for the coils.

#### **7.2.4 Failure Modes & Effects Testing**

As discussed in section 5.1.1, detailed FMEA's were performed by Schneider. The supplemental testing performed by NLI is also identified in section 5.1.1.

#### **7.2.5 ANSI Design Testing**

The Masterpact breaker with the Micrologic trip unit has previously been design tested per the applicable ANSI requirements.

Additional design testing will be performed on each replacement breaker configuration in accordance with the requirements of ANSI C37.59 [18].

### **7.3 Operating History**

#### **7.3.1 Firmware Operating History**

##### **Trip Units**

The following operating history information was provided by Schneider [20]. This data applies to the current generation of the Micrologic hardware and current revision of the ASIC (v.2.7):

- There have been no revisions to either the THROM/MCROM microcode or the ASIC hardware since its production release in 1998.
- Over 50,000 Micrologic trip devices using the current ASIC MCROM microcode revision are in use, with approximately 17,000 deployed in the United States.
- Schneider has been shipping the same version since product rollout during 1998. To date, none have been recalled.
- No outstanding, uncorrected software errors exist at this time.
- Presently, no microcode revisions are planned.
- Schneider intends to support this product for the foreseeable future.

##### **Coils**

The following information was provided by Square D/Schneider. This information is applicable to the current revision of the coil firmware.

- There have been no revisions to either the code or the hardware since the production release in 2002.
- Schneider has been shipping the same version since 2002. To date, none have been recalled. No firmware failures have been identified.
- Approximately 100,000 units have been sold in the past 2 years.
- No outstanding, uncorrected firmware errors exist at this time.

- Presently, no microcode revisions are planned.
- Schneider intends to support this product for the foreseeable future.

NLI dedication tests 100% of the coils across the plant specified control voltage. There have been no coil failures during dedication. NLI has no coils returned due to field failures.

The large installed base with no reported software problems and no software revisions indicates a high level of equipment reliability.

### **7.3.2 Hardware Operating History**

Two hardware modifications have been made to the Micrologic trip device since 2005. These modifications are evaluated in the following sections. These issues are hardware only and do not affect the firmware.

#### **7.3.2.1 Capacitor to Reduce Electromagnetic (EM) Susceptibility**

Inadvertent Ap trips were identified in the fall of 2006 in applications where the breaker was used to start a motor (OE 21873, OE 21799). The trip would occur when the breaker was closed to start a motor. Extensive testing was performed by NLI and Square D. The inadvertent tripping was attributed to a voltage surge during closure of the breaker that is interpreted by the Micrologic trip device as a short circuit condition.

Square D modified the design of the Micrologic circuit to add a filter capacitor. The purpose of the capacitor was to eliminate the inadvertent trip. Surge testing of the modified design was performed at 6kV. The testing addressed the configuration where the breaker is used to start the motor (surge during the breaker closing operation). There were no inadvertent trips. The 6kV test level is much greater than the test levels specified in EPRI TR-102323 and the ANSI standards.

The impact of this modification on the qualification and V&V of the Micrologic trip device is as follows:

- V&V: The modification is a hardware change only. There is no modification of the firmware. There is no impact on the V&V of the Micrologic.
- EMI/RFI qualification: EMI/RFI susceptibility is reduced by the modification. The capacitor is a passive component, so the modification does not impact the EMI/RFI emissions of the trip unit.
- Seismic Qualification: The added capacitor is a small, board mounted device. It is seismically insensitive and will not impact the qualification of the Micrologic.
- Design Life: The capacitor type used in the filter is the same type of capacitor used in other locations in the Micrologic. There is no impact to the design life.
- Reliability: The modification addresses and identified problem and will increase the reliability of the trip unit.

### 7.3.2.2 Performer Plug Modification

In the fall of 2007, two cases additional cases of inadvertent Ap trips were identified (OE 26769). These trips were on breakers with the new Micrologic trip unit design. The trips occurred when the breakers were being used to start motors.

Square D/Schneider evaluated the inadvertent Ap trips. The root cause was identified as the mechanical pin connection between the performer plug and the Micrologic trip device. The performer plug is plugged into the trip unit. The performer plug is factory installed and defines two types of fault protection.

- Maximum instantaneous fault level.
- Maximum close into the fault level: This fault level is lower than the instantaneous level. This protects the circuit breaker if it is closed into a fault.

In a very small number of cases, the mechanical shock of closing the breaker causes a short time discontinuity in the plug connection between the performer plug and the trip unit. This discontinuity causes the “maximum close onto fault level” to revert to a very low value current for a very short time. If this discontinuity occurs during the motor inrush (when the breaker is used to start a motor), this low level can be below the motor inrush current, which would cause the breaker to Ap trip.

The manufacturing tolerance of the female pin connector on the performer plug causes the problem. This problem occurs on a very small number of the connectors.

The design of the performer plug was modified to improve the reliability of the breakers and to eliminate this issue. All breakers supplied after 5/2008 contain the modified performer plug.

The impact of this modification on the qualification and V&V of the Micrologic trip device is as follows:

- V&V: The modification is a hardware change only. There is no modification of the firmware. There is no impact on the V&V of the Micrologic.
- Electromagnetic Interference/Radio Frequency Interference (EMI/RFI) Qualification: The modification does not change the circuit of the performer plug. Therefore, it will not impact the EMI/RFI qualification.
- Seismic Qualification: The modification makes the performer plug/trip unit pin connections tighter. This will increase the seismic resistance of the equipment. There is no impact on the seismic qualification.
- Design Life: There is no change in the materials of the part. There is no impact to the design life.
- Reliability: The modification addresses and identified problem and will increase the reliability of the trip unit.

### **7.3.2.3 Other Operating Experience**

Other nuclear plant operating experience has been reviewed (OE 24418, 24311, and 23935) have been reviewed. These issues are hardware issues and are not related to the Micrologic trip units. These issues have been addressed in the NLI design and dedication activities.

### **7.3.2.4 Coils**

No hardware modifications have been made to the coils since they were released in 2002. No hardware issues have been identified by NLI or Square D. No coils have failed NLI dedication testing (100% sample size) and no coils have been returned from the client due to failures in the field. No nuclear plant operating experience issues (OE's) have been identified for the coils.

## **7.4 Users Manuals**

The Schneider/Square Users Manuals have been reviewed by NLI. The manuals are accurate and provided the required level of detail.

NLI prepares Users Manuals for the supplied equipment. The NLI Users Manuals address the plant specific requirements and nuclear industry specific issues. The NLI Users Manuals include copies of the applicable Schneider/Square D manuals.

## 8.0 CONFIGURATION MANAGEMENT PLAN

### 8.1 Schneider Firmware Configuration Control and Error Reporting

The activities summarized below are performed by Schneider for the long term support of the Micrologic trip unit and coils.

- Configuration management, both revision control and revision verification, is accomplished using the VERILOG tool set. Configuration management requirements are documented in Schneider Electric controlled procedures. The configuration management activities comply, as applicable, with the intent of IEC 1131-1-1992, IEC 1131-4-1995, and IEEE Std. 1042-1987.
- Management, resolution, and communication of customer reported defects are controlled in accordance with the following Schneider/Square D procedures:
  - *Managing Customer Complaints.*
  - *Managing Customer Returns.*
  - *Communication of Product Defects.*
- Upon receipt, a customer complaint is documented in a worldwide product quality database (*Product quality database (LV InSchneider area)*). Locally developed decisions are reviewed and validated at Schneider Electric corporate design and quality assurance. Solutions outside of local capabilities are submitted to Schneider Electric corporate for resolution. Once a solution is implemented and verified, the defect and its resolution are made available to all Schneider Electric service centers for distribution.
- Schneider's corrective action complies with the requirements of ISO 9002-1994 and 9001-2000.
- The mechanism used to implement the customer feedback process is for customer reported errors to be processed and resolved in the USA through the Square D customer service program, which receives updates from the world wide Schneider Electronics network.
- Code revisions:
  - **Trip unit:** Presently, no microcode revisions are planned. Should a product enhancement be made to add additional capability, the THROM constants and thresholds may be changed, but no MCROM microcode revisions would be considered necessary. With any microcode revision, full configuration control measures would be taken. Testing would include regression testing during the integration phase. Microcode design development, testing, maintenance, and retirement activities comply with the intent of a software lifecycle management scheme as describe in IEEE Standard 1074-1995.
  - **Coils:** No changes to the code are planned. If revisions are made, the configuration control activities would be as specified above.

- The metrics that are used for product trends are field failure ranked for the following:
  - Hardware.
  - Software.
  - Electrical.
  - Display.

## **8.2 NLI Configuration Control**

The following process is used by NLI to identify, document, evaluate, and report firmware modifications and errors:

- NLI documents the as-supplied hardware and firmware configuration for 100% of the supplied trip units. The following information is identified for the each trip unit:
  - Trip unit part number and serial number.
  - Chip and firmware part number and revision number, as available.
- NLI contacts Schneider every year and any modifications or reported errors will be identified.
- Errors will be documented and evaluated in accordance with the NLI Nonconformance Report (NCR) process [28]. Notification in accordance with 10CFR21 will be made in accordance with NLI procedures [28], if required.
- Design changes which are not the result of errors will be evaluated by NLI for impact on the existing system and future replacement trip units.
- NLI will submit all NCR's and 10CFR21 reports associated with the trip unit hardware and software to the client. Evaluation of design changes will also be submitted.

This approach is based on the following:

- The Schneider audits and the NLI testing will verify the as-supplied configuration.
- Schneider will not make the source codes available to NLI. Schneider will not freeze the hardware or software configuration.
- Schneider has a controlled program for the following activities :
  - Document revisions to hardware and software.
  - Perform regression testing and/or analysis to fully evaluate the impact of the hardware and software changes on the system. The test method and results are documented in an auditable form.

## **8.3 Plant Lifetime Configuration Control**

Configuration control following delivery of the equipment is the responsibility of the nuclear plant. It is recommended that the configuration control procedures address the following issues:

- Changes to the trip settings using the switches on the front of the trip unit must be procedurally controlled. Note that the same procedural controls are currently implemented on existing solid state trip units.
- The breaker is considered inoperable with the FFTK connected.
- The FFTK can be used to purposefully or inadvertently change the trip

settings/functions on the trip units. Use of the FFTK should be procedurally controlled. The following should be done as a minimum:

- Control access to the FFTK.
- Personnel training on the use of the FFTK.
- The trip settings should be verified just before or after the FFTK is disconnected.
- Communications features external to the circuit breakers cannot be enabled (trip unit, shunt trip, UV, close).
- (xx.P and xx.H series trip units only): If the Incremental Fine Tuning (IFT) feature is used, the following requirements should be met:
  - Procedureally control the trip setpoint changes.
  - Document the ITF settings that are input.
  - Input the ITP settings using the touchpad on the trip unit, not an external connection.
- The cyber security recommendations in section 2.5 of this report should be followed.
- Section 1.2 of this report identifies limitations to the qualified configuration. These limitations must be controlled as follows:
  - Hardware limitations, such as no external power supply or permanent communications, are controlled by the system design.
  - The other limitations are controlled procedurally.

## 9.0 QUALITY ASSURANCE

Project activities were performed in accordance with the NLI Quality Assurance Program which meets the requirements of 10CFR50 Appendix B, 10CFR21 and ASME NQA-1 [19].

## 10.0 MEASUREMENT & TEST EQUIPMENT

Measurement & Test Equipment used by NLI during testing is controlled by the NLI M&TE program (procedure NLI-QUAL-05, latest revision). The NLI test data sheets document the M&TE that is used during the testing. The calibration of M&TE is traceable to NIST or equivalent standards.

## 11.0 REFERENCES

Note: (project specific) indicates NLI documents that are developed for each specific breaker/trip unit supply project.

### Industry/Regulatory Documents

1. IEEE Std 7-4.3.2-1993, "IEEE Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations."
2. IEEE 323-1974/1983, "IEEE Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations."
3. IEEE 344-1975/1987, "IEEE Recommended Practices for Seismic Qualification of Class 1E Equipment for Nuclear Power Generating Stations."
4. EPRI TR-102348, "Guidelines for Licensing of Digital Upgrades", 12/1993.
5. EPRI TR-106439, "Guideline on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications", Final report, October 1996.
6. EPRI TR-102323, "Guidelines for Electromagnetic Interference Testing in Power Plants," revision 1.
7. IEEE 730-1989, "Software Quality Assurance Plans."
8. IEEE 1012-1986, "Standard for Software Verification and Validation Plans."
9. IEEE 1028-1988, "IEEE Standard for Software Review and Audits."
10. ASME NQA-1a-1995, Appendix 7A-2, "Nonmandatory Guidance for Commercial Grade Items", 1995.
11. EPRI 5652, "Guidelines for the Utilization of Commercial Grade Items in Nuclear Safety-Related Applications."
12. IEEE C37.81-1989, "IEEE Guide for Seismic Qualification of Class 1E Metal-Enclosed Power Switchgear Assemblies".
13. IEEE C37.82-1987, "IEEE Standard for the Qualification of Switchgear Assemblies for Class 1E Applications in Nuclear Power Generating Stations".
14. IEEE 384-1977/1981/1992, "Criteria for Separation of Class 1E Equipment and Circuits".
15. NRC R.G. 1.75, "Physical Independence of Electrical Systems".

16. NRC R.G. 1.89, "Qualification of Class 1E Equipment for Nuclear Power Plants".
17. NRC R.G. 1.100, "Seismic Qualification of Class 1E Equipment for Nuclear Power Plants".
18. IEEE C37.59-2002, "IEEE Standard for Conversion of Power Switchgear Equipment".

**NLI and Schneider/Square D Documents**

19. NLI Quality Assurance Manual, Rev. 8, 12/14/07.
20. Schneider Electric manual 48049-137-04, "Micrologic 5.0P and 6.0P Electronic Trip Units", revision dated 05/2003.
21. NLI audit report of Schneider/Square D, report SVR-042181-1, revision 0, (contained in Attachment A of this report).
22. (not used)
23. NLI V&V Plan VVP-042181-1, "Software Verification and Validation Plan for Square D Micrologic Trip unit", revision 0 (contained in Attachment D of this report).
24. NLI design drawings for breaker/trip unit (project specific).
25. NLI dedication plan with dedication test data (project specific).
26. NLI Software/Hardware Validation Test Plan with test data, VVTP-042181-1, revision 0 (contained in Attachment B of this report).
27. NLI Instruction Manual (project specific).
28. NLI Procedure NLI-QUAL-08, "Nonconformances and 10CFR21 Reporting," (latest revision).
29. NLI EMI/RFI plan and report (project specific).
30. Schneider Electric manual 48049-207-03, "MICROLOGIC 2.0, 3.0, and 5.0 Electronic Trip Units", dated 12/01.
31. Seismic plan and report (project specific).
32. NLI Qualification Report Supplement QR-042181-1-SUPP1, "Supplemental Qualification Report for Square D Micrologic Trip Unit".

33. NLI report QR-042181-5, "EMI/RFI Qualification Report for Masterpact Circuit Breaker Shunt Trip and Undervoltage Trip", (latest revision).

**Attachment A**

**Trip Unit Configurations and NLI Audit of Schneider/Square D**

## **Trip Unit Configurations**

## Masterpact® NT and NW Universal Power Circuit Breakers Micrologic® Electronic Trip Systems

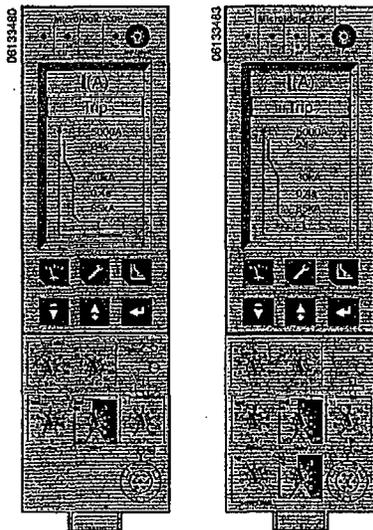
**Table 20: Micrologic Trip Unit Features**

Feature	Micrologic Trip Unit (X = Standard Feature O = Available Option)										
	Standard			Ammeter				Power		Harmonics	
	2.0	3.0	5.0	2.0A	3.0A	5.0A	6.0A	5.0P	6.0P	5.0H	6.0H
LI		X			X						
LSO	X			X							
LSI			X			X		X		X	
LSIG/Ground-Fault Trip <sup>1</sup>							X		X		X
Ground-Fault Alarm/No Trip <sup>1,2</sup>								X		X	
Ground-Fault Alarm and Trip <sup>1,2</sup>									X		X
Adjustable Rating Plugs	X	X	X	X	X	X	X	X	X	X	X
True RMS Sensing	X	X	X	X	X	X	X	X	X	X	X
UL Listed		X	X		X	X	X	X	X	X	X
Thermal Imaging	X	X	X	X	X	X	X	X	X	X	X
Phase-Loading Bar Graph				X	X	X	X	X	X	X	X
LED for Long-Time Pick-Up	X	X	X	X	X	X	X	X	X	X	X
LED for Trip Indication				X	X	X	X	X	X	X	X
Digital Ammeter				X	X	X	X	X	X	X	X
Zone-Selective Interlocking <sup>3</sup>				X		X	X	X	X	X	X
Communications				O	O	O	O	X	X	X	X
LCD Dot Matrix Display								X	X	X	X
Advanced User Interface								X	X	X	X
Protective Relay Functions								X	X	X	X
Neutral Protection <sup>1</sup>								X	X	X	X
Contact Wear Indication								X	X	X	X
Incremental Fine Tuning of Settings								X	X	X	X
Selectable Long-Time Delay Bands								X	X	X	X
Power Measurement								X	X	X	X
Power Quality Measurements										X	X
Waveform Capture										X	X

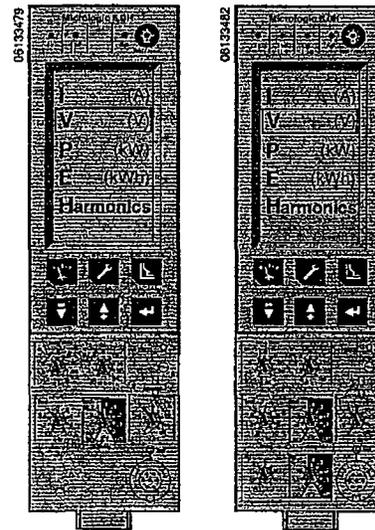
<sup>1</sup> Requires neutral current transformer on three-phase four-wire loads.

<sup>2</sup> Requires the M2C/M6C Programmable Contact Module.

<sup>3</sup> Not available for 2.0A trip unit as upstream devices.



Micrologic 5.0P and 6.0P Trip Units



Micrologic 5.0H and 6.0H Trip Units

**NLI audit report SVR-042181-1 and the supporting Schneider documents are proprietary. These documents are not included in the version of this report that is released to our clients. These documents are available at the NLI facility for review.**

**The Schneider/Square D documents listed below are attachments to the NLI audit report.**

<u>Document #</u>	<u>Title</u>
MQ MDE-E Rev. A	Group Schneider QA Manual
No Document #	Grenoble ISO 9001-2000 ISO Certification for Design and Testing
PAQ 00 H 01 1	AFI Moirans QA Manual
No Document #	Moirans ISO 9001-2001 and ISO 14001-1996 Certificates
PAQ 02 H06 0 00 B	AFI Moirans Receipt Inspection Procedure
No Document #	Montmelian QA Manual, Revision B
No Document #	Montmelian ISO 9001-2001 and ISO14001 -1996 Certificates
No Document #	AMIS ASIC Design Brochure
No Document #	AMI Semiconductor Background, Products, and QA
No Document #	Cadence Design Systems Background and Products
No Document #	Solectron Corporation Background, Products, and QA
60069-001, Rev. A	Mixed Signal ASIC Programming Manual
No Document #	Cadence - System Design and Verification Overview
No Document #	An Introduction to RISC Processors
0600DB9901 8/00	Data Bulletin -- Field Testing and Maintenance Guide for Micrologic Electronic Trip and Thermal-Magnetic Molded Case Circuit Breakers
0603DB0102 8/01	Data Bulletin -- Electronic Trip Insulated Case Circuit Breakers
0613H09902	Micrologic Trip Units – Product Overview'
48049-136-03 02/02	Micrologic A Series Trip Units
48049-137-03 05/02	Micrologic 5.0P and 6.0P Trip Units
48049-183-01 06/01	K669 Full Function Test Kit
Procedure 07, Rev. D	Group Schneider Requirements Definition
Procedure 09, Rev. C	Group Schneider Subcontracting Design Requirements
Procedure 13, Rev. D	Group Schneider Validation of Technical or Design Requirements
Procedure 15, Rev. E	Group Schneider Managing Customer Complaints
Procedure 16, Rev. C	Group Schneider Managing Equipment Returns
Procedure 17, Rev. D	Group Schneider Communication of Product Defects
Procedure 18, Rev. A	Group Schneider Corrective and Preventative Actions
Form PRC 703-1c	Group Schneider Design Review and Production Startup Form
Procedure PAEL-G01	Group Schneider Software Quality Assurance

Procedure PCO-01, Rev. F	Group Schneider Technical and Manufacturing Development Processes
Procedure PCO-03, Rev. B	Group Schneider Purchasing of Inventory Items
Procedure PCO-09, Rev. G	Group Schneider Qualification of Products and Systems
Procedure PCO-10, Rev. D	Group Schneider Project Activities after Product Release
Procedure PCO-11, Rev. E	Group Schneider Transfer of Technical Management after Product Release
Procedure PCO-13, Rev. F	Group Schneider Management of M&TE
Procedure PCO-15, Rev. D	Group Schneider Product Protection Checklist
Procedure PCO-16, Rev. C	Group Schneider Production Planning
Procedure PCO-17, Rev. C	Group Schneider Distribution and Modification of the Production Plan
Procedure PCO-18, Rev. C	Group Schneider Modification of Production Plans
Procedure PCO-19, Rev. D	Record of Proving Test Storage and Distribution of Quality Documents
Procedure PAEL-G01	Group Schneider Software Quality Assurance (Extract)
Test Report PROELA0020	Validation of Micrologic 5.0A Current Measurements w/ NW08
Test Report PROELA0024	Micrologic 2.0A, 3.0A, 5.0A, and 6.0A 1000 Hour Temperature Cycle Test
Test Report PROELA0030	Complete Summary of Micrologic Trip Unit Testing CEI Qualification Testing
No Document #	Group Schneider Index of Activity and Process Instructions and Procedures
PROA_NAA	Group Schneider Specification of the ASIC (Extract)
PROA PROXIMA, Rev. 2.7	Alcatel Specification of the User Specific Integrated Circuit PROA (Extract)
5100513140-B 6/28/01	Failure Modes and Effects Analysis PROXIMA release ELA version (Extract)
A48155	Square D Report - ASIC Verification Testing During Development (Extract)
PR CDC 4230T, Rev. T	Plan for the Four Function Testers PROXIMA (Extract)
R FORVEIL, 2/5/03	Qualification of the Four Function Testers PROXIMA (Extract)
Various Document #s	Micrologic Trip Unit Final Acceptance Tester M&TE Calibration Certificates
Test Report 205490 151a01	Micrologic Trip Unit SN 205490 Factory Post-Assembly Test Results IEC Certificate of Conformity Micrologic Trip Unit 2.0-7.0H w/ Masterpact NW and NT
411_00	IEC Certificate of Conformity Micrologic 5.0A Emissions Test EEC 945 1996-11 F
IEC-60947-2E	Collection Technique No. 149 EMC: Electromagnetic Compatibility
IEC 60947-1	Edition 3.2-2001 Part 1 General Rules
IEC 60947-2	Edition 2.2 2001-11 Part 2 Circuit Breakers
K11-314a-00	Record of Proving Test Micrologic 5.0A w/ NW08 H1
K11-314b-00	Record of Proving Test Micrologic 7.0A w/ NW08 H1
K11-527-00	Record of Proving Test Micrologic 5.0A w/ NW40 BH1
UL and ANSI Certification Test Report for Masterpact NW NW08H1	
UL and ANSI Certification Test Report for Masterpact NW NW08H2	

UL and ANSI Certification Test Report for Masterpact NW NW08L1  
UL and ANSI Certification Test Report for Masterpact NW NW08N1  
UL and ANSI Certification Test Report for Masterpact NW NW16H1  
UL and ANSI Certification Test Report for Masterpact NW NW16H2  
UL and ANSI Certification Test Report for Masterpact NW NW16L1  
UL and ANSI Certification Test Report for Masterpact NW NW16N1  
UL and ANSI Certification Test Report for Masterpact NW NW20H1  
UL and ANSI Certification Test Report for Masterpact NW NW20H2  
UL and ANSI Certification Test Report for Masterpact NW NW20L1  
UL and ANSI Certification Test Report for Masterpact NW NW32H1  
UL and ANSI Certification Test Report for Masterpact NW NW32H2  
UL and ANSI Certification Test Report for Masterpact NW NW32L1  
UL and ANSI Certification Test Report for Masterpact NW NW40H2  
UL and ANSI Certification Test Report for Masterpact NW NW40L1  
UL and ANSI Certification Test Report for Masterpact NW NW50H2  
UL and ANSI Certification Test Report for Masterpact NW NW50L1  
ANSI C37\_90\_Test Report Electromagnetic Compatibility  
Schneider Electric Response to NLI Questions (MS PowerPoint)

## COMMERCIAL GRADE AUDIT REPORT

### Vendors:

Schneider Electric  
Grenoble, France  
Moirans, France  
Montmelian, France

Square D  
Cedar Rapids, IA, USA

Audit Report No.: SVR-042181-01, Revision 1

**Audited Facilities:** Grenoble, France Moirans, France Montmelian, France Cedar Rapids, IA, USA

**Audit Dates:** Various 2-5/2003

### Audit Results:

- Inspection Plan No.: VVP-042181-01 (latest revision)
- Team Member: Mr. Archie C. Bell
- Persons contacted:
  - Mr. Jacques Galla, QC Process Manager - Montmelian, France
  - Mr. Pierre Blanchard, Design Engineer - Grenoble, France
  - Mr. Christian Raymond, Qualification Manager - Grenoble, France
  - Mr. Pierre Miguet, Technical Quality Assurance Manager - Grenoble, France
  - Mr. Charles Yufera, Coordination Manager - Moirans, France
  - Mr. Eric Bettega, Design Engineer - Grenoble, France
  - Mr. Daniel Duc, International Marketing Manager - Grenoble, France
  - Mr. Alan Kuntz, Applications Engineer – Cedar Rapids, IA, USA
  - Mr. Gregg Weiss, Design Engineer – Cedar Rapids, IA, USA

**Audit Performance:** The following activities were performed during this audit.

Interviews with engineering personnel, reviews of testing documents, and analysis of the Micrologic trip unit design documents at Square D's engineering and test facilities in Cedar Rapids, IA. Interviews with the Micrologic trip unit design team and quality assurance representatives, inspection of test facilities, verification of measurement and test equipment calibration, reviews of trip unit design methodology, development documentation, control and testing requirements, and analysis of test results and documentation at Schneider Electric's design and testing facilities in Grenoble, France. Interviews with production and quality control personnel, inspection of trip unit production, testing, and packaging operations, and analysis of assemble methods, test equipment certification, and test reports at Schneider Electric's Micrologic production facilities in Montmelian, France. This is the only facility in the world that assembles the Micrologic trip unit. Interviews with production and quality control personnel, inspection of circuit breaker production, testing, and packaging operations, analysis of receipt, in-process and post-production inspection and test methods, test equipment certification, and documentation of test results at Schneider Electric's Masterpact production facilities in Moirans, France. This is the only facility in the world that assembles the complete Masterpact circuit breaker and its modular components.

**Summary of Results:** Schneider Electric's and Square D's documented and implemented quality assurance programs for development, testing, and manufacturing control of software and hardware complies with NLI QA program requirements.

**NOTE:** See attached **REPORT DATA** for additional information.

**Required Actions:** None.

## REPORT DATA

### A. Background

The Masterpact circuit breaker and Micrologic trip unit design and manufacture are controlled by Schneider Electric and are marketed and supported by four of Schneider Electric's Strategic Business Units – Merlin Gerin, Modicon, Square D, and Telemecanique. The Masterpact circuit breaker and Micrologic trip unit design control and IEC performance testing are performed at Schneider Electric's design and testing facilities in Grenoble, France. Additional testing of the circuit breaker and trip unit was performed at Square D's engineering and test facilities in Cedar Rapids, Iowa. The Masterpact circuit breaker assemblies and components are manufactured and tested at Schneider production and test facilities in Moirans, France. The Micrologic trip units are manufactured and tested at Schneider Electric's production facilities in Montmelian, France. Masterpact circuit breaker IEEE testing and Micrologic trip unit protection function beta testing was performed by Square D's Cedar Rapids, Iowa facility. The NW and NT series circuit breakers are assembled in the United States using the modular components manufactured in Moirans, France. The NW series breakers are assembled in Columbia, South Carolina and the NT series breakers are assembled in Cedar Rapids, Iowa. Final fabrication of the Masterpact circuit breaker in the configurations provided by NLI is performed by Square D Services in West Chester, Ohio.

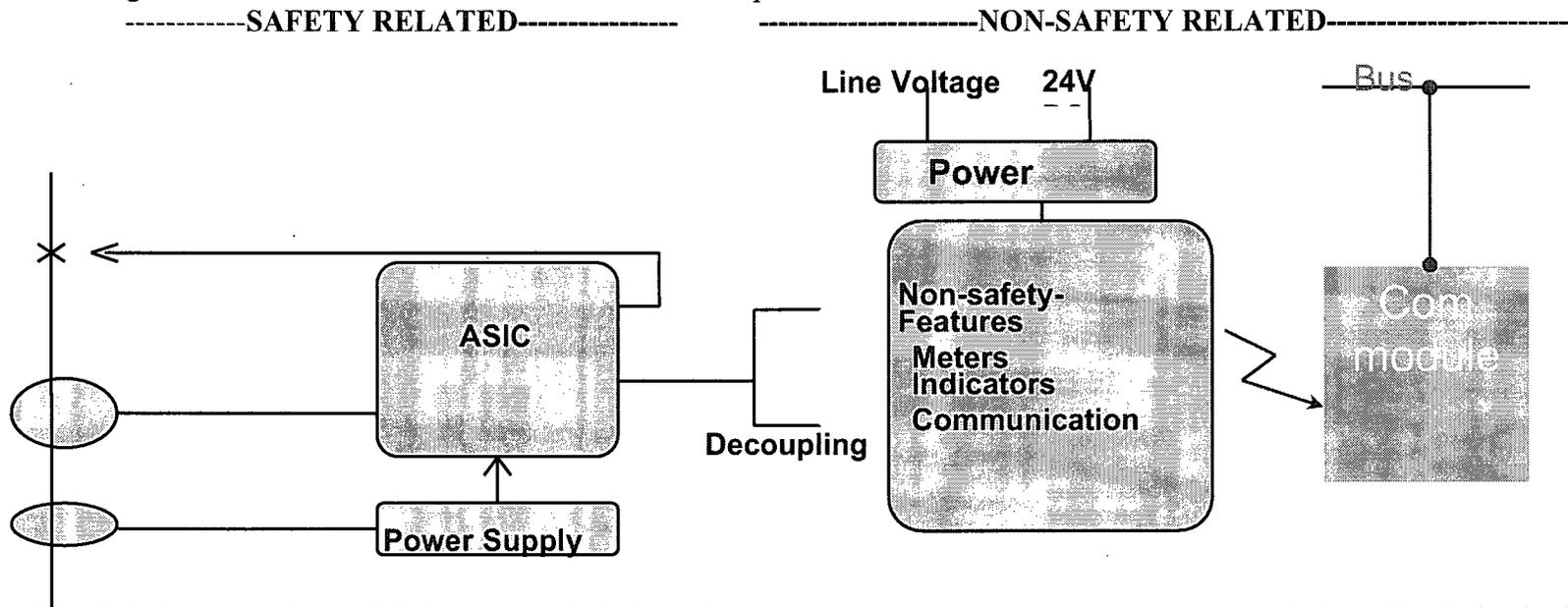
### B. Trip Unit Overview

The Micrologic trip units provide user selectable tripping functions on electronic trip circuit breakers. There are four trip unit versions. All use the identical protection circuitry and programming. The versions are:

- Models 3.0 and 5.0 provide user configurable basic circuit protection: long-time, instantaneous and optional short-time adjustments with no metering or communications functions.
- Models 3.0A, 5.0A, and 6.0A provide user configurable basic circuit protection plus integrated ammeter and phase loading bar graph metering functions, LED trip indication, zone selective interlocking, optional ground-fault protection, and MODBUS communications.
- Models 5.0P and 6.0P provide user configurable basic circuit protection and "A-Model" features plus advanced relay protection, inverse definite minimum time lag (IdmtL) long-time delay, ground-fault alarm and MODBUS communications.
- Models 5.0H and 6.0H provide user configurable basic circuit protection and "P-Model" features plus enhanced monitoring and metering, power quality measurements, and waveform capture.

The Micrologic trip unit architecture is divided into two distinct substructures or circuits. The Application Specific Integrated Circuit, ASIC, provides core protection functions using both digital and analog circuitry. The digital portion of the ASIC supports user selectable safety-related circuit breaker protection functions. The analog portion provides over temperature (trip unit) and instantaneous high current protection. Non-safety related activities, including metering, trip indication, and ASIC failure indication, are accomplished with HC11-series or HC16-series (depending on the trip unit model selected) microprocessor controlled circuitry. The non-safety circuitry is coupled to the ASIC through a serial interface (SIF) data line only. The ASIC has no interface with the non-safety related microprocessor other than providing information for the metering and indicator functions. The ASIC will perform all safety-related protection functions with the non-safety related microprocessor removed from the trip unit. This is evident because the most basic of the Micrologic trip units, the 3.0 and 5.0, perform all of the core protection

functions without any on-board microprocessor or metering and indicator functions. The following is a block diagram of a typical trip unit that has metering and/or indicator functions and communications capabilities:



The digital portion of the ASIC is a hard-coded, deterministic, continuous loop over-current protection device. The design is simplistic in nature and has been designed for high reliability. The ASIC contains two ROM devices – MCROM 32-bit and THROM 16-bit. The MCROM is a masked program device that controls the sequence of activity of the digital portion of the ASIC and provides instructions for the arithmetic manipulation of measured current data and user selected protection variables. The THROM is also a masked program device that provides the constants and threshold information that are used during the comparison of the measured current data to the user selected tripping criteria. Decisions are made by hard-logic methodology. No conditional instructions, jumps, calls, or interrupt functions are used. There are no watchdog functions or conditional branching in the ASIC.

User selectable trip functions are chosen by rotary switch position selection. The number of rotary switches found on a Micrologic trip unit is model specific. For example, the Model 3.0 series has three rotary switches to select: long-time pick up ( $I_r$ ); long-time delay ( $t_r$ ); and instantaneous pickup ( $I_i$ ). The Model 6.0 series has seven rotary switches to select: long-time pick up ( $I_r$ ); long-time delay ( $t_r$ ); short-time pick up ( $I_{sd}$ ); short-time delay ( $T_{sd}$ ); instantaneous pickup ( $I_i$ ); ground-fault pick up ( $I_g$ ); and ground-fault delay ( $t_g$ ). The rotary switch position configures its portion of the hard-wired decision logic by means of and-or gates. Regardless of model, each rotary switch has its own and-or gate matrix. Each matrix is independent but all are contained in the same silicon device. Even though each and-or gate is logically independent, there are some dependent relationships; those relationships are: long-time pick up ( $I_r$ ) and long-time delay ( $t_r$ ); short-time pick up ( $I_{sd}$ ) and short-time delay ( $T_{sd}$ ); and ground-fault pick up ( $I_g$ ); and ground-fault delay ( $t_g$ ).

### C. ASIC Design Overview



**CRITICAL  
CHARACTERISTIC**

**ACCEPTANCE  
CRITERIA**

**RESULTS**

**Quality Assurance  
Program**

Quality Assurance program that controlled the development of the software/hardware.

The software and hardware were developed, manufactured, and tested under the controls of the Schneider Electric and Square D Quality Assurance programs.

Software and hardware design, manufacturing and testing for the trip units are controlled by a documented quality assurance programs. The design, verification, configuration control, manufacturing, and post-production testing of the Masterpact circuit breaker and the Micrologic trip units are controlled by the Schneider Electric quality system. Independent Quality Assurance organizations at the Grenoble, *Grenoble ISO 9001-2000 ISO Certification for Design and Testing*, Moirans, *Moirans ISO 9001-2001 and ISO 14001-1996 Certificates*, and Montmelian, *Montmelian ISO 9001-2001 and ISO14001 -1996 Certificates*, France facilities provide oversight over the design, manufacturing and testing activities.

A documented quality assurance program controls design testing performed at the Square D facility in Cedar Rapids, Iowa. An independent Quality Assurance organization provides oversight of testing activities.

**Verified by inspection, document review, and personnel interview during this audit. SATISFACTORY.**

QA program compliance

Standards cited in QA Program manual and implementing procedures correlate with design, manufacture, and testing of the Masterpact circuit breaker and Micrologic trip units.

Schneider Electric's Grenoble, Moirans, and Montmelian facilities documented QA programs *MQ MDE-E Rev. A Group Schneider QA Manual, PAQ 00 H 01 1 AFI Moirans QA Manual, and Montmelian QA Manual, Revision B* cite the ISO 9001-2000 and ISO 14001 standards as the guideline for determining quality system requirements. Where applicable software design and development microcode design and development activities comply with the requirements of IEC 1131-2-1992, IEC-1131-3-1992, and IEC 1131-4-1995. Where applicable, development and final product testing activities of the integrated trip unit and circuit breaker suite comply with the requirements of IEC 60947-1, IEC 60947-2, NF EN 60947-1, and NF EN 60947-2.

The documented QA program at Square D's Testing Division in Cedar Rapids, Iowa documented QA program cite the ISO 9001-2000 standard as the guideline for determining quality system requirements. Where applicable, product testing activities of the integrated trip unit and circuit breaker suite comply with the requirements of UL 1066, ANSI C37.50, and C37.13.

Both Schneider Electric's and Square D's M&TE maintenance and calibration program documents cite ISO 10012-1 as the guideline for determining quality system requirements.

**Verified by inspection, document review, and personnel interview during this audit. SATISFACTORY.**

QA Program documentation

Hierarchy of QA Program implementing documentation identifies design, manufacture, and testing requirements

Both Schneider Electric's and Square D's quality systems are controlled by hierarchical documentation matrices. Quality program commitments are documented in published QA Program manuals. Quality program implementing procedures are typically grouped by discipline of organizational function such as design, manufacture, inspection and test, material control, purchasing, quality control, and quality assurance. Product or task specific instructions provide specific requirements for work accomplishment - *Group Schneider Index of Activity and Process Instructions and Procedures*.

**Verified by inspection, document review, and personnel interview during this audit. SATISFACTORY.**

Subtier supplier controls

Acceptance methodology complies with ISO 2001-2000 requirements.

Schneider Electric's subtier suppliers are approved on the basis of audits, historical performance, and periodic testing. These activities are procedurally controlled and are performed at the Schneider Electric Grenoble facility.

Schneider Electric uses two primary subtier suppliers to support development and manufacture of the Micrologic trip unit.

Alcatel, now AMI Semiconductor <http://www.amis.com> – (AMIS), wrote the ASIC implementing specification, constructed the prototype test versions of the ASIC, and now manufactures the ASIC semiconductor device, which includes masking the code for the MCROM and THROM devices. AMIS provides the completed, tested silicon devices to Solectron Corporation <http://www.solectron.com>, where the Micrologic printed circuit boards were designed, constructed for prototype testing, and are now manufactured. Solectron Corporation provides the completed, tested printed circuit board assemblies to Schneider Electric's assembly plant in Montmelian, France where the Micrologic trip units are fully assembled and tested.

AMI Semiconductor, *AMI Semiconductor Background, Products, and QA*, and Solectron, *Solectron Corporation Background, Products, and QA*, are both have ISO 9001-2000 compliant quality assurance programs and are certified suppliers of Schneider Electric.

Products provided by certified suppliers are accepted on the basis of Certificates of Test and Conformance provided with the item, batch, or lot.

**Verified by inspection, document review, and personnel interview during this audit. SATISFACTORY.**

**CRITICAL  
CHARACTERISTIC**

**ACCEPTANCE  
CRITERIA**

**RESULTS**

**Software Lifecycle**

Microcode design development, testing, maintenance, and retirement activities comply with the intent of a software lifecycle management scheme as describe in IEEE Standard 1074-1995.

**Verified by procedure reviews, digital file inspections, personnel interviews, and test documentation reviews during this audit. SATISFACTORY.**

Software specification/software requirements.

Software specification documents the detailed software requirements.

The basis of the design of the ASIC is based on the previous generation of the Masterpact ASIC design (NSF and NSJ series circuit breakers), whose core protection functions were accomplished through the use of 350 components. The present ASIC design performs the same core protection functions using 53 components. All of the microcode for the present ASIC digital protection design is new, though the function of the trip unit is conceptually very similar to the previous design.

The current revisions of the design specification documents are located at Square D in Cedar Rapids, Iowa. These documents are: Group Schneider, "*Specification of the ASIC PROA\_NAA*", a 195-page document and Alcatel Mietec, "*Specification of the User Specific Integrated Circuit PROA*", a 50-page document. The Group Schneider specification fully documents both the hardware and software requirements for the ASIC. The requirements for the digital portion of the ASIC include, but not limited to: the methodology for measuring and converting voltage and current levels; the sequencing of calculations; microprocessor properties; and the sequencing of the start-up and run routines. Alcatel Mietec, a division of AMI Semiconductor, is the designer, developer, and manufacturer of the ASIC silicon-based microcircuit chip. Alcatel Mietec developed the ASIC manufacturing specification based upon the Schneider Group's ASIC design specification. The most recent version of the Alcatel specification is revision 2.7 dated 1/5/1999.

**Verified by specification document review, and personnel interviews during this audit. SATISFACTORY.**

Procedural controls used during software development.

Software development controlled by Schneider procedures. Document the procedures used and evaluate process.

Schneider Electric designers chose to manage the digital design and microcode development and testing as a hardware project, which is consistent with the design and validation toolsets provided by ASIC manufacturing houses such as AMI Semiconductor (AMIS). Micrologic design team management and quality assurance activities comply with the intent, where applicable, of the following IEC documents: 1131-1-1992; 1131-2-1992; 1131-3-1992; and 1131-4-1995 for micro-controllers, which roughly correlate to the requirements of IEEE Standards 830-93, 603-91, 828-90, 1042-87, 1008-87, and 1042-87. The titles and content follow European format and in some cases requirements are combined in a single document.

Activities at the Schneider Group design and development facility are controlled by documented procedures and implementation forms. The control and revision of theses procedures is in Grenoble, France. The upper-tier implementing procedures include: *Procedure 07, Rev. D, Requirements Definition; Procedure 09, Rev. C,*

*Subcontracting Design Requirements; Procedure 13, Rev. D, Validation of Technical or Design Requirements; Form PRC 703-1c, Project Startup and Progress Tracking; Procedure PAEL-G01, Software Quality Assurance; Procedure PCO-09, Rev. G, Qualification of Products and Systems; Procedure PCO-19, Rev. D, Storage and Distribution of Quality Documents.*

**Available documents, interviews with the Schneider Electric design team in France, and the demonstrated quality of the deployed trip unit product (no microcode revisions since product rollout) reflect that the Schneider Group design and development activities were accomplished by a professional engineering staff extremely familiar with trip unit design and comfortable in implementing a structured, rigorous approach toward project management within the constraints of the complexity of the overall project.**

**SATISFACTORY.**

Failure Modes & Effects Analysis

Failure Modes & Effects Analysis performed and used during software development.

The Schneider Electric design team in Grenoble developed a FEMA analysis, *5100513140-B 6/28/01 Failure Modes and Effects Analysis PROXIMA release ELA version*, during the initial stages of the writing of the “*Specification of the ASIC PROA\_NAA*”. The FEMA analysis was refined upon receipt of the Alcatel “*Specification of the User Specific Integrated Circuit PROA*”. The completed study contains:

- An external functional analysis methodology showing the ties between the studied item and its environment in order to determine a failure relationship. The methodology used is M.I.S.M.E (Method of Systematic Inventory of the Surrounding Environment). Note: This technique was used as part of the functional and safety requirements analysis performed by the European Organization for Nuclear Research for the CERN Safety Alarm Monitoring System.
- An internal functional analysis by functional block diagram in accordance with MIL-HDBK-217F.
- A dysfunctional analysis showing the consequences of a failure on the operability of the trip unit.
- A quantification of the rate of global failure of the ELA (x.0A trip units) devices using compilations of reliability data for two temperatures 40 and 100°C in both stationary and mobile applications.
- An AMDEC quantified for a temperature of 40°C in a stationary environment ” Note: AMDEC is a technique used for the development of products and processes in order to reduce the risk of failures and to document the actions undertaken. It is part of the QS 9000 ‘whole quality system’ methodology.
- The study concludes that the occurrence of an ASIC failure is  $3.11 \text{ E-6 h}^{-1}$  @ 40°C and  $5.67 \text{ E-6 h}^{-1}$  @ 100°C.

There are two creditable failure modes that impact ASIC operation:

- Loss of clock (gate pulse), which results in a loss of the ASIC’s digital protection functions.
- Loss of power, which results in a loss of all ASIC protection functions.

Neither failure affects circuit breaker operation. If the circuit breaker contacts are closed when a trip unit (ASIC) failure occurs, the contacts will remain closed.

When the digital portion of the ASIC’s protection functions are lost, all user selectable protection functions are lost; however, protection functions are retained for detected high temperature condition and detected current in excess of the circuit breaker’s interrupt rating.

When all ASIC protection functions are lost, no protection functions are retained. This condition is consistent with all electronic trip device designs – analog or digital.

**Verified by FEMA analysis review and personnel interviews during this audit. SATISFACTORY.**

Development and testing approach.

Schneider developed and tested the software in small function based blocks of code. Development and testing documented.

The Micrologic trip unit was designed by the Schneider Group design team located in Grenoble, France using tool sets from Cadence Design Systems <http://www.cadence.com>, *Cadence Design Systems Background and Products*. The design and development process occurred during 1994-1998. A Schneider Group strategic business unit – Square D, performed beta testing of the ASIC design. Flow charts that are contained in the extracts of “Specification of the ASIC PROA\_NAA” depict the design, development, and verification processes.

Code was written in functional blocks or modules, 60069-001, Rev. A *Mixed Signal ASIC Programming Manual*, as documented in specifications “*Specification of the ASIC PROA\_NAA*” and “*Specification of the User Specific Integrated Circuit PROA*”. Development and testing activities included: simulations, fourier analysis, reliability analysis, software testing, hardware testing, and software-hardware integration testing.

ASIC design requirements were documented using Verilog simulation toolsets specifically designed by Cadence, *Cadence - System Design and Verification Overview*, and AMIS, *AMIS ASIC Design Brochure*, for ASIC applications. Data flow was written in a modular, overlay fashion. Design notes are included with the data flow to allow review by a cognizant peer. Design requirements are safeguarded with a tool similar to source safe, which date stamps the file each time that it is saved/closed.

**Review of available documents, interviews performed during the audit, and electronic files inspected at the Schneider Group design and development facility reflect a structured, rigorous approach toward requirements definition, revision control of project related documents, development of test plans, and documentation of developmental testing results. SATISFACTORY.**

Independence of software development and testing.

Independent personnel used.

During the design and development phase, the ASIC design requirements were documented using Verilog design and simulation toolsets specifically designed by Cadence for ASIC applications and in hardcopy design specifications. These activities were procedurally controlled.

The threshold and constant data contained in the THROM was developed in Grenoble, France using a “C” language program that generated theoretically ideal data, which was documented on a Microsoft Excel spreadsheet. Testing in Cedar Rapids, IA validated the THROM data. Correction of the code was performed in Grenoble, France and implemented through a THROM revision. The MCROM machine level code requirements were written in Grenoble, France. The requirements were realized in the silicon microcircuit fabricated by Alcatel, now AMI Semiconductor (AMIS). Black box (input/output) testing only was performed during development due to the simplistic nature of the ASIC architecture. The trip unit was tested by Square D in Cedar Rapids, IA, *A48155 Square D Report - ASIC Verification Testing During Development (Extract)*, to verify that the deterministic instruction loop correctly sequenced the THROM data and the user input digital words. This iterative process

continued until the design requirements were met.

**Available documents, completed interviews, and inspection of the completed tool set electronic files during this audit demonstrate that the Schneider Group design and development activities were accomplished by a professional engineering staff extremely familiar with trip unit design and comfortable in implementing a structured, rigorous approach toward project management within the constraints of the complexity of the overall project. SATISFACTORY.**

Integrated hardware/software testing.

Integrated testing of the hardware/software system was performed.

During prototyping, the designer performed simulations. Integration testing was performed by second party or peer reviewers. This approach is consistent with the intent of IEEE Standards 1008-1987 and 829-1983.

During product development, the integrated circuit breaker and trip unit suite was tested to verify conformance to the design requirements and the IEC standards at the Schneider Electric test facility located in Grenoble, France. These tests included, but were not limited to: *Test Report PROELA0020, Validation of Micrologic 5.0A Current Measurements w/ NW08; Test Report PROELA0024, Micrologic 2.0A, 3.0A, 5.0A, and 6.0A 1000 Hour Temperature Cycle Test; Test Report PROELA0030, Complete Summary of Micrologic Trip Unit Testing IEC Qualification Testing.* Additional testing was performed at the Square D facility to verify conformance to the design requirements and the IEEE standards

The final versions of the masked program device code (located in the MCROM) and the constants and thresholds (located in the THROM) were finalized based on testing, which was performed and documented in accordance with controlled procedures and plans. Report of these activities include, but are no limited to: *K11-314a-00, Record of Proving Test Micrologic 5.0A w/ NW08 H1; K11-314b-00, Record of Proving Test Micrologic 7.0A w/ NW08 H1; and K11-527-00, Record of Proving Test Micrologic 5.0A w/ NW40 BH1.*

After product rollout, Schneider Electric continues to test the integrated circuit breaker and trip unit suites in thee test facility located in Grenoble, France in order to verify product consistency. Certification of these tests included, but were not limited to: *151a01, IEC Certificate of Conformity Micrologic Trip Unit 2.0–7.0H w/ Masterpact NW and NT and 411\_00, IEC Certificate of Conformity Micrologic 5.0A Emissions Test EEC 945 1996-11.*

**Verified by inspection, witnessing of testing, review of test documentation, and personnel interview during this audit. SATISFACTORY.**

Product operating history.

Installed units operating properly. Specify number of operating units, time in service, and number and types of identified problems.

There has been no revision of either the THROM or MCROM microcode or the ASIC hardware product rollout in 1998. Over 50,000 trip units deployed worldwide, 16,000-17,000 units deployed in the USA. They have been shipping the same microcode versions since product rollout.

**Verified by document review, personnel interview, and electronic file review during this audit. SATISFACTORY.**

Error handling.

1. Code errors are identified, documented, evaluated, and reported in a controlled manner by Schneider.
2. Mechanism for reporting and evaluating user reported problems.

Since production release, there have been no microcode updates preformed. Presently, no microcode revision is planned. Should a product enhancement be made to add additional capability, the THROM constants and thresholds may be changed, but no MCROM microcode revisions would be considered necessary. With any microcode revision, full configuration control measures would be taken. Testing would include regression testing, as applicable, during the integration phase.

A mechanism is established for customer reported errors to be processed and resolved in the USA through the Square D customer service program, which receives updates from the world wide Schneider Electronics network. Upon receipt, a customer complaint is documented in a worldwide product quality database. Locally developed decisions are reviewed and validated at Schneider Electric corporate design and quality assurance. Solutions outside of local capabilities are submitted to Schneider Electric corporate for resolution. Once a solution is implemented and verified, the defect and its resolution are made available to all Schneider Electric SBU service centers for distribution.

**Verified by procedure reviews, personnel interviews, and electronic file reviews during this audit. SATISFACTORY.**

Software updates and service bulletins.

Schneider has a formal process to alert customers concerning software updates and provides service bulletins.

Management, resolution, and communication of customer reported defects, hardware upgrades, and software revisions are controlled in accordance with Schneider Electric procedures: *Procedure 15, Rev. E, Managing Customer Complaints; Procedure 16, Rev. C, Managing Equipment Returns; Procedure 17, Rev. D, Communication of Product Defects; and Procedure 18, Rev. A, Corrective and Preventative Actions*

**Verified by procedure reviews, personnel interviews, and electronic file reviews during this audit. SATISFACTORY.**

**CRITICAL  
CHARACTERISTIC**

**ACCEPTANCE  
CRITERIA**

**RESULTS**

**Configuration  
Control**

Revision control.

Revision control used on silicon devices.

Configuration management, both revision control and revision verification, is accomplished using the VERILOG tool set. Configuration management requirements are documented in Schneider Electric controlled procedures. The configuration management activities comply, as applicable, with the intent of IEC 1131-1-1992, IEC 1131-4-1995, and IEEE Std. 1042-1987. Each revision has a unique identifier and is traceable to the design documents.

After product rollout engineering oversight was transferred to sustaining/ product improvement organization. This transfer of responsibility was accomplished in accordance with *Procedure PCO-11, Rev. E, Transfer of Technical Management after Product Release*. Activities after product release are performed in accordance with *Procedure PCO-10, Rev. E, Project Activities after Product Release*.

To date, there have been no revisions of the MCROM or THROM microcode. The requirements for both the MCROM and THROM microcode is contained in "*Specification of the User Specific Integrated Circuit PROA,*" *Revision 2.7*, dated 1/5/99. Should microcode revisions be required in the future due to product enhancement or problems identified in the field, the development, testing, and deployment will be controlled by the same procedures and written with the same tool sets as the original release version.

**Verified by procedure and specification reviews and personnel interviews during this audit.  
SATISFACTORY.**

Manufacturing controls of code.

Controls to assure correct code installed on each unit.

Traceability between development and production code is documented.

Schneider Electric's manufacturing configuration control is a composite of vendor and purchasing control, production planning, material control, manufacturing control, and quality control.

- The requirements for procurement are identified in *Procedure PCO-03, Rev. B, Purchasing of Inventory Items*. Items are purchased from two levels of approved suppliers. Certified supplier's products are accepted without additional testing based upon a defined grading system. Products from uncertified suppliers are subject to acceptance testing, which are performed in accordance with documented plans. Incoming certified products are differentiated from non-certified products by a two-alpha prefix on the item's part number. A Certificate of Test or Certificate of Conformance from the supplier accompanies each certified product shipment.

**Implementation was verified by inspection, procedure reviews, and personnel interviews at Schneider Group's assembly plant in Montmelian, France. SATISFACTORY.**

- Production planning is accomplished in accordance with the following procedures: *Form PRC 703-1c, Design Review and Production Startup, Procedure PCO-18, Rev. C, Production Planning, Procedure PCO-19, Rev. D, Modification of Production Plans, and Procedure PCO-17, Rev. C, Distribution Modification of the Production Plan*. Specific requirements for material, manufacturing, and quality control

are also identified in controlled documents at Schneider Group's assembly plant in Montmelian, France. **Implementation was verified by inspection, procedure reviews, and personnel interviews at Schneider Group's assembly plant in Montmelian, France. SATISFACTORY.**

- Implementation of vendor and purchasing control, production planning, material control, manufacturing control, and quality control practices are accomplished by document review, inspection, and interview of cognizant manufacturing and quality personnel at Schneider Group's assembly plant in Montmelian, France.

**The result of these evaluation activities reflect a well trained and motivated workforce whose activities reflect compliance with documented requirements, excellent material and manufacturing work practices, and an active culture of quality improvement. SATISFACTORY.**

- Automated testing of the completed trip unit assembly verifies the correct hardware and software configuration of the assembly, *Test Report 205490, Micrologic Trip Unit SN 205490 Factory Post-Assembly Test Results*. Automated testing is performed in accordance with Schneider Electric document *PR CDC 4230T, Rev. T, Plan for the Four Function Testers PROXIMA, Revision T*. The automated testing is performed using software controlled M&TE, *Micrologic Trip Unit Final Acceptance Tester M&TE Calibration Certificates*. The verification and validation activities for the testing software is documented in Schneider Electric document *R FORVEIL, 2/5/03, Qualification of the Four Function Testers PROXIMA*. The qualification testing included regression and black box testing.

**Verified by specification document reviews and personnel interviews during this audit. SATISFACTORY.**

Regression testing or evaluations.

Regression testing or evaluations performed when code is revised.

Regression testing is not applicable to this product due the small amount of code written. The THROM contains all thresholds and constants for the calculation of the trip unit protection values. The THROM contains 4 Kbytes of 16-bit digital words. The MCROM contains the microcode which sequence, the digital portion of the ASIC's execution of the overload protection activities. The MCROM contains 2 Kbytes of 32-bit machine language code. Should microcode revisions be required in the future due to product enhancement or problems identified in the field, the testing will be controlled by the same procedures and written with the same tool sets as the original release version.

Micrologic trip unit developmental, functional, qualification, and manufacturing testing is performed in accordance with written plans that identify acceptance criteria, using calibrated Measurement and Testing Equipment, and the results are documented in written reports.

The following testing information has been reviewed: *Test Report PROELA0020, Validation of Micrologic 5.0A Current Measurements; Test Report PROELA0024, Aging Tests Applicable to Micrologic 2.0A, 3.0A, 5.0A, and 6.0A; Test Report A48155, ASIC Developmental Testing, Test Report 205490, Micrologic 5.0A Post Production Testing, Test Report -- EMC per ANSI/IEEE C37.90, Test Report -- Multiple Power Circuit Breaker Frames per UL 1066, ANSI C37.50 and C37.13, EMC per IEC 60947-2 Annex F.*

**Verified by test report reviews, project document inspection, and personnel interviews during this audit. SATISFACTORY.**

**CRITICAL  
CHARACTERISTIC**

**ACCEPTANCE  
CRITERIA**

**RESULTS**

**Software/Hardware**

Data storage.

Per Schneider design specifications.

Data storage in the ASIC is in the form of digital words that are stored in dedicated addresses within a 256x32 RAM in the ASIC.

**Verified by specification document reviews and personnel interviews during this audit. SATISFACTORY.**

Signal conditioning and logic functions

Per Schneider design specifications.

Signal conditioning in the ASIC is limited to analog to digital conversion of AC voltage and current values. Analog voltage values are determined by the use of a fixed value resistance bridge located in the ASIC. Analog current values are determined from current transformers. The analog values are converted to digital words by a silicon-based A to D converter.

Logic functions in the ASIC are limited to hard-wired decisions on the form of and-or gates. There are 6583 and-or gates in the ASIC.

**Verified by specification document reviews, printed circuit board inspections, and personnel interviews during this audit. SATISFACTORY.**

System response time.

Per Schneider design specifications.

A complete protection cycle occurs every 544 microseconds. Poles are evaluated in the sequence: O, A, B, C. The cycle for each pole is 128 microseconds. The decision to trip, or not is made during the final 32 microseconds.

The response time from input to output with change of state:

- Digital: 544 microseconds + user selected trip delay time + 20 milliseconds.
- Analog: 1 microsecond + 20 milliseconds.

**Verified by specification document review and personnel interviews during this audit. SATISFACTORY.**

Remote alarms and indications.

The communication features are not considered safety related and will not be connected in the plant.

There is one failure alarm, Ap, which is a LED display on the trip unit itself. The trip unit designers consider this display as a non-critical for information only output. The circuit breaker will not open if the ASIC fails. This is a deliberate design consideration that provides the operator an opportunity to make the decision as to the appropriateness of interrupting power by opening the circuit breaker. The failure alarm light is activated through a hard-logic decision matrix, which creates a digital word that is read by the non-safety related microcontroller. The non-safety related microcontroller subsequently activates the Ap LED in accordance with its programmed instructions.

Local indication is considered non-safety

There are no safety-related digital communications outside of the ASIC associated with the Micrologic trip unit's performance of its trip functions. The status of the circuit breaker's contacts (OPEN or CLOSED) is communicated by an analog signal sent via auxiliary switch contacts on the circuit breaker itself. These are electrically and

related. physically independent of the trip unit.

There are no safety-related input or output displays or alarms. The Ir trip indicator LED, Isd/Ii trip indicator LED, and Ap self-protection indicator LED are considered by the trip unit designers as non-critical, for information only outputs.

**Verified by specification document reviews, witness of trip unit post-production testing, and personnel interviews during this audit. SATISFACTORY.**

Watchdog timer. Per Schneider design.

There are no hardware or software watchdog timers in the digital portion of the ASIC, *Schneider Electric Response to NLI Questions*.

**Verified by specification document reviews and personnel interviews during this audit. SATISFACTORY.**

Timing and clock control. Per Schneider design.

A 2.0 MHz clock drives the ASIC microprocessor. A crystal oscillator controls the clock frequency. The sequence of events performed by the microprocessor is dictated by the masked code set located in the MCROM. A complete protection cycle occurs every 544 microseconds. Poles are evaluated in the sequence: O, A, B, C. The cycle for each pole is 128 microseconds. The decision to trip, or not is made during the final 32 microseconds.

**Verified by specification document reviews and personnel interviews during this audit. SATISFACTORY.**

Output Alarms Per Schneider design.

There is one failure alarm, Ap, which is a LED display on the trip unit itself. The trip unit designers consider this display as a non-critical for information only output. The circuit breaker will not open if the ASIC fails. This is a deliberate design consideration that provides the operator an opportunity to make the decision as to the appropriateness of interrupting power by opening the circuit breaker. The failure alarm light is activated through a hard-logic decision matrix, which creates a digital word that is read by the non-safety related microcontroller. The microcontroller subsequently activates the Ap LED in accordance with its programmed instructions.

**Verified by specification document review, trip unit developmental test path note inspection, and personnel interviews during this audit. SATISFACTORY.**

Features that could impact operation. There are no features that could interrupt operation (interruptions, diagnostics, manual inputs, non-essential application programs,

No conditional instructions, jumps, branching, calls, of interrupt functions are used in the ASIC's microcode instruction set, *Schneider Electric Response to NLI Questions*.

There is no non-essential or unused code in the ASIC's microcode instruction set, *Schneider Electric Response to NLI Questions*.

There is no provision in the Micrologic trip unit design for manual inputs or data modification.

**Verified by specification document reviews, FEMA analysis inspection, and personnel interview during this audit. SATISFACTORY.**

unauthorized programs or data modifications).

Testing may be performed using a full function test kit by injecting a test current directly into the trip unit through a receptacle on the trip unit. This testing may be performed when the circuit breaker contacts are open or closed. However, the circuit breaker contacts should not be passing current because the test kit secondary current inputs override the current measurement activity of the ASIC, *48049-183-01 06/01, K669 Full Function Test Kit*.

The Micrologic trip unit cannot be replaced when the circuit breaker is closed. The trip unit's long-time rating plug may be replaced when the circuit breaker is closed. NOTE: If the long-time rating plug is removed when the circuit breaker is closed, the overload protection defaults to 40% of the circuit breaker's rating. The time delay remains at user selected levels, *48049-183-01 06/01, K669 Full Function Test Kit*.

**Verified by user manual reviews and personnel interview during this audit. SATISFACTORY.**

Security

The base program is on the ASIC chip and cannot be field modified.

There is no provision or capability to modify, revise, or alter the microcode information contained in the ASIC. The ASIC contains two ROM devices – MCROM 32-bit and THROM 16-bit. The MCROM is a masked program device that controls the sequence of activity of the digital portion of the ASIC and provides instructions for the arithmetic manipulation of measured current data and user selected protection variables. The THROM is also a masked program device that provides the constants and threshold information that are used during the comparison of the measured current data to the user selected tripping criteria, *Schneider Electric Response to NLI Questions*.

**Verified by specification document reviews and personnel interviews during this audit. SATISFACTORY.**

Year 2000 compliance.

Units recognize dates beyond 12/31/99 correctly.

The ASIC does not use or output information that contains day, date, year, or time data, *Schneider Electric Response to NLI Questions*.

**Verified by specification document reviews and personnel interviews during this audit. SATISFACTORY.**

Processor restart and initialization.

Following removal of power, the programmer maintains the settings.

The ASIC startup or restart sequence completes 384 microseconds after the trip unit is powered. The trip unit is powered when the circuit breaker contacts are closed. If power to the circuit breaker contacts is lost, the trip unit will not function unless the user has chosen to provide auxiliary power through the external power supply connector.

When power is restored, the MCROM microcode initiates the ASIC digital protection startup routine. The ASIC begins its digital protection activities within 3 milliseconds of power restoration. The analog protection of the ASIC begins its protection activities within 1 microsecond upon the restoration of power.

There is no loss of the user configurable L, S, I, G functions because they are restored during the startup or restart process. During the 384 microseconds start sequence the digital words created by the interface of the rotary switch positions and the state of the and-or gates are restored. All other information to perform the safety-related function of the ASIC is contained in the MCROM and THROM.

**Verified by specification document review, trip unit developmental test path note inspection, and personnel interviews during this audit. SATISFACTORY.**

Data validity checks      The system contains logic to perform checks of the validity of intermediate results.

There is no input range checking provision or data validity checks during operation. During the start sequence diagnostics activities are limited to verification that the user configurable L, S, I, G are restored to the appropriate RAM addresses. During the run sequence the availability of voltage and current data at the appropriate RAM addresses is confirmed.

**Verified by specification document review, trip unit developmental test path note inspection, trip unit post-production test report review, and personnel interviews during this audit. SATISFACTORY.**

User configurable input values      The user inputs are hard wired switches.

The only user inputs to the ASIC are by rotary switch position selection. Each rotary switch has it's own and-or gate matrix that creates a digital word, which identifies a selected trip condition characteristic. The design prevents invalid of out of range parameter inputs.

**Verified by user specification document reviews, user manual reviews, and personnel interview during this audit. SATISFACTORY.**

Loss of input instruments      Trip unit responds to loss of CT signal per Schneider design.

Analog current values are determined from current transformers. By the nature of the design, the detection of current is highly reliable; however, if there is a winding-to-winding short in the CT, the trip unit would sense an over-current condition and trip the breaker. An open CT winding would be detected by x.0 H-series model trip units, which would initiate a trip action if the out-of-phase condition detection were selected. NOTE: Due to the inherent ruggedness of CT construction, an open CT winding in not considered a creditable failure mechanism.

**Verified by specification document review and personnel interviews during this audit. SATISFACTORY.**

Diagnostics      The programming is deterministic and diagnostics are limited

The digital portion of the ASIC is a hard-coded, deterministic, continuous loop over-current protection device. The design is simplistic in nature and has been designed for high reliability. By design the ASIC start up diagnostic is limited verification of the presence of clock pulses, *Schneider Electric Response to NLI Questions*.

**Verified by specification document review and personnel interviews during this audit. SATISFACTORY.**

Switch settings

The rotary switches used to set the user configurable trip points operate per Schneider Electric design.

User selectable trip functions are chosen by rotary switch position selection. The number of rotary switches found on a Micrologic trip unit is model specific. The rotary switch position configures it's portion of the hard-wired decision logic by means of and-or gates. Regardless of model, each rotary switch has it's own and-or gate matrix. Each matrix is independent but all are contained in the same silicon device.

**Verified by specification document review, Square D developmental test report inspection, trip unit post-production test report review, and personnel interviews during this audit. SATISFACTORY.**

**CRITICAL CHARACTERISTIC**

**ACCEPTANCE CRITERIA**

**RESULTS**

**Programmer specific hardware/software**

Trip unit operation on Masterpact NT and NW breakers.

Programmer mounts and interfaces properly with the Masterpact NT and NW breakers, including physical mounting, wiring, CT interface, ratings plug interface, and flux shifter interface.

Proper trip unit operation and fit-up on Masterpact NT and NW breakers was verified during IEC and ANSI testing performed by Schneider Electric and Square D, *ANSI Certification Test Reports for Masterpact NW08H1, NW08H2, NW08L1, NW08N1, NW16H1, NW16H2, NW16L1, NW16N1, NW20H1, NW20H2, NW20L1, NW32H1, NW32H2, NW32L1, NW40H2, NW40L1, NW50H2, and NW50L1.*

**Verified by IEC and ANSI test report reviews and personnel interviews during this audit. SATISFACTORY.**

The ratings plug interfaces properly with the trip unit.

Programmer + ratings plug provide trip settings per the Square D published trip curves.

Schneider Electric second party contractors and test department personnel in Grenoble, France verified the ratings plug interface with the trip unit during integration testing.

**Verified by inspection during this audit. SATISFACTORY.**

The ratings plug interface with the trip unit was demonstrated during IEC and ANSI testing performed by Schneider Electric and Square D.

**Verified by test report reviews and personnel interviews during this audit. SATISFACTORY.**

Trip settings.	Verify that the trip settings are per the Square D curves.	Trip unit trip command compliance with published curves was verified during developmental testing at Square D and during IEC and ANSI testing performed by Schneider Electric and Square D.  <b>Verified by specification document review, trip unit developmental test path note inspection, IEC and ANSI test report reviews, and personnel interviews during this audit. SATISFACTORY.</b>
I function defeat operates properly.	The function is defeated.  I function defeat does not impact operation of the active functions.	I function defeat operation was verified during integration testing that was performed by Schneider Electric second party contractors and test department personnel in Grenoble, France.  <b>Verified by specification document review, trip unit developmental test path note inspection, and personnel interviews during this audit.</b>
No spurious tripping.	There is no spurious tripping outside the active trip functions and the trip curve.	The IEC and ANSI testing of the production units of the Micrologic trip unit and Masterpact NT and NW breaker suites performed by Schneider Electric and Square D did not identify incidents of spurious tripping. Industry experience has identified incidents of spurious tripping (see section 7.3 of the main body of the V&V report).  <b>Verified by IEC and ANSI test report reviews and personnel interviews during this audit. SATISFACTORY.</b>
Non-safety functions do not interfere with safety related trip function.	Communications and display functions are non-safety related. The communication feature will not be connected in the plant.  Verify that the communication and display functions will not interfere with the trip function.	The only interface between the ASIC and the non-safety related functions is the serial communications line. A shorted or open serial interface line does not interfere with the ASIC's safety related function as demonstrated by FEMA analysis and integration testing that was performed by Schneider Electric second party contractors and test department personnel in Grenoble, France.  <b>Verified by specification document review, trip unit developmental test path note inspection, FEMA document review, and personnel interviews during this audit. SATISFACTORY.</b>



Breaker position on ASIC failure.	The breaker will remain in the current position upon ASIC failure.	The breaker will remain in the current position upon ASIC failure as demonstrated by FEMA analysis and integration testing that was performed by Schneider Electric second party contractors and test department personnel in Grenoble, France.  <b>Verified by specification document review, trip unit developmental test path note inspection, FEMA document review, and personnel interviews during this audit. SATISFACTORY.</b>
Indication on ASIC failure.	If the ASIC fails, and LED on the front of the programmer will light.	The ASIC failure LED on the front of the programmer will light upon ASIC failure as demonstrated by FEMA analysis and integration testing that was performed by Schneider Electric second party contractors and test department personnel in Grenoble, France.  <b>Verified by specification document review, trip unit post-production test report review, and personnel interviews during this audit. SATISFACTORY.</b>
Short circuit protection on ASIC failure.	If the ASIC fails, the programmer will still provide short circuit protection.	The analog portion of the ASIC provides short circuit when the digital portion of the ASIC fails as demonstrated by FEMA analysis and integration testing that was performed by Schneider Electric second party contractors and test department personnel in Grenoble, France.  <b>Verified by specification document review, trip unit developmental test path note inspection, and personnel interviews during this audit. SATISFACTORY.</b>
Battery function.	The battery is not required for the safety related trip function.	Verified by design review. The battery circuit is completely independent to the ASIC power supply circuit.  <b>Verified by specification document review, FEMA analysis review, and personnel interviews during this audit. SATISFACTORY.</b>
Trip unit performance upon loss of clock (gate pulse)	The digital protective function is lost; analog short circuit and thermal trip functions are maintained.	In case of clock (gate) failure, the ASIC stops performing its digital protection functions in accordance with user selected trip parameters and leaves the breaker in the closed position. The Ap indicator LED is lighted to alert operator or maintenance personnel. There is no loss of protection capabilities because the ASIC will continue to trip the circuit breaker when the trip unit (measured by a positive temperature coefficient thermistor) reaches 115-125°C or contact current reaches or exceeds the circuit breaker's instantaneous overload trip interrupt (DIN) rating. When the temperature or instantaneous overload trip current threshold is reached, the circuit breaker contacts will open within 20 milliseconds.  <b>Verified by specification document reviews, FEMA analysis inspection, and personnel interview during this audit. SATISFACTORY.</b>



**Attachment B**

**NLI Validation Test Plan VVTP-042181-1 with Test Data**

**Verification and Validation Test Plan (NLI Validation Test Plan for Micrologic 6.0P Programmer)**

Verification Plan #VVTP-042181-1, Rev. 1

Description: Digital trip device for Square D Mastepact NT and NW low voltage switchgear breakers

Manufacturer / Model: Square D/Schneider Micrologic 6.0P Programmer

Safety Function: To maintain low voltage power circuits during normal operation and interrupt circuits during fault conditions.

Remote communications, interlocks, remote alarms, and history storage and recall are not safety related functions.

Critical Characteristic	Sample Size	Acceptance		
		Criteria	Ref	Method
<b>Notes:</b> 1. This plan includes FMEA testing. 2. All testing will be performed on a Square D Masterpact NT or NW, unless specified otherwise. 3. Functions <ul style="list-style-type: none"> <li>• L = Long time.</li> <li>• S = Short time.</li> <li>• I = Instantaneous.</li> <li>• G = Ground.</li> </ul>				

B.2

Verification Plan #VVTP-042181-1, Rev. 1

Description: Digital trip device for Square D Mastepact NT and NW low voltage switchgear breakers

Manufacturer / Model: Square D/Schneider Micrologic 6.0P Programmer

Safety Function: To maintain low voltage power circuits during normal operation and interrupt circuits during fault conditions.

Remote communications, interlocks, remote alarms, and history storage and recall are not safety related functions.

Critical Characteristic	Sample Size	Acceptance		
		Criteria	Ref	Method
Verification of all trip settings CC#1	1	<p>Programmer actuates per the published trip curve [1] in all applicable normal and abnormal configurations.</p> <p>Function defeat switches operate per design.</p> <p>Signal condition and logic functions are per the Schneider design.</p> <p>Programmer is per the Schneider design and published data.</p> <p>There are no trip unit features that could interrupt operation.</p>	1, 2	Primary injection testing per the test sequence in Attachment I.
Programmer operates on Square D Mastepact NT or NW breaker. CC#1A	1	<p>Programmer can be mounted on the Masterpact NT or NW and interfaces properly with the CT's, ratings plug, and actuator.</p> <p>Programmer operates per the trip curve [1] installed in the Masterpact NT or NW.</p>	1, 2	<p>Primary injection testing per the test sequence in Attachment I.</p> <p>Note: Dedication testing of 100% of the shipped trip units will verify proper operation on each specific breaker.</p>

B.3

Verification Plan #VVTP-042181-1, Rev. 1

Description: Digital trip device for Square D Mastepact NT and NW low voltage switchgear breakers

Manufacturer / Model: Square D/Schneider Micrologic 6.0P Programmer

Safety Function: To maintain low voltage power circuits during normal operation and interrupt circuits during fault conditions.

Remote communications, interlocks, remote alarms, and history storage and recall are not safety related functions.

Critical Characteristic	Sample Size	Acceptance		
		Criteria	Ref	Method
Programmer operates per design with ratings plugs. CC#1B	1	<p>Programmer interfaces properly with the Masterpact ratings plugs.</p> <p>Programmer operates per the trip curve [1] installed in the Masterpact NT and NW with ratings plugs.</p>	1, 2	Primary injection testing per the test sequence in Attachment I.
Output alarms are per design. CC#1C	1	<p>The output alarms that will be operational are the LED's on the front of the trip unit. The remote alarm and communication features will not be connected in safety related application.</p> <p>Verify that the LED alarms and rest operate per design:</p> <ul style="list-style-type: none"> <li>• "alarm": LED on when the trip unit is in an overload condition.</li> <li>• Trip LED: LED on when the trip unit trips and remains on until reset.</li> <li>• "test/reset": button resets the trip LED.</li> </ul>	1, 2	Primary injection testing per the test sequence in Attachment I.

B.4

Verification Plan #VVTP-042181-1, Rev. 1

Description: Digital trip device for Square D Mastepact NT and NW low voltage switchgear breakers

Manufacturer / Model: Square D/Schneider Micrologic 6.0P Programmer

Safety Function: To maintain low voltage power circuits during normal operation and interrupt circuits during fault conditions.

Remote communications, interlocks, remote alarms, and history storage and recall are not safety related functions.

Critical Characteristic	Sample Size	Acceptance		
		Criteria	Ref.	Method
Remote communications, alarms, and interlocks do not impact trip unit operation. CC#1D	1	The remote communications, alarms, and interlock functions will not be connected in the plant and are not qualified for safety related applications.  This testing will verify that the remote communications, alarms, and interlock functions will not impact the safety related protection functions of the trip unit.	1, 2	Primary injection testing per the test sequence in Attachment I.
No spurious tripping. CC#1E	1	The trip unit does not spuriously fire.	1, 2	Primary injection testing per the test sequence in Attachment I.
Operation of the reset button. CC#1F	1	The reset button resets the trip lights.  The breaker trips per the trip curve with and without the reset.	1, 2	Primary injection testing per the test sequence in Attachment I. Test with the programmer reset and not reset.
Programmer restarts after loss of power. CC#2	1	Programmer restarts and operates per design following loss of power.  Note: By design, the trip unit and ASIC technology is designed to operate properly after being unpowered for an indefinite amount of time.	1, 2	Perform injection primary testing after the trip unit has been unpowered for at least 48 hours.  Test per the test sequence in Attachment I.
(not used) CC#3	N/a	N/a	N/a	N/a

8.5



Verification Plan #VVTP-042181-1, Rev. 1

Description: Digital trip device for Square D Mastepact NT and NW low voltage switchgear breakers

Manufacturer / Model: Square D/Schneider Micrologic 6.0P Programmer

Safety Function: To maintain low voltage power circuits during normal operation and interrupt circuits during fault conditions.

Remote communications, interlocks, remote alarms, and history storage and recall are not safety related functions.

Critical Characteristic	Sample Size	Acceptance		
		Criteria	Ref	Method
(not used) CC#4	N/a	N/a	N/a	N/a
(not used) CC#5	N/a	N/a	N/a	N/a
Programmer operates properly with battery remove or dead battery. CC#6	1	Programmer operates properly with the battery removed.  Programmer operates properly with a dead battery installed in the trip unit.	1, 2	Perform primary injection testing with the battery removed and with a dead battery installed. Perform testing with the battery installed and then removed and then reinstalled.  Test per the test sequence in Attachment I.
Memory does not impact trip unit operation. CC#7	1	The trip unit contains memory that records breaker history. Verify that recalling of history from memory does not affect the trip unit settings.	1, 2	Perform primary injection testing of the breaker after recalling history from memory. Verify that the primary injection testing trip times and currents are per the trip curves [1] after history is recalled from memory.  Test per the test sequence in Attachment I.



B.L

Verification Plan #VVTP-042181-1, Rev. 1

Description: Digital trip device for Square D Mastepact NT and NW low voltage switchgear breakers

Manufacturer / Model: Square D/Schneider Micrologic 6.0P Programmer

Safety Function: To maintain low voltage power circuits during normal operation and interrupt circuits during fault conditions.

Remote communications, interlocks, remote alarms, and history storage and recall are not safety related functions.

Critical Characteristic	Sample Size	Acceptance		
		Criteria	Ref	Method
Secondary test set does not impact trip unit settings. CC#8	1	Testing of the trip unit with the secondary test set overrides the switch settings. Verify that the secondary testing does not permanently change the trip unit settings.	1, 2	Perform primary injection testing of the breaker after the secondary injection testing. Verify that the primary injection testing trip times and currents are per the trip curves [1] after testing with the secondary test set.  Test per the test sequence in Attachment I.
Function defeat switches operate per design CC#9	1	The defeat switches for I properly defeats this function.	1, 2	Test per the sequence in Attachment I.
Operation across voltage range CC#10	1	Programmer powers up properly across the voltage range of 300-650vac.  Note: The programmer is powered from the CT's, which provide current to the programmer. Primary injection testing of the breaker provides less than 10 vac. By design, the programmers are designed to operate a very low voltage levels.	1, 2	Test per the sequence in Attachment I.



B.1

Verification Plan #VVTP-042181-1, Rev. 1

Description: Digital trip device for Square D Mastepact NT and NW low voltage switchgear breakers

Manufacturer / Model: Square D/Schneider Micrologic 6.0P Programmer

Safety Function: To maintain low voltage power circuits during normal operation and interrupt circuits during fault conditions.  
 Remote communications, interlocks, remote alarms, and history storage and recall are not safety related functions.

Critical Characteristic	Sample Size	Acceptance		
		Criteria	Ref	Method

**Sample Size:**

A sample size of 1 trip unit is used for the validation testing. The traceability of this testing is based on the following:

- The audit of Schneider verified configuration control.
- Dedication testing will be performed on 100% of the supplied trip units in accordance with the applicable dedication/Factory Acceptance Test plan. The dedication activities include verification of a sample of the trip points 100% of the shipped units.
- Perform some of the testing was performed on a Micrologic model 3.0 to provide added assurance.

The basis for the number of trip points tested during primary and secondary injection testing is as follows:

- The audit of Schneider documented that the logic and programming for the L, S, I, and G functions are separate in the trip unit. Therefore, testing each function separately is acceptable. 100% of the switch settings for each function will be tested to verify that the breaker trips per the published curves [1].
- As discussed above, each function has independent logic and programming, therefore, one function will not interfere with the other functions.
- The signals from the 3 CT's are each compared to the trip settings that are set by the switch. The testing per the plan is only required to be performed on one phase, since this testing is validating that the field settable switches on the trip unit properly set the AND and OR gates. The testing is varied between the phases to provide additional assurance.

**References:**

1. Square D Masterpact Micrologic trip curves, "Masterpact NT/NW Universal Power Circuit Breakers, Section 7: Trip Curves", dated 6/01.
2. Square D Masterpact Micrologic manual 48049-137-04, "Micrologic 5.0P and 6.0P Electronic Trip Units", dated 05/2003.

B.2



resigned original

VVTP Approval Prepared:	<u>Ande</u>	<u>5/6/04</u>	Reviewed:	<u>[Signature]</u>	<u>5/6/04</u>	Approved:	<u>[Signature]</u>	<u>5/6/04</u>
		Date			Date			Date

B.9

**Validation Test Plan for Square D/Schneider Micrologic Programmer  
VVTP-042181-1, revision 0  
Attachment I**

**Data Recording**

Record the following data, as applicable:

- Programmer model and s/n. MicroLogic S/N: 042181-MTU-01
  - Programmer code name and revision. PN: 5164A 6.0P
  - Breaker model and s/n. Masterpact NW32H2
  - Rating plug model and size. 1125-E 3200A
- ONBox 48F18

**PERFORM CC#3, 4, 5A, 5B AFTER THE OTHER CC'S ARE COMPLETED.**

**CC#1, #1A to 1E, #2, #6, #7, #8**

**PRIMARY INJECTION TESTING**

- **Objective:** The purpose of this testing is as follows:
  - (CC#1) Test some combinations of switch settings on the trip unit.
  - (C#1A) Programmer operates on Square D Masterpact NT or NW breaker.
  - (CC#1B) Programmer operates per design with the rating plug installed.
  - (CC#1C) Output alarms are per design.
  - (CC#1D) Remote communications, alarms and interlocks do not impact trip unit operation.
  - (CC#1E) No spurious tripping.
  - (CC#1F) Programmer trips per curve with and without reset.
  - (CC#2) Test to verify that loss of power will not impact the trip unit settings.
  - (CC#6) Test to verify that battery removal or a dead battery will not impact the trip unit safety function.
  - (CC#7) Verify that recalling information from memory will not impact the trip unit safety function.
  - (CC#8) Verify that secondary injection testing does not impact the settings or trip unit function.
  - Primary injection testing of the defeat functions is tested separately in CC#9.

• **Initial Conditions**

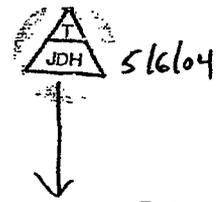
- Programmer installed on the NT or NW breaker.
- Primary power to the bus and trip unit powered.

• **Test Sequence-Primary Injection**

- Perform secondary injection testing and record the results (the purpose of this step is to verify CC#8). Record trip settings, trip time, and SAT/UNSAT:

Instantaneous test #1:	15X	0.036 SECONDS	SAT
Instantaneous test #2:	8X	0.044 SECONDS	SAT
Short time test #1:	10X 0 OFF	0.054 SECONDS	SAT
Short time test #2:	5X .4 ON	0.41 SECONDS	SAT
Long time test #1:	1x 12S	7.8 SECONDS	SAT

FUNCTIONS NOT  
TESTED W/ME  
UNABLE TO BY SECONDARY  
INJECTION TEST SAT.



5/16/04  


- Long time test #2: .5x 12s 26.9 SECONDS SAT
- Perform primary injection testing with the conditions and settings per Table 1 which is attached.

**CC#9 Defeat switches for each function operate properly. Test using primary injection.**

• **Initial Conditions**

- Programmer installed on the breaker.
- Primary power to the bus and trip unit powered.

• **Test Sequence**

- Testing will be by primary injection.
- Record current, time, and trip/no trip for each test.
- Test A phase.

▪ Defeat I only (set to off).

- Inject current in S range and verify trip: 24000 A .42SEC TRIP
- Injection current in I range and verify no trip: 24000 A NO TRIP @ .1SEC.
- Simulate ground fault and verify trip: 1440A 0.26SEC TRIP
- Inject current in L range and verify trip: 6720A 4.2SEC TRIP

5/16/04  


○ Test B phase.

▪ Defeat I only (set to off).

- Inject current in S range and verify trip: 24000A .41SEC TRIP
- Injection current in I range and verify no trip: 24000A NO TRIP @ .1SEC
- Simulate ground fault and verify trip: 1440 A 0.26SEC TRIP
- Inject current in L range and verify trip: 6720A 4.4 SEC TRIP

5/16/04  


○ Test C phase.

▪ Defeat I only (set to off).

- Inject current in S range and verify trip: 24000A .40SEC TRIP
- Injection current in I range and verify no trip: 24000A NO TRIP @ .1SEC
- Simulate ground fault and verify trip: 1440 A 0.27SEC TRIP
- Inject current in L range and verify trip: 6720A 4.3 SEC TRIP

5/16/04  


**CC#10 Programmer operation across primary voltage range.**

• **Initial Conditions**

- Programmer installed on the breaker.
- Primary power to the bus and trip unit powered.

• **Test Sequence**

- Apply 300 vac to each primary phase and verify that the programmer powers up.

Phase A:	<u>300 VAC</u>	<u>SAT</u>
Phase B:	↓	↓
Phase C:	↓	↓

- Apply 650 vac to each primary phase and verify that the programmer powers up.

Phase A:	<u>650 VAC</u>	<u>SAT</u>
Phase B:	↓	↓
Phase C:	↓	↓

B.11

**TABLE 2  
PRIMARY INJECTION TESTING**

The data in each column is as follows:

- Battery in, out, or dead:
  - In: Battery installed.
  - Out: Battery removed.
  - Dead: Battery installed but dead.
- Recall from memory before test:
  - Yes: Recall some information from memory immediately prior to the specified test.
  - No: Do not recall information from memory immediately prior to the specified test.
- Phase: Primary injection to the specified phase.
- Reset before test:
  - No: Do not reset the programmer with the reset button prior to the test.
  - Yes: Reset the programmer with the reset button prior to the test
- Tested functions: Set the trip unit per the specified settings.
- Record other function settings: The functions that are not being tested should be set to random settings. Record these settings.
- Record results:
  - Record trip time and current.
  - Alarm light on when in overload condition (Y, N).
  - Trip light on following trip (Y, N).
  - Reset operates to reset the trip unit (Y, N).
  - (current and time): Record the simulated test current and trip time for the tested function.
- SAT/UNSAT: Document whether the testing meets the published trip curve [1] or not. Verify no spurious trips.

Battery in, out, dead	Recall from memory before test	Phase	Reset?	Tested function	Record other function settings	Record Results (current and time, alarm light, trip light, reset)	SAT/UNSAT
				Instantaneous			
Dead	No	A	No	I=2	Micrologic 6.0P LONG TIME 1.0 s	Current= 6400A Time= 0.04sec	SAT

B.12

RECY 16 S  
 START TIME 5x  
 DUMP .3 on  
 GROUND DEFATED J .4on



					SEE PAGE 11	Alarm: YES Trip: YES Reset: NO	SAT
Dead	No	A	No	I=3		Current= 9600 A Time= 0.02 Sec	SAT
Dead	No	B	No	I=4		Alarm: YES Trip: YES Reset: NO	SAT
Dead	No	B	No	I=6		Current= 12,800 A Time= 0.04 Sec	SAT
Dead	No	B	No	I=6		Alarm: YES Trip: YES Reset: NO	SAT
Dead	No	B	Yes	I=8		Current= 19,200 A Time= 0.02 Sec	SAT
Dead	No	B	Yes	I=8		Alarm: YES Trip: YES Reset: NO	SAT
Dead	No	C	Yes	I=10		Current= 25,600 A Time= 0.04 Sec	SAT
Dead	No	C	Yes	I=10		Alarm: YES Trip: YES Reset: NO	SAT
Dead	No	C	No	I=12		Current= 32,000 A Time= 0.04 Sec	SAT
Dead	No	C	No	I=12		Alarm: YES Trip: YES Reset: NO	SAT
Dead	Yes	C	No	I=15		Current= 38,400 A Time= 0.04 Sec	SAT
Dead	Yes	C	No	I=15		Alarm: YES Trip: YES Reset: NO	SAT
				Ground Fault			
Dead	No	A	No	Lg=A, Tg=.1 on 0.11-0.23 Sec	LONG TIME AND SHORT TIME SET	Current= 1000 A Time= 0.14 Sec	SAT
Dead	No	A	No	Lg=A, Tg=.2 on 0.22-0.35 Sec	TO MAX PICKUP AND DELAY.	Alarm: NO Trip: YES Reset: NO	SAT
Dead	No	A	No	Lg=A, Tg=.3 on 0.33-0.45 Sec	INSTANTANEOUS TURNED TO OFF	Current= 1000 A Time= 0.23 Sec	SAT
Dead	No	A	No	Lg=A, Tg=.3 on 0.33-0.45 Sec	INSTANTANEOUS TURNED TO OFF	Alarm: NO Trip: YES Reset: NO	SAT
Dead	No	A	No	Lg=A, Tg=.4 on 0.5-0.7 Sec	FOR ALL GROUND FAULT	Current= 1000 A Time= 0.40 Sec	SAT
Dead	No	A	No	Lg=A, Tg=.4 off 0.32-0.45 Sec	TESTS.	Alarm: NO Trip: YES Reset: NO	SAT
Dead	No	A	No	Lg=A, Tg=.3 off .24-.32 Sec		Current= 1000 A Time= 0.62 Sec	SAT
Dead	No	A	No	Lg=A, Tg=.3 off .24-.32 Sec		Alarm: NO Trip: YES Reset: NO	SAT
Dead	No	A	No	Lg=A, Tg=.2 off .14-.19 Sec		Current= 1000 A Time= 0.26 Sec	SAT
Dead	No	A	No	Lg=A, Tg=.2 off .14-.19 Sec		Alarm: NO Trip: YES Reset: NO	SAT
Dead	No	A	Yes	Lg=A, Tg=.1 off .08-.14 Sec		Current= 1000 A Time= 0.16 Sec	SAT
Dead	No	A	Yes	Lg=A, Tg=.1 off .08-.14 Sec		Alarm: NO Trip: YES Reset: NO	SAT
Dead	No	A	Yes	Lg=A, Tg=0 off .02-.08 Sec		Current= 1000 A Time= 0.15 Sec	SAT
Dead	No	A	Yes	Lg=A, Tg=0 off .02-.08 Sec		Alarm: NO Trip: YES Reset: YES	SAT
Dead	No	A	Yes	Lg=A, Tg=0 off .02-.08 Sec		Current= 1000 A Time= 0.037 Sec	SAT

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5/6/04

						Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=B, Tg=.1 on 0.08 - 0.14 Sec		Current= <u>1280 A</u> Time= <u>0.097 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=B, Tg=.2 on 0.14 - 0.19 Sec		Current= <u>1280 A</u> Time= <u>0.16 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=B, Tg=.3 on 0.24 - 0.32 Sec		Current= <u>1280 A</u> Time= <u>0.26 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=B, Tg=.4 on 0.32 - 0.48 Sec		Current= <u>1280 A</u> Time= <u>0.40 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=B, Tg=.4 off 0.32 - 0.48 Sec		Current= <u>1280 A</u> Time= <u>0.41 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=B, Tg=.3 off 0.24 - 0.32 Sec		Current= <u>1280 A</u> Time= <u>0.26 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=B, Tg=.2 off 0.14 - 0.19 Sec		Current= <u>1280 A</u> Time= <u>0.16 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=B, Tg=.1 off 0.08 - 0.14 Sec		Current= <u>1280 A</u> Time= <u>0.097 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=B, Tg=0 off 0.02 - 0.08 Sec		Current= <u>1280 A</u> Time= <u>0.037 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=C, Tg=.1 on 0.08 - 0.14 Sec		Current= <u>1440 A</u> Time= <u>0.097 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=C, Tg=.2 on 0.14 - 0.19 Sec		Current= <u>1440</u> Time= <u>0.16 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=C, Tg=.3 on 0.24 - 0.32 Sec		Current= <u>1440 A</u> Time= <u>0.26 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=C, Tg=.4 on 0.32 - 0.48 Sec		Current= <u>1440 A</u> Time= <u>0.40 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	Yes	Lg=C, Tg=.4 off 0.32 - 0.48 Sec		Current= <u>1440 A</u> Time= <u>0.40 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u>	SAT
Dead	No	B	No	Lg=C, Tg=.3 off 0.24 - 0.32 Sec		Current= <u>1440 A</u> Time= <u>0.26 SEC</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=C, Tg=.2 off 0.14 - 0.19 Sec		Current= <u>1440 A</u> Time= <u>0.16 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=C, Tg=.1 off 0.08 - 0.14 Sec		Current= <u>1440 A</u> Time= <u>0.10 SEC</u>	SAT

3.14

5/6/04  
  
 JDH

						Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=C, Tg=0 off 0.02-0.08 SEC		Current= <u>1440 A</u> Time= <u>0.037 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=D, Tg=.1 on 0.08-0.14 SEC		Current= <u>1600 A</u> Time= <u>0.11 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=D, Tg=.2 on 0.14-0.19 SEC		Current= <u>1600 A</u> Time= <u>0.16 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=D, Tg=.3 on 0.19-0.32 SEC		Current= <u>1600 A</u> Time= <u>0.26 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=D, Tg=.4 on 0.32-0.48 SEC		Current= <u>1600 A</u> Time= <u>0.40 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=D, Tg=.4 off 0.32-0.48 SEC		Current= <u>1600 A</u> Time= <u>0.41 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=D, Tg=.3 off 0.24-0.32 SEC		Current= <u>1600 A</u> Time= <u>0.26 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=D, Tg=.2 off 0.14-0.19 SEC		Current= <u>1600 A</u> Time= <u>0.17 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
Dead	No	B	No	Lg=D, Tg=.1 off 0.08-0.14 SEC		Current= <u>1600 A</u> Time= <u>0.11 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
In	No	B	No	Lg=D, Tg=0 off 0.02-0.08 SEC		Current= <u>1600 A</u> Time= <u>0.054 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
In	No	C	No	Lg=E, Tg=.1 on	ALL CURVE SPECS	Current= <u>1760 A</u> Time= <u>0.11 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
In	No	C	No	Lg=E, Tg=.2 on	FOR GROUND FAULT	Current= <u>1760 A</u> Time= <u>0.17 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
In	No	C	No	Lg=E, Tg=.3 on	REPEAT SAME ON	Current= <u>1760 A</u> Time= <u>0.24 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
In	No	C	No	Lg=E, Tg=.4 on	EXACT DELAY.	Current= <u>1760 A</u> Time= <u>0.42 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
In	No	C	No	Lg=E, Tg=.4 off		Current= <u>1760 A</u> Time= <u>0.41 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
In	No	C	No	Lg=E, Tg=.3 off		Current= <u>1760 A</u> Time= <u>0.24 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT
In	No	C	No	Lg=E, Tg=.2 off		Current= <u>1760 A</u> Time= <u>0.17 SEC</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u>	SAT

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						Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=E, Tg=.1 off		Current= 1760 A Time= 0.10 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=E, Tg=0 off		Current= 1760 A Time= 0.048 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=F, Tg=.1 on		Current= 1920 A Time= 0.10 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=F, Tg=.2 on		Current= 1920 A Time= 0.17 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=F, Tg=.3 on		Current= 1920 A Time= 0.27 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=F, Tg=.4 on		Current= 1920 A Time= 0.41 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=F, Tg=.4 off		Current= 1920 A Time= 0.42 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=F, Tg=.3 off		Current= 1920 A Time= 0.28 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=F, Tg=.2 off		Current= 1920 A Time= 0.17 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=F Tg=.1 off		Current= 1920 A Time= 0.11 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=F Tg=0 off		Current= 1920 A Time= 0.054 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=G, Tg=.1 on		Current= 2080 A Time= 0.11 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=G, Tg=.2 on		Current= 2080 A Time= 0.17 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=G, Tg=.3 on		Current= 2080 A Time= 0.28 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=G, Tg=.4 on		Current= 2080 A Time= 0.42 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=G, Tg=.4 off		Current= 2080 A Time= 0.42 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=G, Tg=.3 off		Current= 2080 A Time= 0.28 Sec Alarm: NO Trip: YES Reset: NO	SAT

B.16

						Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=G, Tg=.2 off 0.14-0.19 Sec		Current= 2080 A Time= 0.17 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=G, Tg=.1 off 0.08-0.14 Sec		Current= 2080 A Time= 0.11 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=G, Tg=0 off 0.02-0.05 Sec		Current= 2080 A Time= 0.054 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=H, Tg=.1 on 0.08-0.14 Sec		Current= 2240 A Time= 0.10 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=H, Tg=.2 on 0.14-0.19 Sec		Current= 2240 A Time= 0.18 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=H, Tg=.3 on 0.24-0.32 Sec		Current= 2240 A Time= 0.28 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=H, Tg=.4 on 0.32-0.48 Sec		Current= 2240 A Time= 0.42 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=H, Tg=.4 off 0.32-0.48 Sec		Current= 2240 A Time= 0.41 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=H, Tg=.3 off 0.24-0.32 Sec		Current= 2240 A Time= 0.27 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=H, Tg=.2 off 0.14-0.19 Sec		Current= 2240 A Time= 0.16 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=H Tg=.1 off 0.08-0.14 Sec		Current= 2240 A Time= 0.10 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=H Tg=0 off 0.02-0.05 Sec		Current= 2240 A Time= 0.04 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=J, Tg=.1 on .08-0.14 Sec		Current= 2400 A Time= 0.099 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=J, Tg=.2 on 0.14-0.19 Sec		Current= 2400 A Time= .16 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	No	C	No	Lg=J, Tg=.3 on 0.24-0.32 Sec		Current= 2400 A Time= 0.27 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	Yes	C	No	Lg=J, Tg=.4 on 0.32-0.48 Sec		Current= 2400 A Time= 0.41 Sec Alarm: NO Trip: YES Reset: NO	SAT
In	Yes	C	No	Lg=J, Tg=.4 off 0.32-0.48 Sec		Current= 2400 A Time= 0.41 Sec Alarm: NO Trip: YES Reset: NO	SAT

B17



						Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT
In	Yes	C	No	Lg=J, Tg=.3 off 0.24-0.32sec		Current= <u>2400 A</u> Time= <u>0.27sec</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT
In	Yes	C	No	Lg=J, Tg=.2 off 0.14-0.19sec		Current= <u>2400A</u> Time= <u>0.16sec</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT
In	Yes	C	No	Lg=J Tg=.1 off 0.08-0.14Sec		Current= <u>2400A</u> Time= <u>0.09sec</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT
In	Yes	C	No	Lg=J Tg=0 off 0.02-0.08sec		Current= <u>2400A</u> Time= <u>0.05sec</u> Alarm: <u>NO</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT
				<b>Short Time</b>		
In	No	A	No	Isd=1.5, tsd=.1on	2400 x 1.5 = 3600 A LONG TIME 15X 24S INST. 15X 2.2-4.5sec	Current= <u>3600A</u> Time= <u>2.3sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT
In	No	A	Yes	Isd=1.5, tsd=.2on	4.0 - 9sec	Current= <u>3600A</u> Time= <u>4.1sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u> SAT
In	No	A	Yes	Isd=1.5, tsd=.3on	5 - 12sec	Current= <u>3600A</u> Time= <u>6.7sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u> SAT
In	No	A	Yes	Isd=1.5, tsd=.4on	10.5 - 19sec	Current= <u>3600A</u> Time= <u>10.9sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u> SAT
In	No	A	Yes	Isd=1.5, tsd=.4 off	0.35-0.50 sec	Current= <u>3600A</u> Time= <u>.42sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u> SAT
In	No	A	Yes	Isd=1.5, tsd=.3 off	0.23-0.32sec	Current= <u>3600A</u> Time= <u>.28sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u> SAT
In	No	A	Yes	Isd=1.5, tsd=.2 off	0.14 - 0.20sec	Current= <u>3600A</u> Time= <u>0.18sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u> SAT
In	No	A	Yes	Isd=1.5, tsd=.1 off	0.08 - 0.14sec	Current= <u>3600A</u> Time= <u>0.11sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>YES</u> SAT
In	No	A	No	Isd=1.5, tsd=0 off	0.02 - 0.08sec	Current= <u>3600A</u> Time= <u>0.05sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT
In	No	A	No	Isd=2, tsd=.1on 3200 x 1.5 = 4800A	LONG TIME 15X 24S INST 15X .9 - 2.1sec	Current= <u>4800A</u> Time= <u>1.9sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT
In	No	A	No	Isd=2, tsd=.2on	1.5 - 3sec	Current= <u>4800A</u> Time= <u>2.7sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT
In	No	A	No	Isd=2, tsd=.3on	2.8 - 5.3sec	Current= <u>4800A</u> Time= <u>4.5sec</u> Alarm: <u>YES</u> Trip: <u>YES</u> Reset: <u>NO</u> SAT

B.18

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						Alarm: YES Trip: YES Reset: NO	SAT
In	No	A	No	Isd=2, tsd=.4on	3.8 - 7.2sec	Current= 4800A Time= 6.9sec Alarm: YES Trip: YES Reset: NO	SAT 5/6/04 NO SAT
In	No	A	No	Isd=2, tsd=.4 off	.35 - .50sec	Current= 4800A Time= 0.43sec Alarm: YES Trip: YES Reset: NO	SAT
In	No	A	No	Isd=2, tsd=.3 off	.23 - .32sec	Current= 4800A Time= 0.29sec Alarm: YES Trip: YES Reset: NO	SAT
In	No	B	No	Isd=2, tsd=.2 off	.14 - .20sec	Current= 4800A Time= 0.18sec Alarm: YES Trip: YES Reset: NO	SAT
In	No	B	No	Isd=2, tsd=.1 off	.08 - .14 Sec	Current= 4800A Time= 0.12sec Alarm: YES Trip: YES Reset: NO	SAT
In	No	B	No	Isd=2, tsd=0 off	✓ .02 - .08sec	Current= 4800A Time= 0.065sec Alarm: YES Trip: YES Reset: NO	SAT
In	No	B	No	Isd=2.5, tsd=.1on	4000 x 1.5 = 6000A LONG TIME .5X 245 INST. 15X .58 - .1sec	Current= 6000A Time= 0.86sec Alarm: YES Trip: YES Reset: NO	SAT
In	No	B	No	Isd=2.5, tsd=.2on	.9 - 1.6 sec	Current= 6000A Time= 1.4sec Alarm: YES Trip: YES Reset: NO	SAT
In	No	B	No	Isd=2.5, tsd=.3on	1.5 - 2.7 sec	Current= 6000A Time= 2.4sec Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=2.5, tsd=.4on	2.4 - 4.2 sec	Current= 6000A Time= 3.6sec Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=2.5, tsd=.4 off	.35 - .50sec	Current= 6000A Time= 0.42sec Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=2.5, tsd=.3 off	.23 - .32sec	Current= 6000A Time= 0.28sec Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=2.5, tsd=.2 off	.14 - .20sec on system - .20 sec	Current= 6000A Time= 0.17sec Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=2.5, tsd=.1 off	.08 - .14 sec	Current= 6000A Time= 0.11sec Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=2.5, tsd=0 off	✓ .02 - .08 sec	Current= 6000A Time= .056 sec Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=3, tsd=.1on	4000 x 1.5 = 7200A LONG TIME .5X 245 INST. 15X .4 - .8sec	Current= 7200A Time= 0.57sec Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=3, tsd=.2on	.7 - 1.4sec	Current= 7200A Time= 0.92sec	SAT

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Out	No	B	No	Isd=3, tsd=.3on	1.25 - 2.4 sec <del>5664 .65 - .1 sec</del>	Alarm: YES Trip: YES Reset: NO Current= 7200 A Time= 1.6 sec	SAT
Out	No	B	No	Isd=3, tsd=.4on	1.6 - 3.1 sec <del>5664 .95 - 1.75 sec</del>	Alarm: YES Trip: YES Reset: NO Current= 7200 A Time= 2.4 sec	SAT
Out	No	B	No	Isd=3, tsd=.4 off	.35 - .50 sec	Alarm: YES Trip: YES Reset: NO Current= 7200 A Time= 0.42 sec	SAT
Out	No	B	No	Isd=3, tsd=.3 off	.23 - .32 sec	Alarm: YES Trip: YES Reset: NO Current= 7200 A Time= 0.28 sec	SAT
Out	No	B	No	Isd=3, tsd=.2 off	.14 - .20 sec	Alarm: YES Trip: YES Reset: NO Current= 7200 A Time= 0.17 sec	SAT
Out	No	B	No	Isd=3, tsd=.1 off	.08 - .14 sec	Alarm: YES Trip: YES Reset: NO Current= 7200 A Time= 0.11 sec	SAT
Out	No	B	No	Isd=3, tsd=0 off	.02 - .08 sec	Alarm: YES Trip: YES Reset: NO Current= 7200 A Time= 0.055 sec	SAT
Out	No	B	No	Isd=4, tsd=.1on 8000 x 1.5 = 9600	Long Time .32 245 Inst. 15x .23 - .45 sec	Alarm: YES Trip: YES Reset: NO Current= 9600 A Time= 0.34 sec	SAT
Out	No	B	No	Isd=4, tsd=.2on	.40 - .70 sec	Alarm: YES Trip: YES Reset: NO Current= 9600 A Time= 0.55 sec	SAT
Out	No	B	No	Isd=4, tsd=.3on	.65 - .1 sec	Alarm: YES Trip: YES Reset: NO Current= 9600 A Time= 0.94 sec	SAT
Out	No	B	No	Isd=4, tsd=.4on	.95 - 1.75 sec	Alarm: YES Trip: YES Reset: NO Current= 9600 A Time= 1.4 sec	SAT
Out	No	B	No	Isd=4, tsd=.4 off	.35 - .50 sec	Alarm: YES Trip: YES Reset: NO Current= 9600 A Time= 0.42 sec	SAT
Out	No	B	No	Isd=4, tsd=.3 off	.23 - .32 sec	Alarm: YES Trip: YES Reset: NO Current= 9600 A Time= 0.28 sec	SAT
Out	No	B	No	Isd=4, tsd=.2 off	.14 - .20 sec	Alarm: YES Trip: YES Reset: NO Current= 9600 A Time= 0.17 sec	SAT
Out	No	B	No	Isd=4, tsd=.1 off	.08 - .14 sec	Alarm: YES Trip: YES Reset: NO Current= 9600 A Time= 0.11 sec	SAT
Out	No	B	No	Isd=4, tsd=0 off	.02 - .08 sec	Alarm: YES Trip: YES Reset: NO Current= 9600 A Time= 0.056 sec	SAT
Out	No	B	No	Isd=5, tsd=.1on	0.14 - 0.3 sec	Alarm: YES Trip: YES Reset: NO Current= 12000 A Time= 0.20 sec	SAT

8000 x 1.5 = 12000

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5/6/04



						Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=5, tsd=.2on	0.28 - 0.48 SEC	Current= 12000 A Time= 0.33 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=5, tsd=.3on	0.45 - 0.72 SEC	Current= 12000 A Time= 0.55 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=5, tsd=.4on	0.58 - 0.95 SEC	Current= 12000 A Time= 0.75 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=5, tsd=.4 off	0.35 - 0.50 SEC	Current= 12000 A Time= 0.42 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=5, tsd=.3 off	0.23 - 0.32 SEC	Current= 12000 A Time= 0.28 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=5, tsd=.2 off	0.14 - 0.20 SEC	Current= 12000 A Time= 0.17 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=5, tsd=.1 off	0.08 - 0.14 SEC	Current= 12000 A Time= 0.11 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=5, tsd=0 off	0.02 - 0.08 SEC	Current= 12000 A Time= 0.55 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=6, tsd=.1on 9600 x 1.5 = 14400	0.10 - 0.20 SEC	Current= 14400 A Time= 0.14 Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=6, tsd=.2on	0.18 - 0.35 SEC	Current= 14400 A Time= 0.21 Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=6, tsd=.3on	0.34 - 0.48 SEC	Current= 14400 A Time= 0.36 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=6, tsd=.4on	0.39 - 0.68 SEC	Current= 14400 A Time= 0.56 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	B	No	Isd=6, tsd=.4 off	0.35 - 0.50 SEC	Current= 14400 A Time= 0.42 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=6, tsd=.3 off	0.23 - 0.32 SEC	Current= 14400 A Time= 0.28 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=6, tsd=.2 off	0.14 - 0.20 SEC	Current= 14400 A Time= 0.18 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=6, tsd=.1 off	0.08 - 0.14 SEC	Current= 14400 A Time= 0.11 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=6, tsd=0 off	0.02 - 0.08 SEC	Current= 14400 A Time= 0.056 SEC Alarm: YES Trip: YES Reset: NO	SAT

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						Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=8, tsd=.1on 12500 x 1.5 = 19200A	0.08 - 0.14 SEC	Current= 19200 A Time= 0.11 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=8, tsd=.2on	0.14 - 0.20 SEC	Current= 19200 A Time= 0.17 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=8, tsd=.3on	0.23 - 0.32 SEC	Current= 19200 A Time= 0.28 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=8, tsd=.4on	0.35 - 0.50 SEC	Current= 19200 A Time= 0.42 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=8, tsd=.4 off	0.35 - 0.50 SEC	Current= 19200 A Time= 0.42 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=8, tsd=.3 off	0.23 - 0.32 SEC	Current= 19200 A Time= 0.28 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=8, tsd=.2 off	0.14 - 0.20 SEC	Current= 19200 A Time= 0.17 SEC Alarm: Trip: Reset: NO	SAT
Out	No	C	No	Isd=8, tsd=.1 off	0.08 - 0.14 SEC	Current= 19200 A Time= 0.11 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=8, tsd=0 off	0.02 - 0.08 SEC	Current= 19200 A Time= 0.055 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=10, tsd=.1on 16000 x 1.5 = 24000	instr. OFF 0.08 - 0.14 SEC	Current= 24000 A Time= 0.11 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=10, tsd=.2on	0.14 - 0.20 SEC	Current= 24000 A Time= 0.17 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Isd=10, tsd=.3on	0.23 - 0.32 SEC	Current= 24000 A Time= 0.28 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	Yes	C	No	Isd=10, tsd=.4on	0.35 - 0.50 SEC	Current= 24000 A Time= 0.42 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	Yes	C	No	Isd=10, tsd=.4 off	0.35 - 0.50 SEC	Current= 24000 A Time= 0.42 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	Yes	C	No	Isd=10, tsd=.3 off	0.23 - 0.32 SEC	Current= 24000 A Time= 0.28 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	Yes	C	No	Isd=10, tsd=.2 off	0.14 - 0.20 SEC	Current= 24000 A Time= 0.17 SEC Alarm: YES Trip: YES Reset: NO	SAT
Out	Yes	C	No	Isd=10, tsd=.1	0.08 - 0.14 SEC	Current= 24000 A Time= 0.11 SEC	SAT

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				off		Alarm: YES Trip: YES Reset: NO	SAT
Out	Yes	C	No	Isd=10, tsd=0 off	0.02-0.08 sec	Current= 24000 A Time= 0.056 sec Alarm: YES Trip: YES Reset: NO	SAT
				Long Time	6.0 P		
Out	No	C	No	Ir=.4, tr=.5	STC 10x .40W INST. C15X G.F. DEFERRED	Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	N/A
Out	No	C	No	Ir=.4, tr=1	N/A	Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	N/A
Out	No	C	No	Ir=.4, tr=2 1250 x 3 = 3840	6.5-9.8 sec	Current= 3840 A Time= 7.6 sec Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Ir=.4, tr=4	N/A	Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	N/A
Out	No	C	No	Ir=.4, tr=8 1250 x 3 = 3840	27-38 sec	Current= 3840 A Time= 30.7 Alarm: YES Trip: YES Reset: NO	SAT
Out	No	C	No	Ir=.4, tr=12	N/A	Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	N/A
Out	No	C	No	Ir=.4, tr=16		Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	
Out	No	C	No	Ir=.4, tr=20		Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	
Out	No	C	No	Ir=.4, tr=24		Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	
Out	No	B	No	Ir=.45, tr=.5		Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	
Out	No	B	No	Ir=.45, tr=1		Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	
Out	No	B	No	Ir=.45, tr=2		Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	
Out	No	B	No	Ir=.45, tr=4		Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	
Out	No	B	No	Ir=.45, tr=8		Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	
Out	No	B	No	Ir=.45, tr=12		Current= _____ Time= _____ Alarm: _____ Trip: _____ Reset: _____	



B.23

N/A - This testing was not performed on this trip unit.  
This testing was performed on a separate trip unit (data sheets follow). AS 5/7/09

						Alarm:	Trip:	Reset:	
Out	No	B	No	Ir=.45, tr=16	nk	Current=	Trip:	Time=	NA
Out	No	B	No	Ir=.45, tr=20		Alarm:	Trip:	Reset:	
Out	No	B	Yes	Ir=.45, tr=24		Current=	Trip:	Time=	
Out	No	B	Yes	Ir=.5, tr=.5		Alarm:	Trip:	Reset:	
Out	No	B	Yes	Ir=.5, tr=1		Current=	Trip:	Time=	
Out	No	B	Yes	Ir=.5, tr=2 1600 x 3 = 4800	6.5-9.8 SEC	Alarm: YES	Trip: YES	Reset: YES	SAT
Out	No	B	Yes	Ir=.5, tr=4	nk	Current=	Trip:	Time=	nk
Out	No	B	Yes	Ir=.5, tr=8		Alarm:	Trip:	Reset:	
Out	No	B	No	Ir=.5, tr=12		Current=	Trip:	Time=	
Out	No	B	No	Ir=.5, tr=16 1600 x 3 = 4800	41-62 SEC	Alarm: YES	Trip: YES	Reset: NO	SAT
Out	No	B	No	Ir=.5, tr=20	nk	Current=	Trip:	Time=	nk
Out	No	B	No	Ir=.5, tr=24		Alarm:	Trip:	Reset:	
Out	No	B	No	Ir=.6, tr=.5		Current=	Trip:	Time=	
Out	No	B	No	Ir=.6, tr=1		Alarm:	Trip:	Reset:	
Out	No	B	No	Ir=.6, tr=2		Current=	Trip:	Time=	
Out	No	B	No	Ir=.6, tr=4		Alarm:	Trip:	Reset:	
Out	No	B	No	Ir=.6, tr=8		Current=	Trip:	Time=	

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5/6/04

B.24

Out	No	B	No	Ir=.6, tr=12		Alarm: _____	Trip: _____	Reset: _____	N/A	
Out	No	B	No	Ir=.6, tr=12	N/A	Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	B	No	Ir=.6, tr=16		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	B	No	Ir=.6, tr=20		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	B	No	Ir=.6, tr=24		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.63, tr=.5		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.63, tr=1		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.63, tr=2		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.63, tr=4		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.63, tr=8		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.63, tr=12		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.63, tr=16		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.63, tr=20		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.63, tr=24		Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.7, tr=.5	↓	Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.7, tr=1 2240 x 3 = 6720	3.3- 5 SEC	Current= <u>6720 A</u>	Time= <u>4.2 sec</u>	Alarm: <u>YES</u>	Trip: <u>YES</u>	Reset: <u>NO</u>
Out	No	A	No	Ir=.7, tr=2	N/A	Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____
Out	No	A	No	Ir=.7, tr=4	↓	Current= _____	Time= _____	Alarm: _____	Trip: _____	Reset: _____

B.25

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5/6/04

					N/A	Alarm: _____	Trip: _____	Reset: _____	N/A
Out	No	A	No	I <sub>r</sub> =.7, t <sub>r</sub> =8		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.7, t <sub>r</sub> =12		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.7, t <sub>r</sub> =16		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.7, t <sub>r</sub> =20		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.7, t <sub>r</sub> =24		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.8, t <sub>r</sub> =.5		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.8, t <sub>r</sub> =1		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.8, t <sub>r</sub> =2		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.8, t <sub>r</sub> =4		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.8, t <sub>r</sub> =8		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.8, t <sub>r</sub> =12		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.8, t <sub>r</sub> =16		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.8, t <sub>r</sub> =20		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.8, t <sub>r</sub> =24		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.9, t <sub>r</sub> =.5		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.9, t <sub>r</sub> =1		Current= _____	Time= _____		
						Alarm: _____	Trip: _____	Reset: _____	
Out	No	A	No	I <sub>r</sub> =.9, t <sub>r</sub> =2		Current= _____	Time= _____		

B.26

						Alarm:	Trip:	Reset:		
Out	No	A	No	Ir=.9, tr=4		Current=	_____	Time=	_____	n/a
Out	No	A	No	Ir=.9, tr=8		Alarm:	Trip:	Reset:	_____	
Out	No	A	No	Ir=.9, tr=12		Current=	_____	Time=	_____	
Out	No	A	No	Ir=.9, tr=16		Alarm:	Trip:	Reset:	_____	
Out	No	A	No	Ir=.9, tr=20		Current=	_____	Time=	_____	
Out	No	A	No	Ir=.9, tr=24		Alarm:	Trip:	Reset:	_____	
Out	No	A	No	Ir=1, tr=.5		Current=	_____	Time=	_____	
Out	No	A	No	Ir=1, tr=1		Alarm:	Trip:	Reset:	_____	
Out	No	A	No	Ir=1, tr=2		Current=	_____	Time=	_____	
Out	No	A	No	Ir=1, tr=4		Alarm:	Trip:	Reset:	_____	
Out	Yes	A	No	Ir=1, tr=8		Current=	_____	Time=	_____	
Out	Yes	A	No	Ir=1, tr=12	ST. 10x .40N WST. 15x GF. 0.25mm-10 3200x3 = 9600 39-52 SEC	Current=	9600	Time=	51.3	SAT
Out	Yes	A	No	Ir=1, tr=16		Alarm:	YES Trip: YES	Reset:	YES	
Out	Yes	A	No	Ir=1, tr=20	n/a	Current=	_____	Time=	_____	n/a
Out	Yes	A	No	Ir=1, tr=24		Alarm:	Trip:	Reset:	_____	
Out	Yes	A	No	Ir=1, tr=24		Current=	_____	Time=	_____	
						Alarm:	Trip:	Reset:	_____	



B.21

Check off appropriate test:

TEST DATA SHEET  PRE-SEISMIC  POST-SEISMIC  DEDICATION  OTHER \_\_\_\_\_

TEST DATA FOR: ~~VTP~~ VVTP-042181-1 Rev.1

Item Description Masolact NW WITH Micrologic 6.0P + 3.0 WETS Manufacturer/Vendor: SQUINE D Model/Part No. NW 32 H2

Provide Summary of Test Results.

Check appropriate boxes:  
 All Items Passed. Discrepancy Report(s): If yes, identify below:  Yes  No  N/A  
 List S/N or ID Passed below. Qty passed: \_\_\_\_\_

S/Ns or ID#	CC#	DR#	<input type="checkbox"/> Acceptable	<input type="checkbox"/> Not Acceptable	Initials/Date by PE:
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____

OTHER (where applicable)

Record all M&TE used:

NLI MTE#	M&TE	CAL. DUE DATE	NLI MTE#	M&TE	CAL. DUE DATE
<u>562</u>	<u>TEST SET</u>	<u>7/9/04</u>			
<u>553</u>	<u>Power Supply</u>	<u>N/A</u>			
<u>283</u>	<u>Fluke F7 V</u>	<u>12/26/04</u>			

Update M&TE log on computer Jan 5/6/04  
 Initials & Date

NOTES:

Performed by: JDH Date 5/6/04  
 Verified by: [Signature] Date 5/7/2004  
 Approved by: [Signature] Date 5/7/04

B.28

NOTE: Initial and date after performance of each CC#. Indicate Pass or Fail.

**Validation Test Plan for Square D/Schneider Micrologic Programmer**  
**VVTP-042181-1, revision 0**  
**Attachment I**

**Data Recording**

Record the following data, as applicable:

- Programmer model and s/n.
- Programmer code name and revision.
- Breaker model and s/n.
- Rating plug model and size.

Micrologic 3.0 P/N: 5131A  
LI 13.0  
Masterpact NW 32H2 S/N: 060638110101  
3200 AMP P/N: 11125-E  
ON Box 48816

**PERFORM CC#3, 4, 5A, 5B AFTER THE OTHER CC'S ARE COMPLETED.**

**CC#1, #1A to 1E, #2, #6, #7, #8**

**PRIMARY INJECTION TESTING**

- **Objective.** The purpose of this testing is as follows:
  - (CC#1) Test some combinations of switch settings on the trip unit.
  - (C#1A) Programmer operates on Square D Masterpact NT or NW breaker.
  - (CC#1B) Programmer operates per design with the rating plug installed.
  - (CC#1C) Output alarms are per design.
  - (CC#1D) Remote communications, alarms and interlocks do not impact trip unit operation.
  - (CC#1E) No spurious tripping.
  - (CC#1F) Programmer trips per curve with and without reset.
  - (CC#2) Test to verify that loss of power will not impact the trip unit settings.
  - (CC#6) Test to verify that battery removal or a dead battery will not impact the trip unit safety function.
  - (CC#7) Verify that recalling information from memory will not impact the trip unit safety function.
  - (CC#8) Verify that secondary injection testing does not impact the settings or trip unit function.
  - Primary injection testing of the defeat functions is tested separately in CC#9.
- **Initial Conditions**
  - Programmer installed on the NT or NW breaker.
  - Primary power to the bus and trip unit powered.
- **Test Sequence-Primary Injection**
  - Perform secondary injection testing and record the results (the purpose of this step is to verify CC#8). Record trip settings, trip time, and SAT/UNSAT:
    - Instantaneous test #1: \_\_\_\_\_
    - Instantaneous test #2: \_\_\_\_\_
    - Short time test #1: \_\_\_\_\_
    - Short time test #2: \_\_\_\_\_
    - Long time test #1: \_\_\_\_\_

M/A      AS 5/7/04

				off		Alarm:	Trip:	Reset:	
Out	Yes	C	No	Isd=10, tsd=0 off		Current= _____	Time= _____		
				Long Time		Alarm: _____	Trip: _____	Reset: _____	
Out	No	C	No	Ir=.4, tr=.5 1.3sec - 2.3sec	Microlastic 3.0	Current= <u>3840 A</u>	Time= <u>1.5 sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	C	No	Ir=.4, tr=1 3sec - 4.5sec.	INSTANTANEOUS SET AT 12X FOR	Current= <u>3840 A</u>	Time= <u>3.75sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	C	No	Ir=.4, tr=2 6.2sec - 9sec	Long Time Testing	Current= <u>3840 A</u>	Time= <u>7.0 sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	C	No	Ir=.4, tr=4 13sec - 20sec		Current= <u>3840 A</u>	Time= <u>14.29sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	C	No	Ir=.4, tr=8 25sec - 37sec		Current= <u>3840 A</u>	Time= <u>29.26sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	C	No	Ir=.4, tr=12 41sec - 51sec		Current= <u>3840 A</u>	Time= <u>43.71sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	C	No	Ir=.4, tr=16 52- 63 sec.		Current= <u>3840 A</u>	Time= <u>58.54sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	C	No	Ir=.4, tr=20 65- 83 sec		Current= <u>3840 A</u>	Time= <u>70.77sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	C	No	Ir=.4, tr=24 83- 125 sec.		Current= <u>3840 A</u>	Time= <u>85.34sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	B	No	Ir=.45, tr=.5 1.3sec - 2.3sec		Current= <u>4320 A</u>	Time= <u>1.86sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	B	No	Ir=.45, tr=1 3sec - 4.5sec		Current= <u>4320 A</u>	Time= <u>3.85</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	B	No	Ir=.45, tr=2 6.2sec - 9sec.		Current= <u>4320 A</u>	Time= <u>7.2sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	B	No	Ir=.45, tr=4 13sec - 20sec.		Current= <u>4320 A</u>	Time= <u>15.02sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	B	No	Ir=.45, tr=8 25sec - 37sec.		Current= <u>4320 A</u>	Time= <u>29.11sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat
Out	No	B	No	Ir=.45, tr=12 41sec - 51sec.		Current= <u>4320 A</u>	Time= <u>43.44sec</u>	Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	Sat



Page 2 of 7

B.30

						Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.45, tr=16 52 sec - 63 sec.	Micro Logic 3.0	Current= <u>4320A</u> Time= <u>59.83sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.45, tr=20 65 sec - 83 sec.		Current= <u>4320A</u> Time= <u>72.32sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	Yes	I <sub>r</sub> =.45, tr=24 93 sec - 125 sec.		Current= <u>4320A</u> Time= <u>86.83sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	Yes	I <sub>r</sub> =.5, tr=.5 1.3 sec - 2.3 sec.		Current= <u>4800A</u> Time= <u>1.88sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	Yes	I <sub>r</sub> =.5, tr=1 3 sec. - 4.5 sec.		Current= <u>4800A</u> Time= <u>3.77sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	Yes	I <sub>r</sub> =.5, tr=2 6.2 sec - 9 sec.		Current= <u>4800A</u> Time= <u>7.10sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	Yes	I <sub>r</sub> =.5, tr=4 13 sec. - 20 sec.		Current= <u>4800A</u> Time= <u>14.39sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	Yes	I <sub>r</sub> =.5, tr=8 25 sec - 37 sec.		Current= <u>4800A</u> Time= <u>29.19sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.5, tr=12 41 sec - 51 sec.		Current= <u>4800A</u> Time= <u>43.22sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.5, tr=16 52 sec. - 63 sec.		Current= <u>4800A</u> Time= <u>57.72sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.5, tr=20 65 sec. - 83 sec.		Current= <u>4800A</u> Time= <u>72.14sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.5, tr=24 83 sec. - 125 sec.		Current= <u>4800A</u> Time= <u>86.55sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.6, tr=.5 1.3 sec. - 2.3 sec.		Current= <u>5760A</u> Time= <u>1.74sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.6, tr=1 3 sec. - 4.5 sec.		Current= <u>5760A</u> Time= <u>3.8sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.6, tr=2 6.2 sec - 9 sec.		Current= <u>5760A</u> Time= <u>7.5sec.</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.6, tr=4 13 sec. - 20 sec.		Current= <u>5760A</u> Time= <u>14.87sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> SAT
Out	No	B	No	I <sub>r</sub> =.6, tr=8 25 sec - 37 sec.		Current= <u>5760A</u> Time= <u>29.74sec</u> SAT

Page 3 of 7

13.31

Pass  
TDM 5/7/04

						Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	B	No	Ir=.6, tr=12 41sec - 51sec	Micrologic 3.0	Current= <u>5760A</u> Time= <u>47.22sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	B	No	Ir=.6, tr=16 52sec - 63sec.		Current= <u>5760A</u> Time= <u>57.70sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	B	No	Ir=.6, tr=20 65sec - 83sec		Current= <u>5760A</u> Time= <u>72.06sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	B	No	Ir=.6, tr=24 83sec - 125sec.		Current= <u>5760A</u> Time= <u>86.54</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.63, tr=.5 1.3sec - 2.3sec		Current= <u>6048A</u> Time= <u>1.4sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.63, tr=1 3sec. - 4.5sec.		Current= <u>6048A</u> Time= <u>3.6sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.63, tr=2 6.2sec - 9sec.		Current= <u>6048A</u> Time= <u>7.59sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.63, tr=4 13sec - 20sec.		Current= <u>6048A</u> Time= <u>15.13sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.63, tr=8 26sec - 37sec.		Current= <u>6048A</u> Time= <u>29.24</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.63, tr=12 41sec - 51sec.		Current= <u>6048A</u> Time= <u>45.44sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.63, tr=16 52sec - 63sec.		Current= <u>6048A</u> Time= <u>60.64sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.63, tr=20 65sec. - 83sec.		Current= <u>6048A</u> Time= <u>75.84sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.63, tr=24 83sec - 125sec.		Current= <u>6048A</u> Time= <u>90.60sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.7, tr=.5 1.3 - 2.3 sec		Current= <u>6720A</u> Time= <u>1.5sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.7, tr=1 3 - 4.5 sec		Current= <u>6720A</u> Time= <u>3.6sec.</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.7, tr=2 6.2 - 9 sec		Current= <u>6720A</u> Time= <u>7.69sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.7, tr=4 13 - 20 sec.		Current= <u>6720A</u> Time= <u>14.49sec</u>	SAT

Page 5 of 7

3.32

TDM Pass 5/7/04

						Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.7, tr=8 25-37 sec.	MicroLogic 3-0	Current= <u>6720A</u> Time= <u>29.77sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.7, tr=12 41-51 sec.		Current= <u>6720A</u> Time= <u>42.21sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.7, tr=16 52-63 sec.		Current= <u>6720A</u> Time= <u>59.62sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.7, tr=20 65-83 sec.		Current= <u>6720A</u> Time= <u>74.56sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.7, tr=24 83-125 sec.		Current= <u>6720A</u> Time= <u>89.49sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.8, tr=.5 1.3-2.3 sec.		Current= <u>7680A</u> Time= <u>1.8sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.8, tr=1 3-4.5 sec.		Current= <u>7680A</u> Time= <u>3.6sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.8, tr=2 6.2-9 sec.		Current= <u>7680A</u> Time= <u>7.4sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.8, tr=4 13-20 sec.		Current= <u>7680A</u> Time= <u>14.87sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.8, tr=8 25-37 sec.		Current= <u>7680A</u> Time= <u>29.76sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.8, tr=12 41-51 sec.		Current= <u>7680A</u> Time= <u>46.07sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.8, tr=16 52-63 sec.		Current= <u>7680A</u> Time= <u>59.63sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.8, tr=20 65-83 sec.		Current= <u>7680A</u> Time= <u>77.00</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.8, tr=24 83-125 sec.		Current= <u>7680A</u> Time= <u>92.41sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.9, tr=.5 1.3-2.3 sec.		Current= <u>8640A</u> Time= <u>1.9sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.9, tr=1 3-4.5 sec.		Current= <u>8640A</u> Time= <u>3.8sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u>	SAT
Out	No	A	No	Ir=.9, tr=2 6.2-9 sec.		Current= <u>8640A</u> Time= <u>7.42sec</u>	SAT

Pass  
TDM 5/7/04

Page 5 of 7

B33

						Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=.9, tr=4 13-20 sec.	Microlagic 3.0	Current= <u>8640A</u> Time= <u>15.35sec.</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=.9, tr=8 25-37 sec.		Current= <u>8640A</u> Time= <u>30.77sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=.9, tr=12 41-51 sec.		Current= <u>8640A</u> Time= <u>44.69sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=.9, tr=16 52-63 sec.		Current= <u>8640A</u> Time= <u>61.27sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=.9, tr=20 65-83 sec.		Current= <u>8640A</u> Time= <u>76.85sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=.9, tr=24 83-125 sec.		Current= <u>8640A</u> Time= <u>92.45sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=1, tr=.5 1.3-2.3 sec.		Current= <u>9600A</u> Time= <u>1.8 sec.</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=1, tr=1 3-4.5 sec.		Current= <u>9600A</u> Time= <u>3.82 sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=1, tr=2 6.2-9 sec.		Current= <u>9600A</u> Time= <u>7.6 sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	No	A	No	Ir=1, tr=4 13-20 sec.		Current= <u>9600A</u> Time= <u>14.85sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	Yes	A	No	Ir=1, tr=8 25-37 sec.		Current= <u>9600A</u> Time= <u>29.76sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	Yes	A	No	Ir=1, tr=12 41-51 sec.		Current= <u>9600A</u> Time= <u>44.59sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	Yes	A	No	Ir=1, tr=16 52-63 sec.		Current= <u>9600A</u> Time= <u>61.48sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	Yes	A	No	Ir=1, tr=20 65-83 sec.		Current= <u>9600A</u> Time= <u>74.43sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat
Out	Yes	A	No	Ir=1, tr=24 83-125 sec.		Current= <u>9600A</u> Time= <u>92.45sec</u> Alarm: <u>yes</u> Trip: <u>yes</u> Reset: <u>yes</u> Sat



Pass  
5/2/04

Check off appropriate test:

TEST DATA SHEET  PRE-SEISMIC  POST-SEISMIC  DEDICATION  OTHER \_\_\_\_\_

TEST DATA FOR: VP-VVTP-042181-1, Rev. 1

Item Description Mastepact NW with Micrologic 3.0 Trip Unit Manufacturer/Vendor: Square D Model/Part No. NW32H2

Provide Summary of Test Results.

Check appropriate boxes:  
 All Items Passed. Discrepancy Report(s): If yes, identify below:  Yes  No  N/A  
 List S/N or ID Passed below. Qty passed: \_\_\_\_\_  
Micrologic 3.0 Trip Unit R/P/N: 5131A  
5/7/04

S/Ns or ID#	CC#	DR#	<input type="checkbox"/> Acceptable	<input type="checkbox"/> Not Acceptable	Initials/Date by PE:
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____
_____	_____	_____	<input type="checkbox"/>	<input type="checkbox"/>	_____

OTHER (where applicable)

Record all M&TE used:

NLI MTE#	M&TE	CAL. DUE DATE	NLI MTE#	M&TE	CAL. DUE DATE
<u>562</u>	<u>Breaker Test Set</u>	<u>7/9/04</u>			

Update M&TE log on computer T.M. 5/7/04  
 Initials & Date

NOTES:

Performed by: Tracy Muff  Date 5/7/04  
 Verified by: [Signature] Date 5/7/2004  
 Approved by: [Signature] Date 5/7/04

NOTE: Initial and date after performance of each CC#. Indicate Pass or Fail.

Page 7 of 7

B.35

ALL NUMBERS PRESENT ON BACK OF PROGRAMMER

MicroLogic 3.0 CAT# 5131A ARE AS FOLLOWS:

BAR CODE STICKER TOP: 00033548814

BAR CODE STICKER BOTTOM: MicroLogic 3.0 5100511360

P00335 48814 0026490

ALL NUMBERS PRESENT ON BACK OF PROGRAMMER

MicroLogic 6.0P CAT# 5164A ARE AS FOLLOWS:

BAR CODE STICKER TOP: 00409347059

BAR CODE STICKER BOTTOM: MicroLogic 6.0P 5100511370

P04093 47059 0388119

**MASTERPACT® NT/NW Universal Power Circuit Breakers**  
**Section 7: Trip Curves**

**SECTION 7: TRIP CURVES**

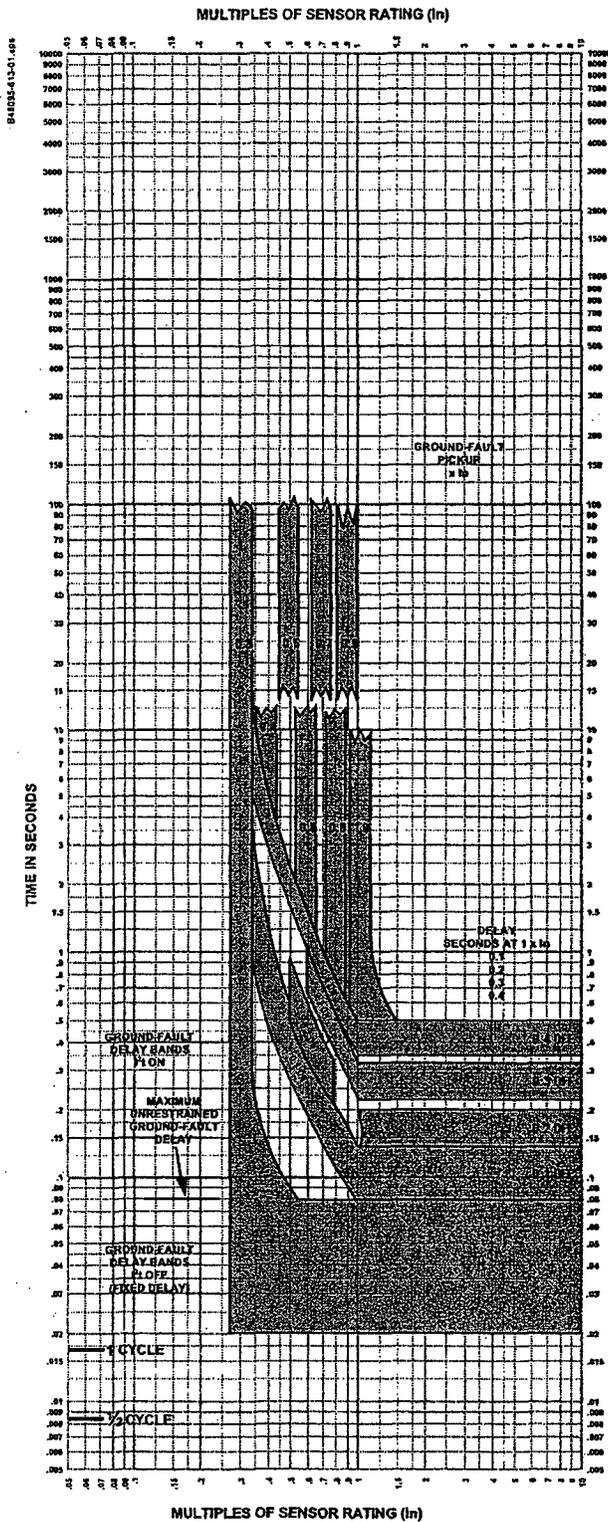
	Page
<b>MICROLOGIC 6.0 A/P/H TRIP UNIT</b>	
<b>WITH ADJUSTABLE GROUND-FAULT PICKUP AND DELAY</b>	
Ground Fault I <sup>2</sup> t OFF and ON, I <sub>n</sub> ≤ 400 A .....	144
Ground Fault I <sup>2</sup> t OFF and ON, 400 A < I <sub>n</sub> ≤ 1200 A .....	145
Ground Fault I <sup>2</sup> t OFF and ON, I <sub>n</sub> > 1200 A .....	146
<b>MICROLOGIC 5.0/6.0 A/P/H TRIP UNIT</b>	
Long-time Pickup and Delay, Short-time Pickup, and I <sup>2</sup> t OFF Delay .....	147
Short-time Pickup and I <sup>2</sup> t ON Delay .....	148
<b>MICROLOGIC 3.0A TRIP UNIT</b>	
Long-time Pickup and Delay .....	149
<b>MICROLOGIC 5.0/6.0 A/P/H TRIP UNIT</b>	
Instantaneous Pickup, 2X to 15X and OFF .....	150
<b>MICROLOGIC 3.0A TRIP UNIT</b>	
Instantaneous Pickup, 1.5X to 12X .....	151
<b>MICROLOGIC 2.0A TRIP UNIT</b>	
Long-time Pickup and Delay, Short-time Pickup with No Delay .....	152
<b>MICROLOGIC 2.0/3.0/5.0/6.0 A/P/H TRIP UNIT</b>	
Instantaneous Override Values .....	153



# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves

**MICROLOGIC 6.0 A/P/H Trip Units**  
**with Adjustable Ground-fault Pickup and Delay**  
**Characteristic Trip Curve No. 613-1**  
**Ground Fault I<sup>2</sup>t OFF and ON**  
**I<sub>n</sub> ≤ 400 A**



The time-current curve information is to be used for application and coordination purposes only.  
 Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

Curve No. 0613TC0001  
 Drawing No. 040095-613-01



# MASTERPACT® NT/NW Universal Power Circuit Breakers

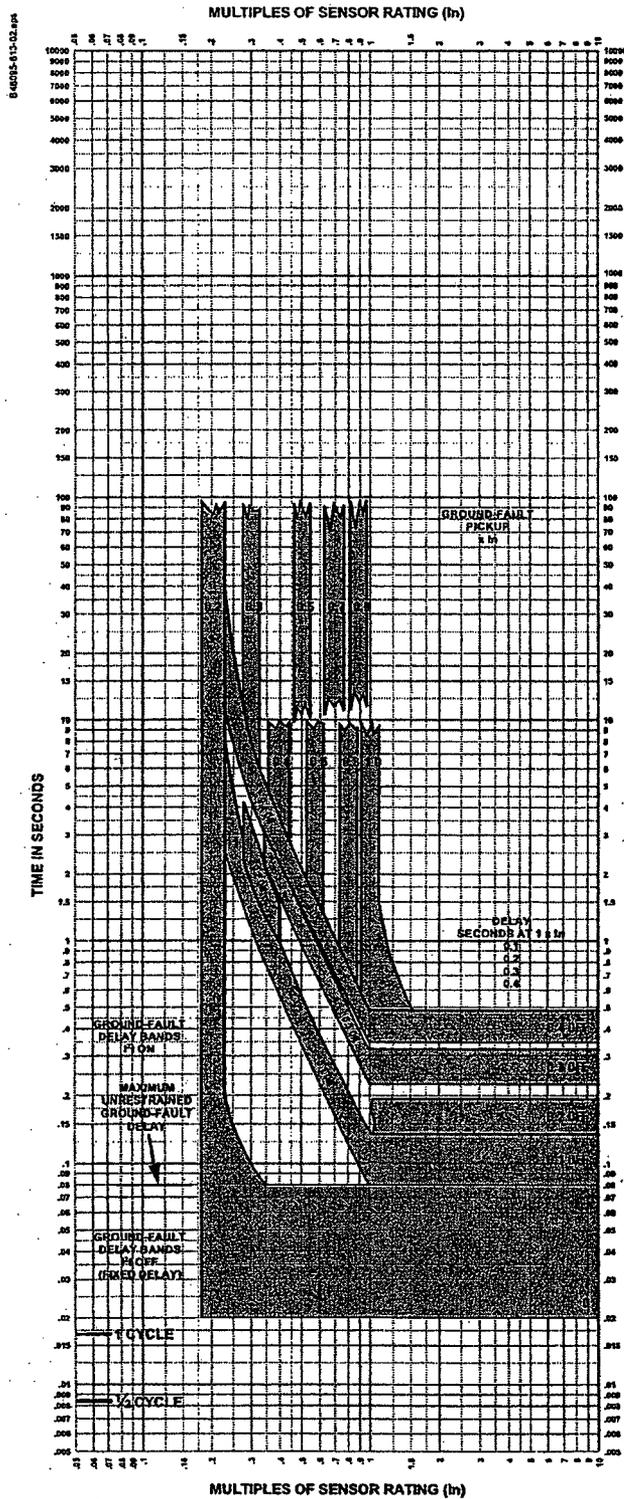
## Section 7: Trip Curves

**MICROLOGIC 6.0 A/P/H Trip Units  
with Adjustable Ground-fault Pickup and Delay**

Characteristic Trip Curve No. 613-2

Ground Fault I<sub>2t</sub> OFF and ON

400 A < I<sub>n</sub> ≤ 1200 A



The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

Curve No. 0613TC0002  
Drawing No. B48095-613-02



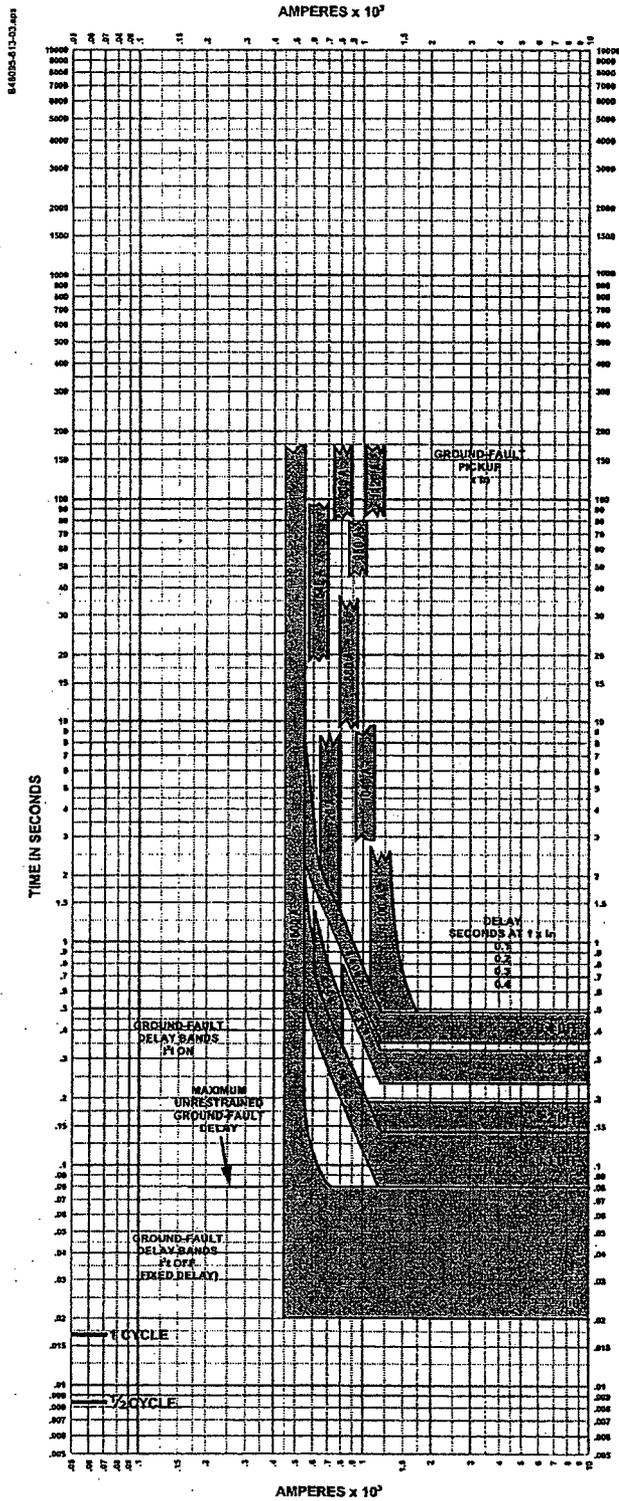
**MASTERPACT® NT/NW Universal Power Circuit Breakers**  
**Section 7: Trip Curves**

**MICROLOGIC 6.0 A/P/H Trip Units**  
**with Adjustable Ground-fault Pickup and Delay**

**Characteristic Trip Curve No. 613-3**

**Ground Fault I<sup>2</sup>t OFF and ON**

**I<sub>n</sub> > 1200 A**



The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

Curve No. 0613TC0003  
 Drawing No. B45095-613-03



B.40

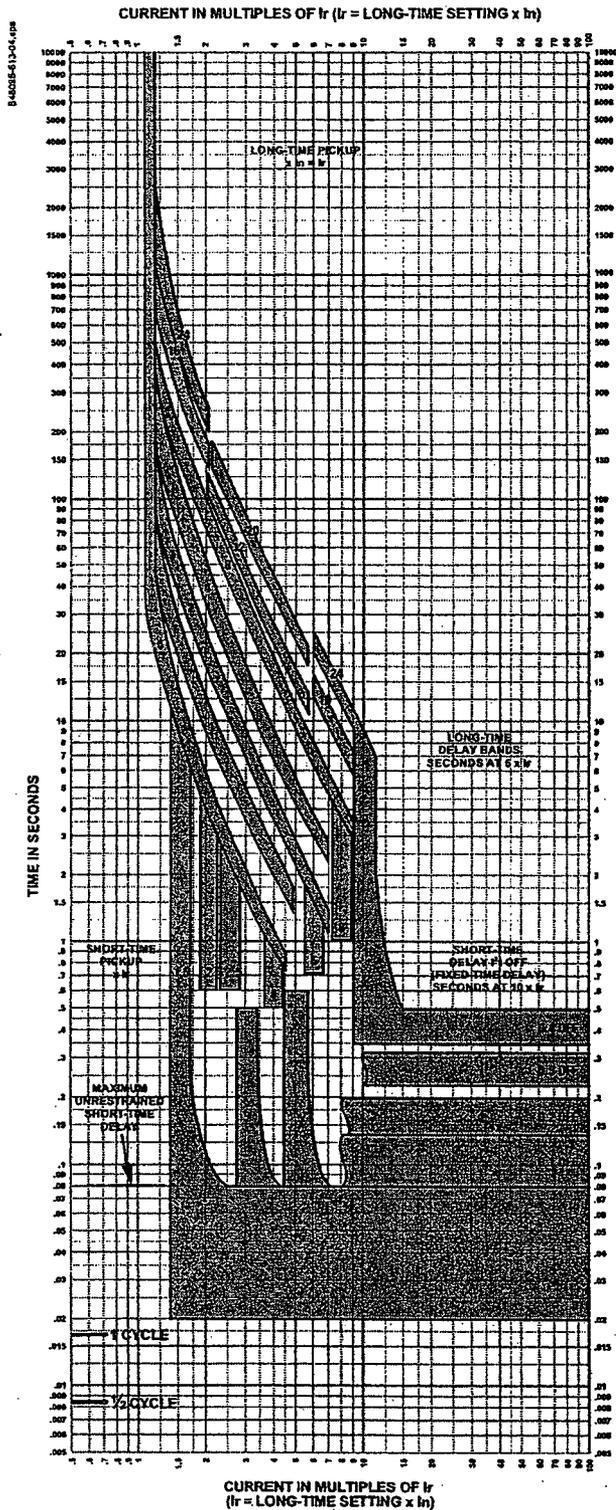
# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves

### MICROLOGIC 5.0/6.0 A/P/H Trip Units

Characteristic Trip Curve No. 613-4

**Long-time Pickup and Delay**  
**Short-time Pickup and I<sup>2</sup>t OFF Delay**



The time-current curve information is to be used for application and coordination purposes only.  
Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

**Notes:**

1. There is a thermal-imaging effect that can act to shorten the long-time delay. The thermal-imaging effect comes into play if a current above the long-time delay pickup value exists for a time and then is cleared by the tripping of a downstream device or the circuit breaker itself. A subsequent overload will cause the circuit breaker to trip in a shorter time than normal. The amount of time delay reduction is inverse to the amount of time that has elapsed since the previous overload. Approximately twenty minutes is required between overloads to completely reset thermal-imaging.
2. The end of the curve is determined by the interrupting rating of the circuit breaker.
3. With zone-selective interlocking ON, short-time delay utilized, and no restraining signal, the maximum unrestrained short-time delay time band applies regardless of the setting.
4. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of the current.
5. For a withstand circuit breaker, instantaneous can be turned OFF. See trip curve 613-7 on page 150 for instantaneous trip curve. See trip curve 613-10 on page 153 for instantaneous override values.
6. Overload indicator illuminates at 100%.

Curve No. 0613TC0004  
Drawing No. 048095-613-04



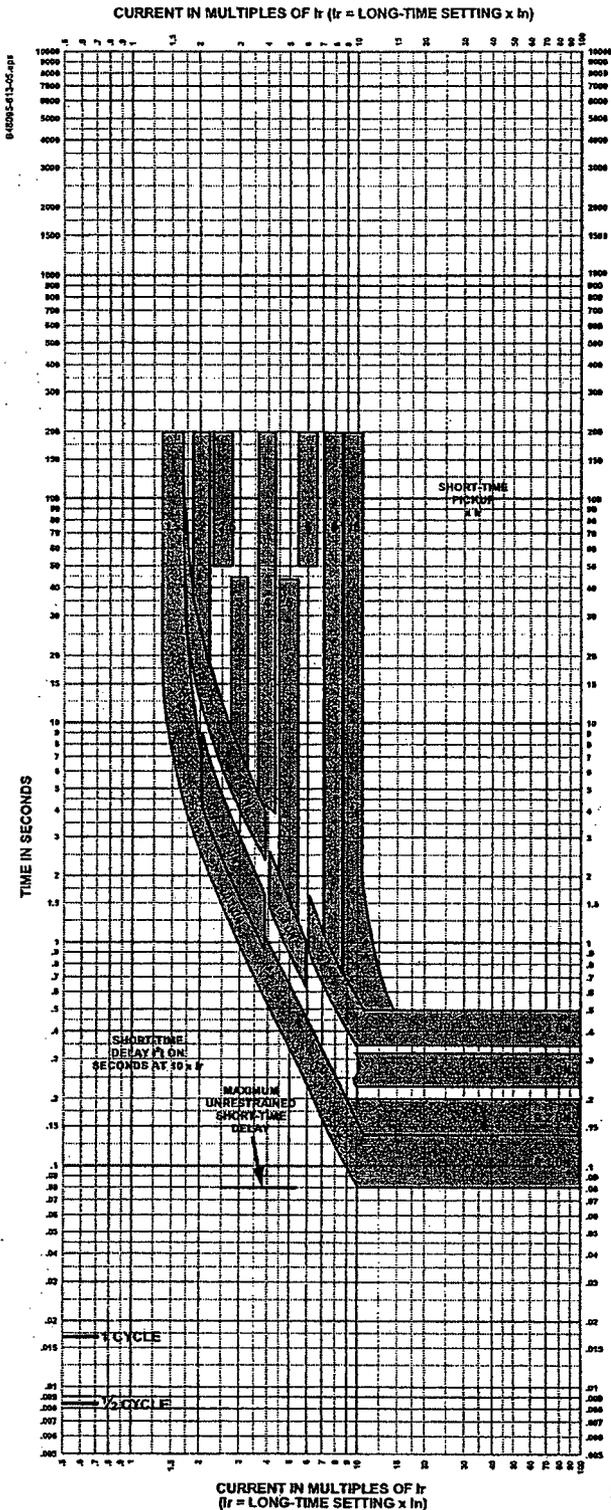
B.41

**MASTERPACT® NT/NW Universal Power Circuit Breakers**  
**Section 7: Trip Curves**

**MICROLOGIC 5.0/6.0 A/P/H Trip Units**

Characteristic Trip Curve No. 613-5

Short-time Pickup and I<sup>2</sup>t ON Delay



The time-current curve information is to be used for application and coordination purposes only.  
 Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

**Notes:**

1. There is a thermal-imaging effect that can act to shorten the long-time delay. The thermal-imaging effect comes into play if a current above the long-time delay pickup value exists for a time and then is cleared by the tripping of a downstream device or the circuit breaker itself. A subsequent overload will cause the circuit breaker to trip in a shorter time than normal. The amount of time delay reduction is inverse to the amount of time that has elapsed since the previous overload. Approximately twenty minutes is required between overloads to completely reset thermal-imaging.
2. The end of the curve is determined by the interrupting rating of the circuit breaker.
3. With zone-selective interlocking ON, short-time delay utilized, and no restraining signal, the maximum unrestrained short-time delay time band applies regardless of the setting.
4. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of current.
5. For withstand circuit breaker, instantaneous can be turned OFF. See trip curve 613-7 on page 150 for instantaneous trip curve. See trip curve 613-10 on page 153 for instantaneous override values.
6. See Trip Curve 613-4 on page 147 for long-time pickup and delay trip curve.

CURRENT IN MULTIPLES OF I<sub>r</sub>  
 (I<sub>r</sub> = LONG-TIME SETTING x I<sub>n</sub>)

Curve No. 0613TC0005  
 Drawing No. 648095-613-05

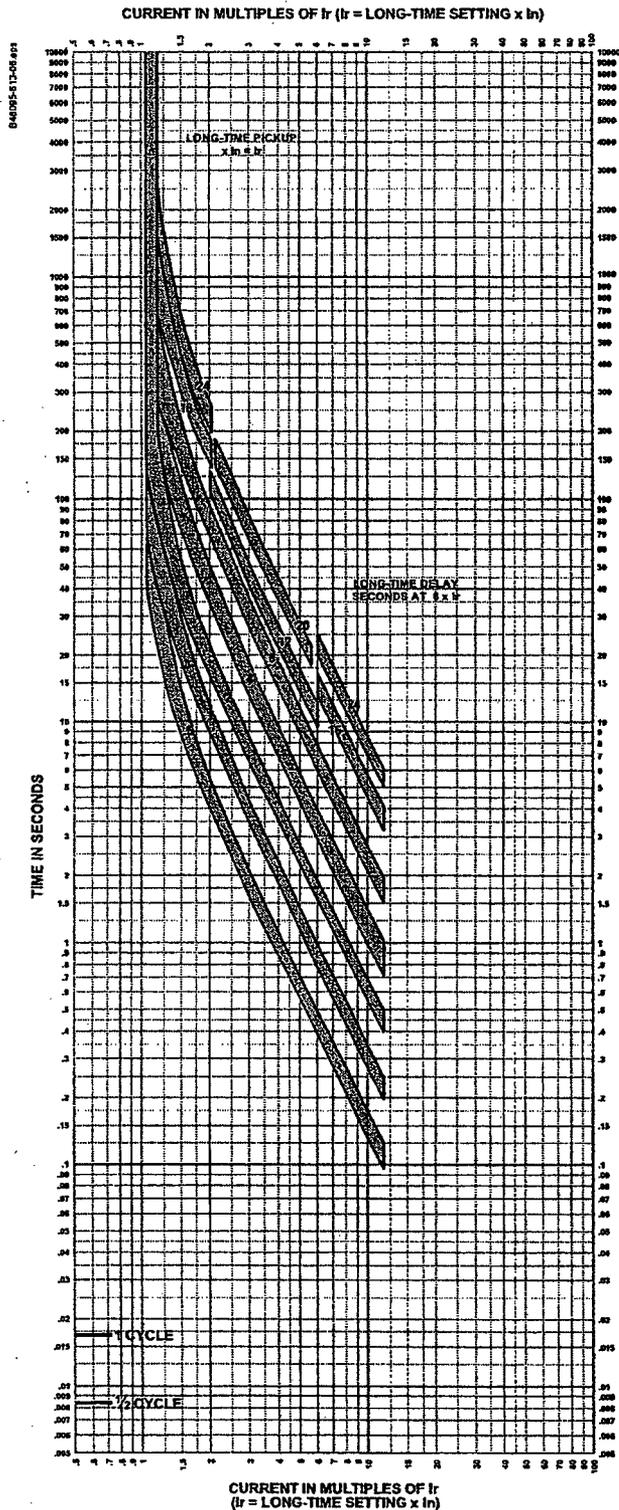


B.42

# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves

### MICROLOGIC 3.0A Trip Unit Characteristic Trip Curve No. 613-6 Long-time Pickup and Delay



The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

**Notes:**

1. There is a thermal-imaging effect that can act to shorten the long-time delay. The thermal-imaging effect comes into play if a current above the long-time delay pickup value exists for a time and then is cleared by the tripping of a downstream device or the circuit breaker itself. A subsequent overload will cause the circuit breaker to trip in a shorter time than normal. The amount of time delay reduction is inverse to the amount of time that has elapsed since the previous overload. Approximately twenty minutes is required between overloads to completely reset thermal-imaging.
2. The end of the curve is determined by the instantaneous setting of the circuit breaker.
3. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of current.
4. See trip curve 613-8 on page 151 for instantaneous pickup trip curve.

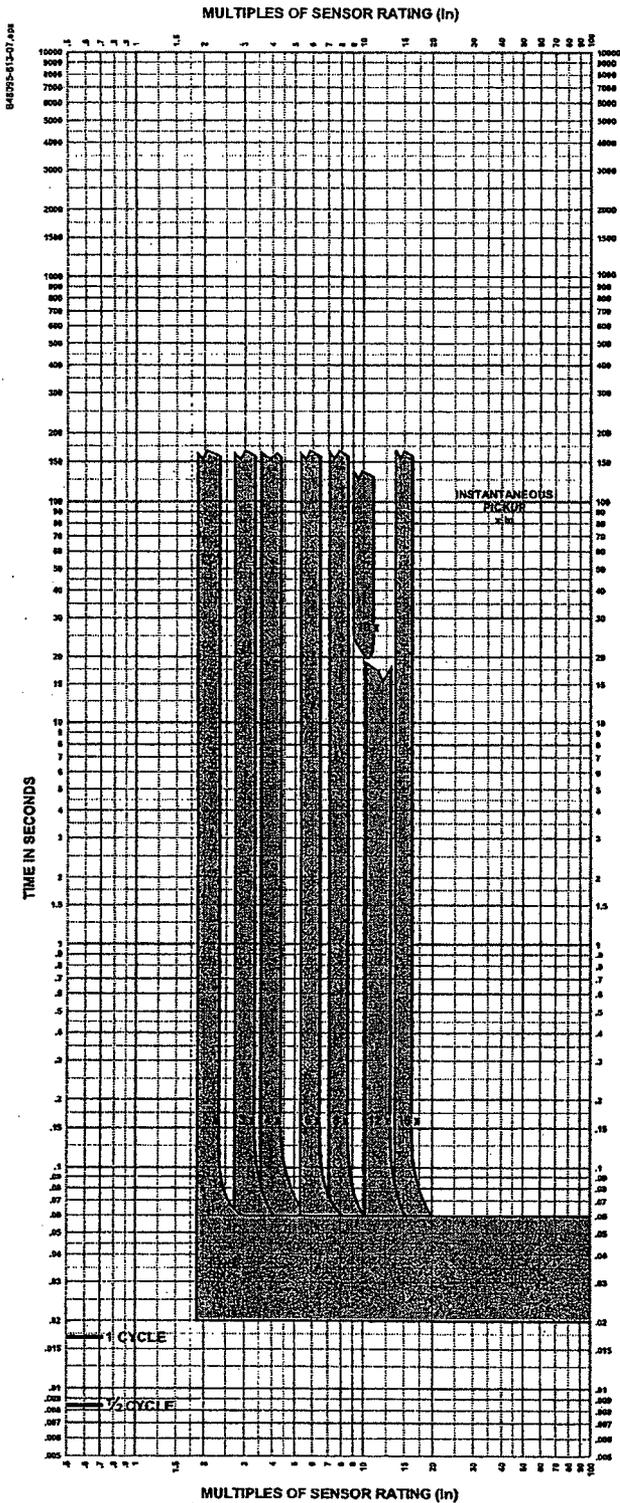


**MASTERPACT® NT/NW Universal Power Circuit Breakers**  
**Section 7: Trip Curves**

**MICROLOGIC 5.0/6.0 Trip Units**

Characteristic Trip Curve No. 613-7

**Instantaneous Pickup, 2X to 15X and OFF**



The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

**Notes:**

1. The end of the curve is determined by the interrupting rating of the circuit breaker.
2. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of current.
3. The instantaneous region of the trip curve shows maximum total clearing times. Actual clearing times in this region can vary depending on the circuit breaker mechanism design and other factors. The actual clearing time can be considerably faster than indicated. Contact your local sales office for additional information.
4. For a withstand circuit breaker, instantaneous can be turned OFF. See trip curve 613-7 on page 150 for the instantaneous trip curve. See trip curve 613-10 on page 153 for the instantaneous override values.
5. See trip curve 613-4 on page 147 and trip curve 613-5 on page 148 for long-time pickup, long-time delay, short-time pickup and short-time delay trip curves.

Curve No. 0613TC0007  
 Drawing No. B46095-613-07



B.44

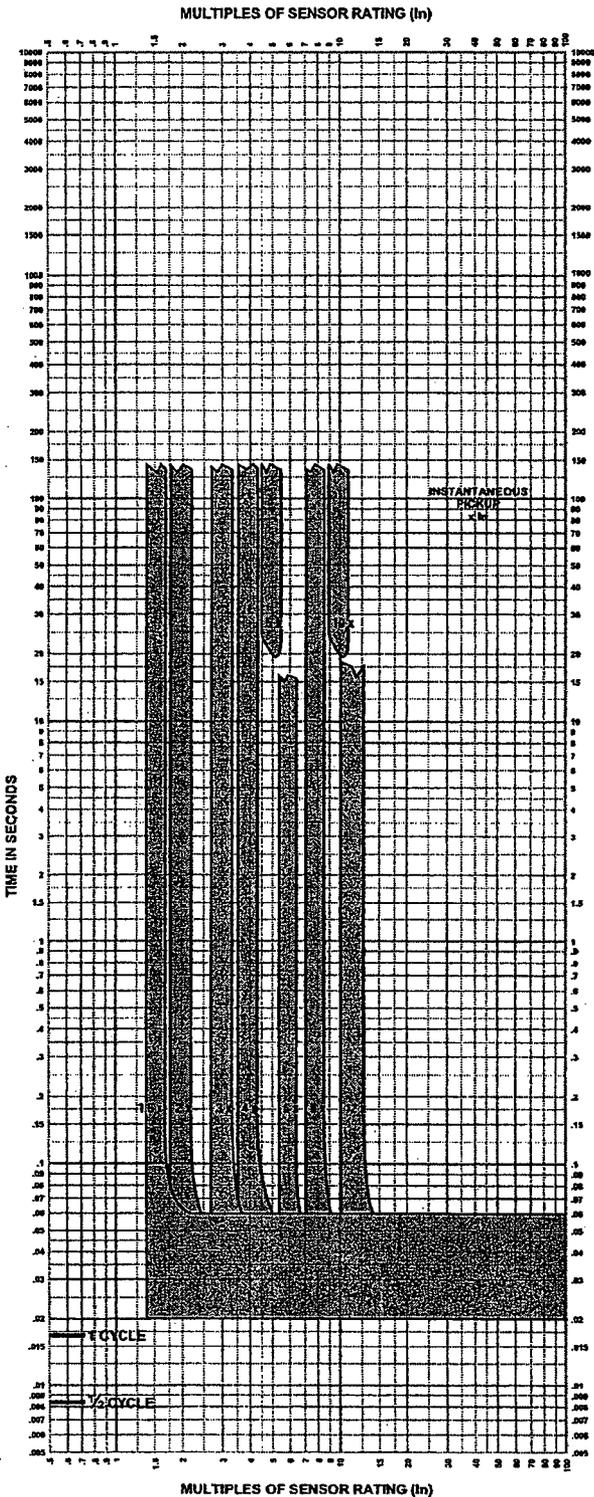
# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves

### MICROLOGIC 3.0A Trip Unit

Characteristic Trip Curve No. 613-8  
Instantaneous Pickup, 1.5X to 12X

B48095-613-06.rpt



The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

**Notes:**

1. The end of the curve is determined by the interrupting rating of the circuit breaker.
2. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of current.
3. The instantaneous region of the trip curve shows maximum total clearing times. Actual clearing times in this region can vary depending on the circuit breaker mechanism design and other factors. The actual clearing time can be considerably faster than indicated. Contact your local sales office for additional information.
4. See trip curve 613-6 on page 149 for long-time pickup and delay trip curves.

Curve No. 0613TC0008  
Drawing No. B48095-613-06



B.45

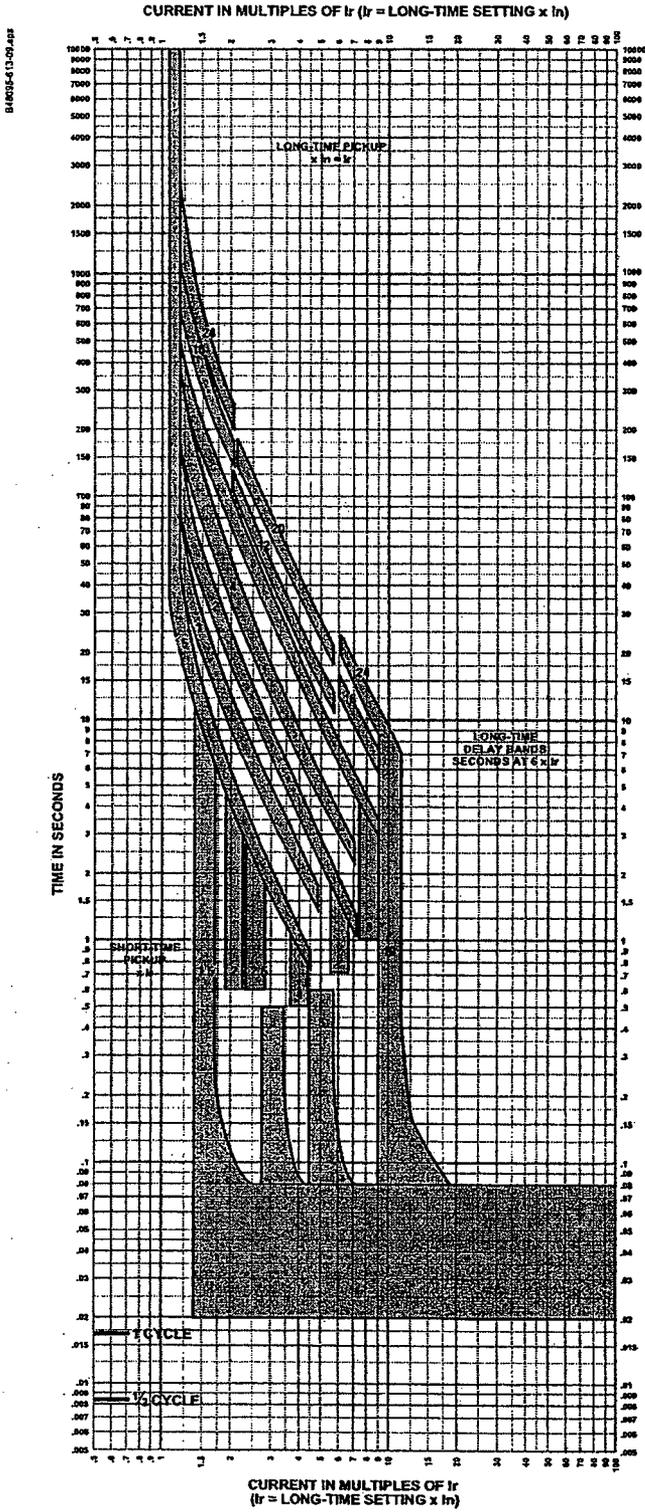
**MASTERPACT® NT/NW Universal Power Circuit Breakers**  
**Section 7: Trip Curves**

**MICROLOGIC 2.0A Trip Unit**  
 Characteristic Trip Curve No. 613-9  
**Long-time Pickup and Delay**  
**Short-time Pickup with No Delay**

The time-current curve information is to be used for application and coordination purposes only.  
 Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

**Notes:**

1. There is a thermal-imaging effect that can act to shorten the long-time delay. The thermal-imaging effect comes into play if a current above the long-time delay pickup value exists for a time and then is cleared by the tripping of a downstream device or the circuit breaker itself. A subsequent overload will cause the circuit breaker to trip in a shorter time than normal. The amount of time delay reduction is inverse to the amount of time that has elapsed since the previous overload. Approximately twenty minutes is required between overloads to completely reset thermal-imaging.
2. The end of the curve is determined by the short-time setting.
3. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of current.
4. Overload indicator illuminates at 100%.



Curve No. 0613TC0009  
 Drawing No. B48095-613-09



B.46

# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves

### MICROLOGIC 2.0/3.0/5.0/6.0 A/P/H Trip Unit

Characteristic Trip Curve 613-10

Instantaneous Override Values

MASTERPACT NW/NT			
ANSI CB Model No.	Inst. Override (kA RMS) +/- 10%	IEC CB Model No.	Inst. Override (kA RMS) +/- 10%
NW08N1 *	24	NW08N1	None
NW08N1	None	NW10N1	None
NW16N1	None	NW12N1	None
NW08H1 *	24	NW16N1	None
NW08H1	None	NW08H1	None
NW16H1	None	NW10H1	None
NW20H1	None	NW12H1	None
NW32H1	None	NW16H1	None
NW08H2 *	24	NW20H1	None
NW08H2	None	NW25H1	None
NW16H2	None	NW32H1	None
NW20H2	None	NW40H1	None
NW32H2	None	NW50H1	None
NW40H2	None	NW63H1	None
NW50H2	None	NW08H2 *	24
NW08H3	85	NW08H2	85
NW16H3	85	NW10H2	85
NW20H3	85	NW16H2	85
NW32H3	85	NW20H2	85
NW40H3	None	NW25H2	85
NW50H3	None	NW32H2	85
NW08L1 *	24	NW40H2	85
NW08L1	35	NW50H2	117
NW16L1	35	NW63H2	117
NW20L1	35	NW20H3	65
NW32L1	117	NW25H3	65
NW40L1	117	NW32H3	65
NW50L1	117	NW40H3	65
NW08HA	None	NW08L1 *	24
NW16HA	None	NW08L1	35
NW20HA	None	NW10L1	35
NW32HA	None	NW12L1	35
NW40HA	None	NW16L1	35
NW50HA	None	NW20L1	35
NT08N1 *	24	NW08H10	None
NT08N1	None	NW10H10	None
NT08H1 *	24	NW12H10	None
NT08H1	42	NW16H10	None
NT08NA	None	NW20H10	None
		NW25H10	None
		NW32H10	None
		NW40H10	None
UL CB Model No.	Inst. Override (kA RMS) +/- 10%	NW08NA	None
NW08N *	24	NW10NA	None
NW08N	40	NW16NA	None
NW12N	40	NW08HA	None
NW16N	40	NW10HA	None
NW20N	40	NW12HA	None
NW08H *	24	NW16HA	None
NW08H	40	NW20HA	None
NW12H	40	NW25HA	None
NW16H	40	NW32HA	None
NW20H	40	NW40HA	None
NW25H	65	NW50HA	None
NW30H	65	NW63HA	None
NW40H	85	NW08HF	85
NW50H	85	NW10HF	85
NW60H	85	NW12HF	85
NW08L *	24	NW16HF	85
NW08L	35	NW20HF	85
NW12L	35	NW25HF	85
NW16L	35	NW32HF	85
NW20L	65	NW40HF	85
NW25L	65	NW08HA10	None
NW30L	65	NW10HA10	None
NW40L	75	NW12HA10	None
NW50L	75	NW16HA10	None
NW60L	75	NW20HA10	None
NW08HF	40	NW25HA10	None
NW12HF	40	NW32HA10	None
NW16HF	40	NW40HA10	None
NW20HF	40	NT08H1	None
NW25HF	65	NT10H1	None
NW30HF	65	NT12H1	None
NW40HF	75	NT16H1	None
NW50HF	75	NT08L1	10
NW60HF	75	NT08H10	None
NT08N *	24	NT10H10	None
NT08N	40	NT12H10	None
NT12N	40	NT16H10	None
NT08H *	24	NT08HA	None
NT08H	40	NT10HA	None
NT12H	40	NT12HA	None
NT08L1	10	NT16HA	None
NT12L1	10	NT08HA10	None
NT08L	10	NT10HA10	None
NT12L	10	NT12HA10	None
NT08HF	40	NT16HA10	None
NT12HF	40		

\* Maximum sensor plug 250 A

**Note:**

1. Faults at or above instantaneous override value will be cleared at twenty milliseconds or less.

Curve No. 6813TC0010  
Drawing No. B48095-613-10



**Micrologic<sup>®</sup> 5.0P and 6.0P  
Electronic Trip Units**

v PLogic-2002-AA



**Unidades de disparo electrónico  
Micrologic<sup>®</sup> 5.0P y 6.0P**

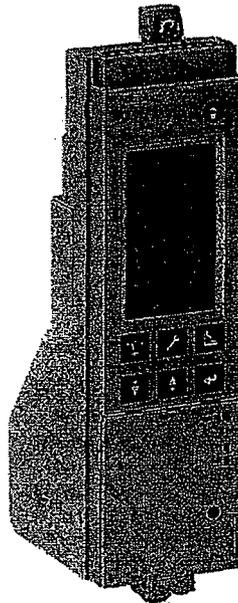
v PLogic-2002-AA

**Déclencheurs électroniques  
Micrologic<sup>®</sup> 5.0P et 6.0P**

v PLogic-2002-AA

Instruction Bulletin  
Boletín de instrucciones  
Directives d'utilisation

Retain for Future Use. / Conservar para  
uso futuro. / À conserver pour usage  
ultérieur.



**Schneider**  
 **Electric**

B.48

VVTP-042101-1, ref[2]

## **Attachment C**

### **Failure Modes & Effects Analysis**

**The Schneider Failure Modes & Effects Analysis (FMEA) is a proprietary document. This document is not included in the version of this report that is released to our clients. This document is available at the NLI facility for review.**

**The following document is attached. This document provides a detailed summary of the Schneider FMEA.**

- **NLI report FS-042181-1, “Summary of the Schneider Electric Failure Modes and Effects Analysis (FMEA) for the Micrologic Trip Device”, revision 0.**

# **NLI**

**NUCLEAR LOGISTICS INC**

**SUMMARY OF THE SCHNEIDER ELECTRIC  
FAILURE MODES AND EFFECTS ANALYSIS (FMEA)  
FOR THE  
MICROLOGIC TRIP DEVICE**

FS-042181-1  
Revision 0  
December 2005

**APPROVAL**

**SUMMARY OF THE SCHNEIDER ELECTRIC  
FAILURE MODES AND EFFECTS ANALYSIS (FMEA)  
FOR THE  
MICROLOGIC TRIP DEVICE**

This summary has been prepared in accordance with the NLI Quality Assurance Program.

Prepared by:  date 12/20/05

Verified by:  date 12/20/05

Approved by:  date 12/20/05

### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Date</u>
0	Original Issue	12/ <u>20</u> /05

## TABLE OF CONTENTS

- 1.0 Introduction
- 2.0 Objectives of the Study
- 3.0 Applicable Reference Documents
- 4.0 FMEA Methodology
- 5.0 FMEA Summary
- 6.0 Summary of Results
- 7.0 NLI Conclusions

## 1.0 INTRODUCTION

Schneider Electric performed Verification and Validation (V&V) of the Micrologic trip device in accordance with European standards. NLI performed V&V of the Micrologic trip device in accordance with U.S. standards, as detailed in NLI report VVR-042181-1. The NLI V&V report took credit for the Failure Modes and Effects Analysis (FMEA) that was performed by Schneider Electric. This report summarizes the Schneider FMEA methodology and results.

The following Schneider Electric document is summarized herein:

- Schneider report 5100513140-B, "Failure Modes and Effects Analysis PROXIMA release ELA version", dated 6/28/01. Note that the original version of the document is in French.

## 2.0 OBJECTIVES OF THE FMEA

During the latter phases of the design of the Micrologic trip unit, the Schneider Electric design team performed an extensive Failure Modes and Effects Analysis (FEMA) to determine the reliability of trip unit and to identify opportunities to improve its reliability. The objectives of the FEMA were as follows:

- To quantify the reliability of the trip unit.
- To comprehensively identify the probability of the failure of a critical component.
- To predict the rate of client returns of the trip unit due to design failures.
- To establish a plan of action to make the product more reliable (extend the mean time to failure).

## 3.0 APPLICABLE REFERENCE DOCUMENTS

The following primary references are cited in the Schneider FMEA:

Number	Description
5 100 512 176-G	Design Document
5 100 513 140-B	Electrical Diagram
MIL HDBK 217F	Compilation of Reliability Data
UTE80810	Compilation of Reliability Data
Catalogue of Siemens & Matsushima components	Component Reliability Data
NF X50-153	Standard describing the M.I.S.M.E method

#### 4.0 FMEA METHODOLOGY

The following methodology was used by Schneider to perform the FMEA:

- An external functional analysis was performed. This methodology shows the ties between the studied item and its environment in order to determine a failure relationship. The methodology used is M.I.S.M.E (method of systematic inventory of the surrounding environment). Note: This technique was used as part of the functional and safety requirements analysis performed by the European Organization for Nuclear Research for the CERN Safety Alarm Monitoring System.
- An internal functional analysis by functional block diagram was performed in accordance with MIL-HDBK-217F.
- A dysfunctional analysis was performed showing the consequences of a failure on the operability of the trip unit.
- Reliability calculations were performed in accordance with MIL-HDBK-217F. The results are summarized in section 5.2 of this report.
- An A.M.D.E.C. quantified for a temperature of 40°C in a stationary environment. Note: AMDEC is a technique used for the development of products and processes in order to reduce the risk of failures and to document the actions undertaken. It is part of the QS 9000 'whole quality system' methodology.

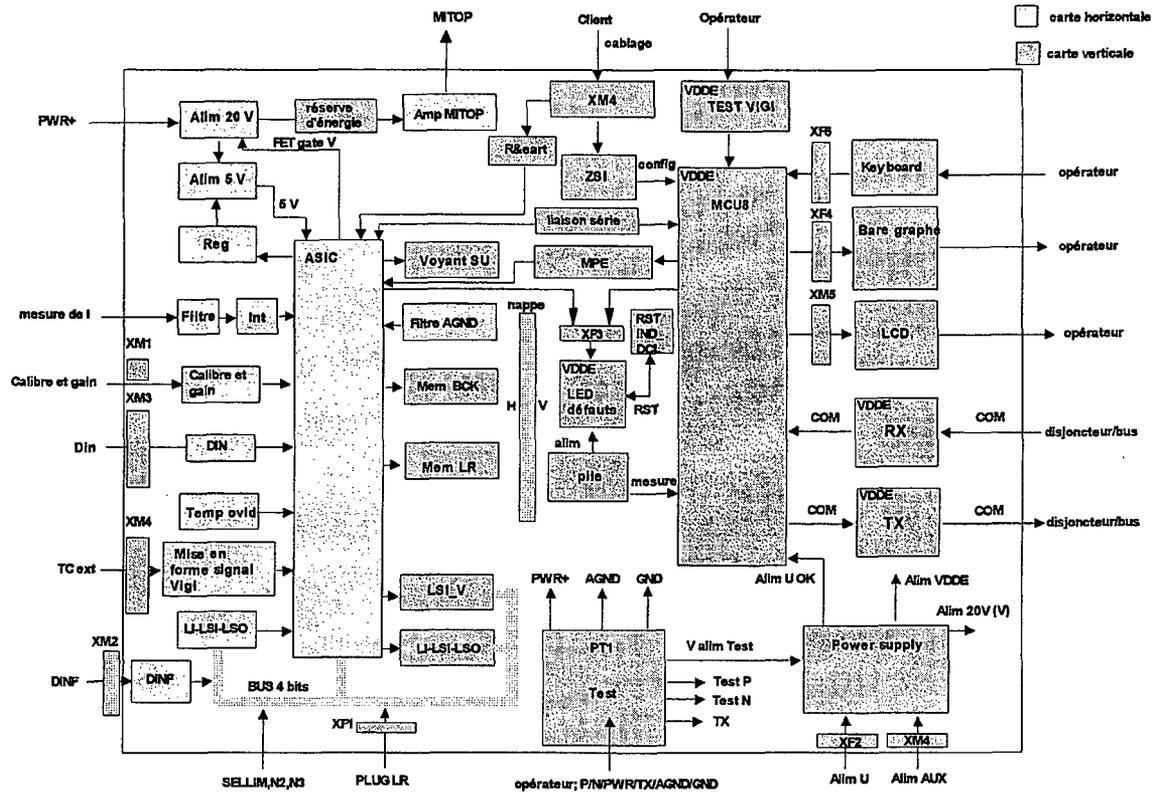
#### 5.0 FMEA SUMMARY

External Analysis. The M.I.S.M.E method addresses the trip unit's reliability in relation to the outside elements with which it interacts. The method is described in the standard NF X50-153. This approach identifies the exogenous variables that might adversely impact the reliability of the trip unit. The identified variables were:

- a. Iron-core CT
- b. Air-core CTs
- c. LR Plug
- d. External power
- e. Physical environment
- f. External communications
- g. Connection with the circuit breaker
- h. Operator (man-machine interface)
- i. Connection to communications nexus.

Internal Analysis. This method addresses the trip unit's reliability in relation to and with the functional areas within the trip unit. This approach identifies the endogenous variables that might adversely impact the reliability of the trip unit. The identified variables were modular, hierarchical, and structural.

A block diagram of the trip unit is presented below.



Evaluation of Global Reliability. This method addresses the trip unit's reliability in relation to the sum of the failure rates of the components under the specified service conditions. The calculation was made with the RELEX 6.2 software, using the methodology described in MIL-HDBK-217 F. Both the Arrhenius methodology and physical testing methodologies were employed to gather data for the variables. Particular emphasis on was placed on hypothesized and historical failure rates of the following components:

- a. MOS devices.
- b. Capacitors.
- c. Clocking devices
- d. Printed circuit board materials and construction.
- e. ASIC materials and construction.
- f. Connectors.
- g. Optical conductors.
- h. Keyboard devices.

Additional component types that were evaluated include the following:

- a. Resistors.
- b. Rotary switches.
- c. Relays.
- d. Integrated circuits.
- e. Inductors.
- f. Transformers.

Design of Subcomponents. The AMDEC methodology is an analysis of the component operation in the circuit and their effects on the functionality of the trip unit. The result of the analysis identified the following components as critical to the trip unit design:

- a. Rotary switches.
- b. MOS devices.
- c. ASIC
- d. Push-button switch
- e. Optical coupler

## 6.0 SUMMARY OF RESULTS

The results of the FMEA are summarized as follows:

- There are no known hardware issues that exist for the ASIC or the microcontroller platform used for the four trip controllers.
- There are no known software issues that exist for the microcontroller platform used in the Ammeter, Power, or Harmonics trip controllers. The Standard variant does not include a microcontroller.
- The total projected failure on demand has a probability of about  $3.11 \times 10^{-6}$  per hour 40°C in fixed service (NLI note: applicable to nuclear power plants). This probability is computed based on worst-case applications. The failure rate is based on excessively conservative data from the US MIL-HDBK-217-F. The actual operating history demonstrates that this kind of failure rate does not occur after the first year.
- Two primary failure modes exist:
  - Loss of clock (gate pulse).
    - This postulated failure results in a loss of the ASIC's digital protection functions. The diverse analog instantaneous and thermal trip functions are maintained.
    - This failure mode is considered a low probability event based on the simplicity of the design and reliability of the parts used. The equipment reliability documented above includes clock failures.
  - Loss of 24 volt DC power.
    - This postulated failure results in a loss of all ASIC protection functions, including the diverse analog instantaneous and thermal trip functions.

- This failure mode is considered a low probability event based on the simplicity of the design and reliability of the parts used. The equipment reliability documented in section 5.2 includes loss of the internal power supply.
- (NLI note: The 24 volt external power has not been certified for Class 1E applications by NLI).
- Both of these failures are acceptable as follows:
  - These are hardware failures in the system and are not a function of the software. The hardware is manufactured with a minimum number of components and is highly reliable.
  - Hardware failure of a proven product like the Micrologic trip device, is a random event. Common cause failure of this type of hardware is not credible.
- Other types of failures are less likely, including coordination failure, loss of differential protection, loss of communication, loss of display, and loss of overload indication.

**NOTE:** The concerns identified during the AMDEC analyses were made the subjects of a Schneider Electric corporate Six Sigma program to identify and evaluate the critical components. The engineers evaluated and reworked the designs as necessary to minimize the risk of failure, based on risk informed analyses. They identified critical components and wrote tight specifications for their suppliers. Components are qualified based on these specifications, which define the requirements as critical characteristics.

## 7.0 NLI CONCLUSION

The following conclusions are made by NLI following review of the Schneider FMEA:

The Schneider/Square D FMEA was performed in a rigorous manner and addresses the relevant potential failure modes. The FMEA identified two hardware failure modes that could impact the trip unit operation. These failure modes were determined to be acceptable.

No potential failure modes have been identified that have unacceptable consequences.

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<sup>1</sup> Six Sigma is a disciplined, data driven approach and methodology for eliminating defects in any process. The term 'Six Sigma' refers to the drive to achieve six standard deviations between the mean and the nearest specification limit. Six Sigma companies use trained, certified staff to conduct measurement-based process improvement projects, designed to reduce variability and enhance quality. The methodology is based on their program's define, measure, analyze, improve, control (DMAIC) paradigm.

**ATTACHMENT D**

**NLI V&V Plan VVP-042181-1**

**SOFTWARE  
VERIFICATION AND VALIDATION PLAN  
FOR  
SQUARE D MICROLOGIC TRIP UNIT**

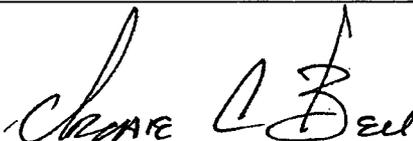
Plan VVP-042181-1  
Revision 1  
June 2004

**APPROVAL**  
**SOFTWARE**  
**VERIFICATION AND VALIDATION PLAN**  
**FOR**  
**SQUARE D MICROLOGIC TRIP UNIT**

This plan has been prepared in accordance with the NLI Quality Assurance Program.

Prepared by:  date 6/2/04

Verified by:  date 6/2/04

Approved by:  date 6/2/04

### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Date</u>
0	Original Issue	04/30/04
1	Added clarifications	6/2/04

## TABLE OF CONTENTS

- 1.0 SCOPE
  - 1.1 Scope
  - 1.2 Codes and Standards
- 2.0 EQUIPMENT IDENTIFICATION
  - 2.1 Equipment Configuration
  - 2.2 Traceability of the Test Specimen to the Production Units
  - 2.3 Safety Function
  - 2.4 Human Machine Interface
- 3.0 SOFTWARE QUALITY ASSURANCE PLAN
  - 3.1 Roles and Responsibilities
  - 3.2 Required Documentation
  - 3.3 Project controls
- 4.0 ABNORMAL CONDITIONS AND EVENTS
  - 4.1 Environmental Service Conditions
  - 4.2 Seismic Service Conditions
  - 4.3 Electromagnetic Interference/Radio Frequency Interference (EMI/RFI)
  - 4.4 Voltage Range
  - 4.5 Infant Mortality of Electronic Components
  - 4.6 Fault in Non Safety Plant System
  - 4.7 Hardware/Software Faults
  - 4.8 Loss of Power
  - 4.9 Overcurrent Condition
- 5.0 FAILURE MODES AND EFFECTS ANALYSIS
- 6.0 REQUIRED SYSTEM CHARACTERISTICS
- 7.0 IMPLEMENTATION OF REQUIRED CHARACTERISTICS
  - 7.1 Commercial Grade Audit of Square D/Schneider
  - 7.2 NLI Testing
- 8.0 CONFIGURATION CONTROL
  - 8.1 As-Supplied Configuration
  - 8.2 Vendor Firmware Configuration Control
  - 8.3 Plant Lifetime Configuration Control

9.0 EVALUATION OF RESULTS

- 9.1 Anomalies
- 9.2 Modifications
- 9.3 Results/Conclusions

10.0 QUALITY ASSURANCE

11.0 MEASUREMENT & TEST EQUIPMENT

12.0 DOCUMENTATION

13.0 REFERENCES

ATTACHMENT A: Equipment Data Sheets

ATTACHMENT B: Seismic RRS

## 1.0 SCOPE

### 1.1 Scope

This Verification & Validation (V&V) program was developed to demonstrate the acceptability of Square D Micrologic trip units to meet the requirements for the use of digital components in safety related applications in nuclear power plants. The Micrologic trip units are used in the Masterpact AC low voltage switchgear breakers (up to 600vac nominal).

The trip units utilize ASIC technology. They are designed, manufactured, and tested by Square D's parent company Schneider Electric and upgraded for safety related applications by NLI. This plan documents the requirements for the V&V of the software/hardware used in the trip devices.

The Micrologic device will be referred to as a "trip unit" or "trip device" in this plan.

The specific range of parameters that will be addressed by this V&V plan are as follows:

- Standard, Ammeter, Power, and Harmonic models of the Micrologic trip device (3.0, 5.0, 3.0A, 5.0A, 6.0A, 5.0P, 6.0P, 5.0H, and 6.0H).
- All potential functions (LSIG)
  - Long time delay.
  - Short time delay.
  - Instantaneous.
  - Ground fault protection.
- The safety function of the trip device is:
  - Proper operation and breaker tripping per the curve.
  - No spurious breaker tripping/operation upon loss of power or other Abnormal Conditions and Events (ACE's).
- All other functions will be considered non-safety related:
  - Displays, communications, interlocking, etc. will be considered to not be safety related functions.
  - This V&V program will verify that the operation, loss of operation, or malfunction of these functions will not impact the safety related function of the trip unit.
  - The basis for this is as follows:
    - Based on our experience, most plants will not require these options. V&V of these options would be on a case by case basis, depending on plant specific requirements.
    - V&V of the interlocking and communication features would be significantly more complicated and would involve 50.59 issues that would be very plant specific.

Qualification of the test specimen will be in accordance with reference 11. Dedication of the production units will be in accordance with reference 6.

## 1.2 Codes and Standards

The software for the trip unit was developed under the controls of the Schneider ISO 9001 quality assurance program. The hardware and firmware are being dedicated for safety related applications by NLI under the controls of the NLI Nuclear Quality Assurance Program [1]. The applicability of the codes and standards are addressed in this section. These codes and standards form the basis for this plan.

Note: Most of the codes and standards referenced in the specification are for control of the entire software lifecycle. Many of the codes and standards are very prescriptive concerning the required activities and documentation. Since this project is the dedication of existing commercial software, only certain requirements of these standards are applicable.

### 1.2.1 EPRI TR-102348 Guidelines on Licensing Digital Upgrades

This V&V plan meets the guidelines of this document.

This industry document provides guidance on software design and quality assurance, commercial grade item dedication, environmental considerations including electromagnetic and radio frequency interference and human machine interface requirements.

### 1.2.2 IEEE 7-4.3.2-1993 IEEE Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations

This V&V plan meets the requirements of IEEE 7-4.3.2-1993 as specified herein.

The main body of this standard provides guidance for software developed under the controls of a nuclear quality assurance program and is not applicable to this plan since the trip unit firmware was developed outside of the criteria in the standard. The main body and other Annex's of this standard were used as guidelines when developing this plan.

The guidelines provided in Annex D, "Qualification of Existing Commercial Computers," were used to develop this plan which provides reasonable assurance that the integrated systems (software and hardware) satisfy the requirements necessary to accomplish the intended safety functions of the equipment. Specifically this plan reflects the objectives of Annex D including:

- Identification of the safety function(s) that the computer systems and software must perform.
- Identification of the critical characteristics that the integrated system must possess in order to accomplish the safety function(s)
- Demonstration testing to validate that the characteristics are implemented acceptably.

Applicable sections of Annex F are used as a guide for evaluation of Abnormal Conditions and

Events (ACEs) which could negatively impact the capability of the trip unit digital controls. ACEs were evaluated to identify external events as well as conditions internal to the digital computer system hardware and software that have the potential to defeating the safety function.

### **1.2.3 EPRI TR-106439 Guidelines on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications**

This V&V plan meets the guidelines of this document.

### **1.2.4 ASME NQA-2a-1990, Part 2.7**

This standard provides detailed prescriptive process and requirements for the development, procurement, maintenance and use of software as applied to the design of nuclear facilities. The process which is described is throughout the lifecycle of the software, from the requirements specification to lifetime maintenance of the system. Technical, test, and documentation requirements are specified for each lifecycle step. The standard is based on the lifecycle model in IEEE 1012. This standard is not applicable, since the software was not developed by the equipment manufacturers in accordance with the requirements of the standard. The software was previously developed, so many of the life cycle phases have been completed by the equipment vendors without performing of the specified steps. Many of the documents prescribed by this standard were not prepared by the equipment vendors.

The lifecycle phases of the software will be evaluated. The procedures and processes used in each lifecycle phase will be documented. The results of each lifecycle phase will also be documented. The lifecycle phase model in IEEE 1012 will be used, as discussed in this plan. The applicable portions of this standard which have been incorporated into this plan are specified below.

Section 10.2, "Software Developed Not Using This Standard," is applicable and will be met in it's entirety. This plan, in conjunction with the equipment manuals, verification and acceptance testing, and final test reports provides the required documentation and evaluations to:

- 1) Determine adequacy of the software/ firmware to support reliable equipment operation.
- 2) Identify the activities to be performed including documentation required to place the software/ firmware under configuration control including:
  - a) Application requirements
  - b) Test plans and test cases required to validate the software/ firmware for acceptability
- 3) Satisfy user documentation requirements including:
  - a) User instructions
  - b) Input and Output Specifications
  - c) Input and Output Formats
  - d) Description of System Limitations
  - e) Information for obtaining user and maintenance support

### **1.2.5 IEEE 1012-1986 IEEE Standard for Software Verification and Validation Plans**

This standard provides a detailed prescriptive process for the development of software verification and validation plans. The process which is described includes verification and validation tasks throughout the lifecycle of the software, from the requirements specification to lifetime maintenance of the system. Technical, test, and documentation requirements are specified for each lifecycle step. This standard is not fully applicable since the software/firmware was previously developed and verification and validation of many of the life cycle phases were not documented in accordance with the standard. The specific format, content, and acceptance criteria in this standard will not be used, since the firmware has previously been developed.

The lifecycle model specified in Figure 1 of the standard will be used during the evaluation of the software. The following lifecycle phases will be evaluated:

- Concept.
- Requirements.
- Design.
- Implementation.
- Testing (Firmware and system integration).
- Installation and Checkout.
- Operation and Maintenance.
- Reporting Requirements.

Table 2.1 of this plan identifies critical characteristics with acceptance criteria for each phase of the software lifecycle. The audits at Schneider and the supplemental testing at NLI will verify that the acceptance criteria are met for the life cycle critical characteristics.

### **1.2.6 IEEE 730-1989 IEEE Standard for Software Quality Assurance Plans**

This standard provides the minimum requirements for preparation and content of quality assurance plans for reviews and audits of software. The standard applies to the development of critical software from the requirements specification to lifetime maintenance of the system. Audit requirements are specified for a number of step and documents, which are prepared in accordance with IEEE 1012-1986.

Since development of the firmware used in the trip unit was not documented in accordance with IEEE-1012-1986, this standard will be used as a guideline. The specific format, content, and acceptance criteria in this standard will not be used. The specific critical characteristics and acceptance criteria which will be evaluated are identified in Table 2.1 of this plan.

The Software Quality Assurance Plan that will be implemented by NLI is specified in section 3 of this plan.

The NLI audit at Schneider Electric will address the following topics identified in section 3 of the standard:

- Documentation.
- Tests.
- Problem reporting and corrective actions.
- Tools, techniques, and methodologies.
- Code control.
- Media control.

This review will provide confirmation that the integrated system design, testing, deployment, and maintenance is in accordance with the Schneider quality assurance program and that there were effective quality assurance controls in place.

Code Control and Media Control at the Schneider facility will be verified by a commercial grade audit as identified in section 7.1 of this plan. Additional integrated hardware and firmware configuration testing will be performed by NLI as described in section 7.2 of this plan. Configuration control following delivery of the units to the plant will be as identified in section 8.0 of this plan.

#### **1.2.7 IEEE 1028-1988 IEEE Standard for Software Reviews and Audits**

This standard provides specific requirements for the implementation of software quality assurance reviews and audits. The process which is described is throughout the lifecycle of the software from the requirements specification to lifetime maintenance of the system. Audit and documentation requirements are specified for all phases of the lifecycle of the software.

Since development of the firmware used in the trip unit were not performed or documented in accordance with IEEE-1012-1986, this standard will be used as a guideline. The specific format, content, and acceptance criteria in this standard will not be used.

This standard will be used as a guideline during the NLI audit at Schneider. The following specific issues will be addressed, as applicable to the actual design, development, testing, and configuration control processes:

- Technical reviews of the vendor integrated system development documentation.
- Inspection of the vendor integrated system verification and validation test documentation.
- Audit of the vendor quality assurance programs used in the software development.
- Testing of the integrated system.

#### **1.2.8 IEEE 828-1990 IEEE Standard for Software Configuration Management**

This standard provides a detailed prescriptive methodology for preparation and implementation

of a configuration management plan for software. Since the software was not developed by Schneider in accordance with this standard, the prescriptive methodology of the standard will not be met.

Configuration control will be addresses as follows:

- The configuration control implemented by Schneider will be documented in the audit as presented in Table 6.1.
- The configuration control activities by NLI and the plant are per section 8 of this plan.

The intent of this standard for a formal configuration control process is met.

### **1.2.9 IEEE 829-1990 IEEE Standard for Software Test Documentation**

This standard provides a detailed prescriptive methodology for the preparation and documentation of software documentation. The required documentation includes a test design specification, test case specification, test procedure specification, test item transmittal report, test log, test incident report, and test summary report. Since the software was not developed by Schneider in accordance with this standard, the prescriptive methodology of the standard will not be met.

Software test documentation will be identified and evaluated as follows:

- Schneider's test procedures, test results, and other test documentation will be reviewed during the audit. See Table 6.1 for the specific attributes that will be reviewed.
- NLI testing will be in accordance with written procedures with test results documented per the NLI Nuclear Quality Assurance Program.

The intent of this standard for a formal software test process is met.

### **1.2.10 IEEE 830-1984 IEEE Standard Guide for Software Requirements Specification**

During the NLI audit of GE, NLI will review the software specification or equivalent document developed by GE. The results of the review will be documented in the Audit Report that will be included in the V&V report.

### **1.2.11 IEEE 1008-1987 IEEE Standard for Software Unit Testing**

This standard provides a detailed prescriptive methodology for software unit testing. Since the software was not developed by Schneider in accordance with this standard, the prescriptive methodology of the standard will not be met.

Software test methodology will be identified and evaluated as follows:

- Schneiders's test procedures, test results, and other test documentation will be reviewed during the audit. See Table 6.1 for the specific attributes that will be reviewed.
- NLI testing will be in accordance with written procedures with test results documented per the NLI Nuclear Quality Assurance Program.

The intent of this standard for a formal software test process is met.

#### **1.2.12 IEEE 1016-1987 IEEE Recommended Practice for Software Design Descriptions**

During the NLI audit of Schneider, NLI will review the software design description or equivalent document developed by Schneider. The results of the review will be documented in the Audit Report that will be included in the V&V report.

#### **1.2.13 IEEE 1063-1987 IEEE Standard for Software User Documentation**

This document provides a detailed prescriptive methodology for the structure, information content, and format for software user documentation. Since the software documentation was not developed by Schneider in accordance with this standard, the prescriptive methodology of the standard will not be met.

NLI has reviewed the Schneider documentation for the trip unit hardware/software system. The documentation is complete and well organized.

The intent of this standard for technically accurate, complete and well organized software documentation is met.

#### **1.2.14 IEEE 1074-1995 IEEE Standard for Developing Software Life Cycle Processes**

This standard provides a detailed prescriptive methodology for the planning, implementation, and documentation of the software lifecycle. Since the software was not developed by Schneider in accordance with this standard, the prescriptive methodology of the standard will not be met.

The software lifecycle planning, implementation, and documentation will be identified and evaluated as follows:

- The controls and documentation by Schneider will be identified and evaluated during the audit of Schneider. See Table 6.1 for the specific lifecycle activities that will be addressed.
- The lifecycle activities that will be performed by NLI will be in accordance with this plan.

The intent of this standard for controlled planning, implementation, and documentation of the software lifecycle is met.

#### **1.2.15 IEEE 1228-1994 IEEE Standard for Software Safety Plans**

This standard provides a detailed prescriptive methodology for the development, procurement, maintenance, and retirement of safety critical software. The purpose is to develop the processes and activities to improve the safety of the critical software. Since the software was not developed by Schneider in accordance with this standard, the prescriptive methodology of the standard will not be met.

The software safety plan will be implemented as follows:

- The audits of Schneider by NLI will document the activities performed by Schneider to improve the safety of the software.
- The dedication testing, design testing, and qualification testing by NLI will improve the safety of the software.

The intent of this standard for controlled planning, implementation, and documentation of the software lifecycle is met.

#### **1.2.16 EPRI 5652 Utilization of Commercial Grade Items in Nuclear Safety Related Applications with supplemental guidance EPRI TR-102260**

These documents provide general guidance for the commercial grade dedication of equipment for use in safety related applications. The dedication and qualification program for the trip devices was developed using the guidance provided in this standard in conjunction with the other standards described in this plan.

#### **1.2.17 IEEE 323-1974/1983 and NRC Regulatory Guide 1.89**

The trip unit will be qualified for the plant specific service conditions per these documents. These requirements of these documents are met.

#### **1.2.18 IEEE 344-1975/1987 and NRC Regulatory Guide 1.100**

The trip unit will be qualified for the plant specific seismic conditions per these documents. These requirements of these documents are met.

#### **1.2.19 IEEE 384-1977/1981/1992 and NRC Regulatory Guide 1.75**

The trip devices are physically and electrically isolated as follows:



- The trip devices are physically located on each circuit breaker. There is no change in the physical independence or separation of the breakers/trip units from the current plant configuration.
- The trip devices have no electrical connection with other trip devices. They are powered from the CT's on the breaker and send and send a signal only to the flux shifter to trip the breaker. There is no change in the electrical separation/isolation from the current plant configuration.

The requirements of these documents are met to the extent that they are met by the current plant configuration.

## **2.0 EQUIPMENT IDENTIFICATION**

### **2.1 Equipment Configuration**

The trip unit is available in a number of configurations, as follows:

- Standard, Ammeter, Power, and Harmonic models of the Micrologic trip device (3.0, 5.0, 3.0A, 5.0A, 6.0A, 5.0P, 6.0P, 5.0H, and 6.0H). Various functions can be defeated to achieve the required protection.
- All potential functions (LSIG).
  - Long time delay.
  - Short time delay.
  - Instantaneous.
  - Ground fault protection.
- Various functions can be defeated to achieve the required protection.
- The equipment data sheets/technical data will be included in the V&V report.

This V&V program will address all of the trip unit configurations, since they all use the same firmware.

The displays, communications, interlocking, and other functions not associated with breaker tripping will be considered to be non-safety related functions and will be addressed as follows:

- The trip units will not be qualified with any communications features operational.
- The built-in communication firmware and hardware will be demonstrated to not impact the operation of the safety related function of circuit protection.

### **2.2 Traceability of the Test Specimens to the Production Units**

Traceability of the test specimen to the production units will be performed. The following methodology will be used to document the traceability:

- The test specimens and the production units will be shown to have the same hardware and configuration:

- Programmer physical configuration.
- Circuit board and chip part and revision, as applicable.
- The test specimens and the production units will be shown to have the same firmware configuration (firmware revision).
- There are no field configurable circuit board settings (DIP switches, jumpers, etc.).
- The functional testing of the test specimen and the dedication testing of the production units will provide added assurance that the production units were manufactured to the same design standards and perform in an equivalent manner to the test specimen.

### **2.3 Safety Function**

The safety functions of the trip devices are:

- Maintain low voltage power circuits during normal conditions, including no spurious tripping.
- Interrupt low voltage circuits in overcurrent conditions.
- The non-safety related features (display, communications, etc.) cannot interfere with the proper operation of the trip unit.

Abnormal Conditions and Events (ACE) are addressed in additional detail in Section 4.0.

### **2.4 Human Machine Interface**

The Human/Machine Interfaces are the switches on the front of the trip unit that are used to set the trip ranges of the trip unit. No programming can be performed on the trip unit.

## **3.0 SOFTWARE QUALITY ASSURANCE PLAN**

Project activities will be performed in accordance with the NLI Nuclear Quality Assurance Program [1] which meets the requirements of 10CFR50 Appendix B, 10CFR21, and ASME NQA-1.

This plan applies to the Square D Micrologic trip units being supplied by NLI on Square D Masterpact low voltage circuit breakers.

This Software Quality Assurance Plan is for the activities that will be performed by NLI. The software was developed under the controls of the Schneider ISO9000 quality program, so this Software Quality Assurance Plan is not applicable to the activities performed by Schneider.

Program [1] which meets the requirements of 10CFR50 Appendix B, 10CFR21, and ASME NQA-1.

This plan applies to the Square D Micrologic trip units being supplied by NLI on Square D Masterpact low voltage circuit breakers.

This Software Quality Assurance Plan is for the activities that will be performed by NLI. The software was developed under the controls of the Schneider ISO9000 quality program, so this Software Quality Assurance Plan is not applicable to the activities performed by Schneider.

### **3.1 Roles and Responsibilities**

The roles and responsibilities of NLI personnel are as follows:

- Quality Assurance:
  - Responsible for the overall quality of the project.
  - Performs independent reviews of the project documents to verify conformance with the NLI Nuclear Quality Assurance Program.
  - Perform software and hardware audits of the Schneider facilities.
- Quality Assurance personnel will perform the following specific project activities:
  - Independent verification that the code burned on the programmable digital chips is traceable to the documented code.
  - Independent verification of the labeling of the programmable digital chips with the code name and revision level.
  - Document the as-supplied configuration of the hardware and software.
- Project Engineer: Responsible for the generation of the project documentation.
- Test Technician: Responsible for performing the functional testing of the trip unit (hardware/software system).

### **3.2 Required Documentation**

The following documentation will be prepared in accordance with the NLI Nuclear Quality Assurance Program:

- V&V Plan.
- NLI Validation Test Plan.
- V&V Report.
- Dedication Plan.
- Dedication Report.
- Audit Plan and Audit Report (to be included in V&V report).
- Instruction Manual.
- Digital Component Configuration Data Sheet (to be included in the Instruction Manual). See section 8.1 of this plan for details.

The following V&V activities are performed per this plan.

- The software V&V activities are as specified in this plan.
- Software configuration management and change control is as specified in section 8.0 of this plan.
- Code and Media Control is as specified in Table 6.1 and section 8.0 of this plan.
- Problem and Error Reporting will be in accordance with section 8.0 of this plan.

Project records will be maintained for the plant lifetime in accordance with the NLI Nuclear Quality Assurance Program [1].

### **3.3 Project Controls**

The following additional project controls will be implemented:

- Design control will be in accordance with the NLI Project Performance Plan.
- Interface control will be in accordance with the NLI Project Performance Plan.
- The following activities will be performed in accordance with the NLI Nuclear Quality Assurance Program [1]:
  - Independent verification and approval of safety related documents.
  - Design reviews.
  - Document control.
  - Vendor audits.
  - Calibration of measurement & test equipment.
  - Personnel qualification.
- Code and Media Control is as specified in Table 6.1 and section 8.0 of this plan.

### **4.0 ABNORMAL CONDITIONS AND EVENTS (ACE's)**

The guidance provided in Annex F of IEEE Standard 7-4.3.2-1993 was used to identify the various ACEs that could impact the capability of the trip unit to perform the intended safety functions. The Abnormal Conditions and Events (ACEs) that could impact the proper operation are identified in this section. The methods which are used to evaluate each of the ACE's are also presented.

**Note: The ACE's and the levels specified below are expected to envelop most of the Class 1E applications in nuclear power plants. Plant specific levels that are not enveloped will be evaluated and tested on a plant specific basis.**

#### **4.1 Environmental Service Conditions**

The following service conditions are defined:

- Operating time: continuous
- Temperature range: 40-104°F (note 1)
- Relative Humidity: 98% (non-condensing) maximum
- Radiation: 5E3 rad gamma

Notes:

1. The maximum temperature of 104°F is the maximum ambient temperature. The trip device will be demonstrated to be acceptable for a total temperature of 121°F (104°F ambient + 17°F in-switchgear temperature rise).

The mild environment qualification will be in accordance with IEEE 323-1974/1983 [3], IEEE C37.81-1989 [23], and IEEE C37.82-1987.

Plant specific service conditions that are greater than the service conditions specified above will be addressed on a case by case basis by analysis or testing.

#### 4.2 Seismic Service Conditions

The trip unit will be qualified by testing for the service conditions as specified in each plant specific seismic qualification plan [11]. The seismic qualification testing will meet the requirements of IEEE 344-1975/1987 [23], IEEE 323-1974/1983 [3], IEEE C37.81-1989 [23], and IEEE C37.82-1987. The test plan provides detailed acceptance criteria for the seismic testing.

The trip unit seismic qualification is to the in-switchgear levels, including any required amplification. Since the trip unit is mounted in the breaker, the breaker and trip unit will be seismically qualified together.

#### 4.3 Electromagnetic Interference/Radio Frequency Interference (EMI/RFI)

EMI/RFI emissions and susceptibility requirements are defined for the trip unit based on EPRI TR-102323, revision 1 [12]. The trip unit will be qualified by testing as specified in the qualification plan [11]. The test plan [11] provides detailed acceptance criteria for the EMI/RFI testing.

#### 4.4 Voltage Range

The trip units are powered by current transformers (CT's) on the main bus. The equipment is required to operate across the plant specified voltage range for the AC bus. The trip units will be tested at the minimum degraded voltage and the maximum overvoltage conditions during the dedication testing [6]. These voltage conditions are specified as follows:

- Typical nominal plant voltages are 480vac and 575vac.
- Minimum voltage will be 480vac (75%) = 360vac.



- Maximum voltage will be 575vac (110%) = 635vac.

#### **4.5 Infant Mortality of Electronic Components**

A total run time of at least 48 hours will be documented during the dedication testing of the production units. This will serve as a burn-in to lower the chances of infant failures of the electronic components [6].

#### **4.6 Fault in Non Safety Plant System**

The Class 1E trip units do not interface with the non-safety plant equipment. The trip unit is self contained within the breaker as follows:

- The trip unit receives power from the CT's on the breakers primary circuit.
- The trip unit sends the trip signal to the flux shifter in the breaker.

The EMI/RFI qualification [11] will verify that EMI/RFI emissions from non-safety plant equipment will not impact the operation of the trip units.

#### **4.7 Hardware/Software Faults**

Potential faults in the hardware or firmware will be evaluated by vendor audit and NLI testing. The fault areas that will be evaluated include programming or logic errors, problems with hardware/software integration, potential for unintended functions, potential for data handling problems, module interface including protocols and control and data linkages and hardware defects. Table 6.1 of this plan identifies the faults that will be addressed.

#### **4.8 Loss of Power**

NLI testing will verify that the trip unit reinitializes and restarts following loss of power with no loss of programming.

By design and construction, the ASIC device is designed to be unpowered for an indefinite amount of time.

#### **4.9 Overcurrent Condition**

One of the safety functions of the trip unit is to trip the breaker in an overcurrent event in accordance with the published trip curves. The following activities will be performed to verify this attribute:

- ANSI design testing will be performed.
  - This testing has been performed by Square D on the Masterpact breaker with Micrologic trip unit.
  - Additional ANSI design testing is required for each replacement breaker

configuration. This testing will be performed on a plant/replacement breaker specific basis and submitted to the client as part of the design testing.

- The NLI audit of Schneider will verify proper programming of the trip curves.
- NLI validation testing will verify proper programming of the trip curves.
- NLI dedication testing will verify proper programming of the trip curve for a sample of the trip points.

## **5.0 FAILURE MODES AND EFFECTS ANALYSIS**

A detailed failure modes and effects analysis (FMEA) was performed by Schneider Electric. The following actions will be performed by NLI:

- The FMEA will be reviewed by NLI personnel for completeness.
- Potential failures due to the identified ACE's will be addressed as specified in section 4.0 of this plan.
- Additional potential failure modes may be identified during the V&V audits of Schneider or NLI qualification and dedication testing. If additional potential failure modes are identified, the failure modes and effects analysis will be updated.

## **6.0 REQUIRED SYSTEM CHARACTERISTICS**

The required system characteristics that the hardware/software systems must possess are identified in Table 6.1. The methods that will be used to document that the required system characteristics are met are also identified in the table.

The system contains the following hardware/software systems:

- Programmer.

Note: The Schneider audit or NLI Validation Testing may identify additional critical characteristics that are not included in Table 6.1. These critical characteristics will be addressed in the V&V Report.

**TRIP UNIT SOFTWARE V&V CRITICAL CHARACTERISTICS**  
**TABLE 6.1**

“Ref” documents are the plans and reports that are used to verify the critical characteristic, as follows:

- VVP-042181-1: This V&V plan.
- VVTP-042181-1: NLI validation test plan to verify the software/hardware design of the trip unit [13]. These are design tests and will be performed on one of the trip units (test specimen or one production unit).
- VP-042181-1: NLI dedication plan [6]. These production tests and inspections will be performed on both of the supplied trip units.
- QP-042181-1: NLI qualification plan [11].
- SV-042181-1: NLI audit plan for the Schneider Micrologic trip unit facilities [21].
- IM-042181-1: Instruction Manual [14].

<u>Critical Characteristic</u>	<u>Acceptance Criteria</u>	<u>Verification/ Validation Method</u>	<u>Ref.</u>
<b><u>Quality Assurance Program</u></b>			
Quality Assurance Program that controlled the development of the software/hardware.	The software and hardware were developed under the controls of the Schneider ISO 9001 quality program.	Audit of Schneider.	SV-042181-1
<b><u>Software Lifecycle</u></b>			
Software specification/software requirements.	Software specification documents the detailed software requirements.	Audit of Schneider.	SV-042181-1
Procedural controls used during software development.	Software development controlled by Schneider procedures. Document the procedures used and evaluate process.	Audit of Schneider.	SV-042181-1
Failure Modes & Effects Analysis	Failure Modes & Effects Analysis performed and used during software development.	Audit of Schneider. Review of Schneider FMEA. Additional testing if required by NLI.	SV-042181-1 VVTP-042181-1

Development and testing approach.	Schneider developed and tested the software in small function based blocks of code. Development and testing documented.	Audit of Schneider.	SV-042181-1
Independence of software development and testing.	Independent personnel used.	Audit of Schneider.	SV-042181-1
Integrated hardware/software testing.	Integrated testing of the hardware/software system was performed.	Audit of Schneider. NLI Validation and Dedication Testing.	SV-042181-1 VVTP-042181-1 VP-042181-1
Product operating history.	Installed units operating properly. Specify number of operating units, time in service, and number and types of identified problems.	Audit of Schneider.	SV-042181-1
Error handling.	1. Code errors are identified, documented, evaluated, and reported in a controlled manner by Schneider. 2. Mechanism for reporting and evaluating user reported problems.	Audit of Schneider. Per section 8.0 of this plan.	SV-042181-1 VVP-042181-1
Problem reporting to plant.	Identified problems are evaluated and reported to the client.	Per NLI procedures as specified in this VVP, Section 8.0.	VVP-042181-1
Software updates and service bulletins.	Schneider has a formal process to alert customers concerning software updates and provides service bulletins,	Audit of Schneider.	SV-042181-1

**Configuration Control**

Revision control.	Revision control used on code, chips, and boards.	Audit of Schneider. NLI inspection and documentation.	SV-042181-1. VP-042181-1.
Programmer hardware configuration	Hardware per Schneider and NLI design documentation and drawings [5].	NLI testing and inspection	VP-042181-1.
Electrical interfaces including wire, terminations, and grounding.	Per NLI design drawings [5].	NLI testing and inspections.	VP-042181-1
Manufacturing controls of code.	Controls to assure correct code installed on each unit.  Traceability between development and production code is documented.	Audit of Schneider.	SV-042181-1
Regression testing or evaluations.	Regression testing or evaluations performed when code is revised.	Audit of Schneider.	SV-042181-1
<b><u>Software/Hardware Critical Characteristics</u></b>			
Data storage.	Per Schneider design specifications.	Audit of Schneider.	SV-042181-1
Signal conditioning and logic functions	Per Schneider design specifications.	Audit of Schneider. NLI testing.	SV-042181-1 VVTP-042181-1

System response time.	Per Schneider design specifications.	Audit of Schneider. NLI Validation and Dedication Testing.	SV-042181-1 VVTP-042181-1 VP-042181-1
Remote alarms and indications.	The communication features are not considered safety related and will not be connected in the plant.  Local indication is considered non-safety related.  The V&V program will verify that the non-safety related communication and local indication features will not impact the safety related functions of the trip unit.	Audit of Schneider. NLI Validation Testing.	SV-042181-1 VVTP-042181-1
Watchdog timer.	Per Schneider design.	Audit of Schneider.	SV-042181-1
Timing and clock control.	Per Schneider design.	Audit of Schneider.	SV-042181-1
Initialization	Per Schneider design.	Audit of Schneider.	SV-042181-1
Output alarms.	Non-safety related. See above.	Audit of Schneider. NLI Validation Testing.	SV-042181-1 VVTP-042181-1
Features which could impact operation.	No features which could interrupt operation (interruptions, diagnostics, manual inputs, non-essential application programs, unauthorized programs or data modifications).	Audit of Schneider. NLI Validation Testing.	SV-042181-1 VVTP-042181-1

Security.	<p>The base program is on the ASIC chip and cannot be field modified.</p> <p>The trip unit does not contain security. The trip settings can be changed from the front of the trip unit. This must be procedurally controlled by the plant. Note that this is no change from solid state trip units currently used in safety related applications.</p>	Plant configuration control per section 8.3 of this plan.	VVP-042181-1
Year 2000 compliance.	Units recognize dates beyond 12/31/99 correctly.	Audit of Schneider.	SV-042181-1
Processor restart and initialization.	Following removal of power, the trip unit maintains the settings.	Audit of Schneider. NLI Validation Testing.	SV-042181-1 VVTP-042181-1
Data validity checks.	The system contains logic to perform checks of the validity of intermediate results.	Audit of Schneider.	SV-042181-1
Input values	The user inputs are hard wired switches. Therefore, no out of range or invalid input parameters can be input to the system.	Not applicable.	Not applicable.
Loss of input instruments.	Loss of signal from the CT's causes the trip unit to trip the breaker.	NLI testing.	VP-042181-1
Diagnostics	Not applicable. The programming is deterministic and diagnostics are not required.	Not applicable.	Not applicable.

**Human Interface Critical  
Characteristics**

Operation setting switches.	Not applicable. There are no touchpads or computers.	NLI testing.	VP-042181-1
Operation of touchpad or computer.	Not applicable. There are no touchpads or computers.	NLI testing.	VP-042181-1
Setting switch security.	Security as specified above.	Per plant configuration control as specified in section 8.3 of this plan.	VVP-042181-1

**Trip Unit specific hardware/software  
critical characteristics**

Programmer operation on Masterpact NT and NW breakers.	Programmer mounts and interfaces properly with the Masterpact NT and NW breakers, including physical mounting, wiring, CT interface, ratings plug interface, and flux shifter interface.	Audit of Schneider. Validation testing by NLI. Dedication testing by NLI.	SV-042181-1 VVTP-042181-1 VP-042181-1
Programmer interfaces properly with ratings plug.	Programmer + ratings plug provide trip settings per the Square D published trip curves.	Audit of Schneider. Validation testing by NLI. Dedication testing by NLI.	SV-042181-1 VVTP-042181-1 VP-042181-1
Trip settings.	Verify that the trip settings are per the Square D curves.	Audit of Schneider. Validation testing by NLI (test all combinations of settings). Dedication testing by NLI (test representative settings).	SV-042181-1 VVTP-042181-1 VP-042181-1

L, S, I, or G function defeat operates properly.	The function is defeated.  Defeat of the L, S, I, or G functions does not impact operation of the active functions.	Audit of Schneider. Validation testing by NLI.	SV-042181-1 VVTP-042181-1
No spurious tripping.	There is no spurious tripping outside the active trip functions and the trip curve.	Audit of Schneider. Validation testing by NLI.	SV-042181-1 VVTP-042181-1
Non safety functions do not interfere with safety related trip function.	Communications and display functions are non-safety related. The communication feature will not be connected in the plant.  Verify that the communication and display functions will not interfere with the trip function.	Audit of Schneider. Validation testing by NLI.	SV-042181-1 VVTP-042181-1
Breaker position on ASIC failure.	The breaker will remain in the current position upon ASIC failure.	Audit of Schneider. Validation testing by NLI.	SV-042181-1 VVTP-042181-1
Indication on ASIC failure.	If the ASIC fails, and LED on the front of the trip unit will light.	Audit of Schneider. Validation testing by NLI.	SV-042181-1 VVTP-042181-1
Short circuit protection on ASIC failure.	If the ASIC fails, the trip unit will still provide short circuit protection.	Audit of Schneider. Validation testing by NLI.	SV-042181-1 VVTP-042181-1
Battery function.	The battery is not required for the safety related trip function.	Audit of Schneider. Validation testing by NLI.	SV-042181-1 VVTP-042181-1

**ACE's Critical Characteristics**

The following ACE's are identified:

- Environmental service conditions.
- Seismic service conditions.
- EMI/RFI.
- Voltage range (undervoltage to overvoltage).
- Infant mortality of electronics.
- Fault in non-safety plant system.
- Hardware/software faults
- Loss of power.

Programmer operates properly when exposed to the identified ACE's. NLI testing.

The referenced QP and VP document the specific requirements and acceptance criteria for each ACE.

VP-042181-1  
QP-042181-1

## **7.0 IMPLEMENTATION OF REQUIRED CHARACTERISTICS**

The activities identified in this section will be performed to verify that trip unit possesses the required characteristics identified in section Table 6.1.

### **7.1 Commercial Grade Audit of Square D/Schneider**

The firmware was developed by Schneider under the controls of their commercial ISO 9001 quality assurance program. NLI will perform a commercial grade audit of the Schneider design and manufacturing facility.

The audits will include review of the controlling procedures and implementation of the critical characteristics specified in Table 6.1.

The documents which are reviewed will be identified in the audit report. The Schneider documents which are made available to NLI will be maintained in accordance with the NLI Quality Assurance Program. Some Schneider documents are proprietary to Schneider and will be reviewed during the audit but will not be released to NLI.

### **7.2 NLI Testing**

Testing and analysis will be performed by NLI to fully document the V&V of the trip units. The testing and analysis address the critical characteristics identified in Table 6.1.

#### **7.2.1 Qualification Testing**

Qualification testing and analysis will be performed in accordance with the qualification plan [11]. The testing will be performed on a single test specimen which is the same configuration as the production units which are being delivered. This testing will include the following:

- EMI/RFI testing.
- Seismic testing.
- Mild environment analysis.

#### **7.2.2 Dedication Testing**

100% of the production units will be dedicated to verify the functional requirements of the computer based systems are met. The dedication will be based on testing as identified in dedication plan VP-042181-1 [6]. The testing specified in the dedication plan will be performed at the NLI facility and/or the Square D facility with NLI personnel witnessing the testing. The dedication testing will include the applicable ANSI Production Tests.

The characteristics that will be verified by testing are identified in Table 6.1.

### **7.2.3 Software/Hardware Design Testing**

NLI will perform supplemental validation testing [13] to verify that the trip units meet the Schneider design specifications. This testing will supplement the data collected during the audit of Schneider.

The characteristics that will be verified by testing are identified in Table 6.1.

### **7.2.4 ANSI Design Testing**

The Masterpact breaker with the Micrologic trip unit has previously been design tested per the applicable ANSI requirements.

Additional design testing will be performed on each replacement breaker configuration in accordance with the requirements of ANSI C37.59 [16].

The ANSI design tests will be submitted to the client.

## **8.0 CONFIGURATION CONTROL**

### **8.1 As-Supplied Configuration**

The NLI Digital Component Configuration Data Sheets [22] will document the as-supplied hardware and firmware configuration. The data sheets will contain the following information for the each trip unit:

- Programmer part number and serial number.
- Chip and firmware part number and revision number, as available.

### **8.2 Vendor Firmware Configuration Control**

The following process will be used to identify, document, evaluate, and report firmware modifications and errors:

- The as-built firmware configuration of the supplied units will be documented and controlled as specified in section 8.1 of this plan.
- NLI will contact Schneider every 6 months and any modifications or reported errors will be identified.
- Errors will be documented and evaluated in accordance with the NLI Nonconformance Report (NCR) process [15]. Notification in accordance with 10CFR21 will be made in accordance with NLI procedures [15], if required.
- Design changes which are not the result of errors will be evaluated by NLI for impact on the existing system and future replacement trip units.
- NLI will submit all NCR's and 10CFR21 reports associated with the trip unit hardware and software to Duke Power. Evaluation of design changes will also be submitted.

This approach is based on the following:

- The Schneider audits and the NLI testing will verify the as-supplied configuration.
- Schneider will not make the source codes available to NLI. Schneider will not freeze the hardware or software configuration.
- Schneider has a controlled program for the following activities (to be verified in the audit):
  - Document revisions to hardware and software.
  - Perform regression testing and/or analysis to fully evaluate the impact of the hardware and software changes on the system. The test method and results are documented in an auditable form.

### **8.3 Plant Lifetime Configuration Control**

Configuration control following delivery of the equipment is the responsibility of the nuclear plant. It is recommended that the configuration control procedures address the following issues:

- Changes to the trip settings using the switches on the front of the trip unit must be procedurally controlled. Note that the same procedural controls are currently implemented on existing solid state trip units.

There are no methods for the user to change the firmware, so no additional controls are required.

## **9.0 EVALUATION OF RESULTS**

### **9.1 Anomalies**

Any anomalous behavior identified during any phase of testing will be documented and evaluated. The evaluation will determine whether the anomaly was due to equipment malfunction, test conditions or an unrelated cause such as improper test setup. If the anomaly was due to the equipment or test conditions, its impact on the safety function of the specimen will be determined. The anomaly disposition will be in one of the following manners based on engineering evaluation:

- No impact on operational requirements or safety function.
- Anomaly acceptable.
- Retest.
- Item not suitable for function/service conditions.

Anomalies which are due to unrelated causes will be identified as such, and the test will be continued.

Anomalies will be documented using the Test Anomaly Form 9.1.

### **9.2 Modifications**

Any modifications made to the test specimen prior to or during the testing sequence will be fully

documented and evaluated. The impact of the modifications on the qualification of the production units will be determined. If the modification has an impact on the qualification of the production units, a retest or partial retest of the test specimen will be performed in the modified configuration. If it can be determined by analysis that the modification has no impact on the qualification of the production units, a retest will not be required. All required retesting and analyses will be documented in the qualification report.

### **9.3 Results/Conclusions**

The results of the V&V activities will be presented in a report. The results will include a positive statement regarding the qualification status of the test specimen and the feasibility of a common cause failure mechanism within the hardware or software.

## **10.0 QUALITY ASSURANCE**

Project activities will be performed in accordance with the NLI Quality Assurance Program which meets the requirements of 10CFR50 Appendix B, 10CFR21 and ASME NQA-1 [1].

**TEST ANOMALY**  
*Form 9.1*

date: \_\_\_\_\_  
Anomaly #: \_\_\_\_\_

**A. IDENTIFICATION**

Test Specimen/Procedure/Equipment: \_\_\_\_\_  
Test Procedure/Step: \_\_\_\_\_  
  
Description:

**B. DISPOSITION**

\_\_\_\_\_

Prepared by: \_\_\_\_\_ date: \_\_\_\_\_  
Reviewed by: \_\_\_\_\_ date: \_\_\_\_\_  
Approved by: \_\_\_\_\_ date: \_\_\_\_\_

## 11.0 MEASUREMENT & TEST EQUIPMENT

Measurement & Test Equipment used will be controlled by the NLI M&TE program (procedure NLI-QUAL-05, Revision 4). The Qualification Report will identify the M&TE which was used. A statement will be made in the Qualification Report as to whether the M&TE are traceable to NIST or equivalent standards.

## 12.0 DOCUMENTATION

A Software Verification & Validation Report will be prepared which summarizes the testing, audits, and evaluations which were performed. The test data sheets, supporting calculations, and any other relevant data will be included in the report, where applicable.

## 13.0 REFERENCES

1. NLI Quality Assurance Manual, Rev. 1, 7/91 including applicable Supplements.
2. IEEE Std 7-4.3.2-1993, "IEEE Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations."
3. IEEE 323-1974/1983, "IEEE Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations."
4. IEEE 344-1975/1987, "IEEE Recommended Practices for Seismic Qualification of Class 1E Equipment for Nuclear Power Generating Stations."
5. NLI design drawings for replacement breaker (project specific). | 
6. NLI dedication plan (project specific).
7. EPRI TR-102348, "Guidelines for Licensing of Digital Upgrades", 12/1993.
8. IEEE 730-1989, "Software Quality Assurance Plans."
9. IEEE 1012-1986, "Standard for Software Verification and Validation Plans."
10. IEEE 1028-1988, "IEEE Standard for Software Review and Audits."
11. NLI qualification plan (project specific). | 
12. EPRI TR-102323, "Guidelines for Electromagnetic Interference Testing in Power Plants", revision 1.
13. NLI Software/Hardware Validation Test Plan, VVTP-042181-1, (latest revision).
14. NLI Instruction Manual (project specific). | 

15. NLI Procedure NLI-QUAL-08, "Nonconformances and 10CFR21 Reporting," (latest revision).
16. (not used)
17. ASME NQA-1a-1995, Appendix 7A-2, "Nonmandatory Guidance for Commercial Grade Items", 1995.
18. EPRI 5652, "Guidelines for the Utilization of Commercial Grade Items in Nuclear Safety-Related Applications."
19. EPRI TR-102323, "Guidelines for Electromagnetic Interference Testing in Power Plants", 9/94.
20. (not used).
21. NLI Source Verification Plan SV-042181-1, "Source Verification Plan for Schneider Programmer", (latest revision).
22. NLI drawings (project specific), "Digital Component Configuration Data Sheet". | Δ
23. IEEE C37.81-1989, "IEEE Guide for Seismic Qualification of Class 1E Metal-Enclosed Power Switchgear Assemblies".
24. IEEE C37.82-1987, "IEEE Standard for the Qualification of Switchgear Assemblies for Class 1E Applications in Nuclear Power Generating Stations".
25. IEEE 384-1977/1981/1992, "Criteria for Separation of Class 1E Equipment and Circuits". | Δ
26. NRC R.G. 1.75, "Physical Independence of Electrical Systems".
27. NRC R.G. 1.89, "Qualification of Class 1E Equipment for Nuclear Power Plants".
28. NRC R.G. 1.100, "Seismic Qualification of Class 1E Equipment for Nuclear Power Plants".

**Attachment A**

**Equipment Data Sheets**

**The equipment data sheets/technical data will be included in the V&V report.**



## **Attachment B**

### **Seismic RRS**

**The seismic RRS are plant specific and the seismic qualification will be performed with the trip unit installed on the specific replacement breaker type. The seismic RRS and TRS will be included in the seismic qualification report for each breaker type/nuclear plant.**



**ATTACHMENT E**

**NLI Validation Test Plan VVTP-042181-2**

**Item Verification Plan**

Verification Plan # VVTP-042181-2, Revision 2  
 Manuf./Model: Square D (Schneider Electric) / Micrologic 6.0P Programmer  
 Identification: Digital trip device for Square D Masterpact NT and NW low voltage switchgear circuit breakers  
 Safety Function: To maintain low voltage power circuits during normal operation and interrupt circuits during fault conditions.  
 Note: This verification plan is a supplement to VVTP-042181-1 and is used in order to test the 4-wire ground fault/neutral protection configuration. The 3-wire ground fault configuration and ground fault trip times have previously been validated.

Critical Characteristic	Sample Size	Acceptance		
		Criteria	Ref	Method
Long-time neutral protection CC#1	1	Acceptance criteria is per the attached test data table.	1, 2, 3	Connect a Masterpact circuit breaker with a Micrologic 6.0P programmer, type A rating plug, 400A sensor plug and external neutral current transformer model S34036. See Ref. 1 for proper wiring. The breaker referenced on the wiring diagram is not the test specimen. Keep the wiring from the current transformer to the trip unit as short as possible. Using a Micrologic test set, defeat the ground fault protection. Use this test setup for all CC's.  Perform long-time primary injection testing on the neutral line per the attached test data table.
Short-time neutral protection CC#2	1	Acceptance criteria is per the attached test data table.	2, 3, 4	Perform short-time primary injection testing on the neutral line per the attached test data table.
Instantaneous neutral protection CC#3	1	Acceptance criteria is per the attached test data table.	2, 5	Perform instantaneous primary injection testing on the neutral line per the attached test data table.

**Item Verification Plan**

Verification Plan # VVTP-042181-2, Revision 2  
 Manuf./Model: Square D (Schneider Electric) / Micrologic 6.0P Programmer  
 Identification: Digital trip device for Square D Masterpact NT and NW low voltage switchgear circuit breakers  
 Safety Function: To maintain low voltage power circuits during normal operation and interrupt circuits during fault conditions.  
 Note: This verification plan is a supplement to VVTP-042181-1 and is used in order to test the 4-wire ground fault/neutral protection configuration. The 3-wire ground fault configuration and ground fault trip times have previously been validated.

Critical Characteristic	Sample Size	Acceptance		
		Criteria	Ref	Method
Neutral CT signal communicates with ground-fault logic of programmer CC#4	1	Acceptance criteria is per the attached test data table.	2, 6	Verify the ground fault logic accounts for the neutral CT signal by primary injection testing per the attached test data table. The neutral current must be the opposite polarity of the phase current. Apply the test current for at least 5 seconds or until the breaker trips. Return the breaker to its original configuration upon completion of testing.



- References:
1. NLI Drawing No. 042181-WD1-AC-SR-2N, Revision 3 (attached).
  2. Schneider Electric Class 0613 Manual, "Masterpact NT and NW Universal Power Circuit Breakers", dated 2004.
  3. Square D Curve No. 0613TC0004, dated 6/01 (attached).
  4. Square D Curve No. 0613TC0005, dated 6/01 (attached).
  5. Square D Curve No. 0613TC0007, dated 6/01 (attached).
  6. Square D Curve No. 0613TC0001, dated 6/01 (attached).

Approval \_\_\_\_\_ Prepared: *JAL* 8/17/05 Reviewed: *MAL* 8/18/05 Approved: *Amel* 8/18/05  
 date date date

Trip Function	LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	i <sup>2</sup> t setting (ST, GF)	Neutral setting	test current / trip time acceptance criteria	Actual trip time of breaker (sec)
CC#1 Neutral Protection (LT @ 300%)	0.4	0.5	10	0.4	Off	J	0.4	off, off	1.6N	768A 1.6 – 2.2 sec	
CC#1 Neutral Protection (LT @ 300%)	0.45	1	10	0.4	Off	J	0.4	off, off	1.6N	864A 3.5 – 5 sec	
CC#1 Neutral Protection (LT @ 300%)	0.5	2	10	0.4	Off	J	0.4	off, off	1.6N	960A 6.8 – 9.2 sec	
CC#1 Neutral Protection (LT @ 300%)	0.6	4	10	0.4	Off	J	0.4	off, off	1N	720A 12 – 18 sec	
CC#1 Neutral Protection (LT @ 300%)	0.63	8	10	0.4	Off	J	0.4	off, off	1N	756A 27 – 37 sec	
CC#1 Neutral Protection (LT @ 300%)	0.7	12	10	0.4	Off	J	0.4	off, off	1N	840A 41 – 51 sec	
CC#1 Neutral Protection (LT @ 300%)	0.8	16	10	0.4	Off	J	0.4	off, off	1/2N	480A 51 – 65 sec	
CC#1 Neutral Protection (LT @ 300%)	0.9	20	10	0.4	Off	J	0.4	off, off	1/2N	540A 65 – 83 sec	



Trip Function	LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	i <sup>2</sup> t setting (ST, GF)	Neutral setting	test current / trip time acceptance criteria	Actual trip time of breaker (sec)
CC#1 Neutral Protection (LT @ 300%)	1	24	10	0.4	Off	J	0.4	off, off	1/2N	600A 83-130sec	
CC#2 Neutral Protection (ST @ 400%)	1	24	1.5	0	Off	J	0.4	off, off	1.6N	3840A 0.02-0.08sec	
CC#2 Neutral Protection (ST @ 400%)	0.9	24	2	0.1	Off	J	0.4	off, off	1.6N	4608A 0.08-0.14sec	
CC#2 Neutral Protection (ST @ 400%)	0.8	24	2.5	0.2	Off	J	0.4	off, off	1.6N	5120A 0.14-0.20sec	
CC#2 Neutral Protection (ST @ 400%)	0.7	24	3	0.3	Off	J	0.4	off, off	1N	3360A 0.22-0.32sec	
CC#2 Neutral Protection (ST @ 400%)	0.63	24	4	0.4	Off	J	0.4	off, off	1N	4032A 0.35-0.50sec	
CC#2 Neutral Protection (ST @ 125%)	0.6	24	5	0.4	Off	J	0.4	on, off	1N	1500A 0.9-1.7sec	
CC#2 Neutral Protection (ST @ 125%)	0.5	24	6	0.3	Off	J	0.4	on, off	1/2N	750A 0.3-0.6sec	



Trip Function	LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	i <sup>2</sup> t setting (ST, GF)	Neutral setting	test current / trip time acceptance criteria	Actual trip time of breaker (sec)
CC#2 Neutral Protection (ST @ 125%)	0.45	24	8	0.2	Off	J	0.4	on, off	1/2N	900A 0.14-0.20sec	
CC#2 Neutral Protection (ST @ 125%)	0.4	24	10	0.1	Off	J	0.4	on, off	1/2N	1000A 0.08-0.14sec	
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	2	J	0.4	off, off	1.6N	2560A ≤ 0.06sec	
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	3	J	0.4	off, off	1.6N	3840A ≤ 0.06sec	
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	4	J	0.4	off, off	1.6N	5120A ≤ 0.06sec	
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	6	J	0.4	off, off	1N	4800A ≤ 0.06sec	
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	8	J	0.4	off, off	1N	6,400A ≤ 0.06sec	



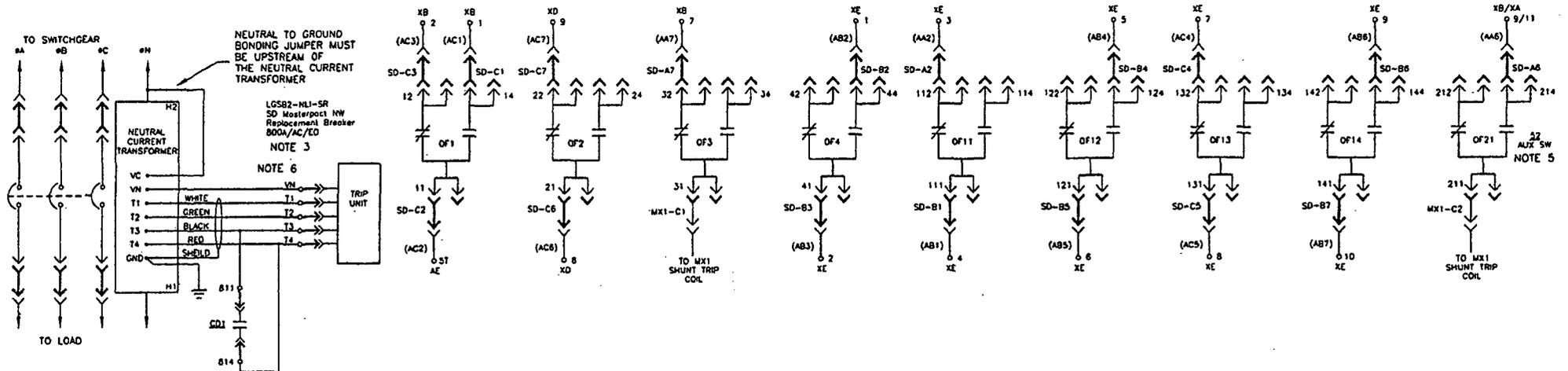
Trip Function	LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	i <sup>2</sup> t setting (ST, GF)	Neutral setting	test current / trip time acceptance criteria	Actual trip time of breaker (sec)
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	10	J	0.4	off, off	1N	8000A ≤ 0.06sec	
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	12	J	0.4	off, off	1/2N	4800A ≤ 0.06sec	
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	15	J	0.4	off, off	1/2N	6000A ≤ 0.06sec	
CC#3 Neutral Protection (Inst. defeated)	1	24	10	0.4	off	J	0.4	off, off	1/2N	4000A 0.35-0.50sec	
CC#3 Neutral Protection Defeated	0.4	0.5	1.5	0.1	off	J	0.4	off, off	off	400A for 60sec (should not trip)	

CC#4

LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	i <sup>2</sup> t setting (ST, GF)	Neutral setting	Test Current for 10 seconds A <sub>φ</sub> , B <sub>φ</sub> , C <sub>φ</sub> , N	Trip time:
1	24	10	0.4	off	A (0.3)	0	off, off	off	+180A, 0, 0, -180A	(acceptance criteria is no trip)
1	24	10	0.4	off	A (0.3)	0	off, off	off	0, +180A, 0, -180A	(acceptance criteria is no trip)
1	24	10	0.4	off	A (0.3)	0	off, off	off	0, 0, +180A, -180A	(acceptance criteria is no trip)
1	24	10	0.4	off	A (0.3)	0	off, off	off	0, 0, +180A, 0	(acceptance criteria is 0.02-0.11 sec)
1	24	10	0.4	off	A (0.3)	0	off, off	off	0, +180A, 0, 0	(acceptance criteria is 0.02-0.11 sec)
1	24	10	0.4	off	A (0.3)	0	off, off	off	+180A, 0, 0, 0	(acceptance criteria is 0.02-0.11 sec)

SWGR	COMPT	BKR NO
10B480	2A	52-48011

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
0	ORIGINAL ISSUE	5/3/05	MB
1	REVISED NEUTRAL CT WIRING, NOTE 6 & ADDED NOTE 7 (ECN#: ECN-042181-14).	6/3/05	MB
2	REVISED RELEASE NUMBER (ECN#: ECN-042181-15).	6/27/05	MB
3	ADDED NOTE 8 (ECN#: ECN-042181-16).	7/20/05	<i>[Signature]</i>



**NOTES:**

- BREAKER SHOWN IN OPEN POSITION.
- THE SD-A, SD-B, AND SD-C SECONDARY CONNECTIONS MATCH EXISTING PSEG GE AKD-6 SWITCHGEAR.
- SEE REFERENCE 2 FOR TRIP DEVICE RATING AND OVERLOAD SETTINGS.
- SEE REFERENCE 3 FOR LISTING OF PSEG BREAKER NUMBERS AND ORIGINAL GE WIRING DIAGRAMS FOR EXTERNAL CONNECTIONS ASSOCIATED WITH THIS WIRING SCHEMATIC.
- NOT ALL AUXILIARY SWITCH CONTACTS ARE SHOWN ON DRAWING. SEE SHEET 1 FOR ALL POSITIONS.
- THE SQUARE-D NEUTRAL CT WILL BE INSTALLED ON THE BUS IN THE EXISTING CUBICLE. THE WIRING WILL BE FIELD WIRED AND INSTALLED. INSTALLATION OF THIS NEUTRAL CT REQUIRES DE-ENERGIZATION OF THE SWITCHGEAR BUS.
- JUMPER OF THE DISCONNECT POSITION SWITCH WILL BE INSTALLED (T4 TO 814 AND T3 AND 811) AND EXISTING JUMPER BETWEEN T1 AND T2 WILL BE REMOVED.
- THE NEUTRAL CURRENT TRANSFORMER USES THE FOLLOWING WIRE: VC AND VN: 14AWG INSULATED, TYPE SIS, 600V, 90 DEG. C, STRANDED WIRE T1 THRU T4 AND GND: ALPHA TFE SHIELDED WIRE, 20AWG, P/N: 45464 OR EQUIVALENT.

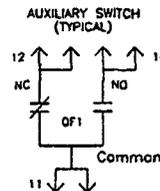
**REFERENCE**

- SQUARE D SERVICES DRAWING NO: AHR89201 (NLI INTERNAL USE ONLY)
- PSEG DRAWING: E-1465-0, ELECTRICAL PROTECTIVE DEVICE SETTINGS.
- NLI DRAWING 042181-ACBRKR-LIST-1A
- PSEG DCP# 80078163

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**LEGEND**

- OF = AUXILIARY CONTACT
- SD = SECONDARY DISCONNECT
- ↔ = CRADLE ASSEMBLY
- ⚡ = CONTROL WIRING



**SAFETY RELATED**

PROJECT: GE AKR REPLACEMENT BREAKER PROJECT FOR HOPE CREEK GENERATING STATION
CLIENT: PUBLIC SERVICE ELECTRIC AND GAS (PSE&G)
BLANKET CONTRACT: 4600001373
RELEASE CONTRACT: 4500282514, 4500303261

<b>NLI</b> NUCLEAR LOGISTICS INC.	
TITLE: INTERNAL WIRING DIAGRAM FOR SDS AC MASTERPACT NW LGSB2 SAFETY RELATED BREAKERS	
Size B	DRAWING No. 042181-WD1-AC-SR-2N
Scale: NTS	WEIGHT: N/A
SHT: 2	OF: 3

DRAWN: <i>[Signature]</i>	Date: 7/19/05
CHECK: <i>[Signature]</i>	Date: 7/19/05
APPROVE: <i>[Signature]</i>	Date: 7/20/05
CUSTOMER:	

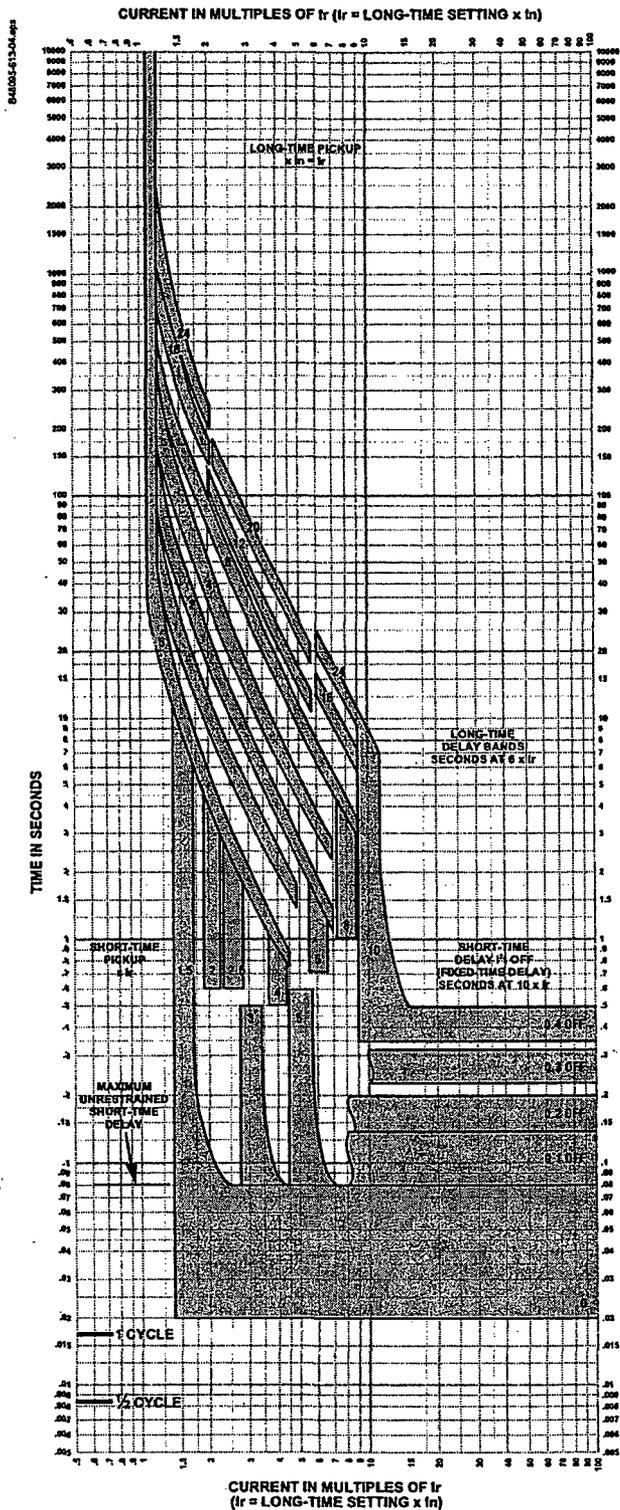
# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves

### MICROLOGIC 5.0/6.0 A/P/H Trip Units

Characteristic Trip Curve No. 613-4

Long-time Pickup and Delay  
Short-time Pickup and I<sup>2</sup>t OFF Delay



The time-current curve information is to be used for application and coordination purposes only.  
Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

#### Notes:

1. There is a thermal-imaging effect that can act to shorten the long-time delay. The thermal-imaging effect comes into play if a current above the long-time delay pickup value exists for a time and then is cleared by the tripping of a downstream device or the circuit breaker itself. A subsequent overload will cause the circuit breaker to trip in a shorter time than normal. The amount of time delay reduction is inverse to the amount of time that has elapsed since the previous overload. Approximately twenty minutes is required between overloads to completely reset thermal-imaging.
2. The end of the curve is determined by the interrupting rating of the circuit breaker.
3. With zone-selective interlocking ON, short-time delay utilized, and no restraining signal, the maximum unrestrained short-time delay time band applies regardless of the setting.
4. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of the current.
5. For a withstand circuit breaker, instantaneous can be turned OFF. See trip curve 613-7 on page 150 for instantaneous trip curve. See trip curve 613-10 on page 153 for instantaneous override values.
6. Overload indicator illuminates at 100%.

Curve No. 0613TC0004  
Drawing No. 048095-613-04



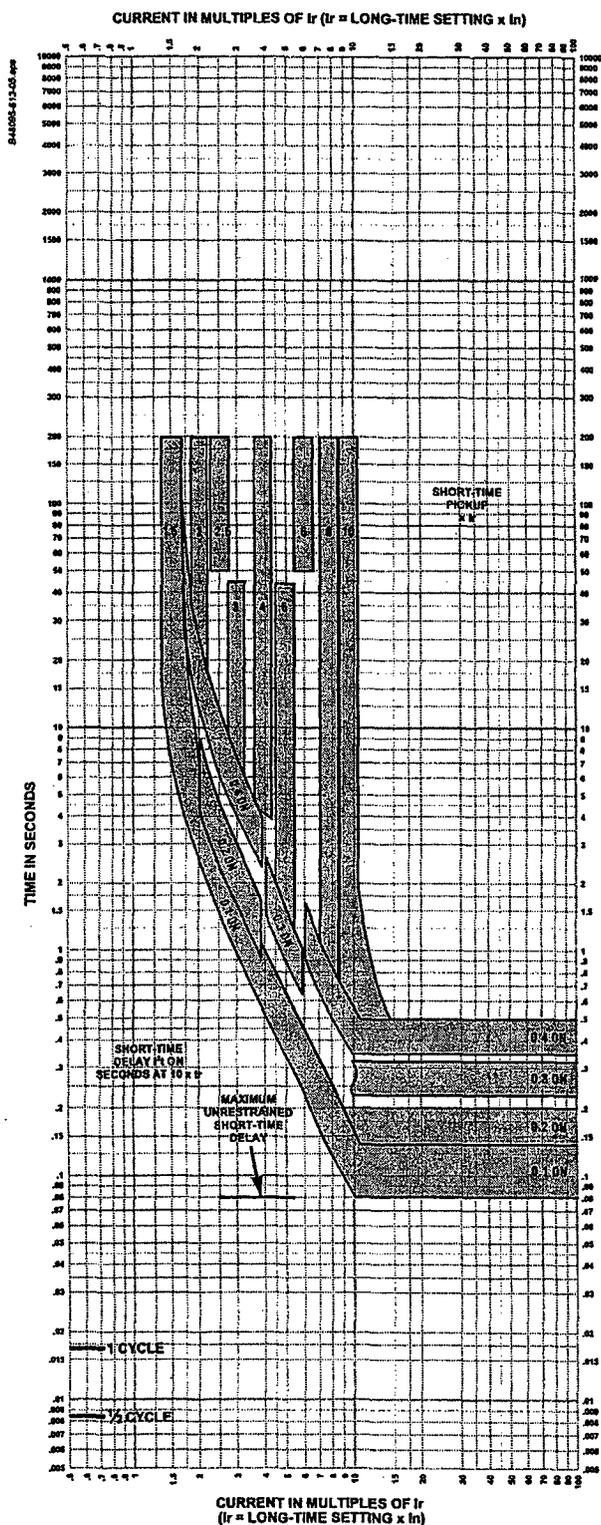
# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves

### MICROLOGIC 5.0/6.0 A/P/H Trip Units

Characteristic Trip Curve No. 613-5

Short-time Pickup and I<sup>2</sup>t ON Delay



The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

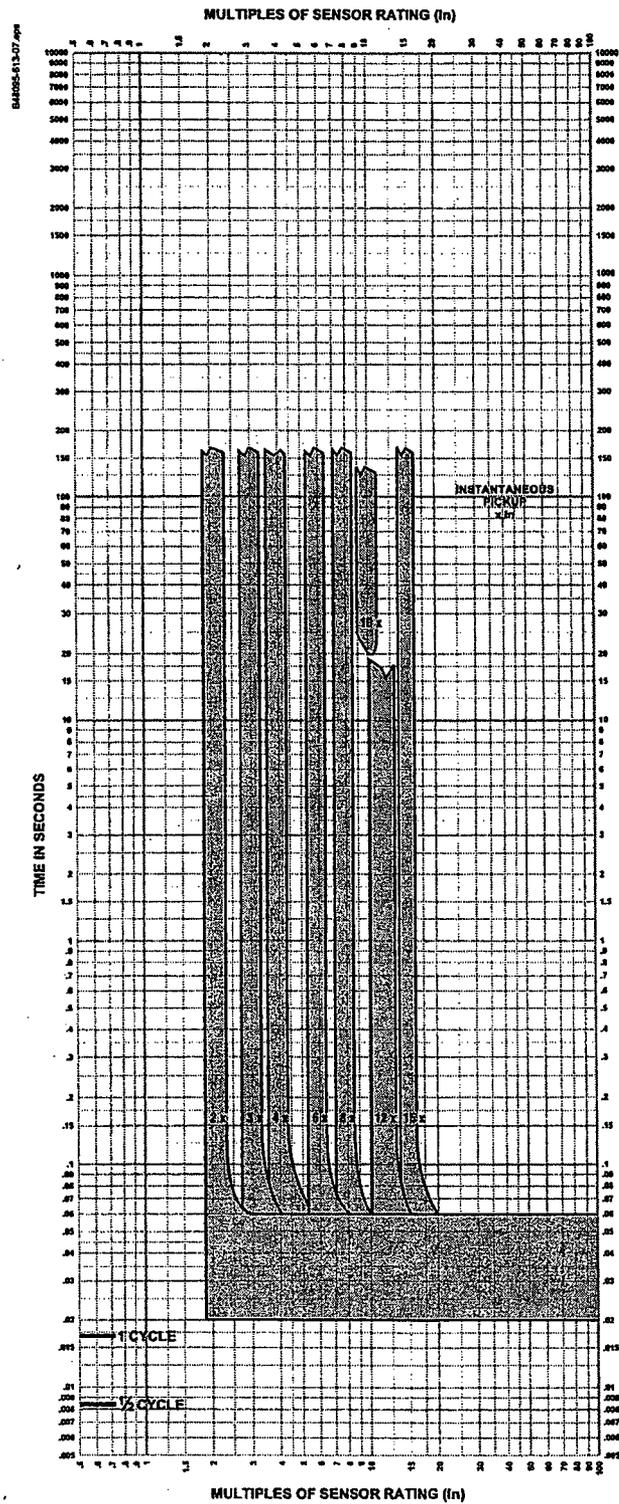
#### Notes:

1. There is a thermal-imaging effect that can act to shorten the long-time delay. The thermal-imaging effect comes into play if a current above the long-time delay pickup value exists for a time and then is cleared by the tripping of a downstream device or the circuit breaker itself. A subsequent overload will cause the circuit breaker to trip in a shorter time than normal. The amount of time delay reduction is inverse to the amount of time that has elapsed since the previous overload. Approximately twenty minutes is required between overloads to completely reset thermal-imaging.
2. The end of the curve is determined by the interrupting rating of the circuit breaker.
3. With zone-selective interlocking ON, short-time delay utilized, and no restraining signal, the maximum unrestrained short-time delay time band applies regardless of the setting.
4. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of current.
5. For withstand circuit breaker, instantaneous can be turned OFF. See trip curve 613-7 on page 150 for instantaneous trip curve. See trip curve 613-10 on page 153 for instantaneous override values.
6. See Trip Curve 613-4 on page 147 for long-time pickup and delay trip curve.

Curve No. 0613TC0905  
Drawing No. 846095-613-05



**MASTERPACT® NT/NW Universal Power Circuit Breakers**  
**Section 7: Trip Curves**



**MICROLOGIC 5.0/6.0 Trip Units**  
**Characteristic Trip Curve No. 613-7**  
**Instantaneous Pickup, 2X to 15X and OFF**

The time-current curve information is to be used for application and coordination purposes only.  
 Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

**Notes:**

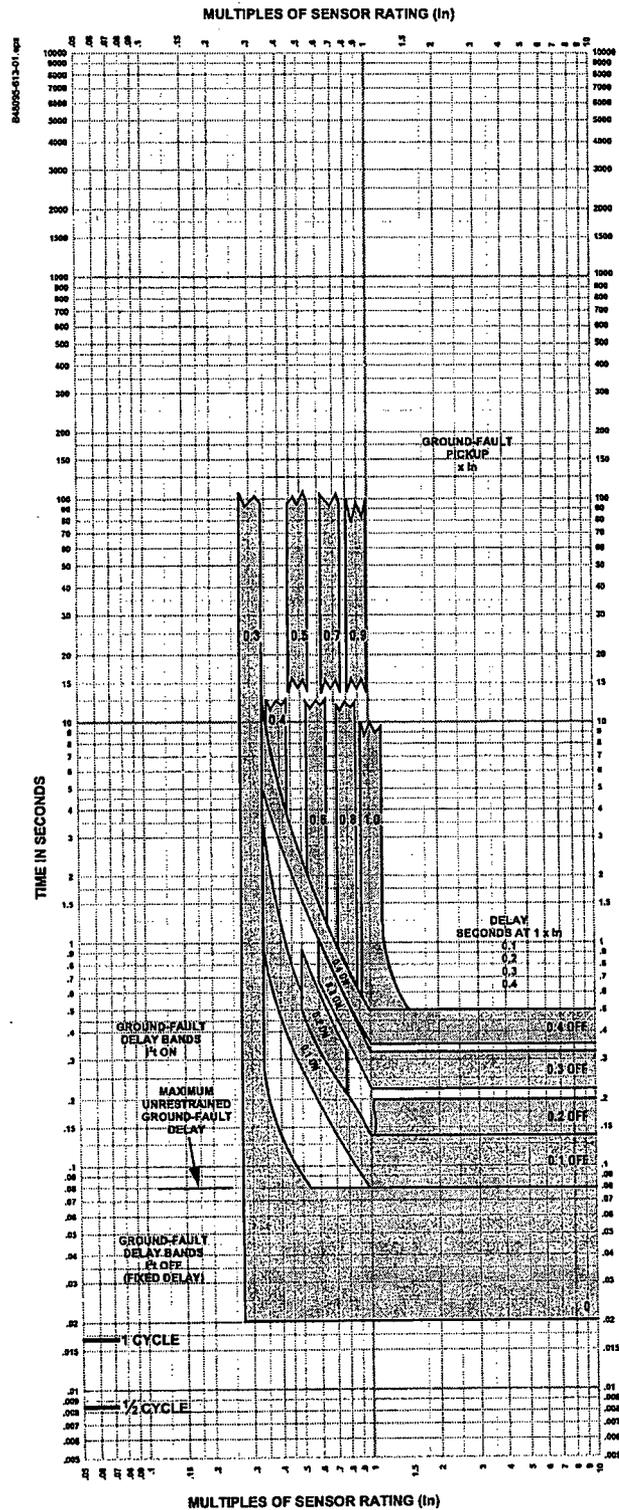
1. The end of the curve is determined by the interrupting rating of the circuit breaker.
2. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of current.
3. The instantaneous region of the trip curve shows maximum total clearing times. Actual clearing times in this region can vary depending on the circuit breaker mechanism design and other factors. The actual clearing time can be considerably faster than indicated. Contact your local sales office for additional information.
4. For a withstand circuit breaker, instantaneous can be turned OFF. See trip curve 613-7 on page 150 for the instantaneous trip curve. See trip curve 613-10 on page 153 for the instantaneous override values.
5. See trip curve 613-4 on page 147 and trip curve 613-5 on page 148 for long-time pickup, long-time delay, short-time pickup and short-time delay trip curves.

Curve No. 0613TC0007  
 Drawing No. 048095-613-07



**MASTERPACT® NT/NW Universal Power Circuit Breakers**  
**Section 7: Trip Curves**

**MICROLOGIC 6.0 A/P/H Trip Units**  
**with Adjustable Ground-fault Pickup and Delay**  
**Characteristic Trip Curve No. 613-1**  
**Ground Fault I<sup>2</sup>t OFF and ON**  
**I<sub>n</sub> ≤ 400 A**



The time-current curve information is to be used for application and coordination purposes only.  
 Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

Curve No. 0613TC0001  
 Drawing No. 848095-613-01



# MASTERPACT® NT/NW Universal Power Circuit Breakers

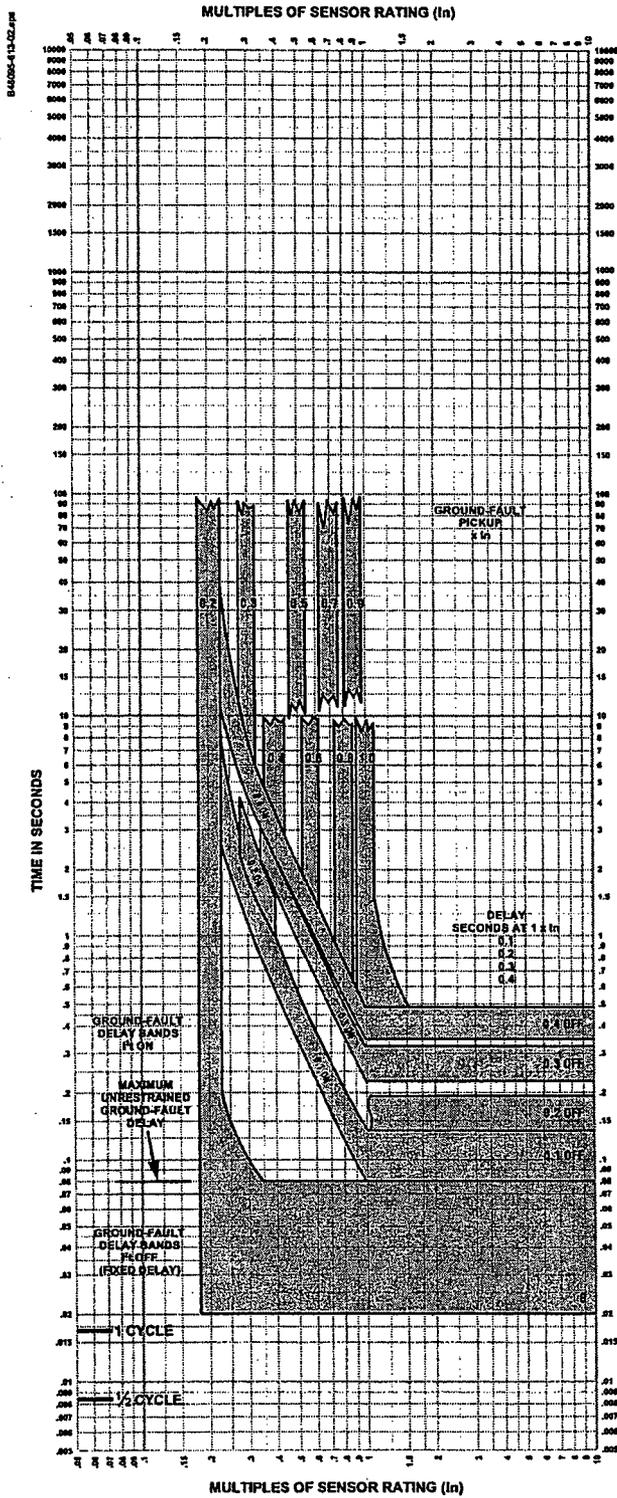
## Section 7: Trip Curves

**MICROLOGIC 6.0 A/P/H Trip Units**  
with Adjustable Ground-fault Pickup and Delay

Characteristic Trip Curve No. 613-2

Ground Fault I<sup>2</sup>t OFF and ON

400 A < I<sub>n</sub> ≤ 1200 A



The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

Curve No. 0613TC002  
Drawing No. B48095-613-02



Trip Function	LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	i <sup>2</sup> t setting (ST, GF)	Neutral setting	test current / trip time acceptance criteria	Actual trip time of breaker (sec)
CC#1 Neutral Protection (LT @ 300%)	0.4	0.5	10	0.4	Off	J	0.4	off, off	1.6N	768A 1.6 - 2.2 sec	1.7 sec.
CC#1 Neutral Protection (LT @ 300%)	0.45	1	10	0.4	Off	J	0.4	off, off	1.6N	864A 3.5 - 5 sec	3.5 3.3 sec T.M. 9-7-05
CC#1 Neutral Protection (LT @ 300%)	0.5	2	10	0.4	Off	J	0.4	off, off	1.6N	960A 6.8 - 9.2 sec	7.0 sec.
CC#1 Neutral Protection (LT @ 300%)	0.6	4	10	0.4	Off	J	0.4	off, off	1N	720A 12 - 18 sec	13.89 sec.
CC#1 Neutral Protection (LT @ 300%)	0.63	8	10	0.4	Off	J	0.4	off, off	1N	756A 27 - 37 sec	27.86 sec.
CC#1 Neutral Protection (LT @ 300%)	0.7	12	10	0.4	Off	J	0.4	off, off	1N	840A 41 - 51 sec	42.37 sec.
CC#1 Neutral Protection (LT @ 300%)	0.8	16	10	0.4	Off	J	0.4	off, off	1/2N	480A 51 - 65 sec	56.88 sec.
CC#1 Neutral Protection (LT @ 300%)	0.9	20	10	0.4	Off	J	0.4	off, off	1/2N	540A 65 - 83 sec	71.45

N  
N x 1.6  
N/2  
off



9/14/05

Trip Function	LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	I <sup>2</sup> t setting (ST, GF)	Neutral setting	test current / trip time acceptance criteria	Actual trip time of breaker (sec)
CC#1 Neutral Protection (LT @ 300%)	1	24	10	0.4	Off	J	0.4	off, off	1/2N	600A 83-130sec	85.55 sec.
CC#2 Neutral Protection (ST @ 400%)	1	24	1.5	0	Off	J	0.4	off, off	1.6N	3840A 0.02-0.08sec	0.04 sec.
CC#2 Neutral Protection (ST @ 400%)	0.9	24	2	0.1	Off	J	0.4	off, off	1.6N	4608A 0.08-0.14sec	0.08 sec.
CC#2 Neutral Protection (ST @ 400%)	0.8	24	2.5	0.2	Off	J	0.4	off, off	1.6N	5120A 0.14-0.20sec	0.16 sec. <span style="border: 1px solid black; padding: 2px;">2</span>
CC#2 Neutral Protection (ST @ 400%)	0.7	24	3	0.3	Off	J	0.4	off, off	1N	3360A 0.22-0.32sec	0.27 sec.
CC#2 Neutral Protection (ST @ 400%)	0.63	24	4	0.4	Off	J	0.4	off, off	1N	4032A 0.35-0.50sec	0.41 sec.
CC#2 Neutral Protection (ST @ 125%)	0.6	24	5	0.4	Off	J	0.4	on, off	1N	1500A 0.9-1.7sec	1.30 sec.
CC#2 Neutral Protection (ST @ 125%)	0.5	24	6	0.3	Off	J	0.4	on, off	1/2N	750A 0.3-0.6sec	0.52 sec.

Trip Function	LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	i <sup>2</sup> t setting (ST, GF)	Neutral setting	test current / trip time acceptance criteria	Actual trip time of breaker (sec)
CC#2 Neutral Protection (ST @ 125%)	0.45	24	8	0.2	Off	J	0.4	on, off	1/2N	900A 0.14-0.20sec	0.18 sec.
CC#2 Neutral Protection (ST @ 125%)	0.4	24	10	0.1	Off	J	0.4	on, off	1/2N	1000A 0.08-0.14sec	0.12 sec.
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	2	J	0.4	off, off	1.6N	2560A ≤ 0.06sec	0.03 sec.
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	3	J	0.4	off, off	1.6N	3840A ≤ 0.06sec	0.03 sec.
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	4	J	0.4	off, off	1.6N	5120A ≤ 0.06sec	0.03 sec.
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	6	J	0.4	off, off	1N	4800A ≤ 0.06sec	0.03 sec.
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	8	J	0.4	off, off	1N	6,400A ≤ 0.06sec	0.03 sec.



Trip Function	LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	i <sup>2</sup> t setting (ST, GF)	Neutral setting	test current / trip time acceptance criteria	Actual trip time of breaker (sec)
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	10	J	0.4	off, off	1N	8000A ≤ 0.06sec	0.03 sec.
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	12	J	0.4	off, off	1/2N	4800A ≤ 0.06sec	0.09 sec. <i>see DR-042181-VV-1</i>
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	15	J	0.4	off, off	1/2N	6000A ≤ 0.06sec	0.10 sec. <i>see DR-042181-VV-1</i>
CC#3 Neutral Protection (Inst. defeated)	1	24	10	0.4	off	J	0.4	off, off	1/2N	4000A 0.35-0.50sec	0.41 sec.
CC#3 Neutral Protection Defeated	0.4	0.5	1.5	0.1	off	J	0.4	off, off	off	400A for 60sec (should not trip)	No Trip e 500.0 sec.

CC#4

LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	I <sup>2</sup> t setting (ST, GF)	Neutral setting	Test Current for 10 seconds A $\phi$ , B $\phi$ , C $\phi$ , N	Trip time:
1	24	10	0.4	off	A (0.3)	0	off, off	off	+180A, 0, 0, -180A	No Trip in 5 sec. (acceptance criteria is no trip)
1	24	10	0.4	off	A (0.3)	0	off, off	off	0, +180A, 0, -180A	No Trip in 5 sec. (acceptance criteria is no trip)
1	24	10	0.4	off	A (0.3)	0	off, off	off	0, 0, +180A, -180A	No Trip in 5 sec. (acceptance criteria is no trip)
1	24	10	0.4	off	A (0.3)	0	off, off	off	0, 0, +180A, 0	0.05 sec. (acceptance criteria is 0.02-0.11 sec)
1	24	10	0.4	off	A (0.3)	0	off, off	off	0, +180A, 0, 0	0.05 sec. (acceptance criteria is 0.02-0.11 sec)
1	24	10	0.4	off	A (0.3)	0	off, off	off	+180A, 0, 0, 0	0.05 sec. (acceptance criteria is 0.02-0.11 sec)

# NLI

## TEST DATA SHEET

NUCLEAR LOGISTICS INC

Check off appropriate tests:

PRE-SEISMIC  POST-SEISMIC  VERIFICATION  OTHER \_\_\_\_\_

Test Data for: VP- VVTP-042181-2, Rev.2 Job Number: 042181 P.E. JI Catalog ID #: N/A

Item Description: Neutral CT Manufacturer: Square D Model/Part No.: S3403L

*(Micrologic 6.0P)*

Provide Summary of Test Results

Check appropriate boxes:

All Items Passed.

List S/N or ID passed below.

Discrepancy Report(s): If yes, identify below:  Yes

No

N/A

Qty passed: 0

S/Ns or ID#

CC#

DR#

20111-001-00001

3

042181-VV-1

Acceptable

Not Acceptable

Initials/Date by PE: JC 9/26/05

Acceptable

Not Acceptable

Initials/Date by PE: \_\_\_\_\_

Other (where applicable)

Record All M&TE Used:

NLI MTE#	Description	Cal. Due Date	NLI MTE#	Description	Cal. Due Date
<u>562</u>	<u>Becker Test Set</u>	<u>6-13-04</u>			

Update M&TE log on computer T.M. 9/8/05  
Initials & Date

NOTES:

Performed By:  Troy Mull Date: 9/8/05  
 Verified by: JAC Date: 9/26/05  
 Approved by: Amber Date: 10/14/05

# DISCREPANCY REPORT

## A. IDENTIFICATION

DR#: 042181-VV-1

Description: VVTP-042181-2, rev. 2, CC#3 specifies the trip time to be  $\leq 0.06$  seconds while testing instantaneous protection. The actual trip times when the neutral protection was set to  $\frac{1}{2}$  N were 0.09 sec. and 0.10 sec.

Affected Hardware/Document/M&TE: VVTP-042181-2, rev. 2; Micrologic trip unit V&V

Initial Evaluation/

Tagging



Conditional Release



Material Hold

Prepared by: *JAL*

date: *9/18/05*

Approved by: *M-B*

date: *9/20/05*

## B. RESOLUTION (Attach additional pages, if required.)

Evaluation: see attached evaluation

Disposition

Acceptable/use as is

Acceptable with limitations noted

Acceptable with ~~rework~~

*on page 3*

Reject/do not use

*additional testing*

*9/20/05*

Code 1 *30*

See NLI-QUAL-06, Rev. II, Table 3.2

Code 2 \_\_\_\_\_

Prepared by: *JAL*

Date: *9/20/05*

Reviewed by: *M-B*

Date: *9/20/05*

Approved by: *Maly*

Date: *9/20/05*

## DISCREPANCY REPORT

Continuation of B. (RESOLUTION)

DR#: 042181-VV-1

Per Square D, the neutral protection instantaneous pickup is only a function of the circuit breaker sensor plug rating and the instantaneous pickup setting. The neutral setting only affects long-time and short-time pickup, not instantaneous pickup. Therefore the current applied while testing instantaneous protection with  $\frac{1}{2}$  N neutral setting is equal to 100% of the instantaneous pickup, not 200% as was intended. The circuit breaker tripped within the tolerances of the trip curve.

Additional testing per the attached table will be performed to properly test the neutral instantaneous protection at 200%.

The V&V testing is acceptable with additional testing.

*The additional testing was performed successfully.*

*✓ 9/26/05*

Trip Function	LT pickup setting (lr)	LT delay setting (tr)	ST pickup setting (lsd)	ST delay setting (tsd)	Inst. pickup setting (li)	GF pickup setting (lg)	GF time delay (tg)	i <sup>2</sup> t setting (ST, GF)	Neutral setting	test current / trip time acceptance criteria	Actual trip time of breaker (sec)
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	2	J	0.4	off, off	1.6N	1600A ≤ 0.06sec	0.03 sec
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	3	J	0.4	off, off	1.6N	2400A ≤ 0.06sec	0.04 sec
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	4	J	0.4	off, off	1.6N	3200A ≤ 0.06sec	0.03 sec
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	12	J	0.4	off, off	1/2N	9600A ≤ 0.06sec	0.04 sec
CC#3 Neutral Protection (Inst. @ 200%)	1	24	10	0.4	15	J	0.4	off, off	1/2N	12 000A ≤ 0.06sec	0.04 sec.

Model No.: Cat# 534036

MTE # 562

Calib. Due Date: 6/13/06

Ser. No.: 20111-001-00001

MTE # \_\_\_\_\_

Calib. Due Date: \_\_\_\_\_

Performed by:  Tracy Muller

Date: 9/26/05

Verified by: [Signature]

Date: 9/26/05

Approved by: [Signature]

Date: 9/26/05

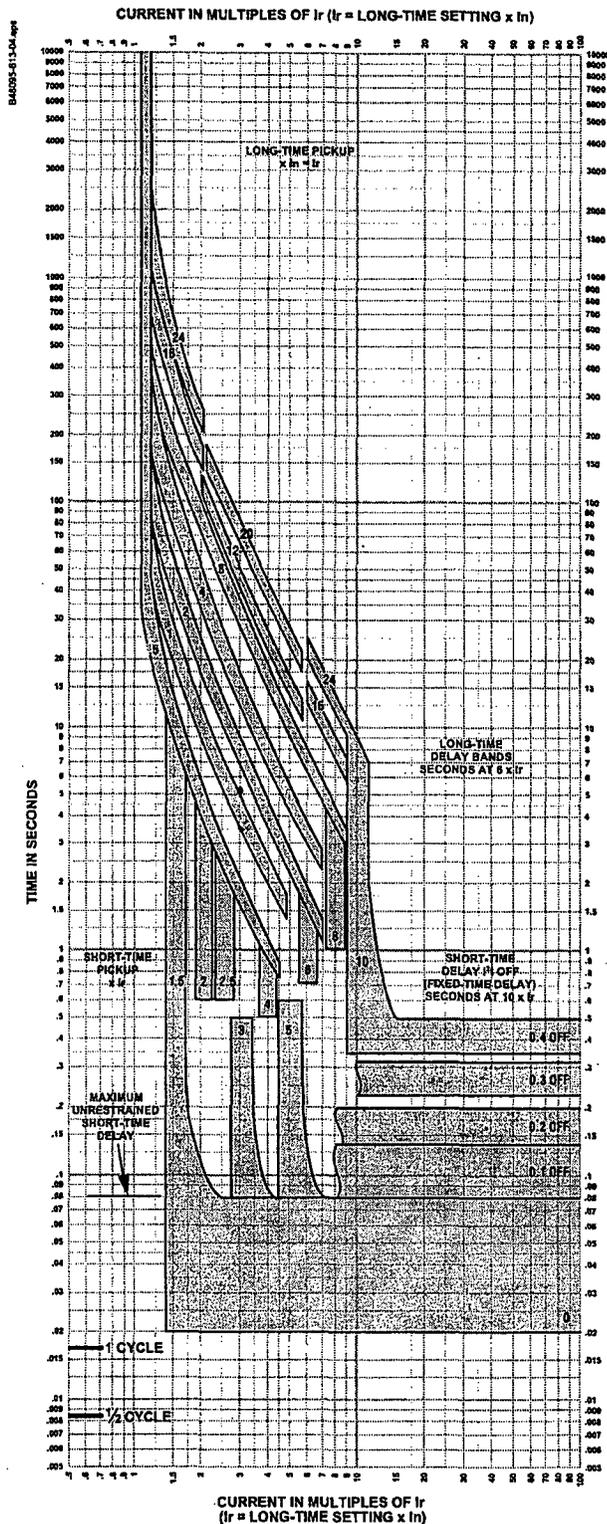
# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves

### MICROLOGIC 5.0/6.0 A/P/H Trip Units

Characteristic Trip Curve No. 613-4

#### Long-time Pickup and Delay Short-time Pickup and I<sup>2</sup>t OFF Delay



The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

**Notes:**

1. There is a thermal-imaging effect that can act to shorten the long-time delay. The thermal-imaging effect comes into play if a current above the long-time delay pickup value exists for a time and then is cleared by the tripping of a downstream device or the circuit breaker itself. A subsequent overload will cause the circuit breaker to trip in a shorter time than normal. The amount of time delay reduction is inverse to the amount of time that has elapsed since the previous overload. Approximately twenty minutes is required between overloads to completely reset thermal-imaging.
2. The end of the curve is determined by the interrupting rating of the circuit breaker.
3. With zone-selective interlocking ON, short-time delay utilized, and no restraining signal, the maximum unrestrained short-time delay time band applies regardless of the setting.
4. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of the current.
5. For a withstand circuit breaker, instantaneous can be turned OFF. See trip curve 613-7 on page 150 for instantaneous trip curve. See trip curve 613-10 on page 153 for instantaneous override values.
6. Overload indicator illuminates at 100%.

Curve No. 0613TC0004  
Drawing No. 848095-613-04



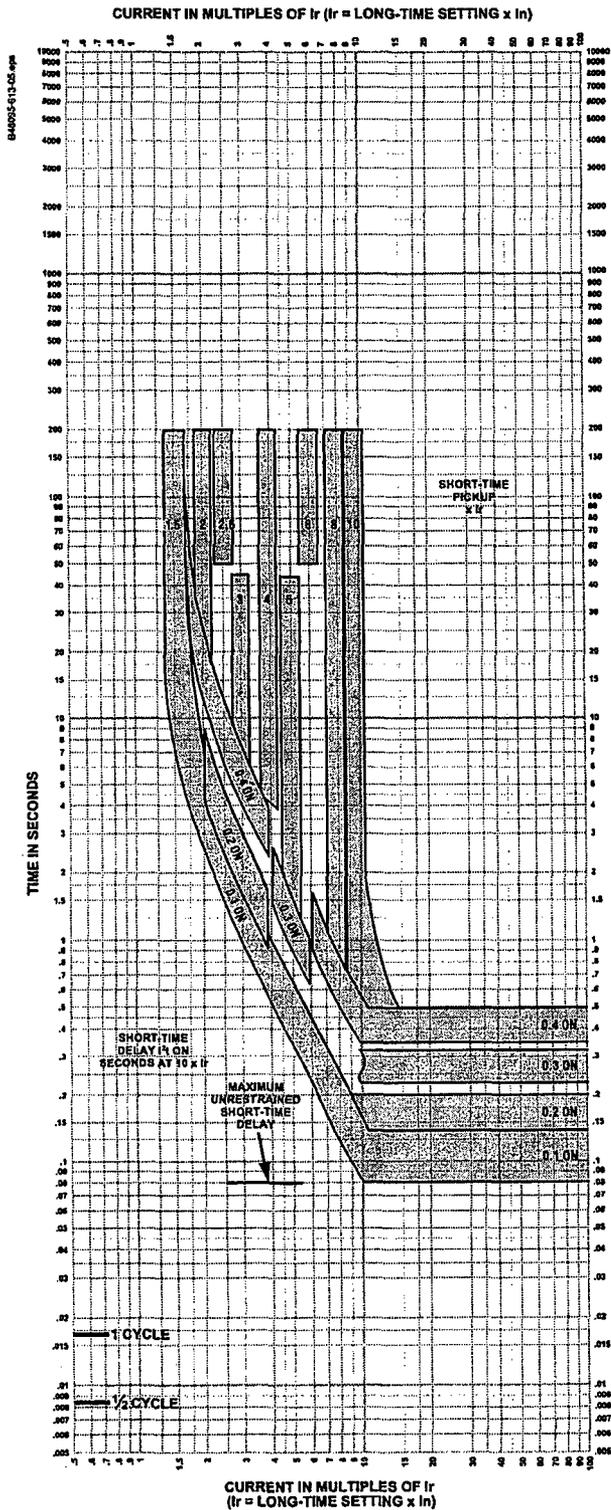
# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves

### MICROLOGIC 5.0/6.0 A/P/H Trip Units

Characteristic Trip Curve No. 613-5

Short-time Pickup and I<sup>2</sup>t ON Delay



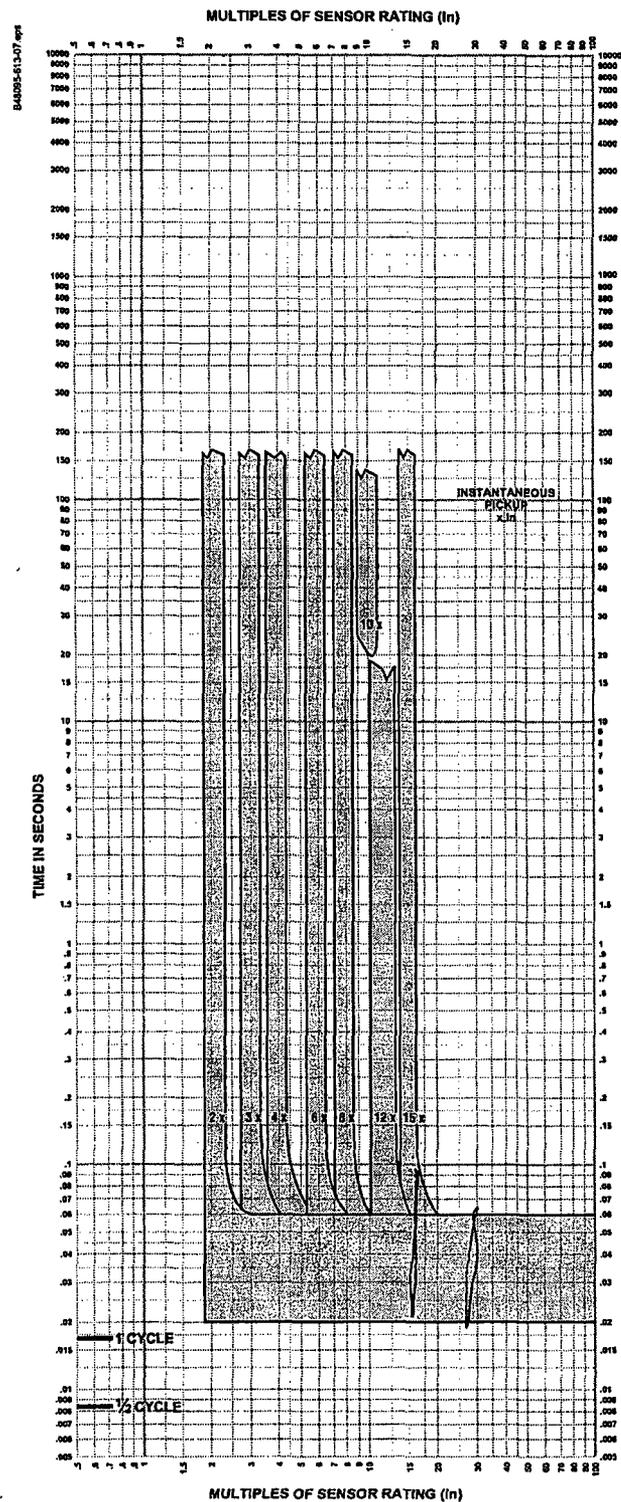
The time-current curve information is to be used for application and coordination purposes only.  
Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

**Notes:**

1. There is a thermal-imaging effect that can act to shorten the long-time delay. The thermal-imaging effect comes into play if a current above the long-time delay pickup value exists for a time and then is cleared by the tripping of a downstream device or the circuit breaker itself. A subsequent overload will cause the circuit breaker to trip in a shorter time than normal. The amount of time delay reduction is inverse to the amount of time that has elapsed since the previous overload. Approximately twenty minutes is required between overloads to completely reset thermal-imaging.
2. The end of the curve is determined by the interrupting rating of the circuit breaker.
3. With zone-selective interlocking ON, short-time delay utilized, and no restraining signal, the maximum unrestrained short-time delay time band applies regardless of the setting.
4. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of current.
5. For withstand circuit breaker, instantaneous can be turned OFF. See trip curve 613-7 on page 150 for instantaneous trip curve. See trip curve 613-10 on page 153 for instantaneous override values.
6. See Trip Curve 613-4 on page 147 for long-time pickup and delay trip curve.

# MASTERPACT® NT/NW Universal Power Circuit Breakers

## Section 7: Trip Curves



### MICROLOGIC 5.0/6.0 Trip Units

Characteristic Trip Curve No. 613-7

Instantaneous Pickup, 2X to 15X and OFF

The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

#### Notes:

1. The end of the curve is determined by the interrupting rating of the circuit breaker.
2. Total clearing times shown include the response times of the trip unit, the circuit breaker opening, and the extinction of current.
3. The instantaneous region of the trip curve shows maximum total clearing times. Actual clearing times in this region can vary depending on the circuit breaker mechanism design and other factors. The actual clearing time can be considerably faster than indicated. Contact your local sales office for additional information.
4. For a withstand circuit breaker, instantaneous can be turned OFF. See trip curve 613-7 on page 150 for the instantaneous trip curve. See trip curve 613-10 on page 153 for the instantaneous override values.
5. See trip curve 613-4 on page 147 and trip curve 613-5 on page 148 for long-time pickup, long-time delay, short-time pickup and short-time delay trip curves.

Curve No. 0613TC0007  
Drawing No. B46095-613-07



# MASTERPACT® NT/NW Universal Power Circuit Breakers

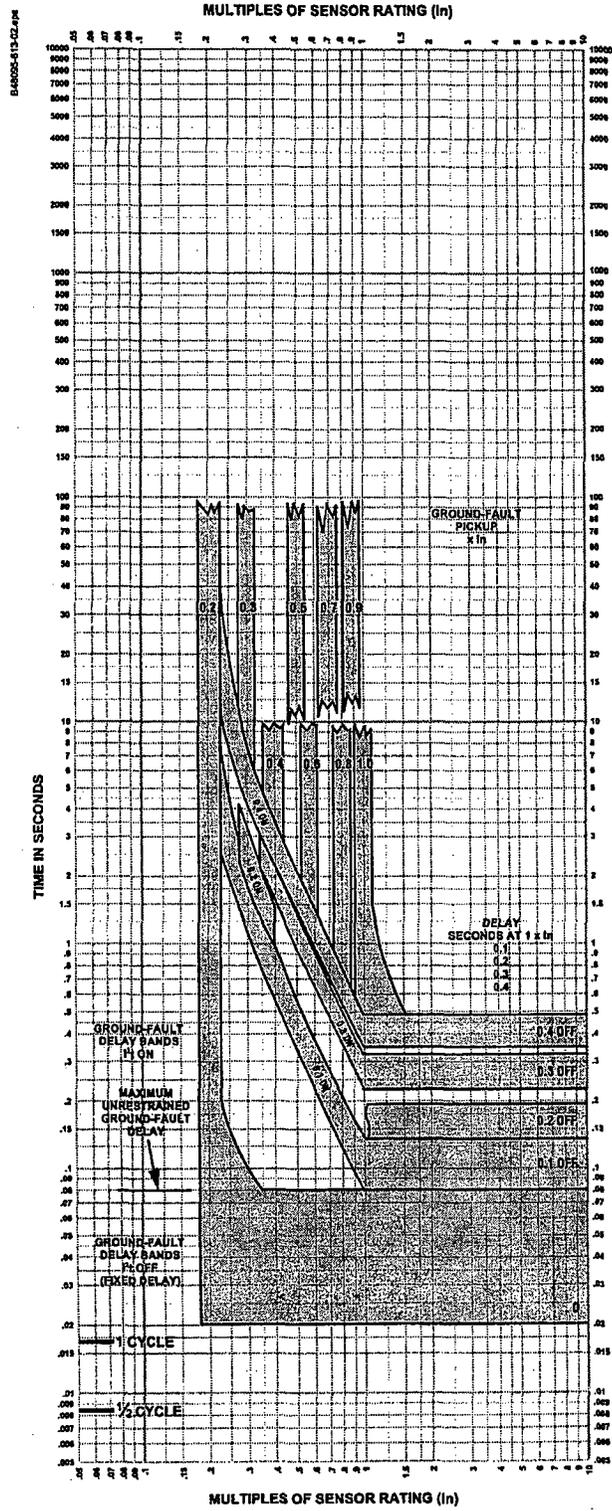
## Section 7: Trip Curves

**MICROLOGIC 6.0 A/P/H Trip Units**  
with Adjustable Ground-fault Pickup and Delay

Characteristic Trip Curve No. 613-2

Ground Fault I<sup>2</sup>t OFF and ON

$$400 \text{ A} < I_n \leq 1200 \text{ A}$$



The time-current curve information is to be used for application and coordination purposes only.

Curves apply from -30°C to +60°C (-22°F to +140°F) ambient temperature.

Curve No. 0613TC0002  
Drawing No. 548095-513-02

