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HFC-6000 Product Line

HFC-SBC06-DPM06 Boards Module Design Specification

System Controller

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Table of Contents

1.	INTRODUCTION	4
2.	FUNCTIONAL DESCRIPTION	5
2.1	EXTERNAL COMMUNICATION	6
2.2	REDUNDANT SYSTEM CONTROLLERS	6
2.3	EXECUTION OF APPLICATION PROGRAMS	9
3.	MODULE ARCHITECTURE.....	9
3.1	MEMORY MAPPING STRUCTURE	12
3.2	PUBLIC MEMORY DATA	13
3.3	REMOTE COMMUNICATION ARCHITECTURE	14
3.3.1	HFC-SBC06 HANDLING OF DDB DATA	16
3.3.2	HFC-SBC06 HANDLING OF UCP MESSAGES	17
3.4	SYS PROCESSOR SECTION	19
3.4.1	SYS PROCESSOR SOFTWARE ARCHITECTURE	21
3.5	ICL PROCESSOR SECTION	25
3.5.1	ICL SOFTWARE ARCHITECTURE	26
3.6	CPC PROCESSOR SECTION	28
3.6.1	CPC PROCESSOR SOFTWARE ARCHITECTURE	29
3.7	HFC-SBC06 AND HFC-DPM06 REDUNDANCY ARCHITECTURE	32
3.8	HFC-SBC06 CPLD DESIGN	35
3.9	SEQUENCE OF EVENTS TIMER	35
3.10	HFC-DPM06 BOARD	36
4.	CONFIGURATION SETUP AND LED DISPLAYS	36
4.1	HFC-SBC06 ONBOARD SWITCH FUNCTIONS	36
4.2	HFC-DPM06 ONBOARD SWITCH FUNCTIONS	37
4.3	HFC-SBC06 ONBOARD JUMPER OPTIONS	37
4.4	LEDS	39
4.4.1	HFC-SBC06 LED FUNCTIONS	39
4.4.1.1	DS3 AND DS4 LEDES	39
4.4.2	HFC-DPM06 LED FUNCTIONS	41

4.5	INSTALLATION OF SYSTEM SOFTWARE AND APPLICATION PROGRAMS	42
4.5.1	SYSTEM CODE TRANSFER TO FLASH.....	42
4.5.2	APPLICATION CODE DOWNLOAD	43
4.5.3	SYSTEM SOFTWARE UPDATES	44
4.6	HARDWARE CONFIGURATION	44
5.	MODULE DESIGN CONSTRAINTS	46
5.1	COMMUNICATION INTERFACE SPECIFICATIONS	46
5.2	OPERATING SYSTEM SPECIFICATION	46
5.3	HARDWARE INTERFACE SPECIFICATIONS	46
5.1	DESIGN SAFETY	46

List of Tables

Table 1.	SYS Processor Configuration Switches.....	37
Table 2.	Jumper Options.....	38
Table 3.	DS3 and DS4 LED Indications for Initialization Failure	40
Table 4.	DS3 and DS4 LED Indications for Individual Tasks	41
Table 5.	DS3 and DS4 LED Failure Indications During Normal Operation.....	41

LIST OF FIGURES

Figure 1.	HFC-6000 System Hierarchy	4
Figure 2.	Redundant HFC-SBC06 Boards with DPM06 Board.....	7
Figure 3.	ICL Network for Redundant Controller Configuration.....	8
Figure 4.	Non-Redundant HFC-SBC06 Board and DPM06 Board.....	9
Figure 5.	HFC-SBC06 / DPM06 Module Architectures.....	11
Figure 6.	Microprocessor Address Space	12
Figure 7.	Public Memory Data Stores.....	13
Figure 8.	DDB Broadcast Data Paths	15
Figure 9.	UCP Point-to-Point Message Path.....	15
Figure 10.	Broadcasting and Filtering of DDB Data	17
Figure 11.	UCP Message Processing.....	18
Figure 12.	System Processor Architecture.....	19
Figure 13.	System Software Architecture.....	23
Figure 14.	ICL Processor Architecture	25
Figure 15.	ICL Software Architecture	27
Figure 16.	CPC Processor Architecture.....	29
Figure 17.	CPC Software Architecture	31
Figure 18.	HFC-SBC06 Redundancy and Failover	33

1. Introduction

The HFC-6000 distributed control system provides plant monitoring and control capabilities, with monitoring and control responsibilities spread over multiple remote control units. The HFC-SBC06 System Controller is the primary board used for implementing plant control functions. This HFC-SBC06-DPM06 Module Design Specification describes the HFC-SBC06 System Controller board and HFC-DPM06 Dual Ported Memory board.

As shown in Figure 1, the HFC-SBC06 System Controller board is positioned in the HFC-6000 system hierarchy between the Operator Station(s), which provides the direct Human Machine Interface to the plant operators, and the I/O boards which provide the signal-level interface to the equipment and devices in the plant.

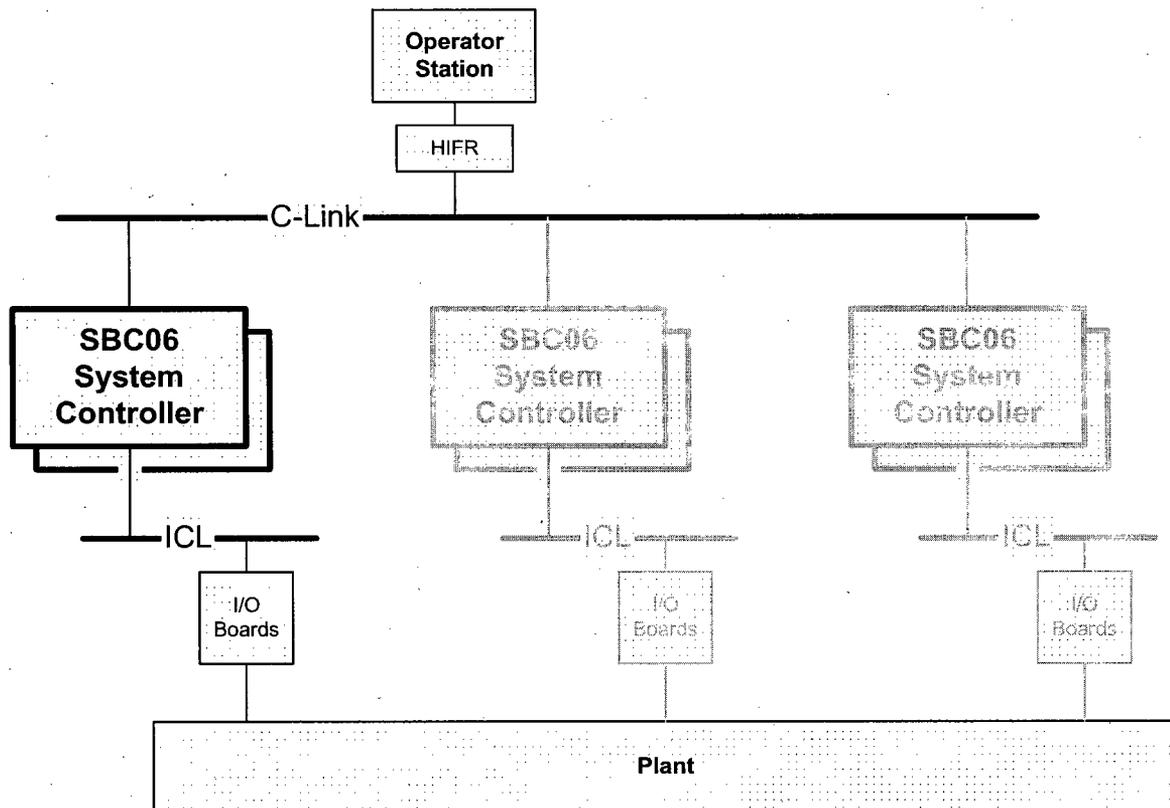


Figure 1. HFC-6000 System Hierarchy

Descriptions of the functional requirements of the HFC-SBC06 System Controller board and HFC-DPM06 board, from an external perspective, are provided in the HFC-6000 Product Line Requirements Specification, RS901-000-01. The design of the HFC-SBC06 and HFC-DPM06

also complies with the detailed requirements spelled out in 700901-04, 700901-05, and RS901-000-37.

The purpose of this document is to describe the operation and functions of the HFC-SBC06 and HFC-DPM06 boards. The discussion of the operation and function of the HFC-SBC06 and HFC-DPM06 will be presented using architectural, design, and implementation information.

Subsequent sections of this document provide architectural and design descriptions of the HFC-SBC06 board. Lower level descriptions of the HFC-SBC06 and HFC-DPM06 are contained in the HFC-SBC06-DPM06 System Controller Module Detailed Design Specification, DS901-000-01. The major functions performed by the HFC-SBC06 and HFC-DPM06 are listed in the next section which contains brief descriptions of the functions and how the HFC-SBC06 or HFC-DPM06 performs the functions.

2. Functional Description

The functions described in this section are the major functions performed by the HFC-SBC06 System Controller. The functional descriptions are presented so as to provide a context for understanding the operation of the HFC-SBC06 and a description of how the functions performed by the HFC-SBC06 System Controller work within the overall architecture of the HFC-6000 distributed control system.

The major functions performed by the HFC-SBC06 System Controller are:

- Communication with other system controllers and workstation PCs connected to the same redundant C-Link (Communication Link), an HFC proprietary network; Broadcasting plant status information;
- Communication with modules connected to the same ICL (Intercommunication Link), another HFC proprietary network; Collecting plant status information and sending plant operation commands;
- Redundant controller operation, System Controller failure detection, failover of the control function to the Secondary System Controller on failure of the Primary System Controller, and maintenance failover.
- Execution of application control programs for the specific control logic;

The following sections supply descriptions of the HFC-SBC06 functional requirements and identify aspects of the HFC-SBC06 that perform functions satisfying the requirements.

2.1 External Communication

Two communication interfaces connect the HFC-SBC06 to other boards and devices in the HFC-6000 system. Two identical 10BaseT interfaces connect the HFC-SBC06 to the redundant fiber optic Communication Link (C-Link) network, an HFC proprietary Ethernet-based network that the HFC-SBC06 uses to transfer data to and from the Operator Stations. Typical data transfers between the Operator Station and a System Controller are operator commands from an Operating Station to the System Controller and plant operation data to the Operator Station. The HFC-SBC06 also uses the C-Link to broadcast its status to other remotes attached to the C-Link.

The other HFC-SBC06 communication interface connects the HFC-SBC06 to the Intercommunication Link (ICL), which is an RS-485 serial network connecting the HFC-SBC06 to its I/O boards. Each HFC-SBC06 has two serial channels (ICL0 and ICL1) with each connecting to different I/O boards. Each serial channel can be linked to up to 32 I/O boards. Input values from plant field devices and output values to plant actuators are transferred between the HFC-SBC06 and I/O boards over the ICL serial network. The ICL network implements a master/slave communication protocol. Only the master can initiate communication, and the slave devices only respond to the master's poll. HFC-SBC06 serves as the master for all communication transfers with its configured ICL stations. Each I/O board operates as a slave node on the ICL network. The HFC-SBC06 polls each configured slave device at regular intervals, and the slave devices receive operation commands in the communication messages and respond with plant status information. Although each HFC-SBC06 board has two physical serial channels connected to different I/O boards, these two physical channels are on one logical link under the ICL protocol, either ICL A or ICL B for the I/O boards. Therefore, each ICL can be linked to up to 64 I/O boards.

Refer to DS002-000-01, C-Link Protocol Component Design Specification, and DS002-000-02, ICL Protocol Component Design Specification for details.

2.2 Redundant System Controllers

The HFC-SBC06 System Controller board is designed to operate in a redundant controller configuration. As shown in Figure 2, a redundant configuration consists of two System Controller boards (HFC-SBC06 A and HFC-SBC06 B) and a HFC-DPM06 dual ported memory board with the DPM06 board installed in between of the two SBC06 boards. Each HFC-SBC06 board in the redundant pair operates in one of two different modes: one board operates in a Primary controller mode, and the other board operates in a Secondary controller mode. Controller mode operation is determined at controller board start-up, with the first HFC-SBC06 to complete its initialization routine becoming the Primary, and the other HFC-SBC06 board defaults to Secondary controller mode.

Each HFC-SBC06 in a redundant pair is connected to redundant C-Link networks for communication with the Operating Station and one of two ICL serial networks that provides communication between the HFC-SBC06 and to each of its I/O boards. Each I/O board connects

with two system controllers via its dual serial ports as shown in Figure 2. The mode (Primary or Secondary) in which the HFC-SBC06 is operating determines how the HFC-SBC06 will use C-Link (Ethernet) and ICL (serial) networks.

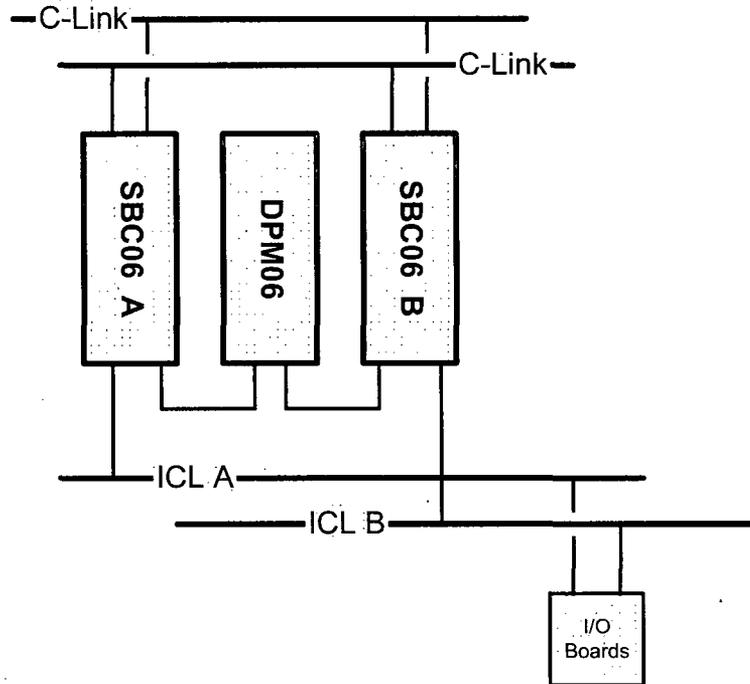


Figure 2. Redundant HFC-SBC06 Boards with DPM06 Board

During redundant operation, the Primary controller periodically copies application and system status data to dual ported memory (DPM) contained on the DPM06 board. The Secondary controller, on the other hand, periodically validates the status data in the DPM and updates its own record of status data if the data is valid. This DPM Transferring Mechanism keeps the secondary controller updated with a current copy of the primary running status and ensures a smooth transition from one controller to the other in the case of failover. During a failover event when control responsibility switches from the Primary to the Secondary, the Secondary uses the most recent application and system status data as an initial state for starting its control of the system. Starting with an initial state that is one second old or less minimizes disturbances to the plant induced by the controller switch over, and prevents potentially hazardous bumping caused by transfer of control. After switch over is complete, the Secondary, which is now the controlling the plant, switches to operation in the Primary control mode. Additional discussion of the failover mechanism is listed DS001-000-08, Failover Mechanism Component Design Specification.

A Maintenance Failover function is supported to perform regular check on the working status of the secondary controller to make sure it will be able to take over the control when the primary controller fails. A pushbutton on the HFC-DPM06 allows failover to be triggered manually.

As shown in Figure 3, the ICL network for a redundant controller configuration includes four physical serial channels for the redundant controllers: ICL A includes ICL A0 and ICL A1 for controller A; ICL B includes ICL B0 and ICL B1 for controller B. A single controller can have up to 64 I/O boards under its control.

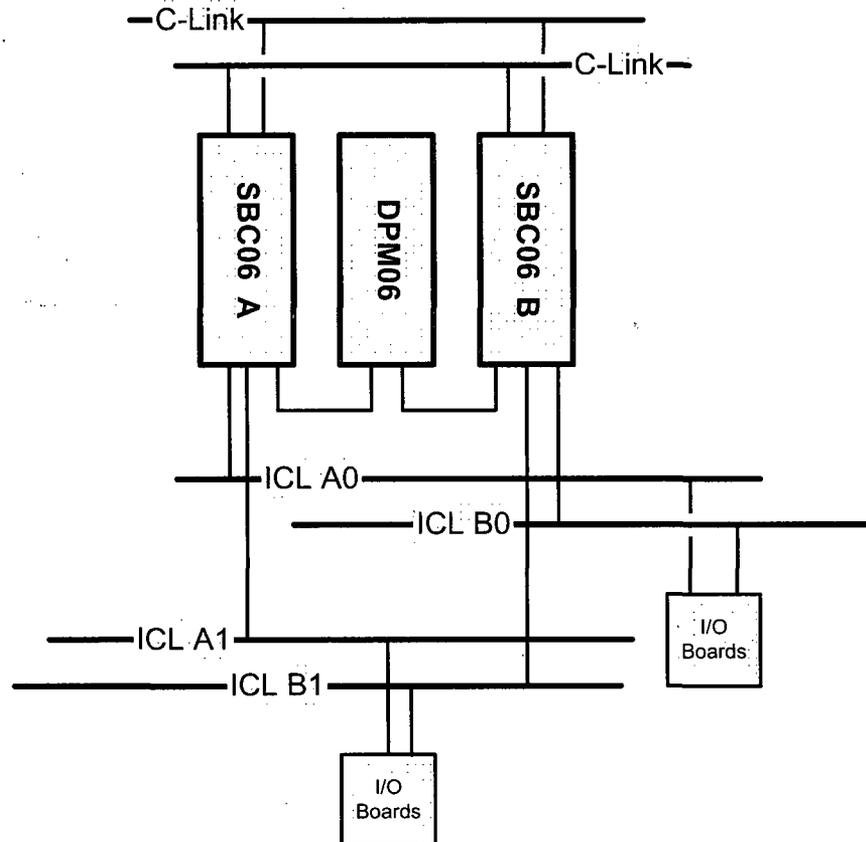


Figure 3. ICL Network for Redundant Controller Configuration

The HFC-SBC06 board may also be configured as a non-redundant System Controller. In a non-redundant configuration, a single HFC-SBC06 is installed in slot 12 or 14 of a 19-inch HFC-6000 controller rack, and a DPM06 is installed in slot 13. (If the system uses 23-inch racks, the controller may be in slot 16 or 18, and the DPM 06 be installed in slot 17.) Configuration switches located on the front edge of the DPM06 board are used to setup a number of system configuration parameters. The HFC-SBC06 must access a DPM06 to read the configuration settings as part of its initialization process.

Another difference between a redundant and non-redundant configuration is that a non-redundant HFC-SBC06 configuration only supports a non-redundant ICL network, as shown in Figure 4 instead of the redundant ICL network shown in Figure 3.

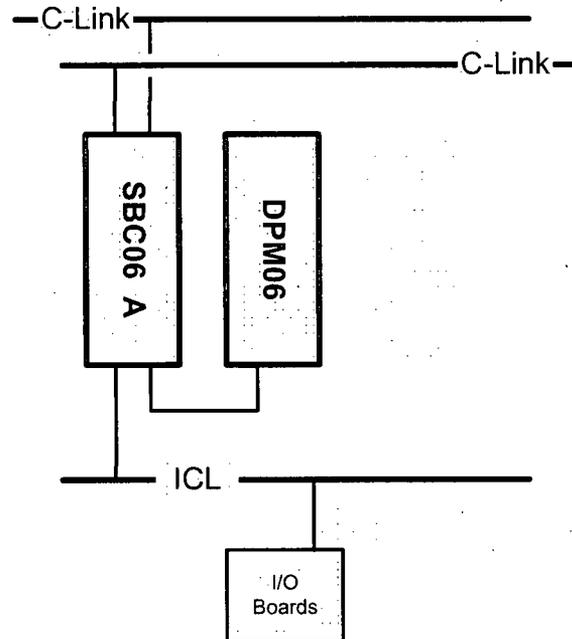


Figure 4. Non-Redundant HFC-SBC06 Board and DPM06 Board

2.3 Execution of Application Programs

The primary function of the HFC-SBC06 System Controller board is to provide control of the plant system actuators based upon the values of system inputs collected from plant field sensors. Control logics, such as arithmetic calculations and logical operations, operate upon field input values to provide control output values that drive plant actuators, operator status displays, and alarm indicators. These control logics are defined in an Application Program, which is installed in the PROM or flash memory in the HFC-SBC06 System Controller. It is transferred to the RAM during power up initialization, and the program is executed during operation of the controller.

Refer to DS001-000-002, Equation Interpreter Component Design Specification, and DS001-000-003, CQ4 Blocks Component Design Specification, for detailed descriptions of control logic algorithms. Refer to UG004-000-01, EWS User's Guide for detailed information about the structure of application program code.

3. Module Architecture

The architecture and design of the HFC-SBC06 board is based upon a partitioning of the module functions between three separate microprocessor sections: the SYS microprocessor section, the ICL microprocessor section, and the CPC microprocessor section. Each microprocessor section is dedicated to a specific set of functional responsibilities, with the SYS processor being the main

processor or system processor for the whole controller and the other two processors being subordinate processors.

The three independent microprocessors uses Public Memory to communicate and coordinate their individual operations. Public Memory is a shared onboard memory (RAM) section that may be accessed by the three microprocessors over a Shared Bus. As shown in Figure 5, the three microprocessors connect to the Public Memory address and data bus (Shared Bus) on the board, with each microprocessor's access to Public Memory controlled by a bus arbitration circuit. Public Memory contains data that is shared by the microprocessors and data that must be transferred between the microprocessors.

In addition to available use of Public Memory, each microprocessor is configured with Private Memory with separate PROM, Flash, and RAM sections. System firmware codes are installed in the PROM or flash memory. Private Memory is accessible only to the microprocessor in that circuit section.

The CPC Section has two RJ45 10BASET ports for the redundant C-Link interface. The ICL Section includes two RS-485 communication links for the ICL.

There is an onboard Sanity circuit for detection of controller failure. The SANE status and PRI (Primary) status signals from the Sanity circuit are routed to the Failover circuit on the HFC-DPM06 board. The Failover circuit supports failover on failure of Primary controller and maintenance failover.

There is a dual-ported memory on the HFC-DPM06 board which is accessible to both the primary and secondary controllers. The three processors connect to the DPM address and data bus, with each processor's access to the DPM controlled by a bus arbitration circuit. Software arrangements coordinate Read and Write to the DPM by the primary and secondary controllers to avoid conflicts or corrupted data.

The System Controller provides Sequence of Events (SOE) master clock with 1 ms resolution over 24 consecutive hours of operation.

Both the HFC-SBC06 and HFC-DPM06 board have DIP switches for controller configuration. These switch settings are accessible to the SYS processor on board.

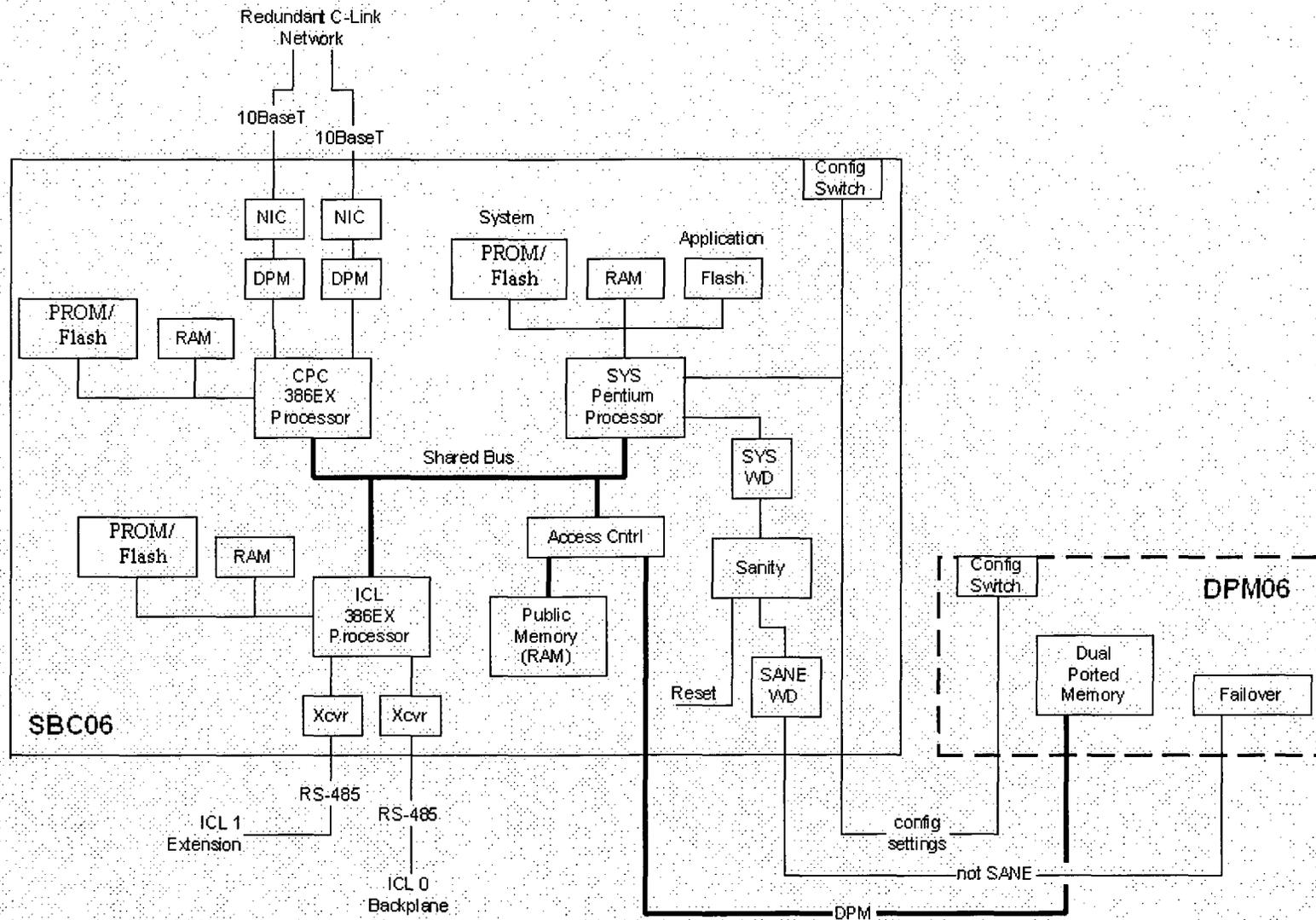


Figure 5. HFC-SBC06 / DPM06 Module Architectures

3.1 Memory Mapping Structure

The individual memory address spaces for the three microprocessors on the HFC-SBC06 board have the same basic structure, with each address space including both Public and Private Memory areas. As shown in Figure 6, the top range of the address space (PROM / Flash) contains executable code. The microprocessor data area (RAM) is mapped to the bottom range of the address space. Public Memory is mapped to the center range of the microprocessor address space.

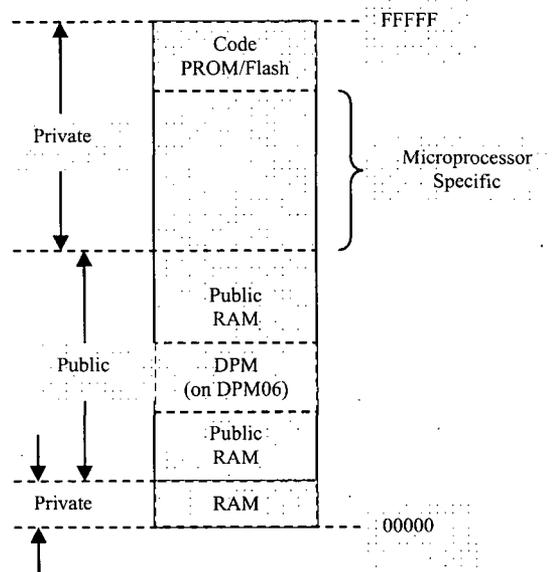


Figure 6. Microprocessor Address Space

The DPM memory area located in Public Memory address space shown in Figure 6 is dual ported memory residing on the DPM06 board installed in the slot next to the HFC-SBC06 board. DPM memory is used by two HFC-SBC06 boards operating as a redundant pair for transferring data between Primary and Secondary.

The Private Memory area shown in Figure 6 labeled **Microprocessor Specific** has different uses within the three processor sections. In the SYS processor section, this area of Private Memory contains the Application Program instructions. In the CPC processor section, this area is mapped to a dual ported memory part that is used to interface the CPC microprocessor to the Ethernet controllers managing low-level communication functions on the C-Link network. In the ICL processor section, this area of Private Memory is not used and contains no RAM, PROM, or Flash memory.

3.2 Public Memory Data

The design of the HFC-SBC06 board uses a Public Memory Data area to allow the three microprocessors to share and transfer data during operation. Public Memory contains a number of data stores used by the microprocessors with the main data stores holding I/O and UCP message data.

The I/O data stores hold data that is accessed and shared by all three microprocessors. As an example of shared data, Public Memory contains three main shared data areas: IO Point Image, Internal Point Image, and DDB Image. These data image areas are used by all three processors on the System Controller board. The data stores shown in Figure 7 are three of the main data items in Public Memory, and these data stores will be encountered a number of times during discussion concerning aspects of the software architectures of the three microprocessor sections on the HFC-SBC06 System Controller board.

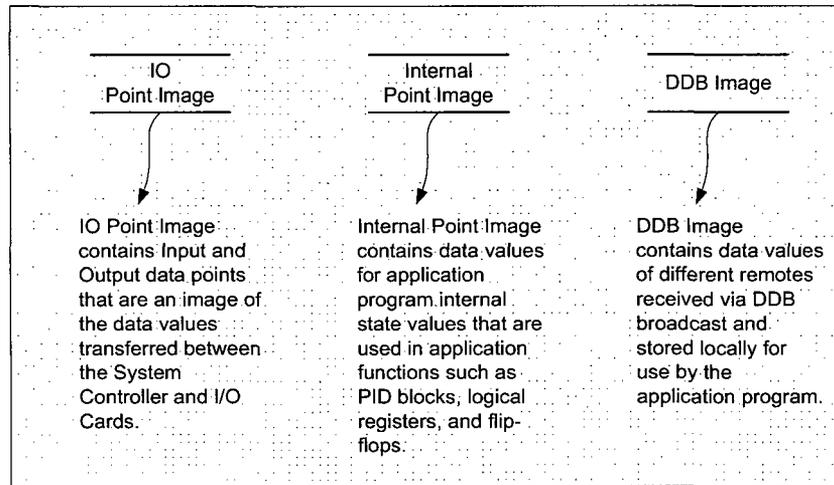


Figure 7. Public Memory Data Stores

The IO Point Image data area holds Input and Output data values that are accessed by:

- the SYS processor during execution of the application program. The SYS processor uses the input data values as the inputs to the application programs and results of execution will be used to update the output data values.
- the ICL processor for storing Input values read from the I/O boards and retrieving Output values that need to be sent to the I/O boards over the ICL serial link;
- the CPC processor for DDB data broadcasts on the C-Link network.

The UCP message data stores hold UCP messages that need to be transferred between the microprocessors. UCP messages are point-to-point communication messages used in HFC control systems. The next section, Section 3.3 provides more descriptions of UCP messages. The UCP messages stored in the Public Memory are mainly operator commands or inquiries from operator workstations and responses from the SBC06 System Controller to the operator workstations. A UCP message is normally processed in the following sequences:

- The CPC processor receives a UCP message from the C-Link and stores it in the Public Memory if the message is not addressed to itself
- The SYS processor retrieves any UCP message addressed to itself from the Public Memory, executes the command and stores the UCP response messages in the Public Memory.
- The ICL processor retrieves any UCP message addressed to itself or ICL I/O boards in the Public Memory, and stores the UCP response message in the Public Memory
- The CPC processor retrieves any UCP response message from the Public Memory and transmits it to the C-Link

3.3 Remote Communication Architecture

Remote communication is used when an HFC-SBC06 System Controller exchanges data with another System Controller, Operator Station, or Engineering Workstation. The HFC-SBC06 supports remote communication over the Communication Link (C-Link) network and provides dual network ports for connection to a redundant C-Link network. Two protocols are used to carry data over the C-Link network. These two protocols are:

- Dynamic Database (DDB) protocol. Refer to DS002-000-001, C-Link Protocol Component Design Specification for detailed descriptions of DDB protocol.
- Universal Communication Packet (UCP) protocol. Refer to DS002-000-003, UCP Protocol Component Design Specification for detailed descriptions of UCP protocol.

The use of one protocol versus the other depends upon whether the data being carried is information that is transferred on a regularly scheduled basis or whether the information is being transferred due to a system event. The DDB protocol is designed to carry data traffic occurring on a regularly scheduled basis, and the UCP protocol is designed to carry a periodic traffic such as operator commands and controller status inquiries.

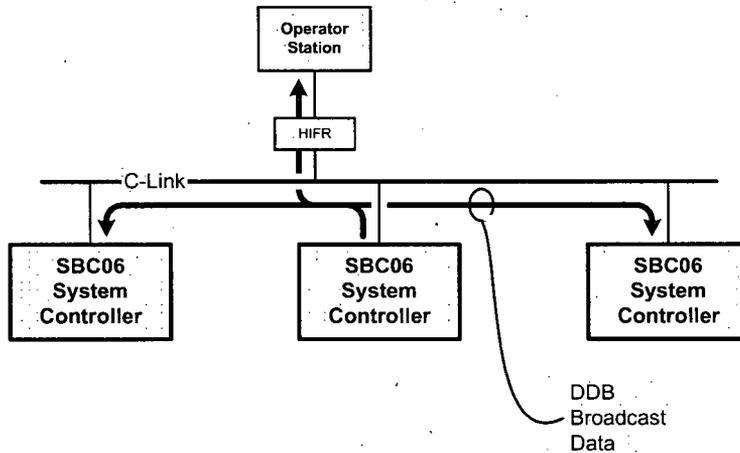


Figure 8. DDB Broadcast Data Paths

The Dynamic Database protocol is a broadcast protocol in which a transmitting node on the C-Link network broadcasts data packets to all nodes on the network. As shown in Figure 8, one network node, the HFC-SBC06 System Controller in center, is broadcasting DDB data while all other nodes are receiving DDB data. The DDB protocol is the method used for transferring system operating data, such as field input values, actuator output values, and control state values, among System Controllers and Operator Workstations. In the HFC-6000 system, DDB data is broadcast from each System Controller in a round-robin sequence.

The Universal Communication Packet protocol is designed as a point-to-point protocol for transferring data that is not sent on a regular basis during system operation.

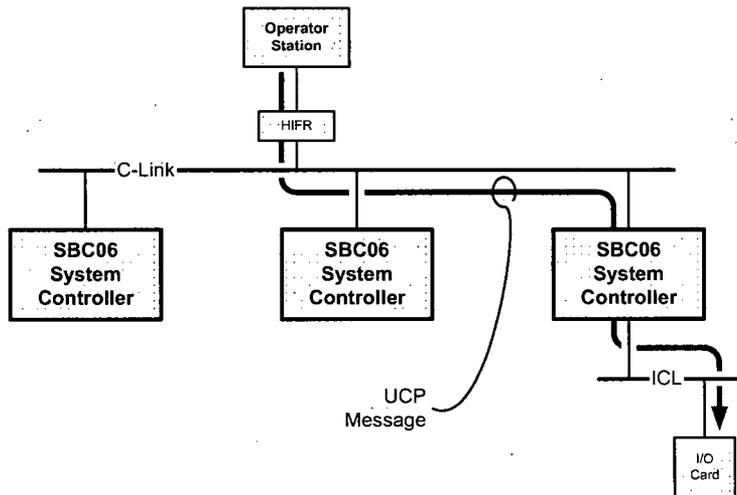


Figure 9. UCP Point-to-Point Message Path

An example of a typical UCP message is an operator query for the status of a device in the plant. As shown in Figure 9, the UCP message originates at the Operator Station and travels to the I/O board connected to the plant device for which the status is being queried.

The complete transaction for this UCP example message actually would consist of two UCP messages. The first message in the transaction would be a UCP request message sent from the Operator Station to the I/O board responsible for the operation of the device. The point-to-point message would be a request for the value control state. The second UCP message in the transaction would also be a UCP response message providing the device control state and going point-to-point from the I/O board to the Operator Station.

Network transmission control for the C-Link network uses a token passing mechanism. In a token passing transmission control scheme, a single node within the network holds the token, and the node with the token is the only one that is allowed to **transmit** data on the C-Link network at a given point in time. While the transmitting node has the token, all other nodes on the network can only receive data. Error detecting functions and mechanisms use network error timers running at each node that are designed to detect token passing errors such as “Lost Token”, “Fail to Pass Token”, “Fail to Claim Token”, and “Token Claim Collision”.

Remote communication for the HFC-SBC06 is handled by the CPC processor. However, data for remote communication may be produced or consumed by any of the three microprocessors on the HFC-SBC06 board. The next two sections describe the CPC processors handling of the data sent and received via remote communication.

3.3.1 HFC-SBC06 Handling of DDB Data

As explained previously, the DDB protocol uses a broadcast of data for transferring information from one node to all other nodes on the network. Each HFC-SBC06 System Controller on the network must be able to both broadcast DDB data and receive DDB data. The specific information that the HFC-SBC06 broadcasts when it has possession of the token is specified in the DDB Broadcast Table. The actual data that is broadcast by the HFC-SBC06 is contained in the IO Point Image and Internal Point Image data stores, as shown in Figure 10. During a DDB broadcast, the CPC processor uses the Broadcast table to determine which data in the two Point Image data stores to select and broadcast on the C-Link.

Not all DDB data broadcast on the C-Link will typically be needed by an HFC-SBC06 for performing its required operations. When the HFC-SBC06 is receiving DDB data from the C-Link, a filter is applied to the data, and only the DDB data specified by the filter is processed CPC processor. As shown in Figure 10, the DDB Filter Table, which lists the DDB data that is needed by the particular HFC-SBC06, is used by the CPC processor to determine which incoming DDB data is to be processed and stored by the CPC processor in the DDB Image data store. DDB data from the C-Link that is **not** listed in the Filter is skipped by the CPC processor.

The I/O Scan Table lists all the configured I/O boards on the ICL for the SBC06 and board information, such as type of I/O points on board, number of points, and assigned point numbers.

The ICL processor uses the I/O Scan Table to determine which I/O board to scan, how to scan it, and where the I/O point values should be stored in the Public Memory.

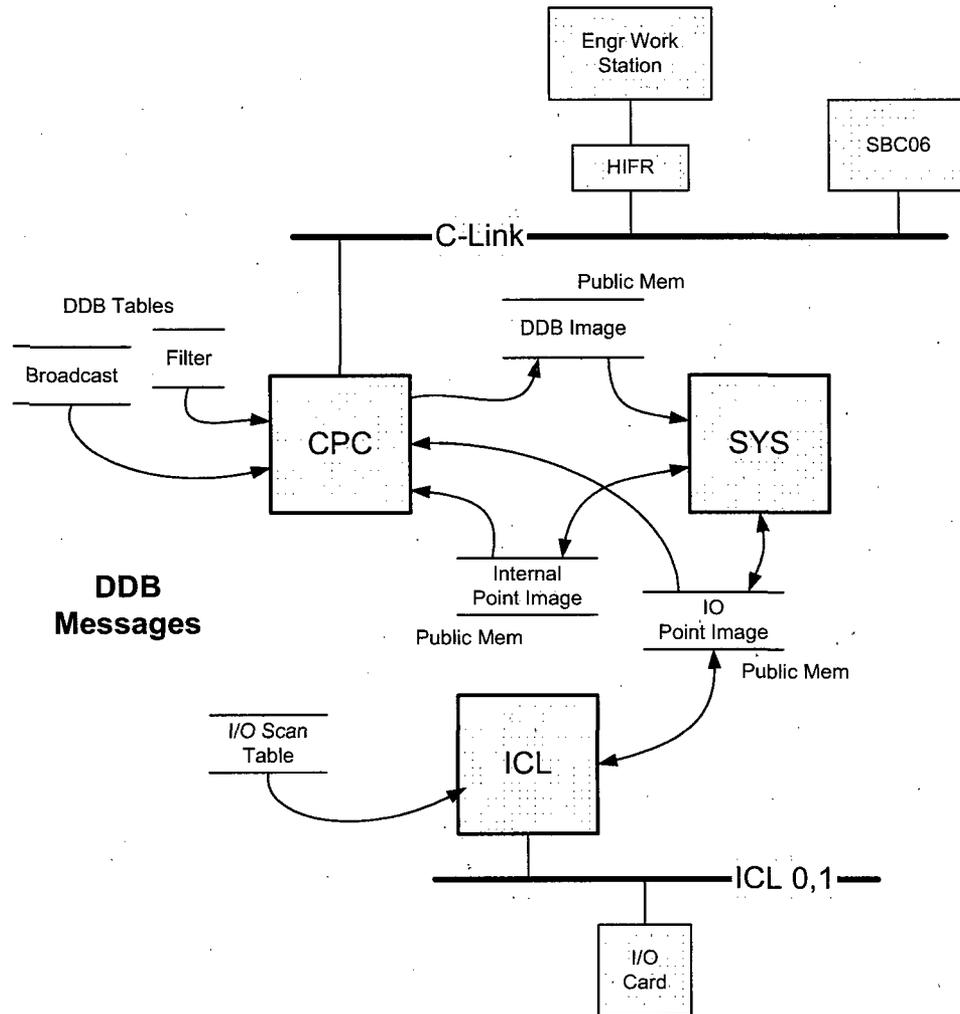


Figure 10. Broadcasting and Filtering of DDB Data

3.3.2 HFC-SBC06 Handling of UCP Messages

UCP messages are designed to be transferred on a point-to-point basis; and as such, any UCP message received by the HFC-SBC06 will either end up being processed by a task running on one of the three HFC-SBC06 processors, or will end up being passed to an I/O board attached to the HFC-SBC06 via the ICL serial network. UCP messages are received from the C-Link network by the CPC processor, which processes the message header to determine where to post the message. If the UCP message is destined for a task running on the CPC processor, the message is stored in a CPC data store for processing by the specific CPC task.

If the UCP message is not addressed to a CPC task, the message will be stored in message data store in Public Memory. As shown in Figure 11, a UCP message addressed to a task running on the SYS processor is stored in the SYS message data store in Public Memory. A UCP message that is addressed to a task running on the ICL processor, or a UCP message addressed to an I/O board, is stored in the ICL message data store in Public Memory.

UCP messages sent from a task running on either the SYS processor or the ICL processor, or a UCP response message received from an I/O board attached to the HFC-SBC06, is stored in respective message data store (SYS messages or ICL messages) in Public Memory.

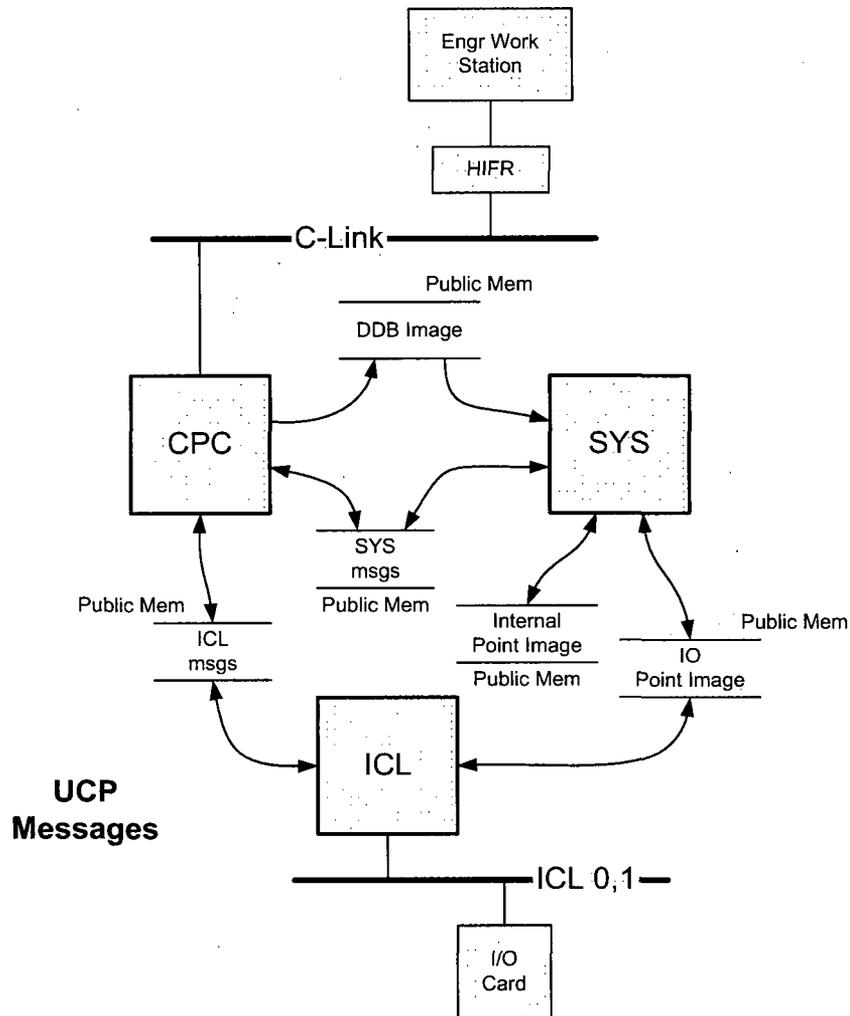


Figure 11. UCP Message Processing

A message event mechanism, with events passed between processors using Public Memory, is used by a processor in the HFC-SBC06 to notify another processor in the HFC-SBC06 that a UCP message has been placed in its respective message data store. Refer to DS001-000-001,

Operating System Component Design Specification for details of the UCP message event mechanism.

3.4 SYS Processor Section

The SYS processor section is based on an Intel Pentium processor. Figure 12 shows the architecture of the SYS Processor section. The major functions of the SYS Processor section are as follows:

- Execution of application programs on I/O point images
- Coordination of the other two processors on board
- Monitoring overall controller status

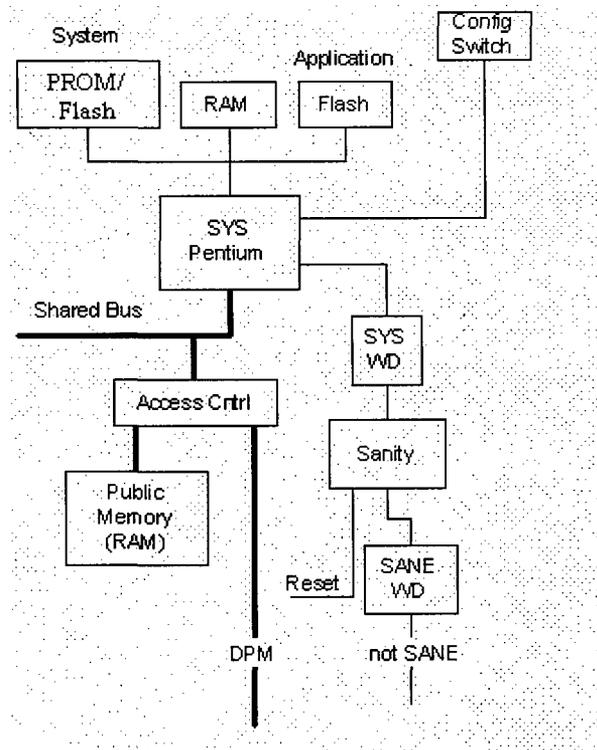


Figure 12. System Processor Architecture

The SYS processor has access to the flash memory that has application programs installed. The application program consists of a sequential set of instructions that are executed by the Equation Interpreter software task. The Equation Interpreter processes the instructions from the

application program to generate digital and analog output values using input values currently in memory. The descriptions of architecture, interface and design of Equation Interpreter component are provided in DS001-000-002, Equation Interpreter Component Design Specification.

The application program in the SYS processor's flash memory also contains DDB Filter Table, DDB Broadcast Table, and I/O Scan Table. During controller initialization, the SYS processor copies these tables from its flash memory to the Public Memory for the use by the CPC Processor and the ICL Processor.

On the HFC-SBC06 board and HFC-DPM06 board, there are DIP switches for controller configuration. The SYS processor reads the switch settings and stores the configuration data in the Public Memory.

As the system processor, the SYS Processor performs initialization for the Public Memory during controller initialization. It configures the Public Memory according to the predefined structure. After the Public Memory Initialization is done, the SYS processor sets a READY flag in the Public Memory to inform the other two subordinate processors that the Public Memory is ready for use.

The other two subordinate processors report to the SYS Processor after they finish initialization successfully and wait for the SYS processor's indication as when to start operating. The SYS Processor, after verifying that all the processors on board have finished initialization, sets a System_Go flag in the public memory, enabling normal operation to begin. The subordinate processors start normal operation after the System_Go flag is set. Thus, the whole controller enters normal operation mode.

Each of the subordinate processor has a "Mailbox" in the Public Memory to report the status of the processor. During normal operation, the subordinate processor periodically updates its mailbox by loading a preset value into it. As a parallel process, the SYS processor monitors subordinate processor running status by decrementing the mailbox at preprogrammed intervals. The setting of mailbox preset value and mailbox decrementing amount and intervals determine how soon a failure of the subordinate processor can be detected.

The SYS processor also maintains the system watchdog timer (a MicroMonitor chip) by strobing the timer periodically. If the SYS processor fails to strobe the watchdog timer, the timer will time out and trigger a failover if the controller is in Primary mode. Refer to details of controller failure detection and failover mechanism in Section 3.7.

The SYS processor maintains a controller status flag in the Public Memory. In case of a status change, the SYS processor updates the controller status flag, so that the two subordinate processors will change their running mode from primary to secondary, or vice versa. This mechanism ensures that the whole controller operates in the same mode: either primary or secondary.

The SYS Processor is also responsible for transferring system status data between the Public Memory and the DPM periodically. If the SYS Processor is in primary mode, it transfers data from the Public Memory to the DPM. If the SYS Processor is in secondary mode, it transfers data from the DPM to the Public Memory. This mechanism keeps the secondary controller updated with system status data and ensures a smooth transition of control in case of a failover from primary controller to secondary controller.

3.4.1 SYS Processor Software Architecture

The SYS Processor software consists of the following routines:

- Initialization
 - Power up/Reset Initialization
 - Controller Configuration
 - Processor Specific Initialization
 - Memory Initialization for Public Memory
 - Task Initialization
- Operating System Component
- Processor Specific Tasks
 - System Tasks
 - DBM Tasks and System Database Manager
 - Equalization Task for DPM
 - Processor Status Monitor Task
 - Equation Applications
 - Equation Interpreter Task
 - Logic Algorithms
 - Analog Processing Algorithms - CQ4 Block Algorithms
 - Timer Interrupt Service Routines
- UCP Utility Component
 - UCP Memory Manager
 - Network Manager for Path Element
 - Network Message Routine
 - UCP Message Handling Tasks

The SYS Processor software is designed based on an operating system common to all processors on the HFC-SBC06 board and a set of configurable tasks that will be run by the operating system. Figure 13 provides an overview of the SYS Processor Software Architecture. The Operating System is mainly a task scheduler, which executes the configured tasks one after another according to a task control block (TCB) list.

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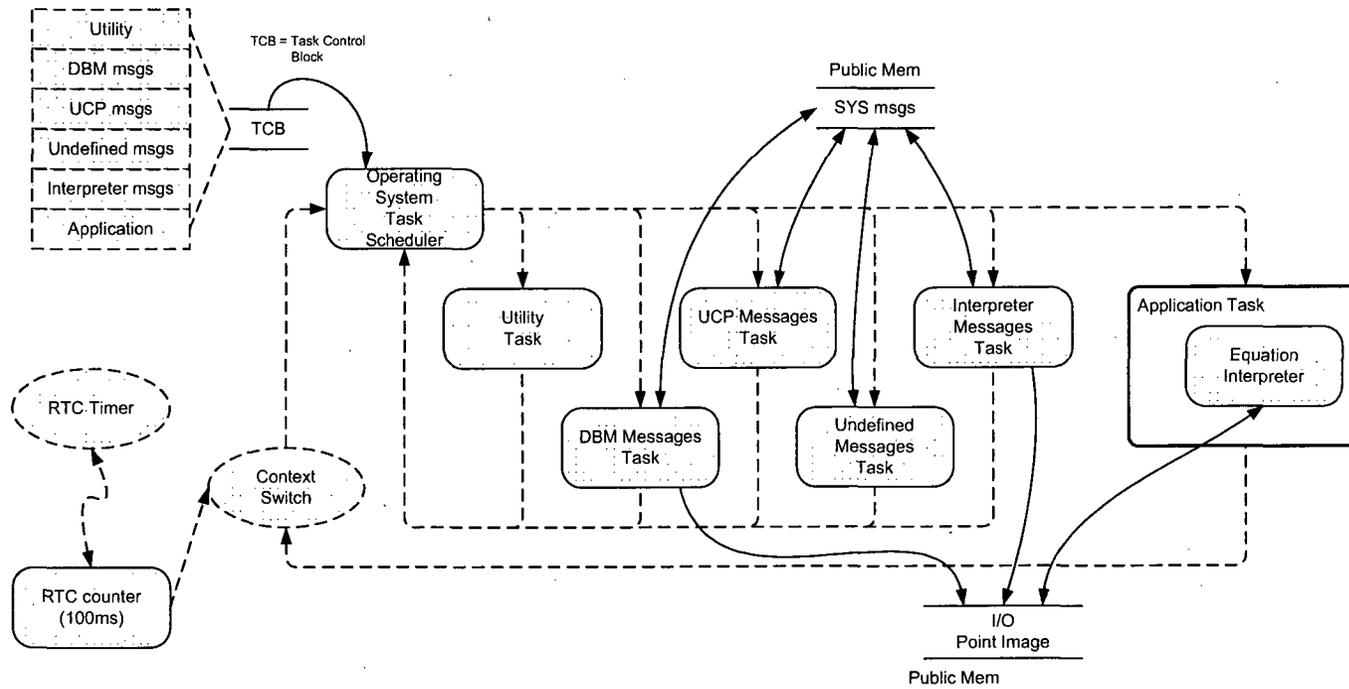


Figure 13. System Software Architecture

The tasks running on the SYS processor are:

- Equation Interpreter Task for running the application program on I/O point images. This is implemented by individual logic subroutines and analog processing algorithms.
 - IOSS_TSK
- UCP Message Handling Tasks which will process the UCP message and call the appropriate routines to provide service to the UCP requests. The services requested include:
 - CQ4INT - CQ4 block update
 - PIDTSK – PID block task,
 - DBMTSK - DBM Task for I/O point images in the Public Memory
 - XEQUAL - Equalization Task for DPM
 - EQMSGTSK - Equation Interpreter service
 - PKTXHG – Packet exchange service
 - UNDEFTSK – handling undefined UCP messages
 - OFFLINETSK – handling UCP messages from EWS workstation intended for offline controllers for updating various controller configuration information. The Equation Interpreter will be stopped so that the application programs will not be executed.
- Operating System tasks:
 - UTILTSK – Performs configured initialization and utility functions
 - UCPTSK - UCP message activity monitoring task
- System processor tasks, such as
 - STATSK - Processor Status Monitor Task
 - IOSTSK - I/O Simulation Task for simulation of the operation of control system like I/O image changes without the presence of real field devices.
 - BLRQ - Build DDB Filter Task, etc.

During initialization, the SYS processor configures several Mailbox utility functions for the OS Utility Task. These mailbox functions are essential to determine the System Controller's Sanity. During every Operating System task scan cycle, these functions will be executed by the Utility Task according to the operation mode of the controller: Primary or Secondary. Refer to Section 3.7.2 for detailed descriptions.

Existing software components will be used to build the SYS Processor software. All of the above tasks, the Operating System and UCP Network Utilities are covered by Component Design Specifications. Refer to Section 5 for the reference document numbers.

The descriptions of Initialization Process are provided in the DS901-000-001, HFC-SBC06 Module Detailed Design Specification.

3.5 ICL Processor Section

The ICL Processor section is based on an Intel 386 processor. Figure 14 shows the architecture of the ICL Processor section. The major function of the ICL Processor section is to handle communication on the ICL to obtain current plant status information from the I/O boards and to send operation commands to the I/O boards.

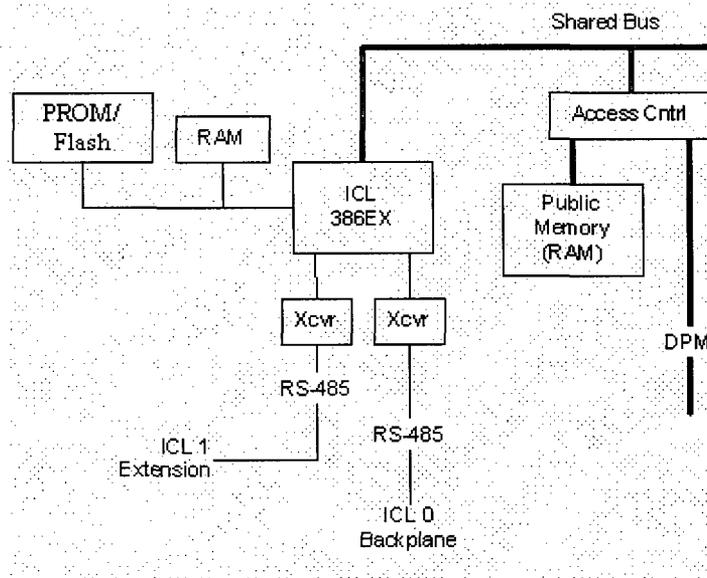


Figure 14. ICL Processor Architecture

The control system interface to field devices in the plant, such as process input sensors and output actuators, is handled by I/O boards mounted in the HFC-6000 board rack. The I/O boards measure signals from field device inputs, convert the measurements to digital images, and control output drive-level signals to plant actuators. The output drive-level signals are the converted values of output images sent to the I/O board from the HFC-SBC06.

The digital images the HFC-SBC06 receives from and sends to the I/O boards are carried by the ICL network that connects the HFC-SBC06 System Controller to its I/O boards. The ICL is structured as an RS-485 network implementing a master/slave communication control protocol. The HFC-SBC06 System Controller board provides the network master function and controls communication on the connected ICL network connected to it. Each I/O board operates as a slave node on the ICL network to which it is attached. The System Controller polls each I/O board, requesting data values for field inputs connected to the I/O board and sending data values for field outputs connected to the I/O board. Only the HFC-SBC06 board will initiate a communication on the ICL with a request message.

The HFC-SBC06 System Controller board has two serial channels: ICL0 and ICL1. ICL0 is on the controller backplane, but it has a connector on the backplane so that it can access boards in expander chassis. ICL1 only goes to expander chassis. Both channels can communicate with

boards in up to two chassis. ICL0 and ICL1 will be connected to different I/O boards but they are logically one ICL. In a redundant configuration, each of the dual serial ports of an I/O board is connected to one of the redundant controllers via an ICL.

The ICL Processor has access to the DPM. This capability is used in a redundant configuration for the secondary ICL Processor to take over the scan task of an I/O board if the primary ICL does not function well with a particular I/O board. If an I/O board does not respond to a regular poll message from the primary ICL Processor, the primary ICL Processor transfers the request message to a dedicated area in the DPM for the secondary ICL Processor to poll that particular I/O board. If the secondary ICL is functional, the secondary ICL processor takes over the scan task for that I/O board and uses the DPM to pass the response data to the primary ICL Processor. Periodically, the secondary ICL Processor performs a loopback test for that I/O board to determine if the primary link is functioning. If the loop test results show that the primary ICL is functioning properly with that I/O board, the primary ICL resumes polling this I/O in its normal sequence.

3.5.1 ICL Software Architecture

The ICL Processor software consists of the following routines:

- Initialization
 - Power up/Reset Initialization
 - Controller Configuration
 - Processor Specific Initialization
 - ICL Communication Initialization
- Operating System Component
- Processor Specific Tasks
 - ICL Scan Task
 - ICL Download Table Routine
 - ICL Scan Routine
 - Primary Mode Routine
 - Build ICL Command
 - Perform Transaction Routine
 - Process Response Routines
 - Secondary Mode Routine
 - Communication Utility Routines
 - Send Message Routine
 - Receive Message Routine
 - ICL Utilities
 - Timer Interrupt Service Routines
- UCP Utilities
 - UCP Memory Manager
 - Network Manager for Path Element
 - Network Message Routine

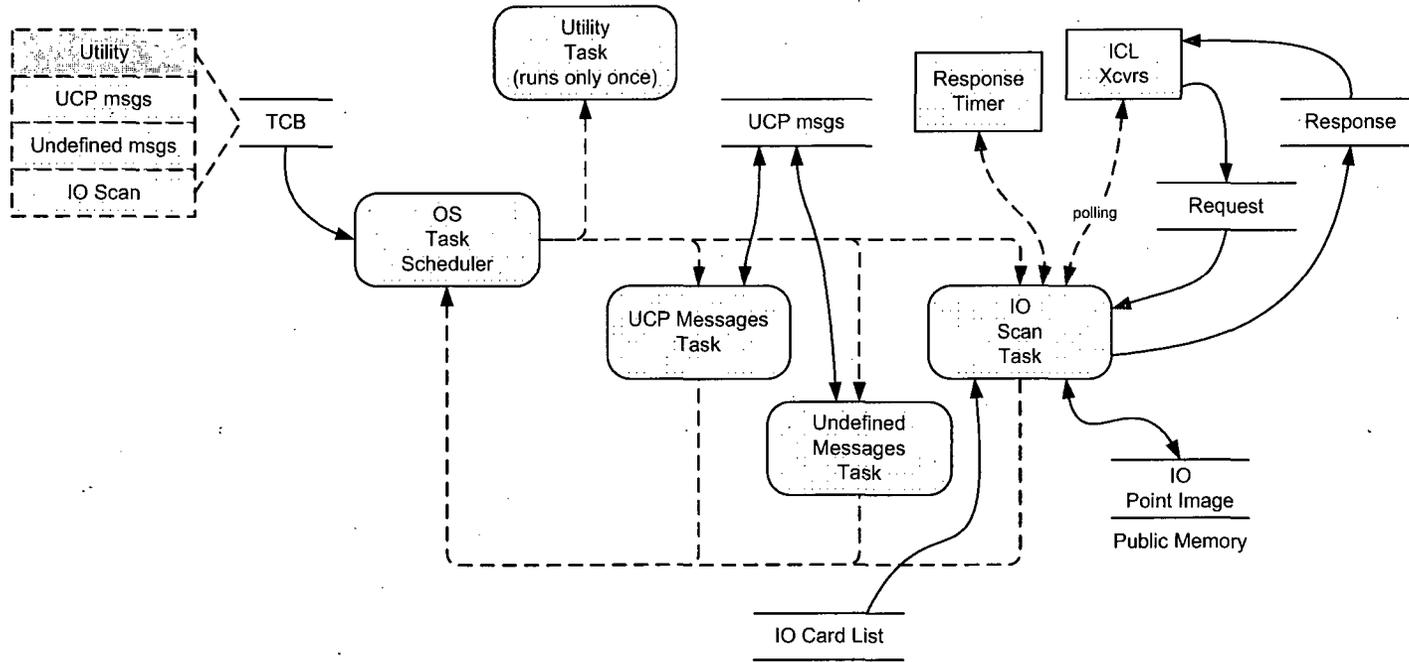


Figure 15. ICL Software Architecture

The ICL Processor software is also designed based on the operating system component common to all processors on the HFC-SBC06 board and a set of configurable tasks that will be run by the operating system. Figure 15 provides an overview of the ICL Processor Software Architecture.

The tasks running on the ICL Processor are:

- ICL I/O Scan Task:
 - IOFSCN
- UCP Message Handling Tasks which will process the UCP message and call the appropriate routines to provide service to the UCP requests. The services requested include:
 - UNDEFTSK – handling undefined UCP messages
 - OFFLINETSK – handling UCP messages intended for offline controllers for updating various controller configuration information
- Operating System tasks:
 - UTILTSK – No utility routines configured
 - UCPTSK - UCP message activity monitoring task

The ICL Processor software does not have any special utility functions configured for the OS Utility Task. So after finishing the initialization part of functions, the OS Utility Task will remove its self from the OS task control block list and will not be executed again.

The existing software components will be used to build the ICL Processor software. All of the above tasks, the Operating System and UCP Network Utilities will be described in Component Design Specifications. Refer to Section 5 for the reference document numbers.

The descriptions of Initialization Process are provided in the DS901-000-001, HFC-SBC06 Module Detailed Design Specification.

3.6 CPC Processor Section

The CPC Processor section is based on an Intel 386 processor. Figure 16 shows the architecture of the CPC Processor section. The CPC Processor section includes hardware for two identical Ethernet channels with twisted pair 10BaseT configuration. The Ethernet interface is implemented with two serial interface network controller chips (NIC). The 10BaseT interface to the C-Link functions in accordance with IEEE 803.2 standards.

The NICs incorporate receiver, transmitter, collision detection, heartbeat, jabber timer, and link integrity test functions. There is one DPM between each NIC and the CPC processor. This DPM provides the memory buffer for the messages received and to be transmitted by the NIC.

The CPC processor controls overall operation of the Ethernet interface to the C-Link, transfer of data to or from the NIC via the DPM, and transfer of data to and from the Public Memory.

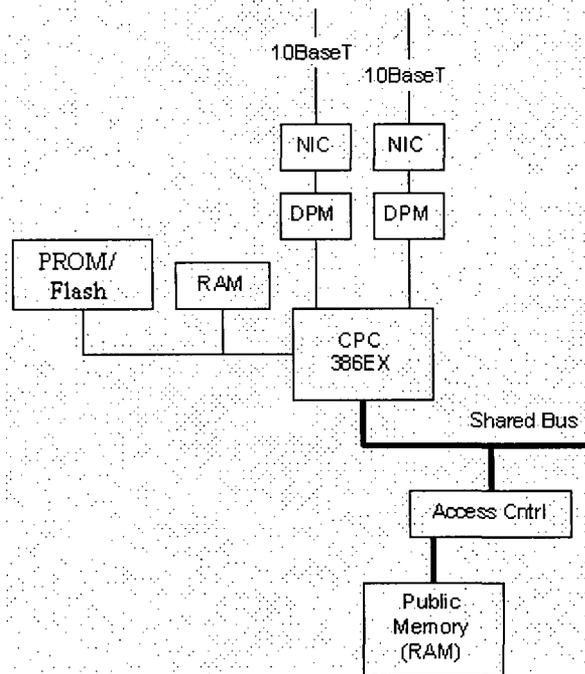


Figure 16. CPC Processor Architecture

3.6.1 CPC Processor Software Architecture

The CPC Processor Software consists of the following routines:

- Initialization
 - Power up/Reset Initialization
 - Controller Configuration
 - Processor Specific Initialization
 - NIC Initialization
 - Tasks Initialization
 - Data Initialization
 - Interrupt Vectors Initialization
- Operating System Component
- Processor Specific Tasks – Communication Tasks
 - Transmit Tasks
 - Interface Transmit Task
 - LLC Transmit Task
 - NIC Transmit Driver

- Receive Tasks
 - Receive ISR
 - LLC Receive Task
 - Interface Receive Task
- Timer Interrupt Service Routines
 - Timer 0 ISR
 - Timer 1 ISR
 - Timer 2 ISR
- DDB Process Routine
 - Get DDB Routine
 - Put DDB Routine
 - Save DDB Routine
- UCP Utilities
 - UCP Memory Manager
 - Network Manager for Path Element
 - Network Message Routine

The CPC Processor software is also designed based on the operating system component common to all processors on the HFC-SBC06 board and a set of configurable tasks that will be run by the operating system. Figure 17 provides an overview of the CPC Processor Software Architecture.

The tasks running on the ICL Processor are:

- C-Link Communication Tasks:
 - LLCRCV – LLC layer receive task
 - LLCTRN – LLC layer transmit task
 - ITFRCV – Interface layer receive task
 - ITFTRN – Interface layer transmit task
- UCP Message Handling Tasks which will process the UCP message and call the appropriate routines to provide service to the UCP requests. The services requested include:
 - UNDEFTSK – handling undefined UCP messages
 - OFFLINETSK – handling UCP messages intended for offline controllers for updating various controller configuration information
- Operating System tasks:
 - UTILTSK – No utility routines configured
 - UCPTSK - UCP message activity monitoring task

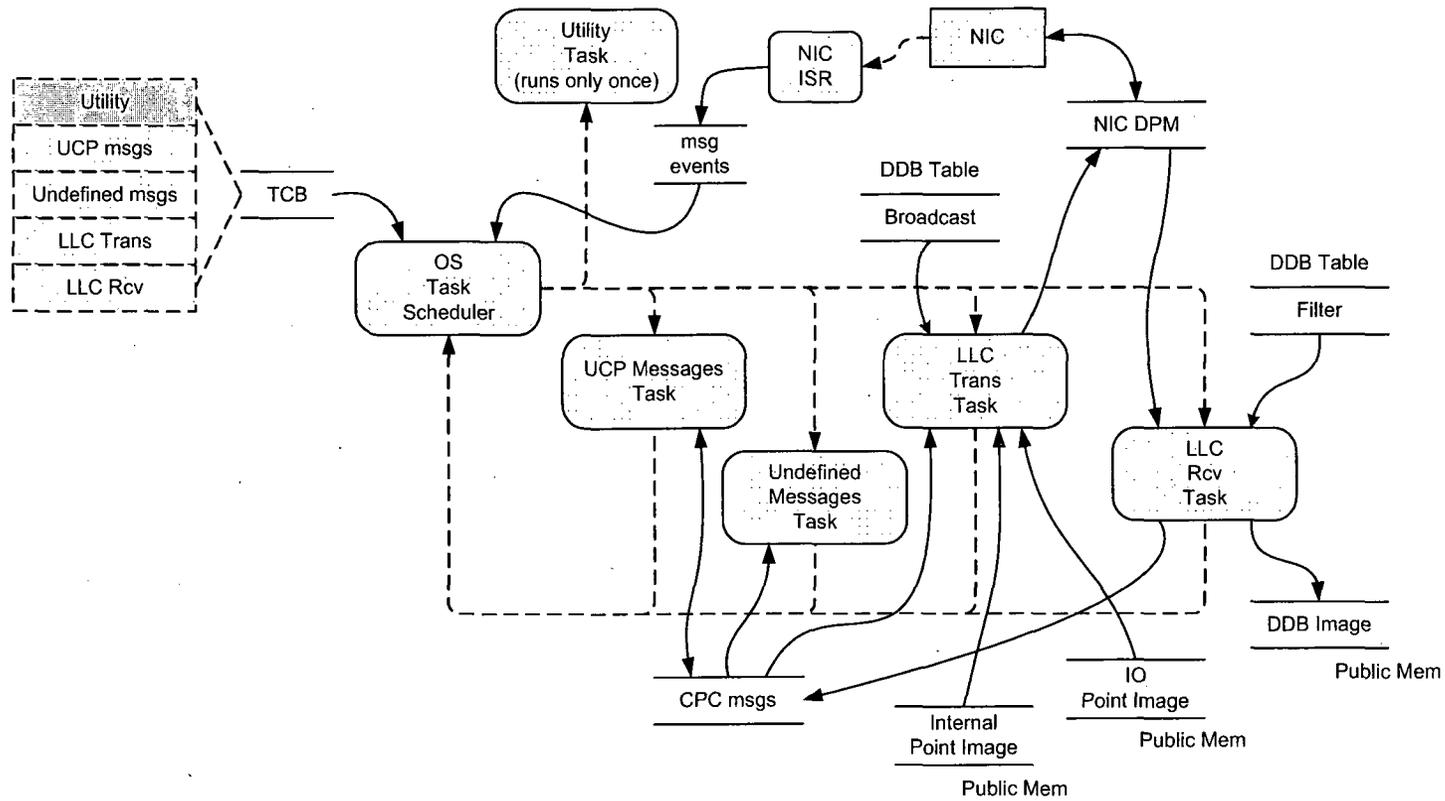


Figure 17. CPC Software Architecture

The CPC Processor software does not have any special utility functions configured for the OS Utility Task. So after finishing the initialization part of functions, the OS Utility Task will remove its self from the OS task control block list and will not be executed again.

The existing software components will be used to build the CPC Processor software. All of the above tasks, the Operating System and UCP Network Utilities will be described in Component Design Specifications. Refer to Section 5 for the reference document numbers.

The descriptions of Initialization Process are provided in the DS901-000-001, HFC-SBC06 Module Detailed Design Specification.

3.7 HFC-SBC06 and HFC-DPM06 Redundancy Architecture

Refer to Section 2.2 for descriptions of Redundant System Controllers. Two HFC-SBC06 boards and a HFC-DPM06 board in the redundant configuration are installed in the three leftmost slots of the HFC-6000 controller rack, with the DPM06 board installed between the two HFC-SBC06 boards. The three boards include hardware and software designed to support redundant controller operation. The main functions of the redundant architecture are as follows:

- Logic to determine controller operation mode: Primary or Secondary
- Failover mechanism on failure of primary controller
- Manual maintenance failover
- Controller failure detection mechanism
- Mechanism to ensure a smooth transition of control during failover

Figure 18 shows the redundancy architecture. Each of the HFC-SBC06 System Controller has a Sanity circuit consisting of mainly a CPLD. This circuit provides a SANE signal and a PRI (primary) signal to indicate the sanity and primary status of the system controller board. These signals are routed to the backplane as inputs to the failover circuit on the HFC-DPM06 board. This failover circuit is implemented mainly by a CPLD, a maintenance failover push button and board edge LEDs.

The Sanity circuit determines the sanity of the controller by the action that the SYS Processor strobes the watchdog timer before it times out. The SYS processor periodically initiates a strobe to the watchdog timer to keep the Sane signal in its active state. If the PRI signal from the other controller is false, the Sanity circuit will produce a true PRI signal. The failover circuit on the DPM06 board activates corresponding output signals to board edge LEDs to indicate that status. However, the Sanity circuit will not make the PRI signal true if the PRI signal from the other controller is already true, which means that the other controller is running in primary mode. This condition causes the controller to operate in secondary mode.

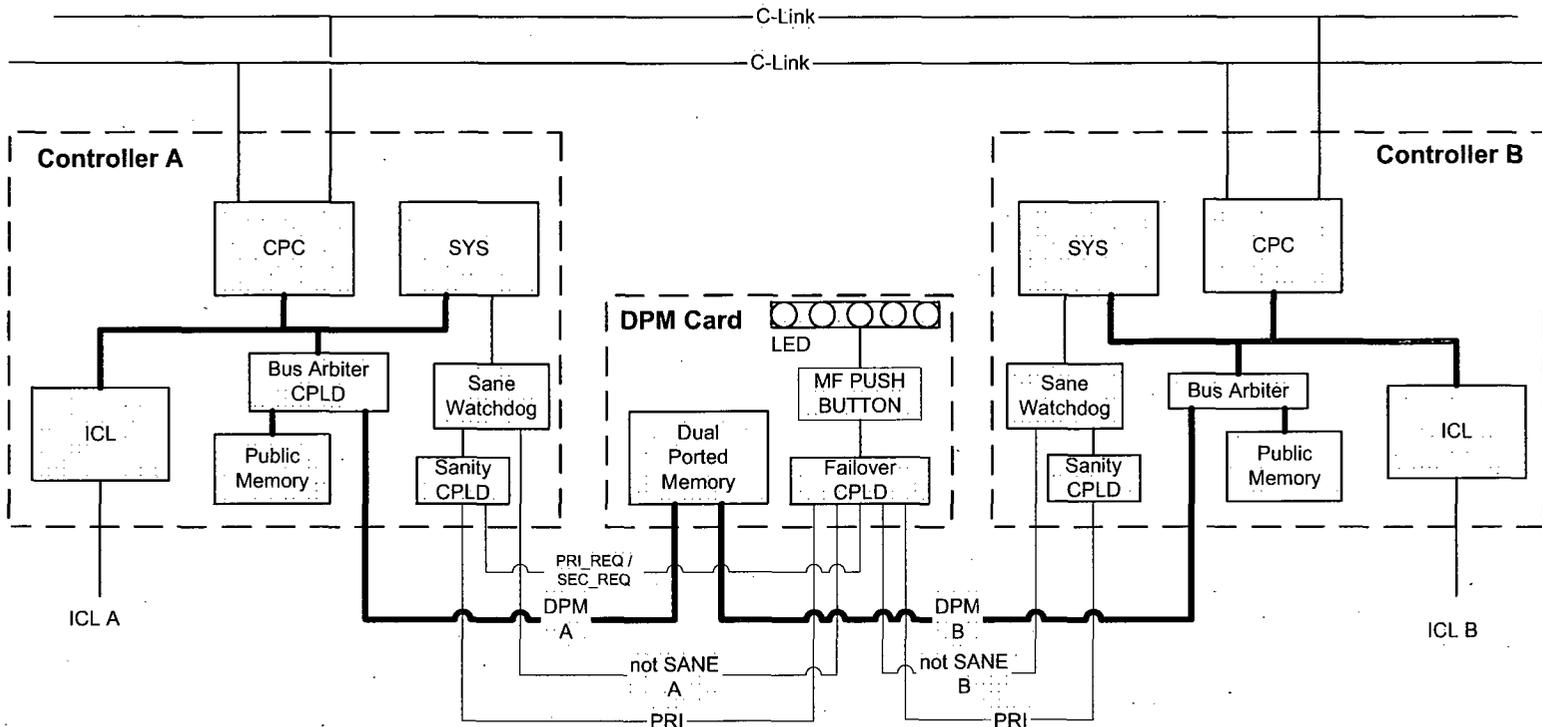


Figure 18. HFC-SBC06 Redundancy and Failover

During the start up of redundant controllers, the SANE signals in both controllers are inactive, and so are the PRI signals. The controller that finishes initialization first sends a strobe to its watchdog timer first. The Sanity circuit sets both the SANE and PRI signals true. The SYS Processor software of this controller reads the PRI signal to determine its operation mode, sets a remote operation status flag to Primary in the Public Memory, and starts operating in Primary mode. The other two subordinate processors of this controller read the operation mode flag in the Public Memory and start operating in Primary mode too. On a parallel process, the other controller finishes initialization, strobes its watchdog timer and becomes sane, but its Sanity circuit can not set the PRI signal to true, because the PRI signal from this controller is already true. So every processor on the other controller will operate in Secondary mode.

The SYS Processor software strobes the Watchdog Timer periodically, so that the SANE signal from the Sanity circuit will remain true. If the software fails to strobe the Watchdog Timer, the watchdog timer will time out. The SANE status signal will then be disabled. The change in SANE signal from true to false will cause the PRI signal to become false. If the controller is currently in secondary mode, the maintenance failover function will be disabled to prevent manual activation of failover while the secondary controller is not functioning properly. If the controller is currently in primary mode, a failover will be triggered. The current primary controller will become secondary, and the current secondary controller will become primary. During the failover process, the SYS Processor detects the need for an operation mode change first by comparing the hardware PRI signal with its current remote operation status. It changes its remote operation status flag in the Public Memory and sets the Synchronization flag to Not_In_Sync. The Operating System on each processor detects that a synchronization of operation status is needed for all tasks running on that processor. After each processor is synchronized, the Operating System on the SYS Processor will clear the Synchronization flag.

As long as both controllers are operating normally (SANE and all applications data validated), the failover circuit on the DPM06 board activates an output to the LED DS1. This display indicates that the maintenance failover function is available. If the user presses the maintenance failover button on the DPM06 board, the failover circuit activates a SEC_REQ signal for controller A if it is currently the Primary controller, or a PRI_REQ signal if it is currently the Secondary controller. This signal causes controller A to initiate failover to controller B by setting its PRI status from Primary to Secondary (with SEC_REQ signal) or from Secondary to Primary (with PRI_REQ signal). Assuming that controller A is the current primary controller, the change of its PRI status will cause the current secondary controller to change its PRI from Secondary to Primary. However, if one of the two controllers loses SANE status, the DS1 LED goes out, and the maintenance failover function is disabled.

Additional information of the Failover Mechanism and DPM Transfer is provided in DS001-000-08, Failover Mechanism Component Design Specification.

3.8 HFC-SBC06 CPLD Design

The HFC-SBC06 utilizes four Xilinx CPLDs and the HFC-DPM06 utilizes one Xilinx CPLD to implement most of the required miscellaneous “hardwired” digital logic functions. These CPLDs, when programmed, function as though they were a matrix of individual logic gates. The algorithms contained within these devices are defined in VHDL source codes.

- **PBUSIF** - This CPLD provides logic necessary to interface the SYS processor’s local bus with the other components on board, such as flash memory access, .
- **SBC6_CHSEL** – This CPLD provides the logic necessary to perform such functions as chip selects, interrupt controller,, I/O ports, timer and processor reset for the SYS processor.
- **SBC6_386C** – This CPLD provides the chip selects, memory read, and memory write control both of the 386EX processors, i.e. CPC processor and ICL processor. It also provides reset logic and public memory access control for these two processors.
- **SBC6_SHARB** – This CPLD defines the address range of the public memory and the DPM as well as providing the SOE (sequence of events) timer.

Details of the data lines defined by these CPLDs are provides in the DS901-000-01, HFC-SBC06 Module Detailed Design Specification.

3.9 Sequence of Events Timer

The HFC-SBC06 system controller maintains a Sequence of Events (SOE) timer over 24 consecutive hours of operations. The SOE timer is used for “time tagging” events that occur system wide. This timer can be synchronized by some master SOE timer located elsewhere in the system, or can be the master timer itself. The SOE timer provides a resolution of 100 μ S for synchronizing similar SOE timers on each I/O boards.

The timer is implemented by a timer with 100 μ S resolution contained in the SBC6_SHARB CPLD. The SOE timer is a 45-bit counter capable of counting 100 μ S intervals for over 100 years. By convention, software algorithms assume some base date and time, such as midnight, Jan. 1, 1980, which corresponds to a counter value of zero. This initial date and time, expressed in seconds, is called the base time. The counter value corresponding to the current time can then be calculated by multiplying the number of seconds that have elapsed since the base by 10,000. Proceeding in this manner, the SOE timer can be loaded with the current time value at initialization.

When the system controller is configured for SOE logging, the SYS processor communicates with configured buffers within the CPLD to transfer commands, the timer preset value, and to read the current timer count. The SYS processor can transfer data to the buffers or read the current count value without disrupting operation of the counter.

3.10 HFC-DPM06 Board

The HFC-DPM06 board provides three onboard DIP switches for the configuration settings of the HFC-SBC06 System Controller board. It also provides a dual ported memory, a failover circuit, LEDs, four bus driver chips, and a maintenance failover push button for redundant controller configuration.

There is a CPLD on the HFC-DPM06 board. This CPLD supports arbitration and bus control functions and maintenance failover. It receives a set of status and control signals from both the redundant System Controller boards. The resulting outputs from the CPLD control operation of the four onboard bus drivers and status displays on the board edge LEDs. The same CPLD also provides logic to support the failover mechanism for redundant system controller configuration.

4. Configuration Setup and LED Displays

The HFC-SBC06 board contains one 8-position DIP switch, two toggle switches and nine jumpers. The switches and jumpers enable manual control of reset, hardware configuration, and programming of the board. Additional configuration switches are physically located on the HFC-DPM06 common board.

4.1 HFC-SBC06 Onboard Switch Functions

SW1 Power on/off, RESET

SW2 Positioned down (toward the board) permits write cycles to onboard flash memory chips. The switch is placed in this position to program flash memory for the ICL and CPC processors and to download the application program to the flash memory of the SYS processor.

Positioned away from the board enables a write-protect function for flash memory. For safety-related applications, the switch should remain in this position for normal operation.

SW4 8-position DIP switch defines operating modes and control parameters as indicated in Table 1.

Table 1. SYS Processor Configuration Switches

Switch	Function
SW4-1	[]
SW4-2	[]
	[]
	[]
SW4-3	[]
SW4-4	[]
SW4-5	[]
SW4-6	[]
SW4-7	[]
SW4-8	[]

4.2 HFC-DPM06 Onboard Switch Functions

Three eight-position DIP switches on the DPM common board control values for the following parameters: [

]

[

]

4.3 HFC-SBC06 Onboard Jumper Options

Table 2 defines the function of each jumper included on the HFC-SBC06 controller.

Table 2. Jumper Options

Jumper	Function
J1	[]
J8	[]
W2	[]
W3	[]
W5	[]
W6	[]
J5	[]
E1, E2	[]

4.4 LEDs

The HFC-SBC06 board contains eight board-edge LEDs, which provide a visual indication of functional status of the controller hardware and software. The HFC-DPM06 board contains five board-edge LEDs, which provide a visual indication of functional status of the controller.

4.4.1 HFC-SBC06 LED Functions

DS1 Includes four LEDs to indicate hardware status of the Ethernet interface as follows:

- DS1-1 flashes on for approximately 50 ms when C-Link channel 1 transmits in TPI mode.
- DS1-2 flashes on for approximately 50 ms when receive data is detected for C-Link channel 1 in TPI mode.
- DS1-3 flashes on for approximately 50 ms when C-Link channel 0 transmits in TPI mode.
- DS1-4 flashes on for approximately 50 ms when receive data is detected for C-Link channel 0 in TPI mode.

DS2 Includes four LEDs . Two LEDs are controlled directly by the P1.6 and P1.7 ports of the ICL microprocessor, and two are controlled by the corresponding ports of the CPC microprocessor.

DS3 and DS4 Includes 8 LEDs controlled by the SYS Processor. Refer to Section 4.4.1.1.

4.4.1.1 DS3 and DS4 LEDs

If the SYS processor detects a failure condition during system initialization/reset, the display freezes with the LEDs displaying a binary code for that fault. Table 3 lists the defined error codes and the error conditions that they represent. Throughout normal operation, the LED display represents a binary code for different processor tasks, and the LED code for a particular task lights while it is running. As a result, all 16 LEDs flicker constantly during this phase of operation. The bottom LED is always on when the board is running normally. Table 4 lists the defined task LED code. If the board detects a failure condition during normal operation, the display freezes with the LEDs displaying a binary code for that fault. Table 5 lists the defined error codes and the error conditions they represent.

Table 3. DS3 and DS4 LED Indications for Initialization Failure

Code	Error Condition
01 _H	[]
02 _H	[]
03 _H	[]
04 _H	[]
05 _H	[]
06 _H	[]
07 _H	[]
08 _H	[]
09 _H	[]
0A _H	[]
0B _H	[]
0C _H	[]
0D _H	[]
0E _H	[]
0F _H	[]
10 _H	[]
11 _H	[]
12 _H	[]
13 _H	[]
14 _H	[]
15 _H	[]
16 _H	[]
17 _H	[]
18 _H	[]
19 _H	[]
1A _H	[]

Table 4. DS3 and DS4 LED Indications for Individual Tasks

Bit	Hex	Task
0	1 _H	[]
2	4 _H	[]
3	8 _H	[]
5	20 _H	[]
6	40 _H	[]
7	80 _H	[]
9	200 _H	[]
10	400 _H	[]
11	800 _H	[]
15	8000 _H	[]
Other	Other	[]

Table 5. DS3 and DS4 LED Failure Indications During Normal Operation

Code	Error Condition
01 _H	[]
02 _H	[]
03 _H	[]
04 _H - 10 _H	[]
11 _H	[]
12 _H	[]
13 _H	[]
14 _H	[]
15 _H	[]
Note: All processor failure codes are defined, but they are functional only if that processor is configured for the control system.	

4.4.2 HFC-DPM06 LED Functions

DS1 Lights when the maintenance failover function is available (controller A and controller B both sane).

DS2 Lights when controller A is primary.

DS3 Lights when controller A is sane.

DS4 Lights when controller B is primary.

DS5 Lights when controller B is sane.

4.5 Installation of System Software and Application Programs

Each of the three onboard processors has a dedicated flash memory and a dedicated PROM for system software. SYS processor also has a dedicated flash memory for its application program code. Switch and jumper selections on the board cause the processor to boot from either the PROM or the flash memory.

At the present time, the system software normally is burned into a separate PROM for each processor, and then each PROM is installed in the PROM sockets associated with the appropriate private memory array. The code is then copied from PROM to flash memory during the initialization sequence. During system development, the application code can either be downloaded to flash or installed in PROM for transfer to flash. Once system development and tuning has been completed, the download function should be disabled to prevent inadvertent alteration of the application code. Throughout the normal operating life of a system, all application code should be transferred to flash from PROM to ensure proper configuration management.

4.5.1 System Code Transfer to Flash

Initially, the flash memory chips are blank. The following steps describe the procedural sequence required to transfer system software code to each of the onboard flash memory chips.

1. Install jumper J1 to enable the SYS processor to boot from its system code PROM.
2. Install the PROM containing system software for the SYS processor in socket U52.
3. Set DIP switch SW4-8 in the ON (toward the board) position.
4. Install jumper J8 to enable the ICL and CPC processors to boot from their system code PROMs.
5. Install the PROM containing the system software for the ICL processor in socket U7.
6. Install the PROM containing the system software for the CPC processor in socket U8.

CAUTION

Make sure that S1 is positioned toward the board before installing it in the board rack. If SW1 is positioned away from the board and power is applied to the rack, power transients could damage components on the board.

7. Mount the board in a controller slot of the HFC-6000 controller board rack.

8. Ensure that power is applied to the board rack, and position S2 toward the board to enable write cycles to flash memory.
9. Ensure that power is applied to the board rack, and position SW1 away from the board.
10. Following application of operating power, the system software will be transferred from U52 to the flash memory for the SYS processor. Successful transfer will be indicated by the following:
 - LED01 lights for several seconds and then goes out.
 - LED00 through LED07 light in sequence.
11. The system software for the ICL and CPC processors should be transferred to flash memory.

NOTE

As long as J1 remains installed, the SYS processor will boot from the PROM installed in socket U52. That code will be compared with the code currently in flash memory; and if it is different, the contents of PROM will be transferred to flash memory and the processor will operate from that code. If J1 is removed, the SYS processor will boot from the flash memory without examining the contents of its PROM.

As long as J8 remains installed, the ICL and CPC processors will boot from their respective PROMs. If SW2 is positioned as write enable, the contents of the PROMs will also be transferred to the flash memories for the two processors.

12. After the installation of the system software to flash, do the following:
 - Remove jumper J1.
 - Set DIP switch SW4-8 OFF (away from the board).
 - Leave jumper J8 installed (for current software design).

4.5.2 Application Code Download

The application program codes can be compiled by an EWS workstation software and downloaded to the controller over the C-Link. This download can be repeated following any modification or update to the application code during application development; however, the download function should be disabled during normal operation to prevent inadvertent changes to the application.

1. Set S1 toward the board to remove power from the board.

2. DIP SW4 can be set to place the software in offline mode (SW4-1 ON and SW4-2 OFF). While operating in this mode, the system software runs normally, but the equation interpreter task does not run.
3. Set S2 toward the board to enable flash write cycles.
4. For redundant controllers, set SW4-5 ON.
5. For redundant controllers, repeat steps *1* through *4* for the second controller.
6. Set S1 away from the board to enable distribution of operating power on the board (both controllers for redundant configurations).
7. At the EWS workstation, compile the final application code for the controller.
8. Download the equations, RQ file, and CQ4 blocks, as applicable.
9. For redundant controllers, initiate failover to the secondary controller.
10. Download the equations, RQ file, and CQ4 blocks as applicable.
11. Set S2 away from the board to disable flash memory write cycles.
12. If the controller was placed in offline mode, power down the controller and set both SW4-1 and SW4-2 OFF to enable normal operation. Power the controller up to enable controller operation to begin.

4.5.3 System Software Updates

If an upgrade is provided for the system software of one or more processors on the controller board following installation, repeat the procedure described in paragraph 4.5.1. Direct download of system programs code to flash memory is not presently supported.

4.6 Hardware Configuration

Refer to Tables 1 and 2 for a general definition of functions controlled by the onboard switches and jumpers. The following steps identify typical switch and jumper settings required for normal operation. Record the specific DIP switch settings required for each controller to be used in the system.

CAUTION

Make sure that S1 is positioned toward the board before removing or installing the board in the board rack. If SW1 is positioned away from the board and power is applied to the rack, power transients could result in damage to components on the board.

1. Set SW4-1 and SW4-2 on the HFC-SBC06 board both in the open position. This configuration enables normal run mode for the system software.
2. If the controller is used as part of a redundant pair, set SW4-5 closed. This enables regular transfers of status from the primary to the secondary via the HFC-DPM06 array.
3. Set SW4-6 closed. This enables the sanity function.
4. Set SW4-7 and SW4-8 both open. This disables software downloads from the EWS workstation.
5. Set DIP switches on the HFC-DPM06 board to provide the following configuration parameters:
 - Set SW2 to the binary value for the remote number assigned to this controller. The valid range is from 0 to 255.
 - Set SW4 to the binary value for the total number of remotes configured for this system (up to 255).
 - Set SW1 to the binary value for the sequence number of this remote on the C-Link. The valid range is from 0 to 31.

CAUTION

The remotes must be configured on the C-Link in numeric sequence with the HIFR assigned the sequence number of 0. If any remote is installed out of sequence, reliable communication with that remote over the C-Link could be disrupted.

6. When the HFC-SBC06 board is used as a redundant controller, a jumper should be installed from node J5-1 to J5-2. This hardware interlock requires the controller chassis to complete its power up initialization sequence successfully (SANE status TRUE) and become the primary controller before the ICL processor can begin transmitting over its serial link. Removing all jumpers results in a configuration in which the transmit interface remains enabled as long as logic power is present.

5. Module Design Constraints

The following is a list of specifications that constraint the design of an HFC-SBC06 board module.

5.1 Communication Interface Specifications

- Document DS002-000-01, C-Link Protocol Component Specification
- Document DS002-000-02, ICL Protocol Component Specification
- Document DS002-000-03, UCP Protocol Component Specification

5.2 Operating System Specification

- Document DS001-000-01, Operating System Component Design Specification
- Document DS001-000-02, Equation Interpreter Component Design specification
- Document DS001-000-03, CQ4 Component Design Specification
- Document DS001-000-06, System Component Design Specification
- Document DS001-000-07, Job Component Design Specification
- Document DS001-000-08, Failover Mechanism Component Design Specification

5.3 Hardware Interface Specifications

- Document 40040901, HFC-BPC01-19 Backplane Specification
- Document 40041401, HFC-BPE01-19 Backplane Specification
- Document DS901-000-34, HFC-BPC01-23 Backplane Specification
- Document DS-901-000-35, HFC-BPE0-23 Backplane Specification
- Document DS-901-000-36, HFC-BPC02-23 Backplane Specification
- Document DS-901-000-37, HFC-BPC02A-23 Backplane Specification
- Document DS901-000-38, HFC-BPC03-23 Backplane Specification

5.1 Design Safety

5.4.1 Main Processor – SC Code

[
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5.4.1.1 Criticality

[

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5.4.1.2 Hazard

[

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5.4.1.3 Security

[

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5.4.1.4 Risk

[

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5.4.2 ICL Processor – SAP Code

5.4.2.1 Criticality

[

]

5.4.2.2 Hazard

[

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5.4.2.3 Security

[

]

5.4.2.4 Risk

[

]

5.4.3 C-Link Processor – SEP Code

5.4.3.5 Criticality

[

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5.4.3.6 Hazard

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5.4.3.7 Security

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5.4.3.8 Risk

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HF Controls Corporation

HFC-6000 Product Line

I/O Module Design Specification

MS901-000-02

Rev C

Effective Date 1/29/2009

Author Gregory Rochford

Reviewer Pat Thibodeau

Approval David Briner



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Table of Contents

1. INTRODUCTION..... 4

2. FUNCTIONAL DESCRIPTION..... 5

3. MODULE ARCHITECTURE..... 6

 3.1 I/O BOARD ARCHITECTURE 6

 3.2 ADDRESS SPACE ARCHITECTURE 9

 3.3 SOFTWARE ARCHITECTURE 10

 3.3.1 X86 SOFTWARE ARCHITECTURE..... 11

 3.3.2 DSP ASSEMBLY SOFTWARE ARCHITECTURE 13

 3.3.3 FAULT DETECTION AND PROCESSING 16

 3.4 ONBOARD SWITCHES, JUMPERS, AND LEADS 16

4. MODULE DESIGN CONSTRAINTS 17

 4.1 COMMUNICATION INTERFACE SPECIFICATIONS 17

 4.2 DETAILED DESIGN SPECIFICATIONS 17

5. DESIGN SAFETY 17

 5.1 COMMON MODULES..... 17

 5.1.1 SECURITY..... 18

 5.1.2 RISK..... 18

 5.2 OUTPUT MODULES..... 19

 5.2.1 CRITICALITY 19

 5.2.2 HAZARD..... 19

 5.2.3 RISK..... 20

5.3	INPUT MODULES	21
5.3.1	CRITICALITY	21
5.3.2	HAZARD.....	21
5.3.3	RISK.....	22
Figure 1.	HFC-6000 System Hierarchy	4
Figure 2.	HFC I/O Board Module Architecture.....	7
Figure 3.	ICL Communication Architecture.....	9
Figure 4.	I/O Board Software Architecture.....	11
Table 1.	List of HFC-6000 I/O Boards	6

1. Introduction

The HFC-6000 distributed control system provides plant monitoring and control capabilities with monitoring and control responsibilities spread over multiple remote control units. The I/O boards are sensors and drivers for implementing plant control functions. They provide signal-level interfaces to the equipment and devices in the plant. As shown in Figure 1, an HFC-6000 I/O board is positioned in the HFC-6000 system hierarchy between the HFC-SBC06 System Controller(s), which is the CPU of HFC-6000 system, and the equipments and devices in the plant.

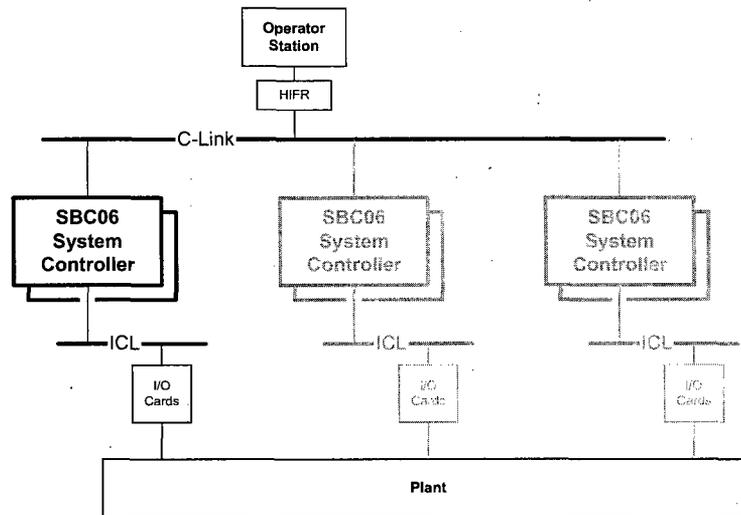


Figure 1. HFC-6000 System Hierarchy

Descriptions and discussions of the functional requirements of the HFC-6000 I/O boards are provided in 700901-06, *HFC-6000 Product Line General I/O Card Requirements Specification*.

Subsequent sections of this document provide top-level architectural and design descriptions of HFC-6000 I/O boards. Two different designs are currently in use. In general, the digital I/O boards employ a common processor kernel based on an Intel microprocessor. The assemblies with AI channels use a Digital Signal Processor (DSP) to control the main processing functions. Both designs provide a common architecture that is used on multiple assemblies. Lower level descriptions of each I/O board are contained in a separate Detailed Design Specification for each board type. The design descriptions of the common software modules and the common hardware characteristics are covered in the individual *HFC-6000 I/O Board Module Detailed Design Specifications*. The purpose of this document is to present the methods and strategies used to accomplish the operation and functions required of an HFC-6000 I/O board. The discussion of the operation and function of an HFC-6000 I/O board are presented using architectural, design, and implementation information.

2. Functional Description

This section describes the major functions performed by both design implementations of HFC-6000 I/O boards. The functional descriptions are presented to provide a context for understanding the internal operation of an HFC-6000 I/O board and how the functions performed by an HFC-6000 I/O board work within the overall architecture of the HFC-6000 distributed control system.

The major functions performed by an HFC-6000 I/O Board are:

- Initialization
- Communication with system controller connected to an Inter-Communication Link (ICL)
- Setting each digital/analog output channel using digital output images, and/or getting digital input images from each digital/analog input channel
- Self diagnostics functions

An I/O board generally has two operation stages: Initialization state and Normal Operation state. Upon power up or reset, the processor firmware will accomplish initialization for hardware, software, and communication set up. During initialization, some self diagnostics tests will be performed, such as RAM Write/Read test and EPROM/flash checksum test. Any error detected at this state is fatal and will cause the software to halt execution.

After completing initialization, the board will enter the Normal Operation stage. During normal operation, the I/O board handles communication with the HFC-SBC06 controller and performs an I/O scan at regular intervals to set digital/analog output channels and/or read digital/analog input channels. An HFC-6000 I/O Board can have digital input channels, digital output channels, analog input channels, and/or analog output channels connected to the field devices and equipments. An I/O board having output channels receives digital images for output channels from an HFC-SBC06 system controller at regular intervals, and then it uses this data to control each output channel. An I/O board with input channels reads the input image for each channel and sends the images of the digital or analog inputs to the HFC-SBC06 system controller at regular intervals.

A communication interface connects an I/O board to the ICL, which is an HFC proprietary, RS-485 serial network connecting the I/O boards to the HFC-SBC06 controller. Input values from plant field devices and output values for plant actuators are transferred between the HFC-SBC06 and I/O boards over the ICL. In addition, each HFC-6000 I/O board maintains internal diagnostic status and can report that status to the HFC-SBC06 controller.

During the time between successive I/O scans, the I/O board performs its self-diagnostics functions, which are mainly RAM tests. If any error is detected by the self-diagnostics tests, the I/O board will re-enter initialization stage to perform a restart.

How an I/O board scans its I/O channels and the specific content of message exchanges with the HFC-SBC06 vary with board type and channel configuration. Table 1 provides a list of

standard HFC-6000 I/O board types and a description of the I/O channels for each board type. Designs of HFC-6000 I/O board types having unique functions or a limited applicability will be covered in separate specifications.

Table 1. List of HFC-6000 I/O Boards

Name	I/O Channels
DO8J	8 channel relay output
DO16C	16 channel solid-state output
DO16J	16 channel relay output
DI16I	16 channel digital input
DC33	2 120-vac digital output and 12 digital input
DC34	2 125-vdc digital output and 12 digital input
DC35	1 120-vac digital output with seal-in circuit and 12 digital input
AI16ED	16 analog input, 0- to 10-v (DSP)
AI16FD	16 analog input, 4- to 20-mA (DSP)
AO8F	8 analog output, 4- to 20-mA
AO8FD	8 analog output, 4- to 20-mA (DSP)
AC36D	4 analog input, 4 analog output (DSP)
AI8LD	8 channel E-type thermocouple input (DSP)
AI8MD	8 channel 100 Ω RTD input (DSP)
AI4K	4 channel pulse input

The architecture of each HFC-6000 I/O board has been developed to support the functions that the board is required to perform. The following sections provide descriptions of the architecture and design of an HFC I/O board and discuss details of the functions performed by an HFC-6000 I/O board.

3. Module Architecture

3.1 I/O Board Architecture

The HFC-6000 product line currently includes two different hardware designs for I/O assemblies. One uses an Intel microprocessor as the main controller for the assembly, and the other uses a Digital Signal Processor (DSP) for this purpose. Figure 2 illustrates the major functional characteristics of an HFC-6000 I/O board. Major features of the I/O boards based on the Intel processor are as follows:

- An on-board 16-bit Intel 80C188EB microprocessor
- Two banks of memory:
 - Upper memory provides up to 64K by 8-bits of EPROM for functional program code storage.
 - Lower memory provides 32K by 8-bit of RAM for temporary storage of data being processed, such as I/O images, ICL messages, diagnostic data, etc.
- Two independent RS-485 serial interfaces for communication with the HFC-SBC06 system controller

- Onboard LEDs to provide a visual indication of board status
- Onboard jumpers and switches to control configuration options
- I/O digital/analog input/output channels
- Each I/O channel includes the circuitry to measure its input signal or to control its output signal. Each analog output channel includes a digital analog converter (DAC) in its I/O circuitry to convert digital images into analog signals. AI channels are configured with a single ADC per board to convert analog signals into digital images.
- An onboard dc-to-dc converter provides regulated +5-vdc logic power
- An onboard switch permits manual reset of the microprocessor
- Two card-edge connectors (P1 and P2) mate with corresponding backplane connectors. Signal assignments for P1 are identical for all I/O boards, so that any board can be inserted in any I/O slot of an HFC-6000 chassis. The P2 connector for each I/O board uses the same hardware, but signal assignments are unique for each board type.

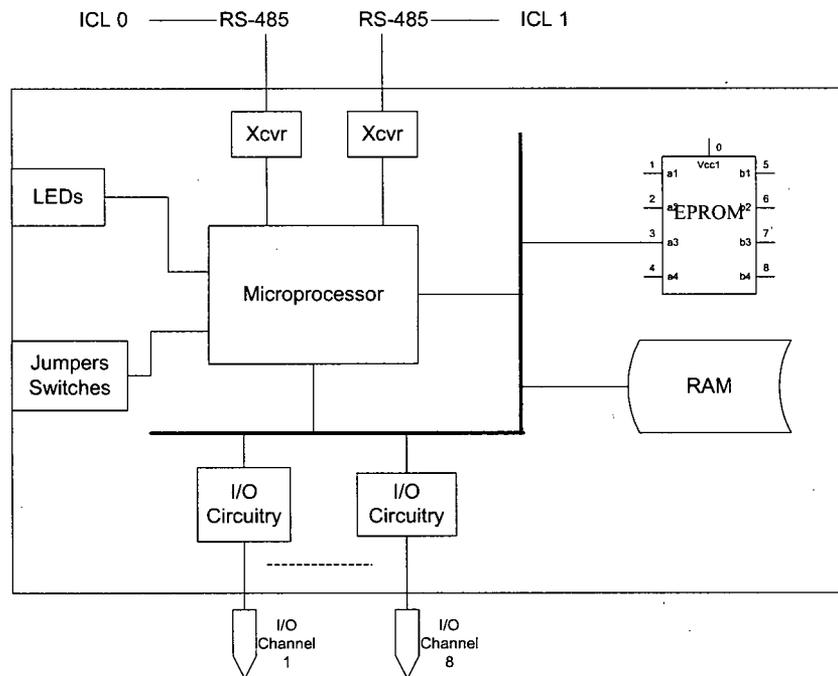


Figure 2. HFC I/O Board Module Architecture

DSP assemblies were developed as functional replacements for the analog I/O boards. Major architectural features of the DSP assemblies are as follows:

- An onboard DSP serves as the main processor for the assembly. The DSP controls the slave interface with the ICL, processes commands received from the HFC-SBC06 system controller, and constructs response messages.
- EEPROM, flash memory, and RAM arrays are embedded within the DSP.
- Redundant RS-485 interfaces enable communication with the HFC-SBC06 system controller.
- Onboard LEDs display operating status.
- Onboard jumpers and switches control configuration options.
- An onboard CPLD runs the scan cycle with each I/O channel.
- Separate hardware is provided for each I/O channel. Each AI channel has a dedicated ADC, and each AO channel has a dedicated DAC.
- The assembly receives redundant 24-vdc power rails from the backplane, and onboard voltage regulators provide all of the voltage levels required by the onboard hardware.
- An onboard switch permits manual reset of the DSP and CPLD.
- Two card-edge connectors (P1 and P2) mate with corresponding backplane connectors. Signal assignments for P1 are identical for all I/O boards, so that any board can be inserted in any I/O slot of an HFC-6000 chassis. The P2 connector for each I/O board uses the same hardware, but signal assignments are unique for each board type.

Each HFC-6000 I/O board supports communication with the HFC-SBC06 controller via the ICL. The ICL is structured as an RS-485 network implementing a master/slave communication control protocol. The HFC-SBC06 System Controller board serves as the network master for all communication transfers with its configured ICL stations. Each I/O board operates as a slave node on the ICL network to which it is attached. The system controller polls each I/O board in station address sequence, requesting data values for input channels and sending data values for output channels. Each I/O board can transmit over the ICL only after it has been polled by the HFC-SBC06 System Controller board.

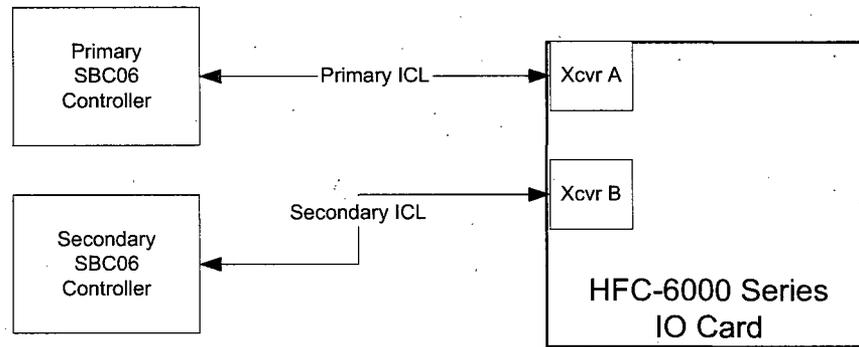


Figure 3. ICL Communication Architecture

As shown in Figure 3, each I/O board has two transceivers that are connected to the redundant ICL channels. Each ICL is connected to a separate HFC-SBC06 controller. The I/O board identifies which link has active communication during initialization and monitors that link as primary. Throughout normal operation of the HFC-6000 control system, one SBC-06 controller functions as primary and controls ICL scans; the other HFC-SBC06 is secondary and serves as a hot spare.

All polling messages from the HFC-SBC06 will be broadcast to every node on the same ICL. However, an I/O board will process only those messages that have its station address. The response messages from an I/O board will be received by the HFC-SBC06 controller only.

The messages carried over the ICL network can be categorized into two types:

- Normal Data Update messages
- Special Request messages using Universal Communication Packet (UCP) protocol

The normal exchange between the master HFC-SBC06 and an ICL station consists of a poll message to that station followed by a poll response from that station. This exchange provides the mechanism for regular I/O data transfer. The ICL protocol also supports several types of special messages that support specific functions. Two major special message types are:

- Diagnostic request message causes the I/O board to return the image of its diagnostic status data in its response message.
- Loopback request message permits the controller to verify normal operation of the secondary ICL.

3.2 Address Space Architecture

For I/O boards with an Intel microprocessor, memory is organized into two banks: one bank of EPROM and one bank of RAM. The memory banks are connected directly to the address and data lines of the microprocessor.

The upper bank of local memory for the microprocessor provides up to 64K by 8 bits of EPROM storage ending with the address of FFFFF_H. Upon power-up or reset, the internal address pointer of the microprocessor begins operation by accessing the data stored at address FFFF0_H in upper memory. Therefore, the first instruction of the initialization code must be located at this address.

The low memory bank provides up to 32K by 8 bits of static RAM for general data storage. Low memory begins at address 00000_H. This portion of memory contains the data and temporary storage buffers defined by the functional code in upper memory.

I/O boards with a DSP have embedded flash, EEPROM, and RAM arrays. The program address space consists of 4M of addressable instructions. The data EEPROM is located at the top of the addressable area and provides 1 Kb of storage ending with address 7FFFFE_H. The instruction flash provides storage for 22 K instructions. The detailed organization and arrangement of the memory structures vary with the specific device being used.

3.3 Software Architecture

Each HFC-6000 I/O board's software will be composed of a set of assembly language programs that will handle hardware and software initialization, I/O scan process, communication with the HFC-SBC06 controllers, and self-diagnostic tests functions. Figure 4 illustrates the functional processes executed by all HFC I/O boards.

RAM Write/Read Test
EPROM Test

Communication Routines

- Receive Interrupt Service Routine
- Process Command Routine
- Create Response Routine

Timer Interrupt Service Routines

This software is based on a set of modules that execute the functions that are common to all of the I/O boards. In addition to the common modules, each board type includes a set of program modules that execute functions unique to it. In general, these functions consist of the I/O channel scan routine and any data processing algorithm that may be required.

Upon power up or reset, the I/O firmware becomes activated. It runs an Initialization Routine to perform hardware and software initialization, processor configuration, and communication set up. During initialization, the RAM read/write and EPROM diagnostics tests are performed. Any error detected at this stage is fatal, and firmware execution will stop.

After initialization, the firmware enters a Main Routine which runs continuously throughout the normal operation. This Main Routine is an infinite loop. It calls an I/O Scan routine at regular intervals to perform the I/O Scan function. Between successive I/O scans, the Main Routine runs an idle task to perform self diagnostics RAM tests. If any failure is detected during self diagnostics tests, the Main Routine will transfer program control to the Initialization Routine to restart the firmware.

All I/O images will be stored in an I/O image buffer in RAM. The I/O Scan Routine will perform an I/O scan by either setting digital/analog output channel using digital output images from the I/O image buffer, and/or reading digital images from each digital/analog input channel and storing them in the I/O image buffer. How the I/O scan is performed varies with the specific type of I/O channels. Therefore, the I/O scan routine typically is different for each board type.

At the end of the I/O Scan routine, a Create Response routine is called to build a response message using the new I/O scan data and to store them in the Communication Message buffer in RAM. This area contains the command message received from the controller and the response message to be transmitted to the controller.

The software is interrupt-driven and handles three types of interrupts: timer interrupt, receive interrupt on the serial communication port, and transmit interrupt on the serial communication port. When an interrupt occurs, the program control is transferred to the configured Interrupt Service Routine. After the interrupt is handled, program control is transferred back to the routine that was running when the interrupt occurred.

When a receive interrupt occurs, indicating that a message is received from the ICL, the Receive Interrupt Service Routine will validate the message and call a Process Command Routine to process the message and to store any output images contained in the message in the I/O image buffer in RAM. Then a communication routine fetches the response message from the Communication Message buffer and transmits it to the HFC-SBC06 controller via the ICL.

Timers are used to control I/O scan intervals, communication response time out, etc. When a timer interrupt occurs, the configured Timer Interrupt Service Routine handles the interrupt.

3.3.2 DSP Assembly Software Architecture

The software for I/O boards based on the DSP consists of two separate programs: the DSP program and a CPLD program. The DSP program primarily controls the onboard ICL interface, and the CPLD program primarily executes the scan cycle. Since the detailed requirements of the scan cycle differ from one I/O board to another, most of the common software functions are controlled by the DSP. The software functions controlled by these two programs are described below.

The DSP program is organized as one main processing loop with various subordinate functions.

Main – This module contains the main program loop for the program. The DSP automatically begins running this module following powerup or reset. It begins operation by setting a Configuration flag and calling the Startup module. After the Startup module returns control, the Main module begins its normal program loop which controls two functions: I/O scan and an idle task.

The idle task runs a RAM diagnostic test repeatedly between successive scan cycles unless an interrupt occurs. The RAM test verifies the integrity of the internal DSP memory. Each time the test is completed successfully, the program triggers a strobe pulse for a watchdog timer that is integral to the DSP. Should the RAM test fail, the program branches back to the initialization sequence.

A programmable timer generates interrupts that are used to trigger periodic tasks. For the present application, these tasks consist of toggling the CPLD watchdog and incrementing the calibration timer. The DSP for AI modules controls two output signals to the CPLD, CAL1 and CAL2. These two signals define four operating states: Normal, LO CAL, HI CAL, and Factory CAL. Throughout normal operation, the DSP program uses the calibration timer to control the logic states of the CAL1 and CAL2 signals, and the CPLD responds accordingly.

The DSP distinguishes between scan cycles for AI channels and for AO channels. If the DSP assembly has AI channels, the DSP program waits until the CPLD notifies it that data is available. Then it initiates serial transfer of the new data from the CPLD to a working buffer. Subsequent processing of the raw count data received from the CPLD varies with operating mode and the type of data being received. After all signal conditioning is

complete, the final AI images are transferred to a response buffer in preparation for transfer to the controller. In contrast, the controller sends AO images to the board over the ICL as part of poll messages. Each time the DSP receives such data, it initiates serial transfer to the CPLD, and transfer of AO images to individual AO channels is controlled by the CPLD program.

Startup – The Main module calls the Startup module immediately after powerup or reset. It executes three major functions:

Configure port control registers, initializes the CPLD, sets control variables to default values, runs a RAM read/write test, and executes a flash checksum test. Any fault at this stage is fatal and results in program termination.

Configure two serial ports for ICL communication.

After the ICL interface is configured, any card specific initialization is accomplished and the first scan cycle is run. Once this is completed successfully, the module resets the Configuration flag and returns control to the Main module.

Qio - This module implements the QIO communication protocol required for the ICL. It creates the appropriate response message for each message received from the controller in accordance with DS002-000-02, ICL Protocol Design Specification. Each time the module is called, it first determines if a normal response or a special response message is required. It then copies the required data from a working buffer into one of two response buffers. Two response buffers are configured to ensure that one will always be available: one contains the current response data, and the other is available for constructing the next response message.

HFC_iocl – This module defines data structures and constants required for the QIO protocol.

UART – This module provides the program code to control operation of the redundant ICL interface. Three major control sequences are included:

Immediately after completion of initialization or following communication timeout, the module enables hunt mode. During this phase of operation, the module monitors first one ICL channel and then the other. This operation continues until the board receives its first valid message. The channel from which it received this message will be configured as the primary ICL and the other as secondary.

Once hunt mode has come to an end, the serial interface will generate an interrupt each time it detects activity on the primary link. After the first byte of a new message has been received from the ICL, the interrupt will trigger the Receive ISR. If the program is still in setup or if the address code is not correct, the ISR will return immediately. Otherwise, it will receive the entire message, perform CRC-16 validation, and call the correct function to complete the processing.

If an error is encountered during message reception, the module identified the error and increments the appropriate error counter.

Timer – The program includes two timer functions. One is used to control activation of periodic tasks; the other is used to control the wait interval for character reception from the ICL.

CPLD – This module provides functions required to interact with the onboard CPLD. The following functions are included:

Initialize the serial interface with the CPLD.

Reset the CPLD program.

Read data available status from the CPLD.

Read scan data from the CPLD

Write scan data to the CPLD.

Miscellaneous Functions – RAM test, EEPROM test, flash test, and CRC-16 validation. These functions are self-contained operations that occur at specific points during program operation.

The CPLD functions as the interface between the DSP and the onboard I/O channel hardware. It does not have any central processor or any single program processing loop. Rather, each program module defines one or more state machines that run in parallel with one another, based on a programmed combination of I/O signals, internal variables, and timing signals. As a result, the CPLD can control I/O scan cycles without DSP supervision, but the DSP uses a CPU_RST signal to disable scan operation during initialization or following watchdog timeout. Since the I/O processing requirements are generally different from one board type to another, each board type will generally require a different CPLD program. The general structure of the CPLD program is as follows:

Top – This constitutes the top-level program module for the CPLD. It contains instantiation statements for each of the other modules in the program and declarations for all signals. All I/O signals defined for the CPLD must be declared as either INPUT or OUTPUT. The instantiation statements constitute program calls to the other modules. Following the list of I/O declarations the Top module may include a series of executable statements. These statements either consist of short routines that do not warrant a separate program file or critical signals used by most of the other modules in the program. Typical common functions include control of chip select signals, LED status signals, reset signals, and the watchdog strobe signal. This module also controls the interrupt signal that notifies the DSP that new data is ready for transfer.

Timer – The Timer module is instantiated in the Top program file and generates the timing signals required to synchronize program operations.

DSP Serial – The CPLD hardware is connected to the DSP by a serial communication link composed of SDI, SDO and SCLK signals. This module controls reception of data from the DSP and then returns the response message (if any).

Hardware Specific Modules. The remaining program modules control the hardware devices associated with the I/O channels themselves. For AI boards, these modules create the buffer for the digital AI images, and also control the A/D conversion cycles. For AO boards, they create the data buffers, control data transfer to the DAC, and control the D/A conversion cycles.

3.3.3 Fault Detection and Processing

During Initialization, the software performs the RAM read/write test and EPROM/flash test to detect any hardware errors in the arrays. Any failure of these tests is fatal and will cause the program to halt execution.

Throughout normal operation, the software performs a RAM read/write self diagnostics test during the idle time between successive I/O scans. Any failure of these tests will cause the program to return to the initialization stage to perform a restart of software.

During communication with the HFC-SBC06 controller, hardware timers will be used to control the communication response time. Any communication timeout will cause the program to go to Communication Setup stage to reconfigure hardware communication channel and re-establish communication with the HFC-SBC06 controller.

3.4 Onboard Switches, Jumpers, and LEDs

This section lists the typical switches and board-edge LEDs for a standard HFC-6000 I/O board. An I/O board may include additional switches, jumpers and LEDs depending on board type. The descriptions of specific switches, jumpers, and LEDs for each particular HFC-6000 I/O board are provided in each board's Module Detailed Design Specification.

Assemblies with Intel processor provide the following minimum combination of user controls and indicators.

Reset Switch – Pushbutton switch accessible through the front bezel enables manual reset of the microprocessor and other major hardware components.

A/B LED – Lit when channel A is selected to receive data from the ICL; extinguished when channel B is selected to receive data from the ICL.

TX LED Flashes when the assembly is transmitting to the ICL.

RX LED Flashes when the assembly is receiving data from the ICL.

Assemblies with the DSP provide the following minimum combination of user controls and indicators.

Reset Switch – Pushbutton switch accessible through the front bezel enables manual reset of the microprocessor and other major hardware components.

LINK LED – Lit red when channel A is selected to receive data from the ICL; lit green when channel B is selected to receive data from the ICL.

TX A LEDFlashes when channel A is transmitting to the ICL.

RX A LEDFlashes when channel A is receiving data from the ICL.

TX B LEDFlashes when channel B is transmitting to the ICL.

RX B LEDFlashes when channel B is receiving data from the ICL.

Additional indicators are provided on a module-by-module basis to indicator overall operating status.

4. Module Design Constraints

The following is a list a specifications that constrain the design of an HFC-6000 I/O board module.

4.1 Communication Interface Specifications

Document DS002-000-02 ICL Protocol Component Specification.

4.2 Detailed Design Specifications

901-000-02, I/O Module Detailed Design Specification
DS901-000-03, HFC-DO8J Detailed Design Specification
DS901-000-17, HFC-DO16C/J Detailed Design Specification
DS901-000-04, HFC-DI16I Detailed Design Specification
DS901-000-05, HFC-DC33 Detailed Design Specification.
DS901-000-06, HFC-DC34 Detailed Design Specification
DS901-000-26, HFC-DC35 Detailed Design Specification
DS901-000-55, HFC-AI16E/FD Detailed Design Specification
DS901-000-08, HFC-AO8F Detailed Design Specification
DS901-000-63, HFC-AO8FD Detailed Design Specification
DS901-000-62, HFC-AC36D Detailed Design Specification
DS901-000-56, AFC-AI8LD Detailed Design Specification
DS901-000-57, HFC-AI8MD Detailed Design Specification
DS901-000-12, HFC-AC4KD Detailed Design Specification

5. Design Safety

5.1 Common Modules

The following paragraphs address those design safety considerations that are common to both input and output modules.

5.1.1 Security

[

]

5.1.2 Risk

[

]

5.2 *Output Modules*

The following paragraphs address the design safety considerations unique to output modules.

5.2.1 Criticality

[

]

5.2.2 Hazard

[

]

5.2.3 Risk

[

]

5.3 *Input Modules*

The following paragraphs address the design safety considerations unique to input modules.

5.3.1 Criticality

[

]

5.3.2 Hazard

[

]

5.3.3 Risk

[

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HFC-6000 Product Line

HFC-SBC06-DPM06

Module Detailed Design Specification

DS901-000-01

**Rev D
(COST REDUCTION VERSION)**

Effective Date	<u>12/12/2008</u>
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Table of Contents

1. INTRODUCTION.....	5
2. HARDWARE DETAILED DESIGN FOR HFC-SBC06	5
2.1 MODULE SPECIFICATION.....	5
2.1.1 <i>Environmental Extremes for Reliable Equipment Operations.....</i>	5
2.1.2 <i>Board Specification.....</i>	5
2.1.3 <i>C-Link - IEEE 802.3 10BASET Communication Links.....</i>	6
2.1.4 <i>ICL - EIA RS-485 communication links.....</i>	6
2.2 ONBOARD POWER DISTRIBUTION	6
2.2.1 <i>Power Distribution.....</i>	6
2.2.2 <i>Hardware Reset</i>	7
2.3 CONNECTOR PINOUTS	7
2.4 SYS PROCESSOR SECTION	9
2.4.1 <i>I/O Map.....</i>	9
2.4.2 <i>Real Time Counter Interrupts.....</i>	11
2.5 ICL PROCESSOR SECTION	11
2.5.1 <i>Interrupt Processing</i>	11
2.5.2 <i>ICL Interface.....</i>	12
2.6 CPC PROCESSOR SECTION.....	13
2.6.1 <i>Interrupt Processing</i>	13
2.6.2 <i>Ethernet Interface</i>	13
2.7 SOE TIMER.....	15
2.8 FPGA	16
3. HARDWARE DETAILED DESIGN FOR HFC-DPM06.....	17
MODULE SPECIFICATION.....	17
3.2 ONBOARD POWER DISTRIBUTION	17
3.3 DIP SWITCH STATUS TRANSFER.....	17
3.4 HARDWARE CONNECTIONS	18
4. MEMORY CONFIGURATION AND ACCESS CONTROL.....	20
4.1 MEMORY CONFIGURATION	20
4.1.1 <i>Private Memory Configuration for the SYS Processor.....</i>	21
4.1.2 <i>Private Memory Configuration for ICL and CPC Processors</i>	21
4.1.3 <i>Public Memory.....</i>	21
4.1.4 <i>Dual Ported Memory</i>	22
4.2 MEMORY ACCESS CONTROL.....	22
4.2.1 <i>Memory Control Signals for the SYS Processor.....</i>	22
4.2.2 <i>I/O and Memory Control for the CPC and ICL Processors</i>	25
4.2.3 <i>Public Memory and DPM Access</i>	26
4.2.4 <i>RAM Access Control.....</i>	26

5. SOFTWARE DETAILED DESIGN SPECIFICATION.....	26
5.1 INITIALIZATION ROUTINES.....	27
5.1.1 <i>General Initialization Sequence</i>	27
5.1.2 <i>SYS Processor Application Data Initialization</i>	29

List of Tables

Table 1. P1 Pin Assignments	8
Table 2. Connector J7 and J9 Pin Assignments	9
Table 3. SYS Processor I/O Map	10
Table 4. Write Function for F490 _H	10
Table 5. Status Port	11
Table 6. NIC-DPM Control Signals.....	14
Table 7. Configuration Data Organization.....	18
Table 8. P1 Pin Assignments	19
Table 9. Memory Control Signals for SYS Processor	23
Table 10. I/O Mapping for 386EX Processors.....	25
Table 11. Memory Control Signals for ICL and CPC Processors	25

List of Figures

Figure 1. Memory Address Space Architecture.....	20
Figure 2. Processor Bus Structure Organization.....	23

1. Introduction

This HFC-SBC06 board and HFC-DPM06 board function together as a System Controller Module in an HFC-6000 control system. The overview of the architecture, functions and module structure of the HFC-SBC06 board and HFC-DPM06 board are provided in document MS901-000-01, HFC-SBC06-DPM06 Module Design Specification. The user of this document should be already familiar with document MS901-000-01. This document provides detailed structure and design descriptions on specific parts or features of the HFC-SBC06 board and HFC-DPM06 board, including hardware characteristics and software implementation methods. Rev D has the changes for the cost reduction consolidation of the 4 Xilinx CPLDs into 1 Lattice FPGA.

2. Hardware Detailed Design for HFC-SBC06

2.1 Module Specification

- Assembly 400417-82 Pentium 133 CPU, CAT5, industrial grade parts

2.1.1 Environmental Extremes for Reliable Equipment Operations

- Temperature: 0° to 55° C (operating)
0° to 70° C (storage)
- Humidity: 5% to 95% RH, non-condensing

2.1.2 Board Specification

- Supply Voltage +24 VDC
- Maximum Power Dissipation 18 Watts
- Onboard Clock Rate(s)

Microprocessor Clock	66.66 MHz
CPC & ICL Processor Clock:	50 MHz
ICL Bit Rate Clock:	11.0592 MHz
CPC Serial Data Clock:	20 MHz
SOE Master Clock	4.000 MHz

- Mounting Requirements

The HFC-6000 product line includes both 19- and 23-in. controller chassis. Slots 12 and 14 of the 19-in. controller rack are designed to accept HFC-6000 controllers; slots 16 and 18 of the 23-in rack are designed for controllers. The slot between the two controller positions is designed to accept an HFC-DPM06 assembly.

2.2.2 Hardware Reset

The HFC-SBC06 board includes a DS1232 MicroMonitor chip (the SYS Watchdog timer) and a DS1233A EconoReset chip to control hardware reset functions. The MicroMonitor chip monitors the voltage level of the +5-vdc power rail, the state of the onboard reset switch (SW1) and normal cycling of the SYS processor. The EconoReset switch monitors the voltage level of the 3.3-vdc logic power rail connected to the SYS processor.

When power is first applied to the board, the low state of both logic power rails causes the two chips to hold the RST_IN/ signal at a low level. After logic power increases above 4.5 vdc, the MicroMonitor chip keeps the RST_IN/ signal low for an additional 350 ms to ensure that all transient signals have dissipated before the three processors begin operation. During subsequent operation, the two chips monitor power for a significant drop in the voltage level of the onboard logic power rails.

When the SYS processor begins running the system software, it must supply a low active STROBE/ pulse to the MicroMonitor at regular intervals. If the delay between successive STROBE/ pulses exceeds .5 seconds, the MicroMonitor chip automatically activates the RST_IN/ signal to reset all three processors on the card. The operator can initiate reset of all components on the card by toggling the S1 power switch on the board.

2.3 Connector Pinouts

The HFC-SBC06 system controller board has one backplane connector (P1) and two RJ45 connectors for communications ports (J7 and J9). The backplane connector (P1) provides contacts for power, communication with the DPM, and the serial ICL for communication with I/O cards in the controller card rack. The two RJ45 connectors provide the interface with the redundant C-Link. Table 1 and Table 2 summarize the specific pin assignments for each connector. One additional JTAG connector (J2) is located on the surface of the card. The connector J2 is used for programming of the FPGA chip. The connector J1 is used for programming of the flash memory associated with the SYS processor. The connector J8 is used for programming of the flash memory associated with the subordinate (B&C) processors. These ports are not used or accessible during normal operation of the controller.

Table 1. P1 Pin Assignments

Category	Pin	Mnemonic	Pin	Mnemonic
Power	[]	[]	[]	[]
Serial Bus	[]	[]	[]	[]
DPM Control	[]	[]	[]	[]
DPM Address Signals	[]	[]	[]	[]
DPM Data Signals	[]	[]	[]	[]
DIP Switch Control	[]	[]	[]	[]

Category	Pin	Mnemonic	Pin	Mnemonic
DIP Switch Data	[[
]]		
Failover Control	[[[[
]]]]
Ethernet to Backplane Connection	[[[[
]]]]

Table 2. Connector J7 and J9 Pin Assignments

Pin	Name
1	[]
2	[]
3	[]
4	[]
5	[]
6	[]
7	[]
8	[]

2.4 SYS Processor Section

2.4.1 I/O Map

The SYS processor, which is a Pentium processor, has no built-in chip select, interrupt controller, I/O ports or timer functions. The Lattice FPGA provides these functions. This section provides descriptions of decoded address provided by the FPGA.

Address decoding is accomplished for three blocks of I/O mapped addresses. The first block of addresses range from F400_H to F4FF_H and are used to access internal programmable peripheral registers within the FPGA. The second block of addresses range from 0200_H to 02FF_H and are used to access I/O ports included in the FPGA. The third block ranges from 0040_H to 007F_H and are used to access the DIP switches and LEDs. Table 3 lists the decoded addresses and their functions.

Table 3. SYS Processor I/O Map

Address Range	I/O Write Function	I/O Read Function
[]	Program upper Chip select logic (UCS)	None
[]	Program middle chip select logic (MCS)	None
[]	Program lower chip select logic (LCS)	None
[]	Program page select logic (flash page frame)	None
[]	Program multiplexed address (flash page latch)	None
[]	Program memory read/write control	Internal input port (status port)
[]	Internal output port (control port)	None
[]	Public memory control enable	None
[]	Sanity control (watchdog timer port)	
[]	Maintenance Failover enable	
[]	LEDs DS3 and DS4	DIPSWITCH 0
[]	LEDs DS3 and DS4	DIPSWITCH 1
[]	LEDs DS3 and DS4	DIPSWITCH 2
[]	LEDs DS3 and DS4	DIPSWITCH 3

The FPGA controls a 16-bit data bus. Data from this bus is used to control the multiplexed address logic, the page select logic, the low chip select logic, the middle chip select logic, the upper chip select logic, the memory read/write control logic, and the status of the external LEDs. It is also used to transfer external DIP switch status information, input port information, and interrupt vector information during interrupt acknowledge cycles.

2.4.1.1 I/O Port F490_H – Memory Control and Status Port

The status of data lines 0 through 4 and data lines 6 and 7 are latched during a **write** to I/O address F490_H. This latch is used to control various memory read, memory write, and memory select signals. Table 4 defines each of these latches and the data lines that control them.

Table 4. Write Function for F490_H

Data Line	Function
0	[]
1	[]
2	[]
3	[]
4	[]
6	[]
7	[]

By controlling the status of these control latches, different memory devices can be “mapped” to the same address. The status of these latches will determine which type of memory is actually accessed. Mapping both flash and RAM to the same address, enabling RAM write and flash read, and disabling flash write and RAM read, allows all memory writes to modify RAM memory while all memory reads come from flash memory. This allows downloads to

be written to RAM while still running from flash until the downloaded data is verified. Disabling flash allows the SYS processor to initially boot from EPROM, transfer the EPROM contents to code flash, and then execute from code flash.

An IO read to address F490_H will return various input port statuses as defined in Table 5.

Table 5. Status Port

Data Line	Signal
0	[]
1	[]
2	[]
3	[]
4	[]
7	[]

2.4.1.2 I/O Port 200_H – Watchdog Timer Port

The internal output port at address 200_H strobes the hardware watchdog on every IO write to that address. Also the software can cause a failover to the secondary controller by writing a “0” on data bit 0 to this address.

2.4.1.3 I/O Port 210_H – Maintenance Failover Enable/Disable Port

IO address 210_H controls the status of the maintenance failover enable circuit. Writing a “1” on data bit 0 to this address will enable maintenance failover, likewise writing a “0” will disable the maintenance failover feature. Writing a “1” on data bit 0 to IO address F4A0_H will lock the public memory bus access, preventing any other processor from accessing the public memory bus.

2.4.2 Real Time Counter Interrupts

On the -82 assembly, the 50 mHz clock is replaced by a 66 mHz and the FPGA divides the clock input by 666,000. These timer interrupts are used by the SYS processor for real time control. When the SYS processor receives an interrupt from the FPGA U27, it generates an interrupt acknowledge cycle and this FPGA responds to this acknowledge cycle by providing interrupt vector 43_H.

2.5 ICL Processor Section

2.5.1 Interrupt Processing

The ICL 80386EX microprocessor includes an internal interrupt controller that provides input ports for one nonmaskable interrupt (NMI), four levels of external maskable interrupts (INT0/ through INT3/), and internal interrupts from programmable timers and a serial communication controller. The four maskable interrupts, and the NMI interrupt are not used for this

application. However, the serial bus interface triggers internal interrupts to coordinate data transfers via the serial transceiver.

2.5.2 ICL Interface

The ICL processor provides two integral serial communication channels (designated channel 0 and channel 1) that can be programmed to support a variety of communication protocols. For the present application, both channels are connected to onboard transceivers that are configured to support RS-485 communication links. The TXD0# and RXD0 ports of the microprocessor are connected to the transceiver for serial channel 0, and the programmable port P1.4 controls the TXEN0 output signal. The TXD1 and RXD1 ports of the microprocessor are connected to the transceiver for serial channel 1, and the programmable port P1.0 controls the TXEN1 output signal. In addition, the card includes three jumper nodes (J5-1, J5-2, and J5-3) that can be used to interlock the TXEN signals with the SANE/ or the PRI/ signals. When the HFC-SBC06 board is used as a redundant controller, a jumper should be installed from node J5-1 to J5-2. This hardware interlock requires the controller chassis to complete its powerup initialization sequence successfully (SANE status TRUE) and become the primary controller before the ICL processor can begin transmitting over its serial link. Removing all jumpers results in a configuration in which the transmit interface remains enabled as long as logic power is present.

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2.6 CPC Processor Section

2.6.1 Interrupt Processing

The CPC 80386EX microprocessor includes an internal interrupt controller that provides input ports for one nonmaskable interrupt (NMI), four levels of external maskable interrupts (INT0/ through INT3/), and internal interrupts from programmable timers and a serial communication controller. The CPC processor receives separate interrupts from the two NIC chips. These inputs are routed to interrupt ports INT0/ and INT1/, respectively, to coordinate data transfers between the processor and the Ethernet hardware interface.

2.6.2 Ethernet Interface

The Ethernet interface is implemented by the DP83902 NIC, which is a single VLSI device that includes the Media Access Control (MAC) and Encode/Decode (ENDEC) with AUI interface and 10BASET interface functions in accordance with IEEE 803.2 standards. (The AUI is not used for this application.) The 10BASET transceiver functional block incorporates receiver, transmitter, heartbeat, loopback, jabber detection, and link integrity functions. The integrated ENDEC module allows Manchester encoding/decoding by means of a differential transceiver and phase-lock loop decoder at 10 Mb/sec. This section also includes a collision detector and diagnostic loopback capability.

The CPC processor is connected to hardware for two identical Ethernet channels designated CH0 and CH1. Major components for each channel include a DPM, serial interface network controller chip (NIC), isolation hardware, and a 20-MHz crystal oscillator (shared by the two channels). A single interrupt signal is routed from each NIC directly to the CPC processor (NIC0_INT to INT2 input port, NIC1_INT to INT1 input port). All other timing and control signals are routed to the FPGA chip, which coordinates all transfers between the NIC and the CPC processor.

2.6.2.1 Interface Configuration

Both Ethernet channels are configured with 10BASET (TPI) physical interfaces; jumper posts W2, W3, W5, and W6 enable the user to configure functional characteristics of the NIC. Following powerup, the hardware circuitry pulls the AUI/TPI port of each NIC low, and logic in the NIC chip enables the TPI interface. TPI interface enables differential RX and TX signal lines with 10BASET interface. Other Ethernet physical interface options are not used and are disabled.

2.6.2.2 FPGA Design for NIC Support

The FPGA supports CPC processor's read and write to the internal registers of the two NIC chips, as well as accesses the contents of the DPM interface to each NIC chip.

The CPC processor's request to access the internal registers of each NIC is used to synchronize these requests with the acknowledge signals from the NICs. The ready input to

the processor is delayed until an acknowledge signal is received from the addressed NIC. This is accomplished through two identical state machines, one for each NIC interface. These state machines detect the CPC processor's request to access that NIC, output the NIC chip select signal, wait for the NIC to respond to the request with an acknowledge, create a properly timed write strobe to the NIC (for write requests), and then release the ready signal to the processor after the proper number of wait states.

The FPGA uses the CPC processor's NIC-DPM requests, the read strobe, and write strobe to create all of the inputs required by the DPM for each NIC. Table 6 lists the output signals for NIC-DPM.

Table 6. NIC-DPM Control Signals

Description	NIC 0	NIC 1
[]	[]	[]
[]	[]	[]
[]	[]	[]
[]	[]	[]
[]	[]	[]

2.6.2.3 CPC Processor's Control Over NIC

The CPC processor controls overall operation of the Ethernet interface, transfer of data to or from the NIC via DPM, and transfer of data to the main processor via public memory. Following powerup or manual reset, the processor can activate NIC0RST/ (port P1.3) and NIC1RST/ (port P1.2) output signals to disable data reception or transmission at both Ethernet ports. After the controller becomes both sane and primary (SANE/ and PRI/ signals both low), the software can disable the reset signals to permit normal operation of the interface to start.

While normal operation of the NIC is enabled, it activates an interrupt (NIC0_INT or NIC1_INT) to the CPC processor following reception of data from the interface, transmission of data to the interface, or after completion of DMA transfer with DPM. The specific response of the processor to this interrupt depends on current status. The process of reading current status requires the following sequence:

1. Place the NIC in slave mode by pulling the NICX_IO/ signal low.
2. Place the address for a particular register on address lines C_LA01 through C_LA04.
3. Run a bus read cycle with the selected NIC.

Similarly, the processor can use the same sequence for transferring command data to a selected internal register of the NIC. The general sequence of operation necessary for the LAN processor to control operation of the interface is as follows:

1. Access public memory and transfer data to be broadcast to local private memory.
2. Initiate DMA transfer of data from private memory to DPM.

3. Initiate communication with the NIC and identify the starting address of the new data.
4. While the NIC is operating in standalone mode, it controls its access to DPM, encoding of data for transmission to the external link, and status monitoring. Once it completes a commanded operation, it activates its interrupt to the processor.
5. After the NIC completes data reception from the external interface, the CPC processor initiates DMA read from DPM to private memory.
6. After completing the DMA transfer, the processor initiates transfer of the new data through public memory to the main processor.

2.7 SOE Timer

The SOE timer is implemented by a timer with 100 μ S resolution contained within the FPGA. [

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2.8 FPGA

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3. Hardware Detailed Design for HFC-DPM06

Module Specification

- Environmental Extremes for Reliable Equipment Operations
 - Temperature: 0° to 55° C (operating)
0° to 70° C (storage)
 - Humidity: 5% to 95% RH, non-condensing
- Supply Voltage +24 VDC +/- 10%
- Maximum Power Dissipation 5.76 Watts
- Mounting Requirements

All HFC-6000 controller racks contain three slots on the right side of the chassis reserved for controller hardware. The middle slot of the three must contain an HFC-DPM06 assembly.

3.2 Onboard Power Distribution

The card receives redundant 24-vdc power feeds from backplane connector P1. The two power feeds are diode auctioneered and routed to FET switch Q9. The gate input of Q9 is connected to two optical isolators in parallel. Optical isolator U9 is connected to a 5-vdc input signal from controller A, and optical isolator U10 is connected to a 5-vdc input signal from controller B. If a 5-vdc input is available either from controller A or from controller B, one of the two optical isolators will become forward biased. While either optical isolator is forward biased, the gate circuit of the FET passes the input power feed to voltage regulator U5, and the voltage regulator provides +5vdc operating power to all other hardware on the card. When both controllers are powered down (or missing), the FET becomes cut off, and operating power is removed from all components on this card.

3.3 DIP Switch Status Transfer

Switch configurable data for the HFC-SBC06 board is organized as four data words. The source for one of these data words is physically located on the controller card, and the source for the remaining three is on the HFC-DPM06 card. The data on the HFC-SBC06 SYSTEM CONTROLLER is organized as the high byte of one data word, and each of the inputs from the DPM card is organized as the low byte of a single data word. When the HFC-SBC06 SYSTEM CONTROLLER is configured to operate as a redundant controller, both controller A and controller B read the switch parameters from the DPM card as part of internal configuration following powerup or reset. Each controller employs three control signals (DIPSW0_A, DIPSW1_A, DIPSW2_A; DIPSW0_B, DIPSW1_B, DIPSW2_B) to enable transfer of the configuration data from the DIP switches. Hardware on the DPM card permits both controllers to read configuration data at the same time without causing bus collisions. Table 7 indicates the content of DIP switch transferred for each combination of DIPSWn

signals. As indicated in the table, the last data word contains SANE and PRIMARY status for the other controller. Each controller can read this status byte periodically throughout normal operation. Control signal DIPSW0_A or DIPSW0_B must be active for any of the DIP switch data to be read.

Table 7. Configuration Data Organization

Control Signal States			Data Transfer Enabled
DIPSW0	DIPSW1	DIPSW2	
[]	[]	[]	[]
[]	[]	[]	[]
[]	[]	[]	[]
[]	[]	[]	[]
[]	[]	[]	[]

3.4 Hardware Connections

The HFC-DPM06 has a single backplane connector (P1). Table 8 summarizes the specific pin assignments for this connector. One JTAG connector (J1) is located on the surface of the card. This connector is used for programming the FPGA chip for the DIP switch interface. This port is not used or accessible during normal operation of the controller.

Table 8. P1 Pin Assignments

Category	Pin	Mnemonic	Pin	Mnemonic
Power	[]	[]	[]	[]
Ground Bus	[]	[]	[]	[]
DPM Control	[]	[]	[]	[]
DPM Address Signals	[]	[]	[]	[]
DPM Data Signals	[]	[]	[]	[]
DIP Switch Control	[]	[]	[]	[]

Category	Pin	Mnemonic	Pin	Mnemonic
DIP Switch Data	[]	[]	[]	[]
Failover Control	[]	[]	[]	[]

4. Memory Configuration and Access Control

Each processor has their private RAM, flash memory, PROM and has access to the public memory area and the dual ported memory on the HFC-DPM06 board. The CPC processor also has access to the NIC-DPM, the dual ported memory for the NIC.

4.1 Memory Configuration

Figure 1 shows the memory address space architecture. Please note that the addresses are just an example, because the starting addresses, size, and configuration of each memory array are all software configurable.

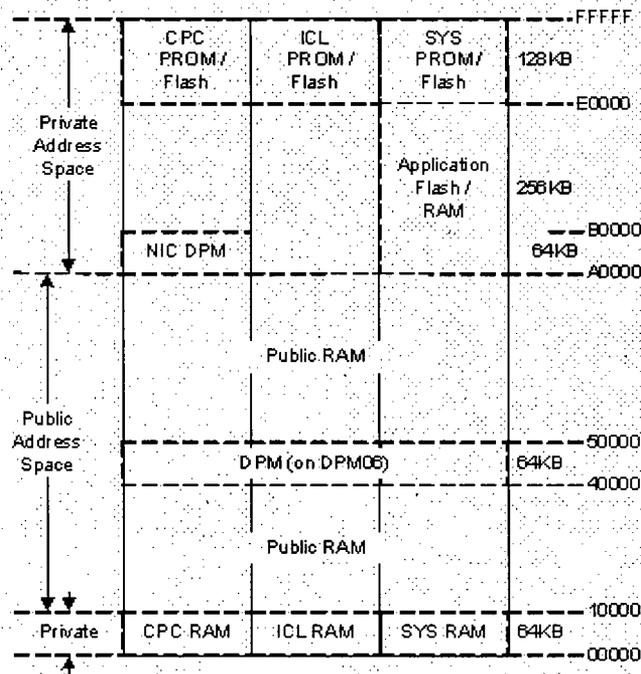


Figure 1. Memory Address Space Architecture

4.1.1 Private Memory Configuration for the SYS Processor

The private memory for the SYS processor is organized into upper, mid, and low memory arrays. The following paragraphs provide descriptions of the private memory configuration of the SYS processor.

- High Memory - The upper bank of private memory can be provided by 256K bytes (128K X 16 bits) of PROM storage or flash memory ending with the address of FFFFF_H. This portion of memory provides storage place for the system software. Access to memory in this bank is enabled by the UCS/ chip-select signal. The choice of PROM or flash memory located in the high memory area is determined by the status of jumper J1.
- Mid Memory - An 8-Mbit boot block flash memory chip (512K X 16) serves as the mid memory array. The starting address of mid memory is set by the system software installed in upper memory, and the memory write function is enabled/disabled by onboard switch S2. The flash memory array provides nonvolatile storage for the controller application program, and S2 can be used to prevent online modification of this program.
- Low Memory - The low memory bank provides 8 Mbit of RAM (two 512K X 8 RAM chips). Low memory begins at address 0000:0000 and is configured to permit full word, low byte, or high byte data transfers. The ending address of the low memory array is controlled by the processor. RAM provides temporary storage place for the execution of the system software.

4.1.2 Private Memory Configuration for ICL and CPC Processors

The ICL and CPC processors have the same memory configuration as described in the following paragraphs.

- High Memory - High memory provides up to 256K bytes (128K X 16bits organization) of PROM storage for system software code. The system software code can be transferred to an 8-Mbit (512K X 16 bits) flash memory. Onboard switch SW2 controls the WRITE ENABLE function for all of the flash memory chips. Once the program software has been transferred to flash memory, the processors can be configured to operate from flash rather than PROM.
- Low Memory - Low memory RAM provides 8 Mbit (two banks of 512K X 8) of volatile memory. Access to RAM is enabled by the CS6#, BLE#, and BHE# signals. RAM provides temporary storage place for the execution of the system software.

4.1.3 Public Memory

The Public Memory on the HFC-SBC06 board provides 8 Mbit (two 512K X 8 bit RAM chips) array of volatile RAM. The public memory array is configured with high and low bytes. As a result, the bus master will have access for high byte, low byte, or full word

read/write transfers. The starting and final address for the array will be software configurable by the SYS processor. This memory area contains all dynamic data that needs to be shared by the three processors on the controller board.

4.1.4 Dual Ported Memory

The DPM array consists of 32 K by 16 bits of volatile RAM configured with high and low bytes in the public memory area. The memory array is physically located on the HFC-DPM06 board in the slot next to the controller (or between two controllers in a redundant configuration). [

] The DPM is used for redundant controller configuration to transfer critical information from the primary controller to the secondary controller at regular intervals. An integral memory controller permits simultaneous access by primary and secondary controllers.

4.2 Memory Access Control

The onboard FPGA provides chip select and control signals for the processors. The FPGA coordinates bus transfers to local private memory as well as access to the common public memory bus. Figure 2 shows processor bus structure organization.

Each processor has a dedicated data bus connected to its private memory and an interface with the public bus for access to public memory and DPM. All logic components in the common section of the controller are connected to the common public bus. The three processors each use this bus to read current status from public memory and to write status updates to public memory. When the controller is operating in a redundant configuration, the Pentium processor on the primary controller also transfers current status from public memory to the DPM array. Similarly, the Pentium processor on the secondary controller transfers updated status from DPM to its public memory array.

Memory access controls are provided by the FPGA which provides chip select and memory access functions for the SYS processor, as well as the ICL and CPC processors.

4.2.1 Memory Control Signals for the SYS Processor

Table 9 lists memory control outputs provided by the FPGA for access to different memories for the SYS processor.

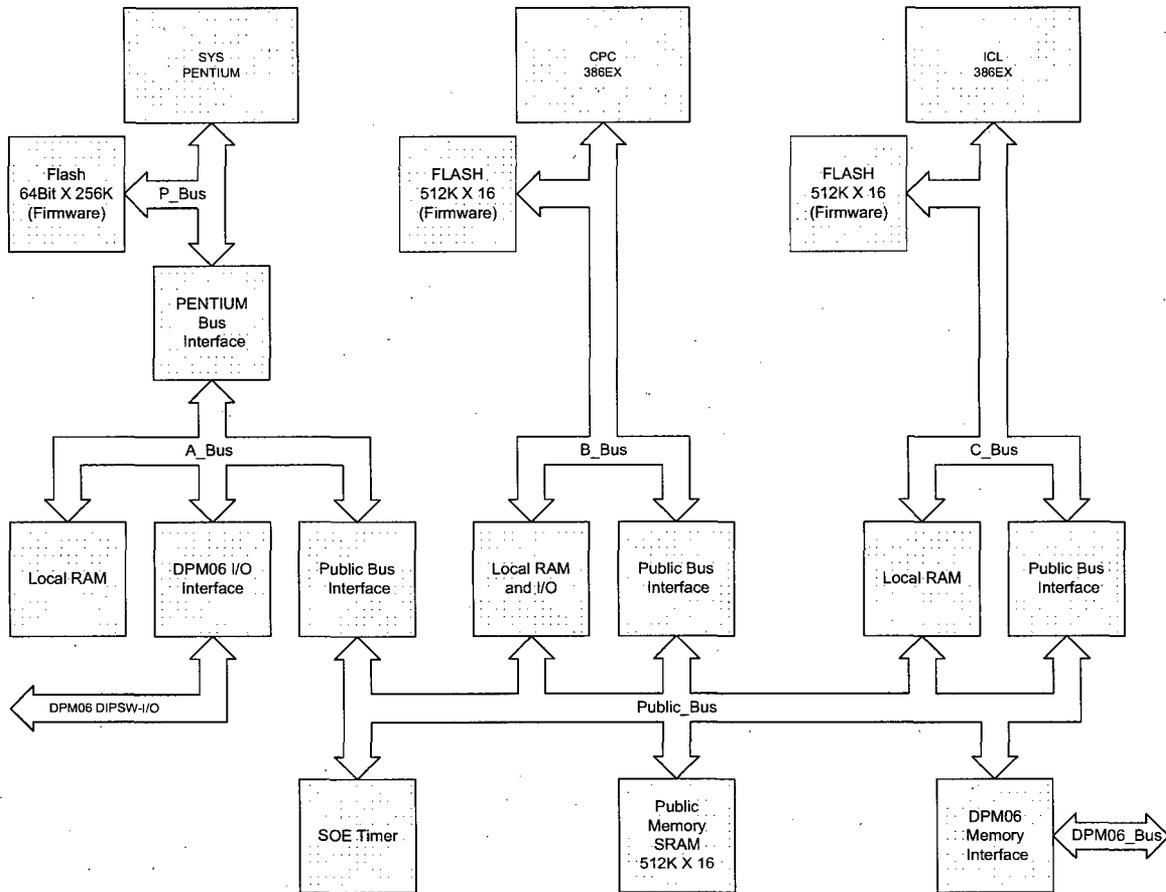


Figure 2. Processor Bus Structure Organization

Table 9. Memory Control Signals for SYS Processor

Signal	Description
EPROM CHIP ENABLE	1) Upper chip select address range if boot strap is installed and EPROM read is enabled (used to boot from EPROM) 2) Middle chip select address range if applications flash is disabled (used when applications is in EPROM).
EPROM READ STROBE	Memory read cycle if EPROM chip enable is active.
CODE FLASH CHIP ENABLE	1) Upper chip select address range if bootstrap is not installed. (Used for normal code execution from code flash) 2) Upper chip select address range if boot strap is installed and code flash write is enabled (used to programming code flash from EPROM when booting from EPROM)
CODE FLASH READ STROBE	All memory read cycles

CODE FLASH WRITE STROBE	Upper chip select address range if code flash write is enabled.
APPLICATIONS FLASH CHIP ENABLE	1) Middle chip select address range if applications flash read is enabled during a memory read cycle (used to read applications program if applications is in flash) 2) Middle chip select address range if applications flash write is enabled during a memory write cycle (used to program applications program into flash)
APPLICATIONS FLASH READ STROBE	1) Memory read cycle if APPLICATIONS CHIP ENABLE is active and applications flash read is enabled.
APPLICATIONS FLASH WRITE STROBE	Memory write cycle if APPLICATIONS CHIP ENABLE is active and applications flash write is enabled.
RAM CHIP ENABLE (LOW BYTE)	1) Low chip select address range is active and low byte enable is active. (used for normal low memory access) 2) Middle chip select address range is active and low byte enable is active if either ram read or ram write is enabled. (used to "overlay" applications flash memory)
RAM CHIP ENABLE (HIGH BYTE)	1) Low chip select address range is active and high byte enable is active. (used for normal low memory access) 2) Middle chip select address range is active and high byte enable is active if either ram read or ram write is enabled. (used to "overlay" applications flash memory)
RAM READ STROBE	1) Memory read cycles to low chip select address range (used for normal memory reads to low memory) 2) Memory read cycles to middle chip select address range if ram read is enabled (used to overlay applications memory)
RAM WRITE STROBE	1) Memory write cycles to low chip select address range (used for normal memory writes to low memory) 2) Memory write cycles to middle chip select address range if ram write is enabled (used to overlay applications memory)
PUBLIC MEMORY SELECT	1) All memory read or write cycles not in any programmed address range.

4.2.2 I/O and Memory Control for the CPC and ICL Processors

The FPGA supports both ICL and CPC processor's I/O ports and memory control functions.

4.2.2.1 I/O Mapping Through The FPGA

The FPGA contains an identical control port, the Data Steering Control Register (DSCR), for each processor. Each processor updates its respective DSCR with an I/O write to address 0080_H. Table 10 lists the functions provided by the DSCR for each processor and the data bus bits that control these functions. These control functions are used to control chip selects, read strobes, and write strobes for the RAM, FLASH, and EPROM memories for the ICL and CPC processors.

Table 10. I/O Mapping for 386EX Processors

DATELINE	FUNCTION
[]	[]
[]	[]
[]	[]
[]	[]
[]	[]

4.2.2.2 Memory Control Signals

The memory control outputs provided for each of the two 80386EX processors are summarized in Table 11.

Table 11. Memory Control Signals for ICL and CPC Processors

Signal	Function
[]	[]
[]	[]
[]	[]
[]	[]
[]	[]
[]	[]
[]	[]
[]	[]
[]	[]
[]	[]

4.2.3 Public Memory and DPM Access

The FPGA provides arbitration for all memory accesses to both onboard public memory and off board dual ported memory. All three processors provide public memory requests into this FPGA. The FPGA determines if the request is for onboard public memory or off board DPM, controls access to the proper memory, and grants access to the requesting processor. If one of the other two processors also request access to the public memory, access is denied to that processor until completion of the memory cycle by the first processor.

The FPGA produces a synchronous ARDY input to the SYS processor, providing support for external ready signals from both public memory accesses and external IO accesses. The FPGA provides synchronous ready signals to the CPC and ICL processors. Processor ready signals are required by the bus arbitration logic, which holds a requesting processor in wait states until the memory access is granted.

In a redundant controller configuration, the FPGA for both controllers have separate onboard bus arbitration logic that permits any of the onboard processors to access its DPM bus. Once access has been granted, the processor can read or write to a selected location in the DPM array without any possible conflict from the redundant controller.

The DPM arbiter logic on the FPGA has a /DPM BSY status signal to indicate when the memory can be accessed. While the /DPM BSY signal is inactive, any of the processors can access DPM by requesting bus access and running a read or write cycle to an address within the DPM address range. No additional bus arbitration or handshaking is required.

4.2.4 RAM Access Control

The RAM access logic on the FPGA permits firmware to coordinate data transfers between the local RAM and the public memory of the controller. When the microprocessor requires access to its RAM, it places the required address on the address bus (LA01 through LA19) and activates the CS6# chip select. After the address signals have stabilized, the microprocessor activates either the WR# or the RD# to enable either a write or a read transfer. The FPGA chip uses the CS6#, BHE#, and BLE# signals to enable high byte, low byte, or full word transfers from local RAM to the microprocessor.

5. Software Detailed Design Specification

Each processor's system software consists of some standard HFC software components and some hardware specific routines. The design specifications of the standard HFC software components are covered in each component's individual detailed design specification. Refer

to Section 5 of the document MS901-000-01 to get a list of component detailed design specifications that are related to the HFC-SBC06 or HFC-DPM06 boards.

This section provides design specification of hardware specific routines or board specific routines, mostly are the initialization processes.

5.1 Initialization Routines

5.1.1 General Initialization Sequence

Each processor on the HFC-SBC06 board goes through a set of initialization sequences before it starts normal operation. These initialization sequences include power up initialization, hardware initialization, processor configuration, and UCP Multitasking Operating System initialization.

5.1.1.1 Reset Initialization and Hardware Initialization

Upon power up or reset, the processor automatically begins processing with the instruction pointer set to the last segment address in high memory (FFFF0_H), which contains the reset initialization routine. This may be flash memory or the PROM, depending on the processor configuration defined by the jumper settings. The reset initialization defines the entry point to the software. Processor software has an EPROM header at the beginning of the file, and the initialization code must jump over this header for continued program execution.

Functional characteristics of the initialization sequence are similar for all processors. The power-up initialization routine configures chip select registers to define the onboard hardware environment such as memory configuration. If the processor is configured to boot from the PROM, then the software will copy the contents of the PROM to the flash memory and start running from the flash memory.

The module proceeds with hardware-specific initialization for that processor and its peripherals. The module performs initial diagnostic tests, such as RAM Read/Write test and EPROM checksum verification. Any fault detected at this stage of operation is fatal and the program execution will terminate after setting fail indications to the LEDs.

After completion of all preliminary hardware initialization and diagnostics, the initialization software provides different paths for the system processor (SYS processor) and subordinate processors (ICL and CPC processors) to perform their individual processor configuration routines.

5.1.1.2 Processor Configuration

The system processor will initialize public memory and define the controller's configuration. The system processor resets the READY code in the public memory early during the Reset Initialization stage. It reads configuration DIP switches settings and application data in its local memory and sets up configuration data for all subordinate processors in a dedicated area in the public memory, well-known to all processors on board. After the system

controller finishes configuration of public memory and becomes SANE, it will set the READY code at the header of the configuration area to indicate completion of the configuration sequence.

The subordinate processors wait till the READY is set in the public memory. After the public memory is ready, the subordinate processors access the public memory and make a local copy of all necessary memory pointers to the public memory and copy other configuration data in their local private memory. Each subordinate processor gets the controller configuration definition in the public memory to build its local copy of all necessary memory pointers. It also goes to its own segment directory in the public memory to get a function code. This function code represents the requested operating mode of the controller by the configuration initialization of the system processor. Two operating modes are supported: Run mode (normal operation), and Self -Test mode.

In the Self-Test mode, the processor performs different kinds of tests based on a request code set up by the DIP switches. The processor stays in the Self-Test mode until the dip switches settings are changed to Run mode. The Run mode is the normal operating mode, and the programs will go to the UCP Multitasking operating system after an OS initialization.

5.1.1.3 UCP Multitasking Operating System Initialization

The UCP Multitasking Operating System is a standard HFC software component. It is mainly a task scheduler that controls the execution of all firmware as well as provides many support functions. During normal operation, the OS component schedules tasks by performing a sequential scan of the defined TCB (task control block) list at regular predefined time intervals, and executes each task in the TCB list if the task's operation status indicates that the task should be executed at that time.

Each processor has unique hardware characteristics and specific functions to fulfill. Various specific initialization routines are required for each processor to set up the hardware and software environment for the operating system to run. These initialization routines are implemented in the processor specific portion of the software. Several initialization routine index tables provide entry to these routines. During the OS initialization, the OS Initialization routine calls these specific initialization routines by going through the initialization routine tables. These initialization routines initialize data structures and add configured tasks to the TCB list for the OS.

Refer to document MS901-000-01, HFC-SBC06-DPM06 Module Design Specification for the list of configured tasks for each processor on board.

After the initialization for TCB is finished, the OS initialization routine loads the processor's mailbox and marks the processor's status flag to Initialization Done and Online in the dedicated area in the public memory.

The system processor keeps on checking the processor status flag for all configured processors to see if all the processors have finished initialization and online. After all the processors have reported Online and Initialization Done, the system processor will set a

SYSTEM_GO flag in the public memory and enters normal operation controlled by the UCP Multitasking operating system. All the subordinate processors, after finding out that the SYSTEM_GO flag is set in the public memory, enters normal operation mode, too.

Refer to document DS001-000-01, OS Component Detailed Design Specification for additional information on the OS Component and its initialization interfaces.

In a redundant controller configuration, the failover mechanism determines which controller is primary and which controller is secondary, and the processors on the primary controller start operating in primary mode and the processors on the secondary controller start operating in secondary mode. Refer to document DS001-000-08, Failover Mechanism Component Detailed Design Specification for additional information.

5.1.2 SYS Processor Application Data Initialization

The SYS processor copies application data contained in its flash memory to the public memory or local RAM. The application data includes the following:

- Equations – Application program for control logics
- I/O Configuration Table – ICL I/O Scan Configuration Table for the ICL Processor
- PIP Definition Table – not used for HFC-SBC06
- RQ Table – DDB Filter Table and Broadcast Table for the CPC Processor
- Block Data – Input Data and Intermediate Calculation Data for CQ4 blocks
- Block Value – Output Value and Quality Word for CQ4 blocks

The Equations, Block Data, and Block Value are used for the SYS processor by the Equation Interpreter Component and CQ4 Component. The I/O Configuration Table is used by the ICL processor to perform I/O scan. The RQ Table is used by the CPC processor for DDB broadcasting and processing of DDB data received from the C-Link.



HF Controls Corporation

HFC-6000 Product Line

HFC-DO8J Board Module Detailed Design Specification

**Eight Channel Relay
Digital Output Board**

DS901-000-03

REV B

January 30, 2009

Author David Briner

Reviewer Pat Thibodeau

Approval Gregory Rochford



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Revision History

Date	Revision	Author	Changes
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Table of Contents

- 1. INTRODUCTION..... 5
- 2. FUNCTIONAL DESCRIPTION..... 5
- 3. HARDWARE DETAILED DESIGN SPECIFICATION 5
 - 3.1 MODULE SPECIFICATION..... 5
 - 3.2 SWITCHES, JUMPERS, AND LED INDICATORS..... 5
 - 3.2.1 *Jumpers*..... 6
 - 3.2.2 *LED Indicators*..... 6
 - 3.3 ONBOARD POWER DISTRIBUTION 6
 - 3.4 DIGITAL DATA OUTPUT PORT..... 6
 - 3.5 HARDWARE CONNECTIONS..... 7
- 4. SOFTWARE DETAILED DESIGN SPECIFICATION..... 8
 - 4.1 I/O SCAN MODULE 8
 - 4.2 PROCESS COMMAND ROUTINE..... 8
 - 4.3 DATA STRUCTURE 8
 - 4.3.1 *I/O Scan Data*..... 8
 - 4.3.2 *Microprocessor Programmable Ports*..... 8
- 5. MODULE IMPLEMENTATION DESCRIPTIONS 9
 - 5.1 HARDWARE SCHEMATICS 9
 - 5.2 HARDWARE COMPONENTS – BILL OF MATERIALS 9
 - 5.3 SOFTWARE SOURCE CODE LISTING..... 9

1. Introduction

The HFC-DO8J assembly is an eight-channel relay digital output board. This assembly operates as a standard DO relay board in an HFC-6000 control system. It receives the images of its digital outputs from an HFC-SBC06 system controller at regular intervals, and uses this data to set the on/off status of each output relay.

The overall architectural design of standard HFC-6000 I/O boards are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification.

This document describes the detailed structure and design of the HFC-DO8J board. The design descriptions of the common software modules of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DO8J board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DO8J board is designed to interface eight field outputs to an HFC-6000 control system. It provides eight relay digital output channels. The board receives the image of its digital outputs from the HFC-SBC06 controller board at regular intervals, and uses this data to set the on/off status of each output relay.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification.

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes
 - Temperature: 0° to 55 C° (operating)
0° to 55 C° (storage)
 - Humidity: 5% to 95%, non-condensing
- Power Requirement
 - External Input Power: +24-vdc, 0.4 A maximum load
- Onboard Clock Rate
 - Microprocessor Clock: 22.1184 MHZ
- Relay contact ratings
 - Up to 30-vdc with 5 A maximum current (resistive load)
 - Up to 250-vac with 5 A maximum current (general use)

3.2 Switches, Jumpers, and LED Indicators

The HFC-DO8J board includes the four card-edge LEDs common to all I/O boards as well as the following components unique to this assembly:

3.2.1 Jumpers

E1-E2 Installed during testing to disable the NMI signal. When the jumper is removed, the D-latch U41-A activates a high NMI signal.

E5-6 Function not currently defined

3.2.2 LED Indicators

DS1-1 Lights when the channel 1 is on

DS1-2 Lights when the channel 2 is on

DS1-3 Lights when the channel 3 is on

DS1-4 Lights when the channel 4 is on

DS2-1 Lights when the channel 5 is on

DS2-2 Lights when the channel 6 is on

DS2-3 Lights when the channel 7 is on

DS2-4 Lights when the channel 8 is on

3.3 ONBOARD POWER DISTRIBUTION

The board receives redundant 24-vdc power feeds from the back plane connector P1. The two power feeds are diode auctioneered, and the resulting 24-vdc output is routed to the following components:

- The onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for logic components on the HFC-DO8J board.
- The combined 24-vdc power line supplies operating power to each of the output relays. A transistor switch in this power line opens whenever the watchdog timer becomes reset.

3.4 Digital Data Output Port

The HFC-DO8J board includes eight relay-controlled DO channels. The ON/OFF image for the eight channels are configured in memory as a single byte of data. During regular scan cycles, the microprocessor copies the DO image from memory to an eight-bit latch, and the resulting output signals from the latch control each DO channel individually.

Each output channel consists of an optocoupler and a mechanical relay with both normally open and normally closed contacts. The optocoupler is configured with a control signal input PTn/ routed from the data output port and the 24-vdc power for the relay. When the digital image for a particular DO channel is ON (PTn/ signal low), the optocoupler becomes forward biased, and 24-vdc power line passes through the optocoupler circuit to the relay coil. While the microprocessor is processing its program code normally, the 24-vdc power line energizes the relay to produce the ON state output. However, if the watchdog timer becomes reset, a transistor switch in the 24-vdc power line opens, removing operating power from all of the relays simultaneously.

3.5 Hardware Connections

The HFC-DO8J board contains board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 back plane. Table 1 lists the pin assignments for connector P1, and Table 2 lists the pin assignments for connector P2. The entries in table 2 distinguish between normally open (NO) and normally closed (NC) contacts. When the relay is deenergized, continuity exists between its NC contact and its common; when it is energized, continuity exists between its NO contact and its common.

Table 1. Connector P1 Pinout Summary

Category	Pin	Mnemonic	Pin	Mnemonic
Power	P1-A1	[]	P1-B1	[]
	P1-C1	[]	P1-A3	[]
	P1-B3	[]	P1-C3	[]
	P1-A5	[]	P1-B5	[]
	P1-C5	[]	P1-A12	[]
	P1-B12	[]	P1-C12	[]
	P1-A14	[]	P1-B14	[]
	P1-C14	[]	P1-A16	[]
	P1-B16	[]	P1-C16	[]
Serial Bus	P1-A9	[]	P1-C9	[]
	P1-B8	[]	P1-A10	[]
	P1-C10	[]	P1-C8	[]
CONTROL	P1-A6	[]	P1-B6	[]
	P1-C6	[]	P1-A7	[]
	P1-B7	[]	P1-C7	[]
	P1-A8	[]		

Table 2. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A32	[]	P2-C32	[]
P2-A31	[]	P2-C31	[]
P2-A30	[]	P2-C30	[]
P2-A29	[]	P2-C29	[]
P2-A28	[]	P2-C28	[]
P2-A27	[]	P2-C27	[]
P2-A26	[]	P2-C26	[]
P2-A25	[]	P2-C25	[]
P2-A24	[]	P2-C24	[]
P2-A23	[]	P2-C23	[]
P2-A22	[]	P2-C22	[]
P2-A21	[]	P2-C21	[]
PS-A20	[]	PS-C20	[]
P2-A19	[]	P2-C19	[]
P2-A18	[]	P2-C18	[]
PS-A17	[]	PS-C17	[]

P2-A16	[]	P2-C16	[]
P2-A15	[]	P2-C15	[]
P2-A14	[]	P2-C14	[]
P2-A13	[]	P2-C13	[]
P2-A12	[]	P2-C12	[]
P2-A11	[]	P2-C11	[]
P2-A10	[]	P2-C10	[]
P2-A9	[]	P2-C9	[]

4. Software Detailed Design Specification

The HFC-DO8J board has a total of eight DO channels that provide both normally open and normally closed contacts. The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DO8J board.

4.1 I/O Scan Module

The HFC-DO8J board firmware has an I/O Scan Module like all other I/O boards, but this module has no function, because the board has no input channels.

4.2 Process Command Routine

For normal update messages, this routine reads the one byte output image for eight channels from the command message and transfers that image to output data latch. For UCP diagnostics messages, the routine executes the common processing functions described in HFC-6000 I/O Board Module Detailed Design Specification.

4.3 Data Structure

This section describes the structure of the DO image and provides a list of the programmable ports used in the software.

4.3.1 I/O Scan Data

The DO8J board has eight DO channels. The eight DO images are organized as a single byte in the poll message received from the SBC06 controller as shown below:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1

4.3.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 3. Programmable Ports Used for DO8J Board

Port	Function	Implementation
P1.2	[]	[]

Port	Function	Implementation
P1.3	[]	[]
P1.6	[]	[]
P1.7	[]	[]
P2.1	[]	[]
P2.3	[]	[]
Port 1 Control Register	[]	[]

5. Module Implementation Descriptions

5.1 Hardware Schematics

The schematic for the HFC-DO8J board is drawing 400458-01.

5.2 Hardware Components – Bill of Materials

The part number of the HFC-DO8J board is 40045701, and its bill of materials is 400457-01.

5.3 Software Source Code Listing

The HFC-DO8J board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- []
- []



HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-DC33 Board

Module Detailed Design Specification

Digital Input/Output Controller Board
Specific for Motor Operated Valve (MOV)

DS901-000-05

Rev D

Effective Date 11/30/07

Author M. Hayes

Reviewer J. Taylor

Approval D. Briner

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Revision History

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Table of Contents

1. INTRODUCTION..... 3

2. FUNCTIONAL DESCRIPTION..... 3

3. HARDWARE DETAILED DESIGN SPECIFICATION 4

 3.1 MODULE SPECIFICATION..... 4

 3.2 CONTROLS, JUMPERS, AND LED INDICATORS 4

 3.3 ONBOARD POWER DISTRIBUTION 6

 3.4 MICROPROCESSOR PERIPHERAL PORTS..... 7

 3.5 INPUT CHANNEL OPERATION 7

 3.6 HARDWARE CONNECTIONS 8

4. SOFTWARE DETAILED DESIGN SPECIFICATION..... 11

 4.1 I/O SCAN MODULE 11

 4.2 PROCESS COMMAND ROUTINE 11

 4.3 DATA STRUCTURE 11

 4.3.1 I/O Scan Data 11

 4.3.2 Microprocessor Programmable Ports 12

5. MODULE IMPLEMENTATION DESCRIPTION..... 13

 5.1 HARDWARE SCHEMATICS 13

 5.2 HARDWARE COMPONENTS – BILL OF MATERIALS 13

 5.3 SOFTWARE SOURCE CODE LISTING..... 13

6. DESIGN SAFETY 13

1. Introduction

The HFC-DC33 is a multi-channel Input/Output (I/O) buffer printed circuit board (PCB). It is used for control, interrogation, and monitoring of field devices in an HFC-6000 control system. The board receives digital messages from its controller, the HFC-SBC06, and sends the image of its 11 digital input (DI) channels.

Descriptions and discussions of the architectural and design descriptions of a standard HFC-6000 I/O board, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-DC33 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DC33 board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DC33 is a special purpose I/O buffer board designed for power plant applications. This buffer is specifically designed to meet the unique control requirements of a dual-coil Motor Operated Valve (MOV) starter. Typical applications include controlling dual coil motor starters while monitoring coil continuity, overloads and the position of the valve.

This board provides a 16-bit 80C188EB microprocessor, 11 DI channels, two 120-vac DO channels, and onboard status sensors. Major functions performed by the microprocessor during normal operation are as follows:

- Responds to data transmissions from the HFC-6000 controller.
- Controls the on/off state of the two DO channels.
- Reads the digital status of the onboard DI channels.
- Reads coil continuity and the presence of ac excitation signals for both DO channels individually.
- Stores the DI image and onboard status in local memory.
- Transmits the digital image of its 11 DI channels back to the HFC-6000 controller.
- Reads seal-in status for each channel.
- Integral transient suppression networks permit reliable operation in high-noise (electrical) environments.
- Optocouplers isolate logic circuits from field wiring.
- Provides direct solid-state control of special dual coil 120-vac output for such field devices as a dual coil Motor Operated Valve (MOV) starter.
- The board includes two banks of memory for an onboard 16-bit Intel 80C188EB microprocessor:
 - High memory provides up to 64K by 8-bits of EPROM for functional program code storage.

- Low memory provides 32K by 8 bits of RAM for temporary storage of message data being processed.
- An onboard dc-to-dc converter provides regulated +5-vdc logic power.
- Provides a seal-in circuit that enables the onboard circuitry to sustain the 120VAC output in the event of controller failure or loss of power to the board.
- An onboard switch enables manual reset of the microprocessor.
- Onboard watchdog timer.
- Provides two output channels for 120-vac, two input channels that monitor continuity of external solenoid coils, and 11 general purpose Digital Inputs (DI).
- Monitors the 48-vdc-interrogation voltage for the 11 general purpose DI channels.
- Onboard LEDs provide visual indication of board status.
- Allows standardization of internal wiring for controlled devices.
- Onboard software provides built-in diagnostics.
- The HFC-DC33 assembly is designed to satisfy seismic category I requirements.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification.

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes
 - Temperature: 0° to 60 C° (operating)
0° to 70 C° (storage)
 - Humidity: 5% to 95%, non-condensing
- Power Requirement Note: AC signals are represented by their rms value.
 - Output Voltage: 60 to 140-vac, 47 to 63 Hz
 - Output Current: 110 amps: inrush, 5 amps continuous
 - External Source Power: 24-vdc at 0.3 A nominal current
 - Interrogation Voltage: 48-vdc
- Onboard Clock Rate
 - Microprocessor Clock: 22.1184 MHZ
- Mounting Requirements
 - The HFC-DC33 mounts vertically in an HFC-6000 card chassis.

3.2 Controls, Jumpers, and LED Indicators

3.2.1 Jumpers

- E1-E2 Installed during calibration to disable the NMI signal. When the jumper is removed, the D-latch U41-A activates a high NMI signal.

3.2.2 Switches

- SW1 Enables manual reset of the 80C188EB microprocessor.
- S3 Permits manual configuration of DI channels 1-11 as isolated or common in any combination
- S1 Enables/Disables the Seal-In circuitry for channel 0 output
- S2 Enables/Disables the Seal-In circuitry for channel 1 output

3.2.3 Reset-able Fuses

- RF1–RF3 Provide overload protection for the +48-vdc interrogation voltage supplied for the 11 DI channels.

3.2.4 LED Indicators

- DS1-1 SYSA/B lights when receive function is enabled for port A; it is out when receive function is enabled for port B.
- DS1-2 TX flashes during serial data transmission over ICL.
- DS1-3 RX flashes during reception of serial data from ICL.
- DS1-4 DMT lights while watchdog timer is being triggered.
- DS2-1 CH0_RDY lights when 120- vac power is available, and CH0 is de-energized and connected to an operational coil
- DS2-2 CH1_RDY lights when 120- vac power is available, and CH1 is de-energized and connected to an operational coil
- DS2-3 PWR PRESENT0 lights when 120-vac power is available for CH0.
- DS2-4 PWR PRESENT1 lights when 120-vac power is available for CH1.
- DS3-1 SEAL IN CH0 lights when seal-in switch for CH0 is enabled and seal-in voltage is present.
- DS3-2 SEAL IN CH1 lights when seal-in switch for CH1 is enabled and seal-in voltage is present.
- DS3-3 CH0 OUT lights when output relay U13 is enabled.
- DS3-4 CH1 OUT lights when output relay U27 is enabled.
- DS4-1 Lights when input channel 1 is on.
- DS4-2 Lights when input channel 2 is on.
- DS4-3 Lights when input channel 3 is on.
- DS4-4 Lights when input channel 4 is on.
- DS5-1 Lights when input channel 5 is on.
- DS5-2 Lights when input channel 6 is on.
- DS5-3 Lights when input channel 7 is on.
- DS5-4 Lights when input channel 8 is on.
- DS6-1 Lights when input channel 9 is on.
- DS6-2 Lights when input channel 10 is on.

- DS6-3 Lights when input channel 11 is on.
DS6-4 No connection, will not illuminate.

3.3 Onboard Power Distribution

The board receives redundant 24-vdc power feeds from the backplane connector P1. The two power feeds are diode auctioneered, and an onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for components on the HFC-DC33 board.

Two +48-vdc interrogation power sources are fed through connector P1 and divided into three branches with each branch supplying power to four channels. A separate reset-able fuse provides overload protection for each branch, and three optocouplers permit the microprocessor to monitor status of the three power lines.

The board receives a nominal 120-vac (60 to 140-vac) power for the two solenoid output channels. When supply power is provided to each channel individually, a bridge rectifier produces a dc status signal that forward biases an optocoupler, enabling the microprocessor to verify power status of each channel. The 120-vac power line is connected to a separate solid state relay for CH0 and CH1. The microprocessor can control these relays independently to enable power output to one or both channels.

120-VAC can be provided to the seal-in circuitry for CH0/CH1 individually. When power is available, a bridge rectifier produces a dc signal that is supplied to a DC-DC converter. If S1 is in the enabled position a 5V signal is available to sustain the output of CH0 in case of controller failure or in loss of 24V power to the board. If S2 is in the enabled position a 5V signal is available to sustain the output of CH1 in case of controller failure or in the loss of 24V power to the board.

3.4 *Microprocessor Peripheral Ports*

The microprocessor controls the following peripheral ports:

- Two digital data input ports
- CH0/CH1 control output port
- Link address data input port
- Redundant serial ports

Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the I/O ports.

The board provides two output latches to control the status of the two 120-vac output channels (CH0 and CH1) and two input buffers to read 15 bits of input data. During an I/O scan, the microprocessor writes the ON/OFF image for CH0 and CH1 to the output latch. The resulting output signals control separate solid state relays. When the microprocessor enables one or both outputs, the corresponding relay becomes enabled and passes the 120-vac power to its output. Similarly, the microprocessor reads input status by running separate read cycles to the two input buffers. The low order byte contains the digital image of PT01/ through PT08/. The high order byte contains the digital image of PT09/ through PT11/, CH0_RDY/, CH1_RDY/, CH0_PWR/, CH1_PWR/, SICH0/, and SICH1/. In addition to the 17 bits of input data, the microprocessor also can read the status of the excitation voltage lines VSEN/, VSEN2/, and VSEN3/. These signals are routed directly to three pins of programmable I/O port P2 of the microprocessor.

The Link address data input port and Redundant serial ports are covered in document DS901-000-02 I/O Board Module Detailed Design Specification.

3.5 *Input Channel Operation*

The HFC-DC33 board contains 20 input channels composed of 11 general purpose DI channels, two coil continuity inputs, two power monitor inputs, two seal-in status inputs, and a separate status monitor for the three excitation voltage lines. Each of the DI channels is composed of a low-pass input filter and optocoupler. The input filter is designed to reject any input signal having a pulse width less than 10 ms in duration, and the optocoupler isolates the internal logic circuitry from the field wiring. When one of these channels receives an active input signal, the optocoupler becomes forward biased and produces a low active output. While any of these outputs is active, the corresponding LED lights. The input circuit for the three VSEN/ input signals is identical, except they do not have an LED indication.

The input circuit for the 120-vac power monitor consists of a bridge rectifier, a low pass filter, and an optocoupler. When the 120-vac power source is present, the rectifier produces a dc signal at the input of the low pass filter network, and the optocoupler activates the CH0_PWR/ status signal.

The circuit for the two coil continuity monitor inputs is similar to that of the power monitor circuit except for input biasing. When the 120-vac output is enabled, the circuit is always

enabled, so the status input is not meaningful. When either output channels are disabled, a small voltage bleeds through the biasing network to the input of the rectifier of that respective channel. If the external coil is present, this small voltage dissipates through the coil and the output from the optocoupler remains disabled. This output is inverted to produce a low active status input (CH0_RDY/ or CH1_RDY/) to the microprocessor. If the external coil is not present or open, the small voltage at the input of the rectifier is sufficient to forward bias the optocoupler, resulting in a high (false) indication for the CH_RDY/ input.

3.6 Hardware Connections

The HFC-DC33 board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Pin assignments for the P1 connector are identical for all I/O boards and can be found in document DS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each DI channel can be configured for either isolated or common mode operation on an individual basis. When operating in common mode, excitation voltage is supplied from this board to the field device being monitored. When operating in isolated mode, external equipment must supply the power to enable or disable the DI indication. Table 2 lists the DIP switch settings and signal assignments required to configure each channel for either mode of operation.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	[]	P2-C1	[]
P2-A2	[]	P2-B2	[]
P2-C2	[]	P2-A3	[]
P2-C3	[]	P2-A4	[]
P2-C4	[]	P2-A5	[]
P2-B5	[]	P2-C5	[]
P2-A6	[]	P2-C6	[]
P2-A7	[]	P2-C7	[]
P2-A8	[]	P2-B8	[]
P2-C8	[]	P2-A9	[]
P2-C9	[]	P2-A10	[]
P2-C10	[]	P2-A11	[]
P2-B11	[]	P2-C11	[]
P2-A12	[]	P2-C12	[]
P2-A13	[]	P2-C13	[]
P2-A14	[]	P2-B14	[]
P2-C14	[]	P2-A15	[]
P2-C15	[]	P2-A16	[]
P2-C16	[]	P2-A17	[]
P2-B17	[]	P2-C17	[]
P2-A18	[]	P2-C18	[]
P2-A19	[]	P2-B19	[]
P2-C19	[]	P2-A20	[]
P2-B20	[]	P2-C20	[]
P2-A21	[]	P2-B21	[]
P2-C21	[]	P2-A22	[]
P2-B22	[]	P2-C22	[]
P2-A23	[]	P2-B23	[]
P2-C23	[]	P2-A24	[]
P2-B24	[]	P2-C24	[]
P2-A25	[]	P2-B25	[]
P2-C25	[]	P2-A26	[]

Table 1 (Continued). Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-B26	[]	P2-C26	[]
P2-A27	[]	P2-B27	[]
P2-C27	[]	P2-A28	[]
P2-B28	[]	P2-C28	[]
P2-A29	[]	P2-B29	[]
P2-C29	[]	P2-A30	[]
P2-B30	[]	P2-C30	[]
P2-A31	[]	P2-B31	[]
P2-C31	[]	P2-A32	[]
P2-B32	[]	P2-C32	[]

Table 2. Input Connection Summary

Channel No.	Type	Positive	Negative	Dipswitch
1	[]	[]	[]	[]
	[]	[]	[]	[]
2	[]	[]	[]	[]
	[]	[]	[]	[]
3	[]	[]	[]	[]
	[]	[]	[]	[]
4	[]	[]	[]	[]
	[]	[]	[]	[]
5	[]	[]	[]	[]
	[]	[]	[]	[]
6	[]	[]	[]	[]
	[]	[]	[]	[]
7	[]	[]	[]	[]
	[]	[]	[]	[]
8	[]	[]	[]	[]
	[]	[]	[]	[]
9	[]	[]	[]	[]
	[]	[]	[]	[]
10	[]	[]	[]	[]
	[]	[]	[]	[]
11	[]	[]	[]	[]
	[]	[]	[]	[]

4. Software Detailed Design Specification

The HFC-DC33 board monitors a total of 20 DI channels. The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DC33 board.

4.1 I/O Scan Module

This I/O Scan Module performs the I/O scan for 11 standard DI channels, two coil continuity status inputs, two power monitor status inputs, and two seal in status inputs. It takes samples to read the status of three interrogation voltages and two bytes of input data during each scan. The loss of any interrogation voltage means that four or more DI images may not be valid, so the module will not update DI images with new readings if no interrogation voltage is present. If any interrogation voltage is false, the Interrogation Voltage Off error bit in the diagnostic byte will be set to indicate a hardware fault. This information will be reported to the controller in the response to a diagnostic request message.

Normally the DI images will be transferred to the Scan Working Buffer only when at least one of three interrogation voltages is present. However, to avoid missing information on the controller side, an interrogation voltage failure counter is used in the I/O scan process. This counter is incremented during each scan cycle where all interrogation voltages are missing. When the accumulated count exceeds a predefined limit, the DI images in the Scan Working Buffer will be updated and reported to the controller, even if no interrogation voltage is present. This counter will remain reset as long as any interrogation voltage line is present.

If a DO channel is set ON, the corresponding coil continuity status input is not meaningful. So the coil continuity status will be reported as "TRUE" to prevent spurious error indications. Only when the corresponding DO channel is not ON will the actual coil continuity status be reported back to the HFC-SBC06 controller.

4.2 Process Command routine

For normal update messages, this routine reads the one byte output image for two output channels from the command message and transfers that image to output data latch. UCP diagnostics messages are processed as described in HFC-6000 I/O Board Module Detailed Design Specification DS002-000-02.

4.3 Data Structure

This section describes the structure of the I/O data images and provides a list of the programmable ports controlled by the software.

4.3.1 I/O Scan Data

The HFC-DC33 board has two DO channels and 11 DI channels. The data field of poll messages received from the HFC-SBC06 controller has the following structure:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PT2	PT1

The data field of the response message to the HFC-SBC06 Controller has the following structure:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1
2	Power Source 1	Power Source 0	Coil 1 Continuity	Coil 0 Continuity	Seal In CH 0	PT11	PT10	PT9

4.3.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 3. Programmable Ports Used for HFC-DC33 Board

Port	Description	Implementation
P1.0	[]	[]
P1.1	[]	[]
P1.2	[]	[]
P1.3	[]	[]
P1.4	[]	[]
P1.5	[]	[]
P1.7	[]	[]
P2.1	[]	[]
P2.3	[]	[]
P2.4	[]	[]
P2.5		
P2.6		
Port 1 Control Register	[]	[]

4.3.3 Failsafe Function

The hardware assembly includes an onboard seal-in circuit. When the seal-in input is configured and the onboard latch enable switch (S1) is closed, the seal-in circuit latches in the true state of the DO signal. The purpose of this circuit is to maintain the energized state of the DO signal even if power is lost from the control system. (The power required to maintain this state must be supplied from the external field equipment.)

Seal-in status is included with the DI image read by the microprocessor during each scan cycle. In the event of ICL timeout, the microprocessor checks seal-in status. If seal-in status is true, then the microprocessor keeps the DO channel energized. If seal in status is false (either because the DO channel is off or the seal-in function is not configured), the microprocessor clears the DO latch for failsafe.

5. Module Implementation Description

5.1 Hardware Schematics

The schematic for the HFC-DC33 board is drawing 400463-01.

5.2 Hardware Components – Bill of Materials

The part number of the HFC-DC33 board is 40046201, and its bill of materials is 400462-01 and 400462-81.

5.3 Software Source Code Listing

The HFC-DC33 board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- []
- []

6. Design Safety

Refer to MS901-000-02 for a discussion of design safety considerations for HFC-6000 I/O modules.



HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-DC34 Board

Module Detailed Design Specification

Digital Input/Output Controller Board
Specific for Electronically Operated Breakers (EOB)

DS901-000-06

Rev D

Effective Date	<u>11/30/07</u>
Author	<u>M. Hayes</u>
Reviewer	<u>J. Taylor</u>
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Table of Contents

1. INTRODUCTION..... 3

2. FUNCTIONAL DESCRIPTION..... 3

3. HARDWARE DETAILED DESIGN SPECIFICATION 4

 3.1 MODULE SPECIFICATION..... 4

 3.2 CONTROLS, JUMPERS, AND LED INDICATORS..... 4

 3.3 ONBOARD POWER DISTRIBUTION 6

 3.4 MICROPROCESSOR PERIPHERAL PORTS..... 6

 3.5 INPUT CHANNEL OPERATION 7

 3.6 HARDWARE CONNECTIONS..... 8

4. SOFTWARE DETAILED DESIGN SPECIFICATION..... 10

 4.1 I/O SCAN MODULE 10

 4.2 PROCESS COMMAND ROUTINE 11

 4.3 DATA STRUCTURE 11

 4.3.1 I/O Scan Data 11

 4.3.2 Microprocessor Programmable Ports 11

5. MODULE IMPLEMENTATION DESCRIPTION..... 13

 5.1 HARDWARE SCHEMATICS 13

 5.2 HARDWARE COMPONENTS – BILL OF MATERIALS 13

 5.3 SOFTWARE SOURCE CODE LISTING..... 13

6. DESIGN SAFETY 13

1. Introduction

The HFC-DC34 is a multi-channel Input/Output (I/O) buffer printed circuit board (PCB). It is used for control, interrogation, and monitoring of field devices in an HFC-6000 control system. Typical applications include monitoring Electrically Operated Breakers (EOB) for overloads. The board receives digital messages from its controller, the HFC-SBC06, and sends the image of its 11 digital input (DI) channels.

Descriptions and discussions of the architecture and design descriptions of a standard HFC-6000 I/O board, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-DC34 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DC34 board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DC34 is a special purpose I/O buffer board designed for power plant applications. This board is designed to provide the specific combination of digital I/O channels needed to control motor starter or switchgear field equipment.

This board provides a 16-bit 80C188EB microprocessor, 11 DI channels, two 125-vdc DO channels, and onboard status sensors. Major functions performed by the microprocessor during normal operation are as follows:

- Responds to data transmissions from the HFC-6000 controller.
- Controls the on/off state of the two output channels.
- Reads the digital status of the onboard DI channels.
- Reads coil continuity and the presence of dc excitation signals for each channel individually
- Stores the DI image and onboard status in local memory.
- Transmits the digital image of its 11 DI channels back to the HFC-6000 controller.
- Reads seal-in status for each channel
- Integral transient suppression networks permit reliable operation in high-noise (electrical) environments.
- Provides input filters and opto-couplers to isolate logic circuits from field wiring.
- Provides direct solid-state control of two 125-vdc outputs for such field devices as an Electrically Operated Breaker (EOB).
- The board includes two banks of memory for an onboard 16-bit Intel 80C188EB microprocessor:
 - High memory provides up to 64K by 8-bits of EPROM for functional program code storage.

- Low memory provides 32K by 8-bits of RAM for temporary storage of message data being processed.
- An onboard dc-to-dc converter provides regulated +5-vdc logic power.
- Provides two seal-in circuits that enable the onboard circuitry to maintain the two 125-VDC output in the event of controller failure.
- An onboard switch enables manual reset of the microprocessor.
- Onboard watchdog timer.
- Provides 48-vdc interrogation voltage for the DI channels.
- Monitors the 48-vdc power sources.
- Onboard LEDs provide visual indication of board status.
- Allows standardization of internal wiring for controlled devices.
- The HFC-DC34 assembly is designed to satisfy seismic category I requirements.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification.

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes
 - Temperature: 0° to 60 C° (operating)
0° to 70 C° (storage)
 - Humidity: 5% to 95%, non-condensing
- Power Requirement
 - Output Voltage: 100 to 150-vdc
 - Output Current: 25 amps: inrush
10 amps, 250ms repeated once per 5 minutes
2 amps continuous
 - External Source Power: 24-vdc at 0.3 A nominal current
 - Interrogation Voltage: 48-vdc
- Onboard Clock Rate 22.1184 MHZ
- Mounting Requirements
 - The HFC-DC34 mounts vertically in an HFC-6000 card chassis.

3.2 Controls, Jumpers, and LED Indicators

3.2.1 Jumpers

E1-E2 Installed during calibration to disable the NMI signal. When the jumper is removed, the D-latch U41-A activates a high NMI signal.

3.2.2 Switches

SW1	Enables manual reset of the 80C188EB microprocessor.
S1	Permits manual configuration of DI channels 1-11 as isolated or common in any combination
S3	Enables/Disables the Seal In mode for CH0
S4	Enables/Disables the Seal In mode for CH1

3.2.3 Reset-able Fuses

RF1–RF3	Provide overload protection for the +48-vdc interrogation voltage supplied for the 11 DI channels.
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3.2.4 LED Indicators

DS1-1	SYSA/B lights when receive function is enabled for port A; it is out when receive function is enabled for port B.
DS1-2	TX flashes during serial data transmission over ICL.
DS1-3	RX flashes during reception of serial data from ICL.
DS1-4	DMT lights while watchdog timer is being triggered.
DS2-1	CH0 RDY lights when 125- vdc power is available, coil test mode is enabled, and the external coil on CH0 is operational.
DS2-2	CH1 RDY lights when 125- vdc power is available, coil test mode is enabled, and the external coil on CH1 is operational.
DS2-3	PWR PRESENT0 lights when 125-vdc power is available for CH0.
DS2-4	PWR PRESENT1 lights when 125-vdc power is available for CH1.
DS3-1	SEAL IN CH0 lights when seal in switch for CH0 is enabled and seal-in voltage is present.
DS3-2	SEAL IN CH1 lights when seal in switch for CH1 is enabled and seal-in voltage is present.
DS3-3	CH0 OUT lights when the CH0 output is enabled.
DS3-4	CH1 OUT lights when the CH1 output is enabled.
DS4-1	Lights when input channel 1 is on.
DS4-2	Lights when input channel 2 is on.
DS4-3	Lights when input channel 3 is on.
DS4-4	Lights when input channel 4 is on.
DS5-1	Lights when input channel 5 is on.
DS5-2	Lights when input channel 6 is on.
DS5-3	Lights when input channel 7 is on.
DS5-4	Lights when input channel 8 is on.
DS6-1	Lights when input channel 9 is on.

DS6-2	Lights when input channel 10 is on.
DS6-3	Lights when input channel 11 is on.
DS6-4	No connection, will not illuminate.

3.3 Onboard Power Distribution

The board receives redundant 24-vdc power feeds from the backplane connector P1. The two power feeds are diode auctioneered, and an onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for components on the HFC-DC34 board.

Two +48-vdc interrogation power sources are fed through connector P1 and divided into three branches with each branch supplying power to four channels. A separate reset-able fuse provides overload protection for each branch, and three opto-couplers permit the microprocessor to monitor status of the three power lines.

The board receives a nominal 125-vdc (100 to 150-vdc) power for the two solenoid output channels. When supply power is available, an input status signal forward biases a corresponding optocoupler, enabling the microprocessor to verify power status of each channel individually. The 125-vdc power line is connected to a separate FET switch for CH0 and CH1. The microprocessor can control these FETs independently to enable power output on one or both channels.

125-VDC can be provided to the seal-in circuitry for CH0/CH1. When power is available, a linear regulator converts 125-VDC to 48-VDC, then a DC-DC converter converts 48VDC to 5VDC. If S3 is in the enabled position and the 125-VDC is supplied to SEAL IN CH0, then a 5V signal is available to sustain the output of CH0 in case of controller failure or in loss of 24V power to the board. If S4 is in the enabled position and the 125-VDC is supplied to SEAL IN CH1, then a 5V signal is available to sustain the output of CH1 in case of controller failure or in loss of 24V power to the board.

3.4 Microprocessor Peripheral Ports

The microprocessor controls the following peripheral ports:

- Two digital data input ports
- CH0/CH1 control output port
- Link address data input port
- Redundant serial ports

Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the I/O ports.

The board provides one output latch to control the status of the two 125-vdc digital output channels (CH0_OUT/ and CH1_OUT/) and two coil monitoring circuits. When one of the DO channels is set on, the corresponding CHx_OUT/ signal from the latch forward biases a solid-state switch, passing 125-vdc power from input source to the output port for that channel. When a DO channel is set off, the microprocessor can activate the coil monitoring circuit. In order for the circuit to produce meaningful results, the onboard software prevents the DO channel and the coil monitoring circuit from being enabled at the same time.

The microprocessor reads input status by running separate read cycles to the two input buffers. The low order byte contains the digital image of PT01/ through PT08/. The high order byte contains the digital image of PT09/ through PT11/, CH0_RDY/, CH1_RDY/, CH0_PWR/, CH1_PWR/, SICH0/, AND SICH1/. In addition to the 17 bits of input data, the microprocessor also can read the status of the excitation voltage lines VSEN/, VSEN2/, and VSEN3/. These signals are routed directly to three pins of programmable I/O port P2 of the microprocessor.

The Link address data input port and Redundant serial ports are covered in document DS901-000-02 I/O Board Module Detailed Design Specification.

3.5 Input Channel Operation

The HFC-DC34 board contains 20 input channels composed of 11 general purpose DI channels, two coil continuity inputs, two power monitor inputs, two seal-in status inputs, and a separate status monitor for the three excitation voltage lines. Each of the DI channels is composed of a low-pass input filter and an optocoupler. The input filter is designed to reject any input signal having a pulse width less than 10 ms in duration, and the optocoupler isolates the internal logic circuitry from the field wiring. When one of these channels receives an active input signal, the optocoupler becomes forward biased and produces a low active output. While any of these outputs is active, the corresponding LED will light. The input circuit for the three VSEN/ input signals is identical, except they do not have an LED indication.

Each of the two input circuits for the 125-vdc power monitor consists of a low pass filter, and an optocoupler. When the 125-vdc power source is present for one or both input channels, the dc signal at the input of the low pass filter network activates a corresponding optocoupler to produce a low active output (CH0_PWR/ and/or CH1_PWR/). If either the CH0_PWR/ or the CH1_PWR/ signal is active, the PWR PRESENT0 LED or PWR PRESENT1 LED lights respectively.

The coil monitor circuit consists of a voltage divider connected to the 125-vdc power source, a low pass filter, and two optocouplers. When the microprocessor deactivates the CHx_OUT/ signal, one optocoupler passes the 125-vdc power source to the input of the voltage divider. This circuit then applies a significantly reduced voltage across the ports of the DO channel. If an external coil is present, a small current passes through the voltage divider network to forward bias the monitoring optocoupler, which then produces a low active CHx_RDY/ status output. If the external circuit is open, no current flows through the circuit, and the monitoring optocoupler remains cut off. If either the CH0_RDY/ or the CH1_RDY/ signal is active, the CH0/1 RDY LED lights.

The seal-in status consists of 125VDC being regulated to 5VDC. The availability of the 5VDC is read by the onboard microprocessor for each of the two channels. When the seal-in circuitry is active (true) the onboard microprocessor will not initiate failsafe for the corresponding DO channel in the event of ICL timeout.

3.6 Hardware Connections

The HFC-DC34 board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Pin assignments for the P1 connector are identical for all I/O boards and can be found in document DS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each DI channel can be configured for either isolated or common mode operation on an individual basis. When operating in common mode, excitation voltage is supplied from this board to the field device being monitored. When operating in isolated mode, external equipment must supply the power to enable or disable the DI input circuit. Table 2 lists the DIP switch settings and signal assignments required to configure each channel for either mode of operation.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	[]	P2-C1	[]
P2-A2	[]	P2-B2	[]
P2-C2	[]	P2-A3	[]
P2-C3	[]	P2-A4	[]
P2-C4	[]	P2-A5	[]
P2-B5	[]	P2-C5	[]
P2-A6	[]	P2-C6	[]
P2-A7	[]	P2-C7	[]
P2-A8	[]	P2-B8	[]

Table 1(Continued). Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-C8	[]	P2-A9	[]
P2-C9	[]	P2-A10	[]
P2-C10	[]	P2-A11	[]
P2-B11	[]	P2-C11	[]
P2-A12	[]	P2-C12	[]
P2-A13	[]	P2-C13	[]
P2-A14	[]	P2-B14	[]
P2-C14	[]	P2-A15	[]
P2-C15	[]	P2-A16	[]
P2-C16	[]	P2-A17	[]
P2-B17	[]	P2-C17	[]
P2-A18	[]	P2-C18	[]
P2-A23	[]	P2-B23	[]
P2-C23	[]	P2-A24	[]
P2-B24	[]	P2-C24	[]
P2-A25	[]	P2-B25	[]
P2-C25	[]	P2-A26	[]
P2-B26	[]	P2-C26	[]
P2-A27	[]	P2-B27	[]
P2-C27	[]	P2-A28	[]
P2-B28	[]	P2-C28	[]
P2-A29	[]	P2-B29	[]
P2-C29	[]	P2-A30	[]
P2-B30	[]	P2-C30	[]
P2-A31	[]	P2-B31	[]
P2-C31	[]	P2-A32	[]
P2-B32	[]	P2-C32	[]

Table 2. Input Connection Summary

Channel No.	Type	Positive	Negative	Dipswitch
1	[]	[]	[]	[]
	[]	[]	[]	[]
2	[]	[]	[]	[]
	[]	[]	[]	[]
3	[]	[]	[]	[]
	[]	[]	[]	[]
4	[]	[]	[]	[]
	[]	[]	[]	[]
5	[]	[]	[]	[]
	[]	[]	[]	[]
6	[]	[]	[]	[]
	[]	[]	[]	[]
7	[]	[]	[]	[]
	[]	[]	[]	[]
8	[]	[]	[]	[]
	[]	[]	[]	[]
9	[]	[]	[]	[]
	[]	[]	[]	[]
10	[]	[]	[]	[]
	[]	[]	[]	[]
11	[]	[]	[]	[]
	[]	[]	[]	[]

4. Software Detailed Design Specification

The HFC-DC34 board monitors a total of 20 DI channels. The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DC34 board.

4.1 I/O Scan Module

This I/O Scan Module performs the I/O scan for 11 standard DI channels, two coil continuity status inputs, 2 power monitor status inputs, and two seal in status inputs. It reads the status of three interrogation voltages and the two bytes of input data during each scan. The loss of any interrogation voltages means that four or more of the DI images may not be valid, so the module will not update DI images with new readings if no interrogation voltage is present. If any interrogation voltage input is false, the Interrogation Voltage Off error bit in the diagnostic byte will be set to indicate a hardware fault. This information will be reported to the controller in the response to a diagnostic request message.

Normally, the DI images are transferred to the Scan Working Buffer when at least one of three interrogation voltages is present. However, to avoid missing information on the controller side, an interrogation voltage failure counter is used in the I/O scan process. This counter is incremented during each scan cycle where all interrogation voltages are missing.

When the accumulated count exceeds a predefined limit, the DI images in the Scan Working Buffer will be updated and reported to the controller even if no interrogation voltage is present. This counter will remain reset as long as any interrogation voltage line is present.

If a DO channel is set ON, the corresponding coil continuity status input is not meaningful. So the coil continuity status will be reported as "TRUE" to prevent spurious error indications. Only when the corresponding DO channel is not ON will the actual coil continuity status be reported back to the HFC-SBC06 controller.

4.2 Process Command routine

For normal update messages, this routine reads the one byte output image for two output channels from command message and transfers that image to output data latch. UCP diagnostics messages are processed as described in HFC-6000 I/O Board Module Detailed Design Specification DS002-000-92.

4.3 Data Structure

This section describes the structure of the I/O data images and provides a list of the programmable ports controlled by the software.

4.3.1 I/O Scan Data

The HFC-DC34 board has 2 DO channels and 11 DI channels. The data field of poll messages received from the HFC-SBC06 controller has the following structure:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	CH1_OUT/	CH0_OUT/

The data field of the response message to the HFC-SBC06 Controller has the following structure:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1
2	Power Source 1	Power Source 0	Coil 1 Continuity	Coil 0 Continuity	Seal In CH0	PT11	PT10	PT9

4.3.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 3. Programmable Ports Used for HFC-DC34 Board

Port	Description	Implementation
P1.0	[]	[]
P1.1	[]	[]
P1.2	[]	[]
P1.3	[]	[]
P1.4	[]	[]
P1.5	[]	[]
P1.7	[]	[]
P2.1	[]	[]
P2.3	[]	[]
P2.4	[]	[]
P2.5		
P2.6		
Port 1 Control Register	[]	[]

4.3.3 Failsafe Function

The hardware assembly includes an onboard seal-in circuit. When the seal-in input is configured and the onboard latch enable switch (S1) is closed, the seal-in circuit latches in the true state of the DO signal. The purpose of this circuit is to maintain the energized state of the DO signal even if power is lost from the control system. (The power required to maintain this state must be supplied from the external field equipment.)

Seal-in status is included with the DI image read by the microprocessor during each scan cycle. In the event of ICL timeout, the microprocessor checks seal-in status. If seal-in status is true, then the microprocessor keeps the DO channel energized. If seal in status is false (either because the DO channel is off or the seal-in function is not configured), the microprocessor clears the DO latch for failsafe.

5. Module Implementation Description

5.1 Hardware Schematics

The schematic for the HFC-DC34 board is drawing 400468-01.

5.2 Hardware Components – Bill of Materials

The part number of the HFC-DC34 board is 40046701, and the bills of material are 400467-01 and 400467-81.

5.3 Software Source Code Listing

The HFC-DC34 board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- []
- []

6. Design Safety

Refer to MS901-000-02 for a discussion of design safety considerations for the HFC-6000 I/O Modules.

HFC Non-proprietary



HF Controls

HF Controls Corporation

HFC-6000 Product Line

**HFC-AI16 Board
Detailed Design Specification**

Sixteen Channel Analog Input Board

DS901-000-07

Rev D

Effective Date 2/2/2009

Author Gregory Rochford

Reviewer Pat Thibodeau

Approval David Briner

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Revision History

Date	Revision	Author	Changes
11/14/03	0	D. Bynum	Initial
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2/13/06	B0	E. Schirmer	SCR 1361
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3/2/07	C	J Taylor	SCR1766; restored software coverage to Rev B
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Table of Contents

Section	Title	Page
1.	INTRODUCTION.....	4
1.1	REFERENCES	4
1.2	SPECIAL TERMS AND ABBREVIATIONS.....	4
2.0	SPECIFICATIONS.....	4
3.0	CONTROLS AND INDICATORS.....	5
4.0	FUNCTIONAL DESCRIPTION.....	6
4.1	OVERVIEW	6
4.2	ONBOARD POWER DISTRIBUTION.....	6
4.3	RESET/INITIALIZATION	6
4.4	MEMORY STRUCTURE.....	7
4.5	INTERRUPT PROCESSING	8
4.6	MICROPROCESSOR PERIPHERAL PORTS.....	8
4.6.1	Analog Input (AI) control output port	8
4.6.2	A/D data input port.....	9
4.7	I/O PORTS	10
5.0	HARDWARE CONNECTIONS.....	10
6.	SOFTWARE DETAILED DESIGN SPECIFICATION.....	10
6.1	BOARD INFORMATION.....	10
6.2	ANALOG INPUT SCAN ALGORITHM	13
6.2.1	Read Channel Raw Value.....	13
6.2.2	Calibration Test Routine	13

6.2.3	<i>AI Algorithm</i>	14
6.3	SINGLE CHANNEL ADJUSTMENT ALGORITHM.....	15
6.4	HFC-AI16F-BOARD SPECIFIC MODULES.....	16
6.4.1	<i>I/O Scan Module</i>	16
6.4.2	<i>Process Command routine</i>	16
6.5	DATA STRUCTURE	16
6.5.1	<i>Scan Data</i>	16
7.	MODULE IMPLEMENTATION DESCRIPTION.....	17
7.1	HARDWARE SCHEMATICS	17
7.2	HARDWARE COMPONENTS – BILL OF MATERIALS	17
7.3	SOFTWARE SOURCE CODE LISTING.....	17
8.	DESIGN SAFETY	17

List of Tables

Section	Title	Page
Table 1.	Connector P2 Pinout Summary.....	11
Table 2.	Input Connection Summary.....	12

1. Introduction

The HFC-AI16 assembly is a 16-channel analog input board. This assembly operates as a standard AI board in an HFC-6000 control system. It receives analog input signals from field equipment at the plant and performs A/D conversion for each channel at regular intervals. The HFC-SBC06 controller initiates communication with a configured HFC-AI16 board during its regular scan cycles, and the HFC-AI16 board returns the current digital image for all input channels.

Descriptions and discussions of the architectural and design descriptions of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-AI16 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-AI16 board will be presented using design, implementation, and configuration information.

1.1 References

700901-06	HFC-6000 I/O Card Requirements Specification
MS901-000-02	HFC-6000 Product Line, I/O Module Design Specification
DS901-000-02	HFC-6000 Product Line, I/O Module Detailed Design Specification
40043301	HFC-AI16 Schematic
WI-ENG-106	Development of Hardware Design Specification

1.2 Special Terms and Abbreviations

I/O	Input/Output
LSB	Least Significant Bit
RAM	Random Access Memory
AI16F	0-20mA 16 Channel Analog Input
AI16E	0-10V 16 Channel Analog Input
AI16R	0-5V 16 Channel Analog Input
A/D	Analog to Digital Converter

2.0 Specifications

- Environmental Extremes
 - Temperature: 0° to 55° C (operating)
 0° to 70° C (storage)
 - Relative Humidity: 5% to 95%, non-condensing
- Power Requirements

External Power Supply: +24 vdc, 0.3 A maximum load.
Excitation voltage: +24 vdc with resettable fuse for each pair of channels and 0.5 A fuse for the combined load

- Onboard Clock Rate
Microprocessor Clock: 22.1184 MHz

- Input Signal Requirements
Signal:

AI16F 249Ω input resistor accepts 0 to 20mA.
AI16E 1 MΩ input resistor accepts 0 to 10V.
AI16R 1 MΩ input resistor accepts 0-5V.

Accuracy: Designed to read input signals accurately to .1% of full scale.

3.0 Controls and Indicators

The firmware determines the overall operating characteristics of the hardware on the HFC-AI16 board. The HFC-AI16 board includes the set of four LEDs common to all I/O board types (DS901-000-02). In addition, the board also includes six jumpers, two potentiometers, three switches, and nine fuses. The function of these components is as follows:

Jumpers

- W36 Installed to supply 24-vdc excitation power for common AI channels.
- W37 Installed to make the analog return and digital return electrical common.
- E1-E2 Installed during calibration to disable both the NMI signal. When this jumper is removed, the D-latch U41-A activates a high NMI signal.
- E5-E6 Not currently defined.

Potentiometers

- R97 Enables the manual adjustment of the ADC offset voltage.
- R98 Enables the manual adjustment of the ADC gain.

Switches

- SW1 Enables user to reset the 80C188EB microprocessor.
- S1 8-position DIP switch enables the user to configure channels 1 through 8 for either common or isolated mode operation (SW ON = COMMON) in any combination.
- S2 8-position DIP switch enables the user configure channels 8 through 16 for either common or isolated mode operation (SW ON = COMMON) in any combination.

Fuses

- F1, Provide separate overload protection on the 24-vdc excitation voltage line for
F2, each pair of input channels
F4-F9
- F3 Provides common overload protection for the excitation power source supplied to
all 16 input channels.

4.0 Functional Description

The HFC-AI16 AI board is controlled by an onboard 80C188EB microprocessor and provides an interface for up to 16 analog field inputs for an HFC-6000 control system. The analog inputs are converted into digital images and stored in onboard RAM. The system controller accesses these values from RAM by sending the appropriate message to the HFC-AI16 board.

4.1 Overview

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification. The major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Performs reset and initialization of onboard hardware.
- Responds to data transmissions from the HFC-6000 controller.
- Samples the analog data from each of the 16 AI channels.
- Performs the Analog-to-Digital (A/D) conversion of field inputs.
- Stores the digital image for each channel in onboard memory.

4.2 Onboard Power Distribution

The board receives redundant 24-vdc power feeds from the backplane connector J1. The two power feeds are diode auctioneered and routed to the following components:

- An onboard voltage regulator converts the 24-vdc source power to +5-vdc power required for logic components on the HFC-AI16 board.
- An onboard voltage regulator (PS1) converts the 24-vdc source power to ± 15 -vdc non-isolated power. This supplies operating power for the non-isolated analog circuitry.
- An onboard voltage regulator (PS2) converts the 24-vdc source power to ± 15 -vdc for the isolated analog circuitry.

When jumper W36 is installed, a 24-vdc power line is divided into 8 branches. Each branch includes a separate reset-able line fuse and supplies excitation power for two AI channels.

4.3 Reset/Initialization

The Micro Monitor chip monitors the voltage level of the +5-vdc power rail, the state of the onboard reset switch (SW1), and normal operation of the microprocessor clock. When

power is first applied to the board, the low state of the logic power rail causes the Micro Monitor chip to hold a /RESIN signal at a low level. After logic power increases above 4.5-vdc, the Micro Monitor chip keeps the /RESIN signal low for an additional 350 ms to ensure that all transient signals have dissipated before the microprocessor begins operation. During subsequent operation, the chip monitors its inputs for actuation of the RESET switch (SW1) or a significant drop in the voltage level of the onboard logic power rail.

When the microprocessor begins running, CLKOUT pulses are routed from the microprocessor to the Micro Monitor chip. If the microprocessor clock stops running for a period of 50 ms, the Micro Monitor chip automatically activates the /RESIN signal to reset the microprocessor. If the operator presses the SW1 RESET switch, circuitry on the board causes the Micro Monitor chip to activate the /RESIN signal. When the operator releases the RESET switch, the /RESIN signal remains low for an additional 350 ms before permitting the microprocessor to resume normal operation.

Watchdog Timer Functions

The HFC-AI16 board is equipped with a watchdog timer circuit composed of a one-shot (U40-A) and a D-latch (U41-A). During initial power-up or manual reset, the output from the Micro Monitor chip holds both the one-shot and D-latch in their reset state. When the /RESIN signal assumes a high state, the one-shot can respond to outputs from the microprocessor.

Programmable output from port P2.1 of the microprocessor is routed to the negative trigger input of the one-shot. During normal operation of the onboard software, the microprocessor must produce a low output pulse from this port once every 950 ms to keep the one-shot at a triggered state. While the one-shot remains triggered, the negative output keeps LED DS5-1 lit, and the positive output enables the transmission function of the redundant serial ports. If the microprocessor stops normally processing its software, the one-shot times out after a period of 950 ms. The resulting transition of the low active output clocks the D-latch, and the low state of the high active output disables transmission over the serial links.

If jumper E1-E2 is not installed, the U41-A D-latch activates a high NMI signal and low TIMEOUTA/ and TIMEOUTB/ signals. The two TIMEOUT/ signals can be used to notify external equipment that this board is not operating, and the NMI signal halts microprocessor operation. As a result, the operator must actuate the RESET switch to initiate hardware reset of the board. If the E1-E2 jumper is installed, the transition of the watchdog timer disables transmission over the serial links, but the NMI signal remains disabled.

4.4 Memory Structure

Memory on the HFC-AI16 board is organized into two banks of private memory for the microprocessor. Private memory for the 80C188EB microprocessor consists of one bank of EPROM and one bank of RAM. The private memory banks are connected directly to the address and data lines of the microprocessor.

80C188EB Microprocessor Upper Memory

The upper bank of local memory for the 80C188EB microprocessor provides up to 64K by 8 bits of EPROM storage ending with the address of FFFFF_H. Access to memory in this bank is

enabled by the UCS/ chip-select and RD/ signals from the microprocessor. When the low active RESIN/ signal returns to a high level following power-up, the internal address pointer of the microprocessor begins operation by accessing the data stored at address FFFF0_H in upper memory. As a result, the first instruction of the initialization code must be located at this address.

80C188EB Microprocessor Low Memory

The low memory bank provides up to 32K by 8 bits of static RAM for general data storage. Low memory begins at address 00000_H, and access to the memory in this range is enabled by the LCS/ signal. This portion of memory contains the data structures and temporary storage buffers defined by the functional code in upper memory.

4.5 Interrupt Processing

The 80C188EB microprocessor provides a modular core for processing interrupts and exception conditions. The chip architecture includes a port for an NMI input, ports for five maskable interrupts (INT0 through INT4), and a variety of internally generated interrupts. For this specific board four of the maskable interrupt inputs (INT0 through INT3) are disabled. The maskable interrupt input INT4 is configured to detect completion of the A/D cycle. By using INT4 in this way, the microprocessor can efficiently read the converted analog data at the appropriate time. The watchdog timer controls the NMI input.

4.6 Microprocessor Peripheral Ports

The microprocessor controls the following peripheral ports:

- Analog Input (AI) control output port
- A/D data input port
- Link address data input port
- Redundant serial port

The link address input port, and the redundant serial port are common to all I/O board types, and are described in document DS901-000-02. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the three I/O ports

4.6.1 Analog Input (AI) control output port

The interface between the microprocessor and the analog section of the board consists of a 16-bit A/D converter, an 8-bit latch, and two BCD-to-decimal decoders. Bits 4 through 7 (formatted as AD0 through AD3) of the data transferred to the latch contain a 4-bit code for the AI channel to be read, and bit 1 (AD6) controls the R/C output to the A/D converter. The 4-bit channel selection code is routed from the output ports of the latch to the input of both BCD-to-decimal decoders via the 8-bit buffer. The buffer has two output enable ports controlled by separate signals from the microprocessor. OE1 is controlled by the output from P1.6, and OE2 is controlled by the output from P1.5. When the microprocessor activates the output from P1.6, the channel select code controls selection of PT00 through PT07; when the output from P1.5 is activated, the channel select code controls selection of PT08 through PT17. PT16 and PT17 control selection of zero and span voltage inputs for a calibration

cycle. The active output signal then forward biases the optocoupler for the selected channel, and it passes the analog input from the field device to an input amplifier.

The input amplifier produces a gain of 1.909 (nominal) into the isolation amplifier. The input circuit for the AI16F is designed for a signal ranging from 0 to 20 mA across a 249 Ω load. The input circuit for the AI16E is designed for 0 to 10V signal range across a 1M Ω resistor. Thus, the normal input to the isolation amplifier should range from 0 to 9.507 vdc. If the input signal from a field device is greater than 20.2 mA (9.601-vdc input to the isolation amplifier), an over-range condition exists. The software should detect any over-range condition. The microprocessor accomplishes over-range detection by monitoring the magnitude of the count value produced by the A/D converter. If the output of the A/D converter is greater than 31460 counts (which corresponds to 9.601-vdc), an over-range error condition exists.

Input channels PT16 and PT17 provide precision voltage levels to enable the microprocessor to evaluate the calibration of the analog circuitry. When PT16 is selected, the onboard circuitry supplies a fixed signal of 0.91-vdc to the input amplifier. When PT17 is selected, the circuitry supplies a fixed signal of 10-vdc to the input amplifier. The microprocessor reads the count values for these two inputs and compares them with expected values from memory. If the drift is less than a fixed tolerance value in memory, the software can calculate a correction factor for each of the field inputs. If the drift exceeds the tolerance value, the software can trigger a calibration error alarm.

4.6.2 A/D data input port

The microprocessor uses the following sequence to select an input channel, initiate A/D conversion, and read the resulting 16-bit digital image from the ADC.

1. The microprocessor writes the channel selected code and a high R/C signal to the output latch.
2. After completion of the write cycle, the microprocessor sets either programmable port P1.5 or P1.6 low to enable generation of the required port selection output signal.
3. The selected channel supplies its signal to the input of the analog circuitry. The high state of the R/C and CS/ signals enable internal sample-and-hold circuits in the ADC to acquire the input signal.
4. After a delay to allow signal stabilization, the microprocessor sets the R/C and CS/ signals low to start the conversion process. The sample-and-hold in the ADC retains the signal acquired during the previous interval.
5. The ADC sets the STS (BUSY/) signal low at the start of the conversion cycle. When the conversion cycle is complete, the STS signal returns to a high level.
6. The low-to-high transition of the STS signal triggers the INT4 input to the microprocessor.

7. The microprocessor sets the R/C signal high and then runs two read cycles to the A/D data input port with the CS/ signal low. The microprocessor sets the AD0 signal low to access the most significant byte of data and sets it high to access the least significant byte of data.
8. The microprocessor can repeat steps 4 through 7 to read the digital image from the sample-and-hold circuit without repeating the acquisition cycle.

4.7 I/O Ports

The HFC-AI16 board contains 16 input channels for analog input signals from external field equipment. Each channel includes a low-pass filter to block electrical noise and an optocoupler to isolate the onboard circuitry from the field circuitry. Each channel includes a connection to an onboard DIP switch that permits configuration for either common or isolated operation on a channel-by-channel basis. When a channel is configured for common mode operation, 24-vdc power is supplied from the board to the field transducer that produces the input signal. When a channel is configured for isolated operation, that channel is electrically isolated from all other components on the board, and the field transducer must provide the power source to drive the input signal.

5.0 Hardware Connections

The HFC-AI16 board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-AI16 and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each AI channel can be configured for either isolated or common operation on an individual basis. Table 2 lists connection requirements for both isolated and common configurations for each channel.

6. Software Detailed Design Specification

The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AI16F board.

6.1 Board Information

The HFC-AI16F board has a total of 16 identical AI channels. Each channel will provides positive and negative terminal connections for a signal in the range of 0-20 mA. The board contains a single A/D converter that will be configured to produce a 16-bit digital image of the analog input for each channel.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	[]	P2-C1	[]
P2-A2	[]	P2-C2	[]
P2-A3	[]	P2-C3	[]
P2-A4	[]	P2-C4	[]
P2-A5	[]	P2-C5	[]
P2-A6	[]	P2-C6	[]
P2-A7	[]	P2-C7	[]
P2-A8	[]	P2-C8	[]
P2-A9	[]	P2-C9	[]
P2-A10	[]	P2-C10	[]
P2-A11	[]	P2-C11	[]
P2-A12	[]	P2-C12	[]
P2-A13	[]	P2-C13	[]
P2-A14	[]	P2-C14	[]
P2-A15	[]	P2-C15	[]
P2-A16	[]	P2-C16	[]
P2-A17	[]	P2-C17	[]
P2-A18	[]	P2-C18	[]
P2-A19	[]	P2-C19	[]
P2-A20	[]	P2-C20	[]
P2-A21	[]	P2-C21	[]
P2-A22	[]	P2-C22	[]
P2-A23	[]	P2-C23	[]
P2-A24	[]	P2-C24	[]

Table 2. Input Connection Summary

Channel No.	Type	Positive	Negative	Dipswitch
1	[]	[]	[]	[]
	[]	[]	[]	[]
2	[]	[]	[]	[]
	[]	[]	[]	[]
3	[]	[]	[]	[]
	[]	[]	[]	[]
4	[]	[]	[]	[]
	[]	[]	[]	[]
5	[]	[]	[]	[]
	[]	[]	[]	[]
6	[]	[]	[]	[]
	[]	[]	[]	[]
7	[]	[]	[]	[]
	[]	[]	[]	[]
8	[]	[]	[]	[]
	[]	[]	[]	[]
9	[]	[]	[]	[]
	[]	[]	[]	[]
10	[]	[]	[]	[]
	[]	[]	[]	[]
11	[]	[]	[]	[]
	[]	[]	[]	[]
12	[]	[]	[]	[]
	[]	[]	[]	[]
13	[]	[]	[]	[]
	[]	[]	[]	[]
14	[]	[]	[]	[]
	[]	[]	[]	[]
15	[]	[]	[]	[]
	[]	[]	[]	[]
16	[]	[]	[]	[]
	[]	[]	[]	[]

6.2 Analog Input Scan Algorithm

Every scan cycle, the scan module performs an AI calibration test, and then calculates the AI offset and gain. If any errors occur during the calibration test, the scan module sets an error bit in the diagnostics byte, marks the normal response as a bad response, and returns.

If no errors occur during the calibration test, the module reads the raw value of each analog input channel from the AD converter, and adjusts the raw value with AI offset and AI gain using the algorithm described in Section 4.2.3 “AI Algorithm.”

After finishing with all channels, the module stores the adjusted raw value in a filter buffer, and calculates a moving average of all records of raw value in the buffer. The filter buffer’s size is predefined. Every scan cycle, a new reading of raw value is added to the buffer, and the earliest reading in the buffer is pushed out.

There are two calibration parameters for each channel that are originally obtained from the EPROM. The software uses these parameters to adjust the filtered AI raw value of each channel for better accuracy. Then the adjusted input images will be saved in the scan work buffer. Refer to Section 4.3 “Single Channel Adjustment Algorithm” for the adjustment algorithm using calibration parameters.

6.2.1 Read Channel Raw Value

During each AI signal reading, control signals are used to initialize the A/D converter (ADC), and to sample the input signal from the selected channel. The output signal STS is linked with the interrupt signal INT4 to the microprocessor. This signal indicates the status of the ADC cycle. It goes low at the beginning of a conversion and returns high when the conversion cycle is complete. The interrupt request register REQST is used to check the ADC conversion complete bit (INT4).

The module takes a predefined number of AI samples per channel and averages the raw count value. The main sequence to scan the image for one AI channel is as follows:

1. Initialize the AI image accumulator to 0
2. Initialize loop counter to sample numbers
3. Select the port for this AI channel
4. Then loop to initialize an A/D conversion, wait till the REQST indicates the completion of A/D conversion, then read data from the A/D converter, and add the sample data to the AI image accumulator
5. After the loop is finished, deselect the port
6. Average the AI image accumulator by sample numbers

6.2.2 Calibration Test Routine

This routine gets the raw values from the low calibration point and the high calibration point. If the low or high calibration point raw value is out of range, the routine will return with error. If there are no errors, the routine calculates AI offset and gain by using low and high calibration point raw values.

For the 15-bit AD converter, the raw value of the low calibration point should be within $0B18H \pm A0H$ counts, and the raw value of the high calibration point should be within $79E0H \pm A0H$ counts. When the raw values are within the acceptable ranges, the calculation of AI offset and AI gain is as follows:

$$\begin{aligned} \text{AI Offset} &= 0B18H - \text{Raw Value of Low Calibration Point} \\ \text{AI Gain} &= 79E0H - (\text{Raw Value of High Calibration Point} + \text{AI Offset}) \end{aligned}$$

6.2.3 AI Algorithm

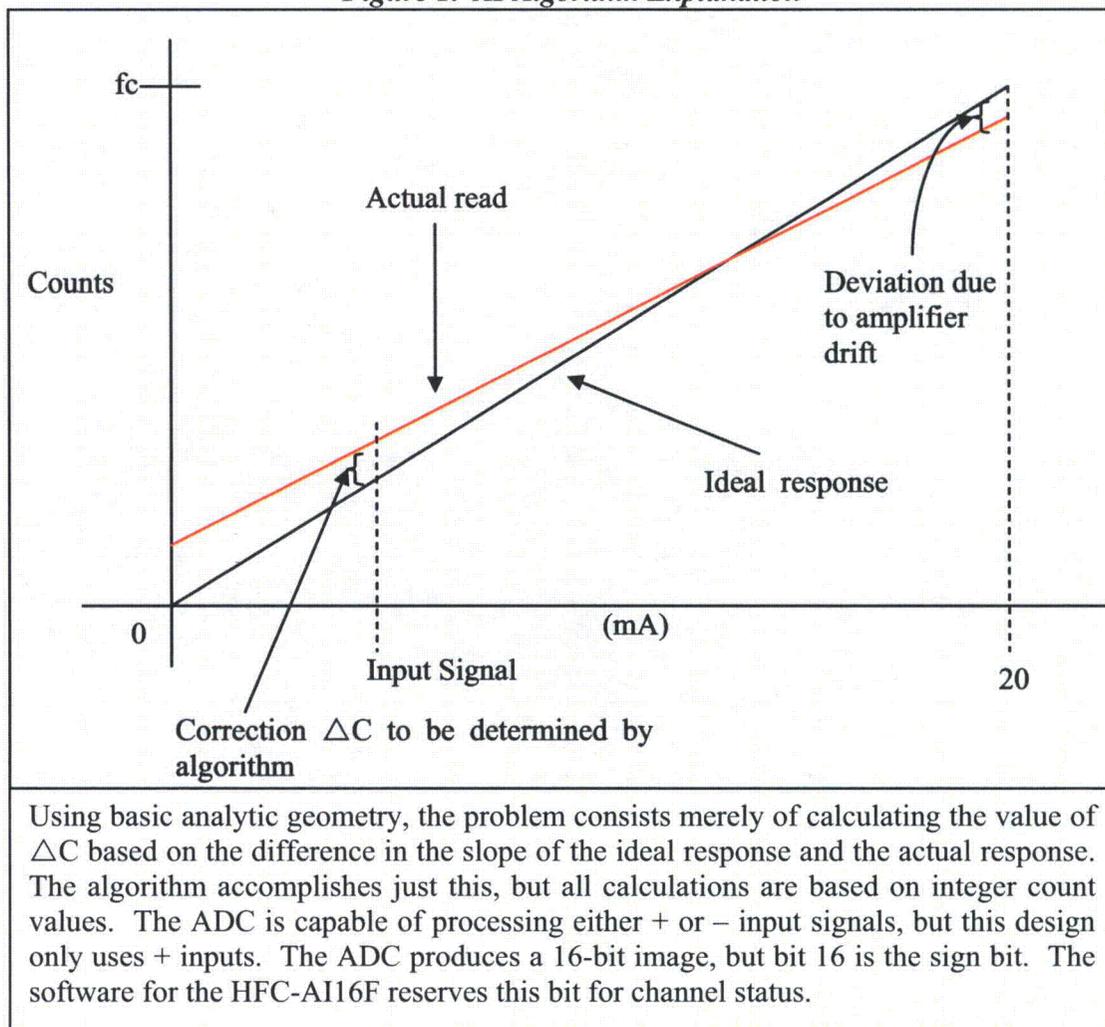
For the 15-bit AD converter, the calculation of AI image is as follows:

[

]

Please see Figure 1 below for an explanation of what this AI Algorithm is accomplishing.

Figure 1. AI Algorithm Explanation



6.3 Single Channel Adjustment Algorithm

The single channel adjustment algorithm is used in the software of AI16I, AO8F, AC36 boards to achieve better accuracy. Offset and gain for each channel will be determined by testing or default to zero, and an EPROM file will be built incorporating the offset and gain parameters in a specific location of EPROM memory. The first time the I/O software enters the scan module, the software obtains the offset and gain parameters from the specific memory location in EPROM to calculate actual raw value for 4 mA and 20 mA of each analog input or analog output channel and saves them in a buffer as two arrays: CALZERO and CALGAIN.

[

]

Both 12-bit and 15-bit adjustment shall be handled according to the board type. 15-bit AI requires over range and under range check. 12-bit AO doesn't have over range or under range, but needs to make sure that negative number is set to 0 and over 0FFFH number clamp to 0FFFH to avoid overflow.

6.4 HFC-AI16F-board Specific Modules

6.4.1 I/O Scan Module

The SCAN module performs AI scan for sixteen channels

6.4.2 Process Command routine

For normal update messages, this routine doesn't do anything because there is no AO channel on card. UCP diagnostics messages are processed as described in document DS002-0000-02.

6.5 Data Structure

6.5.1 Scan Data

The data field of the response message sent to the HFC-SBC06 controller contains AI images for sixteen channels as follows:

Table 3. Byte Assignments For Scan Data

Byte	AI	Byte	AI	Byte	AI	Byte	AI
0	CH1 (L)	8	CH5 (L)	16	CH9 (L)	24	CH13 (L)
1	CH1 (H)	9	CH5 (H)	17	CH9 (H)	25	CH13 (H)
2	CH2 (L)	10	CH6 (L)	18	CH10 (L)	26	CH14 (L)
3	CH2 (H)	11	CH6 (H)	19	CH10 (H)	27	CH14 (H)
4	CH3 (L)	12	CH7 (L)	20	CH11 (L)	28	CH15 (L)
5	CH3 (H)	13	CH7 (H)	21	CH11 (H)	29	CH15 (H)
6	CH4 (L)	14	CH8 (L)	22	CH12 (L)	30	CH16 (L)
7	CH4 (H)	15	CH8 (H)	23	CH12 (H)	31	CH16 (H)

7. Module Implementation Description

7.1 Hardware Schematics

The schematic for the HFC-AI16F board is drawing 400433-01.

7.2 Hardware Components – Bill of Materials

The part number of the HFC-AI16F board is 40043201, and its bill of materials is 400432-01.

7.3 Software Source Code Listing

The HFC-AI16F board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- []
- []

8. Design Safety

Refer to MS901-000-02 for a discussion of design safety issues.

HFC Non-proprietary



HF Controls

HF Controls Corporation

HFC-6000 Product Line

**HFC-AO8 Board
Module Detailed Design Specification**

Eight Channel Analog Output Board

DS901-000-08

Rev D

Effective Date 2/2/2009
Author Gregory Rochford
Reviewer Pat Thibodeau
Approval David Briner

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Revision History

<i>Date</i>	<i>Revision</i>	<i>Author</i>	<i>Changes</i>
11/14/03	0	D. Bynum	Initial
11/21/03	A	D. Bynum	Review comments incorporated
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Table of Contents

Number	Title	Page
1.0	INTRODUCTION.....	4
1.1	REFERENCES	4
1.2	SPECIAL TERMS AND ABBREVIATIONS	4
2.0	SPECIFICATIONS.....	4
3.0	CONTROLS AND INDICATORS.....	5
3.1	JUMPERS	5
3.2	FUSES.....	5
4.0	FUNCTIONAL DESCRIPTION.....	5
4.1	OVERVIEW	6
4.2	POWER DISTRIBUTION	6
4.3	RESET/INITIALIZATION	6
4.4	MEMORY STRUCTURE.....	7
4.5	INTERRUPT PROCESSING	7
4.6	MICROPROCESSOR PERIPHERAL PORTS.....	7
4.6.1	AO Interface.....	7
4.6.2	Fail safe condition data input port	8
5.0	HARDWARE CONNECTIONS.....	9
6.0	SOFTWARE DETAILED DESIGN SPECIFICATION.....	10
6.1	BOARD INFORMATION.....	10
6.2	ANALOG OUTPUT SCAN ALGORITHM.....	10
6.3	SINGLE CHANNEL ADJUSTMENT ALGORITHM.....	10
6.4	HFC-AO8F BOARD SPECIFIC MODULES.....	11
6.4.1	I/O Scan Module	11
6.4.2	Process Command routine	11
6.5	DATA STRUCTURE	11

6.5.1 *Scan Data*.....12

7.0 MODULE IMPLEMENTATION DESCRIPTION.....12

7.1 **HARDWARE SCHEMATICS**12

7.2 **HARDWARE COMPONENTS – BILL OF MATERIALS**12

7.3 **SOFTWARE SOURCE CODE LISTING**.....12

8.0 DESIGN SAFETY12

List of Tables

Number	Title	Page
Table 1.	AO Failsafe Control.....	9
Table 2.	Data Justification of AO Images.....	9
Table 3.	Connector P2 Pinout Summary.....	10
Table 4.	Byte Assignments For Scan Data	12

1.0 INTRODUCTION

The HFC-AO8 assembly is an 8-channel analog output board. This assembly operates as a standard AO board in an HFC-6000 control system. It receives digital output images from the system controller and performs D/A conversion for each channel at regular intervals. The HFC-SBC06 controller initiates communication with a configured HFC-AO8 board during its regular scan cycles, and the HFC-AO8 board receives the current digital image for all output channels from the poll message and returns current status.

Descriptions and discussions of the architectural and design descriptions of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Card Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-AO8 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-AO8 board will be presented using design, implementation, and configuration information.

1.1 REFERENCES

700901-06	HFC-6000 I/O Card Requirements Specification
400473-01	HFC-AO8F Schematic
400472-01	HFC-AO8F 8 channel, 4-20mA Assembly
400472-02	HFC-AO8E 8 channel, 0-10V Assembly
WI-ENG-106	Development of Hardware Design Specification
MS901-000-02	HFC-6000 Product Line, I/O Module Design Specification
DS901-000-02	HFC-6000 Product Line, I/O Module Detailed Design Specification

1.2 SPECIAL TERMS AND ABBREVIATIONS

I/O	Input/Output
LSB	Least Significant Bit
RAM	Random Access Memory
AO8F	0-20mA 8 Channel Analog Output
AO8E	0-10V 8 Channel Analog Output
D/A	Digital to Analog Converter

2.0 SPECIFICATIONS

- Environmental Extremes
 - Temperature: 0° to 55° C (operating)
0° to 70° C (storage)
 - Relative Humidity: 5% to 95%, non-condensing
- Power Requirements

External Power Supply: +24 vdc, 0.4 A maximum load.

- Onboard Clock Rate
Microprocessor Clock: 22.1184 MHz

Output Channel Rating: 0 to 20 mA (-01 assembly) or 0 to 10 V (-02 assembly) with 1/16-A line fuse for each channel and a 0.5-A line fuse for all eight channels

- Mounting Requirements: Mounts vertically in an HFC-6000 chassis

3.0 CONTROLS AND INDICATORS

The firmware determines the overall operating characteristics of the hardware on the HFC-AO8 board. The HFC-AO8 board only includes the set of four LEDs and one switch that are common to all I/O board types (DS901-000-02). However, the board does include eight jumpers and nine fuses. These devices and the functions that they control are as follows:

3.1 JUMPERS

- W3-W5 Fail-state jumpers, refer to paragraph 4.6.2 in this document for more information on the fail-state jumpers.
- W37 Installed to make analog return and digital return electrical common.
- E1-E2 Installed during calibration only to disable the NMI signal. When this jumper is removed, the D-latch U41-A activates a high NMI signal. E1-E2 should be removed for normal operation.
- E5-E6 Function not currently defined.

3.2 FUSES

- F1, F2, Provide separate overload protection for each AO channel.
F4-F9
- F3 Provides common overload protection for the 24-vdc power source to the eight output drivers.

4.0 FUNCTIONAL DESCRIPTION

The HFC-AO8 board is controlled by an onboard 80C188EB microprocessor and provides a hardware interface between an HFC-6000 control system and field equipment requiring analog control signals.

4.1 OVERVIEW

The HFC-AO8 has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Card Module Design Specification. The major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Performs reset and initialization of onboard hardware.
- Responds to data transmissions from the HFC-6000 controller.
- Receives AO images for each channel from the controller and stores that data in local memory.
- Transfers AO images from memory to the Digital-to-Analog (D/A) converter for each channel.
- Controls the D/A conversion process.

4.2 POWER DISTRIBUTION

The board receives redundant 24-vdc power feeds from the back plane connector J1. The two power feeds are diode auctioneered, and the combined 24-vdc power line is divided into four branches. One branch is routed to the input of an onboard voltage regulator. The second branch is routed through a 0.5-A onboard line fuse. The remaining two branches are routed to two ± 15 -vdc power supplies. These separate branches provide operating power for the following functions:

- The onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for logic components on the HFC-AO8 board.
- The fused 24-vdc power trace is routed to the VCC port of the output driver for each Analog Output (AO) channel.
- The two +15-vdc supplies provide operating power to the DAC for each channel. One of the +15-vdc supplies also provides power to a precision 2.5-vdc regulator that provides a reference voltage to all eight DACs.

4.3 RESET/INITIALIZATION

The Micro Monitor chip monitors the voltage level of the +5-vdc power rail, the state of the onboard reset switch (SW1), and normal operation of the microprocessor clock. When power is first applied to the board, the low state of the logic power rail causes the Micro Monitor chip to hold a /RESIN signal at a low level. After logic power increases above 4.5-vdc, the Micro Monitor chip keeps the /RESIN signal low for an additional 350 ms to ensure that all transient signals have dissipated before the microprocessor begins operation. During subsequent operation, the chip monitors its inputs for actuation of the RESET switch (SW1) or a significant drop in the voltage level of the onboard logic power rail.

When the microprocessor begins running, CLKOUT pulses are routed from the microprocessor to the Micro Monitor chip. If the microprocessor clock stops running for a

period of 50 ms, the Micro Monitor chip automatically activates the /RESIN signal to reset the microprocessor. If the operator presses the SW1 RESET switch, circuitry on the board causes the Micro Monitor chip to activate the /RESIN signal. When the operator releases the RESET switch, the /RESIN signal remains low for an additional 350 ms before permitting the microprocessor to resume normal operation.

4.4 MEMORY STRUCTURE

Memory on the HFC-AO8 board is organized into two banks of private memory for the microprocessor. Private memory for the 80C188EB microprocessor consists of one bank of EPROM and one bank of RAM. The private memory banks are connected directly to the address and data lines of the microprocessor.

4.5 INTERRUPT PROCESSING

The 80C188EB microprocessor provides a modular core for processing interrupts and exception conditions. The chip architecture includes an NMI input port, a variety of internally generated interrupts, and ports for five maskable interrupts (INT0 through INT4). For this application, the five maskable interrupt inputs are disabled. The NMI input is configured to halt the processor on a watchdog timeout.

4.6 MICROPROCESSOR PERIPHERAL PORTS

The microprocessor controls the following peripheral ports:

- Digital-to-Analog Converter (DAC) data output port
- Analog Output (AO) select output port
- Fail safe condition data input port
- Link address data input port
- Redundant serial port.

The Link Address input port, and the Redundant serial port are covered for the general case of I/O cards, therefore, they are not discussed here. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the three I/O ports

4.6.1 AO INTERFACE

The interface between the microprocessor and the analog outputs includes both the DAC data output port and the AO select output port. The interface between the microprocessor and each AO channel consists of an 8-bit latch, a one-of-eight demultiplexer, and a separate D/A converter for each channel. Because each AO image consists of 12 bits, the microprocessor must run two write cycles to each DAC. The hardware design for the card requires that the microprocessor transfer the most significant (high) byte of data to the DAC first and then the least significant (low) byte. During the second write cycle, the microprocessor transfers both bytes of data to the internal DAC register, enabling the DAC process to begin. The overall process required for data transfer to a single DAC is as follows:

1. The microprocessor runs an I/O write cycle with programmable output port P1.0 pulled low to transfer the high byte of the AO image to the 8-bit latch. The latch retains this data until it is overwritten by a subsequent write cycle. The output ports of the latch control an 8-bit data bus that is connected to each of the DAC chips.
2. The microprocessor pulls programmable port P1.1 low (CSMSB/) to transfer the high byte of the AO image from the 8-bit data bus into the input register of all DAC chips simultaneously.
3. The microprocessor runs a second write cycle to transfer the low byte of the AO image to the 8-bit latch.
4. The microprocessor places the binary code for the AO channel being processed on address lines A01, A02, and A03. The one-of-eight demultiplexer uses this code to activate the chip select signal (CS/) for the DAC associated with this AO channel.
5. The low active CS/ signal transfers the low byte from the 8-bit data bus into the DAC for the selected channel, and it also transfers the entire AO image into the DAC register.
6. When the CS/ signal returns to a high state, the DAC begins the conversion process.

Each DAC is set to operate in a voltage-switching mode. To ensure accuracy in the voltage-switching mode, the full-scale output of each converter is limited to 2.5-vdc. Therefore, the onboard circuitry provides the DAC with a precision 2.500-vdc reference voltage input.

Once the AO image has been loaded into the DAC register, DAC automatically uses that data to perform D/A conversion, unless overridden by a failsafe condition (controlled by the FH/L and FH/C signals). Of the 16 bits in the DAC register, only 12 bits are used to represent the channel output value; and these 12 bits are either right or left justified in the register, depending on the logic state of the FH/L and FH/C signals (Table 2). The DAC converts the AO image into a corresponding current value, and the current signal provides the input to an amplifier, which produces an output signal between 0 and +5 vdc. This voltage is supplied to the input of a precision voltage-to-current converter, which produces an output signal having a range of 0 to 20 mA.

The DAC produces an analog output that has a full-scale range of 0 to 2.5 vdc. The individual analog channels condition the output to provide 0-20 mA (-01 assembly). The -02 assembly has 499 Ω resistors on each output channel that convert the 0-20 mA signal into a 0- 10 V signal.

4.6.2 FAIL SAFE CONDITION DATA INPUT PORT

The design of the HFC-AO8 includes three jumpers that are used to configure the card for one of three failsafe modes: fail high, fail low, hold last state. Each failsafe jumper (W3, W4, and W5) controls the logic state of a separate input to an 8-bit buffer. The microprocessor can read the status of these jumpers by running a bus read cycle with programmable output port P1.0 pulled low. These inputs enable the software to determine the failure state selected by the jumper strapping. If the card loses communication with the controller, the software can

initiate the transition to the fail high/low state for each channel by transferring the appropriate AO image (00_H or FF_H) to each DAC. However, if a watchdog timeout occurs, the microprocessor stops running. During a watchdog timeout, jumpers W4 and W5 control the failsafe function. These jumpers control the logic state of the FH/L and FH/C signals. If jumper E1-E2 is removed, the logic state of the FH/L and FH/C signals force the DAC into the desired failure state on watchdog timeout. The hard-wired failure state produced by jumpers W4 and W5 following watchdog timeout are defined in Table 1.

In addition to controlling the failsafe response of the DAC, the FH/L signal also determines the required justification of the AO image in the DAC register. The software must read the jumper status in order to provide the proper justification for the AO image before transferring that image to the DAC. Table 2 defines the required justification of the image data based on the status of W5 when the FH/C signal is high.

Table 1. AO Failsafe Control

Jumper	Status	Function
W4	Removed	On watchdog timeout the microprocessor stops operation, and each DAC retains the last AO image received .
W4	Installed	On watchdog timeout the microprocessor stops operation; the high state of the FH/L signal and the low state of the FH/C signal overwrite the AO image in each DAC with all 1s.
W5	Removed	
W4	Installed	On watchdog timeout the microprocessor stops operation; the low state of the FH/L and FH/C signals overwrite the AO image in each DAC with all 0s.
W5	Installed	

Table 2. Data Justification of AO Images

W5	Most Significant Byte								Least Significant Byte							
ON	MSB								LSB x x x x							
OFF	x	x	x	X	MSB			LSB								
	8	7	6	5	4	3	2	1	8	7	6	5	4	3	2	1

5.0 HARDWARE CONNECTIONS

The HFC-AO8 card contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-AO8 and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 3.

Table 3. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	[]	P2-C1	[]
P2-A3	[]	P2-C3	[]
P2-A4	[]	P2-C4	[]
P2-A6	[]	P2-C6	[]
P2-A7	[]	P2-C7	[]
P2-A9	[]	P2-C9	[]
P2-A10	[]	P2-C10	[]
P2-A12	[]	P2-C12	[]

6.0 SOFTWARE DETAILED DESIGN SPECIFICATION

The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AO8F board.

6.1 BOARD INFORMATION

The AO8F card has a total of eight identical AO channels rated for 0-20 mA. Each channel includes a separate 12-bit D/A converter.

6.2 ANALOG OUTPUT SCAN ALGORITHM

An on-board fail-hi / fail-lo jumper provides option for using left justified or right justified output data for the D/A converter. Before writing analog output images to the D/A converters, the software checks if the jumper is installed. If it is installed, the software left-shifts each output image 4 bit positions to make it left-justified. (Each 12-bit image is stored as a single data byte.) If the jumper is not installed, the software leaves the AO images just as they are received from the controller.

There are two calibration parameters for each channel that were originally obtained from the EPROM. The software uses these parameters to adjust the output image of each channel for better accuracy. Then the software strobes the adjusted output image into D/A converter output for each channel. Refer to Section 6.3 for adjustment algorithm using calibration parameters.

6.3 SINGLE CHANNEL ADJUSTMENT ALGORITHM

The single channel adjustment algorithm is used in the software of AI16I, AO8F, AC36 cards to achieve better accuracy. Offset and gain for each channel will be determined by testing or default to zero, and an EPROM file will be built incorporating the offset and gain parameters in a specific location of EPROM memory. First time the I/O software enters scan module,

the software obtains the offset and gain parameters from the specific memory location in EPROM to calculate actual raw value for 4 mA and 20 mA of each analog input or analog output channel and saves them in a buffer as two arrays: CALZERO and CALGAIN.

[

]

The CALZERO array stores for each channel the actual value for 4 mA, i.e. STDZERO adjusted by offset parameter for that channel. The CALGAIN array stores for each channel the actual value for 20 mA, i.e. STDGAIN adjusted by gain parameter for that channel.

Let BX = channel number, then

[

]

Both 12-bit and 15-bit adjustments are handled according to the board type. The 15-bit AI image requires over range and under range checks. The 12-bit AO does not have over range or under range; however, the algorithm sets any negative value to 0 and changes any value above 0FFF_H to 0FFF_H to prevent overflow.

6.4 HFC-AO8F BOARD SPECIFIC MODULES

6.4.1 I/O SCAN MODULE

The HFC-AO8F board firmware has an I/O scan module like all other I/O boards, but because this board has no input channels, this module has no function.

6.4.2 PROCESS COMMAND ROUTINE

For normal update messages, this routine reads eight AO images and transfers them to the Scan Work Buffer. UCP diagnostics messages are processed as described in document DS002-000-02.

6.5 DATA STRUCTURE

6.5.1 SCAN DATA

The data field of the request message coming from the HFC-SBC06 controller contains AO images for eight channels, as follows:

Table 4. Byte Assignments For Scan Data

Byte	AO	Byte	AO
0	CH1 (L)	8	CH5 (L)
1	CH1 (H)	9	CH5 (H)
2	CH2 (L)	10	CH6 (L)
3	CH2 (H)	11	CH6 (H)
4	CH3 (L)	12	CH7 (L)
5	CH3 (H)	13	CH7 (H)
6	CH4 (L)	14	CH8 (L)
7	CH4 (H)	15	CH8 (H)

7.0 MODULE IMPLEMENTATION DESCRIPTION

7.1 HARDWARE SCHEMATICS

The schematic for the HFC-AO8F board is drawing 400471-01.

7.2 HARDWARE COMPONENTS – BILL OF MATERIALS

The part number of the HFC-AO8F board is 40047201, and its bill of materials is 400472-01.

7.3 SOFTWARE SOURCE CODE LISTING

The HFC-AO8F board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- []
- []

8.0 DESIGN SAFETY

Refer to MS901-000-02 for a discussion of design safety for HFC-6000 I/O modules.



HF Controls Corporation

HFC-6000 Product Line

HFC-AI4K

Module Detailed Design Specification

Pulse Input Board

DS901-000-12

Rev B

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Author Gregory Rochford

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Table of Contents

1.0	INTRODUCTION.....	4
2.0	HFC-AI4K FUNCTIONAL DESCRIPTION	4
3.0	HARDWARE DETAILED DESIGN SPECIFICATIONS	4
3.1	MODULE SPECIFICATION.....	4
3.2	ONBOARD POWER DISTRIBUTION	5
3.3	INTERRUPT PROCESSING	5
3.4	MICROPROCESSOR PERIPHERAL PORTS	5
3.4.1	<i>Counter Status Port.....</i>	<i>6</i>
3.4.2	<i>Port Addressing and Control.....</i>	<i>6</i>
3.4.3	<i>Input Channel Configuration.....</i>	<i>7</i>
3.5	CONTROLS, JUMPERS, AND INDICATORS.....	9
3.5.1	<i>Switches.....</i>	<i>9</i>
3.5.2	<i>Jumpers.....</i>	<i>11</i>
3.5.3	<i>Onboard Status Indicators.....</i>	<i>12</i>
3.6	CONFIGURATION PROCEDURE.....	12
3.6.1	<i>Hardware Setup Requirements</i>	<i>12</i>
3.7	HARDWARE CONNECTIONS	13
4.0	SOFTWARE FUNCTIONAL DESIGN DESCRIPTIONS	14
4.1	BOARD SPECIFIC MODULES	14
4.1.1	<i>I/O Scan Module</i>	<i>14</i>
4.1.2	<i>Display Functions During Normal Operation.....</i>	<i>15</i>
4.1.3	<i>Tuning Process.....</i>	<i>15</i>
4.1.4	<i>Process Command Routine.....</i>	<i>15</i>
4.2	DATA STRUCTURE	15
4.2.1	<i>Scan Data.....</i>	<i>15</i>
4.2.2	<i>Microprocessor Programmable Ports</i>	<i>15</i>
4.2.3	<i>Counter Status/Mode Port</i>	<i>17</i>
4.2.4	<i>Input Channels.....</i>	<i>17</i>
4.2.5	<i>Switch Input Port</i>	<i>17</i>
4.2.6	<i>Alphanumeric Display Messages.....</i>	<i>18</i>
5.0	MODULE IMPLEMENTATION DESCRIPTIONS	19
5.1	HARDWARE SCHEMATICS	19
5.2	HARDWARE COMPONENTS – BILL OF MATERIALS	19
5.3	SOFTWARE SOURCE CODE LISTING	19

1.0 Introduction

The HFC-AI4K pulse input printed circuit board (PCB) provides four pulse input channels for an HFC-6000 control system. This assembly operates as a standard I/O board in an HFC-6000 control system. The four input channels of AI4K can be configured to either rate mode or accumulate mode. The rate mode is used to monitor input pulse rate and each input is reported as a standard 12-bit AI point. Accumulate mode is used to maintain a cumulative count of pulses being received and the values are reported as two consecutive AI points.

Descriptions and discussions of the architectural and design descriptions of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

Subsequent sections of this document provide detailed structure and design descriptions of the HFC-AI4K board, with concentration on the specific characteristics of an HFC-AI4K board. The design descriptions of the common software modules of I/O cards are covered in document DS901-000-02, HFC-6000 I/O Card Module Detailed Design Specification.

2.0 HFC-AI4K Functional Description

The HFC-AI4K board is controlled by an onboard 80C188EB microprocessor and provides an interface for up to four analog field inputs and four analog field outputs for an HFC-6000 control system. The AI4K board has onboard switches for manual configuration and status monitoring for each channel. It has an eight-character alphanumeric display to provide a visual indication of operating status.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification. Major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Controls reset and initialization functions.
- Supports channel configuration.
- Samples the pulse input data from each of the input channels.
- Stores the input data image for each channel in local memory.
- Respond to data transmissions from the HFC-6000 controller.

3.0 Hardware Detailed Design Specifications

3.1 Module Specification

- Environmental Extremes
 - Temperature: 0° to 55° C (operating)
0° to 70° C (storage)
 - Relative Humidity: 5% to 95%, noncondensing

- **Power Requirement**
External Power Supply: +24-vdc, 0.4 A maximum load.
Interrogation Voltage: +48-vdc
- **Onboard Clock Rate**
Microprocessor clock 22.1184 MHz
- **Mounting Requirements:** Mounts vertically in HFC-6000 board chassis.
- The HFC-AI8M PCB meets the requirements of seismic category I.
- Low memory provides 32K by 8-bits of nonvolatile RAM for temporary storage of message data being processed. Nonvolatile RAM is used to ensure that channel configuration parameters will be preserved when power is removed from the system.
- **Pulse Input Channel Operating Limits**

Pulse rate: 0 Hz through 20 kHz
Peak voltage level: 12-vdc to 150-vdc
Peak input current: 10 ma (nominal)

3.2 ONBOARD POWER DISTRIBUTION

The board receives redundant 24-vdc power feeds from the backplane connector P1. The two power feeds are diode auctioneered, and an onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for components on the HFC-AI4K board.

The board receives interrogation power (nominally 48-vdc) from the backplane. Proper field input wiring permit the user to configure one or more channels to operate with this interrogation power source. Overload protection is provided by a common line fuse, and an optocoupler permits the microprocessor to monitor status of the power line.

3.3 INTERRUPT PROCESSING

The 80C188EB microprocessor provides a modular core for processing interrupts and exception conditions. The chip architecture includes an NMI input port, a variety of internally generated interrupts, and ports for five maskable interrupts (INT0 through INT4). For this application, all of the maskable interrupt inputs are disabled. The NMI input is controlled by the watchdog timer.

3.4 MICROPROCESSOR PERIPHERAL PORTS

The microprocessor controls the following peripheral ports:

- Link address data input port
- Redundant serial port.

- Switch status input
- Counter status input
- Programmable counter I/O
- Display control
- Status input from each pulse input channel.

The link address input port, and the redundant serial port are common to all I/O board types, and are described in document DS901-000-02. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the six I/O ports

3.4.1 Counter Status Port

The board contains a separately addressable input port for reading the following status input signals:

- CT_EN1 – High state indicates that the counter function for input channels 1 and 2 is enabled.
- CT_EN2 – High state indicates that the counter function for input channels 3 and 4 is enabled.
- RATE0/ - High state indicates that rate mode is selected for input channels 1 and 2.
- RATE1/ - High state indicates that rate mode is selected for input channels 3 and 4.

When rate mode is selected for a particular pair of input channels, the microprocessor uses the CT_EN status input to determine when the sampling period is complete. If rate mode is disabled, the CT_EN status is not meaningful.

3.4.2 Port Addressing and Control

The hardware design of the HFC-AI4K card uses direct addressing to access the remaining hardware ports on the board as well as specific registers within the intelligent devices associated with those ports. When the microprocessor requires access to one of these ports, it sets programmable output P1.0 low and places the address for the desired port on address lines A12, A13, and A14. A demultiplexer decodes the address code to activate one of eight output chip select signals. These signals control access to the following I/O ports:

- Address code 000 is assigned to the onboard eight-character alphanumeric display. When this device is selected, address signals A00 through A05 are used to access internal data and control registers. The microprocessor can then read status data from the internal registers or transfer data to the device for display.
- Address code 001 is assigned to an onboard 82C54 interval counter, and address signals A00 and A01 control access to three eight-bit counters and one control register. The microprocessor can read the current value of a selected counter, set the operating mode for a selected counter, or set a selected counter to a starting value.
- Address code 010 is assigned to the control function for the four pulse input channels. When this code is selected, address signals A00, A01, and A02 are decoded to produce a

single output signal (CLR0/, CLR1/, SET0, or SET1/). The CLR0/ output clears the counters for pulse input channels 1 and 2, and the SET0/ output signal enables the count function for these two channels to start. The CLR1/ and SET1/ signals control the corresponding functions for pulse input channels 3 and 4. These output signals are used to start the sampling interval during rate mode operation.

- Address code 011 is assigned to the switch input port. When this address is selected, the microprocessor can read the status of switches S1, S2, S3, and the rotary switch connected at J5. The status of the excitation voltage is also included with this input data byte. The software uses the switch inputs to control configuration of the pulse input channels and as well as the specific data sent to the onboard display.

Address codes 100 through 111 each enable access to a single 82C55A port controller, and address signals A00 and A01 control access to internal registers of the selected port controller. Each port controller is associated with one of the pulse input channels. An 82C55A port controller includes 24 I/O pins that can be programmed to operate in one of three operating modes. For the present application, all 24 I/O pins are programmed to receive input data from the two 12-bit counters for a particular pulse channel. The microprocessor can read the current count of one or both 12-bit counters by running consecutive read cycles to the internal registers and incrementing address signals A00 and A01 with each read.

3.4.3 Input Channel Configuration

Each input channel consists of a voltage biasing network with a simple RC low-pass filter, an optocoupler, a second low-pass filtering network, a signal conditioning network, and two cascaded 12-bit counters. The 24 output signals from the two counters are routed to one of the programmable port controllers, and a slide switch controls selection of either the accumulate or the rate mode of operation.

3.4.3.1 Input Signal Conditioning

The input network monitors digital pulse (nominally 48-vdc) input signals. These signals are applied across RC low-pass filters (34 kHz shoulder frequency) to the input of transistor switches. When no signal is present, the low-pass filter shunts high frequency noise to ground, and the transistor switch remains cut off. When a positive input is present, the transistor becomes forward biased and passes an output through the base-emitter junction. A Zener diode in the base circuit limits the output voltage to the TTL range upstream from the optocoupler.

The final stage of signal conditioning consists of a second low-pass filter, a voltage comparator configured as a high speed switch, and a NAND gate. The low-pass filter is configured in parallel with the input of the voltage comparator to block any residual signal noise that could produce invalid pulse inputs to the counters. However, because the shoulder frequency of this filter is relatively low (63 Hz to 63 kHz), it also distorts the input waveform. In order to produce a signal having well defined leading and trailing edges, the output from the low-pass filter is connected to the non inverting input of the voltage

comparator. The biasing network connected to the inverting input comparator controls the voltage level at which the device switches its output signal. This network is configured to switch from OFF to ON when the input signal increases above 3.33 volts, and it switches from ON to OFF when the signal decreases below 1.67 volts. The resulting output is connected to a NAND gate and controls the clock input to the first of the two 12-bit counters. The NAND gate inverts the signal so that the trailing edge of each pulse increments the count.

3.4.3.2 Pulse Channel Operation

Selection of rate mode operation for each pair of pulse input channels is controlled by a slide switch. When the slide switch for channels 1 and 2 is in the rate position, switch contacts produce the following control circuits:

- The CT_EN1 signal is NANDed with the input pulse train for channel 1 and channel 2. When the CT_EN1 signal is low, the NAND gate blocks the pulse input, and the counters stop incrementing.
- The CLR0/ signal is routed to the reset port of all four 12-bit counters for these two input channels.
- A high RATE0/ signal is routed to the counter status input port.

When the RATE0/ signal is high, the microprocessor selects tuning parameters for the rate mode from memory. The operator must enter these tuning parameters manually from the rotary switch and the three pushbutton switches during hardware configuration of the card. The tuning parameters control selection between 8-bit and 12-bit resolution, a preset count value, and the maximum pulse rate. The microprocessor controls rate mode operation by configuring the programmable counter for a sampling interval determined by the tuning parameters, and then it clears the 12-bit counters. Once the counters have been cleared, the microprocessor activates the SET1 output. This signal sets a latch that activates the CNT_EN1 output signal. While this signal is high, the interval counter is enabled, and the 12-bit counters increment with each pulse received from the field. When the sampling interval expires, the interval counter produces an output pulse that clears the latch, forcing the CNT_EN1 signal low. The low state of the CNT_EN1 signal blocks further input to the 12-bit counters and notifies the microprocessor that the sampling period is complete. The microprocessor then reads the accumulated count from the port controllers for channels 1 and 2.

When the slide switch for channels 1 and 2 is in the accumulate position, the RATE0/ signal assumes a low level, and the reset input to the 12-bit counters is disabled. While accumulate mode is enabled, all pulses received from the field pass to the clock input port of the first 12-bit counter. When this counter reaches full count, the high-to-low transition of the MSB increments the second 12-bit counter. While accumulate mode is enabled, the counters continue incrementing, and the microprocessor reads the total 24-bit accumulated count at periodic intervals.

3.5 CONTROLS, JUMPERS, AND INDICATORS

The firmware determines the overall operating characteristics of the hardware on the HFC-AI4K board. The HFC-AI4K board includes the set of four LEDs and a RESET pushbutton common to all I/O board types (DS901-000-02). In addition, the board includes jumpers, switches, and onboard indicators. These devices and the functions that they control are as follows:

3.5.1 Switches

The HFC-AI4K pulse input board includes a set of switches that enable configuration of operating parameters.

- S1 INC Actuating this switch when tuning mode is enabled increments the value of the tuning parameter currently being displayed.
- S2 DEC Actuating this switch when tuning mode is enabled decrements the value of the tuning parameter currently being displayed.
- S3 SEL Actuating this switch during normal operating mode displays the value of the indicated parameter. Actuating the SEL switch during tuning mode steps through the tuning parameters in sequence and then saves the new parameter in memory.
- S4 ACCUMULATE/RATE two-position slide-switch selects either the accumulate or the rate modes of operation for input channels 1 and 2.
- S5 ACCUMULATE/RATE two-position slide-switch selects either the accumulate or the rate modes of operation for input channels 3 and 4.
- S6 Four-position DIP switch. Closing a particular switch position configures the corresponding channel for common mode operation. Opening a particular switch position configures the corresponding channel for isolated mode operation.

Inputs from a 17-position rotary switch (J5) control alphanumeric displays presented on U23 and programming functions of the board. The function defined for each switch position is defined in Table 1.

Table 1. Rotary Switch Functions

Position	Function
0	Display off
1	CHANNEL 1. Displays the current value for input channel 1 in either the accumulate or the rate mode of operation.
2	CHANNEL 2. Displays the current value for input channel 2 in either the accumulate or the rate mode of operation.
3	CHANNEL 3. Displays the current value for input channel 3 in either the accumulate or the rate mode of operation.
4	CHANNEL 4. Displays the current value for input channel 4 in either the accumulate or the rate mode of operation.
5	1 & 2 ACCUM/RATE. Displays the current operating mode selected for channels 1 and 2.
6	1 & 2 PRESCALE/RATE. When ACCUMULATE mode is selected for channels 1 and 2, the display indicates the number of pulses that must be received before the accumulator is incremented. When RATE mode is selected, the display indicates the counter resolution (8-bit or 12-bit) and maximum pulse rate selection.
7	3 & 4 ACCUM/RATE. Displays the current operating mode selected for channels 3 and 4.
8	3 & 4 PRESCALE/RATE. Presents the same display as switch position 6 for channels 3 and 4.
9	PRESET CH 1. Actuating the INC/DEC switches enables the user to enter a preset count value for channel 1. Actuating the SEL switch causes the board to display the SAVE TUN prompt. Actuating the SEL switch a second time saves this value in memory.
A	PRESET CH 2. Enables the same tuning function as switch position 9 for input channel 2.
B	PRESET CH 3. Enables the same tuning function as switch position 9 for input channel 3.
C	PRESET CH 4. Enables the same tuning function as switch position 9 for input channel 4.
D	1 & 2 ACCU/RATE. When ACCUMULATE mode is selected for channels 1 and 2, actuating the SEL switch enables the user enter a single prescaler value for the two channels. When RATE mode is selected, the user can enter two tuning parameters. The first time the SEL switch is actuated, the user can select between 8-bit and 12-bit (either 8B or 12B) counter resolution. Actuating the SEL switch again permits the user to select the maximum pulse rate (from 512 up to 20 K for 12-bit or from 50 to 10 K for 8-bit) for channels 1 and 2. Actuating the SEL switch again prompts the user to save the new tuning parameter in memory.
E	3 & 4 ACCU/RATE. Provides the same tuning function as switch position D for channels 3 and 4.
F	Functional test. Actuating the RESET switch and then the SEL switch causes the firmware to step through an internal diagnostic routine. This test displays the current operating mode and the values of the tuning parameters.

3.5.2 Jumpers

E58-E57 Function not currently defined.

E100-E101 Installed during calibration to disable both the NMI signal. When this jumper is removed, the D-latch U4-A activates a high NMI.

The channel input interfaces have four RC low-pass filters whose shoulder frequency is determined by a jumper strap. The jumper position typically installed at the factory selects a filter frequency of 1590 Hz. This filter frequency can be changed in the field as necessary to provide greater attenuation of signal noise. The input channels one through four jumper functions are defined in Table 2.

Table 2. Jumper Configuration

Input Channel 1
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: <ul style="list-style-type: none"> • E102-E103 1590 Hz • E104-E105 159 Hz • E106-E107 15.9 Hz • E108-E109 1.59 Hz
Input Channel 2
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: <ul style="list-style-type: none"> • E110-E111 1590 Hz • E112-E113 159 Hz • E114-E115 15.9 Hz • E116-E117 1.59 Hz
Input Channel 3
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: <ul style="list-style-type: none"> • E118-E119 1590 Hz • E120-E121 159 Hz • E122-E123 15.9 Hz • E124-E125 1.59 Hz
Input Channel 4
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: <ul style="list-style-type: none"> • E126-E127 1590 Hz • E128-E129 159 Hz • E130-E131 15.9 Hz • E132-E133 1.59 Hz

3.5.3 Onboard Status Indicators

The HFC-AI4K provides an eight-character alphanumeric display (U23) that indicates current operating status of the board. During board configuration, the display operates in conjunction with switches S1 through S3 and J5 to enter and save operating parameters. During normal operation, the display operates with the programmable switch (J5) to provide a readout of current values for operating parameters.

3.6 CONFIGURATION PROCEDURE

3.6.1 Hardware Setup Requirements

Before a new HFC-AI4K card can be placed into a system, onboard jumpers and switches must be set to match the specific operating environment that will be required.

1. Each input interface can be configured for isolated or common mode operation. Set each position of DIP switch to select either common mode (switch closed) or isolated mode (switch open) for the corresponding input channel.
2. The input interfaces have four RC low-pass filters whose shoulder frequency is determined by jumper straps (Table 2). The jumper position typically installed at the factory selects a filter frequency of 62.8 kHz. This filter frequency can be changed in the field as necessary to provide greater attenuation of signal noise.
3. Position switches S4 and S5 to select either rate or accumulate mode for the input channels.
4. Insert the board into the selected I/O board slot and power up the chassis.

3.6.1.1 Point Type Configuration

The pulse board reports its data to the controller either as a 12-bit or a 24-bit image. In order to allocate adequate memory in the controller for the input data, the user must configure a pulse input card as an AI8 board type in the I/O configuration table. However, the specific channel and AI point assignments depend on the operating mode selected for each input channel indicated in Table 3.

Table 3. Input Channel Assignments

Input Channel	Rate Mode	Accumulate Mode
1	AI1	AI1 and AI2
2	AI2	AI3 and AI4
3	AI5	AI5 and AI6
4	AI6	AI7 and AI8

3.6.1.2 Input Channel Tuning Parameters

The operator must enter tuning parameters directly into the pulse board using rotary switch (J5) and pushbutton switches (S1 through S3) mounted on the edge of the board. The rotary switch permits the user to read the current values of the data in memory and to revise the tuning parameters for each channel. The following steps outline the process for updating the values of the tuning parameters in memory.

1. Rotary switch positions 9 through C enable the user to update a preset parameter for each channel. This value determines the starting count for the corresponding channel when that channel is in the accumulate mode. The preset value is not used for the rate mode.
2. Rotary switch positions D and E enable the user to enter either a prescaler value (accumulate mode) or a maximum input pulse rate (rate mode).
 - For accumulate mode, the firmware accepts a single prescaler value for each pair of input channels (1 and 2 or 3 and 4). When the prescaler value is either 0 or 1, the counter increments with each input pulse. For any number greater than 1, the prescaler value determines the number of input pulses that must be received before the counter is incremented by 1. Actuating the SEL switch after setting the desired prescaler value saves the tuning parameter in memory.
 - For rate mode, the firmware accepts a separate parameter for counter size and for maximum pulse rate. The first time the SEL switch is incremented, the default counter size is displayed. Actuating the UP or DN switch causes this value to toggle between 8B (8-bit) and 12B (12-bit). Actuating the SEL switch again causes the firmware to display the default maximum pulse rate of 512 Hz. The user can increment this parameter in steps from 512 Hz up to 20,000 Hz for 12 bit by actuating the UP switch. Range for 8 bit is from 50 HZ to 10 KHZ. Actuating the SEL switch after setting both values saves those parameters to memory.

3.7 HARDWARE CONNECTIONS

The HFC-AI4K board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-AC36 and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 4.

Table 4. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	[]	P2-C1	[]
P2-A3	[]	P2-C3	[]
P2-A4	[]	P2-C4	[]
P2-A6	[]	P2-C6	[]
P2-A2 P2-C2 P2-A5 P2-C5	[]		

4.0 Software Functional Design Descriptions

The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AI4K board.

4.1 Board Specific Modules

4.1.1 I/O Scan Module

If it is the first time that the software enters I/O Scan Module after power up or rest, the software runs a tuning test first to compare the mode parameters in memory with mode switch settings. If the parameters match the switch settings, the software can enter the Normal Operation stage for I/O scan. Otherwise, the software enters Tuning Mode to set up all configuration parameters. Refer to Section 4.1.2 for detailed Tuning Process. After tuning, the software goes back to Initialization module to set up interrupt vectors and memory buffers before it re-enters the operating system main routine.

Every scan cycle, a Tuning Test is performed to check if the status of any mode switch has been changed. If there are changes in the mode switch status, the routine will set diagnostic error bit in the diagnostic byte, mark the current normal response as a bad response, and return without performing an I/O scan. Otherwise, the routine proceeds to perform an I/O scan.

It starts reading function switch and command switches and updates display if there are any changes. Refer to Section 4.1.3 for details about the display functions. It reads mode switches settings to decide how to scan the four input channels: Rate mode or Accumulate mode for every two channels, and scans them accordingly.

For rate mode, raw count reading is 8 bit data. If the channel is set for 12-bit rate mode, the raw count is left shift 4 bits to make itself 12 bit. For accumulate mode, the reading result is divided by prescaler setting. The final channel data will be stored in the Scan Working buffer and the routine returns to the operating system main routine.

4.1.2 Display Functions During Normal Operation

During normal operation, the rotary switch J5 can be used to display data currently stored in memory. Refer to position 0 to 8 in Table 1.

4.1.3 Tuning Process

During tuning mode operation, the software will go through different tuning steps depending on mode selected and the configuration parameters entered. Basically, the Tuning Process has the main functions listed in position 9 to F in Table 1. The Switches SEL, INC and DEC are used to make selections for configuration parameters.

4.1.4 Process Command Routine

For normal update requests, this routine has no function. For UCP diagnostics messages, it uses the common processing as described in DS002-000-02 to process UCP request received on the ICL.

4.2 Data Structure

4.2.1 Scan Data

The data field of the response message to the HFC-SBC06 controller contains AI images for eight channels as follows:

Table 5. AI Image

Byte	AI
0	CH1 (L)
1	CH1 (H)
2	CH2 (L)
3	CH2 (H)
4	CH3 (L)
5	CH3 (H)
6	CH4 (L)
7	CH4 (H)

The request message from the SBC06 controller doesn't have a data field.

4.2.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 6 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 6. Programmable Ports Used for the Card

Port	Description	Implementation
P1.0	[]	[]
P1.1	[]	
P1.3	[]	
P1.7	[]	[]
P2.1	[]	[]
P2.3	[]	[]
Port 1 Control	[]	[]

Table 7. On-Board I/O Ports

Addr	On-Board I/O Ports
000	[]
001	[]
010	[]
011	[]
100-111	[]
1000	[]

4.2.3 Counter Status/Mode Port

Two-position slide-switches S4 and S5 control the operation mode of the input channels. S4 selects either the Accumulate or the Rate mode of operation for input channels 1 and 2. S5 selects either the Accumulate or the Rate mode for input channels 3 and 4.

The mode port permits the microprocessor to read the counter status input signals. These inputs indicate which modes are selected for the input channels.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Spare	Spare	Spare	Spare	RATE1	RATE0	CT_EN2	CT_EN1

CT_EN1 – High state indicates that the counter function for input channels 1 and 2 is enabled.

CT_EN2 – High state indicates that the counter function for input channels 3 and 4 is enabled.

RATE0/ - High state indicates that rate mode is selected for input channels 1 and 2.

RATE1/ - High state indicates that rate mode is selected for input channels 3 and 4.

When rate mode is selected for a particular pair of input channels, the CT_EN status input is used to determine when the sampling period is complete. If rate mode is disabled, the CT_EN status is not meaningful.

4.2.4 Input Channels

The AI4K card reports the data for its four pulse input channels as eight AI points to the SBC06 controller. The specific channel and AI point assignments depend on the operating mode of the card.

Table 8. AI Point Assignments to Pulse Input Channels

Mode 1&2	AI 1	AI 2	AI 3	AI 4	Mode 3&4	AI 5	AI 6	AI 7	AI 8
RATE	Ch. 1	Ch. 2	Spare	Spare	RATE	Ch. 3	Ch. 4	Spare	Spare
ACCU	Channel 1		Channel 2		ACCU	Channel 3		Channel 4	

4.2.5 Switch Input Port

Besides the two switches S4 and S5 mentioned above, the card includes four additional switches:

- J5 - 16-position rotary switch controls alphanumeric displays and programming functions of the card. This switch permits the operator to read the current values of the data in memory during normal operation and to enter or revise the configuration parameters for each channel while in tuning mode.
- S1 – INC. Actuating this switch during tuning increments the value of the tuning parameter currently being displayed.
- S2 - DEC. Actuating this switch during tuning decrements the value of the tuning parameter currently being displayed.

- S3 – SEL. Actuating this switch during normal operating mode displays the value of the indicated parameter. Actuating the SEL switch during tuning mode steps through the tuning parameters in sequence and then saves the new parameter in memory.

The switch input port provides the switch status input signals.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
J5 – Rotary Switch				S1-INC	S2-DEC	S3-SEL	Power

4.2.6 Alphanumeric Display Messages

The AI4K provides an eight-character alphanumeric display (U23) that indicates current operating status of the board. During board configuration, the display operates in conjunction with switches S1 through S3 and J5 to enter and save configuration parameters. During normal operation, the display operates with the J5 rotary switch to provide a read-out of current values for operating parameters.

The messages listed in the table below are designed for the display purpose of AI4K card.

Table 9. Display Messages

Message No	Display String
0	ROM ERR
8	RAM ERR
16	BRCH ERR
24	MATH ERR
32	LOG ERR
40	TUNE ERR
48	EPROM OK
56	SUM=
64	CPU ERR
72	CPU OK
80	J3 ON
88	REC. OK
96	REC. ERR
104	XMT 55?
112	XMT AA?
120	J4 ON?
128	COMPLETE
136	TUNE OK
144	TUNE?
152	1&2 RATE
160	3&4 RATE
168	1&2 ACCU
176	3&4 ACCU
184	8B
192	12B

200	' '
208	MOVE SW1
216	MOVE SW2
224	SAVE TUN
232	SAVED
240	HUNTING
248	' '

5.0 Module Implementation Descriptions

5.1 HARDWARE SCHEMATICS

The schematic for the HFC-AI4K card is in drawing 400448-01.

5.2 HARDWARE COMPONENTS – BILL OF MATERIALS

The part number of the HFC-AI4K card is 40044701 and its bill of materials is in file 40044701.txt.

5.3 SOFTWARE SOURCE CODE LISTING

Besides the common software sources for software common modules listed in the HFC-6000 I/O Card Module Detailed Design Specification, the HFC-AI4K card software also includes the following programs:

- []
- []