HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-SBC06-DPM06 Boards
Module Design Specification

System Controller

MS901-000-01

Rev E

INFORMATIONAL

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Table of Contents

1. INTRODUCTION 4
2. FUNCTIONAL DESCRIPTION 5
2.1 EXTERNAL COMMUNICATION 6
2.2 REDUNDANT SYSTEM CONTROLLERS 6
2.3 EXECUTION OF APPLICATION PROGRAMS 9
3. MODULE ARCHITECTURE 9
3.1 MEMORY MAPPING STRUCTURE 12
3.2 PUBLIC MEMORY DATA 13
3.3 REMOTE COMMUNICATION ARCHITECTURE 14
3.3.1 HFC-SBC06 HANDLING OF DDB DATA 16
3.3.2 HFC-SBC06 HANDLING OF UCP MESSAGES 17
3.4 SYS PROCESSOR SECTION 19
3.4.1 SYS PROCESSOR SOFTWARE ARCHITECTURE 21
3.5 ICL PROCESSOR SECTION 25
3.5.1 ICL SOFTWARE ARCHITECTURE 26
3.6 CPC PROCESSOR SECTION 28
3.6.1 CPC PROCESSOR SOFTWARE ARCHITECTURE 29
3.7 HFC-SBC06 AND HFC-DPM06 REDUNDANCY ARCHITECTURE 32
3.8 HFC-SBC06 CPLD DESIGN 35
3.9 SEQUENCE OF EVENTS TIMER 35
3.10 HFC-DPM06 BOARD 36
4. CONFIGURATION SETUP AND LED DISPLAYS 36
4.1 HFC-SBC06 ONBOARD SWITCH FUNCTIONS 36
4.2 HFC-DPM06 ONBOARD SWITCH FUNCTIONS 37
4.3 HFC-SBC06 ONBOARD JUMPER OPTIONS 37
4.4 LEDS 39
4.4.1 HFC-SBC06 LED FUNCTIONS 39
4.4.1.1 DS3 AND DS4 LEDS 39
4.4.2 HFC-DPM06 LED FUNCTIONS 41

4.5 INSTALLATION OF SYSTEM SOFTWARE AND APPLICATION PROGRAMS 42
4.5.1 SYSTEM CODE TRANSFER TO FLASH 42
4.5.2 APPLICATION CODE DOWNLOAD 43
4.5.3 SYSTEM SOFTWARE UPDATES 44
4.6 HARDWARE CONFIGURATION 44
5. MODULE DESIGN CONSTRAINTS 46
5.1 COMMUNICATION INTERFACE SPECIFICATIONS 46
5.2 OPERATING SYSTEM SPECIFICATION 46
5.3 HARDWARE INTERFACE SPECIFICATIONS 46
5.1 DESIGN SAFETY 46

List of Tables

Table 1. SYS Processor Configuration Switches 37
Table 2. Jumper Options 38
Table 3. DS3 and DS4 LED Indications for Initialization Failure 40
Table 4. DS3 and DS4 LED Indications for Individual Tasks 41
Table 5. DS3 and DS4 LED Failure Indications During Normal Operation 41

LIST OF FIGURES

Figure 1. HFC-6000 System Hierarchy 4
Figure 2. Redundant HFC-SBC06 Boards with DPM06 Board 7
Figure 3. ICL Network for Redundant Controller Configuration 8
Figure 4. Non-Redundant HFC-SBC06 Board and DPM06 Board 9
Figure 5. HFC-SBC06 / DPM06 Module Architectures 11
Figure 6. Microprocessor Address Space 12
Figure 7. Public Memory Data Stores 13
Figure 8. DDB Broadcast Data Paths 15
Figure 9. UCP Point-to-Point Message Path 15
Figure 10. Broadcasting and Filtering of DDB Data 17
Figure 11. UCP Message Processing 18
Figure 12. System Processor Architecture 19
Figure 13. System Software Architecture 23
Figure 14. ICL Processor Architecture 25
Figure 15. ICL Software Architecture 27
Figure 16. CPC Processor Architecture 29
Figure 17. CPC Software Architecture 31
Figure 18. HFC-SBC06 Redundancy and Failover 33

1. Introduction

The HFC-6000 distributed control system provides plant monitoring and control capabilities, with monitoring and control responsibilities spread over multiple remote control units. The HFC-SBC06 System Controller is the primary board used for implementing plant control functions. This HFC-SBC06-DPM06 Module Design Specification describes the HFC-SBC06 System Controller board and HFC-DPM06 Dual Ported Memory board.

As shown in Figure 1, the HFC-SBC06 System Controller board is positioned in the HFC-6000 system hierarchy between the Operator Station(s), which provides the direct Human Machine Interface to the plant operators, and the I/O boards which provide the signal-level interface to the equipment and devices in the plant.

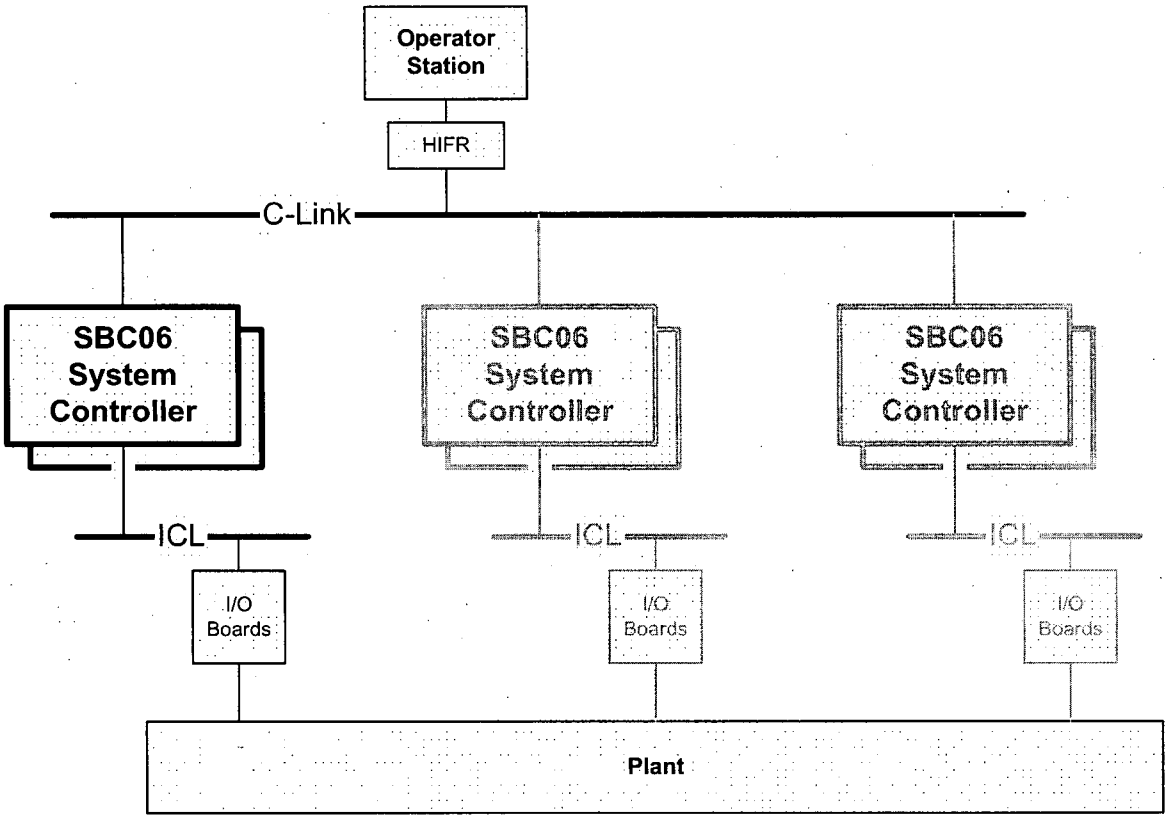

Figure 1. HFC-6000 System Hierarchy

Descriptions of the functional requirements of the HFC-SBC06 System Controller board and HFC-DPM06 board, from an external perspective, are provided in the HFC-6000 Product Line Requirements Specification, RS901-000-01. The design of the HFC-SBC06 and HFC-DPM06

also complies with the detailed requirements spelled out in 700901-04, 700901-05, and RS901-000-37.

The purpose of this document is to describe the operation and functions of the HFC-SBC06 and HFC-DPM06 boards. The discussion of the operation and function of the HFC-SBC06 and HFC-DPM06 will be presented using architectural, design, and implementation information.

Subsequent sections of this document provide architectural and design descriptions of the HFC-SBC06 board. Lower level descriptions of the HFC-SBC06 and HFC-DPM06 are contained in the HFC-SBC06-DPM06 System Controller Module Detailed Design Specification, DS901-000-01. The major functions performed by the HFC-SBC06 and HFC-DPM06 are listed in the next section which contains brief descriptions of the functions and how the HFC-SBC06 or HFC-DPM06 performs the functions.

2. Functional Description

The functions described in this section are the major functions performed by the HFC-SBC06 System Controller. The functional descriptions are presented so as to provide a context for understanding the operation of the HFC-SBC06 and a description of how the functions performed by the HFC-SBC06 System Controller work within the overall architecture of the HFC-6000 distributed control system.

The major functions performed by the HFC-SBC06 System Controller are:

- Communication with other system controllers and workstation PCs connected to the same redundant C-Link (Communication Link), an HFC proprietary network; Broadcasting plant status information;
- Communication with modules connected to the same ICL (Intercommunication Link), another HFC proprietary network; Collecting plant status information and sending plant operation commands;
- Redundant controller operation, System Controller failure detection, failover of the control function to the Secondary System Controller on failure of the Primary System Controller, and maintenance failover.
- Execution of application control programs for the specific control logic;

The following sections supply descriptions of the HFC-SBC06 functional requirements and identify aspects of the HFC-SBC06 that perform functions satisfying the requirements.

2.1 External Communication

Two communication interfaces connect the HFC-SBC06 to other boards and devices in the HFC-6000 system. Two identical 10BaseT interfaces connect the HFC-SBC06 to the redundant fiber optic Communication Link (C-Link) network, an HFC proprietary Ethernet-based network that the HFC-SBC06 uses to transfer data to and from the Operator Stations. Typical data transfers between the Operator Station and a System Controller are operator commands from an Operating Station to the System Controller and plant operation data to the Operator Station. The HFC-SBC06 also uses the C-Link to broadcast its status to other remotes attached to the C-Link.

The other HFC-SBC06 communication interface connects the HFC-SBC06 to the Intercommunication Link (ICL), which is an RS-485 serial network connecting the HFC-SBC06 to its I/O boards. Each HFC-SBC06 has two serial channels (ICL0 and ICL1) with each connecting to different I/O boards. Each serial channel can be linked to up to 32 I/O boards. Input values from plant field devices and output values to plant actuators are transferred between the HFC-SBC06 and I/O boards over the ICL serial network. The ICL network implements a master/slave communication protocol. Only the master can initiate communication, and the slave devices only respond to the master's poll. HFC-SBC06 serves as the master for all communication transfers with its configured ICL stations. Each I/O board operates as a slave node on the ICL network. The HFC-SBC06 polls each configured slave device at regular intervals, and the slave devices receive operation commands in the communication messages and respond with plant status information. Although each HFC-SBC06 board has two physical serial channels connected to different I/O boards, these two physical channels are on one logical link under the ICL protocol, either ICL A or ICL B for the I/O boards. Therefore, each ICL can be linked to up to 64 I/O boards.

Refer to DS002-000-01, C-Link Protocol Component Design Specification, and DS002-000-02, ICL Protocol Component Design Specification for details.

2.2 Redundant System Controllers

The HFC-SBC06 System Controller board is designed to operate in a redundant controller configuration. As shown in Figure 2, a redundant configuration consists of two System Controller boards (HFC-SBC06 A and HFC-SBC06 B) and a HFC-DPM06 dual ported memory board with the DPM06 board installed in between of the two SBC06 boards. Each HFC-SBC06 board in the redundant pair operates in one of two different modes: one board operates in a Primary controller mode, and the other board operates in a Secondary controller mode. Controller mode operation is determined at controller board start-up, with the first HFC-SBC06 to complete its initialization routine becoming the Primary, and the other HFC-SBC06 board defaults to Secondary controller mode.

Each HFC-SBC06 in a redundant pair is connected to redundant C-Link networks for communication with the Operating Station and one of two ICL serial networks that provides communication between the HFC-SBC06 and to each of its I/O boards. Each I/O board connects

with two system controllers via its dual serial ports as shown in Figure 2. The mode (Primary or Secondary) in which the HFC-SBC06 is operating determines how the HFC-SBC06 will use C-Link (Ethernet) and ICL (serial) networks.

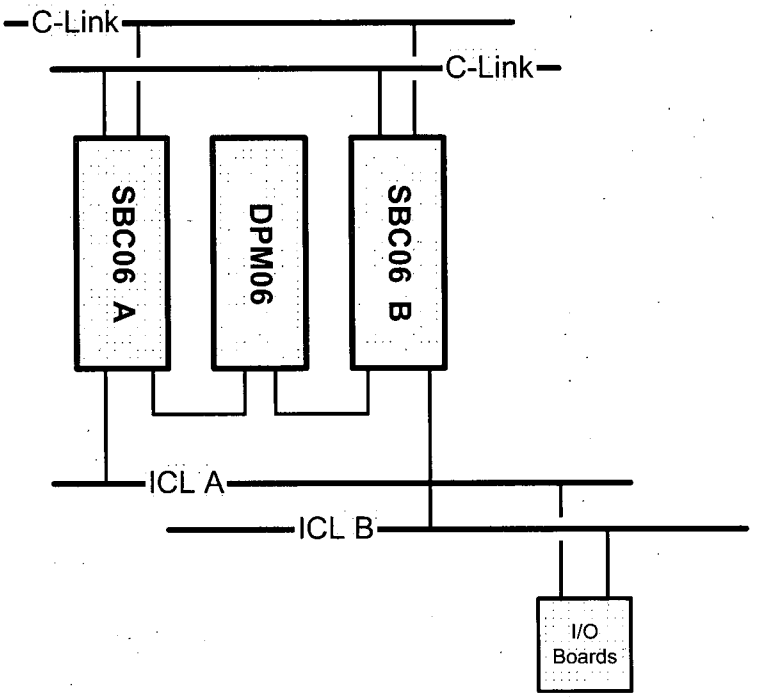

Figure 2. Redundant HFC-SBC06 Boards with DPM06 Board

During redundant operation, the Primary controller periodically copies application and system status data to dual ported memory (DPM) contained on the DPM06 board. The Secondary controller, on the other hand, periodically validates the status data in the DPM and updates its own record of status data if the data is valid. This DPM Transferring Mechanism keeps the secondary controller updated with a current copy of the primary running status and ensures a smooth transition from one controller to the other in the case of failover. During a failover event when control responsibility switches from the Primary to the Secondary, the Secondary uses the most recent application and system status data as an initial state for starting its control of the system. Starting with an initial state that is one second old or less minimizes disturbances to the plant induced by the controller switch over, and prevents potentially hazardous bumping caused by transfer of control. After switch over is complete, the Secondary, which is now the controlling the plant, switches to operation in the Primary control mode. Additional discussion of the failover mechanism is listed DS001-000-08, Failover Mechanism Component Design Specification.

A Maintenance Failover function is supported to perform regular check on the working status of the secondary controller to make sure it will be able to take over the control when the primary controller fails. A pushbutton on the HFC-DPM06 allows failover to be triggered manually.

As shown in Figure 3, the ICL network for a redundant controller configuration includes four physical serial channels for the redundant controllers: ICL A includes ICL A0 and ICL A1 for controller A; ICL B includes ICL B0 and ICL B1 for controller B. A single controller can have up to 64 I/O boards under its control.

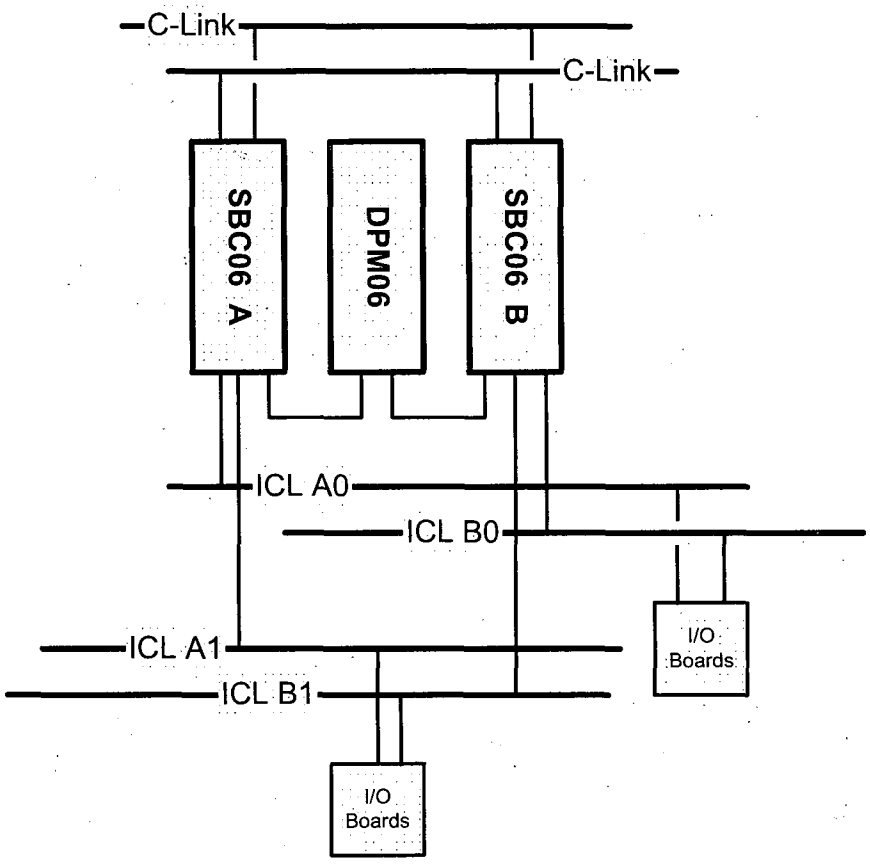

Figure 3. ICL Network for Redundant Controller Configuration

The HFC-SBC06 board may also be configured as a non-redundant System Controller. In a non-redundant of configuration, a single HFC-SBC06 is installed in slot 12 or 14 of a 19-inch HFC-6000 controller rack, and a DPM06 is installed in slot 13. (If the system uses 23-inch racks, the controller may be in slot 16 or 18, and the DPM 06 be installed in slot 17.) Configuration switches located on the front edge of the DPM06 board are used to setup a number of system configuration parameters. The HFC-SBC06 must access a DPM06 to read the configuration settings as part of its initialization process.

Another difference between a redundant and non-redundant configuration is that a non-redundant HFC-SBC06 configuration only supports a non-redundant ICL network, as shown in Figure 4 instead of the redundant ICL network shown in Figure 3.

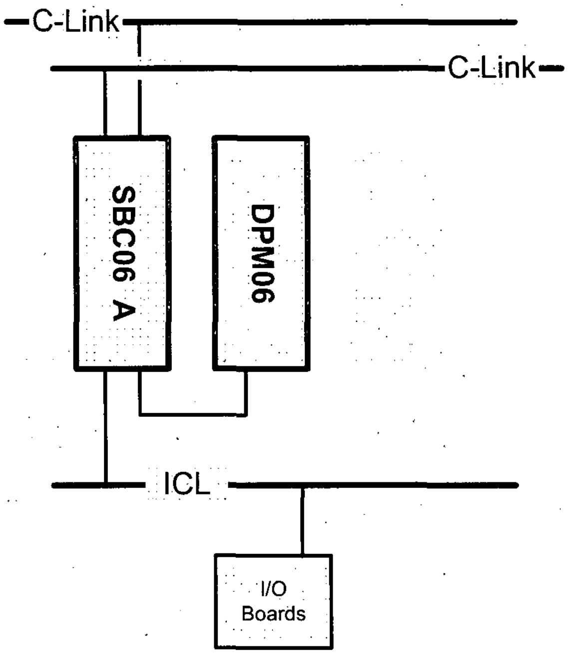

Figure 4. Non-Redundant HFC-SBC06 Board and DPM06 Board

2.3 Execution of Application Programs

The primary function of the HFC-SBC06 System Controller board is to provide control of the plant system actuators based upon the values of system inputs collected from plant field sensors. Control logics, such as arithmetic calculations and logical operations, operate upon field input values to provide control output values that drive plant actuators, operator status displays, and alarm indicators. These control logics are defined in an Application Program, which is installed in the PROM or flash memory in the HFC-SBC06 System Controller. It is transferred to the RAM during power up initialization, and the program is executed during operation of the controller.

Refer to DS001-000-002, Equation Interpreter Component Design Specification, and DS001-000-003, CQ4 Blocks Component Design Specification, for detailed descriptions of control logic algorithms. Refer to UG004-000-01, EWS User's Guide for detailed information about the structure of application program code.

3. Module Architecture

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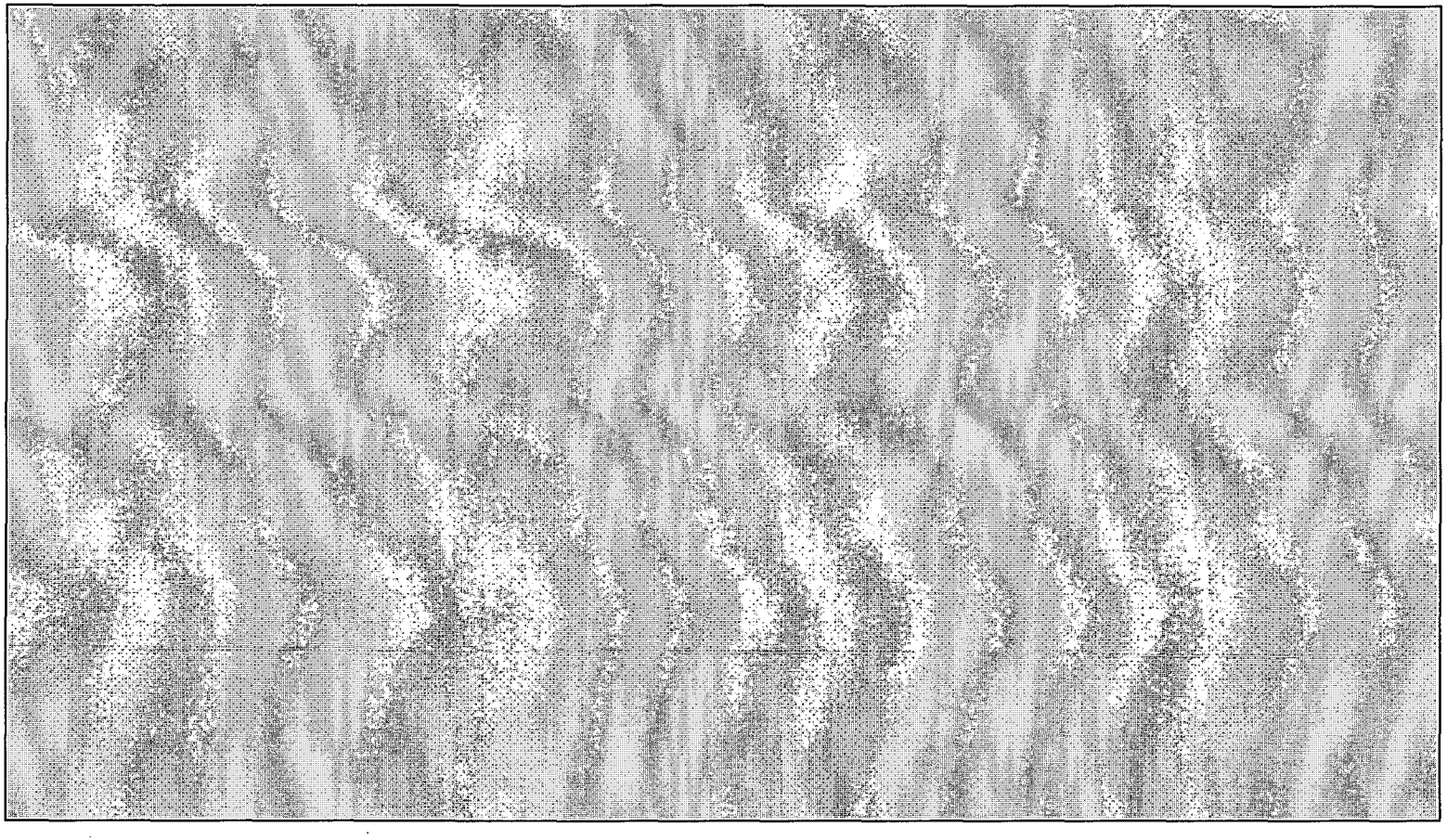

Figure 5. HFC-SBC06 / DPM06 Module Architectures

3.1 Memory Mapping Structure

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Figure 6. Microprocessor Address Space

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3.2 Public Memory Data

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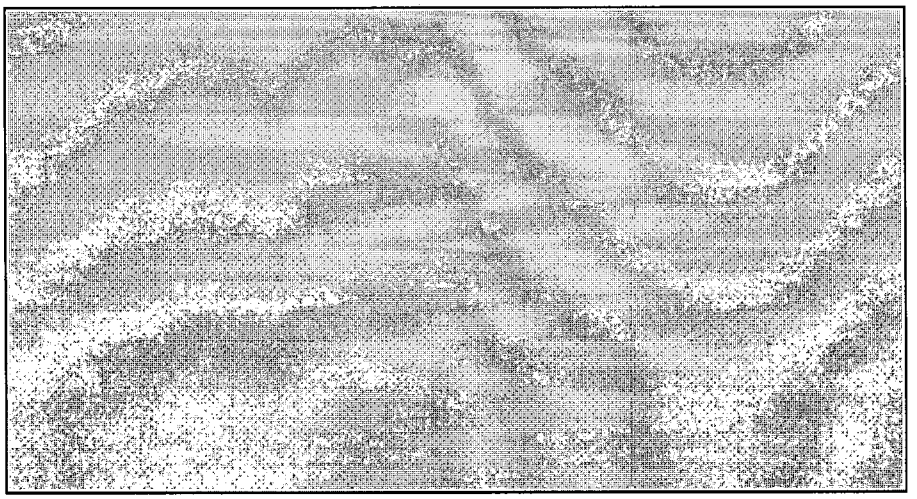

Figure 7. Public Memory Data Stores

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3.3 Remote Communication Architecture

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Figure 8. DDB Broadcast Data Paths

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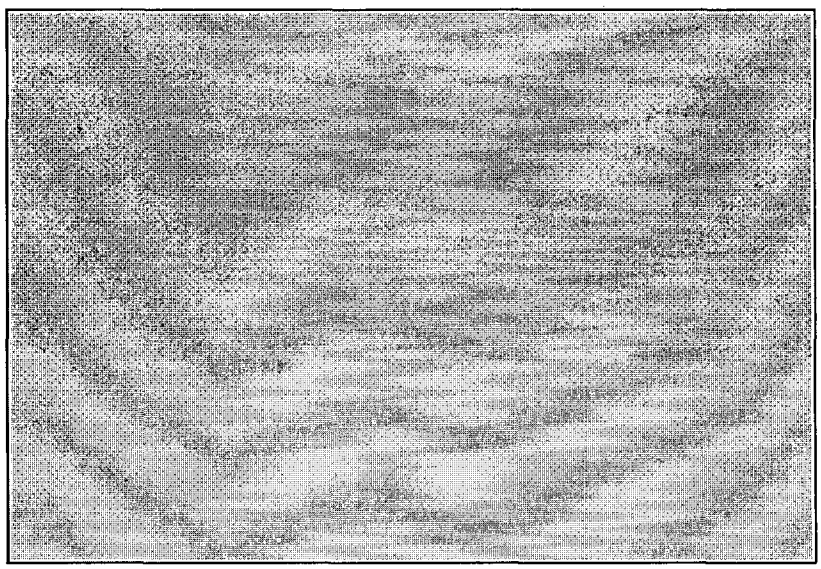

Figure 9. UCP Point-to-Point Message Path

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3.3.1 HFC-SBC06 Handling of DDB Data

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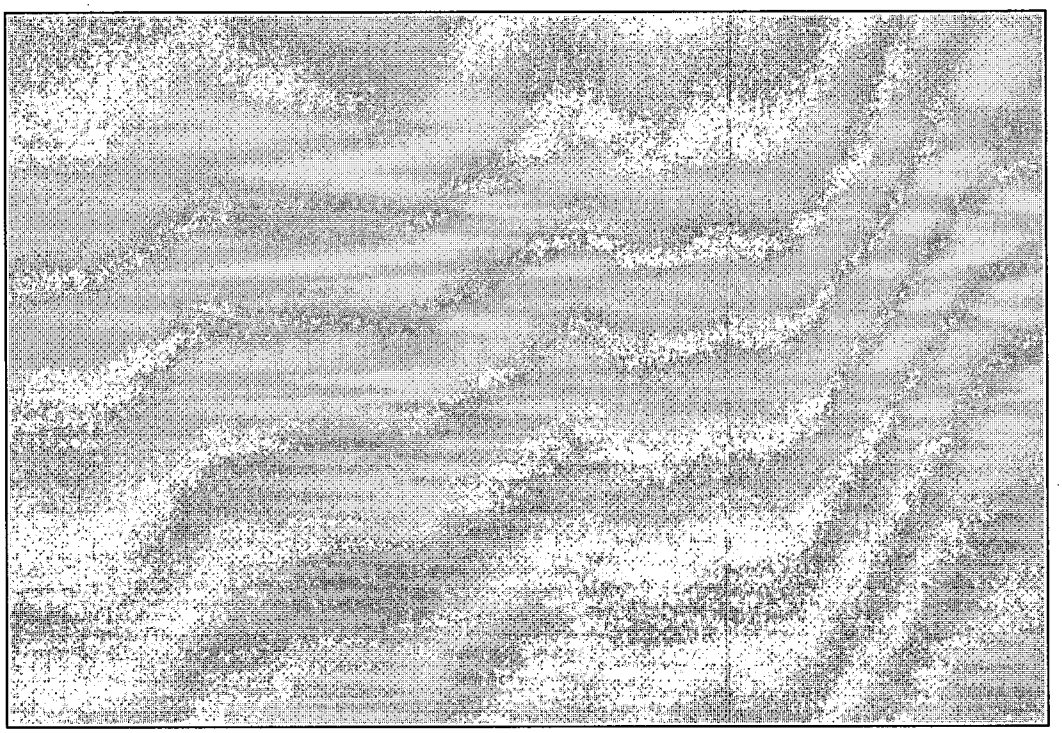

Figure 10. Broadcasting and Filtering of DDB Data

3.3.2 HFC-SBC06 Handling of UCP Messages

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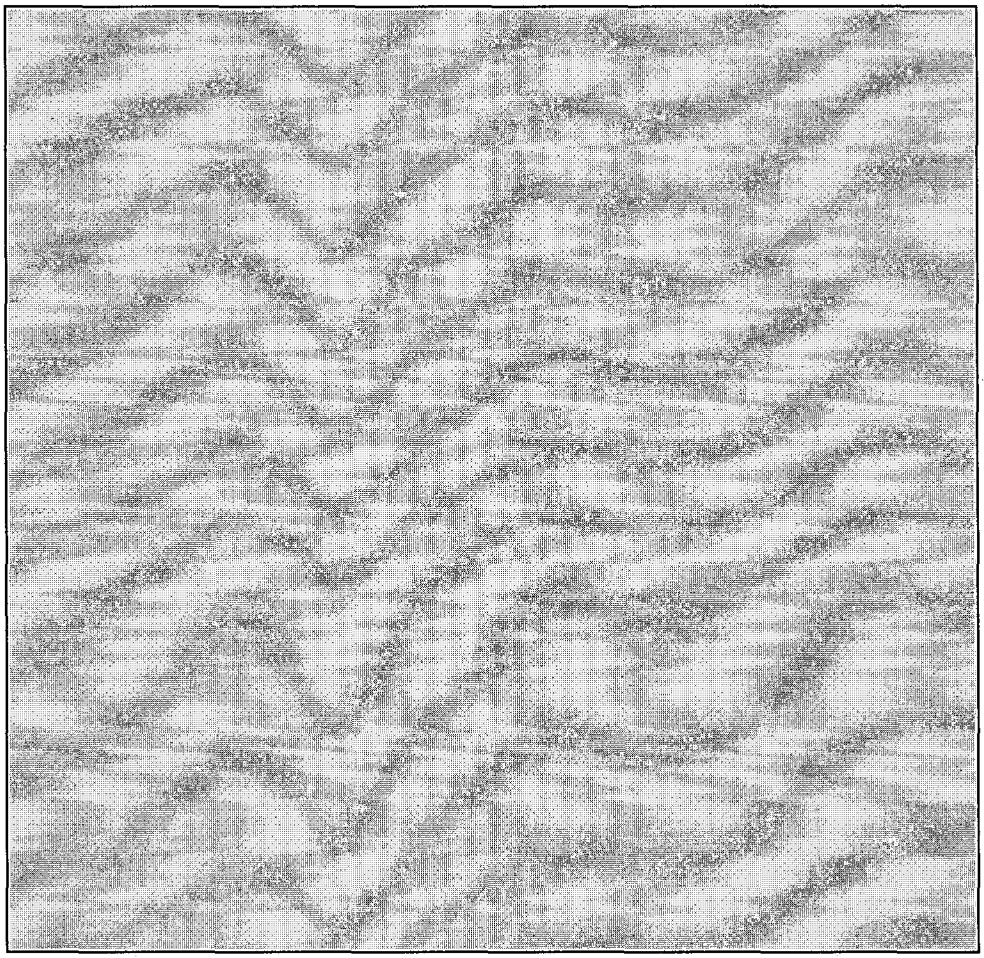

Figure 11. UCP Message Processing

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3.4 SYS Processor Section

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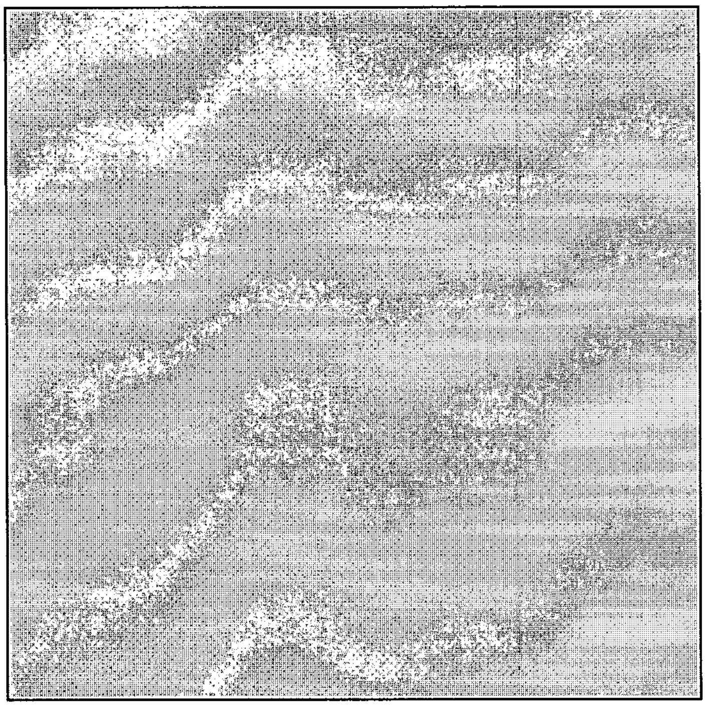

Figure 12. System Processor Architecture

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3.4.1 SYS Processor Software Architecture

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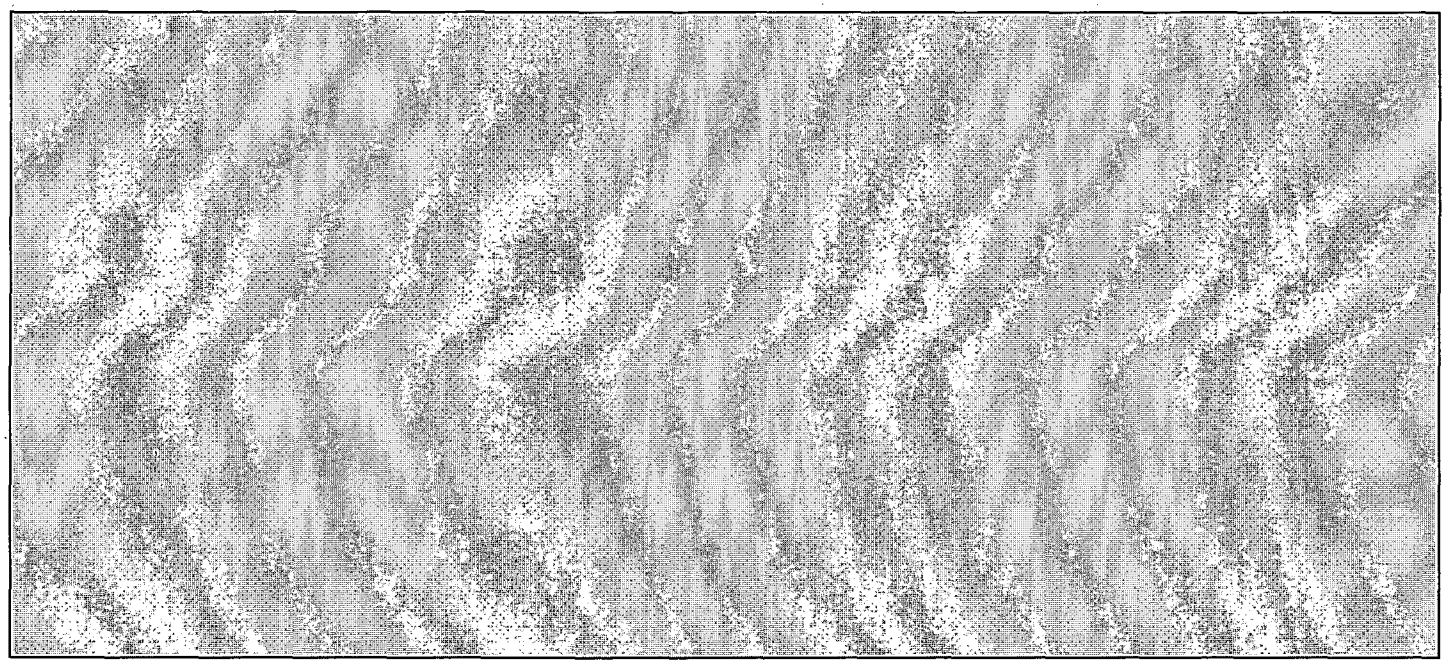

Figure 13. System Software Architecture

The tasks running on the SYS processor are:

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3.5 ICL Processor Section

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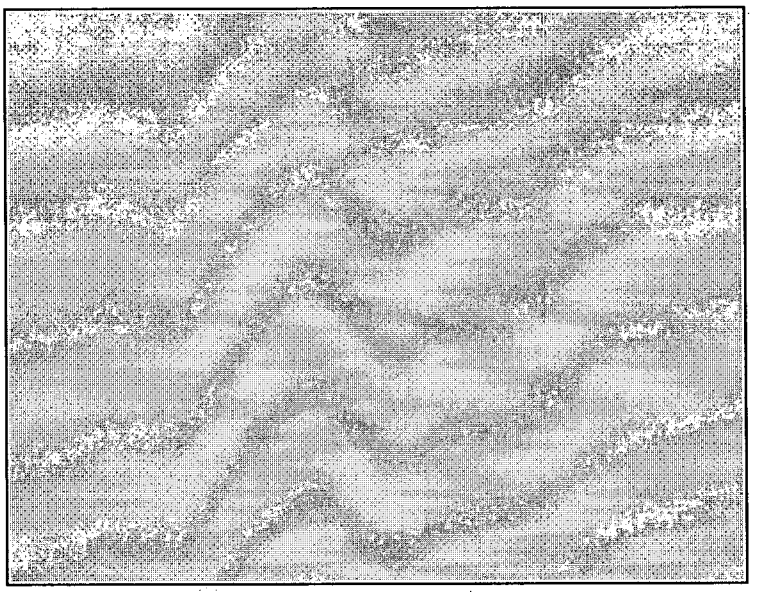

Figure 14. ICL Processor Architecture

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3.5.1 ICL Software Architecture

The ICL Processor software consists of the following routines:

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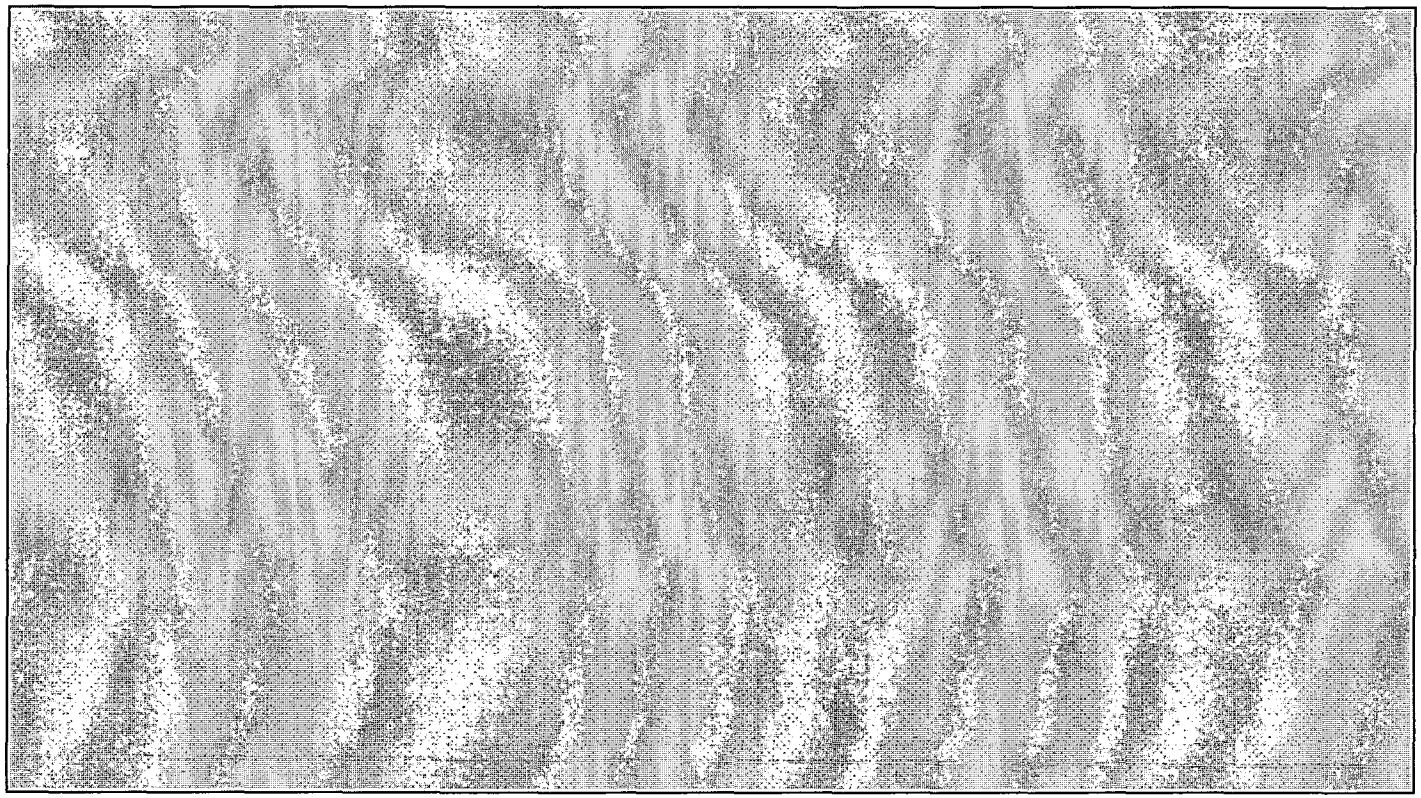

Figure 15. ICL Software Architecture

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3.6 CPC Processor Section

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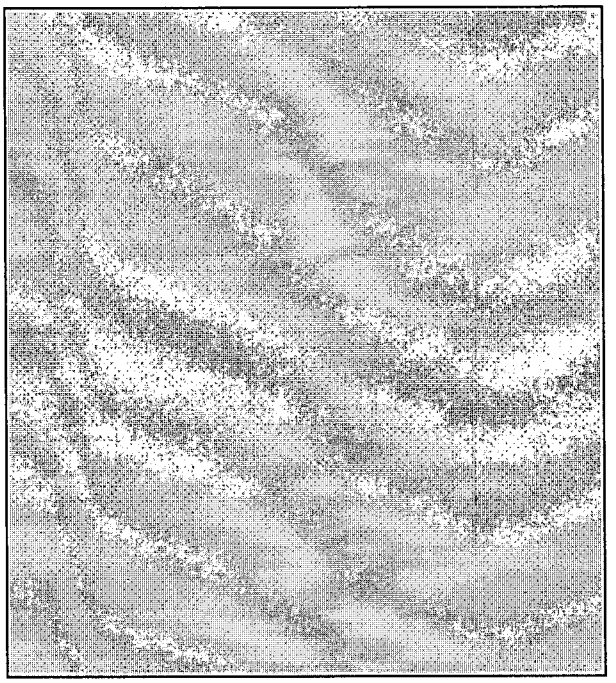

Figure 16. CPC Processor Architecture

3.6.1 CPC Processor Software Architecture

The CPC Processor Software consists of the following routines:

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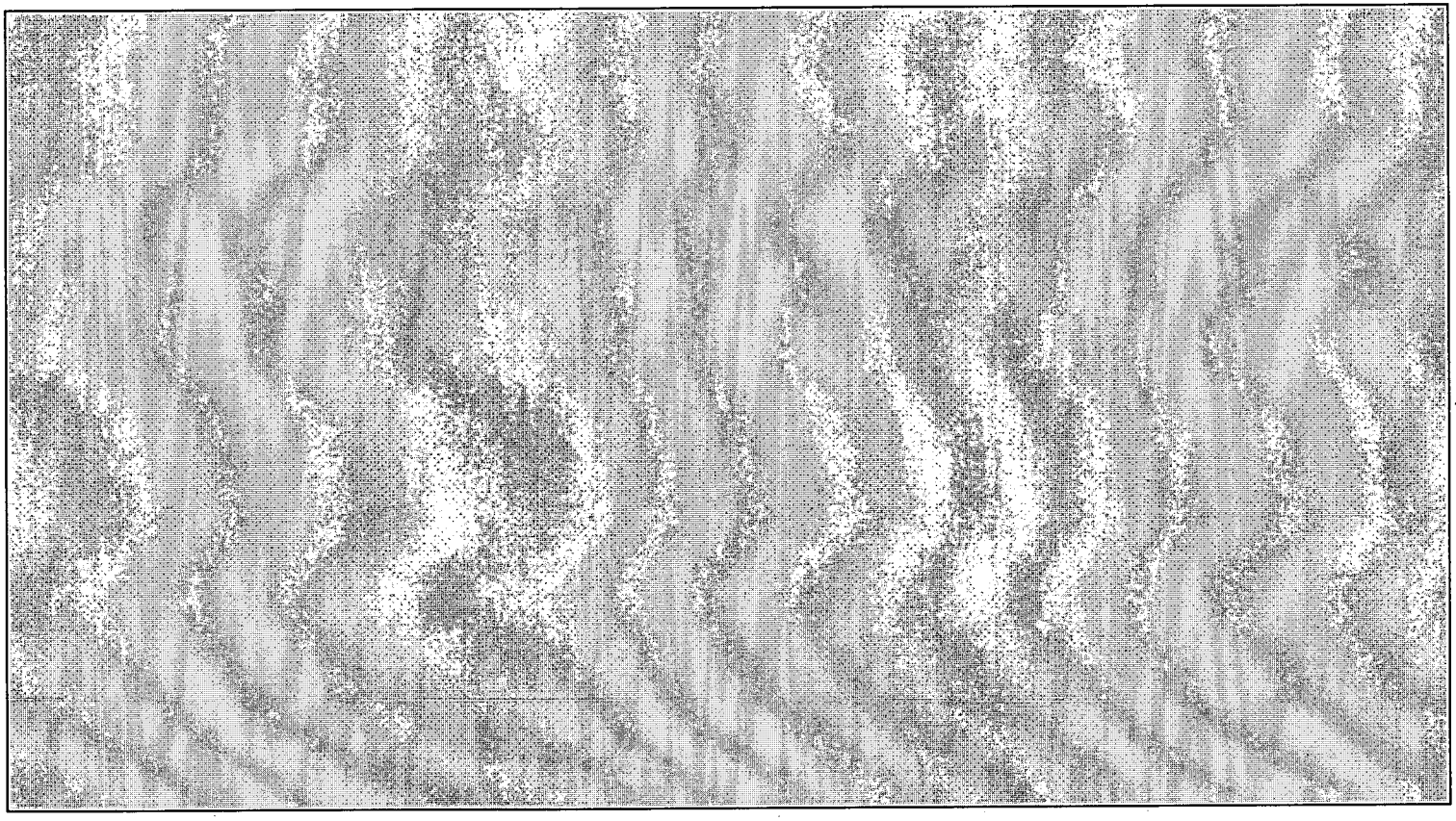

Figure 17. CPC Software Architecture

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3.7 HFC-SBC06 and HFC-DPM06 Redundancy Architecture

Refer to Section 2.2 for descriptions of Redundant System Controllers. Two HFC-SBC06 boards and a HFC-DPM06 board in the redundant configuration are installed in the three leftmost slots of the HFC-6000 controller rack, with the DPM06 board installed between the two HFC-SBC06 boards. The three boards include hardware and software designed to support redundant controller operation. The main functions of the redundant architecture are as follows:

- Logic to determine controller operation mode: Primary or Secondary
- Failover mechanism on failure of primary controller
- Manual maintenance failover
- Controller failure detection mechanism
- Mechanism to ensure a smooth transition of control during failover

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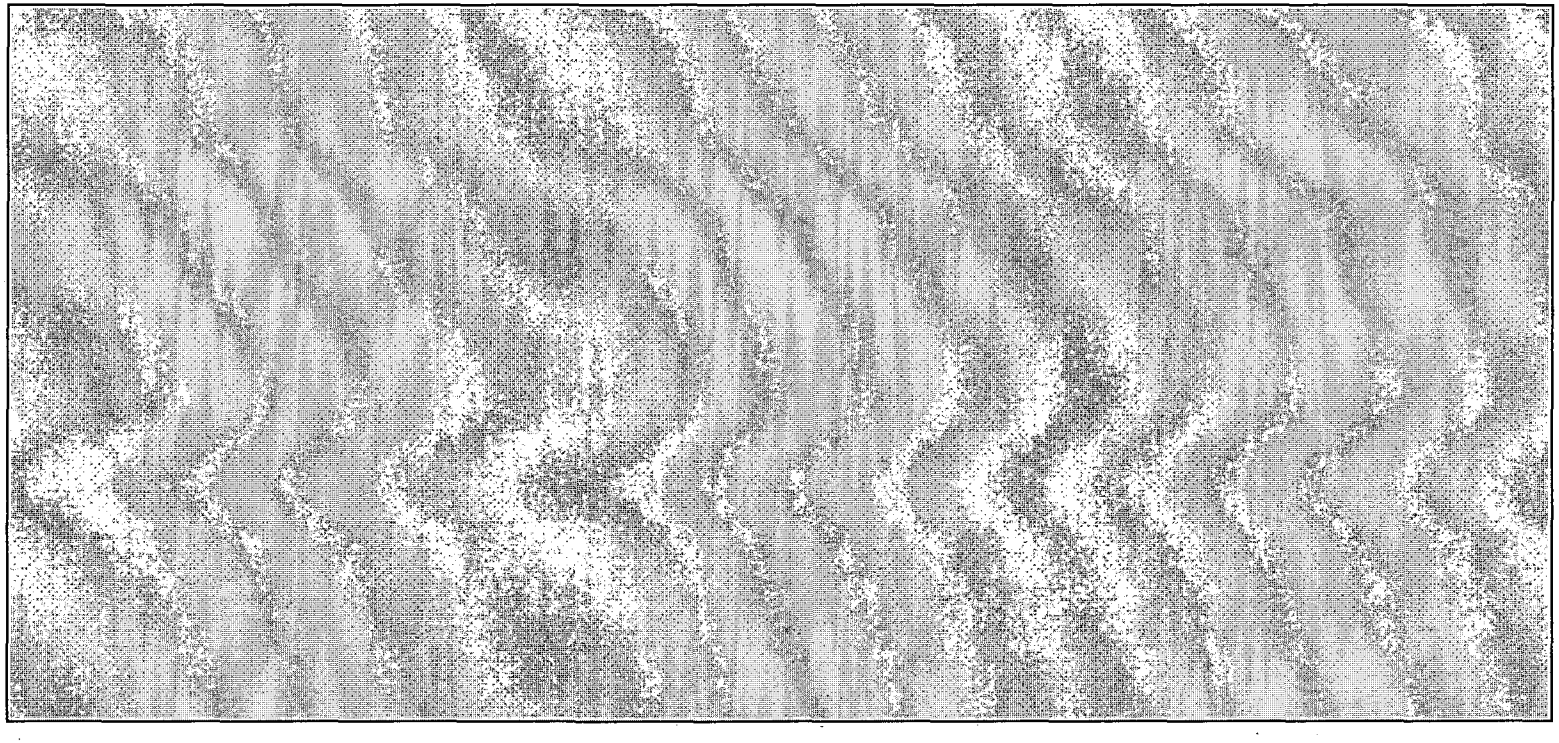

Figure 18. HFC-SBC06 Redundancy and Failover

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3.8 HFC-SBC06 CPLD Design

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3.9 Sequence of Events Timer

The HFC-SBC06 system controller maintains a Sequence of Events (SOE) timer over 24 consecutive hours of operations. The SOE timer is used for "time tagging" events that occur system wide. This timer can be synchronized by some master SOE timer located elsewhere in the system, or can be the master timer itself. The SOE timer provides a resolution of 100 μS for synchronizing similar SOE timers on each I/O boards.

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3.10 HFC-DPM06 Board

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4. Configuration Setup and LED Displays

The HFC-SBC06 board contains one 8-position DIP switch, two toggle switches and nine jumpers. The switches and jumpers enable manual control of reset, hardware configuration, and programming of the board. Additional configuration switches are physically located on the HFC-DPM06 common board.

4.1 HFC-SBC06 Onboard Switch Functions

SW1 Power on/off, RESET

SW2 Positioned down (toward the board) permits write cycles to onboard flash memory chips. The switch is placed in this position to program flash memory for the ICL and CPC processors and to download the application program to the flash memory of the SYS processor.

Positioned away from the board enables a write-protect function for flash memory. For safety-related applications, the switch should remain in this position for normal operation.

SW4 8-position DIP switch defines operating modes and control parameters as indicated in Table 1.

Table 1. SYS Processor Configuration Switches

Switch	Function
SW4-1 SW4-2	XXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXX XXXXXXXXXXXX
SW4-3	XXXXXXXX
SW4-4	XXXXXXXX
SW4-5	XXXXXXXX
SW4-6	XXXXXXXX
SW4-7	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
SW4-8	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

4.2 HFC-DPM06 Onboard Switch Functions

Three eight-position DIP switches on the DPM common board control values for the following parameters:

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4.3 HFC-SBC06 Onboard Jumper Options

Table 2 defines the function of each jumper included on the HFC-SBC06 controller.

Table 2. Jumper Options

Jumper	Function
J1	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
J8	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
W2	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
W3	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
W5	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
W6	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
J5	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
E1, E2	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

4.4 LEDs

The HFC-SBC06 board contains eight board-edge LEDs, which provide a visual indication of functional status of the controller hardware and software. The HFC-DPM06 board contains five board-edge LEDs, which provide a visual indication of functional status of the controller.

4.4.1 HFC-SBC06 LED Functions

DS1 Includes four LEDs to indicate hardware status of the Ethernet interface as follows:

- DS1-1 flashes on for approximately 50 ms when C-Link channel 1 transmits in TPI mode.
- DS1-2 flashes on for approximately 50 ms when receive data is detected for C-Link channel 1 in TPI mode.
- DS1-3 flashes on for approximately 50 ms when C-Link channel 0 transmits in TPI mode.
- DS1-4 flashes on for approximately 50 ms when receive data is detected for C-Link channel 0 in TPI mode.

DS2 Includes four LEDs . Two LEDs are controlled directly by the P1.6 and P1.7 ports of the ICL microprocessor, and two are controlled by the corresponding ports of the CPC microprocessor.

DS3 and DS4 Includes 8 LEDs controlled by the SYS Processor. Refer to Section 4.4.1.1.

4.4.1.1 DS3 and DS4 LEDs

If the SYS processor detects a failure condition during system initialization/reset, the display freezes with the LEDs displaying a binary code for that fault. Table 3 lists the defined error codes and the error conditions that they represent. Throughout normal operation, the LED display represents a binary code for different processor tasks, and the LED code for a particular task lights while it is running. As a result, all 16 LEDs flicker constantly during this phase of operation. The bottom LED is always on when the board is running normally. Table 4 lists the defined task LED code. If the board detects a failure condition during normal operation, the display freezes with the LEDs displaying a binary code for that fault. Table 5 lists the defined error codes and the error conditions they represent.

Table 3. DS3 and DS4 LED Indications for Initialization Failure

Code	Error Condition
01_H	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXX
02_H	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXX
03_H	XXXXXXX
04_H	XXXXXXX
05_H	XXXXXXX
06_H	XXXXXXX
07_H	XXXXXXX
08_H	XXXXXXX
09_H	XXXXXXX
$0A_H$	XXXXXXX
$0B_H$	XXXXXXX
$0C_H$	XXXXXXX
$0D_H$	XXXXXXX
$0E_H$	XXXXXXX
$0F_H$	XXXXXXX
10_H	XXXXXXX
11_H	XXXXXXX
12_H	XXXXXXX
13_H	XXXXXXX
14_H	XXXXXXX
15_H	XXXXXXX
16_H	XXXXXXX
17_H	XXXXXXX
18_H	XXXXXXX
19_H	XXXXXXX
$1A_H$	XXXXXXX

Table 4. DS3 and DS4 LED Indications for Individual Tasks

Bit	Hex	Task
0	1_H	XXXXXXX
2	4_H	XXXXXXX XXXXXXXXXXXXXX
3	8_H	XXXXXXX
5	20_H	XXXXXXXXXXXX
6	40_H	XXXXXXXXXXXX
7	80_H	XXXXXXXXXXXX
9	200_H	XXXXXXXXXXXX
10	400_H	XXXXXXXXXXXXX
11	800_H	XXXXXXX
15	8000_H	XXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXX XXXXXXXXXX
Other	Other	XXXXX

Table 5. DS3 and DS4 LED Failure Indications During Normal Operation

Code	Error Condition
01_H	XXXXXXX
02_H	XXXXXXX
03_H	XXXXXXX
04_H -10_H	XXXXXXX
11_H	XXXXXXX
12_H	XXXXXXX
13_H	XXXXXXX
14_H	XXXXXXX
15_H	XXXXXXX
Note: All processor failure codes are defined, but they are functional only if that processor is configured for the control system.	

4.4.2 HFC-DPM06 LED Functions

DS1 Lights when the maintenance failover function is available (controller A and controller B both sane).

DS2 Lights when controller A is primary.
DS3 Lights when controller A is sane.

DS4 Lights when controller B is primary.
DS5 Lights when controller B is sane.

4.5 Installation of System Software and Application Programs

Each of the three onboard processors has a dedicated flash memory and a dedicated PROM for system software. SYS processor also has a dedicated flash memory for its application program code. Switch and jumper selections on the board cause the processor to boot from either the PROM or the flash memory.

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4.5.1 System Code Transfer to Flash

Initially, the flash memory chips are blank. The following steps describe the procedural sequence required to transfer system software code to each of the onboard flash memory chips.

1. Install jumper J1 to enable the SYS processor to boot from its system code PROM.

2. Install the PROM containing system software for the SYS processor in socket U52.

3. Set DIP switch SW4-8 in the ON (toward the board) position.

4. Install jumper J8 to enable the ICL and CPC processors to boot from their system code PROMs.

5. Install the PROM containing the system software for the ICL processor in socket U7.

6. Install the PROM containing the system software for the CPC processor in socket U8.

CAUTION

Make sure that S1 is positioned toward the board before installing it in the board rack. If SW1 is positioned away from the board and power is applied to the rack, power transients could damage components on the board.

7. Mount the board in a controller slot of the HFC-6000 controller board rack.

8. Ensure that power is applied to the board rack, and position S2 toward the board to enable write cycles to flash memory.

9. Ensure that power is applied to the board rack, and position SW1 away from the board.

10. Following application of operating power, the system software will be transferred from U52 to the flash memory for the SYS processor. Successful transfer will be indicated by the following:

    - LED01 lights for several seconds and then goes out.
    - LED00 through LED07 light in sequence.

11. The system software for the ICL and CPC processors should be transferred to flash memory.

NOTE

> As long as J1 remains installed, the SYS processor will boot from the PROM installed in socket U52. That code will be compared with the code currently in flash memory; and if it is different, the contents of PROM will be transferred to flash memory and the processor will operate from that code. If J1 is removed, the SYS processor will boot from the flash memory without examining the contents of its PROM.
>
> As long as J8 remains installed, the ICL and CPC processors will boot from their respective PROMs. If SW2 is positioned as write enable, the contents of the PROMs will also be transferred to the flash memories for the two processors.

12. After the installation of the system software to flash, do the following:

    - Remove jumper J1.
    - Set DIP switch SW4-8 OFF (away from the board).
    - Leave jumper J8 installed (for current software design).

4.5.2 Application Code Download

The application program codes can be compiled by an EWS workstation software and downloaded to the controller over the C-Link. This download can be repeated following any modification or update to the application code during application development; however, the download function should be disabled during normal operation to prevent inadvertent changes to the application.

1. Set S1 toward the board to remove power from the board.

2. DIP SW4 can be set to place the software in offline mode (SW4-1 ON and SW4-2 OFF). While operating in this mode, the system software runs normally, but the equation interpreter task does not run.

3. Set S2 toward the board to enable flash write cycles.

4. For redundant controllers, set SW4-5 ON.

5. For redundant controllers, repeat steps *1* through *4* for the second controller.

6. Set S1 away from the board to enable distribution of operating power on the board (both controllers for redundant configurations).

7. At the EWS workstation, compile the final application code for the controller.

8. Download the equations, RQ file, and CQ4 blocks, as applicable.

9. For redundant controllers, initiate failover to the secondary controller.

10. Download the equations, RQ file, and CQ4 blocks as applicable.

11. Set S2 away from the board to disable flash memory write cycles.

12. If the controller was placed in offline mode, power down the controller and set both SW4-1 and SW4-2 OFF to enable normal operation. Power the controller up to enable controller operation to begin.

4.5.3 System Software Updates

If an upgrade is provided for the system software of one or more processors on the controller board following installation, repeat the procedure described ion paragraph 4.5.1. Direct download of system programs code to flash memory is not presently supported.

4.6 Hardware Configuration

Refer to Tables 1 and 2 for a general definition of functions controlled by the onboard switches and jumpers. The following steps identify typical switch and jumper settings required for normal operation. Record the specific DIP switch settings required for each controller to be used in the system.

CAUTION

Make sure that S1 is positioned toward the board before removing or installing the board in the board rack. If SW1 is positioned away from the board and power is applied to the rack, power transients could result in damage to components on the board.

1. Set SW4-1 and SW4-2 on the HFC-SBC06 board both in the open position. This configuration enables normal run mode for the system software.

2. If the controller is used as part of a redundant pair, set SW4-5 closed. This enables regular transfers of status from the primary to the secondary via the HFC-DPM06 array.

3. Set SW4-6 closed. This enables the sanity function.

4. Set SW4-7 and SW4-8 both open. This disables software downloads from the EWS workstation.

5. Set DIP switches on the HFC-DPM06 board to provide the following configuration parameters:

   - Set SW2 to the binary value for the remote number assigned to this controller. The valid range is from 0 to 255.

   - Set SW4 to the binary value for the total number of remotes configured for this system (up to 255).

   - Set SW1 to the binary value for the sequence number of this remote on the C-Link. The valid range is from 0 to 31.

CAUTION

The remotes must be configured on the C-Link in numeric sequence with the HIFR assigned the sequence number of 0. If any remote is installed out of sequence, reliable communication with that remote over the C-Link could be disrupted.

6. When the HFC-SBC06 board is used as a redundant controller, a jumper should be installed from node J5–1 to J5–2. This hardware interlock requires the controller chassis to complete its power up initialization sequence successfully (SANE status TRUE) and become the primary controller before the ICL processor can begin transmitting over its serial link. Removing all jumpers results in a configuration in which the transmit interface remains enabled as long as logic power is present.

5. Module Design Constraints

The following is a list of specifications that constraint the design of an HFC-SBC06 board module.

5.1 Communication Interface Specifications

- Document DS002-000-01, C-Link Protocol Component Specification
- Document DS002-000-02, ICL Protocol Component Specification
- Document DS002-000-03, UCP Protocol Component Specification

5.2 Operating System Specification

- Document DS001-000-01, Operating System Component Design Specification
- Document DS001-000-02, Equation Interpreter Component Design specification
- Document DS001-000-03, CQ4 Component Design Specification
- Document DS001-000-06, System Component Design Specification
- Document DS001-000-07, Job Component Design Specification
- Document DS001-000-08, Failover Mechanism Component Design Specification

5.3 Hardware Interface Specifications

- Document 40040901, HFC-BPC01-19 Backplane Specification
- Document 40041401, HFC-BPE01-19 Backplane Specification
- Document DS901-000-34, HFC-BPC01-23 Backplane Specification
- Document DS-901-000-35, HFC-BPE0-23 Backplane Specification
- Document DS-901-000-36, HFC-BPC02-23 Backplane Specification
- Document DS-901-000-37, HFC-BPC02A-23 Backplane Specification
- Document DS901-000-38, HFC-BPC03-23 Backplane Specification

5.1 Design Safety

5.4.1 Main Processor – SC Code

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5.4.1.1 Criticality

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5.4.1.2 Hazard

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5.4.1.3 Security

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5.4.1.4 Risk

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5.4.2 ICL Processor – SAP Code

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5.4.2.2 Hazard

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5.4.2.3 Security

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5.4.2.4 Risk

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5.4.3 C-Link Processor – SEP Code

5.4.3.5 Criticality

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5.4.3.6 Hazard

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5.4.3.7 Security

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5.4.3.8 Risk

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HF Controls Corporation

HFC-6000 Product Line

I/O Module
Design Specification

MS901-000-02

Rev C

INFORMATION ONLY

Effective Date	1/29/2009
Author	Gregory Rochford
Reviewer	Pat Thibodeau
Approval	David Briner

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Revision History

Date	Revision	Author	Changes
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11/18/03	A	B Han	Review comments incorporated
2/23/07	B	J Taylor	SCR 1766
1/27/09	C	G Rochford	Review comments incorporated

Table of Contents

1. INTRODUCTION 4

2. FUNCTIONAL DESCRIPTION 5

3. MODULE ARCHITECTURE 6

3.1 I/O BOARD ARCHITECTURE 6
3.2 ADDRESS SPACE ARCHITECTURE 9
3.3 SOFTWARE ARCHITECTURE 10
3.3.1 X86 SOFTWARE ARCHITECTURE 11
3.3.2 DSP ASSEMBLY SOFTWARE ARCHITECTURE 13
3.3.3 FAULT DETECTION AND PROCESSING 16
3.4 ONBOARD SWITCHES, JUMPERS, AND LEDS 16

4. MODULE DESIGN CONSTRAINTS 17

4.1 COMMUNICATION INTERFACE SPECIFICATIONS 17
4.2 DETAILED DESIGN SPECIFICATIONS 17

5. DESIGN SAFETY 17

5.1 COMMON MODULES 17
5.1.1 SECURITY 18
5.1.2 RISK 18
5.2 OUTPUT MODULES 19
5.2.1 CRITICALITY 19
5.2.2 HAZARD 19
5.2.3 RISK 20

5.3 INPUT MODULES 21
5.3.1 CRITICALITY 21
5.3.2 HAZARD 21
5.3.3 RISK 22

Figure 1. HFC-6000 System Hierarchy 4
Figure 2. HFC I/O Board Module Architecture 7
Figure 3. ICL Communication Architecture 9
Figure 4. I/O Board Software Architecture 11

Table 1. List of HFC-6000 I/O Boards 6

1. Introduction

The HFC-6000 distributed control system provides plant monitoring and control capabilities with monitoring and control responsibilities spread over multiple remote control units. The I/O boards are sensors and drivers for implementing plant control functions. They provide signal-level interfaces to the equipment and devices in the plant. As shown in Figure 1, an HFC-6000 I/O board is positioned in the HFC-6000 system hierarchy between the HFC-SBC06 System Controller(s), which is the CPU of HFC-6000 system, and the equipments and devices in the plant.

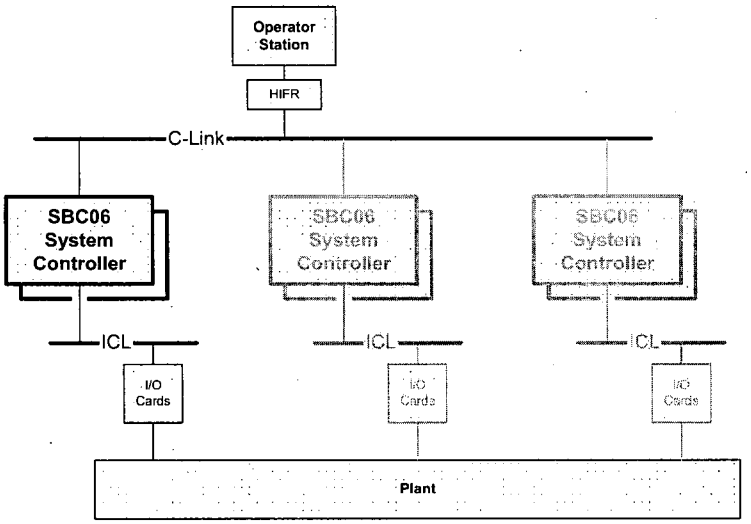

Figure 1. HFC-6000 System Hierarchy

Descriptions and discussions of the functional requirements of the HFC-6000 I/O boards are provided in 700901-06, *HFC-6000 Product Line General I/O Card Requirements Specification.*

Subsequent sections of this document provide top-level architectural and design descriptions of HFC-6000 I/O boards. Two different designs are currently in use. In general, the digital I/O boards employ a common processor kernel based on an Intel microprocessor. The assemblies with AI channels use a Digital Signal Processor (DSP) to control the main processing functions. Both designs provide a common architecture that is used on multiple assemblies. Lower level descriptions of each I/O board are contained in a separate Detailed Design Specification for each board type. The design descriptions of the common software modules and the common hardware characteristics are covered in the individual *HFC-6000 I/O Board Module Detailed Design Specifications.* The purpose of this document is to present the methods and strategies used to accomplish the operation and functions required of an HFC-6000 I/O board. The discussion of the operation and function of an HFC-6000 I/O board are presented using architectural, design, and implementation information.

2. Functional Description

This section describes the major functions performed by both design implementations of HFC-6000 I/O boards. The functional descriptions are presented to provide a context for understanding the internal operation of an HFC-6000 I/O board and how the functions performed by an HFC-6000 I/O board work within the overall architecture of the HFC-6000 distributed control system.

The major functions performed by an HFC-6000 I/O Board are:

- Initialization
- Communication with system controller connected to an Inter-Communication Link (ICL)
- Setting each digital/analog output channel using digital output images, and/or getting digital input images from each digital/analog input channel
- Self diagnostics functions

An I/O board generally has two operation stages: Initialization state and Normal Operation state. Upon power up or reset, the processor firmware will accomplish initialization for hardware, software, and communication set up. During initialization, some self diagnostics tests will be performed, such as RAM Write/Read test and EPROM/flash checksum test. Any error detected at this state is fatal and will cause the software to halt execution.

After completing initialization, the board will enter the Normal Operation stage. During normal operation, the I/O board handles communication with the HFC-SBC06 controller and performs an I/O scan at regular intervals to set digital/analog output channels and/or read digital/analog input channels. An HFC-6000 I/O Board can have digital input channels, digital output channels, analog input channels, and/or analog output channels connected to the field devices and equipments. An I/O board having output channels receives digital images for output channels from an HFC-SBC06 system controller at regular intervals, and then it uses this data to control each output channel. An I/O board with input channels reads the input image for each channel and sends the images of the digital or analog inputs to the HFC-SBC06 system controller at regular intervals.

A communication interface connects an I/O board to the ICL, which is an HFC proprietary, RS-485 serial network connecting the I/O boards to the HFC-SBC06 controller. Input values from plant field devices and output values for plant actuators are transferred between the HFC-SBC06 and I/O boards over the ICL. In addition, each HFC-6000 I/O board maintains internal diagnostic status and can report that status to the HFC-SBC06 controller.

During the time between successive I/O scans, the I/O board performs its self-diagnostics functions, which are mainly RAM tests. If any error is detected by the self-diagnostics tests, the I/O board will re-enter initialization stage to perform a restart.

How an I/O board scans its I/O channels and the specific content of message exchanges with the HFC-SBC06 vary with board type and channel configuration. Table 1 provides a list of

standard HFC-6000 I/O board types and a description of the I/O channels for each board type. Designs of HFC-6000 I/O board types having unique functions or a limited applicability will be covered in separate specifications.

Table 1. List of HFC-6000 I/O Boards

Name	I/O Channels
DO8J	8 channel relay output
DO16C	16 channel solid-state output
DO16J	16 channel relay output
DI16I	16 channel digital input
DC33	2 120-vac digital output and 12 digital input
DC34	2 125-vdc digital output and 12 digital input
DC35	1 120-vac digital output with seal-in circuit and 12 digital input
AI16ED	16 analog input, 0- to 10-v (DSP)
AI16FD	16 analog input, 4- to 20-mA (DSP)
AO8F	8 analog output, 4- to 20-mA
AO8FD	8 analog output, 4- to 20-mA (DSP)
AC36D	4 analog input, 4 analog output (DSP)
AI8LD	8 channel E-type thermocouple input (DSP)
AI8MD	8 channel 100Ω RTD input (DSP)
AI4K	4 channel pulse input

The architecture of each HFC-6000 I/O board has been developed to support the functions that the board is required to perform. The following sections provide descriptions of the architecture and design of an HFC I/O board and discuss details of the functions performed by an HFC-6000 I/O board.

3. Module Architecture

3.1 *I/O Board Architecture*

The HFC-6000 product line currently includes two different hardware designs for I/O assemblies. One uses an Intel microprocessor as the main controller for the assembly, and the other uses a Digital Signal Processor (DSP) for this purpose. Figure 2 illustrates the major functional characteristics of an HFC-6000 I/O board. Major features of the I/O boards based on the Intel processor are as follows:

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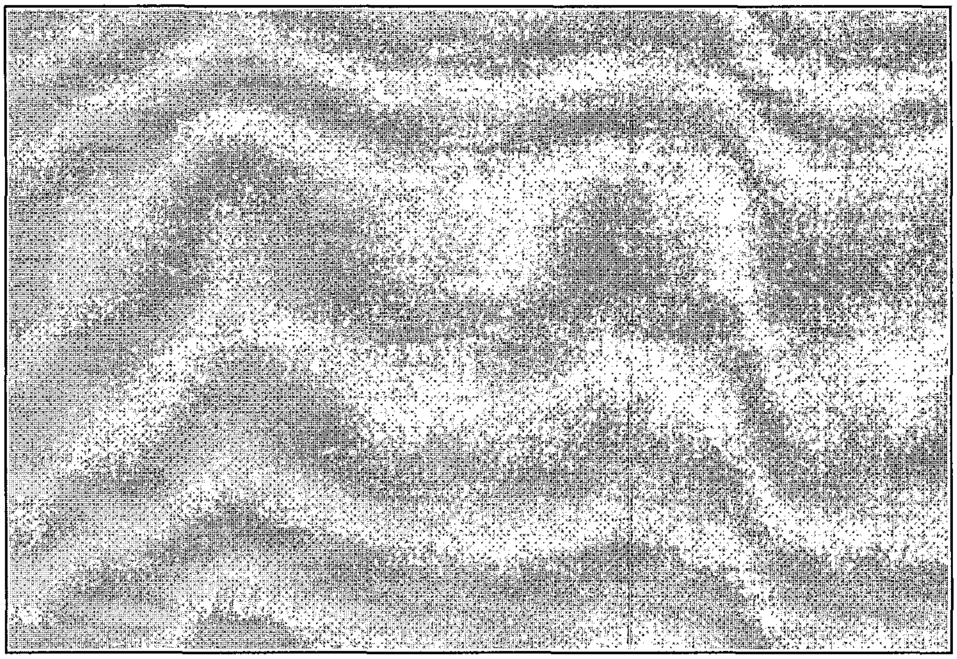

Figure 2. HFC I/O Board Module Architecture

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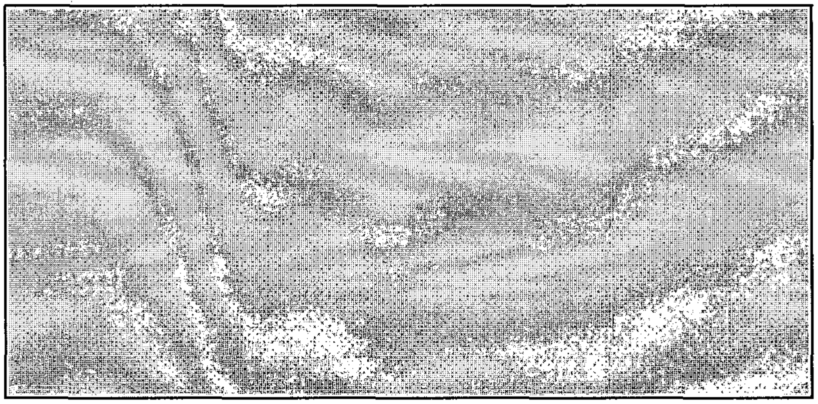

Figure 3. ICL Communication Architecture

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3.2 *Address Space Architecture*

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3.3 *Software Architecture*

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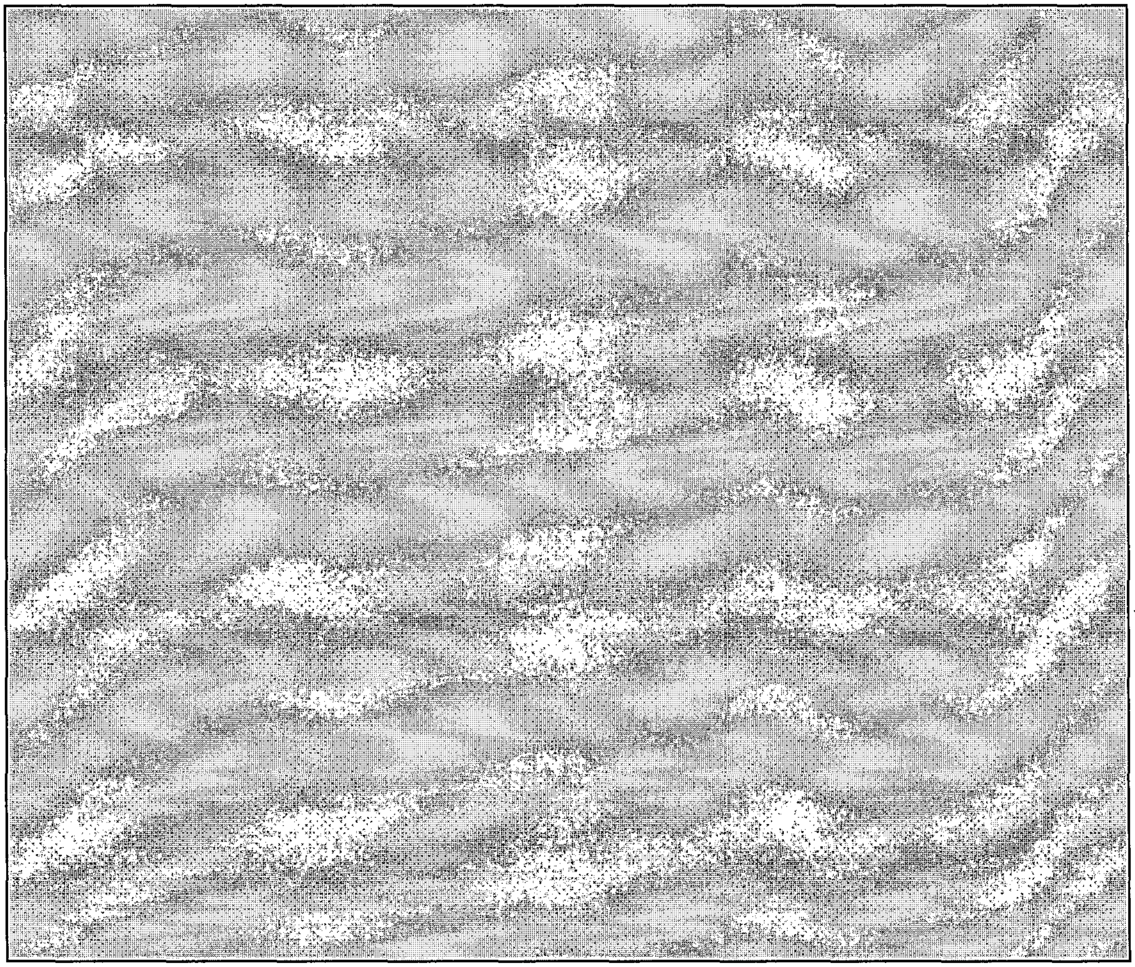

Figure 4. I/O Board Software Architecture

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3.3.1 X86 Software Architecture

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3.3.2 DSP Assembly Software Architecture

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3.3.3 Fault Detection and Processing

During Initialization, the software performs the RAM read/write test and EPROM/flash test to detect any hardware errors in the arrays. Any failure of these tests is fatal and will cause the program to halt execution.

Throughout normal operation, the software performs a RAM read/write self diagnostics test during the idle time between successive I/O scans. Any failure of these tests will cause the program to return to the initialization stage to perform a restart of software.

During communication with the HFC-SBC06 controller, hardware timers will be used to control the communication response time. Any communication timeout will cause the program to go to Communication Setup stage to reconfigure hardware communication channel and re-establish communication with the HFC-SBC06 controller.

3.4 *Onboard Switches, Jumpers, and LEDs*

This section lists the typical switches and board-edge LEDs for a standard HFC-6000 I/O board. An I/O board may include additional switches, jumpers and LEDs depending on board type. The descriptions of specific switches, jumpers, and LEDs for each particular HFC-6000 I/O board are provided in each board's Module Detailed Design Specification.

Assemblies with Intel processor provide the following minimum combination of user controls and indicators.

Reset Switch – Pushbutton switch accessible through the front bezel enables manual reset of the microprocessor and other major hardware components.

A/B LED – Lit when channel A is selected to receive data from the ICL; extinguished when channel B is selected to receive data from the ICL.

TX LED Flashes when the assembly is transmitting to the ICL.

RX LED Flashes when the assembly is receiving data from the ICL.

Assemblies with the DSP provide the following minimum combination of user controls and indicators.

Reset Switch – Pushbutton switch accessible through the front bezel enables manual reset of the microprocessor and other major hardware components.

LINK LED – Lit red when channel A is selected to receive data from the ICL; lit green when channel B is selected to receive data from the ICL.

TX A LEDFlashes when channel A is transmitting to the ICL.

RX A LEDFlashes when channel A is receiving data from the ICL.

TX B LED Flashes when channel B is transmitting to the ICL.

RX B LEDFlashes when channel B is receiving data from the ICL.

Additional indicators are provided on a module-by-module basis to indicator overall operating status.

4. Module Design Constraints

The following is a list a specifications that constrain the design of an HFC-6000 I/O board module.

4.1 Communication Interface Specifications

Document DS002-000-02 ICL Protocol Component Specification.

4.2 Detailed Design Specifications

901-000-02, I/O Module Detailed Design Specification
DS901-000-03, HFC-DO8J Detailed Design Specification
DS901-000-17, HFC-DO16C/J Detailed Design Specification
DS901-000-04, HFC-DI16I Detailed Design Specification
DS901-000-05, HFC-DC33 Detailed Design Specification
DS901-000-06, HFC-DC34 Detailed Design Specification
DS901-000-26, HFC-DC35 Detailed Design Specification
DS901-000-55, HFC-AI16E/FD Detailed Design Specification
DS901-000-08, HFC-AO8F Detailed Design Specification
DS901-000-63, HFC-AO8FD Detailed Design Specification
DS901-000-62, HFC-AC36D Detailed Design Specification
DS901-000-56, AFC-AI8LD Detailed Design Specification
DS901-000-57, HFC-AI8MD Detailed Design Specification
DS901-000-12, HFC-AC4KD Detailed Design Specification

5. Design Safety

5.1 Common Modules

The following paragraphs address those design safety considerations that are common to both input and output modules.

5.1.1 Security

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5.1.2 Risk

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5.2 Output Modules

The following paragraphs address the design safety considerations unique to output modules.

5.2.1 Criticality

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5.2.2 Hazard

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5.3 Input Modules

The following paragraphs address the design safety considerations unique to input modules.

5.3.1 Criticality

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5.3.2 Hazard

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5.3.3 Risk

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HF Controls

HFC-6000 Product Line

HFC-SBC06-DPM06

Module Detailed Design Specification

DS901-000-01

Rev D
(COST REDUCTION VERSION)

Effective Date	12/12/2008
Author	Monty Carpenter
Reviewer	David Briner
Approval	Gregory Rochford

Copyright© 2008 HF Controls Corporation

Revision History

Date	Revision	Author	Changes
04/14/04	0	B. Han	Initial
04/22/04	A	B. Han	Comments incorporated
3/9/07	B	J Taylor	SCR 1766
2/2/08	C	D. Briner	SCR 2006
10/9/08	D	M.Carpenter	Cost Reduced Version (XXXXXX)

Table of Contents

1. INTRODUCTION 5

2. HARDWARE DETAILED DESIGN FOR HFC-SBC06 5

2.1 MODULE SPECIFICATION 5
2.1.1 Environmental Extremes for Reliable Equipment Operations 5
2.1.2 Board Specification 5
2.1.3 C-Link - IEEE 802.3 10BASET Communication Links 6
2.1.4 ICL - EIA RS-485 communication links 6
2.2 ONBOARD POWER DISTRIBUTION 6
2.2.1 Power Distribution 6
2.2.2 Hardware Reset 7
2.3 CONNECTOR PINOUTS 7
2.4 SYS PROCESSOR SECTION 9
2.4.1 I/O Map 9
2.4.2 Real Time Counter Interrupts 11
2.5 ICL PROCESSOR SECTION 11
2.5.1 Interrupt Processing 11
2.5.2 ICL Interface 12
2.6 CPC PROCESSOR SECTION 13
2.6.1 Interrupt Processing 13
2.6.2 Ethernet Interface 13
2.7 SOE TIMER 15
2.8 FPGA 16

3. HARDWARE DETAILED DESIGN FOR HFC-DPM06 17

MODULE SPECIFICATION 17
3.2 ONBOARD POWER DISTRIBUTION 17
3.3 DIP SWITCH STATUS TRANSFER 17
3.4 HARDWARE CONNECTIONS 18

4. MEMORY CONFIGURATION AND ACCESS CONTROL 20

4.1 MEMORY CONFIGURATION 20
4.1.1 Private Memory Configuration for the SYS Processor 21
4.1.2 Private Memory Configuration for ICL and CPC Processors 21
*4.1.3 Public Memory ..... **Error! Bookmark not defined.***
4.1.4 Dual Ported Memory 21
4.2 MEMORY ACCESS CONTROL 22
4.2.1 Memory Control Signals for the SYS Processor 22
4.2.2 I/O and Memory Control for the CPC and ICL Processors 25
4.2.3 Public Memory and DPM Access 26
4.2.4 RAM Access Control 26

5. SOFTWARE DETAILED DESIGN SPECIFICATION 26
5.1 INITIALIZATION ROUTINES 27
5.1.1 General Initialization Sequence 27
5.1.2 SYS Processor Application Data Initialization 29

List of Tables

Table 1. P1 Pin Assignments 8
Table 2. Connector J7 and J9 Pin Assignments 9
Table 3. SYS Processor I/O Map 10
Table 4. Write Function for $F490_H$ 10
Table 5. Status Port 11
Table 6. NIC-DPM Control Signals 14
Table 7. Configuration Data Organization 18
Table 8. P1 Pin Assignments 19
Table 9. Memory Control Signals for SYS Processor 23
Table 10. I/O Mapping for 386EX Processors 25
Table 11. Memory Control Signals for ICL and CPC Processors 25

List of Figures

Figure 1. Memory Address Space Architecture 20
Figure 2. Processor Bus Structure Organization 23

1. Introduction

This HFC-SBC06 board and HFC-DPM06 board function together as a System Controller Module in an HFC-6000 control system. The overview of the architecture, functions and module structure of the HFC-SBC06 board and HFC-DPM06 board are provided in document MS901-000-01, HFC-SBC06-DPM06 Module Design Specification. The user of this document should be already familiar with document MS901-000-01. This document provides detailed structure and design descriptions on specific parts or features of the HFC-SBC06 board and HFC-DPM06 board, including hardware characteristics and software implementation methods. Rev D has the changes for the cost reduction consolidation of xxxxx.

2. Hardware Detailed Design for HFC-SBC06

2.1 Module Specification

- Assembly 400417-82 Pentium 133 CPU, CAT5, industrial grade parts

2.1.1 Environmental Extremes for Reliable Equipment Operations

- Temperature: 0° to 55° C (operating)
  0° to 70° C (storage)
- Humidity: 5% to 95% RH, non-condensing

2.1.2 Board Specification

- Supply Voltage +24 VDC
- Maximum Power Dissipation 18 Watts
- Onboard Clock Rate(s)

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- Mounting Requirements

The HFC-6000 product line includes both 19- and 23-in. controller chassis. Slots 12 and 14 of the 19-in. controller rack are designed to accept HFC-6000 controllers; slots 16 and 18 of the 23-in rack are designed for controllers. The slot between the two controller positions is designed to accept an HFC-DPM06 assembly.

2.1.3 C-Link - IEEE 802.3 10BASET Communication Links

• Transmission medium	100-Ω twisted pair cable, unshielded 22 to 26 AWG wire
• Maximum segment length	100 meters
• Network specifications	Standard IEEE 802.3 10BASET

The 10BaseT connections can be made either by the front card edge or via the HFC-6000 backplane through the HFC-HUB06-16 or HFC-HUB06-EXT for artwork revision D or higher assemblies. For assemblies artwork revision D or lower, the 10BaseT connections can be made only by the front card edge

2.1.4 ICL - EIA RS-485 communication links

• Transmission medium	backplane traces or twisted pair cable
• Signal characteristics	differential signal pair
• Maximum No. of RX/TX on link	32 TX, 32 RX
• Maximum cable length	4000 ft
• Maximum data rate	346 Kbps
• Minimum driver output range	±1.5 V
• Maximum driver output range	±5 V
• Maximum driver short circuit current	250 mA
• TX load impedance	54Ω
• RX input sensitivity	±200 mV
• Maximum RX input resistance	12 KΩ
• RX input voltage range	-7 V to +12 V
• RX logic high level	> 200 mV
• RX logic low level	< 200 mV

2.2 Onboard Power Distribution

2.2.1 Power Distribution

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2.2.2 Hardware Reset

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2.3 Connector Pinouts

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Table 1. P1 Pin Assignments

Category	Pin	Mnemonic	Pin	Mnemonic
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Category	Pin	Mnemonic	Pin	Mnemonic
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XXXX XXXX	XXXX XXXX XXXX XXXX XXXX	XXXX XXXX XXXX XXXX XXXX	XXXX XXXX XXXX XXXX XXXX	XXXX XXXX XXXX XXXX XXXX
XXXX XXXX XXXX	XXXX XXXX XXXX XXXX XXXX XXXX	XXXX XXXX XXXX XXXX XXXX XXXX	XXXX XXXX XXXX XXXX XXXX XXXX	XXXX XXXX XXXX XXXX XXXX XXXX

Table 2. Connector J7 and J9 Pin Assignments

Pin	Name
1	XXXX
2	XXXX
3	XXXX
4	XXXX
5	XXXX
6	XXXX
7	XXXX
8	XXXX

2.4 SYS Processor Section

2.4.1 I/O Map

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Table 3. SYS Processor I/O Map

Address Range	I/O **Write** Function	I/O **Read** Function
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2.4.1.1 I/O Port $F490_H$ – Memory Control and Status Port

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Table 4. Write Function for $F490_H$

Data Line	Function
0	XXXXXXXXXXXXX
1	XXXXXXXXXXXXX
2	XXXXXXXXXXXXX
3	XXXXXXXXXXXXX
4	XXXXXXXXXXXXX
6	XXXXXXXXXXXXX
7	XXXXXXXXXXXXX

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Table 5. Status Port

Data Line	Signal
0	XXXXXXXXXXXXX
1	XXXXXXXXXXXXX
2	XXXXXXXXXXXXX
3	XXXXXXXXXXXXX
4	XXXXXXXXXXXXX
7	XXXXXXXXXXXXX

2.4.1.2 I/O Port 200_H – Watchdog Timer Port

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2.4.1.3 I/O Port 210_H – Maintenance Failover Enable/Disable Port

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2.4.2 Real Time Counter Interrupts

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2.5 ICL Processor Section

2.5.1 Interrupt Processing

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2.5.2 ICL Interface

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2.6 CPC Processor Section

2.6.1 Interrupt Processing

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2.6.2 Ethernet Interface

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2.6.2.1 Interface Configuration

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2.6.2.2 FGA Design for NIC Support

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Table 6. NIC-DPM Control Signals

Description	NIC 0	NIC 1
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2.6.2.3 CPC Processor's Control Over NIC

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2.7 SOE Timer

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2.8 FPGA

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3. Hardware Detailed Design for HFC-DPM06

Module Specification

- Environmental Extremes for Reliable Equipment Operations
  - Temperature: 0° to 55° C (operating)
    0° to 70° C (storage)
  - Humidity: 5% to 95% RH, non-condensing
- Supply Voltage +24 VDC +/- 10%
- Maximum Power Dissipation 5.76 Watts
- Mounting Requirements

All HFC-6000 controller racks contain three slots on the right side of the chassis reserved for controller hardware. The middle slot of the three must contain an HFC-DPM06 assembly.

3.2 Onboard Power Distribution

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3.3 DIP Switch Status Transfer

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Table 7. Configuration Data Organization

Control Signal States			Data Transfer Enabled
DIPSW0	DIPSW1	DIPSW2	
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3.4 Hardware Connections

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Table 8. P1 Pin Assignments

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Category	Pin	Mnemonic	Pin	Mnemonic
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4. Memory Configuration and Access Control

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4.1 Memory Configuration

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Figure 1. Memory Address Space Architecture

4.1.1 Private Memory Configuration for the SYS Processor

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4.1.2 Private Memory Configuration for ICL and CPC Processors

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4.1.3 Public Memory

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4.1.4 Dual Ported Memory

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4.2 Memory Access Control

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4.2.1 Memory Control Signals for the SYS Processor

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XXXXXXXXXXXX

Figure 2. Processor Bus Structure Organization

Table 9. Memory Control Signals for SYS Processor

Signal	Description
XXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX
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4.2.2 I/O and Memory Control for the CPC and ICL Processors

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4.2.2.1 I/O Mapping Through The FPGA

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Table 10. I/O Mapping for 386EX Processors

DATELINE	FUNCTION
0	XXXXXXX
1	XXXXXXX
2	XXXXXXX
3	XXXXXXX
4	XXXXXXX

4.2.2.2 Memory Control Signals

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXX

Table 11. Memory Control Signals for ICL and CPC Processors

Signal	Function
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4.2.3 Public Memory and DPM Access

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4.2.4 RAM Access Control

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5. Software Detailed Design Specification

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5.1 Initialization Routines

5.1.1 General Initialization Sequence

Each processor on the HFC-SBC06 board goes through a set of initialization sequences before it starts normal operation. These initialization sequences include power up initialization, hardware initialization, processor configuration, and UCP Multitasking Operating System initialization.

5.1.1.1 Reset Initialization and Hardware Initialization

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5.1.1.2 Processor Configuration

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5.1.1.3 UCP Multitasking Operating System Initialization

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5.1.2 SYS Processor Application Data Initialization

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HF Controls Corporation

HFC-6000 Product Line

HFC-DO8J Board
Module Detailed Design Specification

Eight Channel Relay
Digital Output Board

DS901-000-03

REV B

January 30, 2009

INFORMATION ONLY

Author David Briner

Reviewer Pat Thibodeau

Approval Gregory Rochford

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INFORMATION ONLY

Revision History

Date	Revision	Author	Changes
10/30/03	0	B Han	Initial
11/11/03	1	B Han	Review comments incorporated
11/19/03	A	B Han	Review comments incorporated
1/30/09	B	D Briner	Review comments incorporated

Table of Contents

1. INTRODUCTION 5

2. FUNCTIONAL DESCRIPTION 5

3. HARDWARE DETAILED DESIGN SPECIFICATION 5

3.1 MODULE SPECIFICATION 5
3.2 SWITCHES, JUMPERS, AND LED INDICATORS 5
3.2.1 Jumpers 6
3.2.2 LED Indicators 6
3.3 ONBOARD POWER DISTRIBUTION 6
3.4 DIGITAL DATA OUTPUT PORT 6
3.5 HARDWARE CONNECTIONS 7

4. SOFTWARE DETAILED DESIGN SPECIFICATION 8

4.1 I/O SCAN MODULE 8
4.2 PROCESS COMMAND ROUTINE 8
4.3 DATA STRUCTURE 8
4.3.1 I/O Scan Data 8
4.3.2 Microprocessor Programmable Ports 8

5. MODULE IMPLEMENTATION DESCRIPTIONS 9

5.1 HARDWARE SCHEMATICS 9
5.2 HARDWARE COMPONENTS – BILL OF MATERIALS 9
5.3 SOFTWARE SOURCE CODE LISTING 9

1. Introduction

The HFC-DO8J assembly is an eight-channel relay digital output board. This assembly operates as a standard DO relay board in an HFC-6000 control system. It receives the images of its digital outputs from an HFC-SBC06 system controller at regular intervals, and uses this data to set the on/off status of each output relay.

The overall architectural design of standard HFC-6000 I/O boards are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification.

This document describes the detailed structure and design of the HFC-DO8J board. The design descriptions of the common software modules of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DO8J board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DO8J board is designed to interface eight field outputs to an HFC-6000 control system. It provides eight relay digital output channels. The board receives the image of its digital outputs from the HFC-SBC06 controller board at regular intervals, and uses this data to set the on/off status of each output relay.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification.

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes
  - Temperature: 0° to 55 C° (operating)
    0° to 55 C° (storage)
  - Humidity: 5% to 95%, non-condensing

- Power Requirement
  - External Input Power: +24-vdc, 0.4 A maximum load

- Onboard Clock Rate
  - Microprocessor Clock: 22.1184 MHZ
- Relay contact ratings
  - Up to 30-vdc with 5 A maximum current (resistive load)
  - Up to 250-vac with 5 A maximum current (general use)

3.2 Switches, Jumpers, and LED Indicators

The HFC-DO8J board includes the four card-edge LEDs common to all I/O boards as well as the following components unique to this assembly:

3.2.1 Jumpers

E1-E2 Installed during testing to disable the NMI signal. When the jumper is removed, the D-latch U41-A activates a high NMI signal.

E5-6 Function not currently defined

3.2.2 LED Indicators

DS1-1 Lights when the channel 1 is on
DS1-2 Lights when the channel 2 is on
DS1-3 Lights when the channel 3 is on
DS1-4 Lights when the channel 4 is on

DS2-1 Lights when the channel 5 is on
DS2-2 Lights when the channel 6 is on
DS2-3 Lights when the channel 7 is on
DS2-4 Lights when the channel 8 is on

3.3 ONBOARD POWER DISTRIBUTION

The board receives redundant 24-vdc power feeds from the back plane connector P1. The two power feeds are diode auctioneered, and the resulting 24-vdc output is routed to the following components:

- The onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for logic components on the HFC-DO8J board.

- The combined 24-vdc power line supplies operating power to each of the output relays. A transistor switch in this power line opens whenever the watchdog timer becomes reset.

3.4 Digital Data Output Port

The HFC-DO8J board includes eight relay-controlled DO channels. The ON/OFF image for the eight channels are configured in memory as a single byte of data. During regular scan cycles, the microprocessor copies the DO image from memory to an eight-bit latch, and the resulting output signals from the latch control each DO channel individually.

Each output channel consists of an optocoupler and a mechanical relay with both normally open and normally closed contacts. The optocoupler is configured with a control signal input PTn/ routed from the data output port and the 24-vdc power for the relay. When the digital image for a particular DO channel is ON (PTn/ signal low), the optocoupler becomes forward biased, and 24-vdc power line passes through the optocoupler circuit to the relay coil. While the microprocessor is processing its program code normally, the 24-vdc power line energizes the relay to produce the ON state output. However, if the watchdog timer becomes reset, a transistor switch in the 24-vdc power line opens, removing operating power from all of the relays simultaneously.

3.5 Hardware Connections

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Table 1. Connector P1 Pinout Summary

Category	Pin	Mnemonic	Pin	Mnemonic
Power	P1-A1	XXXXXXX	P1-B1	XXXXXXX
	P1-C1	XXXXXXX	P1-A3	XXXXXXX
	P1-B3	XXXXXXX	P1-C3	XXXXXXX
	P1-A5	XXXXXXX	P1-B5	XXXXXXX
	P1-C5	XXXXXXX	P1-A12	XXXXXXX
	P1-B12	XXXXXXX	P1-C12	XXXXXXX
	P1-A14	XXXXXXX	P1-B14	XXXXXXX
	P1-C14	XXXXXXX	P1-A16	XXXXXXX
	P1-B16	XXXXXXX	P1-C16	XXXXXXX
Serial Bus	P1-A9	XXXXXXX	P1-C9	XXXXXXX
	P1-B8	XXXXXXX	P1-A10	XXXXXXX
	P1-C10	XXXXXXX	P1-C8	XXXXXXX
CONTROL	P1-A6	XXXXXXX	P1-B6	XXXXXXX
	P1-C6	XXXXXXX	P1-A7	XXXXXXX
	P1-B7	XXXXXXX	P1-C7	XXXXXXX
	P1-A8	XXXXXXX		

Table 2. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A32	XXXXXXX	P2-C32	XXXXXXX
P2-A31	XXXXXXX	P2-C31	XXXXXXX
P2-A30	XXXXXXX	P2-C30	XXXXXXX
P2-A29	XXXXXXX	P2-C29	XXXXXXX
P2-A28	XXXXXXX	P2-C28	XXXXXXX
P2-A27	XXXXXXX	P2-C27	XXXXXXX
P2-A26	XXXXXXX	P2-C26	XXXXXXX
P2-A25	XXXXXXX	P2-C25	XXXXXXX
P2-A24	XXXXXXX	P2-C24	XXXXXXX
P2-A23	XXXXXXX	P2-C23	XXXXXXX
P2-A22	XXXXXXX	P2-C22	XXXXXXX
P2-A21	XXXXXXX	P2-C21	XXXXXXX
PS-A20	XXXXXXX	PS-C20	XXXXXXX
P2-A19	XXXXXXX	P2-C19	XXXXXXX
P2-A18	XXXXXXX	P2-C18	XXXXXXX
PS-A17	XXXXXXX	PS-C17	XXXXXXX

P2-A16	XXXXXXX	P2-C16	XXXXXXX
P2-A15	XXXXXXX	P2-C15	XXXXXXX
P2-A14	XXXXXXX	P2-C14	XXXXXXX
P2-A13	XXXXXXX	P2-C13	XXXXXXX
P2-A12	XXXXXXX	P2-C12	XXXXXXX
P2-A11	XXXXXXX	P2-C11	XXXXXXX
P2-A10	XXXXXXX	P2-C10	XXXXXXX
P2-A9	XXXXXXX	P2-C9	XXXXXXX

4. Software Detailed Design Specification

The HFC-DO8J board has a total of eight DO channels that provide both normally open and normally closed contacts. The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DO8J board.

4.1 I/O Scan Module

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XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

4.2 Process Command Routine

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4.3 Data Structure

This section describes the structure of the DO image and provides a list of the programmable ports used in the software.

4.3.1 I/O Scan Data

The DO8J board has eight DO channels. The eight DO images are organized as a single byte in the poll message received from the SBC06 controller as shown below:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX

4.3.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 3. Programmable Ports Used for DO8J Board

Port	Function	Implementation
P1.2	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX

Port	Function	Implementation
P1.3	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX
P1.6	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX
P1.7	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX
P2.1	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX
P2.3	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX
Port 1 Control Register	XXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXX

5. Module Implementation Descriptions

5.1 Hardware Schematics

The schematic for the HFC-DO8J board is drawing 400458-01.

5.2 Hardware Components – Bill of Materials

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX.

5.3 Software Source Code Listing

The HFC-DO8J board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

DOOSAN

HF Controls

INFORMATION ONLY

HF Controls Corporation

HFC-6000 Product Line

HFC-DC33 Board
Module Detailed Design Specification

Digital Input/Output Controller Board
Specific for Motor Operated Valve (MOV)

DS901-000-05

Rev D

Effective Date	11/30/07
Author	M. Hayes
Reviewer	J. Taylor
Approval	D. Briner

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DOOSAN

HFC

Revision History

Date	Revision	Author	Changes
11/10/03	0	B Lin	Initial draft
11/19/03	A	B Lin	Review comments incorporated
3/3/07	B	J Taylor	SCR 1766.
10/18/07	C	M Hayes	SCR 1706
10/26/07	D	M Hayes	SCR 1958

Table of Contents

1. INTRODUCTION 3

2. FUNCTIONAL DESCRIPTION 3

3. HARDWARE DETAILED DESIGN SPECIFICATION 4

3.1 MODULE SPECIFICATION 4
3.2 CONTROLS, JUMPERS, AND LED INDICATORS 4
3.3 ONBOARD POWER DISTRIBUTION 6
3.4 MICROPROCESSOR PERIPHERAL PORTS 7
3.5 INPUT CHANNEL OPERATION 7
3.6 HARDWARE CONNECTIONS 8

4. SOFTWARE DETAILED DESIGN SPECIFICATION 11

4.1 I/O SCAN MODULE 11
4.2 PROCESS COMMAND ROUTINE 11
4.3 DATA STRUCTURE 11
4.3.1 I/O Scan Data 11
4.3.2 Microprocessor Programmable Ports 12

5. MODULE IMPLEMENTATION DESCRIPTION 13

5.1 HARDWARE SCHEMATICS 13
5.2 HARDWARE COMPONENTS – BILL OF MATERIALS 13
5.3 SOFTWARE SOURCE CODE LISTING 13

6. DESIGN SAFETY 14

1. Introduction

The HFC-DC33 is a multi-channel Input/Output (I/O) buffer printed circuit board (PCB). It is used for control, interrogation, and monitoring of field devices in an HFC-6000 control system. The board receives digital messages from its controller, the HFC-SBC06, and sends the image of its 11 digital input (DI) channels.

Descriptions and discussions of the architectural and design descriptions of a standard HFC-6000 I/O board, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-DC33 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DC33 board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DC33 is a special purpose I/O buffer board designed for power plant applications. This buffer is specifically designed to meet the unique control requirements of a dual-coil Motor Operated Valve (MOV) starter. Typical applications include controlling dual coil motor starters while monitoring coil continuity, overloads and the position of the valve.

This board provides a 16-bit 80C188EB microprocessor, 11 DI channels, two 120-vac DO channels, and onboard status sensors. Major functions performed by the microprocessor during normal operation are as follows:

- Responds to data transmissions from the HFC-6000 controller.
- Controls the on/off state of the two DO channels.
- Reads the digital status of the onboard DI channels.
- Reads coil continuity and the presence of ac excitation signals for both DO channels individually.
- Stores the DI image and onboard status in local memory.
- Transmits the digital image of its 11 DI channels back to the HFC-6000 controller.
- Reads seal-in status for each channel.
- Integral transient suppression networks permit reliable operation in high-noise (electrical) environments.
- Optocouplers isolate logic circuits from field wiring.
- Provides direct solid-state control of special dual coil 120-vac output for such field devices as a dual coil Motor Operated Valve (MOV) starter.
- The board includes two banks of memory for an onboard 16-bit Intel 80C188EB microprocessor:
    - High memory provides up to 64K by 8-bits of EPROM for functional program code storage.

- Low memory provides 32K by 8 bits of RAM for temporary storage of message data being processed.
- An onboard dc-to-dc converter provides regulated +5-vdc logic power.
- Provides a seal-in circuit that enables the onboard circuitry to sustain the 120VAC output in the event of controller failure or loss of power to the board.
- An onboard switch enables manual reset of the microprocessor.
- Onboard watchdog timer.
- Provides two output channels for 120-vac, two input channels that monitor continuity of external solenoid coils, and 11 general purpose Digital Inputs (DI).
- Monitors the 48-vdc-interrogation voltage for the 11 general purpose DI channels.
- Onboard LEDs provide visual indication of board status.
- Allows standardization of internal wiring for controlled devices.
- Onboard software provides built-in diagnostics.
- The HFC-DC33 assembly is designed to satisfy seismic category I requirements.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification.

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes
  - Temperature: 0° to 60 C° (operating)
    0° to 70 C° (storage)
  - Humidity: 5% to 95%, non-condensing

- Power Requirement — Note: AC signals are represented by their rms value.
  - Output Voltage: 60 to 140-vac, 47 to 63 Hz
  - Output Current: 110 amps: inrush, 5 amps continuous
  - External Source Power: 24-vdc at 0.3 A nominal current
  - Interrogation Voltage: 48-vdc

- Onboard Clock Rate
  - Microprocessor Clock: 22.1184 MHZ

- Mounting Requirements
  - The HFC-DC33 mounts vertically in an HFC-6000 card chassis.

3.2 Controls, Jumpers, and LED Indicators

3.2.1 Jumpers

E1-E2 Installed during calibration to disable the NMI signal. When the jumper is removed, the D-latch U41-A activates a high NMI signal.

3.2.2 Switches

SW1 Enables manual reset of the 80C188EB microprocessor.

S3 Permits manual configuration of DI channels 1-11 as isolated or common in any combination

S1 Enables/Disables the Seal-In circuitry for channel 0 output

S2 Enables/Disables the Seal-In circuitry for channel 1 output

3.2.3 Reset-able Fuses

RF1–RF3 Provide overload protection for the +48-vdc interrogation voltage supplied for the 11 DI channels.

3.2.4 LED Indicators

DS1-1 SYSA/B lights when receive function is enabled for port A; it is out when receive function is enabled for port B.
DS1-2 TX flashes during serial data transmission over ICL.
DS1-3 RX flashes during reception of serial data from ICL.
DS1-4 DMT lights while watchdog timer is being triggered.

DS2-1 CH0_RDY lights when 120- vac power is available, and CH0 is de-energized and connected to an operational coil
DS2-2 CH1_RDY lights when 120- vac power is available, and CH1 is de-energized and connected to an operational coil
DS2-3 PWR PRESENT0 lights when 120-vac power is available for CH0.
DS2-4 PWR PRESENT1 lights when 120-vac power is available for CH1.
DS3-1 SEAL IN CH0 lights when seal-in switch for CH0 is enabled and seal-in voltage is present.
DS3-2 SEAL IN CH1 lights when seal-in switch for CH1 is enabled and seal-in voltage is present.
DS3-3 CH0 OUT lights when output relay U13 is enabled.
DS3-4 CH1 OUT lights when output relay U27 is enabled.

DS4-1 Lights when input channel 1 is on.
DS4-2 Lights when input channel 2 is on.
DS4-3 Lights when input channel 3 is on.
DS4-4 Lights when input channel 4 is on.

DS5-1 Lights when input channel 5 is on.
DS5-2 Lights when input channel 6 is on.
DS5-3 Lights when input channel 7 is on.
DS5-4 Lights when input channel 8 is on.

DS6-1 Lights when input channel 9 is on.
DS6-2 Lights when input channel 10 is on.

DS6-3 Lights when input channel 11 is on.
DS6-4 No connection, will not illuminate.

3.3 Onboard Power Distribution

The board receives redundant 24-vdc power feeds from the backplane connector P1. The two power feeds are diode auctioneered, and an onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for components on the HFC-DC33 board.

Two +48-vdc interrogation power sources are fed through connector P1 and divided into three branches with each branch supplying power to four channels. A separate reset-able fuse provides overload protection for each branch, and three optocouplers permit the microprocessor to monitor status of the three power lines.

The board receives a nominal 120-vac (60 to 140-vac) power for the two solenoid output channels. When supply power is provided to each channel individually, a bridge rectifier produces a dc status signal that forward biases an optocoupler, enabling the microprocessor to verify power status of each channel. The 120-vac power line is connected to a separate solid state relay for CH0 and CH1. The microprocessor can control these relays independently to enable power output to one or both channels.

120-VAC can be provided to the seal-in circuitry for CH0/CH1 individually. When power is available, a bridge rectifier produces a dc signal that is supplied to a DC-DC converter. If S1 is in the enabled position a 5V signal is available to sustain the output of CH0 in case of controller failure or in loss of 24V power to the board. If S2 is in the enabled position a 5V signal is available to sustain the output of CH1 in case of controller failure or in the loss of 24V power to the board.

3.4 Microprocessor Peripheral Ports

The microprocessor controls the following peripheral ports:

- Two digital data input ports
- CH0/CH1 control output port
- Link address data input port
- Redundant serial ports

Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the I/O ports.

The board provides two output latches to control the status of the two 120-vac output channels (CH0 and CH1) and two input buffers to read 15 bits of input data. During an I/O scan, the microprocessor writes the ON/OFF image for CH0 and CH1 to the output latch. The resulting output signals control separate solid state relays. When the microprocessor enables one or both outputs, the corresponding relay becomes enabled and passes the 120-vac power to its output. Similarly, the microprocessor reads input status by running separate read cycles to the two input buffers. The low order byte contains the digital image of PT01/ through PT08/. The high order byte contains the digital image of PT09/ through PT11/, CH0_RDY/, CH1_RDY/, CH0_PWR/, CH1_PWR/, SICH0/, and SICH1/. In addition to the 17 bits of input data, the microprocessor also can read the status of the excitation voltage lines VSEN/, VSEN2/, and VSEN3/. These signals are routed directly to three pins of programmable I/O port P2 of the microprocessor.

The Link address data input port and Redundant serial ports are covered in document DS901-000-02 I/O Board Module Detailed Design Specification.

3.5 Input Channel Operation

The HFC-DC33 board contains 20 input channels composed of 11 general purpose DI channels, two coil continuity inputs, two power monitor inputs, two seal-in status inputs, and a separate status monitor for the three excitation voltage lines. Each of the DI channels is composed of a low-pass input filter and optocoupler. The input filter is designed to reject any input signal having a pulse width less than 10 ms in duration, and the optocoupler isolates the internal logic circuitry from the field wiring. When one of these channels receives an active input signal, the optocoupler becomes forward biased and produces a low active output. While any of these outputs is active, the corresponding LED lights. The input circuit for the three VSEN/ input signals is identical, except they do not have an LED indication.

The input circuit for the 120-vac power monitor consists of a bridge rectifier, a low pass filter, and an optocoupler. When the 120-vac power source is present, the rectifier produces a dc signal at the input of the low pass filter network, and the optocoupler activates the CH0_PWR/ status signal.

The circuit for the two coil continuity monitor inputs is similar to that of the power monitor circuit except for input biasing. When the 120-vac output is enabled, the circuit is always

enabled, so the status input is not meaningful. When either output channels are disabled, a small voltage bleeds through the biasing network to the input of the rectifier of that respective channel. If the external coil is present, this small voltage dissipates through the coil and the output from the optocoupler remains disabled. This output is inverted to produce a low active status input (CH0_RDY/ or CH1_RDY/) to the microprocessor. If the external coil is not present or open, the small voltage at the input of the rectifier is sufficient to forward bias the optocoupler, resulting in a high (false) indication for the CH_RDY/ input.

3.6 Hardware Connections

The HFC-DC33 board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Pin assignments for the P1 connector are identical for all I/O boards and can be found in document DS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each DI channel can be configured for either isolated or common mode operation on an individual basis. When operating in common mode, excitation voltage is supplied from this board to the field device being monitored. When operating in isolated mode, external equipment must supply the power to enable or disable the DI indication. Table 2 lists the DIP switch settings and signal assignments required to configure each channel for either mode of operation.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	XXXXXXXXXXXXXX	P2-C1	XXXXXXXXXXXXXX
P2-A2	XXXXXXXXXXXXXX	P2-B2	XXXXXXXXXXXXXX
P2-C2	XXXXXXXXXXXXXX	P2-A3	XXXXXXXXXXXXXX
P2-C3	XXXXXXXXXXXXXX	P2-A4	XXXXXXXXXXXXXX
P2-C4	XXXXXXXXXXXXXX	P2-A5	XXXXXXXXXXXXXX
P2-B5	XXXXXXXXXXXXXX	P2-C5	XXXXXXXXXXXXXX
P2-A6	XXXXXXXXXXXXXX	P2-C6	XXXXXXXXXXXXXX
P2-A7	XXXXXXXXXXXXXX	P2-C7	XXXXXXXXXXXXXX
P2-A8	XXXXXXXXXXXXXX	P2-B8	XXXXXXXXXXXXXX
P2-C8	XXXXXXXXXXXXXX	P2-A9	XXXXXXXXXXXXXX
P2-C9	XXXXXXXXXXXXXX	P2-A10	XXXXXXXXXXXXXX
P2-C10	XXXXXXXXXXXXXX	P2-A11	XXXXXXXXXXXXXX
P2-B11	XXXXXXXXXXXXXX	P2-C11	XXXXXXXXXXXXXX
P2-A12	XXXXXXXXXXXXXX	P2-C12	XXXXXXXXXXXXXX
P2-A13	XXXXXXXXXXXXXX	P2-C13	XXXXXXXXXXXXXX
P2-A14	XXXXXXXXXXXXXX	P2-B14	XXXXXXXXXXXXXX
P2-C14	XXXXXXXXXXXXXX	P2-A15	XXXXXXXXXXXXXX
P2-C15	XXXXXXXXXXXXXX	P2-A16	XXXXXXXXXXXXXX
P2-C16	XXXXXXXXXXXXXX	P2-A17	XXXXXXXXXXXXXX
P2-B17	XXXXXXXXXXXXXX	P2-C17	XXXXXXXXXXXXXX
P2-A18	XXXXXXXXXXXXXX	P2-C18	XXXXXXXXXXXXXX
P2-A19	XXXXXXXXXXXXXX	P2-B19	XXXXXXXXXXXXXX
P2-C19	XXXXXXXXXXXXXX	P2-A20	XXXXXXXXXXXXXX
P2-B20	XXXXXXXXXXXXXX	P2-C20	XXXXXXXXXXXXXX
P2-A21	XXXXXXXXXXXXXX	P2-B21	XXXXXXXXXXXXXX
P2-C21	XXXXXXXXXXXXXX	P2-A22	XXXXXXXXXXXXXX
P2-B22	XXXXXXXXXXXXXX	P2-C22	XXXXXXXXXXXXXX
P2-A23	XXXXXXXXXXXXXX	P2-B23	XXXXXXXXXXXXXX
P2-C23	XXXXXXXXXXXXXX	P2-A24	XXXXXXXXXXXXXX
P2-B24	XXXXXXXXXXXXXX	P2-C24	XXXXXXXXXXXXXX
P2-A25	XXXXXXXXXXXXXX	P2-B25	XXXXXXXXXXXXXX
P2-C25	XXXXXXXXXXXXXX	P2-A26	XXXXXXXXXXXXXX

Table 1 (Continued). Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-B26	XXXXXXXXXXXXXX	P2-C26	XXXXXXXXXXXXXX
P2-A27	XXXXXXXXXXXXXX	P2-B27	XXXXXXXXXXXXXX
P2-C27	XXXXXXXXXXXXXX	P2-A28	XXXXXXXXXXXXXX
P2-B28	XXXXXXXXXXXXXX	P2-C28	XXXXXXXXXXXXXX
P2-A29	XXXXXXXXXXXXXX	P2-B29	XXXXXXXXXXXXXX
P2-C29	XXXXXXXXXXXXXX	P2-A30	XXXXXXXXXXXXXX
P2-B30	XXXXXXXXXXXXXX	P2-C30	XXXXXXXXXXXXXX
P2-A31	XXXXXXXXXXXXXX	P2-B31	XXXXXXXXXXXXXX
P2-C31	XXXXXXXXXXXXXX	P2-A32	XXXXXXXXXXXXXX
P2-B32	XXXXXXXXXXXXXX	P2-C32	XXXXXXXXXXXXXX

Table 2. Input Connection Summary

Channel No.	Type	Positive	Negative	Dipswitch
1	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
2	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
3	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
4	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
5	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
6	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
7	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
8	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
9	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
10	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
11	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX

4. Software Detailed Design Specification

The HFC-DC33 board monitors a total of 20 DI channels. The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DC33 board..

4.1 I/O Scan Module

This I/O Scan Module performs the I/O scan for 11 standard DI channels, two coil continuity status inputs, two power monitor status inputs, and two seal in status inputs. It takes samples to read the status of three interrogation voltages and two bytes of input data during each scan. The loss of any interrogation voltage means that four or more DI images may not be valid, so the module will not update DI images with new readings if no interrogation voltage is present. If any interrogation voltage is false, the Interrogation Voltage Off error bit in the diagnostic byte will be set to indicate a hardware fault. This information will be reported to the controller in the response to a diagnostic request message.

Normally the DI images will be transferred to the Scan Working Buffer only when at least one of three interrogation voltages is present. However, to avoid missing information on the controller side, an interrogation voltage failure counter is used in the I/O scan process. This counter is incremented during each scan cycle where all interrogation voltages are missing. When the accumulated count exceeds a predefined limit, the DI images in the Scan Working Buffer will be updated and reported to the controller, even if no interrogation voltage is present. This counter will remain reset as long as any interrogation voltage line is present.

If a DO channel is set ON, the corresponding coil continuity status input is not meaningful. So the coil continuity status will be reported as "TRUE" to prevent spurious error indications. Only when the corresponding DO channel is not ON will the actual coil continuity status be reported back to the HFC-SBC06 controller.

4.2 Process Command routine

For normal update messages, this routine reads the one byte output image for two output channels from the command message and transfers that image to output data latch. UCP diagnostics messages are processed as described in HFC-6000 I/O Board Module Detailed Design Specification DS002-000-02.

4.3 Data Structure

This section describes the structure of the I/O data images and provides a list of the programmable ports controlled by the software.

4.3.1 I/O Scan Data

The HFC-DC33 board has two DO channels and 11 DI channels. The data field of poll messages received from the HFC-SBC06 controller has the following structure:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PT2	PT1

The data field of the response message to the HFC-SBC06 Controller has the following structure:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1
2	Power Source 1	Power Source 0	Coil 1 Continuity	Coil 0 Continuity	Seal In CH 0	PT11	PT10	PT9

4.3.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 3. Programmable Ports Used for HFC-DC33 Board

Port	Description	Implementation
P1.0	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.1	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.2	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.3	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.4	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.5	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.7	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P2.1	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P2.3	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P2.4	XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX
P2.5	XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX
P2.6		XXXXXXXXXXXXXXXXXXXX
Port 1 Control Register	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX

4.3.3 Failsafe Function

The hardware assembly includes an onboard seal-in circuit. When the seal-in input is configured and the onboard latch enable switch (S1) is closed, the seal-in circuit latches in the true state of the DO signal. The purpose of this circuit is to maintain the energized state of the DO signal even if power is lost from the control system. (The power required to maintain this state must be supplied from the external field equipment.)

Seal-in status is included with the DI image read by the microprocessor during each scan cycle. In the event of ICL timeout, the microprocessor checks seal-in status. If seal-in status is true, then the microprocessor keeps the DO channel energized. If seal in status is false (either because the DO channel is off or the seal-in function is not configured), the microprocessor clears the DO latch for failsafe.

5. Module Implementation Description

5.1 Hardware Schematics

The schematic for the HFC-DC33 board is drawing 400463-01.

5.2 Hardware Components – Bill of Materials

The part number of the HFC-DC33 board is 40046201, and its bill of materials is 400462-01 and 400462-81.

5.3 Software Source Code Listing

The HFC-*DC33* board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- xxxxxxxxxxxxxxxxx
- xxxxxxxxxxxxxxxxx

6. Design Safety

Refer to MS901-000-02 for a discussion of design safety considerations for HFC-6000 I/O modules.

DOOSAN

HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-DC34 Board
Module Detailed Design Specification

Digital Input/Output Controller Board
Specific for Electronically Operated Breakers (EOB)

DS901-000-06

Rev D

INFORMATION ONLY

Effective Date	11/30/07
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DOOSAN

HFC

Revision History

Date	Revision	Author	Changes
11/12/03	0	B Lin	Initial draft
11/19/03	A	B Lin	Review comments incorporated
3/2/07	B	J Taylor	SCR 1766
10/18/07	C	M Hayes	SCR 1706
11/13/07	D	M Hayes	SCR 1958

Table of Contents

1. INTRODUCTION 3

2. FUNCTIONAL DESCRIPTION 3

3. HARDWARE DETAILED DESIGN SPECIFICATION 4

3.1 MODULE SPECIFICATION 4
3.2 CONTROLS, JUMPERS, AND LED INDICATORS 4
3.3 ONBOARD POWER DISTRIBUTION 6
3.4 MICROPROCESSOR PERIPHERAL PORTS 6
3.5 INPUT CHANNEL OPERATION 7
3.6 HARDWARE CONNECTIONS 8

4. SOFTWARE DETAILED DESIGN SPECIFICATION 10

4.1 I/O SCAN MODULE 10
4.2 PROCESS COMMAND ROUTINE 11
4.3 DATA STRUCTURE 11
4.3.1 I/O Scan Data 11
4.3.2 Microprocessor Programmable Ports 11

5. MODULE IMPLEMENTATION DESCRIPTION 13

5.1 HARDWARE SCHEMATICS 13
5.2 HARDWARE COMPONENTS – BILL OF MATERIALS 13
5.3 SOFTWARE SOURCE CODE LISTING 13

6. DESIGN SAFETY 13

1. Introduction

The HFC-DC34 is a multi-channel Input/Output (I/O) buffer printed circuit board (PCB). It is used for control, interrogation, and monitoring of field devices in an HFC-6000 control system. Typical applications include monitoring Electrically Operated Breakers (EOB) for overloads. The board receives digital messages from its controller, the HFC-SBC06, and sends the image of its 11 digital input (DI) channels.

Descriptions and discussions of the architecture and design descriptions of a standard HFC-6000 I/O board, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-DC34 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DC34 board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DC34 is a special purpose I/O buffer board designed for power plant applications. This board is designed to provide the specific combination of digital I/O channels needed to control motor starter or switchgear field equipment.

This board provides a 16-bit 80C188EB microprocessor, 11 DI channels, two 125-vdc DO channels, and onboard status sensors. Major functions performed by the microprocessor during normal operation are as follows:

- Responds to data transmissions from the HFC-6000 controller.
- Controls the on/off state of the two output channels.
- Reads the digital status of the onboard DI channels.
- Reads coil continuity and the presence of dc excitation signals for each channel individually
- Stores the DI image and onboard status in local memory.
- Transmits the digital image of its 11 DI channels back to the HFC-6000 controller.
- Reads seal-in status for each channel
- Integral transient suppression networks permit reliable operation in high-noise (electrical) environments.
- Provides input filters and opto-couplers to isolate logic circuits from field wiring.
- Provides direct solid-state control of two 125-vdc outputs for such field devices as an Electrically Operated Breaker (EOB).
- The board includes two banks of memory for an onboard 16-bit Intel 80C188EB microprocessor:
    - High memory provides up to 64K by 8-bits of EPROM for functional program code storage.

- Low memory provides 32K by 8-bits of RAM for temporary storage of message data being processed.
- An onboard dc-to-dc converter provides regulated +5-vdc logic power.
- Provides two seal-in circuits that enable the onboard circuitry to maintain the two 125-VDC output in the event of controller failure.
- An onboard switch enables manual reset of the microprocessor.
- Onboard watchdog timer.
- Provides 48-vdc interrogation voltage for the DI channels.
- Monitors the 48-vdc power sources.
- Onboard LEDs provide visual indication of board status.
- Allows standardization of internal wiring for controlled devices.
- The HFC-DC34 assembly is designed to satisfy seismic category I requirements.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification.

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes
  - Temperature: 0° to 60 C° (operating)
    0° to 70 C° (storage)
  - Humidity: 5% to 95%, non-condensing

- Power Requirement
  - Output Voltage: 100 to 150-vdc
  - Output Current: 25 amps: inrush
    10 amps, 250ms repeated once per 5 minutes
    2 amps continuous
  - External Source Power: 24-vdc at 0.3 A nominal current
  - Interrogation Voltage: 48-vdc
- Onboard Clock Rate 22.1184 MHZ
- Mounting Requirements
  - The HFC-DC34 mounts vertically in an HFC-6000 card chassis.

3.2 Controls, Jumpers, and LED Indicators

3.2.1 Jumpers

E1-E2 Installed during calibration to disable the NMI signal. When the jumper is removed, the D-latch U41-A activates a high NMI signal.

3.2.2 Switches

SW1 Enables manual reset of the 80C188EB microprocessor.

S1 Permits manual configuration of DI channels 1-11 as isolated or common in any combination

S3 Enables/Disables the Seal In mode for CH0

S4 Enables/Disables the Seal In mode for CH1

3.2.3 Reset-able Fuses

RF1–RF3 Provide overload protection for the +48-vdc interrogation voltage supplied for the 11 DI channels.

3.2.4 LED Indicators

DS1-1 SYSA/B lights when receive function is enabled for port A; it is out when receive function is enabled for port B.
DS1-2 TX flashes during serial data transmission over ICL.
DS1-3 RX flashes during reception of serial data from ICL.
DS1-4 DMT lights while watchdog timer is being triggered.

DS2-1 CH0 RDY lights when 125- vdc power is available, coil test mode is enabled, and the external coil on CH0 is operational.
DS2-2 CH1 RDY lights when 125- vdc power is available, coil test mode is enabled, and the external coil on CH1 is operational.
DS2-3 PWR PRESENT0 lights when 125-vdc power is available for CH0.
DS2-4 PWR PRESENT1 lights when 125-vdc power is available for CH1.
DS3-1 SEAL IN CH0 lights when seal in switch for CH0 is enabled and seal-in voltage is present.
DS3-2 SEAL IN CH1 lights when seal in switch for CH1 is enabled and seal-in voltage is present.
DS3-3 CH0 OUT lights when the CH0 output is enabled.
DS3-4 CH1 OUT lights when the CH1 output is enabled.

DS4-1 Lights when input channel 1 is on.
DS4-2 Lights when input channel 2 is on.
DS4-3 Lights when input channel 3 is on.
DS4-4 Lights when input channel 4 is on.

DS5-1 Lights when input channel 5 is on.
DS5-2 Lights when input channel 6 is on.
DS5-3 Lights when input channel 7 is on.
DS5-4 Lights when input channel 8 is on.

DS6-1 Lights when input channel 9 is on.

DS6-2 Lights when input channel 10 is on.
DS6-3 Lights when input channel 11 is on.
DS6-4 No connection, will not illuminate.

3.3 Onboard Power Distribution

The board receives redundant 24-vdc power feeds from the backplane connector P1. The two power feeds are diode auctioneered, and an onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for components on the HFC-DC34 board.

Two +48-vdc interrogation power sources are fed through connector P1 and divided into three branches with each branch supplying power to four channels. A separate reset-able fuse provides overload protection for each branch, and three opto-couplers permit the microprocessor to monitor status of the three power lines.

The board receives a nominal 125-vdc (100 to 150-vdc) power for the two solenoid output channels. When supply power is available, an input status signal forward biases a corresponding optocoupler, enabling the microprocessor to verify power status of each channel individually. The 125-vdc power line is connected to a separate FET switch for CH0 and CH1. The microprocessor can control these FETs independently to enable power output on one or both channels.

125-VDC can be provided to the seal-in circuitry for CH0/CH1. When power is available, a linear regulator converts 125-VDC to 48-VDC, then a DC-DC converter converts 48VDC to 5VDC. If S3 is in the enabled position and the 125-VDC is supplied to SEAL IN CH0, then a 5V signal is available to sustain the output of CH0 in case of controller failure or in loss of 24V power to the board. If S4 is in the enabled position and the 125-VDC is supplied to SEAL IN CH1, then a 5V signal is available to sustain the output of CH1 in case of controller failure or in loss of 24V power to the board.

3.4 Microprocessor Peripheral Ports

The microprocessor controls the following peripheral ports:

- Two digital data input ports
- CH0/CH1 control output port
- Link address data input port
- Redundant serial ports

Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the I/O ports.

The board provides one output latch to control the status of the two 125-vdc digital output channels (CH0_OUT/ and CH1_OUT/) and two coil monitoring circuits. When one of the DO channels is set on, the corresponding CHx_OUT/ signal from the latch forward biases a solid-state switch, passing 125-vdc power from input source to the output port for that channel. When a DO channel is set off, the microprocessor can activate the coil monitoring circuit. In order for the circuit to produce meaningful results, the onboard software prevents the DO channel and the coil monitoring circuit from being enabled at the same time.

The microprocessor reads input status by running separate read cycles to the two input buffers. The low order byte contains the digital image of PT01/ through PT08/. The high order byte contains the digital image of PT09/ through PT11/, CH0_RDY/, CH1_RDY/, CH0_PWR/, CH1_PWR/, SICH0/, AND SICH1/. In addition to the 17 bits of input data, the microprocessor also can read the status of the excitation voltage lines VSEN/, VSEN2/, and VSEN3/. These signals are routed directly to three pins of programmable I/O port P2 of the microprocessor.

The Link address data input port and Redundant serial ports are covered in document DS901-000-02 I/O Board Module Detailed Design Specification.

3.5 Input Channel Operation

The HFC-DC34 board contains 20 input channels composed of 11 general purpose DI channels, two coil continuity inputs, two power monitor inputs, two seal-in status inputs, and a separate status monitor for the three excitation voltage lines. Each of the DI channels is composed of a low-pass input filter and an optocoupler. The input filter is designed to reject any input signal having a pulse width less than 10 ms in duration, and the optocoupler isolates the internal logic circuitry from the field wiring. When one of these channels receives an active input signal, the optocoupler becomes forward biased and produces a low active output. While any of these outputs is active, the corresponding LED will light. The input circuit for the three VSEN/ input signals is identical, except they do not have an LED indication.

Each of the two input circuits for the 125-vdc power monitor consists of a low pass filter, and an optocoupler. When the 125-vdc power source is present for one or both input channels, the dc signal at the input of the low pass filter network activates a corresponding optocoupler to produce a low active output (CH0_PWR/ and/or CH1_PWR/). If either the CH0_PWR/ or the CH1_PWR/ signal is active, the PWR PRESENT0 LED or PWR PRESENT1 LED lights respectively.

The coil monitor circuit consists of a voltage divider connected to the 125-vdc power source, a low pass filter, and two optocouplers. When the microprocessor deactivates the CHx_OUT/ signal, one optocoupler passes the 125-vdc power source to the input of the voltage divider. This circuit then applies a significantly reduced voltage across the ports of the DO channel. If an external coil is present, a small current passes through the voltage divider network to forward bias the monitoring optocoupler, which then produces a low active CHx_RDY/ status output. If the external circuit is open, no current flows through the circuit, and the monitoring optocoupler remains cut off. If either the CH0_RDY/ or the CH1_RDY/ signal is active, the CH0/1 RDY LED lights.

The seal-in status consists of 125VDC being regulated to 5VDC. The availability of the 5VDC is read by the onboard microprocessor for each of the two channels. When the seal-in circuitry is active (true) the onboard microprocessor will not initiate failsafe for the corresponding DO channel in the event of ICL timeout.

3.6 Hardware Connections

The HFC-DC34 board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Pin assignments for the P1 connector are identical for all I/O boards and can be found in document DS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each DI channel can be configured for either isolated or common mode operation on an individual basis. When operating in common mode, excitation voltage is supplied from this board to the field device being monitored. When operating in isolated mode, external equipment must supply the power to enable or disable the DI input circuit. Table 2 lists the DIP switch settings and signal assignments required to configure each channel for either mode of operation.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	XXXXXXXXX	P2-C1	XXXXXXXXX
P2-A2	XXXXXXXXX	P2-B2	XXXXXXXXX
P2-C2	XXXXXXXXX	P2-A3	XXXXXXXXX
P2-C3	XXXXXXXXX	P2-A4	XXXXXXXXX
P2-C4	XXXXXXXXX	P2-A5	XXXXXXXXX
P2-B5	XXXXXXXXX	P2-C5	XXXXXXXXX
P2-A6	XXXXXXXXX	P2-C6	XXXXXXXXX
P2-A7	XXXXXXXXX	P2-C7	XXXXXXXXX
P2-A8	XXXXXXXXX	P2-B8	XXXXXXXXX

Table 1(Continued). Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-C8	XXXXXXXXX	P2-A9	XXXXXXXXX
P2-C9	XXXXXXXXX	P2-A10	XXXXXXXXX
P2-C10	XXXXXXXXX	P2-A11	XXXXXXXXX
P2-B11	XXXXXXXXX	P2-C11	XXXXXXXXX
P2-A12	XXXXXXXXX	P2-C12	XXXXXXXXX
P2-A13	XXXXXXXXX	P2-C13	XXXXXXXXX
P2-A14	XXXXXXXXX	P2-B14	XXXXXXXXX
P2-C14	XXXXXXXXX	P2-A15	XXXXXXXXX
P2-C15	XXXXXXXXX	P2-A16	XXXXXXXXX
P2-C16	XXXXXXXXX	P2-A17	XXXXXXXXX
P2-B17	XXXXXXXXX	P2-C17	XXXXXXXXX
P2-A18	XXXXXXXXX	P2-C18	XXXXXXXXX
P2-A23	XXXXXXXXX	P2-B23	XXXXXXXXX
P2-C23	XXXXXXXXX	P2-A24	XXXXXXXXX
P2-B24	XXXXXXXXX	P2-C24	XXXXXXXXX
P2-A25	XXXXXXXXX	P2-B25	XXXXXXXXX
P2-C25	XXXXXXXXX	P2-A26	XXXXXXXXX
P2-B26	XXXXXXXXX	P2-C26	XXXXXXXXX
P2-A27	XXXXXXXXX	P2-B27	XXXXXXXXX
P2-C27	XXXXXXXXX	P2-A28	XXXXXXXXX
P2-B28	XXXXXXXXX	P2-C28	XXXXXXXXX
P2-A29	XXXXXXXXX	P2-B29	XXXXXXXXX
P2-C29	XXXXXXXXX	P2-A30	XXXXXXXXX
P2-B30	XXXXXXXXX	P2-C30	XXXXXXXXX
P2-A31	XXXXXXXXX	P2-B31	XXXXXXXXX
P2-C31	XXXXXXXXX	P2-A32	XXXXXXXXX
P2-B32	XXXXXXXXX	P2-C32	XXXXXXXXX

Table 2. Input Connection Summary

Channel No.	Type	Positive	Negative	Dipswitch
1	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
2	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
3	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
4	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
5	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
6	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
7	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
8	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
9	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
10	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX
11	XXXX	XXXX	XXXX	XXXX
	XXXX	XXXX	XXXX	XXXX

4. Software Detailed Design Specification

The HFC-DC34 board monitors a total of 20 DI channels. The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DC34 board.

4.1 I/O Scan Module

This I/O Scan Module performs the I/O scan for 11 standard DI channels, two coil continuity status inputs, 2 power monitor status inputs, and two seal in status inputs. It reads the status of three interrogation voltages and the two bytes of input data during each scan. The loss of any interrogation voltages means that four or more of the DI images may not be valid, so the module will not update DI images with new readings if no interrogation voltage is present. If any interrogation voltage input is false, the Interrogation Voltage Off error bit in the diagnostic byte will be set to indicate a hardware fault. This information will be reported to the controller in the response to a diagnostic request message.

Normally, the DI images are transferred to the Scan Working Buffer when at least one of three interrogation voltages is present. However, to avoid missing information on the controller side, an interrogation voltage failure counter is used in the I/O scan process. This counter is incremented during each scan cycle where all interrogation voltages are missing.

When the accumulated count exceeds a predefined limit, the DI images in the Scan Working Buffer will be updated and reported to the controller even if no interrogation voltage is present. This counter will remain reset as long as any interrogation voltage line is present.

If a DO channel is set ON, the corresponding coil continuity status input is not meaningful. So the coil continuity status will be reported as "TRUE" to prevent spurious error indications. Only when the corresponding DO channel is not ON will the actual coil continuity status be reported back to the HFC-SBC06 controller.

4.2 Process Command routine

For normal update messages, this routine reads the one byte output image for two output channels from command message and transfers that image to output data latch. UCP diagnostics messages are processed as described in HFC-6000 I/O Board Module Detailed Design Specification DS002-000-92.

4.3 Data Structure

This section describes the structure of the I/O data images and provides a list of the programmable ports controlled by the software.

4.3.1 I/O Scan Data

The HFC-DC34 board has 2 DO channels and 11 DI channels. The data field of poll messages received from the HFC-SBC06 controller has the following structure:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	CH1_OUT/	CH0_OUT/

The data field of the response message to the HFC-SBC06 Controller has the following structure:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1
2	Power Source 1	Power Source 0	Coil 1 Continuity	Coil 0 Continuity	Seal In CH0	PT11	PT10	PT9

4.3.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 3. Programmable Ports Used for HFC-DC34 Board

Port	Description	Implementation
P1.0	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.1	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.2	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.3	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.4	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.5	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.7	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P2.1	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P2.3	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P2.4 P2.5 P2.6	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
Port 1 Control Register	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX

4.3.3 Failsafe Function

The hardware assembly includes an onboard seal-in circuit. When the seal-in input is configured and the onboard latch enable switch (S1) is closed, the seal-in circuit latches in the true state of the DO signal. The purpose of this circuit is to maintain the energized state of the DO signal even if power is lost from the control system. (The power required to maintain this state must be supplied from the external field equipment.)

Seal-in status is included with the DI image read by the microprocessor during each scan cycle. In the event of ICL timeout, the microprocessor checks seal-in status. If seal-in status is true, then the microprocessor keeps the DO channel energized. If seal in status is false (either because the DO channel is off or the seal-in function is not configured), the microprocessor clears the DO latch for failsafe.

5. Module Implementation Description

5.1 Hardware Schematics

The schematic for the HFC-DC34 board is drawing 400468-01.

5.2 Hardware Components – Bill of Materials

The part number of the HFC-DC34 board is 40046701, and the bills of material are 400467-01 and 400467-81.

5.3 Software Source Code Listing

The HFC-DC34 board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- XXXXXXX
- XXXXXXX

6. Design Safety

Refer to MS901-000-02 for a discussion of design safety considerations for the HFC-6000 I/O Modules.

HFC Non-proprietary

DOOSAN

HF Controls

INFORMATION ONLY

HF Controls Corporation

HFC-6000 Product Line

HFC-AI16 Board
Detailed Design Specification

Sixteen Channel Analog Input Board

DS901-000-07

Rev D

Effective Date	2/2/2009
Author	Gregory Rochford
Reviewer	Pat Thibodeau
Approval	David Briner

XXXXXXXXXX

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Revision History

Date	Revision	Author	Changes
11/14/03	0	D. Bynum	Initial
11/19/03	A	D. Bynum	Review comments incorporated
2/13/06	B0	E. Schirmer	SCR 1361
10/17/06	B	D. Briner	SCR 1361 / CR2006-0249
3/2/07	C	J Taylor	SCR1766; restored software coverage to Rev B
2/2/09	D	G Rochford	Review comments incorporated

able of Contents

Section Title Page

1. INTRODUCTION 4

1.1 REFERENCES 4
1.2 SPECIAL TERMS AND ABBREVIATIONS 4

2.0 SPECIFICATIONS 4

3.0 CONTROLS AND INDICATORS 5

4.0 FUNCTIONAL DESCRIPTION 6

4.1 OVERVIEW 6
4.2 ONBOARD POWER DISTRIBUTION 6
4.3 RESET/INITIALIZATION 7
4.4 MEMORY STRUCTURE 7
4.5 INTERRUPT PROCESSING 8
4.6 MICROPROCESSOR PERIPHERAL PORTS 8
4.6.1 Analog Input (AI) control output port 8
4.6.2 A/D data input port 9
4.7 I/O PORTS 10

5.0 HARDWARE CONNECTIONS 10

6. SOFTWARE DETAILED DESIGN SPECIFICATION 10

6.1 BOARD INFORMATION 10
6.2 ANALOG INPUT SCAN ALGORITHM 13
6.2.1 Read Channel Raw Value 13
6.2.2 Calibration Test Routine 13

6.2.3 AI Algorithm 14
6.3 SINGLE CHANNEL ADJUSTMENT ALGORITHM 15
6.4 HFC-AI16F-BOARD SPECIFIC MODULES 16
6.4.1 I/O Scan Module 16
6.4.2 Process Command routine 16
6.5 DATA STRUCTURE 16
6.5.1 Scan Data 16

7. MODULE IMPLEMENTATION DESCRIPTION 17

7.1 HARDWARE SCHEMATICS 17
7.2 HARDWARE COMPONENTS – BILL OF MATERIALS 17
7.3 SOFTWARE SOURCE CODE LISTING 17

8. DESIGN SAFETY 17

List of Tables

Section Title Page

Table 1. Connector P2 Pinout Summary 11
Table 2. Input Connection Summary 12

1. Introduction

The HFC-AI16 assembly is a 16-channel analog input board. This assembly operates as a standard AI board in an HFC-6000 control system. It receives analog input signals from field equipment at the plant and performs A/D conversion for each channel at regular intervals. The HFC-SBC06 controller initiates communication with a configured HFC-AI16 board during its regular scan cycles, and the HFC-AI16 board returns the current digital image for all input channels.

Descriptions and discussions of the architectural and design descriptions of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-AI16 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-AI16 board will be presented using design, implementation, and configuration information.

1.1 References

700901-06	HFC-6000 I/O Card Requirements Specification
MS901-000-02	HFC-6000 Product Line, I/O Module Design Specification
DS901-000-02	HFC-6000 Product Line, I/O Module Detailed Design Specification
40043301	HFC-AI16 Schematic
WI-ENG-106	Development of Hardware Design Specification

1.2 Special Terms and Abbreviations

I/O	Input/Output
LSB	Least Significant Bit
RAM	Random Access Memory
AI16F	0-20mA 16 Channel Analog Input
AI16E	0-10V 16 Channel Analog Input
AI16R	0-5V 16 Channel Analog Input
A/D	Analog to Digital Converter

2.0 Specifications

- Environmental Extremes

Temperature:	0° to 55° C (operating)
	0° to 70° C (storage)
Relative Humidity:	5% to 95%, non-condensing

- Power Requirements

External Power Supply: +24 vdc, 0.3 A maximum load.
Excitation voltage: +24 vdc with resetable fuse for each pair of channels and 0.5 A fuse for the combined load

- Onboard Clock Rate
  Microprocessor Clock: 22.1184 MHz

- Input Signal Requirements
  Signal:

AI16F	249Ω input resistor accepts 0 to 20mA.
AI16E	1 MΩ input resistor accepts 0 to 10V.
AI16R	1 MΩ input resistor accepts 0-5V.

Accuracy: Designed to read input signals accurately to .1% of full scale.

3.0 Controls and Indicators

The firmware determines the overall operating characteristics of the hardware on the HFC-AI16 board. The HFC-AI16 board includes the set of four LEDs common to all I/O board types (DS901-000-02). In addition, the board also includes six jumpers, two potentiometers, three switches, and nine fuses. The function of these components is as follows:

Jumpers

W36 Installed to supply 24-vdc excitation power for common AI channels.

W37 Installed to make the analog return and digital return electrical common.

E1-E2 Installed during calibration to disable both the NMI signal. When this jumper is removed, the D-latch U41-A activates a high NMI signal.

E5-E6 Not currently defined.

Potentiometers

R97 Enables the manual adjustment of the ADC offset voltage.

R98 Enables the manual adjustment of the ADC gain.

Switches

SW1 Enables user to reset the 80C188EB microprocessor.

S1 8-position DIP switch enables the user to configure channels 1 through 8 for either common or isolated mode operation (SW ON = COMMON) in any combination.

S2 8-position DIP switch enables the user configure channels 8 through 16 for either common or isolated mode operation (SW ON = COMMON) in any combination.

Fuses

F1, F2, F4-F9 Provide separate overload protection on the 24-vdc excitation voltage line for each pair of input channels

F3 Provides common overload protection for the excitation power source supplied to all 16 input channels.

4.0 Functional Description

The HFC-AI16 AI board is controlled by an onboard 80C188EB microprocessor and provides an interface for up to 16 analog field inputs for an HFC-6000 control system. The analog inputs are converted into digital images and stored in onboard RAM. The system controller accesses these values from RAM by sending the appropriate message to the HFC-AI16 board.

4.1 Overview

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification. The major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Performs reset and initialization of onboard hardware.
- Responds to data transmissions from the HFC-6000 controller.
- Samples the analog data from each of the 16 AI channels.
- Performs the Analog-to-Digital (A/D) conversion of field inputs.
- Stores the digital image for each channel in onboard memory.

4.2 Onboard Power Distribution

The board receives redundant 24-vdc power feeds from the backplane connector J1. The two power feeds are diode auctioneered and routed to the following components:

- An onboard voltage regulator converts the 24-vdc source power to +5-vdc power required for logic components on the HFC-AI16 board.

- An onboard voltage regulator (PS1) converts the 24-vdc source power to ± 15-vdc non-isolated power. This supplies operating power for the non-isolated analog circuitry.

- An onboard voltage regulator (PS2) converts the 24-vdc source power to ± 15-vdc for the isolated analog circuitry.

When jumper W36 is installed, a 24-vdc power line is divided into 8 branches. Each branch includes a separate reset-able line fuse and supplies excitation power for two AI channels.

4.3 Reset/Initialization

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Watchdog Timer Functions

The HFC-AI16 board is equipped with a watchdog timer circuit composed of a one-shot (U40-A) and a D-latch (U41-A). During initial power-up or manual reset, the output from the Micro Monitor chip holds both the one-shot and D-latch in their reset state. When the /RESIN signal assumes a high state, the one-shot can respond to outputs from the microprocessor.

Programmable output from port P2.1 of the microprocessor is routed to the negative trigger input of the one-shot. During normal operation of the onboard software, the microprocessor must produce a low output pulse from this port once every 950 ms to keep the one-shot at a triggered state. While the one-shot remains triggered, the negative output keeps LED DS5-1 lit, and the positive output enables the transmission function of the redundant serial ports. If the microprocessor stops normally processing its software, the one-shot times out after a period of 950 ms. The resulting transition of the low active output clocks the D-latch, and the low state of the high active output disables transmission over the serial links.

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4.4 Memory Structure

Memory on the HFC-AI16 board is organized into two banks of private memory for the microprocessor. Private memory for the 80C188EB microprocessor consists of one bank of EPROM and one bank of RAM. The private memory banks are connected directly to the address and data lines of the microprocessor.

80C188EB Microprocessor Upper Memory

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80C188EB Microprocessor Low Memory

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4.5 Interrupt Processing

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4.6 Microprocessor Peripheral Ports

The microprocessor controls the following peripheral ports:

- Analog Input (AI) control output port
- A/D data input port
- Link address data input port
- Redundant serial port

The link address input port, and the redundant serial port are common to all I/O board types, and are described in document DS901-000-02. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the three I/O ports

4.6.1 Analog Input (AI) control output port

The interface between the microprocessor and the analog section of the board consists of a 16-bit A/D converter, an 8-bit latch, and two BCD-to-decimal decoders. Bits 4 through 7 (formatted as AD0 through AD3) of the data transferred to the latch contain a 4-bit code for the AI channel to be read, and bit 1 (AD6) controls the R/C output to the A/D converter. The 4-bit channel selection code is routed from the output ports of the latch to the input of both BCD-to-decimal decoders via the 8-bit buffer. The buffer has two output enable ports controlled by separate signals from the microprocessor. OE1 is controlled by the output from P1.6, and OE2 is controlled by the output from P1.5. When the microprocessor activates the output from P1.6, the channel select code controls selection of PT00 through PT07; when the

output from P1.5 is activated, the channel select code controls selection of PT08 through PT17. PT16 and PT17 control selection of zero and span voltage inputs for a calibration cycle. The active output signal then forward biases the optocoupler for the selected channel, and it passes the analog input from the field device to an input amplifier.

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Input channels PT16 and PT17 provide precision voltage levels to enable the microprocessor to evaluate the calibration of the analog circuitry. When PT16 is selected, the onboard circuitry supplies a fixed signal of 0.91-vdc to the input amplifier. When PT17 is selected, the circuitry supplies a fixed signal of 10-vdc to the input amplifier. The microprocessor reads the count values for these two inputs and compares them with expected values from memory. If the drift is less than a fixed tolerance value in memory, the software can calculate a correction factor for each of the field inputs. If the drift exceeds the tolerance value, the software can trigger a calibration error alarm.

4.6.2 A/D data input port

The microprocessor uses the following sequence to select an input channel, initiate A/D conversion, and read the resulting 16-bit digital image from the ADC.

1. The microprocessor writes the channel selected code and a high R/C signal to the output latch.

2. After completion of the write cycle, the microprocessor sets either programmable port P1.5 or P1.6 low to enable generation of the required port selection output signal.

3. The selected channel supplies its signal to the input of the analog circuitry. The high state of the R/C and CS/ signals enable internal sample-and-hold circuits in the ADC to acquire the input signal.

4. After a delay to allow signal stabilization, the microprocessor sets the R/C and CS/ signals low to start the conversion process. The sample-and-hold in the ADC retains the signal acquired during the previous interval.

5. The ADC sets the STS (BUSY/) signal low at the start of the conversion cycle. When the conversion cycle is complete, the STS signal returns to a high level.

6. The low-to-high transition of the STS signal triggers the INT4 input to the microprocessor.

7. The microprocessor sets the R/C signal high and then runs two read cycles to the A/D data input port with the CS/ signal low. The microprocessor sets the AD0 signal low to access the most significant byte of data and sets it high to access the least significant byte of data.

8. The microprocessor can repeat steps 4 through 7 to read the digital image from the sample-and-hold circuit without repeating the acquisition cycle.

4.7 I/O Ports

The HFC-AI16 board contains 16 input channels for analog input signals from external field equipment. Each channel includes a low-pass filter to block electrical noise and an optocoupler to isolate the onboard circuitry from the field circuitry. Each channel includes a connection to an onboard DIP switch that permits configuration for either common or isolated operation on a channel-by-channel basis. When a channel is configured for common mode operation, 24-vdc power is supplied from the board to the field transducer that produces the input signal. When a channel is configured for isolated operation, that channel is electrically isolated from all other components on the board, and the field transducer must provide the power source to drive the input signal.

5.0 Hardware Connections

The HFC-AI16 board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-AI16 and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each AI channel can be configured for either isolated or common operation on an individual basis. Table 2 lists connection requirements for both isolated and common configurations for each channel.

6. Software Detailed Design Specification

The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AI16F board.

6.1 Board Information

The HFC-AI16F board has a total of 16 identical AI channels. Each channel will provides positive and negative terminal connections for a signal in the range of 0-20 mA. The board contains a single A/D converter that will be configured to produce a 16-bit digital image of the analog input for each channel.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	XXXXXXX	P2-C1	XXXXXXX
P2-A2	XXXXXXX	P2-C2	XXXXXXX
P2-A3	XXXXXXX	P2-C3	XXXXXXX
P2-A4	XXXXXXX	P2-C4	XXXXXXX
P2-A5	XXXXXXX	P2-C5	XXXXXXX
P2-A6	XXXXXXX	P2-C6	XXXXXXX
P2-A7	XXXXXXX	P2-C7	XXXXXXX
P2-A8	XXXXXXX	P2-C8	XXXXXXX
P2-A9	XXXXXXX	P2-C9	XXXXXXX
P2-A10	XXXXXXX	P2-C10	XXXXXXX
P2-A11	XXXXXXX	P2-C11	XXXXXXX
P2-A12	XXXXXXX	P2-C12	XXXXXXX
P2-A13	XXXXXXX	P2-C13	XXXXXXX
P2-A14	XXXXXXX	P2-C14	XXXXXXX
P2-A15	XXXXXXX	P2-C15	XXXXXXX
P2-A16	XXXXXXX	P2-C16	XXXXXXX
P2-A17	XXXXXXX	P2-C17	XXXXXXX
P2-A18	XXXXXXX	P2-C18	XXXXXXX
P2-A19	XXXXXXX	P2-C19	XXXXXXX
P2-A20	XXXXXXX	P2-C20	XXXXXXX
P2-A21	XXXXXXX	P2-C21	XXXXXXX
P2-A22	XXXXXXX	P2-C22	XXXXXXX
P2-A23	XXXXXXX	P2-C23	XXXXXXX
P2-A24	XXXXXXX	P2-C24	XXXXXXX

Table 2. Input Connection Summary

Channel No.	Type	Positive	Negative	Dipswitch
1	Isolated	P2-A1	P2-C1	XXXXXXX
	Common	P2_A2	P2-A1	XXXXXXX
2	Isolated	P2-A3	P2-C3	XXXXXXX
	Common	P2_C2	P2-A3	XXXXXXX
3	Isolated	P2-A4	P2-C4	XXXXXXX
	Common	P2_A5	P2-A4	XXXXXXX
4	Isolated	P2-A6	P2-C6	XXXXXXX
	Common	P2_C5	P2-A6	XXXXXXX
5	Isolated	P2-A7	P2-C7	XXXXXXX
	Common	P2_A8	P2-A7	XXXXXXX
6	Isolated	P2-A9	P2-C9	XXXXXXX
	Common	P2_C8	P2-A9	XXXXXXX
7	Isolated	P2-A10	P2-C10	XXXXXXX
	Common	P2_A11	P2-A10	XXXXXXX
8	Isolated	P2-A12	P2-C12	XXXXXXX
	Common	P2_C11	P2-A12	XXXXXXX
9	Isolated	P2-A13	P2-C13	XXXXXXX
	Common	P2_A14	P2-A13	XXXXXXX
10	Isolated	P2-A15	P2-C15	XXXXXXX
	Common	P2_C14	P2-A15	XXXXXXX
11	Isolated	P2-A16	P2-C16	XXXXXXX
	Common	P2_A17	P2-A16	XXXXXXX
12	Isolated	P2-A18	P2-C18	XXXXXXX
	Common	P2_C17	P2-A18	XXXXXXX
13	Isolated	P2-A19	P2-C19	XXXXXXX
	Common	P2_A20	P2-A19	XXXXXXX
14	Isolated	P2-A21	P2-C21	XXXXXXX
	Common	P2_C20	P2-A21	XXXXXXX
15	Isolated	P2-A22	P2-C22	XXXXXXX
	Common	P2_A23	P2-A22	XXXXXXX
16	Isolated	P2-A24	P2-C24	XXXXXXX
	Common	P2_C23	P2-A24	XXXXXXX

6.2 Analog Input Scan Algorithm

Every scan cycle, the scan module performs an AI calibration test, and then calculates the AI offset and gain. If any errors occur during the calibration test, the scan module sets an error bit in the diagnostics byte, marks the normal response as a bad response, and returns.

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XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

After finishing with all channels, the module stores the adjusted raw value in a filter buffer, and calculates a moving average of all records of raw value in the buffer. The filter buffer's size is predefined. Every scan cycle, a new reading of raw value is added to the buffer, and the earliest reading in the buffer is pushed out.

There are two calibration parameters for each channel that are originally obtained from the EPROM. The software uses these parameters to adjust the filtered AI raw value of each channel for better accuracy. Then the adjusted input images will be saved in the scan work buffer. Refer to Section 4.3 "Single Channel Adjustment Algorithm" for the adjustment algorithm using calibration parameters.

6.2.1 Read Channel Raw Value

During each AI signal reading, control signals are used to initialize the A/D converter (ADC), and to sample the input signal from the selected channel. The output signal STS is linked with the interrupt signal INT4 to the microprocessor. This signal indicates the status of the ADC cycle. It goes low at the beginning of a conversion and returns high when the conversion cycle is complete. The interrupt request register REQST is used to check the ADC conversion complete bit (INT4).

The module takes a predefined number of AI samples per channel and averages the raw count value. The main sequence to scan the image for one AI channel is as follows:

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6.2.2 Calibration Test Routine

This routine gets the raw values from the low calibration point and the high calibration point. If the low or high calibration point raw value is out of range, the routine will return with error. If there are no errors, the routine calculates AI offset and gain by using low and high calibration point raw values.

For the 15-bit AD converter, the raw value of the low calibration point should be within 0B18H ± A0H counts, and the raw value of the high calibration point should be within 79E0H ± A0H counts. When the raw values are within the acceptable ranges, the calculation of AI offset and AI gain is as follows:

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

6.2.3 AI Algorithm

For the 15-bit AD converter, the calculation of AI image is as follows:

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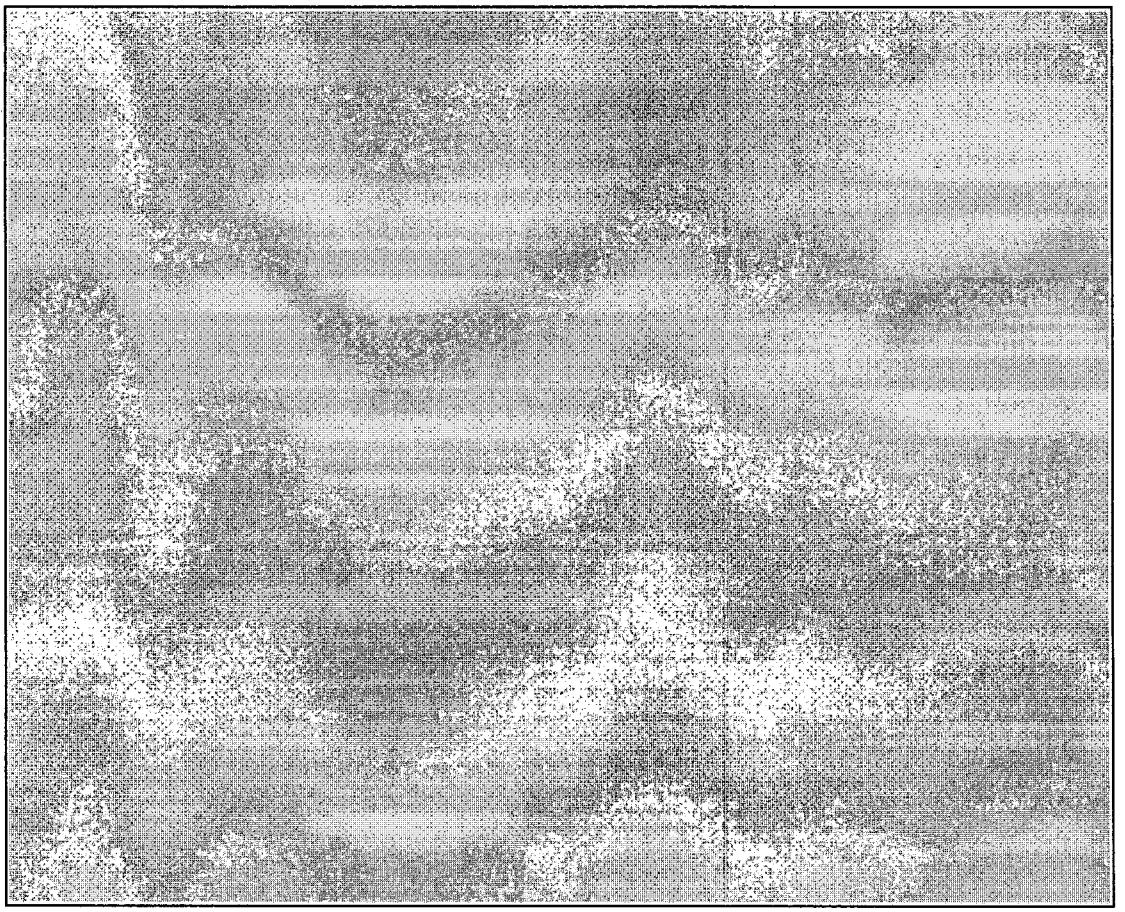
Figure 1. AI Algorithm Explanation



6.3 Single Channel Adjustment Algorithm

The single channel adjustment algorithm is used in the software of AI16I, AO8F, AC36 boards to achieve better accuracy. Offset and gain for each channel will be determined by testing or default to zero, and an EPROM file will be built incorporating the offset and gain parameters in a specific location of EPROM memory. The first time the I/O software enters the scan module, the software obtains the offset and gain parameters from the specific memory location in EPROM to calculate actual raw value for 4 mA and 20 mA of each analog input or analog output channel and saves them in a buffer as two arrays: CALZERO and CALGAIN.

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XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

The CALZERO array stores for each channel the actual value for 4 mA, i.e. STDZERO adjusted by offset parameter for that channel. The CALGAIN array stores for each channel the actual value for 20 mA, i.e. STDGAIN adjusted by gain parameter for that channel.

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6.4 HFC-AI16F-board Specific Modules

6.4.1 I/O Scan Module

The SCAN module performs AI scan for sixteen channels

6.4.2 Process Command routine

For normal update messages, this routine doesn't do anything because there is no AO channel on card. UCP diagnostics messages are processed as described in document DS002-0000-02.

6.5 Data Structure

6.5.1 Scan Data

The data field of the response message sent to the HFC-SBC06 controller contains AI images for sixteen channels as follows:

Table 3. Byte Assignments For Scan Data

Byte	AI	Byte	AI	Byte	AI	Byte	AI
0	XXXXX	8	XXXXX	16	XXXXX	24	XXXXX
1	XXXXX	9	XXXXX	17	XXXXX	25	XXXXX
2	XXXXX	10	XXXXX	18	XXXXX	26	XXXXX
3	XXXXX	11	XXXXX	19	XXXXX	27	XXXXX
4	XXXXX	12	XXXXX	20	XXXXX	28	XXXXX
5	XXXXX	13	XXXXX	21	XXXXX	29	XXXXX
6	XXXXX	14	XXXXX	22	XXXXX	30	XXXXX
7	XXXXX	15	XXXXX	23	XXXXX	31	XXXXX

7. Module Implementation Description

7.1 Hardware Schematics

The schematic for the HFC-AI16F board is drawing 400433-01.

7.2 Hardware Components – Bill of Materials

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

7.3 Software Source Code Listing

The HFC-AI16F board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

8. Design Safety

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

DOOSAN

HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-AO8 Board
Module Detailed Design Specification

Eight Channel Analog Output Board

DS901-000-08

Rev D

INFORMATION ONLY

Effective Date	2/2/2009
Author	Gregory Rochford
Reviewer	Pat Thibodeau
Approval	David Briner

XXXXXXXXXX

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Revision History

Date	*Revision*	*Author*	*Changes*
11/14/03	0	D. Bynum	Initial
11/21/03	A	D. Bynum	Review comments incorporated
3/08/06	B	D. Briner	SCR 1298
3/2/07	C	J Taylor	SCR 1766; restored software coverage to Rev B.
2/2/09	D	G Rochford	Review comments incorporated

Table of Contents

Number **Title** **Page**

1.0 INTRODUCTION....4
1.1 REFERENCES....4
1.2 SPECIAL TERMS AND ABBREVIATIONS....4
2.0 SPECIFICATIONS....4
3.0 CONTROLS AND INDICATORS....5
3.1 JUMPERS....5
3.2 FUSES....5
4.0 FUNCTIONAL DESCRIPTION....5
4.1 OVERVIEW....6
4.2 POWER DISTRIBUTION....6
4.3 RESET/INITIALIZATION....6
4.4 MEMORY STRUCTURE....7
4.5 INTERRUPT PROCESSING....7
4.6 MICROPROCESSOR PERIPHERAL PORTS....7
4.6.1 AO Interface....7
4.6.2 Fail safe condition data input port....8
5.0 HARDWARE CONNECTIONS....9
6.0 SOFTWARE DETAILED DESIGN SPECIFICATION....10
6.1 BOARD INFORMATION....10
6.2 ANALOG OUTPUT SCAN ALGORITHM....10
6.3 SINGLE CHANNEL ADJUSTMENT ALGORITHM....10
6.4 HFC-AO8F BOARD SPECIFIC MODULES....11
6.4.1 I/O Scan Module....11
6.4.2 Process Command routine....11
6.5 DATA STRUCTURE....11

6.5.1 Scan Data 12

7.0 MODULE IMPLEMENTATION DESCRIPTION 12

7.1 HARDWARE SCHEMATICS 12
7.2 HARDWARE COMPONENTS – BILL OF MATERIALS 12
7.3 SOFTWARE SOURCE CODE LISTING 12

8.0 DESIGN SAFETY 12

List of Tables

Number **Title** **Page**

Table 1. AO Failsafe Control 9
Table 2. Data Justification of AO Images 9
Table 3. Connector P2 Pinout Summary 10
Table 4. Byte Assignments For Scan Data 12

1.0 INTRODUCTION

The HFC-AO8 assembly is an 8-channel analog output board. This assembly operates as a standard AO board in an HFC-6000 control system. It receives digital output images from the system controller and performs D/A conversion for each channel at regular intervals. The HFC-SBC06 controller initiates communication with a configured HFC-AO8 board during its regular scan cycles, and the HFC-AO8 board receives the current digital image for all output channels from the poll message and returns current status.

Descriptions and discussions of the architectural and design descriptions of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Card Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-AO8 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-AO8 board will be presented using design, implementation, and configuration information.

1.1 REFERENCES

700901-06	HFC-6000 I/O Card Requirements Specification
400473-01	HFC-AO8F Schematic
400472-01	HFC-AO8F 8 channel, 4-20mA Assembly
400472-02	HFC-AO8E 8 channel, 0-10VAssembly
WI-ENG-106	Development of Hardware Design Specification
MS901-000-02	HFC-6000 Product Line, I/O Module Design Specification
DS901-000-02	HFC-6000 Product Line, I/O Module Detailed Design Specification

1.2 SPECIAL TERMS AND ABBREVIATIONS

I/O	Input/Output
LSB	Least Significant Bit
RAM	Random Access Memory
AO8F	0-20mA 8 Channel Analog Output
AO8E	0-10V 8 Channel Analog Output
D/A	Digital to Analog Converter

2.0 SPECIFICATIONS

- Environmental Extremes
  - Temperature: 0° to 55° C (operating)
    0° to 70° C (storage)
  - Relative Humidity: 5% to 95%, non-condensing
- Power Requirements

External Power Supply: +24 vdc, 0.4 A maximum load.

- Onboard Clock Rate
  Microprocessor Clock: 22.1184 MHz

Output Channel Rating: 0 to 20 mA (-01 assembly) or 0 to 10 V (-02 assembly) with 1/16-A line fuse for each channel and a 0.5-A line fuse for all eight channels

- Mounting Requirements: Mounts vertically in an HFC-6000 chassis

3.0 CONTROLS AND INDICATORS

The firmware determines the overall operating characteristics of the hardware on the HFC-AO8 board. The HFC-AO8 board only includes the set of four LEDs and one switch that are common to all I/O board types (DS901-000-02). However, the board does include eight jumpers and nine fuses. These devices and the functions that they control are as follows:

3.1 JUMPERS

W3-W5 Fail-state jumpers, refer to paragraph 4.6.2 in this document for more information on the fail-state jumpers.

W37 Installed to make analog return and digital return electrical common.

E1-E2 Installed during calibration only to disable the NMI signal. When this jumper is removed, the D-latch U41-A activates a high NMI signal. E1-E2 should be removed for normal operation.

E5-E6 Function not currently defined.

3.2 FUSES

F1, F2, F4-F9 Provide separate overload protection for each AO channel.

F3 Provides common overload protection for the 24-vdc power source to the eight output drivers.

4.0 FUNCTIONAL DESCRIPTION

The HFC-AO8 board is controlled by an onboard 80C188EB microprocessor and provides a hardware interface between an HFC-6000 control system and field equipment requiring analog control signals.

4.1 OVERVIEW

The HFC-AO8 has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Card Module Design Specification. The major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Performs reset and initialization of onboard hardware.
- Responds to data transmissions from the HFC-6000 controller.
- Receives AO images for each channel from the controller and stores that data in local memory.
- Transfers AO images from memory to the Digital-to-Analog (D/A) converter for each channel.
- Controls the D/A conversion process.

4.2 POWER DISTRIBUTION

The board receives redundant 24-vdc power feeds from the back plane connector J1. The two power feeds are diode auctioneered, and the combined 24-vdc power line is divided into four branches. One branch is routed to the input of an onboard voltage regulator. The second branch is routed through a 0.5-A onboard line fuse. The remaining two branches are routed to two ±15-vdc power supplies. These separate branches provide operating power for the following functions:

- The onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for logic components on the HFC-AO8 board.

- The fused 24-vdc power trace is routed to the VCC port of the output driver for each Analog Output (AO) channel.

- The two +15-vdc supplies provide operating power to the DAC for each channel. One of the +15-vdc supplies also provides power to a precision 2.5-vdc regulator that provides a reference voltage to all eight DACs.

4.3 RESET/INITIALIZATION

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4.4 MEMORY STRUCTURE

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4.5 INTERRUPT PROCESSING

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4.6 MICROPROCESSOR PERIPHERAL PORTS

The microprocessor controls the following peripheral ports:

- Digital-to-Analog Converter (DAC) data output port
- Analog Output (AO) select output port
- Fail safe condition data input port
- Link address data input port
- Redundant serial port.

The Link Address input port, and the Redundant serial port are covered for the general case of I/O cards, therefore, they are not discussed here. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the three I/O ports

4.6.1 AO INTERFACE

The interface between the microprocessor and the analog outputs includes both the DAC data output port and the AO select output port. The interface between the microprocessor and each AO channel consists of an 8-bit latch, a one-of-eight demultiplexer, and a separate D/A converter for each channel. Because each AO image consists of 12 bits, the microprocessor must run two write cycles to each DAC. The hardware design for the card requires that the microprocessor transfer the most significant (high) byte of data to the DAC first and then the least significant (low) byte. During the second write cycle, the microprocessor transfers both bytes of data to the internal DAC register, enabling the DAC process to begin. The overall process required for data transfer to a single DAC is as follows:

1. The microprocessor runs an I/O write cycle with programmable output port P1.0 pulled low to transfer the high byte of the AO image to the 8-bit latch. The latch retains this data until it is overwritten by a subsequent write cycle. The output ports of the latch control an 8-bit data bus that is connected to each of the DAC chips.

2. The microprocessor pulls programmable port P1.1 low (CSMSB/) to transfer the high byte of the AO image from the 8-bit data bus into the input register of all DAC chips simultaneously.

3. The microprocessor runs a second write cycle to transfer the low byte of the AO image to the 8-bit latch.

4. The microprocessor places the binary code for the AO channel being processed on address lines A01, A02, and A03. The one-of-eight demultiplexer uses this code to activate the chip select signal (CS/) for the DAC associated with this AO channel.

5. The low active CS/ signal transfers the low byte from the 8-bit data bus into the DAC for the selected channel, and it also transfers the entire AO image into the DAC register.

6. When the CS/ signal returns to a high state, the DAC begins the conversion process.

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX.

Once the AO image has been loaded into the DAC register, DAC automatically uses that data to perform D/A conversion, unless overridden by a failsafe condition (controlled by the FH/L and FH/C signals). Of the 16 bits in the DAC register, only 12 bits are used to represent the channel output value; and these 12 bits are either right or left justified in the register, depending on the logic state of the FH/L and FH/C signals (Table 2). The DAC converts the AO image into a corresponding current value, and the current signal provides the input to an amplifier, which produces an output signal between 0 and +5 vdc. This voltage is supplied to the input of a precision voltage-to-current converter, which produces an output signal having a range of 0 to 20 mA.

The DAC produces an analog output that has a full-scale range of 0 to 2.5 vdc. The individual analog channels condition the output to provide 0-20 mA (-01 assembly). The –02 assembly has 499 Ω resistors on each output channel that convert the 0-20 mA signal into a 0- 10 V signal.

4.6.2 FAIL SAFE CONDITION DATA INPUT PORT

The design of the HFC-AO8 includes three jumpers that are used to configure the card for one of thee failsafe modes: fail high, fail low, hold last state. Each failsafe jumper (W3, W4, and W5) controls the logic state of a separate input to an 8-bit buffer. The microprocessor can read the status of these jumpers by running a bus read cycle with programmable output port P1.0 pulled low. These inputs enable the software to determine the failure state selected by the jumper strapping. If the card looses communication with the controller, the software can XXX

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Table 1. AO Failsafe Control

Jumper	Status	Function
W4	XXXXX	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
W4	XXXXX	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
W5	XXXXX	
W4	XXXXX	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
W5	XXXXX	

Table 2. Data Justification of AO Images

W5	Most Significant Byte								Least Significant Byte							
ON	MSB											LSB	x	x	x	x
OFF	x	x	x	X	MSB											LSB
	8	7	6	5	4	3	2	1	8	7	6	5	4	3	2	1

5.0 HARDWARE CONNECTIONS

The HFC-AO8 card contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-AO8 and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 3.

Table 3. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	XXXXX	P2-C1	XXXXX
P2-A3	XXXXX	P2-C3	XXXXX
P2-A4	XXXXX	P2-C4	XXXXX
P2-A6	XXXXX	P2-C6	XXXXX
P2-A7	XXXXX	P2-C7	XXXXX
P2-A9	XXXXX	P2-C9	XXXXX
P2-A10	XXXXX	P2-C10	XXXXX
P2-A12	XXXXX	P2-C12	XXXXX

6.0 SOFTWARE DETAILED DESIGN SPECIFICATION

The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AO8F board.

6.1 BOARD INFORMATION

The AO8F card has a total of eight identical AO channels rated for 0-20 mA. Each channel includes a separate 12-bit D/A converter.

6.2 ANALOG OUTPUT SCAN ALGORITHM

An on-board fail-hi / fail-lo jumper provides option for using left justified or right justified output data for the D/A converter. Before writing analog output images to the D/A converters, the software checks if the jumper is installed. If it is installed, the software left-shifts each output image 4 bit positions to make it left-justified. (Each 12-bit image is stored as a single data byte.) If the jumper is not installed, the software leaves the AO images just as they are received from the controller.

There are two calibration parameters for each channel that were originally obtained from the EPROM. The software uses these parameters to adjust the output image of each channel for better accuracy. Then the software strobes the adjusted output image into D/A converter output for each channel. Refer to Section 6.3 for adjustment algorithm using calibration parameters.

6.3 SINGLE CHANNEL ADJUSTMENT ALGORITHM

The single channel adjustment algorithm is used in the software of AI16I, AO8F, AC36 cards to achieve better accuracy. Offset and gain for each channel will be determined by testing or default to zero, and an EPROM file will be built incorporating the offset and gain parameters in a specific location of EPROM memory. First time the I/O software enters scan module,

the software obtains the offset and gain parameters from the specific memory location in EPROM to calculate actual raw value for 4 mA and 20 mA of each analog input or analog output channel and saves them in a buffer as two arrays: CALZERO and CALGAIN.

For 12 bit: XXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXX

The CALZERO array stores for each channel the actual value for 4 mA, i.e. STDZERO adjusted by offset parameter for that channel. The CALGAIN array stores for each channel the actual value for 20 mA, i.e. STDGAIN adjusted by gain parameter for that channel.

Let BX = channel number, then

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXX

Both 12-bit and 15-bit adjustments are handled according to the board type. The 15-bit AI image requires over range and under range checks. The 12-bit AO does not have over range or under range; however, the algorithm sets any negative value to 0 and changes any value above $0FFF_H$ to $0FFF_H$ to prevent overflow.

6.4 HFC-AO8F BOARD SPECIFIC MODULES

6.4.1 I/O SCAN MODULE

The HFC-AO8F board firmware has an I/O scan module like all other I/O boards, but because this board has no input channels, this module has no function.

6.4.2 PROCESS COMMAND ROUTINE

For normal update messages, this routine reads eight AO images and transfers them to the Scan Work Buffer. UCP diagnostics messages are processed as described in document DS002-000-02.

6.5 DATA STRUCTURE

6.5.1 SCAN DATA

The data field of the request message coming from the HFC-SBC06 controller contains AO images for eight channels, as follows:

Table 4. Byte Assignments For Scan Data

Byte	AO	Byte	AO
0	XXXXX	8	XXXXX
1	XXXXX	9	XXXXX
2	XXXXX	10	XXXXX
3	XXXXX	11	XXXXX
4	XXXXX	12	XXXXX
5	XXXXX	13	XXXXX
6	XXXXX	14	XXXXX
7	XXXXX	15	XXXXX

7.0 MODULE IMPLEMENTATION DESCRIPTION

7.1 HARDWARE SCHEMATICS

The schematic for the HFC-AO8F board is drawing 400471-01.

7.2 HARDWARE COMPONENTS – BILL OF MATERIALS

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

7.3 SOFTWARE SOURCE CODE LISTING

The HFC-AO8F board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

8.0 DESIGN SAFETY

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

HFC Non-proprietary

HF Controls Corporation

HFC-6000 Product Line

HFC-AI4K
Module Detailed Design Specification

Pulse Input Board

DS901-000-12

Rev B

INFORMATION ONLY

Effective Date	2/4/2009
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HFC Proprietary

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Date	Revision	Author	Changes
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Table of Contents

1.0 INTRODUCTION 4

2.0 HFC-AI4K FUNCTIONAL DESCRIPTION 4

3.0 HARDWARE DETAILED DESIGN SPECIFICATIONS 4

3.1 MODULE SPECIFICATION 4
3.2 ONBOARD POWER DISTRIBUTION 5
3.3 INTERRUPT PROCESSING 5
3.4 MICROPROCESSOR PERIPHERAL PORTS 5
3.4.1 Counter Status Port 6
3.4.2 Port Addressing and Control 6
3.4.3 Input Channel Configuration 7
3.5 CONTROLS, JUMPERS, AND INDICATORS 9
3.5.1 Switches 9
3.5.2 Jumpers 11
3.5.3 Onboard Status Indicators 12
3.6 CONFIGURATION PROCEDURE 12
3.6.1 Hardware Setup Requirements 12
3.7 HARDWARE CONNECTIONS 13

4.0 SOFTWARE FUNCTIONAL DESIGN DESCRIPTIONS 14

4.1 BOARD SPECIFIC MODULES 14
4.1.1 I/O Scan Module 14
4.1.2 Display Functions During Normal Operation 15
4.1.3 Tuning Process 15
4.1.4 Process Command Routine 15
4.2 DATA STRUCTURE 15
4.2.1 Scan Data 15
4.2.2 Microprocessor Programmable Ports 15
4.2.3 Counter Status/Mode Port 17
4.2.4 Input Channels 17
4.2.5 Switch Input Port 17
4.2.6 Alphanumeric Display Messages 18

5.0 MODULE IMPLEMENTATION DESCRIPTIONS 19

5.1 HARDWARE SCHEMATICS 19
5.2 HARDWARE COMPONENTS – BILL OF MATERIALS 19
5.3 SOFTWARE SOURCE CODE LISTING 19

1.0 Introduction

The HFC-AI4K pulse input printed circuit board (PCB) provides four pulse input channels for an HFC-6000 control system. This assembly operates as a standard I/O board in an HFC-6000 control system. The four input channels of AI4K can be configured to either rate mode or accumulate mode. The rate mode is used to monitor input pulse rate and each input is reported as a standard 12-bit AI point. Accumulate mode is used to maintain a cumulative count of pulses being received and the values are reported as two consecutive AI points.

Descriptions and discussions of the architectural and design descriptions of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

Subsequent sections of this document provide detailed structure and design descriptions of the HFC-AI4K board, with concentration on the specific characteristics of an HFC-AI4K board. The design descriptions of the common software modules of I/O cards are covered in document DS901-000-02, HFC-6000 I/O Card Module Detailed Design Specification.

2.0 HFC-AI4K Functional Description

The HFC-AI4K board is controlled by an onboard 80C188EB microprocessor and provides an interface for up to four analog field inputs and four analog field outputs for an HFC-6000 control system. The AI4K board has onboard switches for manual configuration and status monitoring for each channel. It has an eight-character alphanumeric display to provide a visual indication of operating status.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification. Major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Controls reset and initialization functions.
- Supports channel configuration.
- Samples the pulse input data from each of the input channels.
- Stores the input data image for each channel in local memory.
- Respond to data transmissions from the HFC-6000 controller.

3.0 Hardware Detailed Design Specifications

3.1 Module Specification

- Environmental Extremes

Temperature:	0° to 55° C (operating)
	0° to 70° C (storage)
Relative Humidity:	5% to 95%, noncondensing

- Power Requirement
  External Power Supply: +24-vdc, 0.4 A maximum load.
  Interrogation Voltage: +48-vdc

- Onboard Clock Rate
  Microprocessor clock 22.1184 MHz

- Mounting Requirements: Mounts vertically in HFC-6000 board chassis.

- The HFC-AI8M PCB meets the requirements of seismic category I.

- Low memory provides 32K by 8-bits of nonvolatile RAM for temporary storage of message data being processed. Nonvolatile RAM is used to ensure that channel configuration parameters will be preserved when power is removed from the system.

- Pulse Input Channel Operating Limits

  Pulse rate: 0 Hz through 20 kHz
  Peak voltage level: 12-vdc to 150-vdc
  Peak input current: 10 ma (nominal)

3.2 ONBOARD POWER DISTRIBUTION

The board receives redundant 24-vdc power feeds from the backplane connector P1. The two power feeds are diode auctioneered, and an onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for components on the HFC-AI4K board.

The board receives interrogation power (nominally 48-vdc) from the backplane. Proper field input wiring permit the user to configure one or more channels to operate with this interrogation power source. Overload protection is provided by a common line fuse, and an optocoupler permits the microprocessor to monitor status of the power line.

3.3 INTERRUPT PROCESSING

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XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

3.4 MICROPROCESSOR PERIPHERAL PORTS

The microprocessor controls the following peripheral ports:

- Link address data input port

- Redundant serial port.
- Switch status input
- Counter status input
- Programmable counter I/O
- Display control
- Status input from each pulse input channel.

The link address input port, and the redundant serial port are common to all I/O board types, and are described in document DS901-000-02. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the six I/O ports

3.4.1 Counter Status Port

The board contains a separately addressable input port for reading the following status input signals:

- CT_EN1 – High state indicates that the counter function for input channels 1 and 2 is enabled.
- CT_EN2 – High state indicates that the counter function for input channels 3 and 4 is enabled.
- RATE0/ - High state indicates that rate mode is selected for input channels 1 and 2.
- RATE1/ - High state indicates that rate mode is selected for input channels 3 and 4.

When rate mode is selected for a particular pair of input channels, the microprocessor uses the CT_EN status input to determine when the sampling period is complete. If rate mode is disabled, the CT_EN status is not meaningful.

3.4.2 Port Addressing and Control

The hardware design of the HFC-AI4K card uses direct addressing to access the remaining hardware ports on the board as well as specific registers within the intelligent devices associated with those ports. When the microprocessor requires access to one of these ports, it sets programmable output P1.0 low and places the address for the desired port on address lines A12, A13, and A14. A demultiplexer decodes the address code to activate one of eight output chip select signals. These signals control access to the following I/O ports:

- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

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3.4.3 Input Channel Configuration

Each input channel consists of a voltage biasing network with a simple RC low-pass filter, an optocoupler, a second low-pass filtering network, a signal conditioning network, and two cascaded 12-bit counters. The 24 output signals from the two counters are routed to one of the programmable port controllers, and a slide switch controls selection of either the accumulate or the rate mode of operation.

3.4.3.1 Input Signal Conditioning

The input network monitors digital pulse (nominally 48-vdc) input signals. These signals are applied across RC low-pass filters (34 kHz shoulder frequency) to the input of transistor switches. When no signal is present, the low-pass filter shunts high frequency noise to ground, and the transistor switch remains cut off. When a positive input is present, the transistor becomes forward biased and passes an output through the base-emitter junction. A Zener diode in the base circuit limits the output voltage to the TTL range upstream from the optocoupler.

The final stage of signal conditioning consists of a second low-pass filter, a voltage comparator configured as a high speed switch, and a NAND gate. The low-pass filter is configured in parallel with the input of the voltage comparator to block any residual signal noise that could produce invalid pulse inputs to the counters. However, because the shoulder frequency of this filter is relatively low (63 Hz to 63 kHz), it also distorts the input

waveform. In order to produce a signal having well defined leading and trailing edges, the output from the low-pass filter is connected to the non inverting input of the voltage comparator. The biasing network connected to the inverting input comparator controls the voltage level at which the device switches its output signal. This network is configured to switch from OFF to ON when the input signal increases above 3.33 volts, and it switches from ON to OFF when the signal decreases below 1.67 volts. The resulting output is connected to a NAND gate and controls the clock input to the first of the two 12-bit counters. The NAND gate inverts the signal so that the trailing edge of each pulse increments the count.

3.4.3.2 Pulse Channel Operation

Selection of rate mode operation for each pair of pulse input channels is controlled by a slide switch. When the slide switch for channels 1 and 2 is in the rate position, switch contacts produce the following control circuits:

- The CT_EN1 signal is NANDed with the input pulse train for channel 1 and channel 2. When the CT_EN1 signal is low, the NAND gate blocks the pulse input, and the counters stop incrementing.

- The CLR0/ signal is routed to the reset port of all four 12-bit counters for these two input channels.

- A high RATE0/ signal is routed to the counter status input port.

When the RATE0/ signal is high, the microprocessor selects tuning parameters for the rate mode from memory. The operator must enter these tuning parameters manually from the rotary switch and the three pushbutton switches during hardware configuration of the card. The tuning parameters control selection between 8-bit and 12-bit resolution, a preset count value, and the maximum pulse rate. The microprocessor controls rate mode operation by configuring the programmable counter for a sampling interval determined by the tuning parameters, and then it clears the 12-bit counters. Once the counters have been cleared, the microprocessor activates the SET1 output. This signal sets a latch that activates the CNT_EN1 output signal. While this signal is high, the interval counter is enabled, and the 12-bit counters increment with each pulse received from the field. When the sampling interval expires, the interval counter produces an output pulse that clears the latch, forcing the CNT_EN1 signal low. The low state of the CNT_EN1 signal blocks further input to the 12-bit counters and notifies the microprocessor that the sampling period is complete. The microprocessor then reads the accumulated count from the port controllers for channels 1 and 2.

When the slide switch for channels 1 and 2 is in the accumulate position, the RATE0/ signal assumes a low level, and the reset input to the 12-bit counters is disabled. While accumulate mode is enabled, all pulses received from the field pass to the clock input port of the first 12-bit counter. When this counter reaches full count, the high-to-low transition of the MSB increments the second 12-bit counter. While accumulate mode is enabled, the counters

continue incrementing, and the microprocessor reads the total 24-bit accumulated count at periodic intervals.

3.5 CONTROLS, JUMPERS, AND INDICATORS

The firmware determines the overall operating characteristics of the hardware on the HFC-AI4K board. The HFC-AI4K board includes the set of four LEDs and a RESET pushbutton common to all I/O board types (DS901-000-02). In addition, the board includes jumpers, switches, and onboard indicators. These devices and the functions that they control are as follows:

3.5.1 Switches

The HFC-AI4K pulse input board includes a set of switches that enable configuration of operating parameters.

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

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XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

Inputs from a 17-position rotary switch (J5) control alphanumeric displays presented on U23 and programming functions of the board. The function defined for each switch position is defined in Table 1.

Table 1. Rotary Switch Functions

Position	Function
0	XXXXXXXXXXXXX
1	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
2	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
3	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
4	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
5	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
6	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
7	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
8	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
9	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
A	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
B	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
C	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
D	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
E	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
F	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

3.5.2 Jumpers

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

The channel input interfaces have four RC low-pass filters whose shoulder frequency is determined by a jumper strap. The jumper position typically installed at the factory selects a filter frequency of 1590 Hz. This filter frequency can be changed in the field as necessary to provide greater attenuation of signal noise. The input channels one through four jumper functions are defined in Table 2.

Table 2. **Jumper Configuration**

Input Channel 1
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: • XXXXXXXXXX • XXXXXXXXXX • XXXXXXXXXX • XXXXXXXXXX
Input Channel 2
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: • XXXXXXXXXX • XXXXXXXXXX • XXXXXXXXXX • XXXXXXXXXX
Input Channel 3
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: • XXXXXXXXXX • XXXXXXXXXX • XXXXXXXXXX • XXXXXXXXXX
Input Channel 4
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: • XXXXXXXXXX • XXXXXXXXXX • XXXXXXXXXX • XXXXXXXXXX

3.5.3 Onboard Status Indicators

The HFC-AI4K provides an eight-character alphanumeric display (U23) that indicates current operating status of the board. During board configuration, the display operates in conjunction with switches S1 through S3 and J5 to enter and save operating parameters. During normal operation, the display operates with the programmable switch (J5) to provide a readout of current values for operating parameters.

3.6 CONFIGURATION PROCEDURE

3.6.1 Hardware Setup Requirements

Before a new HFC-AI4K card can be placed into a system, onboard jumpers and switches must be set to match the specific operating environment that will be required.

1. Each input interface can be configured for isolated or common mode operation. Set each position of DIP switch to select either common mode (switch closed) or isolated mode (switch open) for the corresponding input channel.

2. The input interfaces have four RC low-pass filters whose shoulder frequency is determined by jumper straps (Table 2). The jumper position typically installed at the factory selects a filter frequency of 62.8 kHz. This filter frequency can be changed in the field as necessary to provide greater attenuation of signal noise.

3. Position switches S4 and S5 to select either rate or accumulate mode for the input channels.

4. Insert the board into the selected I/O board slot and power up the chassis.

3.6.1.1 Point Type Configuration

The pulse board reports its data to the controller either as a 12-bit or a 24-bit image. In order to allocate adequate memory in the controller for the input data, the user must configure a pulse input card as an AI8 board type in the I/O configuration table. However, the specific channel and AI point assignments depend on the operating mode selected for each input channel indicated in Table 3.

Table 3. Input Channel Assignments

Input Channel	Rate Mode	Accumulate Mode
1	XXXXXXX	XXXXXXX
2	XXXXXXX	XXXXXXX
3	XXXXXXX	XXXXXXX
4	XXXXXXX	XXXXXXX

3.6.1.2 Input Channel Tuning Parameters

The operator must enter tuning parameters directly into the pulse board using rotary switch (J5) and pushbutton switches (S1 through S3) mounted on the edge of the board. The rotary switch permits the user to read the current values of the data in memory and to revise the tuning parameters for each channel. The following steps outline the process for updating the values of the tuning parameters in memory.

1. Rotary switch positions 9 through C enable the user to update a preset parameter for each channel. This value determines the starting count for the corresponding channel when that channel is in the accumulate mode. The preset value is not used for the rate mode.

2. Rotary switch positions D and E enable the user to enter either a prescaler value (accumulate mode) or a maximum input pulse rate (rate mode).

   - For accumulate mode, the firmware accepts a single prescaler value for each pair of input channels (1 and 2 or 3 and 4). When the prescaler value is either 0 or 1, the counter increments with each input pulse. For any number greater than 1, the prescaler value determines the number of input pulses that must be received before the counter is incremented by 1. Actuating the SEL switch after setting the desired prescaler value saves the tuning parameter in memory.

   - For rate mode, the firmware accepts a separate parameter for counter size and for maximum pulse rate. The first time the SEL switch is incremented, the default counter size is displayed. Actuating the UP or DN switch causes this value to toggle between 8B (8-bit) and 12B (12-bit). Actuating the SEL switch again causes the firmware to display the default maximum pulse rate of 512 Hz. The user can increment this parameter in steps from 512 Hz up to 20,000 Hz for 12 bit by actuating the UP switch. Range for 8 bit is from 50 HZ to 10 KHZ. Actuating the SEL switch after setting both values saves those parameters to memory.

3.7 HARDWARE CONNECTIONS

The HFC-AI4K board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-AC36 and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 4.

Table 4. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1	XXXXXXX	P2-C1	XXXXXXX
P2-A3	XXXXXXX	P2-C3	XXXXXXX
P2-A4	XXXXXXX	P2-C4	XXXXXXX
P2-A6	XXXXXXX	P2-C6	XXXXXXX
P2-A2 P2-C2 P2-A5 P2-C5	XXXXXXX		

4.0 Software Functional Design Descriptions

The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AI4K board.

4.1 Board Specific Modules

4.1.1 I/O Scan Module

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
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4.1.2 Display Functions During Normal Operation

During normal operation, the rotary switch J5 can be used to display data currently stored in memory. Refer to position 0 to 8 in Table 1.

4.1.3 Tuning Process

During tuning mode operation, the software will go through different tuning steps depending on mode selected and the configuration parameters entered. Basically, the Tuning Process has the main functions listed in position 9 to F in Table 1. The Switches SEL, INC and DEC are used to make selections for configuration parameters.

4.1.4 Process Command Routine

For normal update requests, this routine has no function. For UCP diagnostics messages, it uses the common processing as described in DS002-000-02 to process UCP request received on the ICL.

4.2 Data Structure

4.2.1 Scan Data

The data field of the response message to the HFC-SBC06 controller contains AI images for eight channels as follows:

Table 5. AI Image

Byte	AI
0	XXXXX
1	XXXXX
2	XXXXX
3	XXXXX
4	XXXXX
5	XXXXX
6	XXXXX
7	XXXXX

The request message from the SBC06 controller doesn't have a data field.

4.2.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 6 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 6. Programmable Ports Used for the Card

Port	Description	Implementation
P1.0	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P1.1	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	
P1.3	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	
P1.7	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P2.1	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
P2.3	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX
Port 1 Control	XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXX	Initialize the register with $0B_H$ (00001011).

Table 7. On-Board I/O Ports

Addr	On-Board I/O Ports
000	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
001	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
010	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
011	Switch input port. Refer to 4.2.5.
100-111	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1000	Counter Status/Mode input. Refer to 4.2.3.

4.2.3 Counter Status/Mode Port

Two-position slide-switches S4 and S5 control the operation mode of the input channels. S4 selects either the Accumulate or the Rate mode of operation for input channels 1 and 2. S5 selects either the Accumulate or the Rate mode for input channels 3 and 4.

The mode port permits the microprocessor to read the counter status input signals. These inputs indicate which modes are selected for the input channels.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX

CT_EN1 – High state indicates that the counter function for input channels 1 and 2 is enabled.
CT_EN2 – High state indicates that the counter function for input channels 3 and 4 is enabled.
RATE0/ - High state indicates that rate mode is selected for input channels 1 and 2.
RATE1/ - High state indicates that rate mode is selected for input channels 3 and 4.

When rate mode is selected for a particular pair of input channels, the CT_EN status input is used to determine when the sampling period is complete. If rate mode is disabled, the CT_EN status is not meaningful.

4.2.4 Input Channels

The AI4K card reports the data for its four pulse input channels as eight AI points to the SBC06 controller. The specific channel and AI point assignments depend on the operating mode of the card.

Table 8. AI Point Assignments to Pulse Input Channels

Mode 1&2	AI 1	AI 2	AI 3	AI 4	**Mode 3&4**	AI 5	AI 6	AI 7	AI 8
RATE	XXX	XXX	XXX	XXX	**RATE**	XXX	XXX	XXX	XXX
ACCU	Channel 1		Channel 2		**ACCU**	Channel 3		Channel 4	

4.2.5 Switch Input Port

Besides the two switches S4 and S5 mentioned above, the card includes four additional switches:

- J5 - 16-position rotary switch controls alphanumeric displays and programming functions of the card. This switch permits the operator to read the current values of the data in memory during normal operation and to enter or revise the configuration parameters for each channel while in tuning mode.
- S1 – INC. Actuating this switch during tuning increments the value of the tuning parameter currently being displayed.
- S2 - DEC. Actuating this switch during tuning decrements the value of the tuning parameter currently being displayed.

- S3 – SEL. Actuating this switch during normal operating mode displays the value of the indicated parameter. Actuating the SEL switch during tuning mode steps through the tuning parameters in sequence and then saves the new parameter in memory.

The switch input port provides the switch status input signals.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
XXXXXXX				XXX	XXX	XXX	XXX

4.2.6 Alphanumeric Display Messages

The AI4K provides an eight-character alphanumeric display (U23) that indicates current operating status of the board. During board configuration, the display operates in conjunction with switches S1 through S3 and J5 to enter and save configuration parameters. During normal operation, the display operates with the J5 rotary switch to provide a read-out of current values for operating parameters.

The messages listed in the table below are designed for the display purpose of AI4K card.

Table 9. Display Messages

Message No	Display String
0	XXXXXXX
8	XXXXXXX
16	XXXXXXX
24	XXXXXXX
32	XXXXXXX
40	XXXXXXX
48	XXXXXXX
56	XXXXXXX
64	XXXXXXX
72	XXXXXXX
80	XXXXXXX
88	XXXXXXX
96	XXXXXXX
104	XXXXXXX
112	XXXXXXX
120	XXXXXXX
128	XXXXXXX
136	XXXXXXX
144	XXXXXXX
152	XXXXXXX
160	XXXXXXX
168	XXXXXXX
176	XXXXXXX
184	XXXXXXX
192	XXXXXXX

200	XXXXXXX
208	XXXXXXX
216	XXXXXXX
224	XXXXXXX
232	XXXXXXX
240	XXXXXXX
248	XXXXXXX

5.0 Module Implementation Descriptions

5.1 HARDWARE SCHEMATICS

The schematic for the HFC-AI4K card is in drawing 400448-01.

5.2 HARDWARE COMPONENTS – BILL OF MATERIALS

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXX

5.3 SOFTWARE SOURCE CODE LISTING

Besides the common software sources for software common modules listed in the HFC-6000 I/O Card Module Detailed Design Specification, the HFC-AI4K card software also includes the following programs:

- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
- XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

DOOSAN

HF Controls

INFORMATION ONLY

QUALITY PLANS

QUALITY PROCESS PROCEDURE

Procedure No. **QPP 2.1** Revision: **E**

Effective Date: **5/12/2009**

Prepared By: Gregory Morton

Reviewed By: Jonathan Taylor

Approved By: Charles McKinney

QUALITY PLANS

HFC Non-proprietary

Date	Revision	Author	Changes
5/11/09	E	G. Morton	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

TABLE OF CONTENTS

Section Page

1. 0 PURPOSE AND SCOPE 3

2. 0 ORGANIZATIONAL RESPONSIBILITIES 3

3. 0 REFERENCES 3

4. 0 GENERAL INFORMATION 3

5. 0 PROCEDURE 4

5.1 Project Initiation 4
5.2 Project Quality Plan (PQP) 9
5.3 Spares Quality Plans (SQP) 9
5.4 Project Management 9
5.5 Project and Spares Order Close-Out 9

6.0 QA RECORDS 9

7.0 ATTACHMENTS 9

7.1 Project Quality Plan 9
7.2 Spares Quality Plan 9
7.3 Quality Assurance Programs 9

1.0 PURPOSE AND SCOPE

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
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2.0 ORGANIZATIONAL RESPONSIBILITIES

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3.0 REFERENCES

3.1. QPP 2.2, "General Indoctrination and Training"

3.2. QPP 7.2, "Commercial Grade Item Evaluation"

3.3. QPP 10.1, "Receipt, In-Process and Final Inspections"

3.4. QPP 16.1, "Corrective Action Program"

3.5. QPP 17.1, "Quality Records"

3.6. QPP 19.1, "Contract Review"

4.0 GENERAL INFORMATION

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5.0 PROCEDURE

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6.0 QA RECORDS

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7.0 ATTACHMENTS

Attachments 7.1, 7.2 and 7.3 are forms that are related to this procedure. These forms shall carry the same revision as this procedure. To access them, click on the link provided.

7.1 Project Quality Plan
..\Forms\QPP 2.1, Attachment 7.1, Project Quality Plan, Rev E.doc

7.2 Spares Quality Plan
..\Forms\QPP 2.1, Attachment 7.2, Spares Quality Plan, Rev E.doc

7.3 Quality Assurance Programs
..\Forms\QPP 2.1, Attachment 7.3, Quality Assurance Programs, Rev E.doc

HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-SBC06-DPM06 Boards
Module Design Specification

System Controller

MS901-000-01

Rev E

Effective Date	03-27-09
Author/Title	Gregory Rochford
Reviewer/Title	Ivan Chow
Approval/Title	Terrence Gerardis

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HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-SBC06-DPM06 Boards
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MS901-000-01

Rev E

Effective Date	03-27-09
Author/Title	Gregory Rochford
Reviewer/Title	Ivan Chow
Approval/Title	Terrence Gerardis

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HFC Proprietary

HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-SBC06-DPM06 Boards
Module Design Specification

System Controller

MS901-000-01

Rev E

Effective Date 03-27-09

Author/Title Gregory Rochford

Reviewer/Title Ivan Chow

Approval/Title Terrence Gerardis

HFC Proprietary
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DOOSAN

HF Controls

INFORMATION ONLY

QUALIFICATION OF TEST PERSONNEL

QUALITY PROCESS PROCEDURE

Procedure No. **QPP 2.6** Revision: **D**

Effective Date: **5/12/2009**

Prepared By: Ivan Chow

Reviewed By: Charles McKinney

Approved By: Ed Herchenrader

QUALIFICATION OF TEST PERSONNEL

HFC Non-proprietary

Revision History

Date	Revision	Author	Changes
5/11/09	D	I. Chow	XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXX

TABLE OF CONTENTS

Section — Page

1. 0 PURPOSE AND SCOPE 3

2. 0 ORGANIZATIONAL RESPONSIBILITIES 3

3. 0 REFERENCES 3

4. 0 GENERAL INFORMATION 3

5. 0 PROCEDURE 3

5.1. Levels of Capability 3
5.2. Limited Certification 4
5.3. Education, Experience, and Training 4
5.4. Training 5
5.5. Evaluation and Certification of Personnel 6
5.6. Examination 7
5.7. Physical Capabilities 8
5.8. Certification 8
5.9. Performance 8

6. 0 QA RECORDS 9

7. 0 ATTACHMENTS 9

7.1. Minimum Levels of Capability for Test Personnel (General Functions) 9
7.2. Record of Evaluation 9
7.3. Instructions for Completing Record of Evaluation Form 9
7.4. Certification Record, Test Personnel 9

QUALIFICATION OF TEST PERSONNEL

HFC Non-proprietary

1.0 PURPOSE AND SCOPE

1.1. The purpose of this procedure is to define the requirements for training, qualification, and certification of personnel who perform tests on HFC products.

2.0 ORGANIZATIONAL RESPONSIBILITIES

2.1. XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

2.2 XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

3.0 REFERENCES

3.1. QPP 17.1, "Quality Records"

4.0 GENERAL INFORMATION

4.1. XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

5.0 PROCEDURE

5.1. Levels of Capability

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5.2. Limited Certification

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5.3. Education, Experience, and Training

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5.4. Training

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5.5. Evaluation and Certification of Personnel

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5.6. Examination

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5.7. Physical Capabilities

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5.8. Certification

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5.9. Performance

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6.0 QA RECORDS

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7.0 ATTACHMENTS

7.1. Minimum Levels of Capability for Test Personnel (General Functions)

7.2. Record of Evaluation

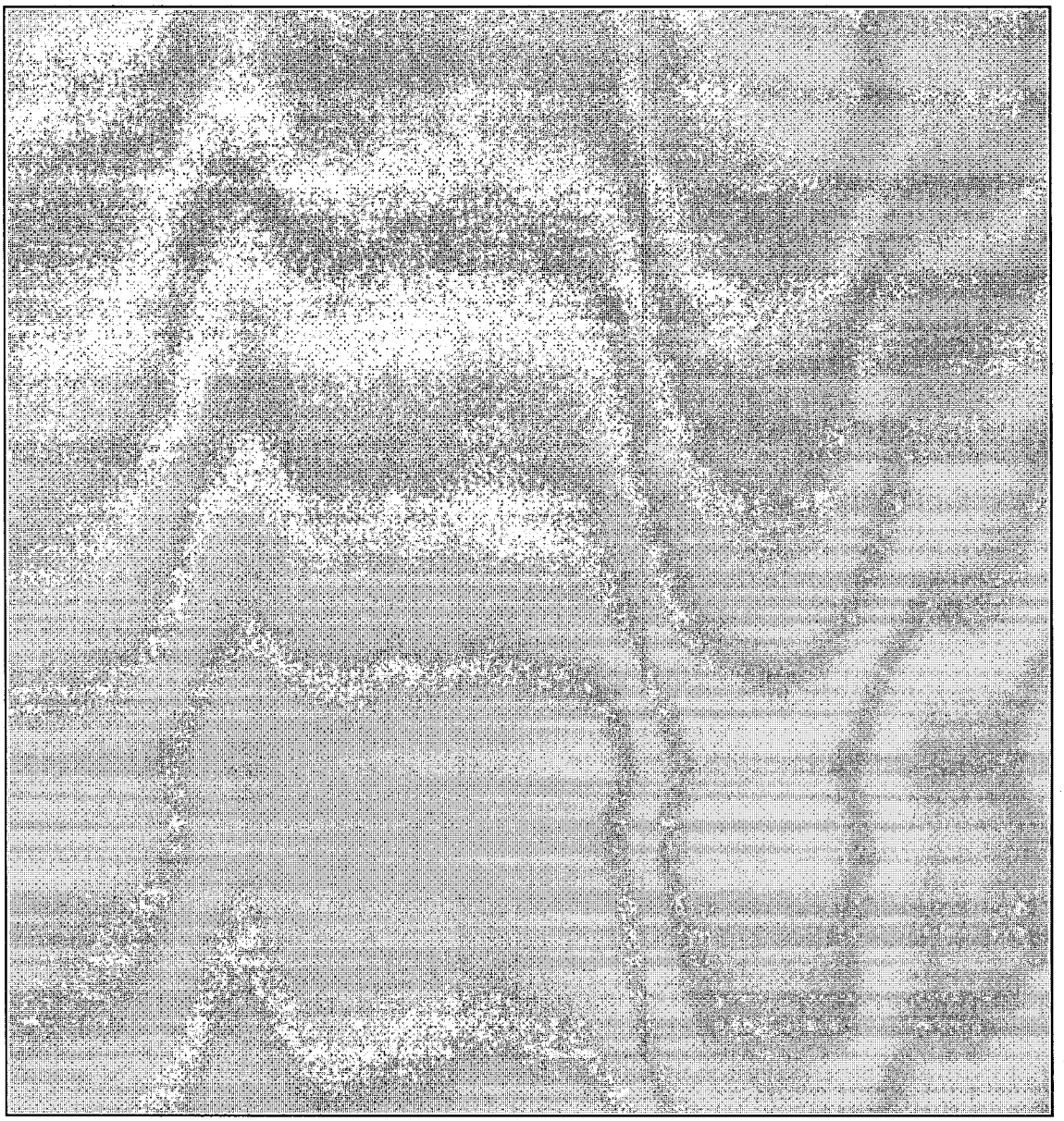
7.3. Instructions for Completing Record of Evaluation Form

7.4. Certification Record, Test Personnel

ATTACHMENT 7.1

Minimum Levels of Capability for Test Personnel

(General Functions)



QUALIFICATION OF TEST PERSONNEL

HFC Non-proprietary

ATTACHMENT 7.2

HF Controls

RECORD OF EVALUATION

Name: _____ **Discipline/Level:** _____

ATTACHMENT 7.3

Instructions for Completing Record of Evaluation Form

The following are instructions for completing the Record of Evaluation form used to document the evaluation of a candidate's education, experience, credentials of professional competence, and the results of capability testing, specialized training, and management assessment of factors not specified in the Record of Evaluation form.

SECTION I

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SECTION II

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SECTION III

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ATTACHMENT 7.3

Instructions for Completing Record of Evaluation Form (Con't)

SECTION IV

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SECTION V

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SECTION VI

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QUALIFICATION OF TEST PERSONNEL

HFC Non-proprietary

ATTACHMENT 7.4

HF Controls

Certification Record
Test Personnel

Name of Certified Individual:_____

Method/Discipline:_____

Level of Certification:_____

Certification Notes:

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HFC Non-proprietary

DOOSAN

HF Controls

INFORMATION ONLY

SOURCE CODE REVIEW

WORK INSTRUCTION-ENGINEERING DEPARTMENT

Work Instruction No: **WI-ENG-830** Revision: **B**

Effective Date: 3/10/2009

Prepared By: Ivan Chow

Reviewed By: Xu Huang

Approved By: Terrence A. Gerardis

Revision History

Date	Rev	Author	Changes
2/2/09	B	I. Chow	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

INFORMATION ONLY

Table Of Contents

Section — Page

1. 0 PURPOSE AND SCOPE 3

2. 0 ORGANIZATIONAL RESPONSIBILITIES 3

3. 0 ACRONYMS AND REFERENCES 3

4. 0 GENERAL INFORMATION 4

5. 0 PROCEDURE 4

6. 0 QA RECORDS 6

7. 0 ATTACHMENTS 6

1.0 PURPOSE AND SCOPE

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2.0 ORGANIZATIONAL RESPONSIBILITIES

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3.0 ACRONYMS AND REFERENCES

3.1 Acronyms

CGSI	Commercial Grade Software Item
HFC	HF Controls
QPP	Quality Process Procedures
WI	Work Instructions

3.2 References

IEC 880 -1986	"Software for computers in the safety systems of nuclear power stations"
IEEE 1028-1988	"Standard for Software Reviews and Audits"
QPP 3.1	"Design Control"
QPP 3.2	"Software Lifecycle"

4.0 GENERAL INFORMATION

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5.0 PROCEDURE

5.1 Obtaining the source code:

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5.2 The scope of a complete review should include the following:

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5.3 After completing of the review, for all HFC internal system program codes, the reviewer shall fill out the Software Source Code Record Form contained in Section 7.1.

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6.0 QA RECORDS

6.1 Completed Software Module Review Q/A Record.

7.0 ATTACHMENTS

7.1 Software Module Code Review Record.

ATTACHMENT 7.1

Software Module Code Review Record

REVIEWER:_____ **DATE:**_____

MANAGER OF S/W DEVELOPMENT: _____ **DATE:**_____
V&V PROJECT MANAGER: _____ **DATE:**_____

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