NSD-NRC-98-5516

Westinghouse Electric Corporation

Energy Systems

Nuclear Services Division

PO Box 355
Pittsburgh Pennsylvania 15230-0355

January 15, 1998

U.S. Nuclear Regulatory Commission
ATTN: Document Control Desk
Washington, DC 20555-0001

ATTENTION: NRC Operations Center

Subject: Notification of the Potential Existence of Defects Pursuant to 10CFR21

Westinghouse has identified a possible defect in a basic component that could potentially create a substantial safety hazard and therefore is deemed reportable under 10CFR21.21(a).

Background/Evaluation

Westinghouse was recently notified of Solid State Protection System (SSPS) circuits that were not fully tested during semi-automatic testing of the system. The circuits not fully tested are the Feedwater Isolation Memory Circuit and the P10 Source Range Block Memory Circuit. These circuits rely on paralleling each input to provide an output without utilizing the retentive memory. The original testing arrangement did not verify that both of the parallel inputs are operational because the signal (e.g., P-4 for feedwater isolation) that initiates the retentive memory was present at the logic gate input during testing. An open logic input isolation diode may prevent the desired output from the logic gate.

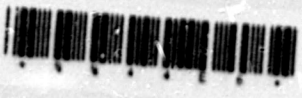
Safety Significance

For all plants that utilize the SSPS, this logic gate initiates feedwater isolation on a safety injection signal or a hi-hi steam generator water level signal. Safety injection initiates a reactor trip and, for most plants, the hi-hi steam generator water level initiates a turbine trip through separate logic which leads to a reactor trip. These functions provide a P-4 (reactor trip) signal so feedwater isolation is initiated with only a slight delay (milliseconds). For Sequoyah Units 1 & 2 and Watts Bar the turbine trip signal from hi-hi steam generator water level is not initiated separately and depends on the proper functioning of the logic gate with parallel inputs, as does feedwater isolation. The lack of feedwater isolation could lead to water carryover into the steam lines for these plants.

The same type of circuit is used for the P-10 Source Range Block function. This is a back-up function to P-6 and if both of these malfunctioned it would be detectable by observing that the source range was not blocked as power increased.

Plant Applicability

This 10CFR Part 21 notification applies to the feedwater isolation function at Sequoyah Units 1 & 2 and Watts Bar.



Recommendations/Corrective Actions

Westinghouse has determined that circuit modifications are not required to test both parallel inputs. By pressing the reset switch, the retentive memory signal (e.g., P-4 for feedwater isolation) is defeated and the ability to obtain an output from the logic gate confirms that both inputs are functioning. Westinghouse has communicated this information to all plants utilizing the SSPS via Technical Bulletin ESBU-TB-97-09, dated December 17, 1997 (attached). It is the understanding of Westinghouse that Sequoyah and Watts Bar have made procedural changes to implement the recommended testing.

If you have any questions regarding the notification, please call me at 412/374-5282.

Sincerely,

H. A. Sepp, Manager
Regulatory and Licensing Engineering

ENERGY
SYSTEMS
BUSINESS
UNIT

Westinghouse Technical Bulletin

An advisory notice of a recent technical development pertaining to the installation or operation of Westinghouse-supplied Nuclear Plant equipment. Recipients should evaluate the information and recommendation, and initiate action where appropriate.

P.O. BOX 355, Pittsburgh, PA 15230

Subject			Number
SSPS Testing For Feedwater Isolation			ESBU-TB-97-09
System(s)			Date
Solid State Protection System (SSPS)			December 17, 1997
Affected Plants			S.O.(s) 387
Westinghouse NSSS With Solid State Protection System			
References	Affects Safety Related Equipment	Yes ☒ No ☐	Sheet 1 of 8

SUMMARY

Westinghouse was notified of Solid State Protection System circuits that were not fully tested during Semi-automatic testing of the system. This condition was discovered by a utility during a generic review of Logic System testing. The circuits not fully tested are the Feedwater Isolation Memory Circuit and the P10 Source Range Block Memory Circuit. Westinghouse recommends a special Memory function test to verify proper operation of these circuits. No circuit modifications are required to perform the recommended tests.

BACKGROUND INFORMATION

Westinghouse was notified of a Solid State Protection System circuit that was not fully tested during Semi-automatic testing of the system. This condition was discovered during a generic review of logic system testing.

Additional Information, if Required, may be Obtained from the Originator. Telephone 412-374-3630 or (WIN) 284-3630.

Originator

Thomas D. Harbaugh, Sr. Engineer
Vintage I&C Engineering, SSPS System Engineer

Approval

H. A. Sepp, Manager
Regulatory and Licensing Engineering

Thomas N. Miller, Manager
Vintage I&C Engineering, NPD, I & C Engineering

The circuits not fully tested are the Feedwater Isolation Memory Circuit and the P10 Source Range Block Memory Circuit. Both circuits are tested as a memory function. However, both circuits also provide outputs from the memory circuit even if all of the memory inputs are not present at the circuit inputs. The Demand or SET inputs to the Memory function use parallel inputs to allow for circuit outputs without using the retentive memory.

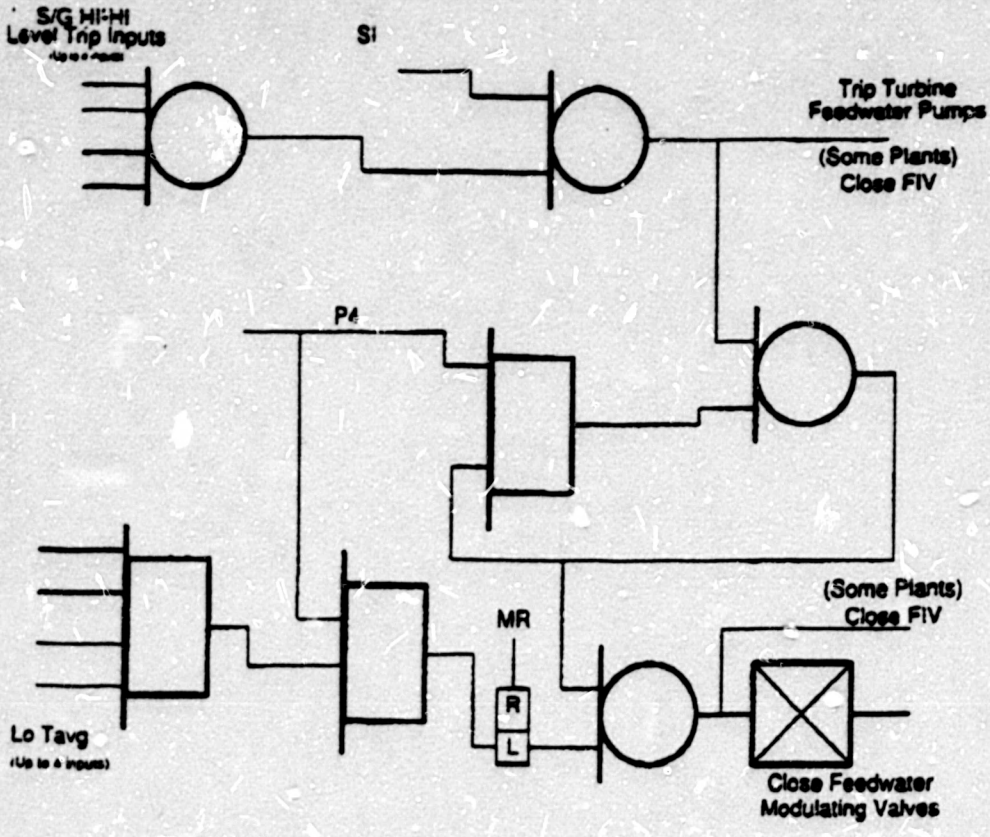
The current testing arrangement does not verify that the parallel inputs to the memory function are viable. Open input isolation diodes in the circuit could prevent having required outputs when desired. This Technical Bulletin identifies the two Memory circuits within the Solid State Protection System that use parallel inputs and are not fully tested with the Semi-automatic tester.

CIRCUIT DESCRIPTION

Feedwater Isolation Memory Circuits

In some plants the Close Feedwater Valves signal closes both the Feedwater Isolation valves and the Modulating Feedwater valves from the same isolation signal. In other applications, the Feedwater Isolation valves are operated by the Turbine trip/Feed Pump trip signal and the memory circuit only operates the modulating valves. Typical descriptions of the logic and testing problems are covered in this description. This discussion covers the typical arrangement for most plant sites. This description centers on the problem of not fully testing parallel inputs into a logic board used to provide a memory function within the SSPS. A review of the SSPS schematics shows many small differences between implementation of the feedwater isolation. It was determined that two main logic schemes were used to implement feedwater isolation and that specific implementation of these schemes allows for variances in the application. Each plant is encouraged to review their SSPS System schematic to determine which portions of the following descriptions apply to their application. Both of the logic schemes explained in this bulletin are taken from typical SSPS schematics.

The first logic scheme for closing the feedwater valves is shown in the following figure:



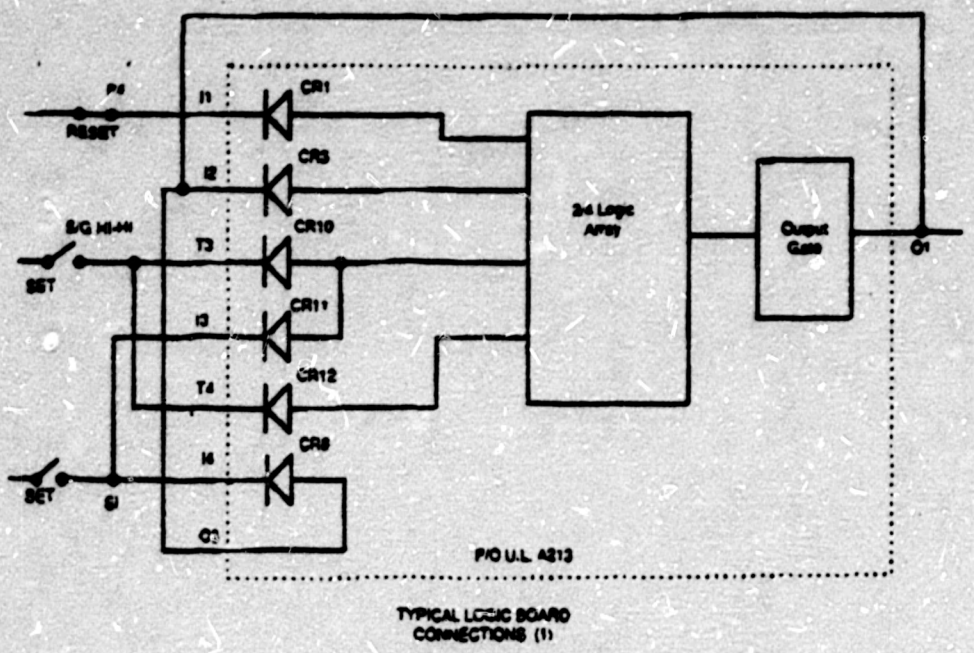
TYPICAL FEEDWATER
ISOLATION LOGIC (1)

The above logic diagram shows that the feedwater valves are to be closed on either a demand from an SI actuation or a Steam Generator HI-HI Water level. This close feedwater valve demand is latched in as a memory function when the P4 (RX Trip Breaker Open) signal is present.

The demand for Feedwater Valves close is a SI "OR" HI-HI Water Level "OR" retentive memory latch output based on P4 "AND" P4 Seal-in (Demand feedback). Feedwater valves are also closed by P4 "AND" Low Tavg. It is the first "OR" (SI/SG HI-HI) that the following circuit description details. The Low Tavg "AND" P4 close the feedwater valves if the reactor is tripped (P4) and the plant is at Low Tavg and a manual reset clears the feedwater demand.

Because the circuit must pass the close feedwater valve demand with or without the retentive memory function, the logic board must be connected in such a way as to pass the demand signal without having the P4 signal present at the logic input. A retentive memory circuit must perform a 2/4 logic function before the signal will pass through to the memory output. Usually this is provided by a demand and set signal and unlatched by a reset signal. A normal retentive circuit would have the SI or SG HI-HI provide the demand as one-of-two inputs to the memory logic. The second input would be provided by the P4 signal. The output would be tied back to an input to keep the memory latched until P4 was removed.

The following Figure shows the circuit arrangement to implement the logic shown in the above referenced logic figure and description. Because the current problem involves testing of the circuit, the figure shows test input configurations. Actual inputs are identified by signal input names and would be paralleled to the test inputs.



TYPICAL LOGIC BOARD CONNECTIONS (1)

NOTE:

The above circuit shows SI and SG HI-HI being "ORed" at the input to the memory circuit. Some applications use a separate logic circuit to "OR" these two signals.

The above figure shows that the O1 output is tied back to the I2 input. The switch inputs are for circuit testing and can be disregarded for this description. The SI demand is tied to both the I3 input and the I4 input. The I4 input connects back to the O3 output which connects to the I2 input. The Steam Generator HI-HI level connects to the T3 and to the T4 inputs. If an SI demand signal is present, the I4 input connects internally to O3 output which is connected externally to the I2 input. The O3 to I2 to O1 connection bypasses the memory function and causes the Feedwater Isolation demand to be present at the O1 output any time the I4 input is set. The same SI demand is tied to the I3 input and has no affect at the O1 output as long as the I4 input is present. The O1 output tied back to the I2 input provides no function at this time. If the SI demand is removed the feedwater isolation demand at the O1 output is removed as long as P4 is not present at the I1 input.

If a Steam Generator HI-HI demand is present at the T3 and T4 inputs, the 2/4 logic is met and the output at O1 demands the feedwater valves to close. The O1 output still has no effect on the circuit. If the S/G HI-HI demand is removed at the input, the 2/4 logic would not be met to maintain the output at O1. If the S/G HI-HI demand is present at the input without P4 present, the O1 output will change to demand feedwater isolation as long as the demand signals are present at the T3/T4 inputs. Only if P4 input becomes present while either input (SI or SG HI-HI) is being demanded will the retentive memory (seal-in) function.

The circuit is tested by the Memory function test on the Semi-automatic Test Panel. Test switch S506 uses two of its positions for this circuit operation. These are shown on the above figure as the SET and RESET inputs to the logic circuit. The RESET portion of the test is tied at the P4/I1 input line for both memory tests. This maintains a logic set (low) condition to the memory circuit as if P4 were present. Pressing the RESET switch opens the contact and causes the memory circuit to unlatch. The first of the two memory tests input the SET input as if it were a Steam Generator HI-HI input. Pressing the SET switch inputs a S/G HI-HI demand (low) at the T3 and T4 inputs causing the 2/4 logic to be met and setting the O1 output (LOW). This ties back to the I2 input and in combination with the P4 (RESET) at

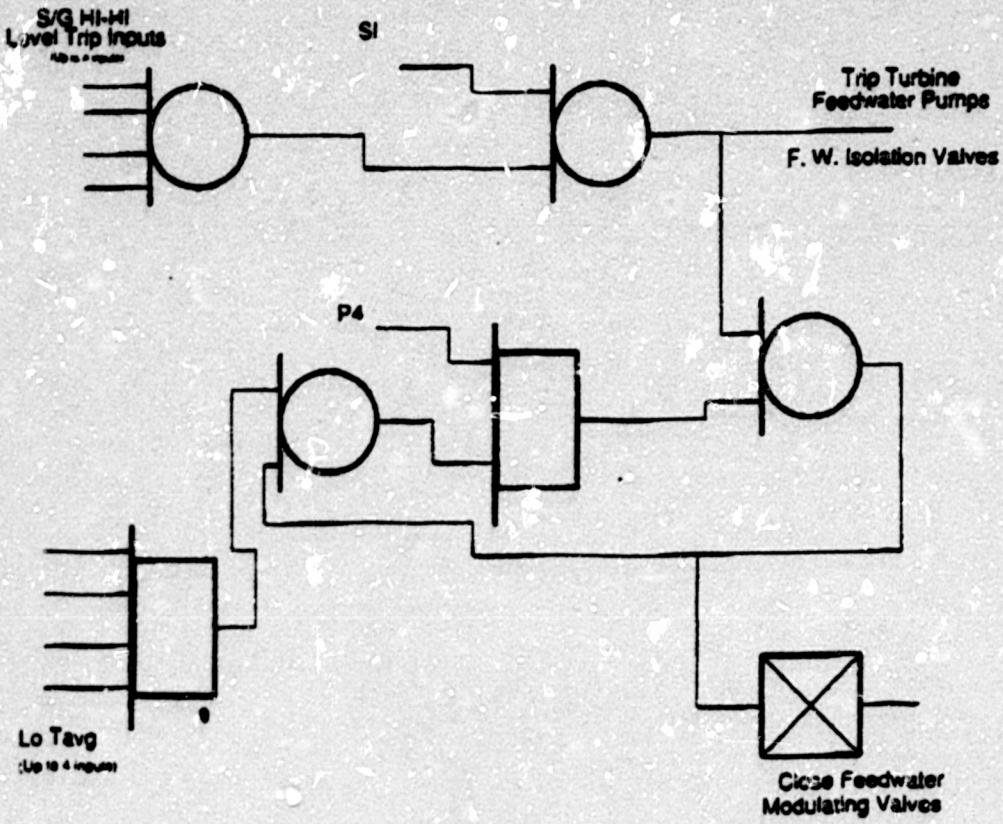
I1 maintains the 2/4 logic when the SET switch is released. Although not shown, the Memory Test lamp is tied to the O1 output.

The second memory test inputs the SI demand (low) at the I4 and I3 inputs. This memory output makes up as soon as the I4 input is set and latches the output via the O1/O3 to I2 input and the P4 (RESET). The I3 input is bypassed in this arrangement and has no affect on the circuit operation. As long as the I4 input is functional, the O3/O1 connection actuates the feedwater valve closed demand. If P4 occurs during this I4 demand, the I2 (I4/O3) input and the I1 (P4) input meet the 2/4 logic to latch the memory.

Logic circuits that provide the inputs to this memory circuit are tested for their operation by the semi-automatic tester. The Safeguards Driver circuit that is tied at the O1 output is tested by the Semi-automatic tester. The Memory function provided by this circuit is tested by the SET and RESET functions of the Semi-automatic tester. The function of the SI or S/G HI-HI demand causing the Feedwater valves to close without P4 is not fully tested. The following describes this test circuit operation.

When the memory circuit is tested, the P4 demand is present until the RESET switch is pressed. This always provides half of the 2/4 logic for the memory function. Any input at T4 or T3 will meet the second half of the 2/4 logic for memory operation. For example, if CR10 is open, the P4 (RESET) input at I1 is present. The S/G HI-HI is input by pressing the SET Switch. This input passes to both the T3 and T4 inputs. CR10 is part of the isolation for the T3 input. The T3 input would be blocked by the open CR10. However, the T4 input will pass through CR12 and fulfill the 2/4 logic for the memory function to operate. The same is true if CR12 is open and diode CR10 is operational. Because of the I4, O3, I2, and O1 arrangement, the SI input is not affected by this test arrangement. The I3 inputs acts like a parallel input that has no affect on circuit operation. Only the circuit for the I4 input requires extra testing. If CR6 (I4) input were open, the SET input would be tied to only the I3 input. The combination of the RESET (P4 at I1) and the SET input at I3 will allow the memory circuit to pass its memory function test. If only a SI signal were present at the I3 input, the circuit would not operate until P4 became present.

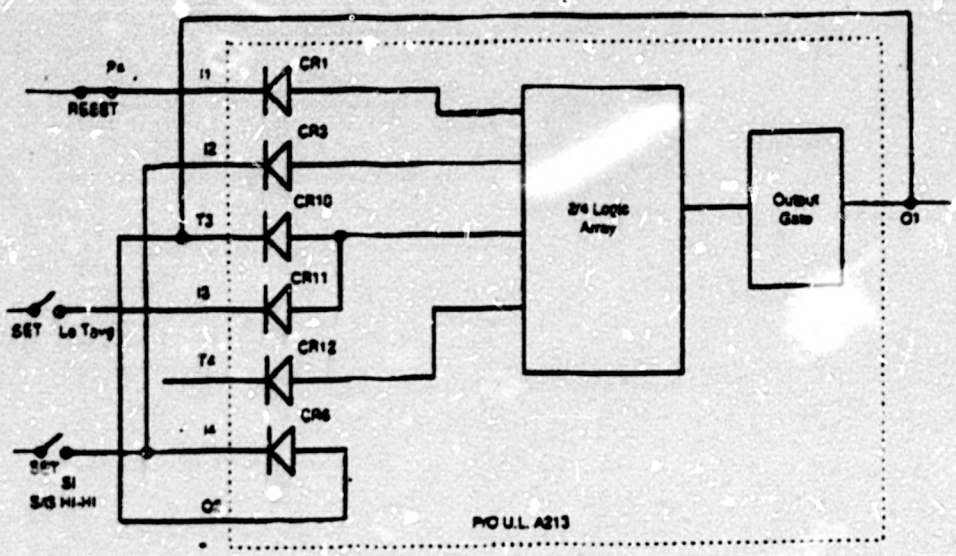
The following figure shows the logic for the second logic arrangement used to close the Feedwater valves:



TYPICAL FEEDWATER
ISOLATION LOGIC (2)

The above logic is similar to the first logic description. The main difference in this logic arrangement is the implementation of the P4 and Low Tavg. Low Tavg "OR" Feedback from the with P4 seal-in can latch the memory function. The Low Tavg "AND" P4 will close the feedwater valves. This is similar to the first logic scheme. If the reactor is tripped (P4) and the plant is at Low Tavg, the feedwater valves will close. The logic arrangement allows for feedback of the close Feedwater valves demand (P4 seal-in) signal "OR" Low Tavg in coincidence with P4 to latch the memory function.

The following circuit description implements the logic diagram and its functional description just referenced. As before, because the current problem involves testing, the circuit shows the test input connections. Actual trip and ESF actuation inputs would be parallel to the test inputs and are identified on the drawing by signal names.



TYPICAL LOGIC BOARD CONNECTIONS (2)

NOTE:

The above circuit shows an application where the SI and SG HI-HI signals were "ORed" on a separate logic circuit and input to the memory circuit on the same input line. Some applications "OR" these two inputs at the input to the memory circuit.

The parallel arrangement of I4 and I2 are similar to the first other logic arrangement discussed. For passing the SI/SG HI-HI signals immediately, only CR6 must be capable of conduction. The I4 input ties to the O3 output which ties to both the T3 input and O1 output. This arrangement bypasses the I2 input as long as CR6 is viable. The circuit requires an output as soon as an SI or SG HI-HI input is set. This is accomplished by I4 to O3 to T3 and I2. If CR6 is open, the circuit will not output on just SI/SG HI-HI demand because the I2 input does not meet the 2/4 logic input for the memory function. If CR3 is open, the circuit will provide an output from the I4 input alone. The I2 input serves no function as long as I4 input can be processed.

The testing scheme uses two Memory function tests to verify the circuit operation. The RESET is applied to the I1 input and simulates P4 being present at all times. The first memory test applies a SET to I4/I2 and simulates SI/SG HI-HI inputs. The second memory test applies a SET to I3 and simulates the Low Tavg inputs. This test arrangement does not test the CR6 and CR3 diodes.

P10 Source Range Block Memory Circuit

The other memory test that has the same type of application is found in the Source Range Block circuit. This arrangement is present at the P10 inputs on Logic card A408 in the Source Range Block circuits. In this case, P10 is applied to both the I1 and I2 inputs of the SR Block memory card. P6 is applied at T4 and the manual block function is applied at the I3 input. The O1 output is tied back to the T3 input to provide the retentive memory function.

One of the two memory tests for this circuit applies a SET at the P10 input. P10 provides an automatic SR Block if this has not been provided by the time the P10 power level is reached. It is intended to be a

back-up to P6 and keep the SR High Voltage deenergized. Two inputs are used by P10 to meet the 2/4 logic for memory circuit operation. The memory test does not separate P10 inputs and no other tests in SSPS verify this P10 operation. In this case, either CR1 or CR3 being open may not be detected by the memory function test

WESTINGHOUSE RECOMMENDATIONS.

Westinghouse has determined that no circuit modifications are required to test the above referenced conditions. Westinghouse does recommend that a special Memory function test be accomplished to verify the operation of the isolation diodes in these circuits.

Westinghouse recommends that each site review their specific application and implementation of the Feedwater Isolation circuit. Some applications show the SI and SG HI-HI inputs to the circuit are "ORed" at the input to the memory circuit. Other applications show the SI and SG HI-HI signals are "ORed" on a separate logic circuit and are input to the memory circuit on the same input lines. For the applications where the SI and SG HI-HI inputs are "ORed" at the memory circuit inputs, two special memory tests are required because both signal inputs use parallel inputs to the memory circuit (see the figure for Typical Logic Board Connections (1) in this bulletin). The applications that use a separate logic circuit to "OR" the SI and SG HI-HI signals require only one special memory test. The single input is the only parallel input (see figure Typical Logic Board Connections (2) in this bulletin).

For the SI and S/G HI-HI circuits, opening the P4 input while operating the SET inputs will allow only the SI and S/G HI-HI input to operate the O1 output. Opening P4 can be accomplished by pressing the RESET switch when performing this memory function test.

Special Memory Tests

The special memory test can be performed as part of the bi-monthly surveillance already being performed on the SSPS. Each plant must review the SSPS schematics and Technical Manual documentation to determine which position(s) of the Memory Test switch are used to test the A213 memory circuit. When aligned to perform the Memory function test for the A213 memory circuit, press the RESET Switch and hold it down. At the same time press the SET switch and verify that the memory test lamp lights. Release the SET switch and verify that the memory test lamp goes off. Release the RESET switch and complete the normal memory function test for that position.

By holding the RESET switch, the 2/4 logic for the memory circuit is only met by the two inputs from the SET switch. If either of the two input diodes are open, this test will not light the output memory test lamp. This test must be completed for each of the inputs that provide parallel inputs to the logic circuit.

For the Source Range Circuit, align the Memory function for the P10 input (e.g. S506-4). Press the RESET switch and hold it down. At the same time, press the SET switch and verify the Memory test lamp turns on. Release the SET switch and verify the Memory test lamp is off. Release the RESET switch and complete a normal memory function test. The memory test lamp will not light if either CR1 or CR3 are open on the A408 Logic Board.

For additional information, questions, or comments please contact the appropriate Westinghouse Commercial Product Manager (CPM) for each affected plant. The CPM will forward all information to the appropriate product line system engineer.

GENERAL INFORMATION or OTHER

EVENT NUMBER: 33542

LICENSEE: WESTINGHOUSE ELECTRIC COMPANY
CITY: PITTSBURGH REGION: 1
COUNTY: STATE: PA
LICENSE#: AGREEMENT: N
DOCKET:

NOTIFICATION DATE: 01/15/98
NOTIFICATION TIME: 14:07 [ET]
EVENT DATE: 01/15/98
EVENT TIME: 00:00[EST]
LAST UPDATE DATE: 01/15/98

NOTIFICATIONS

NRC NOTIFIED BY: JOHN GALEMBUSH
HQ OPS OFFICER: BOB STRANSKY

VERN HODGE NRR

EMERGENCY CLASS: NOT APPLICABLE
10 CFR SECTION:
CCCC 21.21 UNSPECIFIED PARAGRAPH

EVENT TEXT

10 CFR PART 21 REPORT REGARDING TESTING OF SOLID STATE PROTECTION SYSTEM LOGIC

WESTINGHOUSE WAS RECENTLY NOTIFIED OF SOLID STATE PROTECTION SYSTEM (SSPS) CIRCUITS THAT WERE NOT FULLY TESTED DURING SEMI-AUTOMATIC TESTING OF THE SYSTEM. THE CIRCUITS NOT FULLY TESTED ARE THE FEEDWATER ISOLATION MEMORY CIRCUIT AND THE P-10 SOURCE RANGE BLOCK MEMORY CIRCUIT. THESE CIRCUITS RELY ON PARALLELING EACH INPUT TO PROVIDE AN OUTPUT WITHOUT UTILIZING THE RETENTIVE MEMORY. THE ORIGINAL TESTING ARRANGEMENT DID NOT VERIFY THAT BOTH OF THE PARALLEL INPUTS ARE OPERATIONAL BECAUSE THE SIGNAL (E.G., P-4 FOR FEEDWATER ISOLATION) THAT INITIATES THE RETENTIVE MEMORY WAS PRESENT AT THE LOGIC GATE INPUT DURING TESTING. AN OPEN LOGIC INPUT ISOLATION DIODE MAY PREVENT THE DESIRED OUTPUT FROM THE LOGIC GATE.

FOR ALL PLANTS THAT UTILIZE THE SSPS, THIS LOGIC GATE INITIATES FEEDWATER ISOLATION ON A SAFETY INJECTION SIGNAL OR A HI-HI STEAM GENERATOR WATER LEVEL SIGNAL. SAFETY INJECTION INITIATES A REACTOR TRIP AND, FOR MOST PLANTS, THE HI-HI STEAM GENERATOR WATER LEVEL INITIATES A TURBINE TRIP THROUGH SEPARATE LOGIC WHICH LEADS TO A REACTOR TRIP. THESE FUNCTIONS PROVIDE A P-4 (REACTOR TRIP) SIGNAL SO FEEDWATER ISOLATION IS INITIATED WITH ONLY A SLIGHT DELAY (MILLISECONDS). FOR SEQUOYAH UNITS 1 AND 2 AND WATTS BAR THE TURBINE TRIP SIGNAL FROM HI-HI STEAM GENERATOR WATER LEVEL IS NOT INITIATED SEPARATELY AND DEPENDS ON THE PROPER FUNCTIONING OF THE LOGIC GATE WITH PARALLEL INPUTS, AS DOES FEEDWATER ISOLATION. THE LACK OF FEEDWATER ISOLATION COULD LEAD TO WATER CARRYOVER INTO THE STEAM LINES FOR THESE PLANTS.

THE SAME TYPE OF CIRCUIT IS USED FOR THE P-10 SOURCE RANGE BLOCK FUNCTION.

(Continued on next page)

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THIS IS A BACK-UP FUNCTION TO P-6 AND IF BOTH OF THESE MALFUNCTIONED IT WOULD BE DETECTABLE BY OBSERVING THAT THE SOURCE RANGE WAS NOT BLOCKED AS POWER INCREASED..

WESTINGHOUSE HAS DETERMINED THAT CIRCUIT MODIFICATIONS ARE NOT REQUIRED TO TEST BOTH PARALLEL INPUTS. BY PRESSING THE RESET SWITCH, THE RETENTIVE MEMORY SIGNAL (E.G., P-4 FOR FEEDWATER ISOLATION) IS DEFEATED AND THE ABILITY TO OBTAIN AN OUTPUT FROM THE LOGIC GATE CONFIRMS THAT BOTH INPUTS ARE FUNCTIONING. WESTINGHOUSE HAS COMMUNICATED THIS INFORMATION TO ALL PLANTS UTILIZING THE SSPS VIA TECHNICAL BULLETIN ESBU-TB-97-09, DATED DECEMBER 17, 1997.