WESTINGHOUSE

TOPICAL REPORT

EAGLE-21

MICROPROCESSOR-BASED

PROCESS PROTECTION SYSTEM

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PREPARED BY: L. E. Erin 1-14-87

L. E. Erin, Senior Engineer
Instrumentation and Control
Systems Licensing

APPROVED BY: D E Long for P. J. Morris 1/15/87

P. J. Morris, Manager
Instrumentation and Control
Systems Licensing

APPROVED BY: C. E. Corl 1/14/87

C. E. Corl, Manager
Process Control Application

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ABSTRACT

Process Instrumentation is comprised of those devices (and their interconnection into systems) which measure and process signals for temperature, pressure, fluid flow, and fluid levels. Process instrumentation specifically excludes nuclear and radiation measurements.

Process Instrumentation includes equipment which performs functions such as: process measurement, signal conditioning, dynamic compensation, calculations, setpoint comparison, alarm actuation, indication and recording, which are all necessary for day-to-day operation of the Nuclear Steam Supply System as well as for monitoring the plant and providing initiation of protective functions upon approach to unsafe plant conditions. The Westinghouse Eagle-21 microprocessor based process protection upgrade system is applicable for those instrument systems which are "safety-related" as defined by IEEE Std. 279-1971, "Criteria for Protection Systems for Nuclear Power Generating Stations". The Eagle-21 portion of process instrumentation includes all necessary devices with the exception of transmitters, indicators, and recorders.

The Westinghouse Eagle-21 microprocessor-based process protection system is a functional replacement for existing analog process protection equipment used to monitor process parameters at nuclear generating stations and initiate actuation of the reactor trip and engineering safeguards systems.

1.0 INTRODUCTION

The majority of nuclear power generation stations presently employ analog process protection equipment. This equipment, was designed in the 1960's and early 1970's. As illustrated in Figure 1-1, the analog protection system receives inputs from sensors, provides information to the operator, performs calculations on these values, and compares the results to allowable limits. If the limits are exceeded, a partial reactor trip is generated. External logic performs a voting algorithm on the partial trips from the four redundant protection sets, and conditionally generates a reactor trip. A similar path exists for the generation of engineered safeguard system actuations. These actuations mitigate the effects of an undesired event. The process protection system also provides isolated signals for use by non-safety systems such as the control system, the plant computer, and portions of the control board.

Westinghouse Process Protection Systems include three generations of analog electronics: Foxboro H-Line, Westinghouse 7100 Series, and Westinghouse 7300 Series Equipment.

The first generation of analog process protection equipment was Foxboro H-Line which is described in WCAP 7671 "Topical Report Process Instrumentation for Westinghouse Nuclear Steam Supply Systems." This equipment was manufactured for use during the 1965 - 1972 time frame. Twenty-four nuclear generating stations utilize this equipment.

The second generation of analog process protection equipment was the Westinghouse 7100 Series, also described in WCAP 7671. This equipment was manufactured for use during the 1970 - 1973 time frame. Thirteen nuclear generating stations utilize this equipment.

The third generation of analog process protection equipment was the Westinghouse 7300 Series, described in WCAP 7913 "Process Instrumentation for Westinghouse Nuclear Steam Supply Systems (4 Loop Plants Using WCID 7300

Series Process Instrumentation). This equipment was manufactured for use during the 1973 - 1983 time frame. Forty-four nuclear generating stations utilize this equipment.

As a result of technological advances, the earlier analog process protection systems are rapidly approaching the point of obsolescence. Additionally, utility personnel have identified the following difficulties with the analog systems:

A. Time consuming calibration and surveillance test procedures.
B. Extensive maintenance time for troubleshooting and repair.
C. Difficulty in maintaining equipment qualification.
D. Difficulty in maintaining adequate spare parts inventory.
E. Lack of expansion space to install hardware for functional upgrades and plant improvements.

The Westinghouse Eagle-21 Process Protection System is a modular microprocessor based upgrade system for replacing the existing analog process protection equipment. Features of the Eagle-21 equipment include the following:

A. Automatic surveillance testing to significantly reduce the time required to perform surveillance tests.

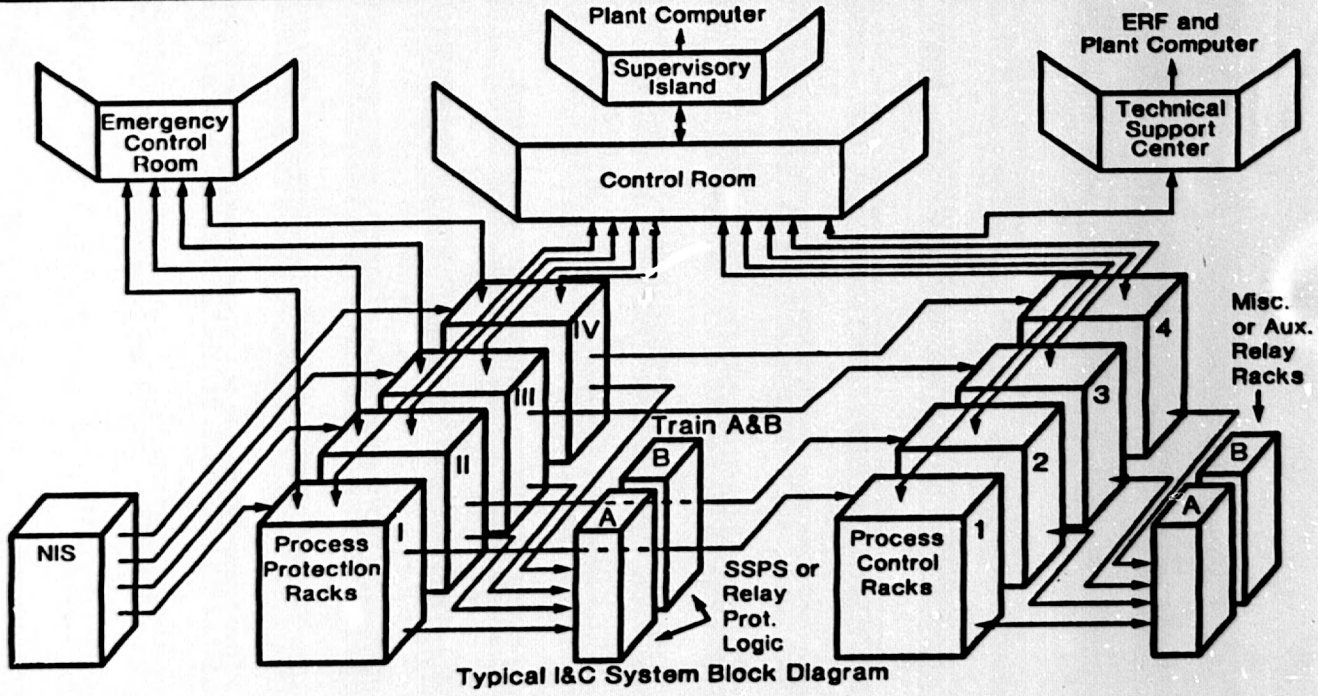
B. Self calibration to eliminate rack drift and time consuming calibration procedures.

C. Self diagnostics to reduce the time required for troubleshooting.

D. Significant expansion capability to easily accommodate functional upgrades and plant improvements.

E. Modular design to allow for a phased installation into existing process racks and use of existing field terminations.

EAGLE-21
IMPLEMENTATION



Typical I&C System Block Diagram

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FIGURE 1-1

2.0 DESIGN PHILOSOPHY AND FEATURES

The Eagle-21 Process Protection System, as shown in Figure 2-1, is a digital form, fit, and functional replacement for the existing analog equipment. All system inputs (from plant sensors) and system outputs (reactor trip logic, engineered safety features logic, indication and control) are preserved. Thus, the installation of Eagle-21 process equipment has no affect on the existing external interfaces.

2.1.1 Typical Analog Process Channel

A typical analog process protection instrument channel is shown in Figure 2-2. A field sensor is connected to cabinet mounted terminal blocks. The process electronics power the field sensor and perform signal conditioning, calculation, trip logic, and isolation operations on the input signal. Each element of the process is an individual electronic module or printed circuit board assembly. Typical functions performed by these modules are as follows: loop power supply, summation, lead/lag, multiplication, comparator, square root, amplification, signal conversion, and isolation.

2.1.2 Typical Eagle-21 Process Channel

A typical Eagle-21 Process Protection Instrument Channel is shown in Figure 2-3. A field sensor is connected to cabinet mounted terminal blocks. The process electronics power the sensor and perform signal conditioning, calculation, and isolation operations on the input signal. However, each element of the process is not an individual electronic module or printed circuit board assembly. A multiple channel Analog Input module is used to power the field sensor(s) and perform signal conditioning. All calculations for the process channel functions are performed by a centralized Loop Calculation Processor (LCP). Typical functions performed by the Loop Calculation Processor are as follows: summation, lead/lag, multiplication, comparator, averaging, and square root conversion. Trip logic is provided through multiple channel Partial Trip Output modules. Multiple channel isolated analog outputs are provided by Analog Output modules. In addition, all Eagle-21 process protection channels are configured to perform automatic surveillance testing via a centralized Test Sequence Processor (TSP).

Typical protection channels which may be processed with the Eagle-21 Process Protection System are as follows:

A. Average Temperature and Delta Temperature
B. Pressurizer Pressure
C. Pressurizer Water Level
D. Steam Flow and Feedwater Flow
E. Reactor Coolant Flow
F. Turbine Impulse Chamber Pressure
G. Steam Pressure
H. Containment Pressure
I. Reactor Coolant Wide Range Temperatures
J. Reactor Coolant Wide Range Pressure
K. Boric Acid Tank Level
L. Pressurizer Liquid and Vapor Temperatures
M. Steam Generator Narrow Range and Wide Range Water Level

2.2 INSTALLATION

The Eagle-21 Process Protection System is a modular electronics upgrade package for the existing analog plant process protection equipment. The Eagle-21 equipment has been designed to fit into existing process racks and to interface with other plant systems in a manner identical to the existing analog equipment. The design maintains the existing field terminals to avoid new cable pulls or splices within the rack. The components for each rack are built into subassemblies which can be easily installed into the existing racks. All internal rack cabling is pre-fabricated. The subassemblies are tested in a factory mock-up to verify proper fit and operation. Detailed installation procedures and drawings (formatted to match plant procedures and drawings) are provided with each system.

An example of Eagle-21 hardware being installed into an existing process rack is depicted in Figure 2-4.

2.3 System Design Features

2.3.1 Single Failure Criterion

The Eagle-21 Process Protection System is designed to provide three or four instrumentation channels and outputs to two trip logic trains for each protective function. These redundant channels and trains are electrically isolated and physically separated. Thus, any single failure within a channel or train will not prevent a required protective system action.

2.3.2 Instrument Power Source

Electrical power for the Eagle-21 Process Protection System instrumentation is obtained from four separate instrument busses that are equal to each other in reliability and quality of the power available. The arrangement of the four busses with respect to the ultimate power source is covered in detail in the FSAR for each plant. The use and availability of the four busses is important to the plant instrumentation in the following ways:

A. Each of the four protection sets is assigned to one of the instrument busses and no other.

B. Instrument channels are arranged so that loss of any one bus will not force a trip of the reactor. However, all reactor trip bistables and most of the safeguards bistables will trip in that protection set. (e.g. all 2 out of 3 reactor trip logic will revert immediately to a condition of 1 out of 2 logic.)

C. Loss of any one bus will not put the plant in an unprotected condition.

D. Coincident loss of any two busses will trip the reactor immediately as a result of the preferred failure mode of the bistables and initiate most safeguards action associated with those protection sets (e.g. two of the logic inputs for each associated 2 out of 3 or 2 out of 4 logic will immediately exist as trip signals).

2.3.3 Channel Integrity

The Eagle-21 Process Protection System has been designed to operate and maintain necessary functional capability under extremes of conditions relating to environment, energy supply, malfunctions and accidents. The environmental and energy supply extremes throughout which the system will perform are detailed in Section 4.0.

2.3.4 Channel Independence

Within the Eagle-21 Process Protection System, there are four separate and independent rack sets. Channels which provide signals for the same protective functions are each located in different rack sets ensuring that they will be independent and physically separated. Since all equipment within any rack is associated with a single Protection Channel Set (PCS), there is no requirement for separation of wiring and components within the rack.

2.3.5 Control and Protection System Interaction

The Eagle-21 Process Protection System functions completely independent from the control systems. Its' operation in protecting the plant from unsafe conditions is not affected by any fault or malfunction in the control systems.

The transmission of signals from the Eagle-21 Process Protection System to the control systems is through isolation devices that are classified as part of the protection system. No credible fault at the output of an isolation device can prevent the associated Eagle-21 Protection System channel from meeting the minimum performance requirements specified in the design bases. Fault testing of the isolation devices is described in more detail in Section 4.0 of this document.

The same type of electrical isolation is also used to separate from the Eagle-21 Protection System, those signals (such as RCS average temperature), which are required and used to control actual plant variables. For this use, however, consideration must be given to possible protection channel failures that can both prevent a particular trip signal from that channel and cause the

control system to drive the plant toward the unsafe condition for which the particular trip signal is needed. In each case where this is possible, four protection channels have been provided and 2 out of 4 logic is used. In the event that one channel fails, two out of three logic will remain and the plant remains fully protected even when degraded by a second random failure.

2.3.6 Automatic Surveillance Testing

The Eagle-21 Process Protection System performs automatic surveillance testing at the digital process protection racks via a portable Man Machine Interface (MMI) test cart. The MMI test cart is connected to the process rack by inserting a connector into the process rack test panel. Using the MMI, the "Surveillance Test" option is then selected. Following instructions entered through the MMI, the rack test processor automatically performs the following operations:

1. Selection of the individual process channel to be tested.

2. Calibration of the test reference signals and verification of the tester time base.

3. Placement of the individual channel bistables in either "Channel Trip" or "Bypass" (password protected) mode.

   A. Bypass Mode -- bypasses the individual channel bistable outputs to the logic circuitry to force the associated logic input relays to remain in the non-tripped state until the "bypass" is removed.

   B. Channel Trip Mode -- Interrupts the individual channel bistable outputs to the logic circuitry to de-energize the associated logic input relay(s).

4. Activation of the test injection signal.

5. Performance of Analog to Digital (A/D) converter test, and engineering unit values conversion test.

6. Performance of dynamic algorithm and bistable setpoint accuracy tests.

7. Performance of channel time response test.

8. Completion of test cycle and automatically remove "Channel Trips" and/or "Bypasses".

9. Verification of the calibration of the test reference signals.

10. Display of test results on the MMI screen.

Interruption of the bistable output to the logic circuitry for any reason (test, maintenance purposes, or removed from service) causes that portion of the logic to be actuated and accompanied by a channel trip alarm and channel status light in the control room. Each channel is fully testable via the portable MMI test cart.

Status lights on the process rack test panel indicate when the associated bistables have tripped. The value (in engineering units) that caused the bistable to trip is displayed on the MMI screen.

2.3.7 Calibration

The Eagle-21 Process Protection System provides for continuous on-line self-calibration of analog input signals. The Digital Filter Processor (DFP) provides high and low reference signals to a multiplexer circuit on each analog input channel. The DFP then compares the output of its' Analog to Digital (A/D) Converters to the high and low reference signals to determine if any errors have been introduced by analog signal processing and A/D conversion. If necessary, the DFP automatically adjusts the D/A gain and offset to eliminate any errors that have been introduced.

2.3.8 Channel Bypass

The Eagle-21 Process Protection equipment is designed to permit any one channel to be maintained, and when required, tested during power operation

without initiating a protective action at the systems level. During such operation, the process protection system continues to satisfy single failure criterion.

If an Eagle-21 protection channel has been bypassed for any purpose, a signal is provided to allow this condition to be continuously indicated in the control room.

The Eagle-21 design has provided for administrative controls and multiple levels of security for bypassing a protection channel. To place a protection channel in bypass, an individual must have access to the following:

A. Man-Machine Interface test cart.

B. Keyboard for the MMI test cart.

C. Key for the process rack door. A status light on the control board alerts the operator that the protection set has been entered. If a technician mistakenly opens the doors of two protection sets, the operator is alerted by an annunciator.

D. Key for the rack mounted test panel selector switch.

E. Password that is entered through the MMI keyboard.

Additionally, it is not possible to disconnect the MMI test cart from an Eagle-21 protection rack and leave a channel in "bypass" (see Section 3.2.5).

2.3.9 Access to Setpoint Adjustments

The Eagle-21 design has provided for administrative controls and multiple levels of security for access to setpoint and tuning constant adjustments. In order to adjust a setpoint or tuning constant in the Eagle-21 system, an individual must have access to the following:

A. Man-Machine Interface(MMI) test cart
B. Keyboard for the MMI test cart

C. Key for the process rack door (see Section 2.3.8, Item C)
D. Key for the rack mounted test panel selector switch
E. Password which must be entered through the MMI keyboard
F. Allowable range for the specific parameter to be updated, otherwise the attempted entry is rejected.

2.3.10 Diagnostics

The Eagle-21 Process Protection equipment provides specific diagnostic information to the user via numerous printed circuit card and test panel status LEDs, as well as information available through the portable Man-Machine-Interface (MMI). This design feature allows for easy recognition, location, replacement, and repair or adjustment of malfunctioning components or modules.

EAGLE-21
DESIGN PHILOSOPHY

- Form, fit and function replacement

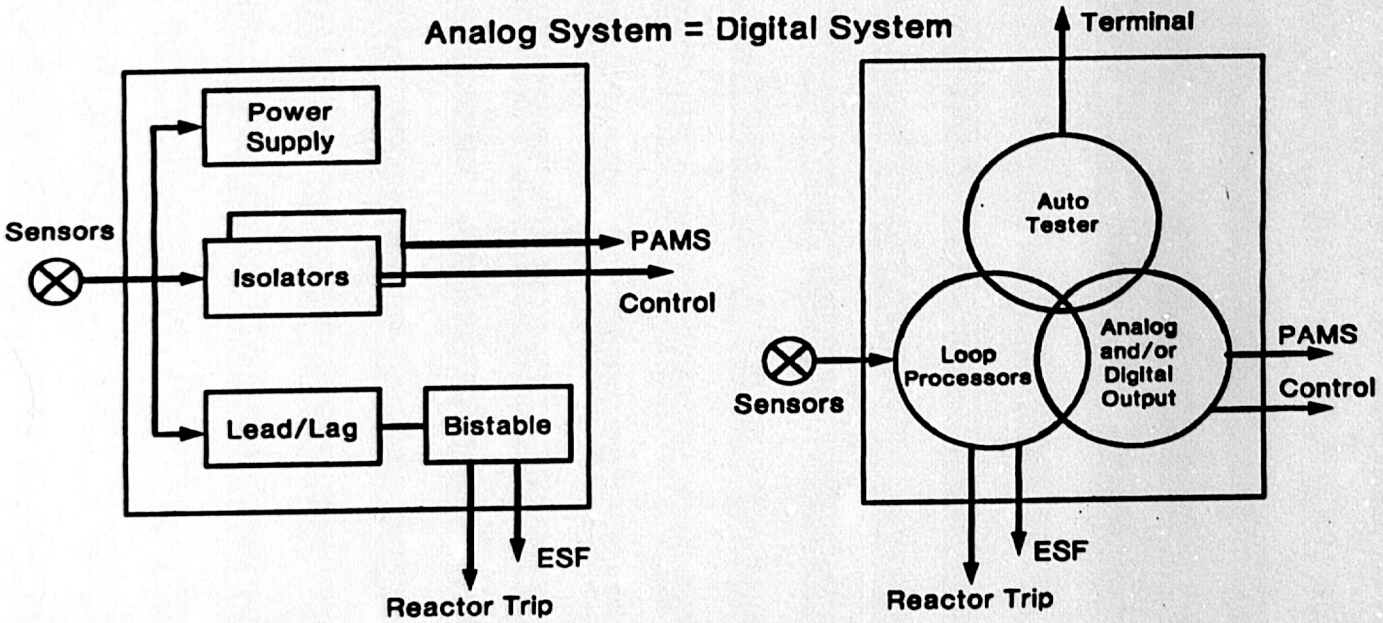

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FIGURE 2-1

Typical Analog Process Protection Channel

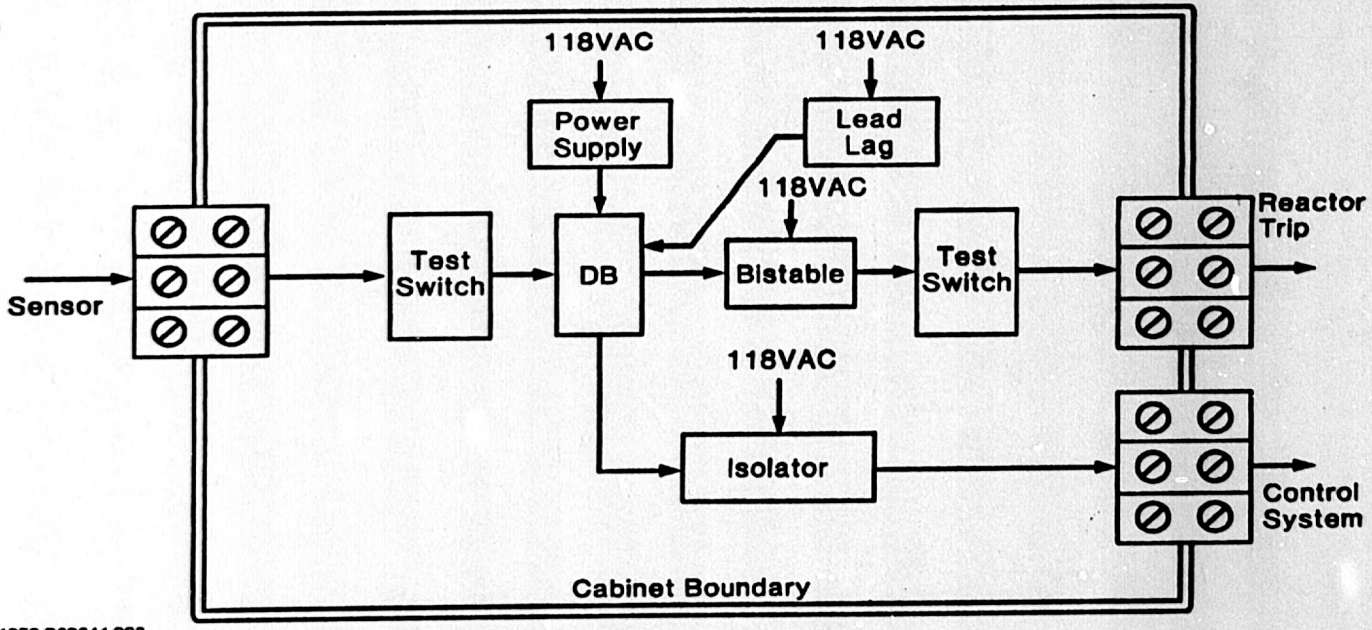

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FIGURE 2-2

EAGLE-21 IMPLEMENTATION

Typical Eagle-21 Process Protection Channel with automatic tester and PAMS

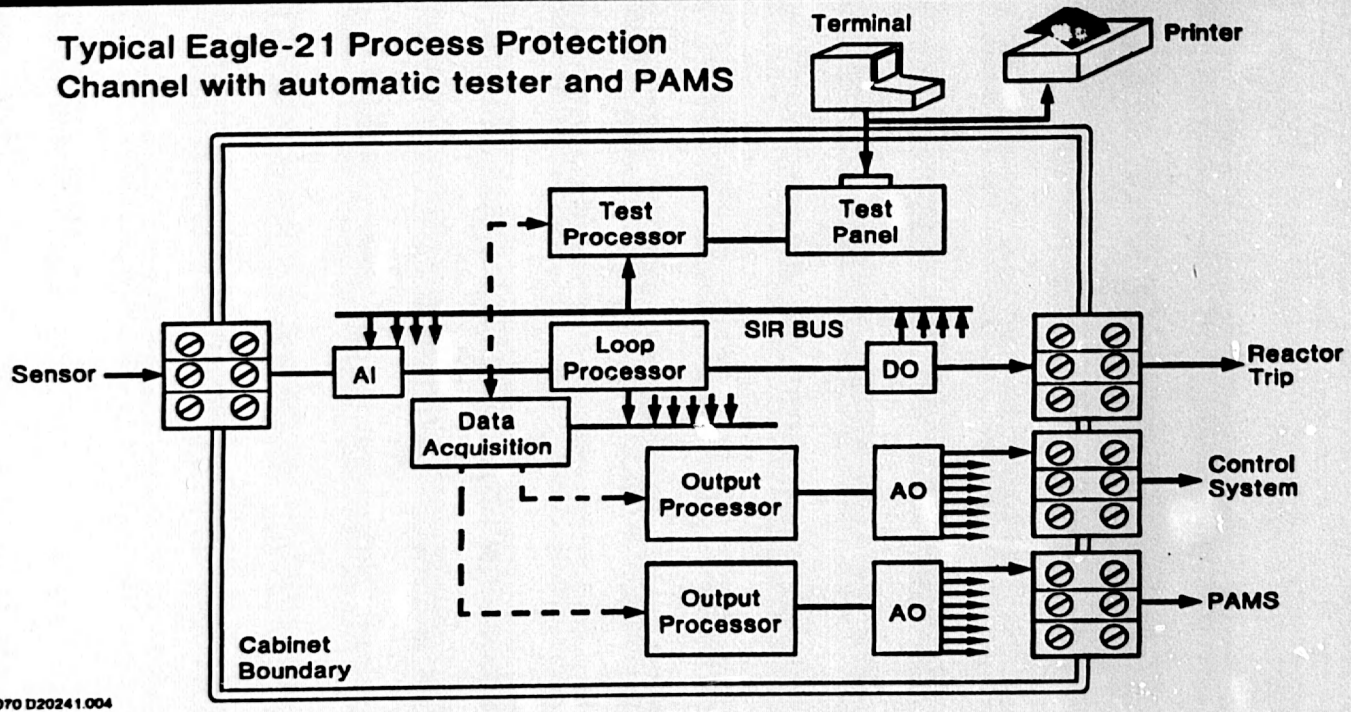

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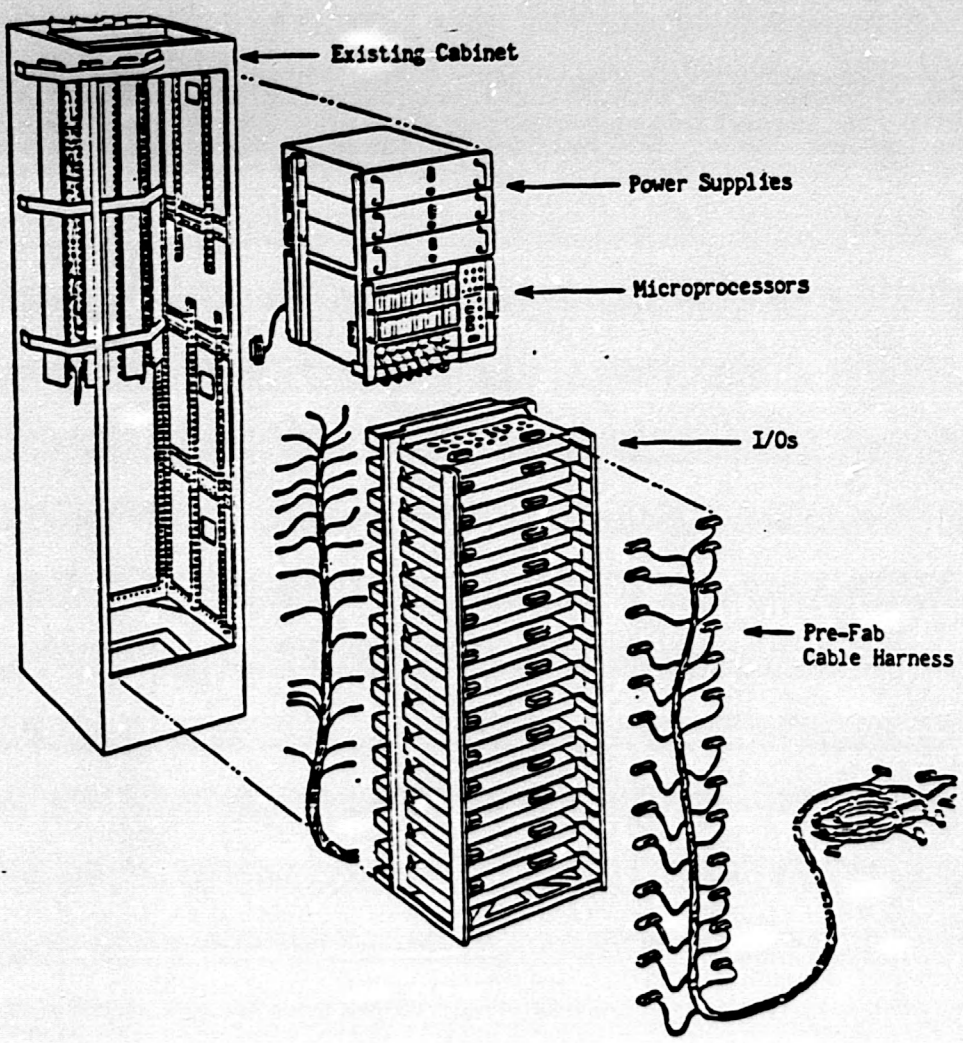
FIGURE 2-3



Existing Cabinet Installation of
Eagle 21 Equipment

FIGURE 2-4

3.0 TECHNICAL DESCRIPTION

3.1 Eagle-21 Architecture

The Eagle-21 Process Protection System replaces existing analog process protection equipment with multiple microprocessor based subsystems. Typically for each Eagle-21 protection system, three subsystems are used: a Loop Processor Subsystem, a Tester Subsystem, and an Input/Output Subsystem (see Figure 3-1). An overall view of the Eagle-21 architecture is shown on Figure 3-5.

3.1.1 Input/Output (I/O) Subsystem

The input portion of the I/O subsystem (see Figure 3-2) consists of customized Analog Input and Contact Input signal conditioning modules specially designed for use in Process Protection Systems of nuclear generating stations. These modules satisfy all of the unique signal conditioning, signal conversion, isolation, buffering, termination and testability requirements.

The signal conditioning modules are configurable to accept various process inputs including: 10-50 mA current loop (active or passive), 4-20 mA current loop (active or passive), 0-10 vdc, RTD's and field contacts. Both the Analog Input and Contact Input Modules provide signals to the Loop Processor Subsystem. These modules also interface with the Tester Subsystem for test and diagnostic purposes.

The output portion of the I/O subsystem consists Analog Output, Contact Output and Partial Trip Output modules. These modules receive data from the Loop Processor Subsystem and construct analog, contact, and trip logic output signals. Class 1E isolation is provided for all analog and contact output signals.

To minimize the total installation effort for the Eagle-21 equipment, the existing input/output interfaces are fully emulated. In plants with more advanced control or display equipment, Class 1E isolated data links may be extended directly to those systems, thereby eliminating the analog hardware at both ends.

3.1.2 Loop Processor Subsystem

The Loop Processor Subsystem is that portion of the Eagle-21 system which computes all of the algorithms and comparisons for the protective functions. A Loop Processor Subsystem (see Figure 3-3) consists of a Digital Filter Processor (DFP), Loop Calculation Processor (LCP), Communication Controller, Digital I/O Module, and a Digital to Analog (D/A) converter.

The Digital Filter Processor receives analog signals from Analog Input Modules and performs both Analog to Digital (A/D) conversions and anti-aliasing filtering operations on the input signals. The outputs of the Digital Filter Processor are then passed on the Loop Calculation Processor.

The Loop Calculation Processor performs calculations for protection channel functions, data comparison to setpoint values, and initiation of trip signals based on the data received from the Digital Filter Processor.

The Communication Controller collects information from the Loop Calculation Processor and transmits it to the Tester Subsystem.

The Digital I/O module is utilized to process contact inputs, contact outputs, and trip logic output signals.

The D/A converter module is utilized to convert digital values from the Loop Calculation Processor into analog values which are sent to analog output modules for further processing.

3.1.3 Tester Subsystem

The Tester Subsystem is the focal point of human interaction with the protection system. Together with the Man-Machine-Interface (MMI) Test Cart it provides the interface which allows test personnel to adjust setpoints and tuning constants, and to perform surveillance tests on the protection system. A Tester Subsystem (see Figure 3-4) consists of a Test Sequence Processor (TSP), Communication Controller, Digital to Analog (D/A) Converter Module, Digital I/O Module, and an Analog to Digital (A/D) Converter Module.

The Test Sequencer Processor (TSP) reads information from the Communication Controller, Digital I/O Module, A/D Converter, and the MMI Test Cart. This information allows the TSP to monitor the overall status of the Eagle-21 protection rack, perform self diagnostics, and initiate surveillance testing. The TSP provides information to the Communication Controller, Digital I/O Module, D/A Converter, and MMI Test Cart. This information provides for status indication and creation of the Signal Injection and Response (SIR) bus. This bus is distributed through the signal conditioning modules and allows the Tester Subsystem to control and test each module.

The Communication Controller receives information from the Loop Processor Subsystem Communication Controller. This information is then read by the TSP which allows it to monitor the status of the LCP. The Tester Subsystem Communication Controller also provides a serial link to the Test Panel, which allows for information display and printing when connected to the MMI Test Cart.

The D/A Converter Module receives digital information from the TSP and converts it into high resolution analog signals that are used for test injection via the Signal Injection and Response (SIR) bus.

The Digital I/O module receives information from the TSP and provides signals to a Contact Output Module that provides contacts for field devices.

The A/D converter module samples all analog output values and converts them into digital values, which are read by the TSP, and compared to the calculated values for analog outputs to ensure that the actual analog outputs are correct.

3.1.3.1 Man-Machine-Interface (MMI)

A portable test cart is connected to the Eagle-21 rack mounted test panel to provide the Man-Machine-Interface (MMI) to the Protection System. The MMI permits the user to perform the following functions:

A. Display all setpoints and tuning constants (on line).

B. Modify all setpoints and tuning constants (off line). Setpoints and tuning constants must be entered within a preset range or they will not be accepted by the MMI.

C. Display specified input values (on line).

D. Display specified intermediate values (on line).

E. Display specified output values (on line).

F. Display diagnostic information (on line).

G. Run surveillance tests on each channel as detailed in paragraph 2.3.5.

H. Provide a hardcopy printout of test results.

3.2 Eagle-21 Hardware Description

The Eagle-21 Process Protection System is comprised of a number of hardware modules and sub-assemblies which are described in this section.

3.2.1 Analog Input Module

The analog input module provides the interface between process transmitters, RTD's and the Eagle-21 computer hardware. Each analog input module provides the capability to interface with a maximum of four inputs. Analog input modules are capable of interfacing with both 4-20 mA and 10-50 mA current loops, 0 to 10 VDC signals, and four-wire RTD inputs.

The 4-20 mA and 10-50 mA current loops are arranged as two-wire current loops with the transmitter power supplied from the analog input module. Separate current loop power supplies and separate signal conditioning circuitry are provided for each transmitter.

The 0-10 vdc inputs are arranged as two-wire double-ended input signals. Separate signal conditioning circuitry is provided for each input signal.

The RTD inputs are arranged to accept a four-wire input configuration. The RTD excitation current source is supplied from the analog input module. Separate current sources and separate signal conditioning circuits are provided for each RTD input.

Included on the analog input module are provisions for automatic testing and automatic calibration. The automatic testing is accomplished via the Tester Subsystem. The analog input module communicates serially with the Test Sequence Processor (TSP) over the Signal Injection and Response (SIR) Bus. Test commands are transmitted to the input module which allows a selected analog input channel to switch from the field sensor to one of the multiple analog reference signals controlled by the TSP and carried by the SIR Bus. The value and characteristics (ramp rate etc.) of the analog reference signal is user-selected via the Man-Machine Interface (MMI).

On-line calibration is controlled continuously by the Loop Calculation Processor (LCP) to eliminate potential gain and offset drift in the analog hardware of the input module and the analog-to-digital (A/D) converter located on the Digital Filter Processor (DFP). During a calibration cycle, the DFP sends a command to the analog input module to switch from the field sensor to either the high or low on-board precision reference. The values that the DFP receives for the calibration references are used to calculate a correction factor that is applied to the input signal.

Referring to Figure 3-6, the analog input module provides the following features for each input signal:

A. High Input Impedance: The circuitry of the analog input module is designed to provide a high input impedance to minimize errors due to loading the current loop dropping resistors and RTD's.

B. Power Source: A 30 vdc current loop power source and a RTD excitation current source of 1 mA (nominal) are provided. Each power source output is provided with a RFI filter and a surge withstand network.

C. Passive Filters: Passive filter networks at the signal input to the board provide RFI filtering and the surge withstand network needed to meet surge withstand requirements. The surge withstand filter also provides for a high frequency cutoff to prevent signal aliasing.

D. Auto Test Signal Injection: A relay is provided on the input board to disconnect input signals and to provide for injection of test signals. This feature is under control of the Test Sequence Processor.

E. Calibration Reference Injection: A multiplexer and calibration reference source are included on the input board to allow input circuit calibration checks by injecting high and low reference signals into the input circuitry. This provides a two point check of the input circuit calibration. Calibration data acquisition is under control of the Loop Calculation Processor.

F. Signal Translation: A differential signal amplifier is used to translate the input signal to a standard level that is compatible with the D/A converter input. This amplifier and associated circuitry is designed to operate in a fully floating configuration.

G. Input Signal Monitoring: A buffered test connector is included on the analog input module as an interface point for sensor testing.

3.2.2 Contact Input Module

The contact input module provides the interface between field contact devices and the Eagle-21 computer hardware. Each contact input module is capable of processing either four complementary contact pairs, or eight independent contacts. The output signals from the contact input module are read directly by the Loop Calculation Processor through digital I/O ports.

Referring to Figure 3-7, the contact input module provides the following features for each contact input:

A. Contact Configuration: The contact input module, provides the capability to accept normally open and normally closed contact pairs through either a three or four-wire input configuration. The three wire configuration is preferred to simplify plant wiring and terminations. A complementary (normally open/normally closed contact pair) configuration provides the ability to detect input circuit failures. The module can also accept single contact inputs however, this configuration does not accommodate input circuit failure detection.

B. Surge Withstand: A surge withstand network is provided at the input of the board to meet surge withstand requirements.

C. Auto Test Signal Injection: A switching function is provided to allow the injection of contact input test signals. This feature is under control of the Test Sequence Processor. The complementary contacts are tested as a pair. This arrangement allows for confirmation of the test signal being disconnected after the test. This is accomplished by trying to inject test signal inputs to the board after the input is reconnected to the normal operating condition. If the output does not follow the test signal, then disconnection of the test signal is confirmed.

D. Power Supply: Isolated power supplies are provided for each contact input circuit to sense contact position and maintain independence between contacts. A 48 vdc (nominal) supply is used to provide good contact wetting. The power supplies are arranged to allow the input boards to be connected in parallel.

E. De-bounce: A contact de-bounce feature is provided as part of the module design to prevent switching transient contact bounce from being erroneously read by the Loop Calculation Processor.

3.2.3 Analog Output Module

The analog output module (Figure 3-8) provides an interface between the Eagle-21 computer hardware and field devices. Each analog output module is capable of providing up to eight channels of analog outputs.

The analog output module converts a 0 to 5 vdc signal from the Loop Calculation Processor into an electrically isolated 4 to 20 mA or 10 to 50 mA current transmitter or a 0 to 10 vdc voltage source. The analog output module features surge suppression and electrical isolation to prevent destructive transients from propagating from the field conductors back through the Eagle-21 hardware.

On-line calibration checks are continuously performed by the Tester Subsystem. An isolated feedback signal derived from the analog output module output is digitized and transmitted to the Test Sequence Processor where it is compared to the calculated output value. If a tolerance limit is exceeded, an error signal is reported.

Additional features of the analog output module are:

A. Status LED's for "Power On" and individual "Channel On" indication.

B. "Range Select" switches to choose the proper range of output loop resistance which will maximize the power transfer efficiency.

3.2.4 Contact Output Module

The contact output module (Figure 3-9) provides the interface between field devices operated by contact logic and the Eagle-21 computer hardware. Each contact output module is capable of providing up to eight complementary contact pairs for output purposes. The Loop Calculation and Test Sequence Processors control the relay status/contact logic through Digital I/O cards connected to the IEEE Std. 796 bus.

The contact output module provides the following features for each output:

A. Surge Withstand: A surge withstand network is provided for each output of the module to meet surge withstand requirements.

B. Isolation: Each output circuit provides electrical isolation. This maintains electrical independence and prevents damage due to transients conducted into the system through the contact output module.

C. Status LED's for "Power On" and individual relay "energization status" indication.

3.2.5 Partial Trip Output Module

The partial trip output module (Figure 3-10) provides the interface between the Eagle-21 computer hardware and the trip logic system. Each partial trip module is capable of providing up to four channels of logic outputs. The trip output module converts a signal from the Loop Calculation Processor into an On/Off voltage used to drive relays in the trip logic system. Additional features of the partial trip output module are:

A. Jumper selectable normally-energized or normally-deenergized logic outputs.

B. Capability to set a channel in either "channel trip" or "bypass" mode in conjunction with the MMI test cart.

C. Toggle switch for each output to provide the capability to manually generate a channel trip independent of the MMI test cart.

D. Status LED's to indicate the state of each output channel.

E. Deadman Timer for each channel to automatically remove a "bypass" condition which has been set if a signal is not received from the Tester Subsystem via the Man-Machine-Interface test cart. Thus, it is not possible to disconnect the MMI test cart from an Eagle-21 protection rack and leave a channel in "bypass."

F. Deadman Timer for each channel to automatically set a "channel trip" if a signal is not received from the Loop Processor Subsystem.

3.2.6 Microprocessor Card Chassis Modules

3.2.6.1 Intel iSBC 88/40A

The Intel iSBC 88/40A is a measurement and control computer with enhanced numeric processing capability. The iSBC 88/40A provides 16 differential input channels and is utilized as both an A/D Converter and a Digital Filter Processor (DFP).

In application, the iSBC 88/40A (DFP) performs the following operations:

A. Read analog inputs
B. Analog-to-digital conversion
C. Input calibration readings and adjustment
D. Onboard diagnostics
E. Digital filtering

The input data is placed into shared memory for access by the Loop Calculation Processor (LCP).

3.2.6.2 Intel iSBC 286/12

The Intel iSBC 286/12 is a 16-bit single board computer designed as a board-level solution for high-speed, real-time, multi-tasking, and multiprocessor system applications. Intel iSBC 286/12 boards serve as the Loop Calculation Processor (LCP), Test Sequence Processor (TSP), and Man-Machine-Interface (MMI) Processor.

When serving as the LCP, the iSBC 286/12 performs the following operations:

A. All calculations for process channel algorithms.
B. Data comparison to setpoint values.
C. Initiation of channel trip signals.

When functioning as the TSP, the iSBC 286/12 has an on-board serial communication link which together with high resolution digital to analog converters create the Signal Injection and Response (SIR) bus. The SIR bus is used for

monitoring and testing of all analog input, contact input, and partial trip output modules. The TSP also reads information from the LCP via a Communication Controller and determines the overall status of the Eagle-21 system.

When serving as a MMI Processor, the iSBC 286/12 performs the following functions:

A. Converts data to ASCII format for output to display.
B. Converts operator inputs from ASCII to real numbers.
C. Performs error and limit checking on all operator inputs.

3.2.6.3 Intel iSBC 88/45

The Intel iSBC 88/45 is an advanced data communications processor which has the capability to both transmit and receive information.

In application, an iSBC 88/45 operates as a "slave" communication controller for the Loop Processor Subsystem Multibus, the Tester Subsystem Multibus, and the MMI Test Cart Multibus.

The Loop Processor Subsystem uses an iSBC 88/45 to transmit data to the Tester Subsystem. The Tester Subsystem uses its iSBC 88/45 to receive data from the Loop Processor Subsystem and to both transmit data to, and receive data from the MMI Test Cart. Likewise, the MMI Test Cart uses its iSBC 88/45 to both transmit data to, and receive data from the Tester Subsystem.

3.2.6.4 Intel iSBC 519

The Intel iSBC 519 is a programmable Input/Output (I/O) expansion board. The iSBC 519 provides 72 programmable I/O lines.

In application, the iSBC 519 is utilized to process digital I/O signals for both the Loop Processor and Tester Subsystems. The Loop Calculation and Test Sequence Processors interface with their associated iSBC 519 and either read a signal which represents a digital input or write a value that the iSBC 519 converts to a digital output.

3.2.6.5 Data Translation DT-1742

The Data Translation DT-1742 is a high level (± .625 vdc to ± 10 vdc) analog-to-digital converter with programmable gain capability. Each DT-1742 module is capable of processing up to 16 differential input channels.

In application, the Data Translation DT-1742 is utilized to monitor analog output values from the Input/Output Subsystem. This data is then read by the Test Sequence Processor and compared to the value that was calculated by the Loop Calculation Processor to ensure that the analog outputs are correct.

3.2.6.6 Datel Intersil ST-716

The Datel Intersil ST-716 is a high resolution (16-bit) digital-to-analog (0 to 10 vdc) converter. Each ST-716 module is capable of providing up to eight channels of high resolution analog outputs.

In application, the Test Sequence Processor writes a value to the ST-716. The ST-716 converts this value into a high resolution analog signal that is sent to Analog Input Modules via the Signal Injection and Response (SIR) bus and utilized as a test injection signal for surveillance testing.

3.2.6.7 Burr-Brown MP8316-V

The Burr-Brown MP8316-V is a 12-bit resolution digital-to-analog (0 to 5 vdc) converter. Each MP8316-V module is capable of providing up to 16 channels of analog outputs.

In application, the Loop Calculation Processor writes a value to the MP8316-V. The MP8316-V converts this value into an analog signal which is sent to an Analog Output Module for further processing.

3.2.7 Miscellaneous Hardware

3.2.7.1 Microprocessor Card Chassis

The Eagle-21 microprocessor card chassis is an assembly which provides access to two independent IEEE Std. 796 Busses for up to a maximum of eight printed circuit boards per bus. One bus is for the Loop Processor Subsystem and the other bus is for the Tester Subsystem. It provides cooling to these boards as well as physical restraint and allowance for power cable attachment. The microprocessor card chassis is assembled from four major sub-assemblies: a chassis weldment, a backplane, a fan assembly, and a status panel.

3.2.7.2 DC Power Supply Chassis

The Eagle-21 standard power supply chassis is a modular assembly which is capable of providing dc power from a 118 VAC, 60 Hertz source which will operate over the range of 90 to 132 VAC and 47 to 440 Hertz.

Each Eagle-21 rack contains two power supply chassis. One chassis provides dc power to the Loop Processor Subsystem Multibus and the Input/Output Subsystem, the second chassis provides dc power to the Tester Subsystem and the Input/Output Subsystem. Each chassis houses two dc power supplies. One supply provides (+5, +12, and -12) vdc to the microprocessor card chassis and the second supply provides +15 vdc to the input/output cards.

3.2.7.3 Test Panel

Each Eagle-21 process protection rack contains a Test Panel Assembly. The test panel is divided into three sections: Status Indications, Test Points, and Man-Machine-Interface.

The Status Indication section of the Test Panel provides status indication ("channel trip" or "bypass") for all trip logic output channels. This section also provides status indication for self-diagnostics such as "cabinet overtemperature."

The Test Point section of the Test Panel provides test points where a dc voltage may be read for every analog input.

The Man-Machine-Interface section of the Test Panel provides a connector, test points, and a selector switch. The connector is used for hookup to the Man-Machine-Interface Test Cart. The test points are user selectable such that any data within the Eagle-21 rack can be made available at the test points. The selector switch has positions for Normal, Test, and Parameter Update.

A protection set rack door must be opened to access its Eagle-21 Test Panel. A status light on the control board alerts the operator that the protection set has been entered. If a technician mistakenly opens the doors of two protection sets, the operator is alerted by an annunciator.

3.2.7.4 Termination Frame

The Eagle-21 Termination Frames are modular assemblies which accommodate a single Input/Output printed circuit board. The Termination Frame serves to stiffen the Input/Output board against seismic input and provides terminals for power and signal connections. Each Eagle-21 process protection rack will contain sixteen termination frames, installed one above the other in a structure known as the termination framework.

3.2.7.5 Cabinet Cooling Assembly

Each Eagle-21 process protection rack is equipped with a 300 cubic feet per minute (cfm) squirrel cage blower assembly. This assembly will be located in the bottom of the rack and provide for a "chimney effect" by forcing air up through the rack and out of the top.

3.3 Software

3.3.1 Software Development

The Eagle-21 Process Protection System software has been designed to be modular in structure (See Figure 3-11). This dictates that all executable code be contained in a module or subroutine. The main program simply determines the sequence for execution of these modules. The main program contains a 'restart' section, a section that is executed only once on restart, and a looping section that is continually executing. Initialization routines are in the restart section and process function routines are in the looping section.

Overall software development follows a general format of four layers. The first and bottom layer contains the main program and support functions. The second layer is a library of general purpose modules. These modules are comparable to a single analog printed circuit board. They perform one function and can be used in many different applications. The third layer is a library of standard protection functions which are built primarily from general purpose modules. These functions are comparable to a standard set of analog cards which bring together simple circuits to perform a a specific task. The fourth and top layer is the configuration layer. This layer contains plant specific information which tailors the generic functions to project specific applications. The configuration layer typically represents approximately 0.5 percent of all code. This provides a high degree of confidence in the overall software code because the bottom three layers are standardized and do not change from project to project. It is only the configuration layer which needs to be 'programmed' for specific applications.

Representative samples for each of the four layers of software are provided:

A. Main Program and Support Routines:

- o on line diagnostics
- o engineering unit conversion
- o self calibration
- o limit checking
- o program sequencing

B. Library of General Purpose Modules:

- o Summation
- o Square Root
- o Multiplication
- o Division
- o Lead/Lag
- o High Select
- o Low Select
- o High Trip Comparator
- o Low Trip Comparator

C. Library of Standard Protection Functions

- o Average Temperature and Delta Temperature
- o Pressurizer Pressure
- o Pressurizer Level
- o Containment Pressure
- o Steam Generator Water Level

D. Configuration Layer:

- o Plant-Specific Tag Numbers
- o Analog Input Assignments
- o Channel Trip Assignments
- o Setpoints and Tuning Constants

3.3.2 Software Implementation

All of the executing software is supplied in PROM medium with tunable parameters stored in EEPROM for ease of change. All of the software and documentation is kept under strict configuration management control. All software follows the standards established for software design, which include the following:

A. Language is high-level, easy to maintain language except where necessary for reasons such as timing

B. No interrupts are allowed

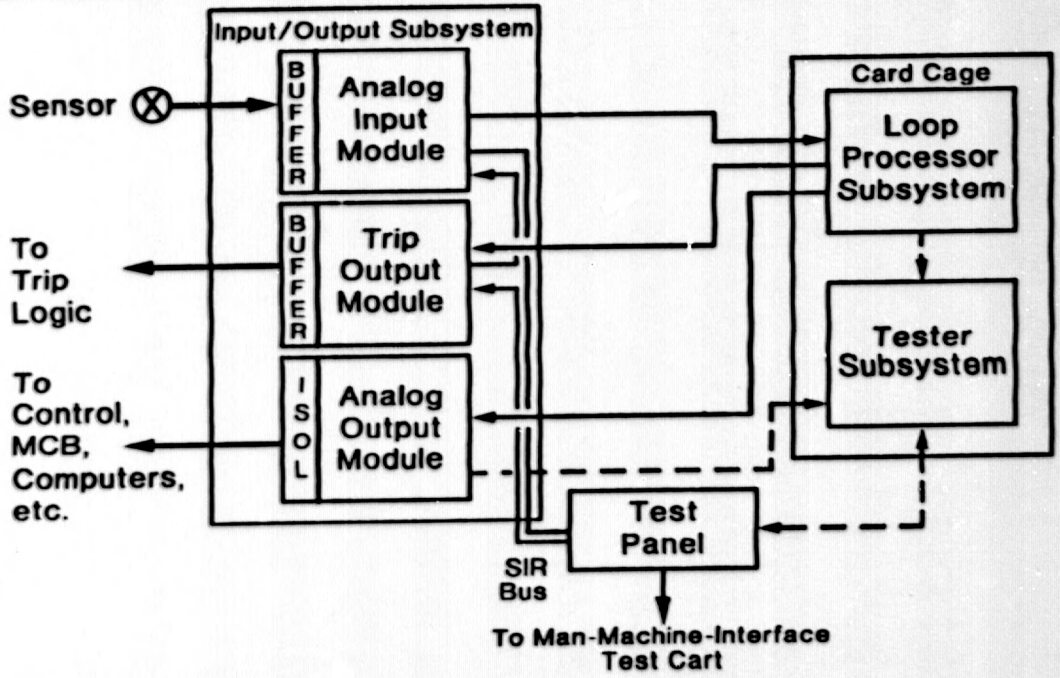
C. No re-entrance is allowed

D. Code format conforms to standards for both high-level and assembly language routines

E. Go to statements are not allowed

F. All programs are single task (no operating system, or multi-tasking system)

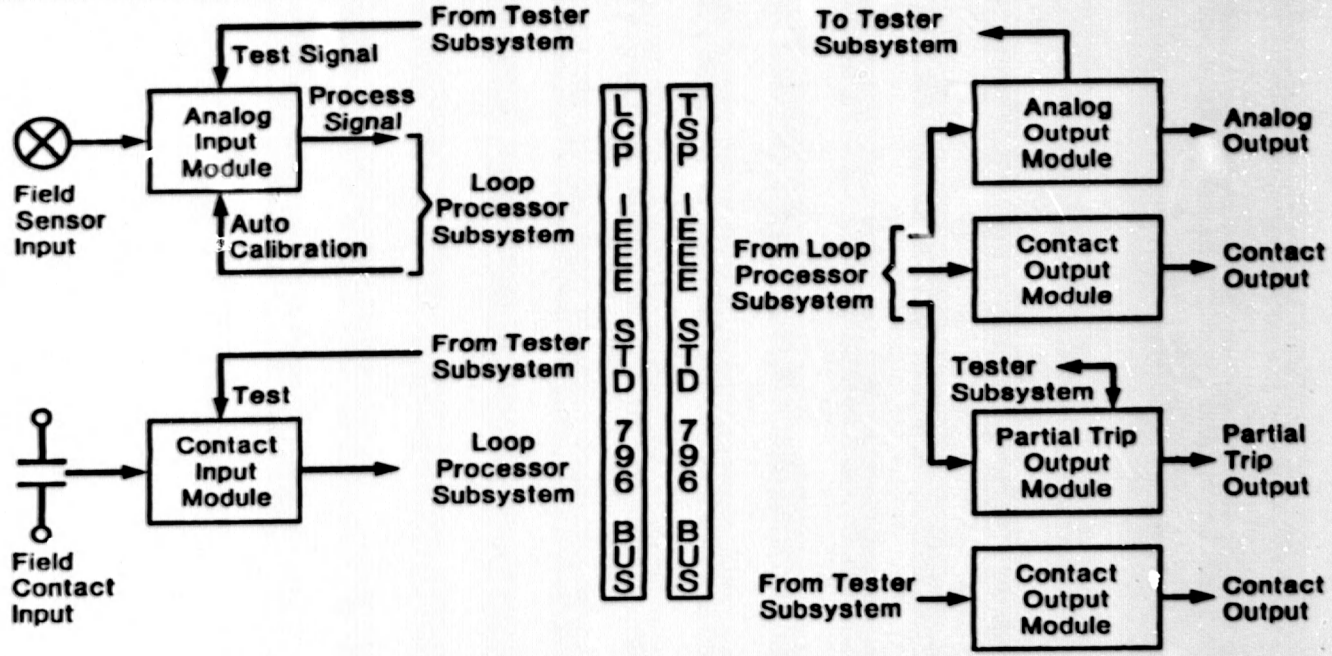
EAGLE-21 SUBSYSTEMS



1070 D20241.005

FIGURE 3-1

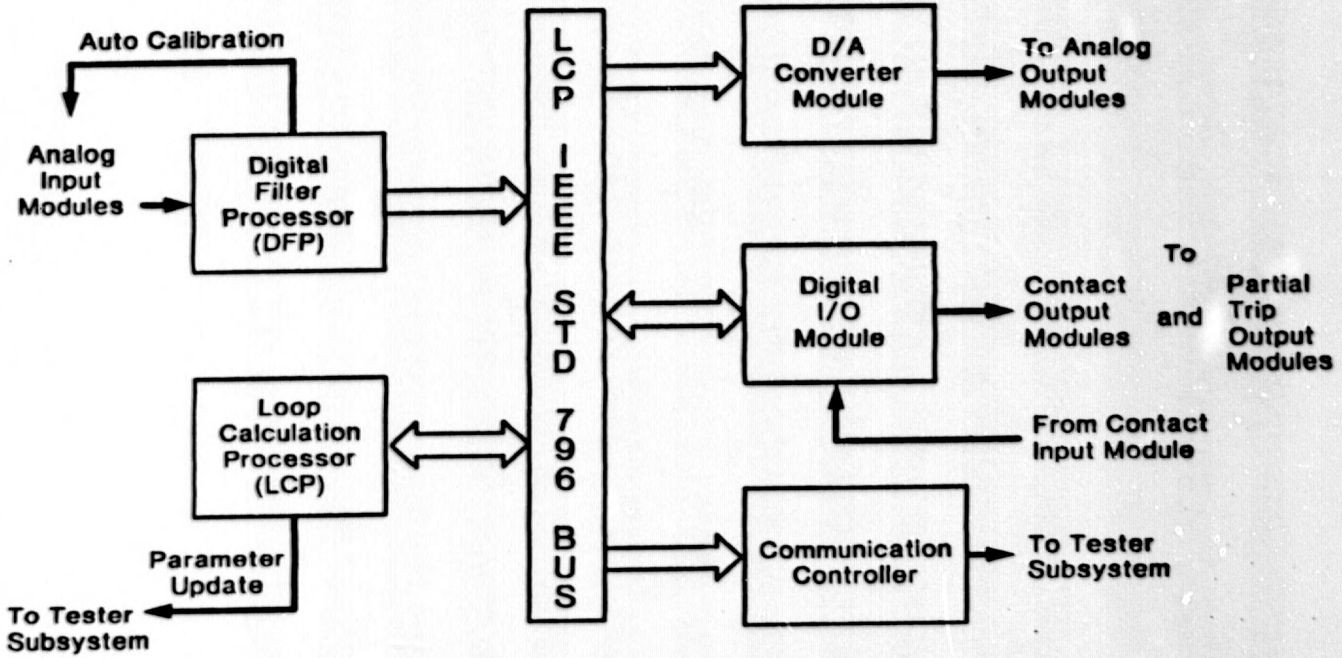
EAGLE-21
INPUT/OUTPUT SUBSYSTEM



1070 D20241.007

FIGURE 3-2

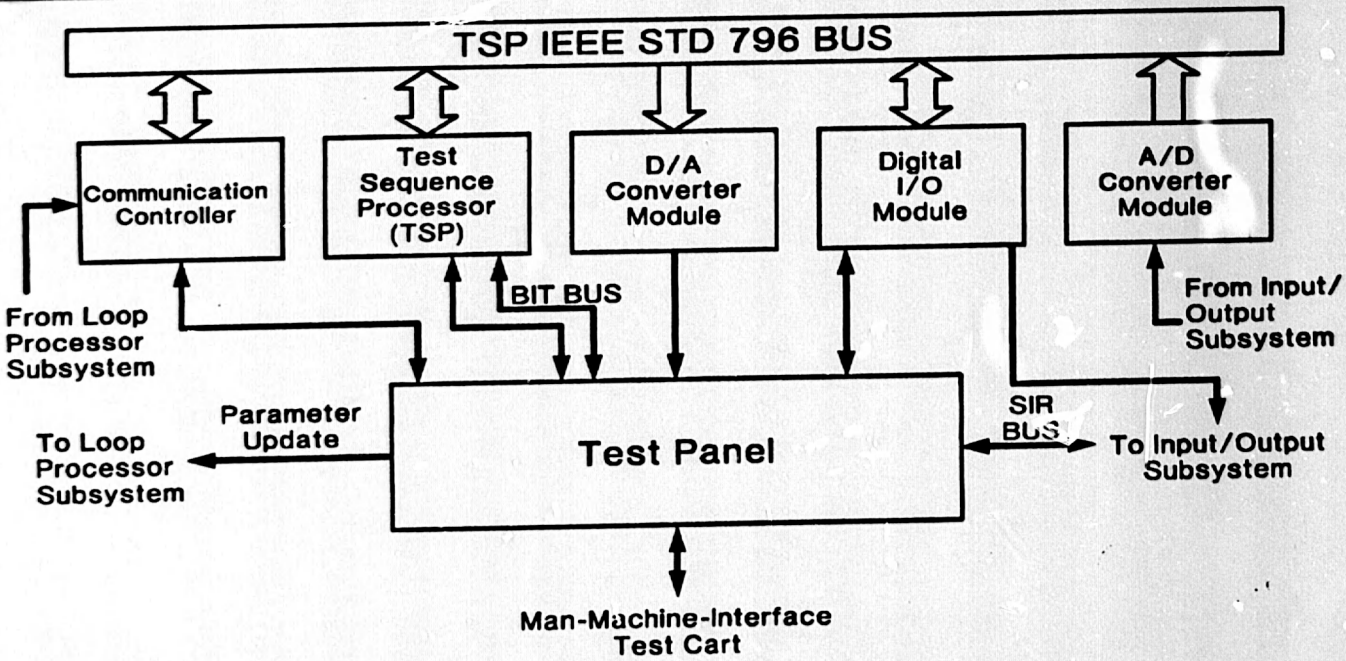
EAGLE-21
LOOP PROCESSOR SUBSYSTEM



1070 D20241.008

FIGURE 3-3

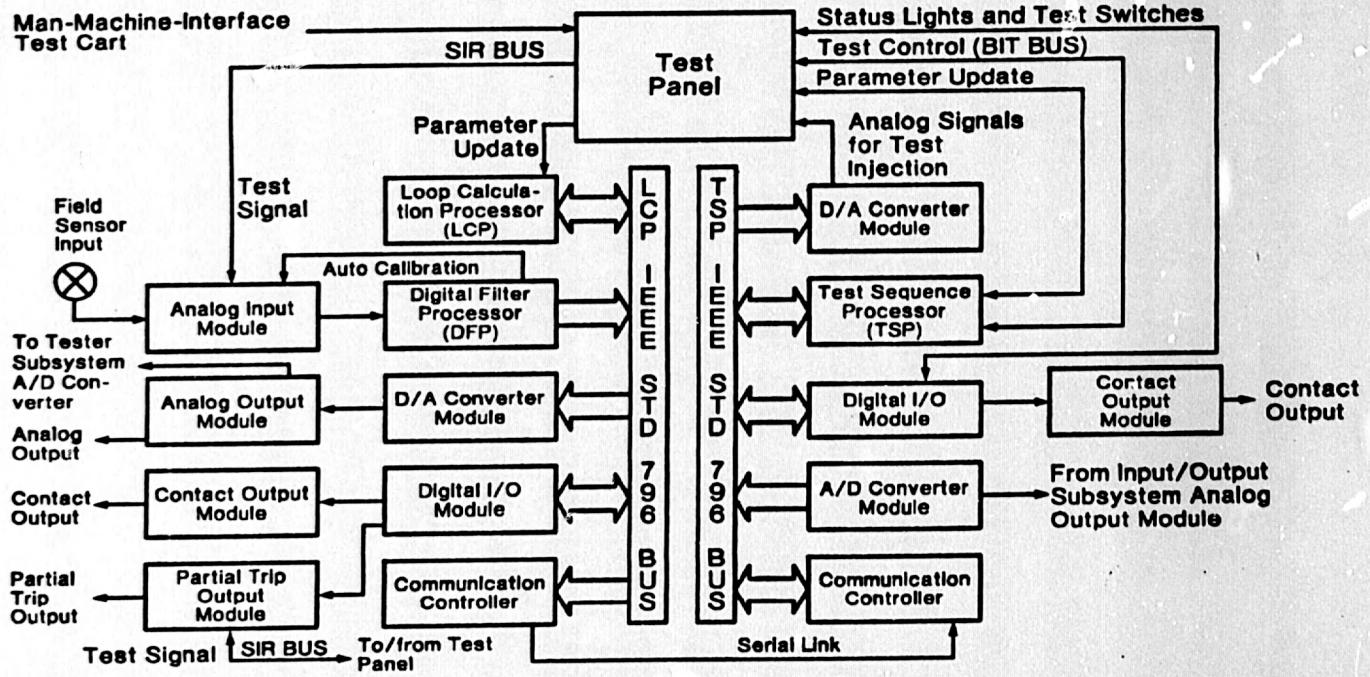
EAGLE-21
TESTER SUBSYSTEM



1070 D20241.009

FIGURE 3-4

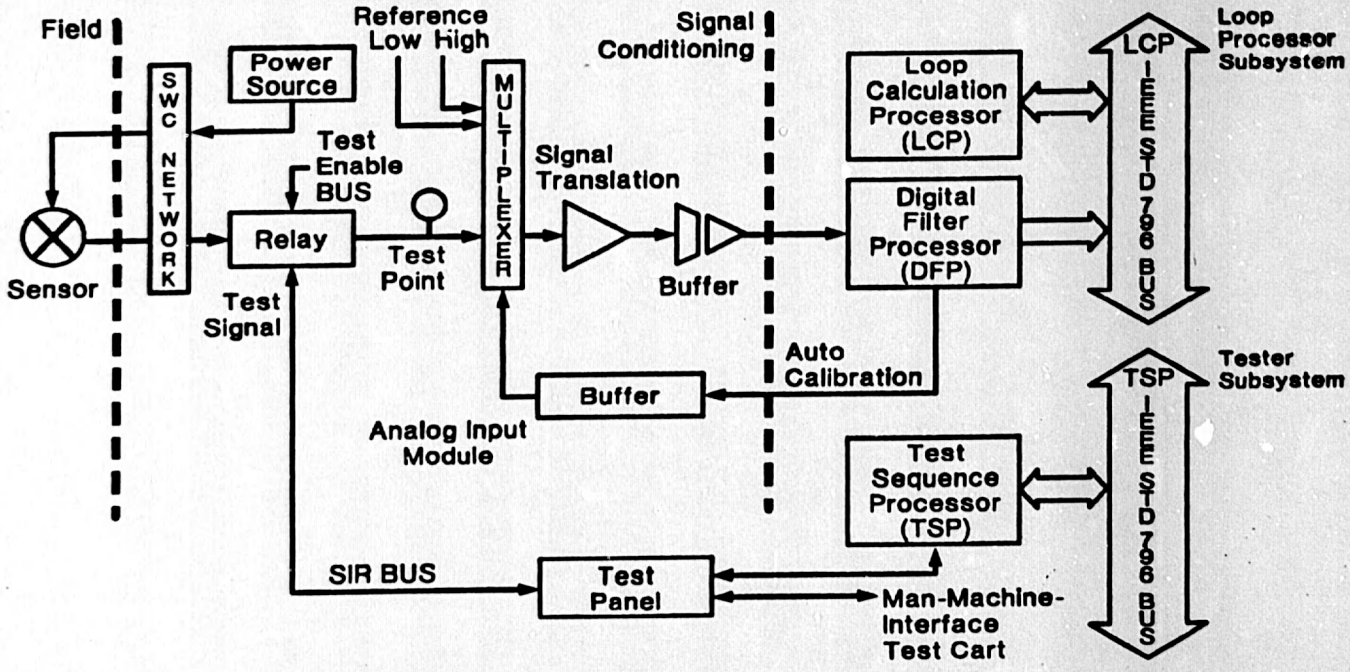
EAGLE-21 ARCHITECTURE



1070 D20241.010

FIGURE 3-5

ANALOG INPUT FUNCTIONAL CONFIGURATION



1070 D202411.006

FIGURE 3-6

CONTACT INPUT FUNCTIONAL CONFIGURATION

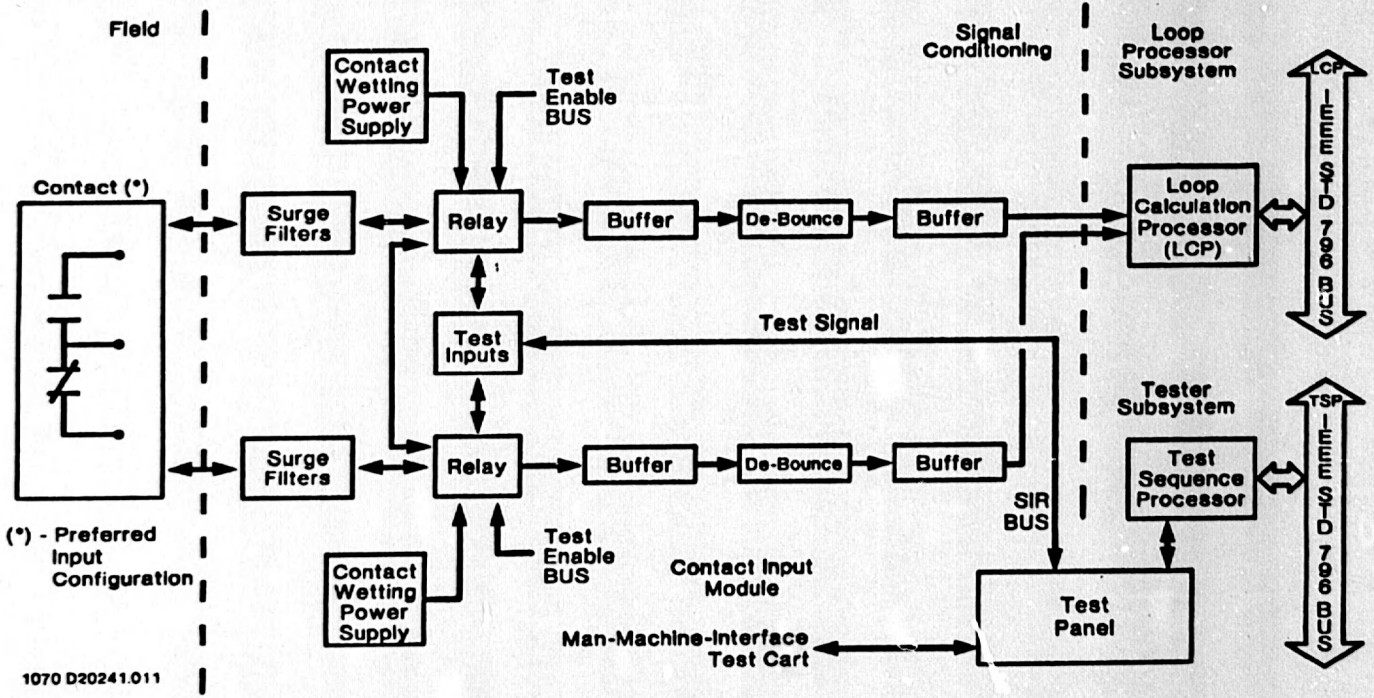


FIGURE 3-7

ANALOG OUTPUT FUNCTIONAL CONFIGURATION

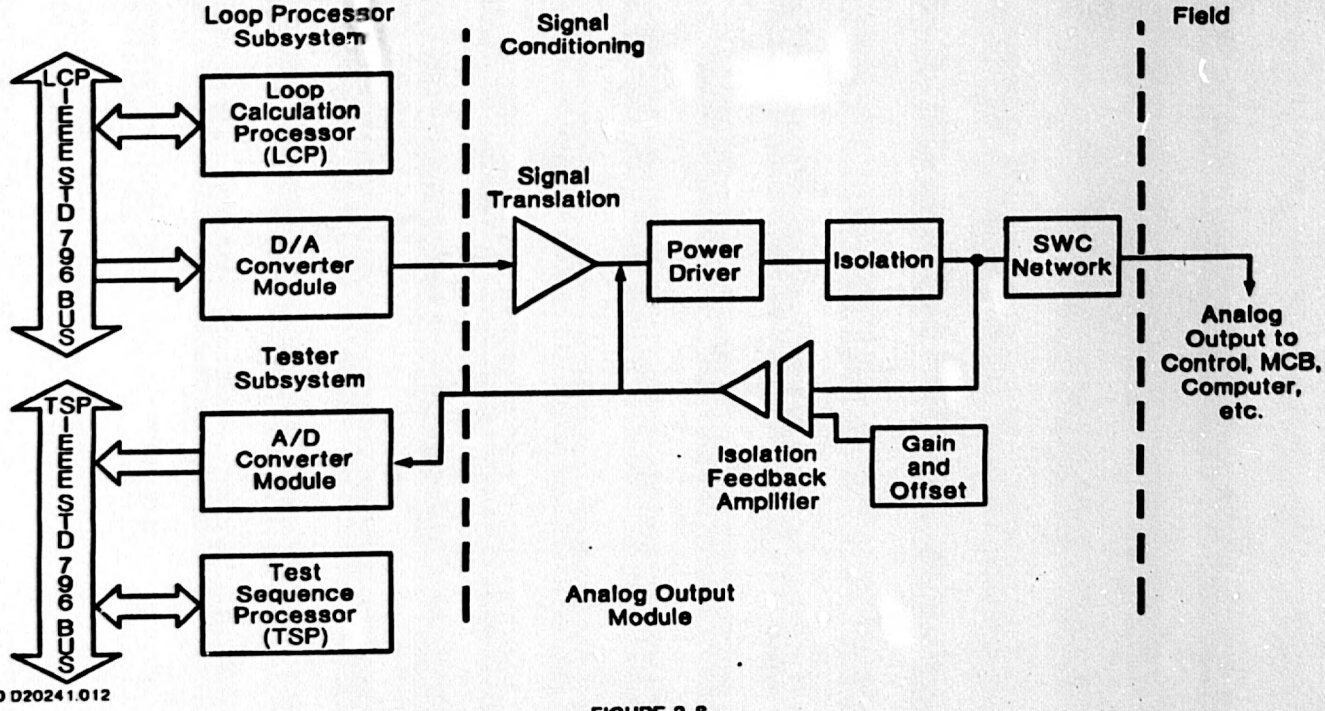


FIGURE 3-8

CONTACT OUTPUT FUNCTIONAL CONFIGURATION

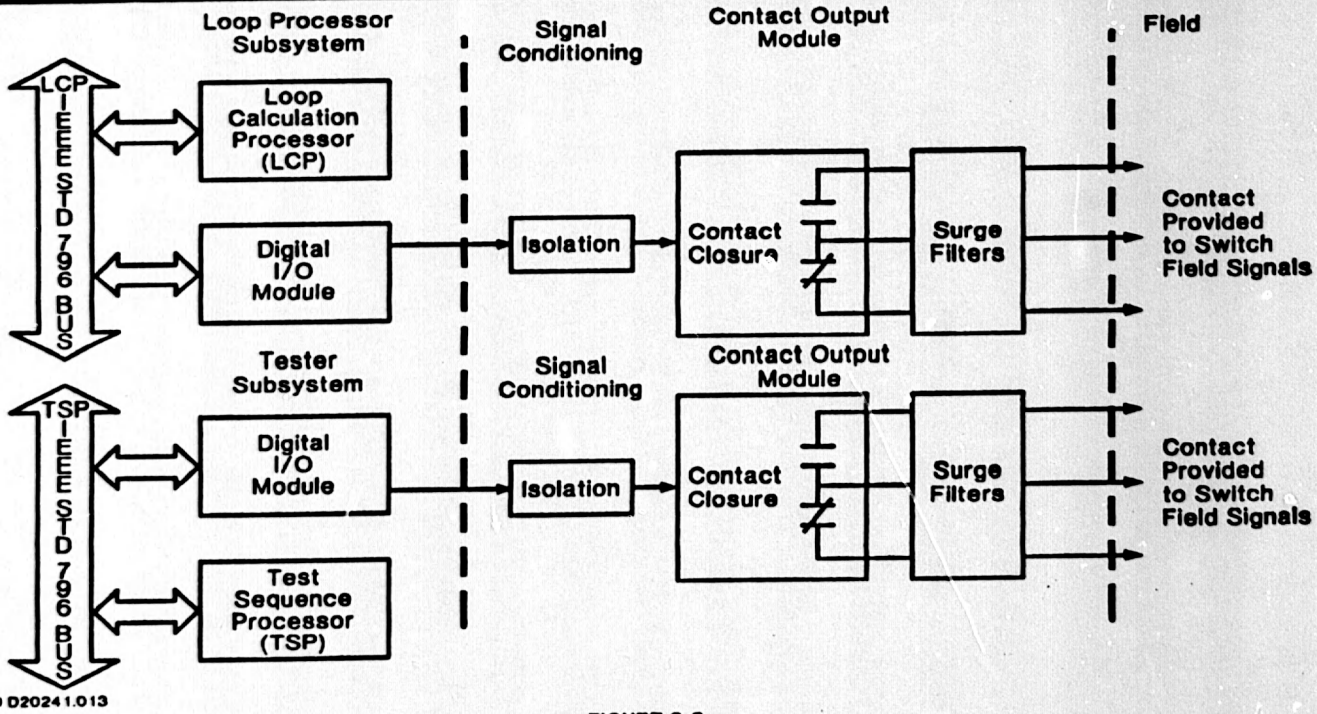
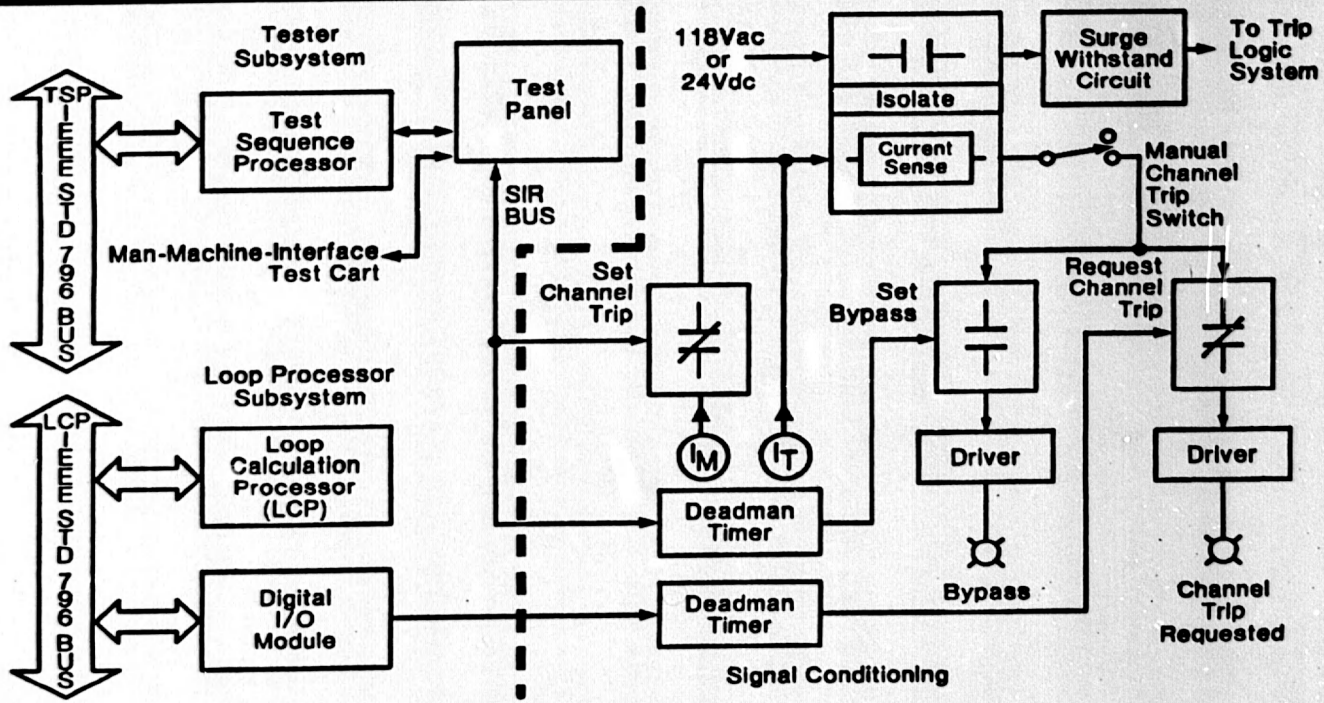


FIGURE 3-9

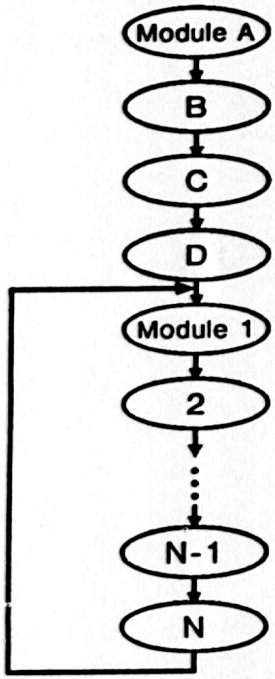
PARTIAL TRIP OUTPUT FUNCTIONAL CONFIGURATION



1070 D20241.014

FIGURE 3-10

SOFTWARE DEVELOPMENT



Deterministic Approach:

- Asynchronous operation of all microprocessors
- No executive (completely distributed processing)
- No interrupts
- Modular software
- Modules are single entry, single exit
- Modules exit to point-of-call
- Modules programmed in a high-level structured language
- Each module has a design performance specification and verificaton test specification

- Restart at Module A; normal operaton: Modules 1 through N

1070 D20241.015

FIGURE 3-11

4.0 EQUIPMENT QUALIFICATION

4.1 Equipment Qualification Background

In November of 1974, the NRC issued Regulatory Guide 1.89, "Qualification of Class 1E Equipment for Nuclear Power Plants" which endorsed IEEE Std. 323-1974, "IEEE Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations" and in March of 1976 the NRC issued Regulatory Guide 1.100, "Seismic Qualification of Electrical Equipment for Nuclear Power Plants" which endorsed IEEE Std. 344-1975, "IEEE Recommended Practices for Seismic Qualification of Class 1E Equipment for Nuclear Power Generating Stations."

Westinghouse recognized that NRC approval of testing methodology and parameters prior to performance of the test is desirable to avoid retesting. Therefore, the initial strategy with the 323-1974 Qualification Program was to obtain NRC approval prior to implementation of the Qualification program. To accomplish this, in October 1975, Westinghouse issued WCAP-8587, Revision 0, "Methodology for Qualifying Westinghouse WRD-Supplied NSSS Safety-Related Electrical Equipment" and in May 1980, Westinghouse issued WCAP-9714, "Methodology for the Seismic Qualification of Westinghouse WRD Supplied Equipment." Meetings were held with the NRC staff to discuss qualification methods. Based on this interaction and state-of-art methodology, revisions were made to WCAP-8587. As a result, WCAP-8587, Revision 6 and WCAP 9714 were accepted by the NRC staff in a letter from Cecil O. Thomas, Chief, Standardization and Special Projects Branch, Division of Licensing, to E. P. Rahe, Jr., Manager, Nuclear Safety Department, Westinghouse Electric Corporation, dated November 10, 1983.

4.2 Equipment Qualification Program Description

The Equipment Qualification Program demonstrates that the Eagle-21 Process Protection Equipment is capable of performing its designated safety-related functions under all specified environmental and seismic conditions. This is accomplished by testing as follows:

4.2.1 Environmental Testing (IEEE Std. 323-1974)

The Eagle-21 equipment is tested under both "normal" and "abnormal" environmental conditions.

Normal:

Temperature	60-80	Degrees F
Relative Humidity	30-50	Percent
Voltage	120	Vac
Frequency	60	Hertz

Abnormal:

Temperature	82-120	Degrees F
Relative Humidity	95-35	Percent
Voltage	108-132	Vac
Frequency	63-57	Hertz

4.2.2 Seismic Testing (IEEE Std. 344-1975)

The Eagle-21 equipment is subjected to multi-axis, multi-frequency inputs in accordance with Regulatory Guide 1.100. The equipment is subjected to both Operation Basis Earthquakes (OBEs) and Safe Shutdown Earthquake (SSE) events.

4.3 Equipment Qualification Documentation

The overall equipment qualification documentation plan consists of three sets of documents:

1. WCAP-8587 "Methodology for Qualifying Westinghouse WRD Supplied NSSS Safety Related Electrical Equipment" which is a Westinghouse Class 3 (Non-Proprietary) report and represents the generic program parent document and describes the basis methodology for the Westinghouse equipment qualification program.

2. WCAP-8587, Supplement 1 "Equipment Qualification Data Packages" (EQDP) is also a Westinghouse Class 3 (Non-Proprietary) report which represents a summary of the program testing. This document identifies the equipment performance specifications and acceptance criteria. Upon completion of testing, this document will be revised to include a summary of test results.

3. WCAP-8687, Supplement 2 "Equipment Qualification Test Reports," (EQTR) is a Westinghouse Class 2 (Proprietary) report and presents specific methods used during testing and results of those tests. All test reports will be coded to the appropriate EQDP reference number.

5.0 NOISE, FAULT, SURGE WITHSTAND CAPABILITY, AND RADIO FREQUENCY INTERFERENCE TESTS

5.1 Test Description

The Noise, Fault, Surge Withstand Capability, and Radio Frequency Interference (RFI) tests demonstrate that the Eagle-21 process protection equipment is capable of performing its designated safety-related functions when subjected to these specified conditions. This testing is accomplished as follows:

5.1.1 Noise Tests

The Eagle-21 equipment is subjected to four types of noise testing:

A. Random Noise

Peak Value: 20 V
Frequency: 10 KHz - 10 MHz

B. Crosstalk Noise -- Chattering Relay Test

1. 118 Vac relay coil, .3 amp nominal
2. 125 Vdc relay coil, .22 amp nominal

C. Military Specification Noise (MIL-N-1900B).

Noise Source No. 1

Voltage: 115 Vdc
Inductance: 3 H
Resistance: 500 ohm

Noise Source No. 2

Voltage: 115 Vac
Inductance: 100 mH
Resistance: 2 ohm

D. High Voltage Transient Noise

Peak value:	3.3 kV
Frequency:	1.25 MHz
Repetition rate:	120 Hz

5.1.2 Fault Tests

The Eagle-21 process equipment is subjected to following fault voltages:

A. 125 vac, 60 Hertz.

B. 580 vac, 60 Hertz

C. 125 vdc

D. 250 vdc

5.1.3 Surge Withstand Capability (SWC) Tests (IEEE Std 472-1974)

The Eagle-21 process equipment is subjected to the following surge signals:

Peak value:	3.3 kV
Frequency:	1.25 MHz
Repetition rate:	120 Hz
Duration:	2 seconds

5.1.4 Radio Frequency Interference (RFI) Tests

The Eagle-21 process equipment is subjected to the following classes of field strengths:

A. 3 V/M and 10 V/M over the entire frequency range of 20 MHz to 1 GHz.

B. 20 V/M over the frequency range of 20 MHz to 500 MHz.

5.2 Test Documentation

The Eagle-21 Noise, Fault, Surge and Radio Frequency Interference (RFI) tests and results will be documented in a separate WCAP.

6.0 DESIGN, VERIFICATION AND VALIDATION PLAN

6.1 Background

Westinghouse introduced the concept of microprocessor based Protection Systems in the early 1970's on the Integrated Protection System (IPS) which was part of the RESAR 414 standard plant. The software verification program conducted on the prototype is documented in WCAP-9153 "414 Integrated Protection System Prototype Verification Program", and WCAP-9739 "Summary of Westinghouse Integrated Protection System Verification and Validation Program".

Building upon the experience gained in performing software Verification and Validation on the IPS prototype and implementing the "lessons learned" from the Nuclear Regulatory Commission (NRC) audit process, a much improved V&V program was defined for the South Texas Qualified Display Processing System (QDPS). The "Design, Verification and Validation Plan for the South Texas Project Qualification Display Processing System" was transmitted to the NRC in a letter from M. R. Wisenburg (Manager of Nuclear Licensing Branch No. 3) dated September 24, 1985. To date, four NRC audits including a "closeout" have been conducted on the South Texas QDPS V&V process with successful results.

The Eagle-21 V&V process is the same as the one conducted on the South Texas QDPS modified only to the extent of refining the process based on previous experience and resolution of NRC audit comments.

The Eagle-21 Design, Verification and Validation Plan is attached as "Appendix A" to this report.

6.2 Applicable Standards

The standards which are applicable to the Eagle-21 Design, Verification and Validation Plan are listed below:

A. IEEE Std. 603-1980

"IEEE STANDARD CRITERIA FOR SAFETY SYSTEMS FOR NUCLEAR POWER GENERATING STATIONS"

B. REGULATORY GUIDE 1.153, December, 1985

"CRITERIA FOR POWER, INSTRUMENTATION, AND CONTROL PORTIONS OF SAFETY SYSTEMS"

-- Regulatory Guide 1.153 endorses the guidance IEEE Std. 603-1980.

C. ANSI/IEEE-ANS-7-4.3.2 -- 1982

"APPLICATION CRITERIA FOR PROGRAMMABLE DIGITAL COMPUTER SYSTEMS IN SAFETY SYSTEMS OF NUCLEAR POWER GENERATING STATIONS"

-- ANSI/IEEE-ANS-7-4.3.2 -- 1982 expands and amplifies the requirements of IEEE Std. 603-1980.

D. REGULATORY GUIDE 1.52, November 1985

"CRITERIA FOR PROGRAMMABLE DIGITAL COMPUTER SYSTEM SOFTWARE IN SAFETY-RELATED SYSTEMS OF NUCLEAR PLANTS"

-- Regulatory Guide 1.152 endorses the guidance of ANSI/IEEE-ANSI-7-4.3.2.

7.0 COMPLIANCE WITH CRITERIA

7.1 IEEE Std. 279-1971

"Criteria for Protection Systems for Nuclear Power Generating Stations. Some of the information in this report demonstrates the means with which the Eagle-21 Process Protection equipment satisifies the applicable requirements detailed in Section 4 of the above criteria. References are provided as follows:

Requirement 4.1 "General Functional Requirement"

-- This report in general describes the Eagle-21 process equipment and its performance requirements.

Requirement 4.2 "Single Failure Criterion"

-- See Section 2.3.1

Requirement 4.4 "Equipment Qualification"

-- See Section 4.0

Requirement 4.5 "Channel Integrity"

-- See Sections 2.3.3, 4.2 and 5.0

Requirement 4.6 "Channel Independence"

-- See Section 2.3.4

Requirement 4.7 "Control and Protection System Interaction"

-- See Section 2.3.5

Requirement 4.9 "Capability for Sensor Checks"

-- See Section 2.3.6

Requirement 4.10 "Capability for Test and Calibration"

-- See Sections 2.3.6 and 2.3.7

Requirement 4.11 "Channel Bypass or Removal from Operation"

-- See Section 2.3.8

Requirement 4.13 "Indication of Bypasses"

-- See Section 2.3.8

Requirement 4.14 "Access to Means for Bypasses"

-- See Section 2.3.8

Requirement 4.18 "Access to Set Point Adjustments, Calibration, and Test Points"

-- See Sections 2.3.7, 2.3.8, and 3.2.7.3

Requirement 4.21 "System Repair"

-- See Section 2.3.10

APPENDIX A

EAGLE-21 REPLACEMENT HARDWARE

DESIGN, VERIFICATION AND VALIDATION PLAN

DESIGN SPECIFICATION SHEET
WESTINGHOUSE FORM 54064G

WESTINGHOUSE ELECTRIC CORPORATION
Nuclear Energy Systems
P.O. Box 355
Pittsburgh, Pennsylvania 15230

DESIGN SPECIFICATION	DATED	REVISION NO.	DATED	ORIGINAL ISSUE	SUPERSEDES PREVIOUS REVISIONS
408A47	11/7/86	1	1/9/87	☐	☒

PROJECT: Generic

EQUIPMENT: EAGLE 21 Replacement Hardware Design, Verification and Validation Plan

SHOP ORDER: 322/393

SYSTEM: Process Protection System

ATTACHMENTS

Reviewed by: S E Long / L E. Erin 11-18-86
Nuclear Safety

REV. 1 S E Long / L E. Erin 01-09-87

☒ NON PROPRIETARY
☐ WESTINGHOUSE PROPRIETARY:

APPROVALS

	ORIGINAL ISSUE	REV. 1	REV. 2	REV. 3	REV. 4	REV. 5	REV. 6
AUTHOR	J.B.Waclo 11/18/86 I.J.Tennenbaum	1/13/87 1/13/87					
SHOP ORDER HOLDER	C.E.Corl 11/18/86 J.B.Waclo 11/18/86	REC 1/13/87 1/13/87					
MANAGER	D.P.Adomaitis 11/18/86	DPA 1/13/87					
PRODUCT ASSURANCE	B.F.Barnett For BFB 11/18/86	RES 1/13/87					
PROJECT MANAGER	W.C.Gangloff 11/15/86	WCG 1/13/87					

TABLE OF CONTENTS

1.0 INTRODUCTION

1.1 Purpose

The purpose of this plan is to provide a description of the design, verification, and validation process and the general organization of activities that are being used in these areas on the Eagle-21 Process Protection System replacement hardware. The material contained herein is modeled after the guidance provided in (a) the 414 Integrated Protection System Prototype Verification Program, which was presented to the NRC in 1977 as part of the Westinghouse RESAR 414 system, (b) ANSI/IEEE-ANS-7-4.3.2-1982 and (c) Regulatory Guide 1.152, and (d) the Design, Verification, and Validation Plan implemented for the South Texas Qualified Display Processing System (QDPS).

1.2 System Functions

The Eagle-21 Process Protection System replacement hardware performs the following major functions:

1. Reactor Trip Protection (Channel Trip to Voting Logic)

2. Engineered Safeguard Features (ESF) Actuations.

3. Isolated Outputs to Control Systems, Control Panels, and Plant Computers.

4. Isolated Outputs to information displays for Post Accident Monitoring (PAM) indication.

5. Automatic Surveillance Testing to verify channel performance.

1.3 System Architecture

The Eagle-21 System Architecture is shown in Figure 1. The basic subsystems are:

1. Loop Processor Subsystem

   The Loop Processor Subsystem receives a subset of the process signals, performs one or more of the protection algorithms, and drives the appropriate channel trip (or partial engineered safeguards actuation) signals. It also drives the required isolated outputs.

2. Tester Subsystem

   The Tester Subsystem serves as the focal point of the human interaction with the channel set. It provides a user-friendly interface that permits test personnel to configure (adjust setpoints and tuning constants), test, and maintain the system.

3. Input/Output (I/O)

The microprocessor based system interfaces with the field signals through various input/output (I/O) modules. These modules accommodate the plant signals and test inputs from the Tester Subsystem, which periodically monitors the integrity of the Loop Processor Subsystem.

2.0 REFERENCES

The following is a list of relevant industrial standards which were considered in the development of this plan:

1. ANSI/IEEE-ANS-7-4.3.2.-1982, "Application Criteria for Programmable Digital Computer Systems in Safety Systems of Nuclear Power Generating Stations"

2. IEEE Std. 279-1971, "Criteria for Protection Systems for Nuclear Power Generating Stations"

3. IEEE Std. 603-1980, "Criteria for Safety Systems for Nuclear Power Generating Stations"

4. WCAP 9153, "414 Integrated Protection System Prototype Verification Program," Westinghouse Electric Corp., August 1977.

5. WCAP 9740, "Summary of the Westinghouse Integrated Protection System Verification and Validation Program," Westinghouse Electric Corp., September 1984.

6. Regulatory Guide 1.97, Rev. 2, "Instrumentation for Light-Water-Cooled Nuclear Power Plants to Assess Plant and Environs Conditions During and Following an Accident," December 1980

7. ANSI/ASME NQA-1-1983, "Quality Assurance Program Requirements for Nuclear Power Plants"

8. IEEE Std 729-1983, "Standard Glossary of Software Engineering Terminology"

9. IEEE Std 730-1981, "Standard for Software Quality Assurance Plans"

10. IEEE Std 828-1983, "Standard for Software Configuration Management Plans"

11. IEEE Std 829-1983, "Standard for Software Test Documentation"

12. IEEE Std 830-1984, "Guide to Software Requirements Specifications"

13. NBS Special Publication 500-75 (February 1981), "Validation, Verification and Testing of Computer Software"

14. NBS Special Publication 500-93 (September 1982), "Software Validation, Verification, Testing Technique and Tool Reference Guide"

15. NBS Special Publication 500-98 (November 1982), "Planning for Software Validation, Verification and Testing"

16. IEC SC 45A/WG-A3 (January 1984), "Draft: Software for computer in the Safety System of Nuclear Power Stations"

17. Regulatory Guide 1.152, "Criteria for Programmable Digital Computer System Software in Safety-Related Systems of Nuclear Power Plants"

18. Regulatory Guide 1.153, "Criteria for Power, Instrumentation, and Control Portions of Safety Systems"

19. Design, Verification and Validation Plan for the South Texas Project - Qualified Display Processing System. Design Specification Number 955842, Revision 3, July 1985.

3.0 DEFINITIONS

The definitions in this section establish the meaning of words in the context of their use in this plan.

COMPUTER SOFTWARE BASELINE - The computer program, computer data and computer program documentation which comprises the complete representation of the computer software system at a specific stage of its development.

DESIGN REVIEW - A meeting or similar communication process in which the requirements, design, code, or other products of a development project are presented to a selected individual or group of personnel for critique.

FUNCTIONAL TESTING (FT) - Exercise of the functional properties of the program to the design requirements.

FUNCTIONAL TEST REVIEW (FTR) - A review which is performed on the documented functional tests that were run by the programmer on his code.

INSPECTION - An evaluation technique in which software requirements, design, code, or other products are examined by a person or group other than the designer to de ct faults, differences between development standards, and other problems.

INTEGRATION TESTS - Tests performed during the hardware-software integration process prior to microprocessor system validation to verify compatibility of the software and the microprocessor system hardware.

MODULE (M) - Refers to a significant partial functional capability of a subprogram and consists of more than one unit. Modules are usually stand-alone procedures or routines which may call other lower level modules or units.

PEER REVIEW - An evaluation technique in which software requirements, design, code, or other products are examined by persons whose rank, responsibility, experience, and skill are comparable to that of the designer.

PROGRAM - Totality of software in a system or one independent part of software of a distributed system implemented by a particular CPU.

SOFTWARE DESIGN SPECIFICATION (SDS) - A document which represents the designer's definition of the way the software is designed and implemented to accomplish the functional requirements, specifying the expected performance. An SDS can be for a system, subsystem, module, or unit.

SOFTWARE DEVELOPMENT PERSONNEL - A team of individuals or an individual assigned to design, develop and document software.

SOFTWARE TEST SPECIFICATION (STS) - A document detailing the tests to be performed, test environment, acceptance criteria and the test methodology. An Approved SDS document forms the basis for the STS.

SOURCE CODE REVIEW (SCR) - A review which is performed on the source code.

SUBPROGRAM (SP) - Refers to a major functional subset of a program and is made up of one or more modules. A subprogram is typically represented by the software executed by a single processor.

STRUCTURAL TESTING (ST) - Comprehensive exercise of the software program code and its component logic structures.

UNIT (U) - The smallest component in the system software architecture, consisting of a sequence of program statements that in aggregate perform an identifiable service.

VALIDATION - The test and evaluation of the integrated computer system to ensure compliance with the functional, performance and interface requirements

VERIFICATION - The process of determining whether or not the product of each phase of the digital computer system development process fulfills all the requirements imposed by the previous phase.

VERIFIER(S) - An individual or group of individuals assigned to review source code, generate test plans, perform tests, and document the test results for a microprocessor system. If the activity is extensive, a chief verifier will be appointed to guide and lead the Verification and Validation personnel.

VERIFICATION TEST REPORT (VTR) - A document containing the test results. In conjunction with the Software Test Specification it contains enough information to enable an independent party to repeat the test and understand it.

4.0 SYSTEM DEVELOPMENT

The development of the Eagle 21 System, as shown in Figure 2, involves three stages:

1. Definition
2. Design
3. Implementation and Test

A brief description of each stage is given below:

1) The definition stage is characterized by the statement of the objective to be achieved, the construction of an initial project plan, and a high-level definition of the system. During this stage, the overall functional requirements of the system are identified. Within Westinghouse, these requirements are brought together in a System Design Requirements document.

2) The design stage is characterized by the decomposition of these System Design Requirements into System Design Specifications and Hardware and Software Design Specifications of sufficient detail to enable the implementation of the system. The Software Design Specifications for the system are then further decomposed into subsystem, module and unit specifications.

3) The implementation and test stage is characterized by the actual construction of the hardware, coding of the various software entities, and testing. The software development team is responsible for the writing, assembling, testing, and documenting the computer code. As the software entities are completed, beginning at the unit level, they are formally turned over to the verifiers for final independent review and/or testing as specified in Section 5.0.

   Software development can be viewed as a sequence of well-defined steps similar to system development. The System Design Specification is used to generate Software Design Specifications which in turn are used to develop high level language programs. These programs are converted by a compiler into assembly language, then by the assembler into machine code. The linker combines groups of assembled code with the library to produce relocatable object code for input to the loader. The loader generates the absolute code which is then burned into read only memory (ROM).

   The use of a high level language allows the designer to express his ideas in a form that is more natural to him. The computer adjusts to his language and not he to the language of the computer. Software written in a high level language is more readily reviewed by an independent party who may not be familiar with the computer assembly language instruction set. Some features of the high level language aid the development of reliable software. For example, block structuring helps identify and reduce the number of possible execution paths.

   As part of testing, the various hardware components and software entities are assembled in a stepwise manner. Additional testing at each step to ensures that each component performs its required function when integrated with its associated components.

The final activity associated with the system implementation and testing stage is the testing of the system. A system test plan is derived from

the system functional requirements and system design specifications to confirm that the system exhibits a level of functionality and performance which meets or exceeds the stated requirements. This final system test is referred to as the Factory Acceptance Test.

Several design assurance techniques are utilized throughout all stages of the development process to ensure that the hardware and software components meet the required specifications.

Formal design reviews are held within Westinghouse to ensure that the System Design Specifications meet the System Functional Requirements. The design review team consists of a group of knowledgeable multidisciplineary engineers to ensure that all aspects of the design are reviewed.

During the implementation and test stage, acceptance testing and review are conducted by the designers on the hardware components, circuit boards, and subsystems to ensure they exhibit a level of functionality consistent with the Hardware Design Specifications and Software Design Specifications.

The final design assurance technique utilized is the execution of the system Factory Acceptance Test to ensure the system performance meets the system functional requirements and system design specifications.

5.0 SYSTEM VERIFICATION

5.1 Introduction

With the application of programmable digital computer systems in safety systems of nuclear power generating stations, designers are obligated to conduct independent reviews of the software associated with the computer system to ensure the functionality of software to a level consistent with that described in the system requirements.

Section 5.2 provides an overview of the verification philosophy. Section 5.3 describes the verification techniques utilized in performing the verification process. Section 5.4 describes the matrix that the verification personnel use for determining the level of verification that should be applied to each software entity. Section 5 concludes by defining the application of the verification matrix to the Eagle-21 Replacement Hardware.

5.2 Verification Philosophy

Figure 2 illustrates the integration of the system verification and validation process with the system design process. The verification process may be divided into two distinct phases: verification of design documentation, and verification of software.

As shown on figure 2, independent verification is performed at each step of the definition and design stages. For example, independent verification will occur to ensure that the decomposition from the

functional requirements and the software requirements to the system design requirements has been performed properly and thoroughly. Similarly, an independent review will be conducted in the decomposition from the system design requirements to the system design specification. Figure 2 illustrates where an independent review and signoff will be conducted during the design process. Verification of the design documentation will be completed prior to the implementation and test phase.

During the implementation and test stage, when the writing, testing, assembling, and documenting associated with each software entity (beginning at the unit level) is completed by the design team, the software entity is formally turned over to the verifier. At this point, an independent review and/or testing of the software entities is performed to verify that the functionality of the software entities meet the applicable Software Design Specifications. After the verifier is satisfied that all requirements are met, the software is configured for use in the final system and subsequent system validation process.

Figure 3 illustrates the philosophy utilized in conducting the software verification process. The verification process begins at the unit software level, i.e., the simplest building block in the software. After all software units that are utilized in a software module are verified, the verifier proceeds to verify that module. Not only is the software module verified to meet the module Software Design Specification, but the verifier ensures that the appropriate units are utilized in generating the software module.

After all software modules necessary to accomplish a software subprogram are verified to meet the applicable Software Design Specifications, the verifier proceeds to verify that subprogram. As in the case of the software module, the verifier not only verifies that the subprogram meets the applicable Software Design Specifications, but also verifies that the appropriate software modules were utilized in generating the subprogram entity. This verification philosophy ensures that the verifier tests and/or reviews the interface between the software unit, module and subprogram entities.

Depending upon the hardware implementation, the verification process may utilize system hardware in the verification of the software modules and subsystems.

5.3 Verification Techniques

Verification techniques used in software development fall into two basic categories: review and testing.

5.3.1 Reviews

There are three types of reviews used in the verification of software: Design documentation reviews, code reviews and functional test reviews.

5.3.1.1 Design Documentation Review

This activity involves the comparison of a design document for a subsystem, module, or unit to the design document of the component above it to ensure that all of the performance requirements stated in the higher level document are met.

5.3.1.2 Source Code Review

Source code review, as opposed to code testing, is a verification method in which the software program is examined visually. The operation of the software is deduced and compared with the expected operation. In effect, the operation of the software is simulated mentally to confirm that it agrees with the specification.

Source code reviews will be used to verify the transformation from a Design Specification into high level code. High level code is easy to read and understand, and therefore full inspection at that level is feasible.

5.3.1.3 Functional Test Review

A functional test review is a review by the verifier of the documentation associated with the functional tests which were performed by the designer. This review will provide a high degree of assurance that the software performs the functions specified in the design requirements.

5.3.2 Software Testing

Software tests can be divided into two categories: structural and functional.

5.3.2.1 Structural Testing

Structural testing, which attempts to comprehensively exercise (via computer emulation) the software program code and its component logic structures, is usually applied at the unit level. The functionality of the program is verified along with the internal structure utilized within the program to implement the required function.
Structural testing requires that the verifier inspect the code and understand how it functions before selecting the test inputs. The test inputs should be chosen to exercise all the possible control paths within the software component. If this is not possible, the test inputs should be chosen to exercise every statement within the component. For example, if

a trigonometric function is calculated in several different ways, depending on the range of the input argument, then the test inputs include tests for the argument in each of these ranges, as well as on the boundaries between ranges. In particular, they exercise the upper limit, the lower limit, and at least one intermediate value within each range.

5.3.2.2 Functional Testing

In the functional approach to program testing, the internal structure of the program is ignored during the test data selection. Tests are constructed from the functional properties of the program which are specified in the Design Specification. Functional testing is the method most frequently used at the module or subsystem level. Examples of functional testing include random testing and special cases by function.

Random testing is the method of applying a test input sequence chosen at random. The method can be used in the following circumstances: to simulate real time events that are indeed random; to increase the confidence level in the correctness of a very complex module; to test a subsystem or a system where it is not necessary to test all the possible paths; to get a quantitative measure on the accuracy of a numeric calculation; or to get a measure of the average time required by some calculation.

Special cases by function can be deduced from the Design Specification of the module and will determine some test cases. For example, a subroutine for matrix inversion should be tested using almost-singular and ill-conditioned matrices. Subroutines which accept arguments from a specified range should be tested with these arguments at the extreme points of the range. An arithmetic package should be tested with variables which have the largest and smallest mantissa, largest and smallest exponent, all zeroes, and all ones and negative variables.

5.4 Verification Matrix

The choice of particular verification techniques to be utilized on a system component is a function of the following parameters:

A. The safety classification of the system

B. The hierarchical level of the software component (unit, module or subprogram)

5.4.1 Safety Classification

The safety classification of an item is defined according to IEEE-279-1971 and IEEE Std 603-1980. In general, the safety classification of the system establishes the verification requirements for the system. However, since all the components contained in the system do not necessarily perform equal safety functions, a higher or lower level of verification may be assigned to specific system components depending on the exact functions performed. If a different level of verification is assigned to a component, the interactions between that component and the other components in the system must be carefully considered and reviewed.

5.4.2 Hierarchical Level of Software Components

For software that is organized in a hierarchical structure, the intricacies of the actual code can not be easily grasped at the upper levels. For all but simple systems it is prudent to approach verification in a progressive manner, beginning at the unit level. It is at the unit level that the code can be most easily inspected or comprehensively tested as necessary.

As the software is built up into higher level components during the integration stage, it becomes possible to demonstrate complete processing functions. This process allows the validation of functional performance requirements. Thus, validation testing assumes a functional theme, with the main emphasis on the interaction between subsystems and their interfaces.

5.4.3 Justification of Matrix Elements

Considering the parameters detailed above, different verification methods are required for different subsystems and software components. Figure 4 illustrates, in tabular form, the levels of verification. The software component columns identify the levels of software. Each element of the matrix specifies the type of testing or review that will be performed on the software component within that classification. The justification of each matrix element follows.

5.4.3.1 Class 1 E Associated Software

The software associated with actuation and/or implementation of reactor trip, engineered safety features, and information displays for manually controlled actions (as defined by IEEE Std. 279-1971 and IEEE Std. 603-1980) must receive the highest level (level 1) of verification identified. As such, all software must be

structurally tested to ensure that all lines indeed meet the intended design specification. Since the plant operators rely upon the automatic actuation of the reactor trips and/or engineered safeguards actuations, as well as information displays for manually controlled actions, the highest level of confidence must be afforded.

5.4.3.2 Non-Class 1E Associated Software

Any associated software that is not directly related to Class 1E variables will receive level 2 verification. This software has the following criteria:

1. Does not generate any Class 1E information.

2. Has no impact on the Class 1E function.

3. Has no direct electrical path to erroneously alter a Class 1E function or its data.

5.4.4. Application of the Verification Matrix and Criteria Utilized for Software Testing for the Eagle-21 Replacement Hardware

5.4.4.1 The Eagle-21 Replacement system can be divided into two groups: 1) that which performs Class 1E protection functions, has impact on Class 1E functions, and which tests Class 1E functions and 2) that which monitors the system and provides non-class 1E information to the user.

The first group consists of the following (Reference Figure 1):

1. All of the Loop Processor Subsystem

2. The portion of the Tester Subsystem that runs surveillance tests and therefore, has an impact on the I/O modules

3. That portion of the Tester Subsystem which controls communication to the Loop Processor for parameter update.

4. That portion of the MMI cart which allows the operator to input new parameters and which does the limit checking on those inputs.

This group, which meets the criteria for Section 5.4.3.1, will be verified at level 1 to give the highest degree of confidence to this code.

The second group consists of the following (Reference Figure 1):

1. That portion of the Tester Subsystem which has no direct link to the Loop Processor other than a read-only datalink. This includes the software which updates the test panel lights and outputs analog trend points.

2. All of the MMI software except that listed in 4) above.

This group will be verified at level 2 since it meets the criteria of section 5.4.3.2.

5.4.4.2 Criteria Utilized for Software Testing

This criteria will be applied to level 1 software units (Refer to Figure 4).

Past experience has demonstrated that emulation testing of very simple procedures is not necessary and that the resources spent testing these procedures could be better applied to the larger, more error-prone code. The following are the criteria used to determine if a procedure can be classified as "simple" and subject to a strict source code review as opposed to testing. If any one of the following statements is true, testing will be performed as usual.

1. The verifier determines that this particular procedure is a unique case and, while all other conditions are satisfied, a code and documentation review is not adequate and that testing should still be performed.

2. Math operations (+, -, /) are done by this procedure and involve at least one variable that is not ROM based and is not a data constant.

3. Logical operations are done by this procedure and the result is used in a manner other than as an ordinary TRUE/FALSE or where the resulting logical byte is NOT accessed according to the definitions:
TRUE equates to (0=0)
FALSE equates to (0=1)

4. Logical operations are done by this procedure for the purpose of setting or clearing (masking) status or control bits.

5. There is more than one path to the procedure due to the use of one or more of the following PLM control statements:
DO-CASE
DO-WHILE

ITERATIVE DO BLOCKS (DO counter = start TO end)
IF-THEN
GO TO

6. The procedure consists of more than twenty executable statements. The term "executable statement" is defined as any statement other than the procedure declare, procedure end, or comments.

7. The procedure includes one or more internal procedures.

6.0 SYSTEM VALIDATION

6.1 Validation Philosophy

Whereas the system verification process verifies the decomposition of the system requirement documents in the definition and design stage and also verifies the functionality of the software entities (unit, module, and subprogram) beginning from the smallest software entity and progressing to the program level, the system validation process is performed to demonstrate the system functionality. By conducting the system validation test, the results demonstrate that the system design meets the system functional requirments. Hence, any inconsistencies that occurred during the system development, in this area, that were not discovered during the various design verification activities discussed in Section 5.0, would indeed be reviewed, identified, and tracked by the verifiers through resolution by the design team.
Following completion of the system validation test, the user can indeed have a high degree of confidence that the system functional requirements are met.

6.2 Validation Testing Overview

During verification, a bottom-up microscopic approach is utilized to thoroughly and individually review and/or test each piece of software within the total system. This requires a significant effort and verifies that each software element operates properly as a stand-alone entity.

Validation complements the verification process and not only insures that the final implemented system satisfies the top-level functional requirements but also that good engineering practice was utilized during the design and implementation of the system. Following are the major phases of validation:

* Top-down functional requirements testing
* Prudency review of the design and its implementation
* Specific Man-Machine Interface (MMI) testing

The macroscopic top-down functional requirements phase of validation testing treats the system as a black box while the prudency review phase requires that the internal structure of the

integrated software/hardware system be analyzed in great detail. Due to this dual approach, validation testing provides a level of thoroughness and testing accuracy which is at least equivalent to that which occurs during verification and insures detection of any deficiencies that occurred during the design process but not discovered during verification. Validation testing is performed on the verified software residing within the final target hardware.

6.2.1 General Description

The Validation plan defines a methodology that must be followed to perform a series of top-down functional requirement based reviews and tests which compliment the bottom-up approach utilized during the Verification testing phase.

Four independent types of reviews and/or tests are to be conducted to insure over-all system integrity:

1. Functional Requirements Testing - this insures that the design meets the functional requirements.

2. Abnormal-mode Testing - this insures that the design operates properly under abnormal-mode conditions.

3. System Prudency Review/Testing - this ensures that good design practice was utilized in the design and implementation of critical areas of the system. The items covered within this section require the internals of the system design and implementation to be analyzed in detail.

4. Specific Man-Machine Interface testing - this insures that the operator interface utilized to modify the system's data-base performs properly under normal-mode and abnormal-mode data-entry sequences. This is a critical area requiring special attention due to the impact on the software of the system-level information which can be modified via this interface.

The functional requirements and abnormal-mode testing phases of Validation utilize a black-box systems approach while the System Prudency Review/Testing phase emphasizes the need to understand the internal operations and interactions within the system.

6.2.2 Top Level Functional Requirements

The functional requirements serve as the basis for identifying the tests that must be conducted during the Validation testing phase.

6.2.3 Functional Requirements Testing

The Validation functional requirements testing phase consists of the following steps:

1. Functional requirements decomposition

   The top-level functional requirements must be decomposed into detailed sub-requirements. For each sub-requirement, a test or a series of tests must be identified and performed to insure that the specific sub-requirement is satisified.

   Some sub-requirements are fairly general so it is important that the same individual that performs the decomposition also provides the interpretation as to the type of test which must be executed to insure that the sub-requirement is met.

2. Validation test procedure generation

   Once the decomposition has occurred, the specifics of the test(s) must be defined in test procedural form such that it (they) can be conducted during validation testing.

3. Validation test execution (Refer to Section 7.3)

   The detailed tests per the Validation test procedures must be conducted by a Validation Test Technician and the results must be reviewed by the Validation Test Engineer.

Each functional sub-requirment must be uniquely identified. The test procedure generated to test each sub-requirement must be cooresponding identified for ease of cross-referencing.

6.2.4 Abnormal-Mode Testing

During this phase of Validation the functional requrements are reviewed to define a series of abnormal conditions underwhich the system must operate properly without results in or causing any inadvertent or detrimental actions.

The Validation abnormal-mode testing phase consists of the following steps:

1. Functional requirements decomposition

   The top-level functional requirements must be reviewed to identify detailed abnormal-mode conditions. The type of test that must be conducted to exercise the system under each abnormal-mode condition must also be defined.

2. Validation test procedure generation

   Once the decomposition has occurred, the specifics of

the test(s) must be defined in test procedural form such that it (they) can be conducted during Validation testing.

3. Validation test execution (Refer to Section 7.3)

   The detailed tests per the test procedures must be conducted by a Validation Test Technician and the results must be reviewed by the Validation Test Engineer.

Each abonormal-mode condition must be uniquely identified. The test procedure generated to test each sub-requirement must be correspondingly identified for ease of cross-referencing.

6.2.5 System Prudency Review/Testing

During this phase of Validation, the system design and implementation is analyzed and reviewed against the "System Prudency Checklist". The system must be evaluated against this checklist to insure that good engineering practice has been followed.

The System Prudency Checklist addresses the following critical design areas:

* Firmware program storage
* Data-base information storage
* Multiple-processor shared memory architectures
* Data-link oriented system architectures
* Diagnostics
* System time synchronization

Most of these items do not relate directly to a functional requirement or to a series of functional requirements but address the issue of integrated system integrity.

7.0 DEVELOPMENT, VERIFICATION AND VALIDATION ORGANIZATION

During the system design process, two independent functions will be utilized: one for development, and one for verification. The software development personnel receive the System Design Specification, generate the Software Design Specifications, and then designs, develops, tests, and documents the code. The verification personnel receive the released code and its documentation, performs the required reviews and tests as dictated by the Software Verification Level within the Verification Matrix and produces a Verification Test Report (VTR).

This type of organization has several advantages. The use of two

independent entities introduces diversity to the process of software generation and reduces the probability of undetected errors. Another benefit is that such a scheme forces the designer to produce sufficient and unambiguous documentation before verification can take place.

Functional independence is essential to achieve these goals. In particular, the two functions will have separate lead engineers. Note that the development personnel submits the code for verification only after the development team has confirmed the code to its satisfaction. Errors discovered (debugging) during the development phase testing are not required to be documented by the verification engineers.

The use of the above procedures does not preclude the possibility that the developer of one module may be the verifier of a different module, as long as that person did not participate in the design or coding of the module being verified.

7.1 Development Activity

The composition of the development team is dependent upon the functions that are required to be performed by the team. Typical team functions include the following:

7.1.1 Chief Programmer

This is the team software leader who is responsible for the software technical matters. The duties of the Chief Programmer include:

a. Software Design Specification

The chief programmer has the responsibility for the development of the Software Design Specifications, which are based on the System Design Specification.

b. Architecture

Global decisions on the structure of the software, decomposition and data base are made by the chief programmer.

c. Coding

Some critical sections of the programs (both in terms of importance and complexity) can be coded by the chief programmer.

d. General

The chief programmer supervises the rest of the team in software technical matters.

7.1.2 Programmers

It is anticipated that there will be more than one programmer,

and that at least one programmer will function as a back-up to the chief programmer. The programmers' tasks are to develop the code for modules and/or sub-systems as directed by the Software Design Specifications.

7.2 Verification Activity

The functions of the verification team are as follows:

7.2.1 Chief Verifier

Team leader who is responsible for all technical matters. The duties of the Chief Verifier include:

a. Review System Design Requirements and Specifications received from the development engineer for completeness and unambiguity. (This review may be performed by another qualified individual who is independent of the design area being reviewed.)

b. Review the Software Design Specifications received from the development engineer for completeness and unambiguity.

c. Review verifier's Software Test Specificatins for completeness.

d. Oversee verification of critical sections in the software.

e. Supervise and consult with the verification team.

f. Review Test Reports

7.2.2 Verifiers

a. Perform source code inspections and review Software Design Specifications.

b. Write Software Test Specifications.

c. Run tests on subprograms, modules and units.

d. Write test reports.

7.2.3 Librarian Function

The Librarian performs the following duties in the maintenance of the Verification Software Library:

a. Responsible for the storage and configuration control of the computer software being verified as follows:

(1) Establishes identification of each software element (i.e. unit, module, subprogram) within the Computer Software Baseline (CSB)

(2) Enforces procedures for software and documentation changes during reverification effort

(3) Maintains configuration control of the current CSB

b. Controls the transmittal of computer software to authorized personnel only

c. Ensures no unauthorized changes occur to the CSB

7.3 Validation Function

The functions of the Validators are as follows:

7.3.1 Chief Verifier

a. Coordinate total Validation program

b. Review Validation testing results and write final report

c. Supervise and consult with the validators

7.3.2 Functional Requirements Decomposer (optional/Chief Verifier)

a. Coordinate Validation of a specific area

b. Review functional decomposition for completeness and accuracy (this review may be performed by another qualified individual who is independent of the design area being reviewed)

7.3.3 Lead Validator (optional/Chief Verifier)

a. Coordinate Valdation of a specific area

b. Review functional decomposition for completeness and accuracy (this review may be performed by another qualified individual who is independent of the design area being reviewed)

c. Review and approve test procedure vs functional requirement test specification to insure test procedure is adequate

d. Along with the Librarian, insure that proper verified code is being validated

7.3.4 Validation Test Engineer

a. Write Validation test procedures

b. Oversee Validation testing and review test results

c. Generate Validation Trouble Reports

7.3.5 Librarian

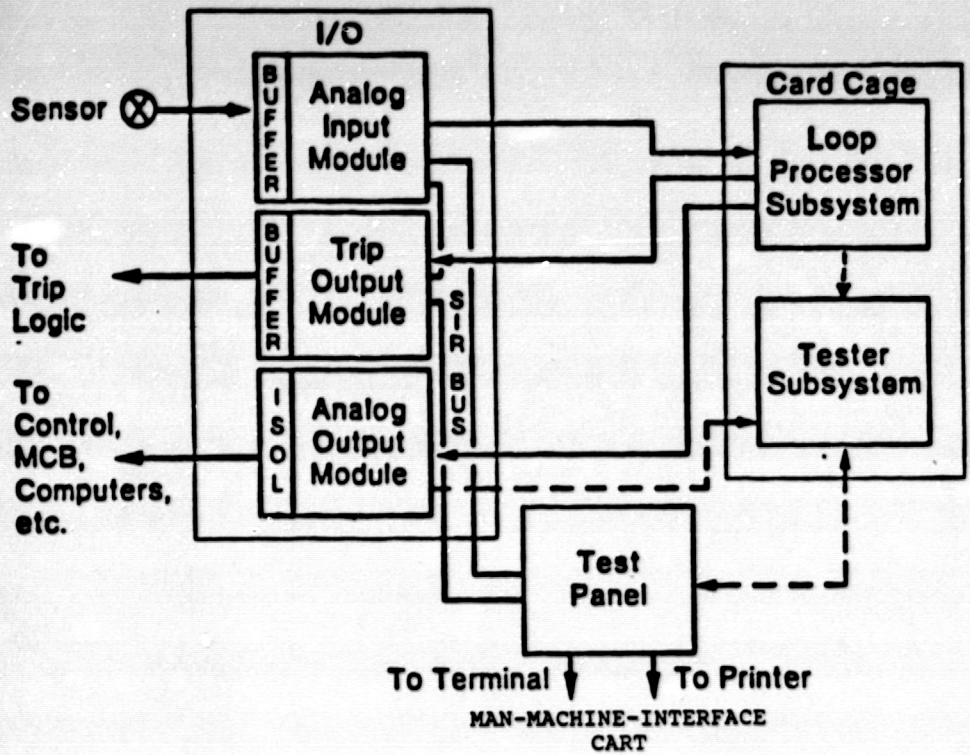
a. Coordinate with the Chief Verifier/Lead Validator(s) and/or Validation test Engineers to insure that proper verified code is being validated.

b. Coordinate dissemination of Validation trouble reports to the appropriate design engineer.

7.3.6 Validation Test Technician

a. Perform Validation tests under direction of the Validation Test Engineer

b. Document test results



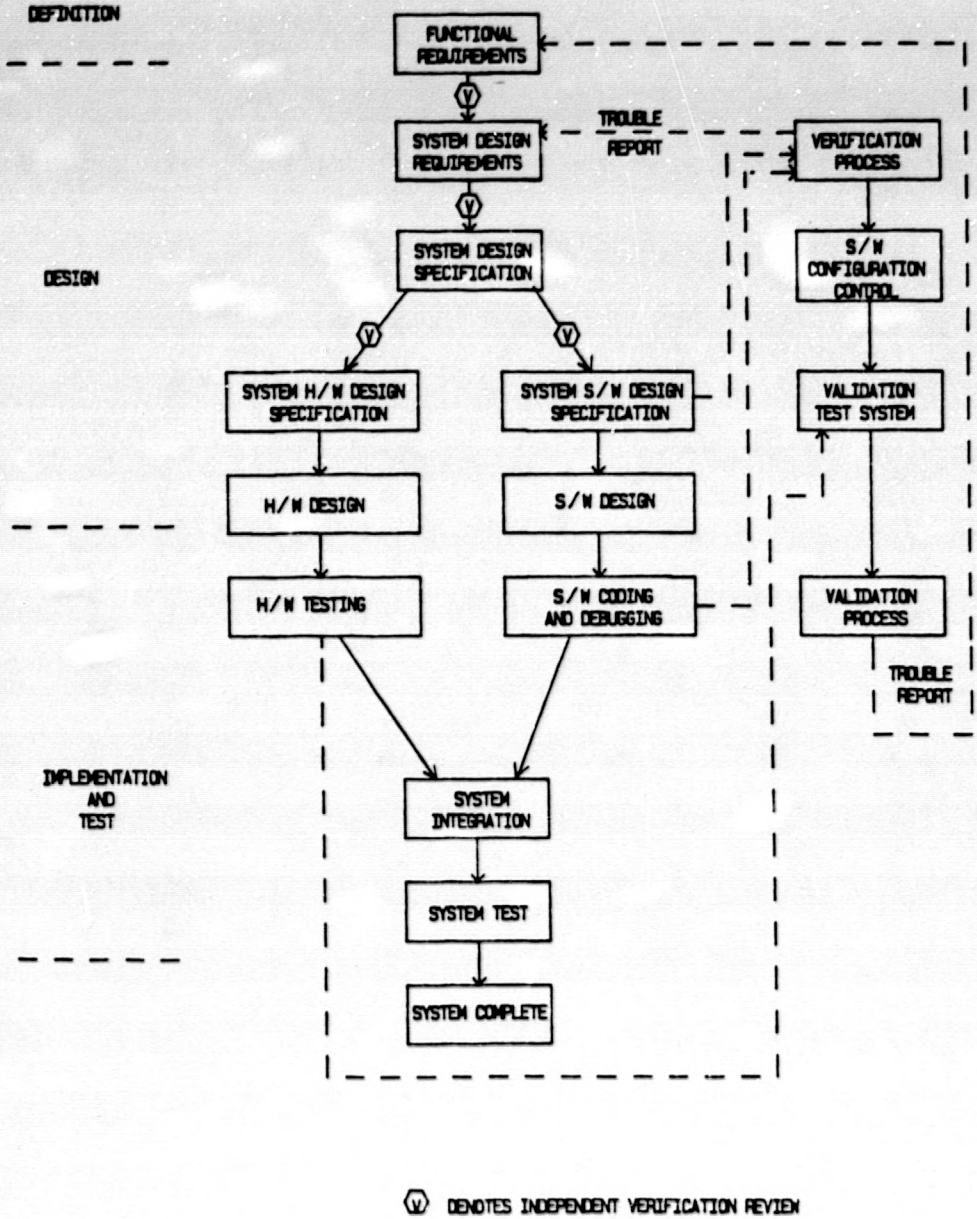
EAGLE - 21

PROCESS PROTECTION SYSTEM

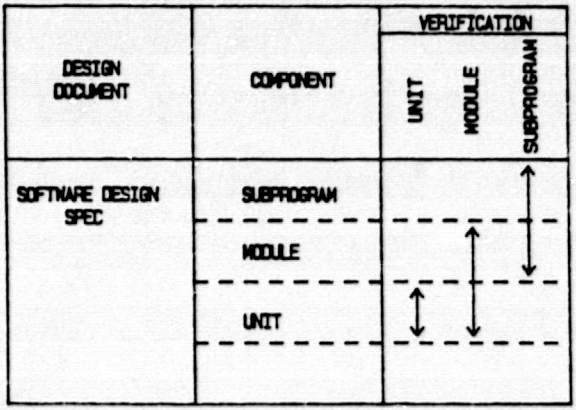
ARCHITECTURE

FIGURE 1

FIGURE 2
DESIGN, VERIFICATION AND VALIDATION PROCESS



(V) DENOTES INDEPENDENT VERIFICATION REVIEW



SOFTWARE VERIFICATION PROCESS

FIGURE 3

SOFTWARE VERIFICATION LEVEL	SOFTWARE COMPONENT			
	UNIT	MODULE	SUBPROGRAM	
1	• NOTE 1 ST	ST	ST	INDEPENDENT TESTING
2	FTR	FTR	FTR	↑ SEPARATE REVIEW ↓

ST = STRUCTURAL TESTING
FTR = FUNCTIONAL TEST REVIEW

• NOTE 1: REFERENCE CRITERIA IN SECTION 5.4.4.2

SOFTWARE VERIFICATION MATRIX
FIGURE 4