HF CONTROLS

HFC-6000 Control System

ERD111 – Control System Qualification Project

Test Specimen Validation Test Procedure
TP0408B

Rev B

NON-PROPRIETARY

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8/23/03	A0	J Taylor	Preliminary Draft
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1.0 PURPOSE AND SCOPE

A specially configured HFC-6000 control system (Test Specimen) has been configured for generic qualification as a commercially available control system for safety-related applications in nuclear power plants. This procedure covers functional verification of the hardware configuration of the Test Specimen following reconfiguration in preparation for repetition of the seismic test. This test will be performed prior to repetition of the Prudency and Operability test at HFC, and it will be repeated after the Test Specimen is assembled on the Seismic Simulator table at Wyle.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

This test procedure constitutes part of the prequalification testing for the HFC-6000 control system. These tests have been developed to document the baseline performance of the control system Test Specimen prior to the start of qualification stress testing.

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants

2.2 HFC DOCUMENTATION

TN0401	Master Test Plan
VV0414	Master Configuration List
700907-01	TSAP Logic Diagram
700907-02	Single-Loop Controller TSAP Logic Diagram
700908-01	HPAT Logic Diagram
SCR 912	

2.3 HFC INTERNAL STANDARDS AND PROCEDURES

QPP 5.1	Review and Approval of Quality Documents
QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-205	Develop Software/Firmware Test Procedure
372000-43	WIN_EWS User's Guide

2.4 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

CSM	Control Switch Module
EWS	Engineering Workstation (HFC PC software utility)
HIFR	Host Interface Remote

HPAT	HFC Plant Automated Tester
JCRT	Java CRT (HFC PC software utility)
LED	Light Emitting Diode
M/A	Manual/Automatic
PC	Personal Computer
RTD	Resistance Thermal Detector
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test System Application Program

3.0 PREREQUISITES

The following paragraphs define the equipment, setup, and configuration requirements for conducting the TSAP Validation Tests.

3.1 EQUIPMENT REQUIRED

This test will be conducted after rewiring and reconfiguration of the Test Specimen is complete to verify that wiring and logic changes have been incorporated correctly. Minimum equipment requirements for running this test are as follows:

- Fully integrated Test Specimen with updated TSAP logic 700907-01 and 700907-02.
- HPAT configured as required by 700908-01.
- All communication links and I/O cables installed as indicated by 700915-00.
- Multimeter

3.2 ENVIRONMENTAL CONDITIONS

The TSAP validation test will be conducted at HFC and at Wyle Labs under ambient environmental conditions.

3.3 TEST PERSONNEL

All of the testing and monitoring functions will be conducted by one or more qualified HFC test engineers both at the HFC facility and at Wyle Labs.

3.4 PRECAUTIONS

WARNING

Certain I/O circuits are energized with high voltages and may carry potentially hazardous current loads. Exercise caution whenever working around exposed terminals or circuitry.

3.5 RED-LINE POLICY

The HFC policy for entering red-line corrections into a test procedure are presented in paragraph 2.6 of TN0401. Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.6 TEST SETUP REQUIREMENTS

Validation that test setup is complete: _____
Name/Date

4.0 TEST SEQUENCE

The overall validation test will verify all I/O signal routing and functional operation of the Test Specimen prior to the start of the Operability and Prudency tests.

4.1 I/O SIGNAL ROUTING VERIFICATION

4.2 SIMULATED CONTROL FUNCTIONAL TESTS

The TSAP for the main Test Specimen controller includes six simulated digital control loops and three simulated analog control loops; the TSAP for the single-loop controller includes one simulated digital control loop. Functional operation of the logic for these loops was validated during the original execution of the TSAP Validation Test (TP0408). The present test will be limited to validation of the logic changes made prior to the rerun of the seismic qualification test.

4.2.1 TO6 Air Circuit Breaker Control Logic

The only modification to this logic consisted in the addition of a software switch to permit selection between CRT control of CSM inputs and the hardware interface with the physical CSM.

4.2.2 TO7 Solenoid Control Logic

The only change to this logic consisted in the addition of the software switch to enable/disable JCRT control of the CSM inputs.

4.2.3

TO8 Non Reversing Motor Starter Control Logic

The only change to this logic consisted in the addition of the software switch to enable/disable JCRT control of the CSM inputs.

4.2.4 TO9 Reversing Motor Starter Control Logic

The only change to this logic consisted in the addition of the software switch to enable/disable JCRT control of the CSM inputs.

4.2.5 TO10 Simulated ESFAS Control Logic

No change was made to this logic, so no additional testing is necessary.

4.2.6 TO12 Simulated Main Feedwater Isolation Valve Control Logic

The only change to this logic consisted in the addition of the software switch to enable/disable JCRT control of the CSM inputs.

4.2.7 Simulated Analog Control Loops

All changes to the TSAP logic diagrams consisted in the incorporation of redline corrections that had been made in the code during the previous testing. No further testing of these modifications is required. However, the hardware interface with the M/A stations was not previously available. If the HFC-PCC06 is operational, testing will consist of verifying M/A station functions for each loop.

4.2.8 Single Loop Controller Logic

The single loop controller TSAP contains simulated switchgear control logic. This logic was modified to permit installation of the HFC-PSR06 module in the rack. The modification consisted of removing the HFC-DC34 module from slot 1 and deleting all associated logic and I/O wiring.

5.0 ACCEPTANCE CRITERIA

Acceptable results for the TSAP consists in verification of the specific conditions listed in Table

Table 1. TSAP Acceptance Criteria

I/O Wiring	
	Each output point is connected to the input point identified on the logic diagram.
	Each SOE point is connected to the correct SOE channel.
	Wiring for each chatterbox point clearly labeled with a wire tag.
Digital Loops	
	The software switch on the main index page enables/disables JCRT control of CSM control inputs.
	If the HFC-PCC06 is operational, the hardware CSMs enable functional control of logic operation.
Analog Loops	
	If the HFC-PCC06 is operational, the hardware M/A stations enable functional control of logic operation; if the HFC-PCC06 is not operational, software meterfaces can control loop operation.
SLC Logic	
	The analog BOE signal controls dynamic operation of logic operation.

6.0

ATTACHEMENTS

The following forms are attached to this document:

- Test Equipment Log

7.0 QA RECORDS

Completion of the test procedure will be indicated by individual signoffs within this document. Both the test procedure with completed signoffs and the attached Test Equipment Log will be regarded as permanent QA records and will be filed in accordance with the Project Quality Plan.

Test Data Record

Test Plan: TN0401, Attachment D
Test Equipment Log

Test Equipment	Instrument ID	Cal Due Date

Test Engineer _____ Date _____

HFCONTROLS

HFC-6000 Control System

ERD111 – Control System Qualification Project

ESD Test Procedure
TP0409

Rev C

NON-PROPRIETARY

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1/03	0	J Taylor	Preliminary Draft
1/03	1	J Taylor	Review comments incorporated
2/03	A	J Taylor	Initial Release
4/03	B	J Taylor	Product line name changed to HFC-6000
1/20/04	C	J Taylor	Inc. comments from outside consultants and changes for final design configuration

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1.0 PURPOSE AND SCOPE

The HFC-6000 control system (Test Specimen) is designed to operate in a wide variety of industrial applications. The control system hardware may be installed both in an electrical equipment room and at various other locations near the equipment under control. In either case, the potential exists for exposure of sensitive electronic components to high voltage electrostatic discharges. The test covered by this document subjects each major component of the Test Specimen to simulated ESD pulses to establish its capability to withstand such discharges without disabling or disrupting normal operation.

The following references in the EPRI TR-107330 standard define the scope and content for this procedure: 4.3.8, Table 5-1, 6.3.1.B, 6.4.2

The level of ESD immunity required is defined in EPRI TR-102323-R1 Appendix B Paragraph 3.5. ESD testing will be conducted by Wyle Laboratories based on Wyle Test procedure 50044-10 Appendix I. The test method to be used is defined by IEC 1000-4-2 (equivalent to IEC 801-2).

2.0 REFERENCES

2.0 INDUSTRY STANDARDS

This test procedure has been developed to encompass ESD immunity testing requirements for Class 1E control system equipment as stipulated by the following standards.

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants
EPRI TR-102323-R1	Guidelines for Electromagnetic Interference Testing in Power Plants
IEC 1000-4-2	Electromagnetic Compatibility, Part 4: Testing and measurement techniques – Section 2: Electrostatic discharge immunity test (technically equivalent to IEC 801-2)

2.0 RELATED PLANS AND PROCEDURES

TN0401	Master Test Plan
TP0401	Integration (Setup and Checkout) Procedure
TP0402	Operability Test Procedure
TP0403	Prudency Test Procedure
TP0404	Environmental Stress Test Procedure
VV0414	Master Configuration List

50044-10 Wyle Test Procedure for Electromagnetic Interference Testing on a HFC-6000 Control System

2.0 SUPPORT DOCUMENTATION

700715-00 Test Specimen I/O Wiring Schematic
700907-01 Schematic Wiring Diagram, TSAP
700907-02 Schematic Wiring Diagram, Single Loop Controller
700909-01 Controller Arrangement Diagram
700910-01 Card Layout, Class Q Safety-Related USNRC Test Racks
700912-01 System Assembly Drawings
700916-01 Power Distribution, TSAP Configuration
700916-02 Power Distribution, Single Loop Configuration

2.0 HFC INTERNAL STANDARDS AND PROCEDURES

QPP 5.1 Review and Approval of Quality Documents
WI-ENG-003 Configuration Management
WI-ENG-205 Develop Software/Firmware Test Procedure

2.0 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

CSM	Control Switch Module
EUT	Equipment Under Test (See Test Specimen)
HAS	Historical Archiving System
HPAT	HFC Plant Automated Tester
M/A	Manual/Automatic
MCL	Master Configuration List
SOE	Sequence of Events
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TSAP	Test System Application Program

3.0 TEST PREREQUISITES

The following paragraphs provide detailed requirements for setup and performance of the ESD test. Wyle Laboratories test personnel will be responsible for installing the Test Specimen in the test chamber and for applying the ESD test pulses to individual components under test. HFC test personnel will be responsible for controlling functional operation of the Test Specimen and for detecting any failure during test.

3.0 EQUIPMENT REQUIRED

A detailed listing of hardware and software components of the Test Specimen are provided in Attachment A of TN0401, Master Test Plan for the Control System Qualification Project. Detailed requirements for component interconnection of the equipment are provided by the engineering drawings listed in paragraph 2.3. Detailed requirements

for arranging Test Specimen components are provided by paragraph 3.3 of this document and in Wyle Test Procedure 50044-10 Appendix I. HFC test procedures TP0402 and TP0403 provide a list of the test equipment required to run the Operability and Prudency tests. The Wyle test procedure lists all test equipment to be supplied by Wyle Laboratories. Additional test equipment that HFC personnel will require during execution of this test is as follows:

- Fluke 187 Multimeter or equivalent

3.1.1 Test Facility Requirements

Wyle Laboratories will be responsible for supplying the ESD test signal generator and test chamber that complies with requirements of IEC 1000-4-2.

The test facility shall provide the following climatic environment:

- Ambient temperature between 15° C and 35° C
- Relative humidity between 30% and 60%
- Atmospheric pressure between 860 mbar and 1060 mbar

3.1 TEST PERSONNEL

The ESD test will be conducted at Wyle Laboratories. One or more qualified test engineers supplied by Wyle will mount the Test Specimen in the test chamber and apply ESD test pulses to specified points of the equipment. A qualified test engineer from HFC will oversee setup of the Test Specimen, conduct all functional tests, and certify all test records produced during the test period.

3.1 RED-LINE POLICY

The HFC policy for entering red-line corrections into a test procedure are presented in paragraph 2.6 of TN0401. Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.1 EQUIPMENT SETUP

The Test Specimen consists of several modular chassis, a power supply rack, a flat panel display, CSMs and M/A stations for simulated control loops, communication hardware, and mechanical support structures in the form of an open frame. The Test Specimen will be initially received and configured prior to performing an environmental stress test (HFC test procedure TP0404). Following completion of the environmental stress test, the Test Specimen will be transported with minimal disassembly and reconfigured at the test chamber for the next test to be conducted. The following steps outline general setup requirements for the ESD tests. The procedure is based on the following presumptions:

- Test Specimen components (panels and chassis) are transported to the ESD test chamber without disassembly from their mechanical support structures.
- The mechanical support structures will be installed inside the test chamber, and the HPAT and monitoring equipment will be located outside the test chamber.
- System configuration will consist merely of reconnecting electrical, communication, and power cables.
- If equipment setup was accomplished for a previous test in the same test chamber, repetition of this setup procedure will not be necessary, except for inspecting the equipment to detect and correct any physical damage that might have been caused by previous tests (steps 3, 10, and 11).

Sign off each step as it is executed, and then sign final verification after setup is satisfactorily completed.

Validation that hardware setup is complete: _____
Name/date

3.1 PRECAUTIONS

The ESD test pulse consists of a high voltage spark discharge. Direct contact with this discharge could result in severe injury to personnel. All test personnel shall observe applicable safety precautions while the test signal is being applied.

4.0 TEST SEQUENCE

4.0 PRE TEST

After completing equipment setup, the following pre test shall be conducted to verify that the equipment is fully operational. Initial each step as it is executed.

Validation that pretest is complete: _____

Name/Date

4.0 ESD TEST EXECUTION

4.1.1 General Criteria

The following items summarize the general methods for test pulse application listed in IEC 1000-4-2 Paragraph 8.3.1:

- Discharges shall be applied only to those surfaces or components that are normally accessible during system operation. This includes all exterior surfaces of the HFC-6000 chassis and the front panels of the switch modules and M/A stations.

- Discharges shall be applied only to those components that are normally accessed by the customer during operation. However, because ESD warnings have been issued for all circuit cards, no discharge shall be applied directly to internal components.

- Internal components of the switch modules or M/A stations are not accessible during normal use. Accordingly, no discharge shall be applied to these units with their protective case removed.

- The test voltage shall be increased from minimum up to the test level in order to determine the failure threshold. The final voltage shall not exceed 8 kV for direct contact discharges or 15 kV for air discharges. (Refer to Wyle Test Procedure 50044-10 Appendix I.)

- The test shall be conducted using single discharges with the most sensitive polarity selected. A minimum of 10 discharges shall be applied to preselected points with at least a 1-second interval between successive discharges.

- The ESD generator shall be held perpendicular to the surface to which the discharge is being applied. The tip of the electrode shall be brought up to the surface as rapidly as possible without causing damage to the electrode. The return cable from the discharge generator shall be kept at least 0.2 m from the component under test while the discharge is being applied.

- The HPAT will log the static TSAP I/O points (TP0404 Table 1 and Table 2) during ESD testing to detect disruption of controlled outputs, and communication error counters will be monitored to detect disruption of data transfers.

Table 1 lists the specific points to be exposed to the ESD test discharge and identifies the type of discharge to be used for each. Paragraph 4.2.2 describes the test sequence for HFC personnel while the ESD pulses are being applied.

Table 1. ESD Test Points

Component	Location	Discharge Type
		Contact
		Contact
		Contact
		Contact
		Air
		Air
		Air
		Contact
		Contact
		Air
		Air
		Air
		Air
		Air
		Air
		Air
		Air

Table 1. ESD Test Points (Cont)

Component	Location	Discharge Type
		Contact
		Contact
		Contact
		Contact
		Air
		Air
		Contact
		Contact
		Contact
		Contact
		Air

4.1.2 HFC Test Procedure

All ESD discharges will be applied in accordance with Wyle Test Procedure 50044-10 Appendix I. HFC personnel shall perform the following steps while the ESD test is in progress.

4.1.3 Post Test

After applying discharges to all locations listed in Table 1, run a comprehensive post test as follows.

5.0 ACCEPTANCE CRITERIA

Overall acceptance criteria for each component subjected to the ESD waveform shall be as follows:

- Application of the ESD test waveform does not disrupt normal operation of the Test Specimen or result in invalid transitions of any I/O channel, as indicated by the static point test log and the communication error counters.

- Failure of one controller will not be considered as a failure condition if the secondary controller takes over primary operation for the redundant pair.

- The Test Specimen performance remains within tolerance limits after exposure to the ESD test waveforms, and indicated by the pre test and post test Operability test results.

Each test record shall distinguish between four different categories of response:

- **Normal performance**. The equipment displays no degradation or deviation from the performance observed before the start of ESD testing.

- **Temporary degradation**. The equipment displays some deviation from performance observed before the start of testing but returns to normal operation without operator intervention.

- **Temporary loss of function**. The equipment displays deviation from performance observed before the start of testing but returns to normal operation following operator intervention or system reset.

- **Permanent degradation**. The system displays loss of function that cannot be restored due to component damage, damage to program software, or loss of data.

6.0 QA RECORDS

The following documentation shall be generated during the environmental test. These documents will be considered QA records and processed in accordance with the Project Quality Plan.

- TP0401 Test Results Record (pretest results)
- Burst of Events Test Results Record (pre test report file)
- Operability Test Results Record (pre test report file)
- Operability Test Results Record (post test report file)
- Completed test procedure signoffs in each of the test procedure documents.
- Completed test result records appended to this document.
- HAS and SOE report files covering the period during the ESD test
- Alarm log file for the period during the ESD test

Test Results Record

Test Plan: TN0401, Attachment H

ESD Test Equipment Log

Test Equipment	Instrument ID	Cal Due Date

Test Reviewer/Date

Test Results Record

Test Plan: TN0401, Attachment H
ESD Tests

CSM HS-183

Item	Description	Signoff
1	Communication link error count record • ICL error count at start of test: _____ • ICL error count at end of test: _____ • C-Link error count at start of test: _____ • C-Link error count at end of test: _____	_____ Test Engineer
2	Processing disruption (alarm/static data/comm. Errors): • Metal mounting plate _____ Time: _____ • Top mounting screw _____ Time: _____ • CSM front plate _____ Time: _____ • Top switch bezel _____ Time: _____ • Top switch lens _____ Time: _____ • Top switch LED sockets _____ Time: _____ • CSM meter lens _____ Time: _____	_____ Test Engineer
3	Describe type of disruption: (1) Temporary Degradation, (2) Temporary loss of function, (3) Permanent Degradation. Record the maximum pulse withstood. • Metal mounting plate _____ Max pulse: _____ • Top mountins screw _____ Max pulse: _____ • CSM front plate _____ Max pulse: _____ • Top switch bezel _____ Max pulse: _____ • Top switch lens _____ Max pulse: _____ • Top switch LED sockets _____ Max pulse: _____ • CSM meter lens _____ Max pulse: _____	_____ Test Engineer

_____
Test Reviewer/Date

Test Results Record

Test Plan: TN0401, Attachment H
ESD Tests

M/A Station FIK-135

Item	Description	Signoff
1	Communication link error count record • ICL error count at start of test: _____ • ICL error count at end of test: _____ • C-Link error count at start of test: _____ • C-Link error count at end of test: _____	_____ Test Engineer
2	Processing disruption (alarm/static data/comm. Errors): • Metal mounting plate _____ Time: _____ • Metal bezel _____ Time: _____ • Top mounting screw _____ Time: _____ • MANUAL switch _____ Time: _____ • Front panel _____ Time: _____	_____ Test Engineer
3	Describe type of disruption: (1) Temporary Degradation, (2) Temporary loss of function, (3) Permanent Degradation. Record maximum pulse withstood. • Metal mounting plate _____ Max pulse: _____ • Metal bezel _____ Max pulse: _____ • Top mounting screw _____ Max pulse: _____ • MANUAL switch _____ Max pulse: _____ • Front panel _____ Max pulse: _____	_____ Test Engineer

_____
Test Reviewer/Date

Test Results Record

Test Plan: TN0401, Attachment H
ESD Tests

Flat Panel Display

Item	Description	Signoff
1	Communication link error count record • ICL error count at start of test: _____ • ICL error count at end of test: _____ • C-Link error count at start of test: _____ • C-Link error count at end of test: _____	_____ Test Engineer
2	Processing disruption (alarm/static data/comm. Errors): • Front screen _____ Time: _____ • Mounting bezel _____ Time: _____ • Communication cable _____ Time: _____ • G key top _____ Time: _____ • Between G and H keys _____ Time: _____ • Trackball _____ Time: _____	_____ Test Engineer
3	Describe type of disruption: (1) Temporary Degradation, (2) Temporary loss of function, (3) Permanent Degradation. Record maximum pulse withstood. • Front screen _____ Max pulse: _____ • Mounting bezel _____ Max pulse: _____ • Communication cable _____ Max pulse: _____ • G key top _____ Max pulse: _____ • Between G and H keys _____ Max pulse: _____ • Trackball _____ Max pulse: _____	_____ Test Engineer

_____
Test Reviewer/Date

Test Results Record

Test Plan: TN0401, Attachment H
ESD Tests

Controller Chassis

Item	Description	Signoff
1	Communication link error count record • ICL error count at start of test: _____ • ICL error count at end of test: _____ • C-Link error count at start of test: _____ • C-Link error count at end of test: _____	_____ Test Engineer
2	Processing disruption (alarm/static data/comm. Errors): • Chassis _____ Time: _____ • Front bezel _____ Time: _____ • SBC06 power switch _____ Time: _____ • FPC06 power switch _____ Time: _____ • DPM switch _____ Time: _____ • C-Link connector _____ Time: _____	_____ Test Engineer
3	Describe type of disruption: (1) Temporary Degradation, (2) Temporary loss of function, (3) Permanent Degradation. Record the maximum pulse withstood. • Chassis _____ Max pulse: _____ • Front bezel _____ Max pulse: _____ • SBC06 power switch _____ Max pulse: _____ • FPC06 power switch _____ Max pulse: _____ • DPM switch _____ Max pulse: _____ • C-Link connector _____ Max pulse: _____	_____ Test Engineer

If pulse produced disruption when applied to more than one board type, record the board types affected.

_____
Test Reviewer/Date

Test Results Record

Test Plan: TN0401, Attachment H
ESD Tests

Expander Chassis

Item	Description	Signoff
1	Communication link error count record • ICL error count at start of test: _____ • ICL error count at end of test: _____ • C-Link error count at start of test: _____ • C-Link error count at end of test: _____	_____ Test Engineer
2	Processing disruption (alarm/static data/comm. Errors): • Chassis _____ Time: _____ • Front bezel _____ Time: _____ • SBC06 power switch _____ Time: _____ • FPC06 power switch _____ Time: _____ • DPM switch _____ Time: _____ • C-Link connector _____ Time: _____	_____ Test Engineer
3	Describe type of disruption: (1) Temporary Degradation, (2) Temporary loss of function, (3) Permanent Degradation. Record the maximum pulse withstood. • Chassis _____ Max pulse: _____ • Front bezel _____ Max pulse: _____ • SBC06 power switch _____ Max pulse: _____ • FPC06 power switch _____ Max pulse: _____ • DPM switch _____ Max pulse: _____ • C-Link connector _____ Max pulse: _____	_____ Test Engineer

If pulse produced disruption when applied to more than one board type, record the board types affected.

_____
Test Reviewer/Date

Test Results Record

Test Plan: TN0401, Attachment H
ESD Tests

Single Loop Chassis

Item	Description	Signoff
1	Communication link error count record • ICL error count at start of test: _____ • ICL error count at end of test: _____ • C-Link error count at start of test: _____ • C-Link error count at end of test: _____	_____ Test Engineer
2	Processing disruption (alarm/static data/comm. Errors): • Chassis _____ Time: _____ • Front bezel _____ Time: _____ • SBC06 power switch _____ Time: _____ • FPC06 power switch _____ Time: _____ • DPM switch _____ Time: _____ • C-Link connector _____ Time: _____	_____ Test Engineer
3	Describe type of disruption: (1) Temporary Degradation, (2) Temporary loss of function, (3) Permanent Degradation. Record the maximum pulse withstood. • Chassis _____ Max pulse: _____ • Front bezel _____ Max pulse: _____ • SBC06 power switch _____ Max pulse: _____ • FPC06 power switch _____ Max pulse: _____ • DPM switch _____ Max pulse: _____ • C-Link connector _____ Max pulse: _____	_____ Test Engineer

If pulse produced disruption when applied to more than one board type, record the board types affected.

_____
Test Reviewer/Date

Test Results Record

Test Plan: TN0401, Attachment H
ESD Tests

Power Supply Chassis

Item	Description	Signoff
1	Communication link error count record • ICL error count at start of test: _____ • ICL error count at end of test: _____ • C-Link error count at start of test: _____ • C-Link error count at end of test: _____	_____ Test Engineer
2	Processing disruption (alarm/static data/comm. Errors): • Chassis _____ Time: _____ • Module A 24 V _____ Time: _____ • Module A 48 V _____ Time: _____ • Single loop bracket _____ Time: _____ • Single loop switch _____ Time: _____	_____ Test Engineer
3	Describe type of disruption: (1) Temporary Degradation, (2) Temporary loss of function, (3) Permanent Degradation. Record the maximum pulse withstood. • Chassis _____ Max pulse: _____ • Module A 24 V _____ Max pulse: _____ • Module A 48 V _____ Max pulse: _____ • Single loop bracket _____ Max pulse: _____ • Single loop switch _____ Max pulse: _____	_____ Test Engineer

_____
Test Reviewer/Date

HF CONTROLS

HFC-6000 Control System

ERD111 - Control System Qualification Program

Burn-in Test Procedure
TP0410

Rev C

NON-PROPRIETARY

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Author/Title Jonathan Taylor

Reviewer/Title Angela Han

Approval/Title Allen Hsu

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4/15/02	0	J Taylor	Preliminary Draft
7/17/03	A	J Taylor	
9/29/03	B	J Taylor	Modify test to execute burn-in prior to starting system integration.
12/6/04	C	J Taylor	SCR 882 – Incorporate red lines after completion of testing

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1.0 PURPOSE AND SCOPE

The circuit card assemblies for HFC-6000 control system (Test Specimen) will be run in a normal operating environment for a minimum period of 352 hours prior to system integration. The purpose of this test is to detect any early-life failures of component circuit cards. The scope of test will include two and a half times the total number of cards required for the complete test specimen. Circuit card assemblies not included in the initial configuration of the test specimen will be reserved as spares to be used as replacements for any card that fails during the subsequent qualification tests.

The following references in the EPRI TR-107330 specification define the content and scope of this test procedure: 5.2.F.

2.0 REFERENCES

2.0 INDUSTRY STANDARDS

This test procedure constitutes part of the prequalification testing for the HFC-6000 control system. These tests have been developed to document the baseline performance of the control system Test Specimen prior to the start of qualification stress testing.

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants

2.0 RELATED PLANS AND PROCEDURES

TN0401	Master Test Plan
VV0414	Master Configuration List

2.0 HFC INTERNAL STANDARDS AND PROCEDURES

QPP 5.1	Review and Approval of Quality Documents
QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-205	Develop Software/Firmware Test Procedure

2.0 REFERENCE DOCUMENTS

700907-01	Schematic Wiring Diagram, TSAP
700909-01	System Arrangement, Controller-FOT Configuration
700916-01	Power Distribution, TSAP Configuration
700916-02	Power Distribution, Single-Loop Configuration

1.5 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

CSM	Control Switch Module
DPM	Dual-Ported Memory
FOT	Fiber-Optics Transmitter
HAS	Historical Archiving System
HIFR	Host Interface Remote
M/A	Manual/Automatic
MCL	Master Configuration List
RH	Relative Humidity
TSAP	Test Application – a synthetic application program to be used for qualification testing.
UPS	Uninterruptable Power Supply

3.0 TEST PREREQUISITES

The following paragraphs define the conditions that must be established and maintained throughout the duration of the burn-in test.

3.0 EQUIPMENT REQUIRED

A detailed listing of hardware and software components of the Test Specimen are provided in Attachment A of TN0401, Master Test Plan for the Control System Qualification Project. The burn-in test will be conducted in a standard 19-inch equipment cabinet equipped with four HFC-6000 card racks and a redundant power supply. Internal power distribution and interconnection of the four racks will conform with 700907-01, Power Distribution.

The following equipment and facilities will be required during performance of this test.

- HFC-6000 test racks composed of one controller rack and one or more expander racks. The racks shall be supplied with +24 and +48 vdc power and interconnected for rack-to-rack communication.

- PC workstation with EWS suite of software installed. The PC workstation shall be connected with the test rack via an FOT and fiber-optic C-Link. HIFR software may be operating directly on this workstation.

- The copy of the Burn-in Test Procedure in hand is a controlled copy of the current revision according to Document Control records.

3.0 EQUIPMENT TO BE TESTED

The following circuit card assemblies will be included in the burn-in test.

Quantity	Module Type	Description

3.0 ENVIRONMENTAL CONDITIONS

The test will be conducted in a mild environment without temperature or humidity stress conditions being imposed. The normal operating environment for the Test Specimen shall be as follows:

Temperature	50° to 104° F
Relative Humidity	7% to 90% noncondensing

1.9 TEST PERSONNEL

The burn-in test will be conducted at the in-house test facility of HFC. All testing and monitoring functions will be conducted by a qualified HFC test engineer.

3.0 EQUIPMENT SETUP

The test will be conducted with redundant controllers installed in the HFC-6000 card racks installed and I/O cards installed in any combination in the remaining slots. The switch and jumper configuration on the I/O cards is not significant for this test. However, the two controller cards should be configured for redundant operation as remote 1. The required switch and jumper arrangement is as follows:

HFC-SBC06 Configuration		
Jumper	**Installed = X**	**Function**
J1	X	Causes main processor to boot from flash memory.
J5		Permits ICL operation when controller is sane and primary.
J8	X	Causes ICL and CPC processors to boot from EPROM.
W2		Not used.
W3		Disables test mode.
W5		Not used.
W6		Disables test mode.
E1		Not used.
E2		Not used.

SW3							
1	2	3	4	5	6	7	8
O	C	O	O	O	O	O	O

HFC-DPM06 Configuration

SW1							
1	2	3	4	5	6	7	8
C	O	O	O	O	O	O	O

SW2							
1	2	3	4	5	6	7	8
C	O	O	O	O	O	O	O

SW4							
1	2	3	4	5	6	7	8
O	C	O	O	C	C	C	O

Prepare the equipment for burn-in test as follows:

4.0

BURN-IN TEST SEQUENCE

The burn-in test requires a minimum period of 352 hours of operation. During that period, all cards under test must remain in a normal operating state. Only those cards that complete the burn-in test satisfactorily will be placed into inventory for subsequent use as part of the HFC-6000 test specimen.

The test engineer shall maintain a separate test record for each card being tested. The test record shall include the following information:

- Card name, part number, serial number, and software ID.
- Card rack and slot designation (if applicable) for burn-in test.
- Data and time burn-in test started.
- Date and time when burn-in test will end successfully.
- Date and time when card was removed from the burn-in test.
- Description of equipment failure (if any).

NOTE

The 352-hour burn-in period is cumulative for each individual card. If power must be removed from the test chassis before the end of the total burn-in period, the test can resume from the point at which it was interrupted.

Failure and removal of individual cards from the test rack before completion of the test period does not invalidate the burn-in test for the remaining cards.

5.0 ACCEPTANCE CRITERIA

Acceptance criteria for successful completion of the burn-in test are as follows:

- The card edge LEDs for each card under test indicate normal operation throughout the entire test interval.

6.0 QA RECORDS

The following QA records shall be generated during this test:

- MCL – The MCL (Master Configuration List) will be generated as a spreadsheet document that will contain the specific identification data for each card included in the Test Specimen and each approved spare. If a card fails during any phase of testing, failure status and the nature of the failure will be recorded in the MCL for that card.

- Test Record for each card tested. A blank test record is appended as Attachment A to this document.

Burn-in Test Results Record **Attachment A**
Test Plan: TN-4-1, Attachment D

Card Name _____ Part No._____ ID _____

Test Bed Rack and Slot _____

Test Summary

Item	Description	Signoff
1	Record date and time burn-in test period started.	_____ Date/Time
2	Record date and time burn-in test period will end successfully.	_____ Date/Time
3	Burn-in test period aborted due to component failure. Failed component identified and rejected.	_____ Test Engineer/date
4	Record date and time burn-in test stopped either following complete 352-hour period was completed or following component failure.	_____ Date/Time

Burn-in Test Log

Item	Description	Signoff
1	Record date and time that normal operation is verified during burn-in test period.	_____ Date/Time
2		_____ Date/Time
3		_____ Date/Time
4		_____ Date/Time
5		_____ Date/Time
6		_____ Date/Time
7		_____ Date/Time
8		_____ Date/Time

_____
Test Reviewer/Date

HF Controls

HF CONTROLS CORPORATION

HFC-6000 Control System

ERD111 – Control System Qualification Project

Isolation Test Procedure

TP0411

Rev C

NON-PROPRIETARY

Effective Date 01-03-05

Author/Title Jonathon Taylor

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Approval/Title Allen Tsu

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Revision History

Date	Revision	Author	Changes
2/03	0	J Taylor	Preliminary Draft
3/6/03	A	J Taylor	Comments incorporated
1/20/04	B	J Taylor	Review comments incorporated; final design configuration included
12/3/04	C0	J Taylor	SCR 882 – Incorporate red lines after completion of tests.

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1.0 PURPOSE AND SCOPE

The HFC-6000 control system (Test Specimen) is designed to operate in a wide variety of industrial applications. The control system hardware may be installed both in an electrical equipment room and at various other locations near the equipment under control. When I/O chassis are physically located in a remote location with respect to the controller hardware, they will be connected to the controller by means of a dedicated fiber-optic communication link. This link will provide the mechanism for ensuring physical and electrical isolation between a Class 1E controller and all non-Class 1E equipment in an installation. This document covers specific testing to demonstrate two categories of isolation:

- Channel-to-channel isolation of I/O ports under ordinary operation
- Class 1E to non-Class 1E isolation.

The following references in the EPRI TR-107330 standard define the content and scope for this test procedure: 4.3.2, 4.3.3, 4.3.4.3.E, 4.3.4.4.E, 4.6.4, 4.6.8, 6.3.6, 8.6.1.C.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

This test procedure has been developed to encompass module-level isolation testing and Class 1E isolation testing for control system equipment as stipulated by the following standards.

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants
ANSI/IEEE 384	Standard Criteria for Independence of Class 1E Equipment and Circuits

2.2 RELATED PLANS AND PROCEDURES

DD0401	Test Specimen Design Description
TN0401	Master Test Plan
TP0401	Integration (Setup and Checkout) Procedure
TP0402	Operability Test Procedure
TP0403	Prudency Test Procedure
TP0404	Environmental Stress Test
VV0414	Master Configuration List
Deleted	

2.3 SUPPORT DOCUMENTATION

700715-00	Test Specimen I/O Wiring Schematic
700907-01	Schematic Wiring Diagram, TSAP
700907-02	Schematic Wiring Diagram, Single Loop Controller
700909-01	Controller Arrangement Diagram
700910-01	Card Layout, Class Q Safety-Related USNRC Test Rack
700912-01	System Assembly Drawings
700916-01	Power Distribution, TSAP Configuration
700916-02	Power Distribution, Single Loop Configuration

2.4 HFC INTERNAL STANDARDS AND PROCEDURES

QPP 5.1	Review and Approval of Quality Documents
WI-ENG-003	Configuration Management
WI-ENG-205	Develop Software/Firmware Test Procedure

2.5 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

2.5.1 Acronyms

AI	Analog Input
AO	Analog Output
CSM	Control Switch Module
DI	Digital Input
DO	Digital Output
HAS	Historical Archiving System
HPAT	HFC Plant Automated Tester
I/O	Input/Output
LAN	Local Area Network
LED	Light Emitting Diode
M/A	Manual/Automatic
MCL	Master Configuration List
RTD	resistance Thermal Detector
TC	Thermocouple
TSAP	Test System Application Program

2.5.2 Definition of Terms

The following list provides a list of terms and acronyms used in this test procedure.

Group A set of input channels that share a common ground. A group may consist of a single channel or any subset of the total number of channels on a particular input card.

Test Specimen HFC-6000 control system components configured for NRC qualification tests.

3.0 TEST PREREQUISITES

The following paragraphs provide detailed requirements for setup and performance of tests to demonstrate normal channel-to-channel isolation of I/O hardware and Class 1E to non-Class 1E isolation. These tests will be conducted at the HFC facilities with HFC personnel applying the test waveforms and monitoring functional operation of the Test Specimen and for detecting any failure during test.

3.1 EQUIPMENT REQUIRED

A detailed listing of hardware and software components of the Test Specimen are provided in Attachment A of TN0401, Master Test Plan for the Control System Qualification Project. Detailed requirements for component interconnection are provided by engineering drawings listed in paragraph 2.3. Detailed requirements for arranging Test Specimen components are provided by paragraph 3.3 of this document. The following equipment and facilities will be required during performance of this test.

- Ac and dc voltage source for generating isolation test signals
- Fluke 187 Multimeter or equivalent
- HP 8116A Function Generator or equivalent
- Tektronix TDS3034 Logic Analyzer or equivalent
- HFC HPAT Automated Tester
- The Test Specimen will require two ac power sources with both sources set to normal operating levels.
- The test environment shall provide a grounding system that conforms with requirements of 700916-01 and 900916-02.
- The test will be conducted in a mild environment. No special conditions of temperature or humidity will be imposed.

3.2 TEST PERSONNEL

Isolation testing will be conducted at HFC. One or more qualified HFC test engineers conduct all functional tests, and certify all test records produced during the test period.

3.3 RED-LINE POLICY

The HFC policy for entering red-line corrections into a test procedure are presented in paragraph 2.6 of TN0401. Such entries may be used to correct errors of content and procedural sequence in test documents or in engineering drawings to prevent disruption of a test in progress.

3.4 CHANNEL-TO-CHANNEL ISOLATION

The following tests cover channel-to-channel isolation tests applicable to each of the individual I/O card types. The primary purpose of these tests is to demonstrate immunity to channel-to-channel interference during a design basis event. The test signals will be applied to I/O channels both in the Class 1E portion of the Test Specimen and to I/O channels in the expansion rack. The general approach to testing will consist of two phases:

- First, selected channels will be subjected to the Class 1E isolation test signal. If the component under test exhibits acceptable isolation from other components within the system, application of additional test signals to that channel type will be bypassed.

- If the component under test does not exhibit acceptable isolation in response to the initial Class 1E test signal, additional testing will be conducted to determine the maximum test signal that can be applied to that type of channel without affecting performance of other portions of the Test Specimen.

3.4.1 Normal Channel-to-Channel Isolation Test Signal

The minimum acceptable level of channel-to-channel isolation for normal operation differs for each card type. A detailed summary of isolation level requirements and acceptance criteria are listed in Table 1. The following list presents the minimum acceptable level of isolation on a channel-to-channel or group-to-group basis.

- ±30 v peak for AI channels on a group basis
- 40 v peak for 24-vdc discrete inputs on a group basis
- 40-vdc for pulse input channels on a group basis
- 600 v peak applied for 30 seconds for 120-vac discrete output channels on a group basis
- 600 vac and 250 vdc applied for 30 seconds for AO channels
- Twice the nominal output voltage for discrete output channels and serial I/O channels on a group basis

3.4.2 Class 1E Isolation Test Signal

This isolation test refers to demonstration of electrical isolation of class 1E control equipment from non-class 1E equipment as well as isolation between different Class 1E channels. The minimum signal levels required for this test will be as follows:

- 600 vac applied for 30 seconds
- 250 vdc applied for 30 seconds

3.5 EQUIPMENT SETUP

The Test Specimen consists of several modular chassis, a power supply rack, a flat panel display, CSMs and M/A stations for simulated control loops, communication hardware, and mechanical support structures in the form of an open frame. The Test Specimen will be initially received at Wyle and configured prior to performing an environmental stress test (HFC test procedure TP0404). Following completion of the environmental stress test, the test specimen will be transported with minimal disassembly and reconfigured at the test chamber for the next test to be conducted. The isolation test will be the last of the qualification tests to be executed at Wyle. The following steps outline general setup requirements for the isolation test. The procedure is based on the following presumptions:

- Test specimen components (panels and chassis) are transported to the test chamber without disassembly from their mechanical support structures.
- The mechanical support structures will be installed inside the test chamber, and the HPAT and monitoring equipment will be located outside the test chamber.
- System configuration will consist merely of reconnecting electrical, communication, and power cables.
- If equipment setup was accomplished for a previous test in the same test chamber, repetition of this setup procedure is not necessary.

Validation that hardware setup is complete: _____
Name/Date

3.6 PRECAUTIONS

Surge testing involves large amplitude voltage and current transient signals that can pose significant risk to personnel and equipment. The following precautions shall be observed throughout execution of the test sequence to avoid injury to personnel and unnecessary damage to equipment.

- Voltage levels used for Class 1E isolation testing are potentially lethal. Only qualified personnel should perform such tests with all applicable safety precautions enforced.

- Catastrophic failure of equipment under test can result in explosion or fire. The test area should be equipped with fire protection equipment as well as hand-held fire extinguishers.

- Test personnel should not monitor the Test Specimen directly while the test signals are being applied.

4.0 SEQUENCE OF TESTING

4.1 PRE TEST

After completing equipment setup, the following pre test shall be conducted to verify that the equipment is fully operational:

4.2 ISOLATION TEST CASES

4.2.1 Class 1E Isolation

The following test cases list the Class 1E to non-Class 1E isolation requirements for each type of I/O channel specified in EPRI TR-107330. A representative channel from each type of I/O module in the Test Specimen will be exposed to the indicated level of test signal(s).

NOTE

All channels of the same type on any particular module are identical. Each test case will be executed by selecting a single representative channel of the indicated hardware type at random.

I/O modules having more than one type of channel on the same hardware assembly shall be subjected to the test signal for both channel types.

1EO1. For current input (4 to 20 mA) AI modules, 600 vac and 250 vdc for 30 seconds each. The following channels will be tested:

1EO2. For RTD input channels, 600 vac and 250 vdc for 30 seconds each. The following channel will tested:

1EO3. For thermocouple input channels, 600 vac and 250 vdc for 30 seconds each. The following channel will be tested:

1EO4. For 120-vac discrete input channels, 600 vac and 250 vdc for 30 seconds each. **Not applicable for this system.**

1EO5. For 125-vdc discrete input channels, 600 vac and 250 vdc for 30 seconds each. **Not applicable for this system.**

1EO6. For 48-vdc discrete input channels, 600 vac and 250 vdc for 30 seconds each. The following channels will be tested:

1EO7. For pulse input channels, 600 vac and 250 vdc for 30 seconds each. The following channel will be tested:

1EO8. For analog output channels, 600 vac and 250 vdc for 30 seconds each. The following channels will be tested:

1EO9. For solid-state ac discrete output channels, 600 vac and 250 vdc for 30 seconds each. The following channel will be tested:

1EO10. For solid-state dc discrete output channels, 600 vac and 250 vdc for 30 seconds each. The following channel will be tested:

1EO11. For serial I/O channels, 600 vac and 250 vdc for 30 seconds each. The following channel will be tested:

1EO12. For relay discrete output channels, 600 vac and 250 vdc for 30 seconds each. The following channel will tested:

4.2.2 Channel-to Channel (Non-Class 1E) Isolation

The following test cases list the minimum channel-to-channel isolation requirement for each type of I/O card as specified in EPRI TR-107330.

NOTE

If the Class 1E test resulted in destructive failure of the channel under test, either the failed module may be replaced, or test the alternate channel may be tested.

ISO1. For current input (4 to 20 mA) AI modules, group-to-group isolation shall be at least ±30 v peak. The following channels will be tested:

ISO2. For RTD input channels, group-to-group isolation shall be at least ±30 v peak.

ISO3. For thermocouple input channels, group-to-group isolation shall be at least ±30 v peak.

ISO4. For 120-vac discrete input channels, group-to-group isolation shall be at least 600 v peak. **Not applicable for this system.**

ISO5. For 125-vdc discrete input channels, group-to-group isolation shall be at least 600 v peak. **Not applicable for this system.**

ISO6. For 48-vdc discrete input channels, group-to-group isolation shall be at least 100 vdc.

ISO7. For pulse input channels, group-to-group isolation shall be at least 40 vdc.

ISO8. For analog output channels, group-to-group. Module-to-module, and module-to-backplane isolation shall be a minimum of 600 vac and 250 vdc applied for 30 seconds.

ISO9. For solid-state 120-ac discrete output channels, group-to-group isolation shall be at least 600 v peak.

ISO10. For solid-state 125-dc discrete output channels, group-to-group isolation shall be at least twice the nominal output voltage (250 vdc).

ISO11. For serial I/O channels, group-to-group isolation shall be at least 300 vdc applied for 30 seconds.

ISO12. For relay discrete output channels, group-to-group isolation shall be at least 600 v peak.

Table 1 provides a summary the test channels, alternate test channels, signal connection points, and points to be monitored for each test case.

Table 1. Summary of Isolation Test Channels

Test Cases	Test Channel		Alternate Channel		Monitor Channel ID
	Channel ID	Cable Contacts	Channel ID	Cable Contacts	
1E01 ISO1					
1E02 ISO2					
1E03 ISO3					
1E06 ISO6					
1E07 ISO7					
1E08 ISO8					

Table 1. Summary of Isolation Test Channels (Cont)

Test Cases	Test Channel		Alternate Channel		Monitor Channel ID
	Channel ID	Cable Contacts	Channel ID	Cable Contacts	
1E09 ISO9					
1E010 ISO10					
1E011 ISO11					
1E012					

4.3 TEST PREPARATION

None of the automated Operability and Prudency tests will be running during execution of the isolation test. However, the SOE and HAS loggers will be used to monitor static points, and the alarm process utility will be used to monitor system operation for failure conditions.

Verification that test preparation is complete: _____
Name/Date

4.4 TEST EXECUTION

The purpose of this test is to determine the level of isolation provided by each I/O channel type in the Test Specimen. The representative I/O channels listed in paragraph 4.2.1 will be subjected to the Class 1E isolation test waveforms **first**. If a channel successfully meets the criteria for Class 1E isolation, no further test will be executed for that channel type. If a channel fails to meet the Class 1E isolation acceptance criteria, the magnitude of the test signal will reduced to the level required for channel-to-channel isolation listed in paragraph 4.2.2. If that channel passes this test, then the magnitude of the test signal will be progressively increased in order to determine the maximum level of isolation that module can provide.

CAUTION

None of the channels selected for test are connected to the HPAT. When applying the test signal, ensure that all other disconnected wires in the harness are held away from the test signal leads. Arcing from the test leads to the I/O harness could result in damage to the HPAT **and** invalidate results of the isolation test.

NOTE

Hot swapping of failed I/O modules is permitted. The failed module and the nature of the failure shall be recorded as part of the test report. The replacement module shall be identified in the Master Configuration List.

5.0 ACCEPTANCE CRITERIA

Overall acceptance criteria for each circuit type to be tested are listed in Table 2.

Table 2. Isolation Test Acceptance Criteria

Test Case	Channel Type	Test Signal	Acceptance Criteria
Normal Channel-to-Channel Isolation (Minimum Acceptable Levels)			
All			No disruption in operation for any other channel on the card or any other module in the chassis occurs.
ISO1	4 to 20 mA AI	±30 v peak group-to-group isolation	No channel other than the one under test changes by more than 0.05%.
ISO2	RTD AI	±30 v peak max group-to-group isolation	No channel other than the one under test changes by more than 0.05%.
ISO3	TC AI	±30 v peak max group-to-group isolation	No channel other than the one under test changes by more than a 0.54° F (0.3° C).
ISO4	120 vac DI	600 v peak group-to-group isolation	No channel other than the one under test exhibits invalid transitions.
ISO5	125 vdc DI	600 v peak group-to-group isolation	No channel other than the one under test exhibits invalid transitions

Table 2. Isolation Test Acceptance Criteria (Cont)

Test Case	Channel Type	Test Signal	Acceptance Criteria
ISO6	48 vdc DI	100 vdc group-to-group isolation	No channel other than the one under test exhibits invalid transitions
ISO7	Pulse Input	40 vdc group-to-group isolation	No channel other than the one under test exhibits invalid transitions
ISO8	AO	600 vac max for 30 sec 250 vdc max for 30 sec	No channel other than the one under test changes by more than 0.05% while the signal is applied.
ISO9	Solid-state 120 vac ac DO	600 v peak group-to-group isolation	No disruption in operation for any other channel on the card occurs.
ISO10	Solid-state dc DO	Twice nominal output voltage group-to-group isolation	No disruption in operation for any other channel on the card occurs
ISO11	Serial channel	300 vdc peak max port-to-port isolation applied for 30 seconds	No disruption in operation for any other channel, the main processor, or any other module occurs
ISO12	Relay DO	600 v peak group-to-group isolation	No disruption in operation for any other channel on the card occurs
Class-1E Isolation			
1EO1	4 to 20 mA AI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1EO2	RTD AI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1EO3	TC AI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1EO4	120 vac DI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1EO5	125 vdc DI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1EO6	48 vdc DI	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1EO7	Pulse Input	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected.
1EO8	AO	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected No other channel on the module under test shall change by more than 0.05%.
1EO9	Solid-state 120 vac ac DO	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected
1EO10	Solid-state dc DO	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected
1EO11	Serial Channel	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected
1EO12	Relay DO	600 vac for 30 sec 250 vdc for 30 sec	No module other than the one subjected to the test signal is affected

6.0 QA RECORDS

The following documentation shall be generated during isolation testing:

- Historical archive database (electronic file)
- Completed portions of TP0411 procedure
- Operability and Prudency test reports (preliminary test).
- Completed TP0411 Test Results Report sheets
- SOE and HAS logger report files during test period.

All electronic files will be transferred to two CDs as soon as practical after completion of the test procedure. The CDs and manually written test data records will be considered QA records and processed in accordance with the Project Quality Plan.

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Tests

Test Equipment	Instrument ID	Cal Due Date

Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E01/ISO1
Channel Under Test: 3,AI,63 (3,AI,62 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E01/ISO1
Channel Under Test: 1,AI,894 (1,AI,885 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E02/ISO2
Channel Under Test: 1,AI,965 (1,AI,964 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E03/ISO3
Channel Under Test: 1,AI,1043 (1,AI,1042 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E06/ISO6
Channel Under Test: 3,DI,32 (3,DI,31 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	Test Engineer
3	Did channel under test experience destructive failure? Describe:	Test Engineer
4	Record approximate time 250 vdc test signal was applied.	Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	Test Engineer
6	Did channel under test experience destructive failure? Describe:	Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	Test Engineer

Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E06/ISO6
Channel Under Test: 1,DI,325 (1,DI,332 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E06/ISO6
Channel Under Test: 1,DI,265 (1,DI,270 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	Test Engineer
3	Did channel under test experience destructive failure? Describe:	Test Engineer
4	Record approximate time 250 vdc test signal was applied.	Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	Test Engineer
6	Did channel under test experience destructive failure? Describe:	Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	Test Engineer

Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E06/ISO6
Channel Under Test: 1,DI,311 (1,DI,308 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	Test Engineer
3	Did channel under test experience destructive failure? Describe:	Test Engineer
4	Record approximate time 250 vdc test signal was applied.	Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	Test Engineer
6	Did channel under test experience destructive failure? Describe:	Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	Test Engineer

Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E07/ISO7
Channel Under Test: 1,AI,1021 (1,AI,1022 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E08/ISO8
Channel Under Test: 3,AO,63 (3,AO,62 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E08/ISO8
Channel Under Test: 1,AO,822 (1,AO,823 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E09/ISO9
Channel Under Test: 1,DO,262 (1,DO,261 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E010/ISO10
Channel Under Test: 1,DO,82 (1,DO,81 alternate)

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E011/ISO11
Channel Under Test: Station 2B (Station 3B)

Item	Description	Signoff
1	Record approximate time 30 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 30 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 30 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 30 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

Test Data Record

Test Plan: TN0401, Attachment H
Isolation Test Case: 1E012/ISO12
Channel Under Test: 3,DO,56

Item	Description	Signoff
1	Record approximate time 600 vac test signal was applied.	_____ Test Engineer
2	Describe disruption, if any, on application of 600 vac test signal.	_____ Test Engineer
3	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
4	Record approximate time 250 vdc test signal was applied.	_____ Test Engineer
5	Describe disruption, if any, on application of 250 vdc test signal.	_____ Test Engineer
6	Did channel under test experience destructive failure? Describe:	_____ Test Engineer
7	If the module failed to meet Class 1E isolation acceptance criteria, record the maximum level of isolation achieved:	_____ Test Engineer

_____
Test Reviewer/Date

HF Controls

HF CONTROLS CORPORATION

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HFC-6000 Control System

ERD111 – Control System Qualification Project

Baseline Testing Summary Report

TS901-000-22

Rev B

Effective Date	10/16/2007
Author/Title	Jon Taylor/Ron Musick
Reviewer/Title	John A. Stevens
Approval/Title	Terrence A. Gerardis

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Date	Revision	Author	Changes
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9/23/04	1	X. Li	Incorporate BOE change
10/12/04	2	X. Li	Incorporate Accuracy, Timer, BOE Changes
10/14/04	2A	J Taylor	Updated coverage for timer, power loss, power interrupt test, SLC BOE waveform, serial failure test, and serial noise test
10/20/04	3	X. Li	Incorporate review changes
11/09/04	3a	X. Li	Revise DO operability section
11/10/04	3b	Steve Yang	Updated Section 4
11/11/04	A	Steve Yang	Released
10/16/07	B	Jon Taylor Ron Musick	Revised Scope of Topical Report

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1.0 PURPOSE

HFC is qualifying its HFC-6000 control system for safety-related applications in U.S. nuclear power plants. The approach taken for this qualification effort is based on the guidance provided in EPRI-TR-107330, Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants.

This document identifies the specific HFC-6000 components that have been subjected to qualification testing, the equipment configurations, test equipment, test setup, test system application programs used, acceptance criteria and the base line testing performed.

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2.0 SCOPE

The scope of this document is to:

1. Identify the specific HFC-6000 components that have been subjected to qualification testing.
2. Define the baseline test configuration that combines modules of the Test Specimen and the Test System Application Program (TSAP). The performance of a set of base line acceptance tests on this configuration constitutes the system integration testing for the Test Specimen.
3. Define the base line testing which was conducted on the baseline test configuration prior to performance of the qualification test program.
4. Define the baseline HFC-6000 Control System operability and prudency, test results, applicable accuracies, and time responses against which qualification test results will be evaluated.
5. Evaluation of post qualification Operability and Prudency test results, against base line testing results.

3.0 REFERENCES AND ACRONYMS

3.1 REFERENCES

EPRI TR-107330 Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants

TN0401 HFC-6000 Control Systems, ERD111- Control System Qualification Project Master Test Plan

ATP0402 HFC-6000 Control Systems, ERD111- Control System Qualification Application Software Objects Test Plan

TP0410 HFC-6000 Control Systems, ERD111- Control System Qualification Project Burn-in Test Procedure

TP0401 HFC-6000 Control Systems, ERD111- Control System Qualification Project Integration (Set-up and Check-out) Procedure

TP0402 HFC-6000 Control Systems, ERD111- Control System Qualification Project Operability Test procedure

TP403 HFC-6000 Control Systems, ERD111- Control System Qualification Project Prudency Test procedure
VV0404 Master Configuration List, BURN IN PCBS.xls, Excel Spreadsheet Prepared by David Briner, ERD111 Post Seismic CD
DD0401 Test Specimen Design Description
TS901-000-30 Summary Report for Burn-in Test, Setup and Checkout Test, TSAP Validation Test.
TR001-000-02 Application Software Objects Test Report

3.2 ACRONYMS

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ASO	Application Software Objects
BOE	Burst of Events
CPC	Communication Protocol Controller
CR	Condition Report
CRC	Cyclical Redundancy Check
DCS	Distributed Control System
DDB	Dynamic Database
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
EWS	Engineering Workstation
HAS	Historical Archiving System
HFC	HF Controls
HIFR	Host Interface Remote
HMI	Human Machine Interface
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
I/O	Input/Output
JCRT	Java CRT Workstation
LAN	Local Area Network
M/A	Manual/Automatic
MCL	Master Configuration List
MTP	Master Test Plan
OIS	Operator Interface Station
OBE	Operating Basis Earthquake
PCB	Printed Circuit Board
PCC	Peripheral Communication Controller
PROM	Programmable Read Only Memory
RFI	Radio Frequency Interference
RRS	Required Response Spectrum.
RTD	Resistance Temperature Detector
SOE	Sequence of Events
SSE	Safe Shutdown Earthquake
TOD	Time of Day
TSAP	Test System Application Program
UCP	Universal Communication Protocol

4.0 HFC-6000 Components for Qualification Testing

4.1 HFC-6000 System Overview

HF Controls provides integrated digital systems to support nuclear power plant safety, control, and information functions. The HFC-6000 digital safety systems meet regulatory requirements for safety system quality, qualification, redundancy, fault tolerance, deterministic performance, isolation and independence. The overall architecture of HF Controls distributed safety, control, and information systems forms the basis to meet the requirements for nuclear power plant applications.

The HFC-6000 safety system is designed to operate with either single or multiple control units in each channel. The primary CPU Module (CPUM) in a unit is the system controller (HFC-SBC06), which supports the execution of control logic programs and I/O scans. All three functions are handled by dedicated 64/32 bit microprocessors. A redundant configuration of system controllers includes two HFC-SBC06 controller boards and one HFC-DPM06 dual ported memory board.

The Figure 4-1 illustrates the general arrangement of the HFC-6000 control system as it was configured for qualification testing. A subset of the components pictured in the illustration has been selected for presentation to the NRC for generic qualification. Major functions of these components are as follows:

- The CPU Module (CPUM) provides status monitoring and operational control for the control system hardware, and it also executes the specific application program.
- The flat panel display, Control Switch Modules, and M/A stations illustrated in the diagram represent the operator interface for a control system. The C-Link, PC workstations, and other support equipment illustrate utilities for offline programming and maintenance functions. These elements were included with the test configuration but are excluded from consideration for generic qualification.
- Input/Output Modules (IOM) provide the hardware interface to controlled field devices and are implemented by different types of I/O printed circuit boards. Each I/O board has a redundant serial interface to the controllers. This serial interface employs a proprietary poll-response inter-communication link (ICL) protocol for communication between the I/O boards and the system controllers. With a redundant controller configuration, each ICL is connected with one system controller. The I/O boards can be accessed locally or remotely.
- The Power Supply Module (PSM) represents the redundant rack mounted power supply set. This hot swappable redundant power supply provides 24 vdc for both controller and I/O modules.

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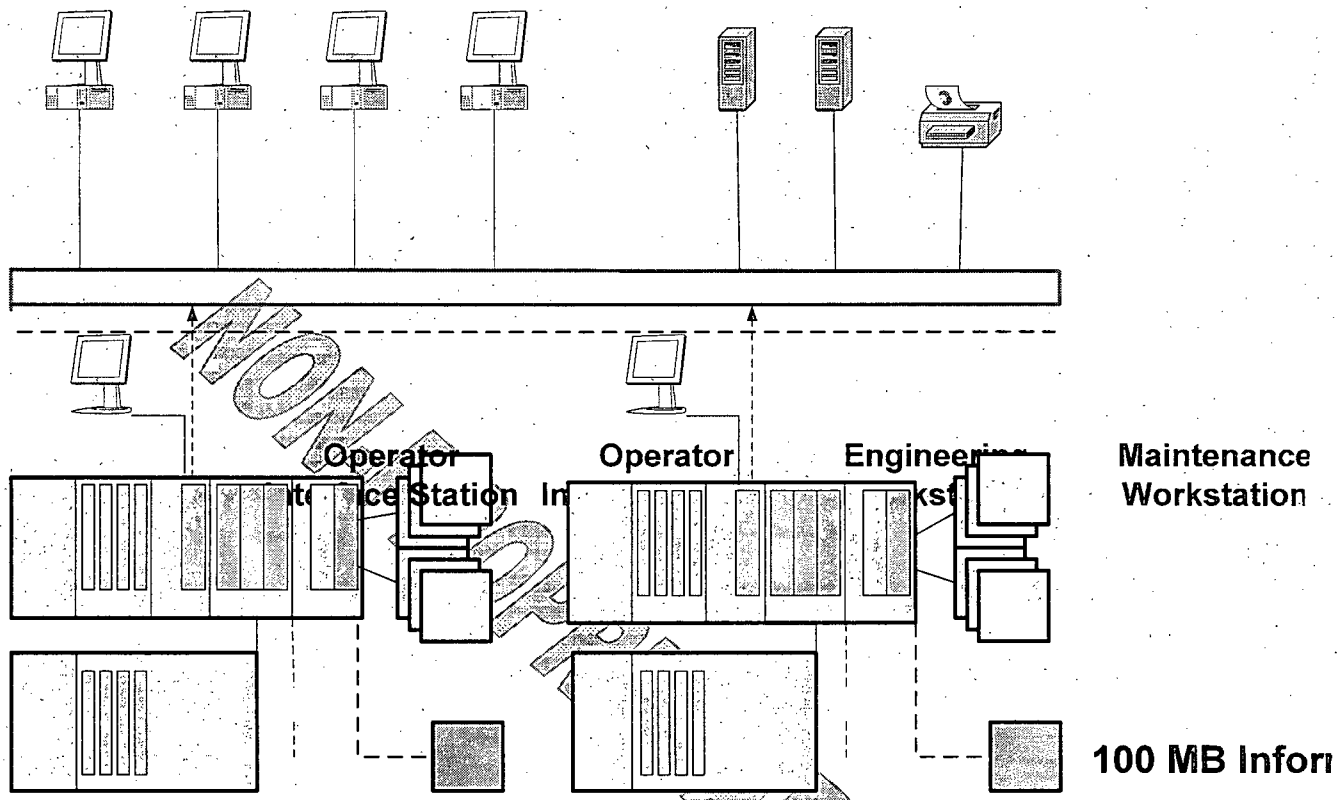

Figure 4-1. HFC-6000 System Arrangement Diagram.

4.2 HFC-6000 Components for Qualification Testing

This section describes the hardware components that have been used for qualification test. They include various I/O, communication, power supply and controller modules and chassis. The software components for qualification testing will be described in the software qualification.

4.2.1 System Controller Module

The HFC-6000 distributed control system provides plant monitoring and control functions with monitoring and control capabilities spread over multiple remote control units. The HFC-SBC06 System Controller is the primary module used for implementing plant safety functions. The HFC-SBC06 System Controller module is positioned in the HFC-6000 system to interface with the I/O modules, which provide the signal-level interface to the equipment and devices under monitoring or control.

Descriptions of the functional requirements of the HFC-SBC06 System Controller module and HFC-DPM06 Dual Ported Memory module, from an external perspective, are provided in the HFC-6000 Product Line Requirements Specification, RS901-000-01. Detail level descriptions of the HFC-SBC06 and HFC-DPM06 are contained in the HFC-SBC06-DPM06 System Controller Module Detailed Design Specification, DS901-000-01.

The principal functions supervised by the HFC-SBC06 System Controller are:

- Redundant controller operation, system diagnostic, failure detection and failover;
- Execution of application control programs for the specific control logic;
- Communication with I/O modules through ICL (Intercommunication Link);

The HFC-SBC06 System Controller module is designed to operate in a redundant controller configuration consisted of two HFC-SBC06 modules and one HFC-DPM06 module. The primary HFC-SBC06 performs the main functions of the system controller while the secondary HFC-SBC06 operates as a "hot spare" for the primary HFC-SBC06. Controller modes are determined at controller module start-up, with the first HFC-SBC06 to complete initialization becoming primary. The other HFC-SBC06 module defaults to secondary. The HFC-DPM06 module provides shared memory between the redundant HFC-SBC06 modules that keeps the secondary HFC-SBC06 module updated with a current copy of the primary running status. This mechanism ensures a smooth transition from one controller to the other in the event of failover.

The Maintenance Failover function permits manual verification of the working status of both the primary and the Secondary controller to make sure it will be able to take over control in the event that the Primary controller fails.

The HFC-6000 safety system provides a communication interface to support transfer of data and status between system components. The communication interface connects the HFC-SBC06 to the Intercommunication Link (ICL). The ICL is an RS-485 serial network connecting the HFC-SBC06 to its I/O modules or HFC-PCC06 interface controller modules. The ICL network implements a deterministic master/slave communication protocol.

The HFC-SBC06 module contains three separate microprocessor sections including the SYS microprocessor section and the ICL microprocessor section. The C-Link microprocessor section is also included on this module, but it is not part of this qualification program. Each microprocessor section is dedicated to a specific set of functional responsibilities, with the SYS processor being the main processor for the whole controller and the other two acting as subordinate processors. The SYS processor section is implemented with an Intel Pentium processor. It executes application programs, coordinates operation of the other two processors, and monitors their collective status. The ICL processor section is based on an Intel 386 processor. It supports communication with the I/O modules or HFC-PCC06 module through the ICL.

The three independent microprocessors use Public Memory to communicate and coordinate their individual operations. Public Memory is a shared onboard RAM section that may be accessed by the three microprocessors over a Shared Bus. The three microprocessors connect to the Public Memory address and data bus (Shared Bus) on the module, with each microprocessor's access to Public Memory controlled by a bus arbitration circuit. Public Memory houses data that is shared by the microprocessors and data that must be transferred between the microprocessors.

In addition to common access to Public Memory, each microprocessor is configured with a Private Memory composed of separate PROM, Flash, and RAM sections. A set of system firmware is

installed in the PROM or flash memory. Private Memory is accessible only to the microprocessor in that circuit section.

There is an onboard Sanity circuit for detection of controller failure. The SANE status and PRI (Primary) status signals from the Sanity circuit are routed to the Failover circuit on the HFC-DPM06 module. The Failover circuit supports failover on failure of the primary controller as well as maintenance failover.

A dual-ported memory array on the HFC-DPM06 module is accessible to both the Primary and Secondary controllers. The three processors connect to the DPM address and data bus, with each processor's access to the DPM controlled by a bus arbitration circuit. Software arrangements coordinate Read and Write to the DPM by the Primary and Secondary controllers to avoid conflicts or corrupted data.

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4.2.2 Input /Output Modules

The HFC-6000 I/O modules provide signal-level interface to the equipment and devices which are being monitored or controlled. The major functions performed by the HFC-6000 I/O Module are:

- Measuring input signals or setting output signals
- Communication with HFC-SBC06 system controller through the ICL to report digital input images or receive digital output images;
- Self-diagnostic functions

An I/O module having output channels receives digital images for its output channels from an HFC-SBC06 system controller at regular intervals and uses this data to control each output point. An I/O module with input channels converts the input signal for each channel into a digital image, and sends these images to the HFC-SBC06 system controller at regular intervals.

Each HFC-6000 I/O Module has a similar architecture as depicted by Figure 4-2.

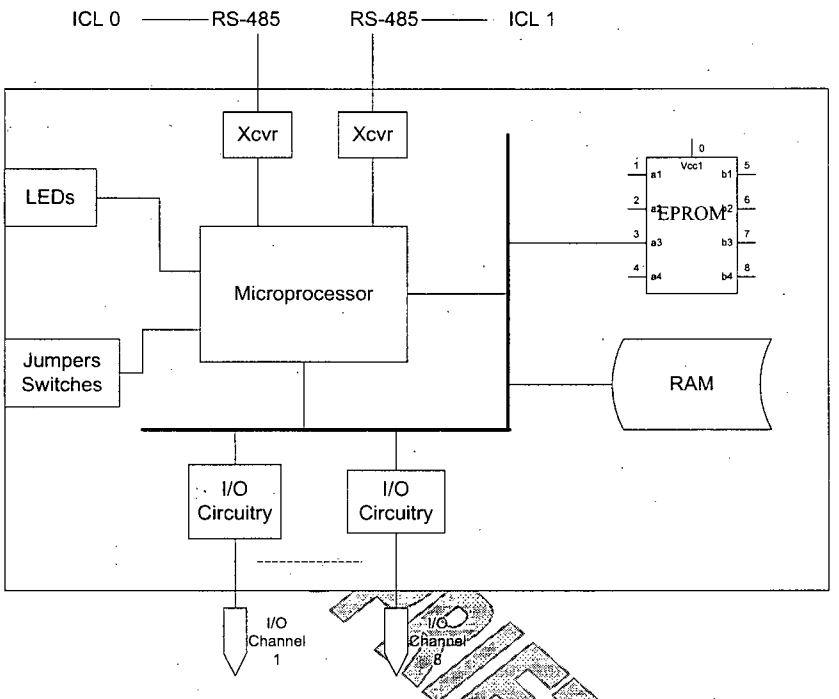

Figure 4-2. HFC I/O Module Architecture.

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Common features of all HFC-6000 I/O modules are as follows:

- An onboard 16-bit Intel 80C188EB microprocessor
- Two banks of memory:
- Upper memory provides up to 64K of 8-bit words in PROM for functional program code storage.
- Lower memory provides 32K of 8-bit words in RAM for temporary storage of data being processed, such as I/O images, ICL messages, diagnostic data, etc.
- Two independent RS-485 serial interfaces for communication with the HFC-SBC06 system controller
- Onboard LEDs to provide a visual indication of module status
- Onboard jumpers and switches for configuration options
- I/O interfaces
- Each I/O point includes circuitry to measure its input signal or to control its output signal. Each analog output point includes a 16 bit digital analog converter (DAC) in its I/O circuitry to convert digital images into analog signals. Analog input points are configured with a single 16-bit analog/digital converter (ADC) per module to convert analog signals into digital images.
- An onboard dc-to-dc converter that provides regulated +5-vdc logic power
- An onboard switch that permits manual reset of the microprocessor
- Two card-edge connectors (P1 and P2) mate with corresponding backplane connectors. Signal assignments for P1 are identical for all I/O modules, so that any module can be

inserted in any I/O slot of an HFC-6000 chassis. The P2 connector for each I/O module uses the same hardware, but signal assignments are unique for each module type.

- Onboard watchdog timer triggers reset on response to microprocessor timeout condition.

Each HFC-6000 I/O module supports communication with the HFC-SBC06 controller via the ICL as shown in Figure 4-3. Each I/O module has two transceivers that are connected to the redundant ICL channels. Each ICL is connected to a separate HFC-SBC06 controller. The I/O module identifies which link has active communication rights during initialization and monitors that link as primary. Throughout normal operation of the HFC-6000 control system, one HFC-SBC06 controller functions as primary and polls the I/O modules. The messages carried over the ICL network are either normal data update or diagnostics messages.

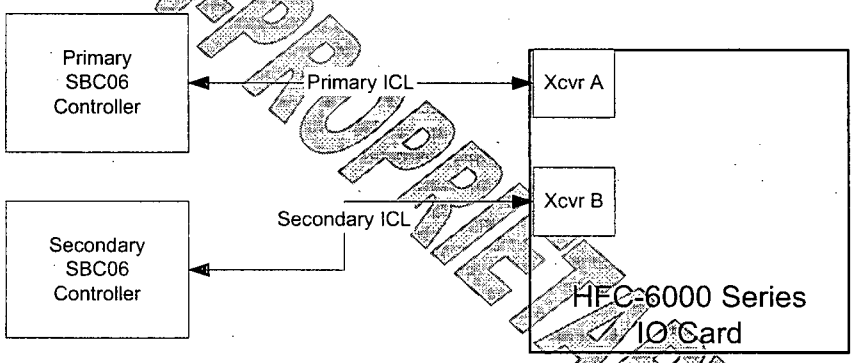

Figure 4-3. ICL Communication Architecture.

NON-PROPRIETARY

Table 4-1 provides a list of the current HFC-6000 I/O Module types and a description of the I/O channels for each module type. Some module types have a combination of input and output points.

Table 4-1. List of HFC-6000 I/O Modules.

Name	I/O Channels
DO8J	8 channel digital relay output
DI16I	16 channels digital input
DC33	2 channel 120-vac digital output and 12 digital input
DC34	2 channel 125-vdc digital output and 12 digital input
AI16F	16 channels analog input
AO8F	8 channel analog output
AI8M	8 channel 100Ω RTD input
AI4K	4 channel pulse input

The overall architectural design of standard HFC-6000 I/O modules and its standard functions are provided by document MS901-000-02, "HFC-6000 I/O Module Design Specification." The design descriptions of the common software modules of I/O modules are described in document DS901-000-02, "HFC-6000 I/O Module Detailed Design Specification."

4.2.1.1 Relay Output Module

The HFC-DO8J assembly is an eight-channel relay digital output module. It receives the images of its digital outputs from an HFC-SBC06 system controller at regular intervals, and uses this data to set the on/off status of each output relay. This module is controlled by an onboard 80C188EB microprocessor. The ON/OFF images for the eight channels are held in memory as a single byte of data.

4.2.1.2 Digital Input Module

The HFC-DI16I assembly is a 16-channel digital input module. The assembly operates as a standard DI module in an HFC-6000 control system. The HFC-DI16I module reads the digital data of its input channels at regular intervals and stores the image in onboard RAM. This module is controlled by an onboard 80C188EB microprocessor.

4.2.1.3 Digital Controller Module

The HFC-DC33 is a special purpose, multi-channel I/O buffer module designed for nuclear power plant applications. It is used by the HFC-6000 for control, interrogation, and monitoring of field devices. This buffer is specifically designed to meet the unique control requirements of a dual-coil Motor Operated Valve (MOV) starter. Typical applications include controlling dual coil motor starters while monitoring coil continuity, overloads and valve position.

This module is controlled by an onboard 80C188EB microprocessor and provides 12 general-purpose DI channels, two 120-vac DO channels, and onboard status sensors, including two coil continuity inputs, one power monitor input, and a separate status monitor for the three excitation voltage lines.

4.2.1.4 Digital Control of Breakers Module

The HFC-DC34 is a multi-channel Input/Output (I/O) buffer printed circuit module (PCB). It is used for control, interrogation, and monitoring of field devices in an HFC-6000 control system. Typical applications include monitoring Electrically Operated Breakers (EOB) for overloads. This module is designed to provide the specific combination of digital I/O channels needed to control motor starter or switchgear field equipment.

This module is controlled by an onboard 80C188EB microprocessor and provides 12 general-purpose DI channels, two 125-vdc DO channels, and onboard status sensors including two coil continuity inputs, two power monitor inputs, and a separate status monitor for the three excitation voltage lines.

NON-PROPRIETARY

4.2.1.5 Analog Input Module

The HFC-AI16F module operates as a standard AI module in an HFC-6000 control system. This module is controlled by an onboard 8C188EB microprocessor and provides an interface for up to 16 analog field inputs. It samples the AI readings, performs analog to digital conversion for each channel at regular intervals, and stores the resulting digital images in onboard RAM prior to transfers to the controller.

4.2.1.6 Analog Output Module

The HFC-AO8F module operates as the standard AO module in an HFC-6000 control system. It receives digital images from the system controller and performs digital to analog conversion for each channel at regular intervals. The HFC-SBC06 controller initiates communication with a configured HFC-AO8F module during its regular scan cycles while the HFC-AO8F module receives the current digital image for all output channels from the poll message and returns current status.

4.2.1.7 RTD Input Module

The HFC-AI8M Resistance Temperature Detector (RTD) printed circuit module (PCB) is an input-conditioning device for an HFC-6000 control system. This module receives the voltage images of its isolated analog inputs from external resistors and presents them for conversion into a digital count value image for each channel at regular time intervals.

4.2.1.8 Pulse Input Module

The HFC-AI4K module provides four input channels for processing pulse signals from field equipment. The four channels are organized as two pairs, and configuration parameters for each pair can be entered by switches that are accessible at the front bezel. These configuration parameters permit selection of rate or accumulate mode. When the rate mode is selected for a particular pair of channels, hardware counters produce a count value that represents the frequency of the input signal. When the accumulate mode is selected, the counter increments with each input pulse, and the microprocessor scales the input based on the pre-scaled value. In either case the count image for each channel is stored in local memory and reported to the ICL controller during each regular I/O scan.

4.2.3 Communication Modules

The HFC 6000 System being qualified includes an intrinsic ICL communication network. Communication support is integrated into the system controller and I/O modules. Several communication modules are required for the implementation of this communication network. The following figure depicts the configuration. The following subsections provide descriptions of this communication network and modules.

NON-PROPRIETARY

5.0 HFC-6000 TEST SETUP DESCRIPTION

5.1 Test System Hardware Configuration

Figure 5-1 illustrates the overall layout of the Test Specimen and indicates the boundary between the safety-related and non-safety-related portions of the system. Only the safety related portion of the system was subjected to the qualification tests described in the Qualification System Master Test Plan, TN0401.

The Test Specimen was composed of four 19-inch card chassis mounted on an open cabinet frame to simulate cabinet installation. These card chassis were configured to encompass every feature of the HFC-6000 architecture to be qualified. One of these chassis was configured with redundant controller hardware, the system power supply, and I/O modules linked directly to the controller. Two of the remaining card chassis illustrated in Figure 5-1 were linked directly to the controller as expander I/O chassis. The remaining card chassis (labeled local I/O in Figure 5-1) contained I/O cards linked to the controller via a fiber-optic communication link. The overall configuration simulated the hardware arrangement of a redundant remote controller that is physically located in an equipment room and a local I/O chassis that is physically located near the equipment under control.

The controller hardware supported one serial communication link being qualified:

- A redundant Intercommunication Link (ICL) enables direct connection with up to a total of 53 I/O cards (or a maximum of 848 I/O points), which may be located in the same chassis as the controller, an expander chassis, a local I/O chassis, or a combination of local and remote chassis. When configured to communicate with a local I/O chassis, a redundant fiber-optic link serves as the communication medium to ensure electrical isolation from non-class 1E equipment.

The controller hardware supported a second serial communication link not being qualified, but part of the test system:

- A redundant Communication Link (Test C-Link) provides the communication gateway with external workstations. This network is an Ethernet LAN that employs the TCP/IP protocol to enable data transfer between the controller and PC workstations. When more than one controller is connected to the C-Link, each controller acquires link mastership for a fixed interval in a round-robin sequence. While a particular controller is link master, it can broadcast its accumulated data to the link. Between successive masterships, a controller can receive both broadcast data and specifically addressed UCP messages from the link.

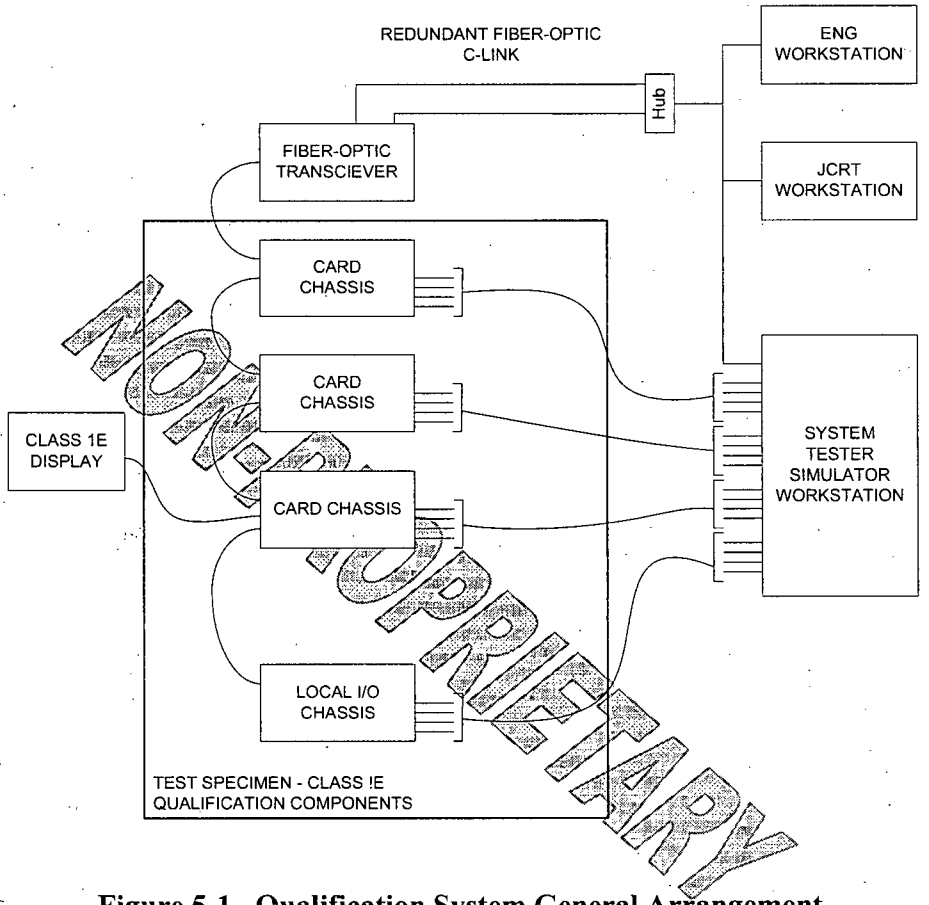

Figure 5-1. Qualification System General Arrangement.

5.1.1 Modular Card Chassis

5.1.2 Circuit Card Hardware

The qualification system included at least one of every module type to be qualified. All hardware designs were based on an architecture that HFC has employed over many years. The complete set

of hardware modules currently planned for the HFC-6000 product line is listed in Table 5-1; however, not all of the modules are included in the Qualification Report as stated in the notes to the table. Additional card types beyond those listed may be added following the initial qualification.

Table 5-1. HFC-6000 Product Line Family

Designation	Function
HFC-ILR06	I/O Link Repeater/Terminator
HFC-PSR06*	Rack-Mounted Power Supply
HFC-PSM	Chassis-Mounted Modular Power Supply
HFC-SBC06	Master Controller
HFC-AC36E** HFC-AC38*	4-Point AI and 4-Point AO Card (4- to 20-mA) 4-Point AI and 4-Point AO Card (0- to 10-v)
HFC-AI16E* HFC-AI16F	16-Point Analog Input Card (0- to 10-v) 16-Point Analog Input Card (4- to 20 Ma)
HFC-AI8L**	Eight-Point Thermocouple Input Card
HFC-AI8M	Eight-Point RTD Input Card, 100-ohm
HFC-AO8E* HFC-AO8F	Eight-Point Analog Output Card (0- to 10-v) Eight-Point Analog Output Card (4- to 20 mA)
HFC-AI4K	Four-Point Pulse Input Card
HFC-DC33	Special Function Card – Dual 120 vac Output, 12-Point Discrete Input with Dual Coil Continuity Monitor
HFC-DC34	Special Function Card – Dual 125 vdc Output, 12-Point Discrete Input with Dual Coil Continuity Monitor
HFC-DC35Q*	Special Function Card – One 120 vac Output, 12-Point Discrete Input with Single Coil Continuity Monitor
HFC-DI8A* HFC-DI8B* HFC-DI8G*	8-Point High-Level (120-vac) Discrete Input Card 8-Point High-Level (125-vdc) Discrete Input Card 8-Point High-Level (250-vdc) Discrete Input Card
HFC-DI16I	16-Point High Level (48-vdc) Discrete Input Card with SOE Function
HFC-DO8J	8-Point Relay (dry contact) Output Card
HFC-DPM06	Dual Ported Memory
HFC-CSM-0N**	Control Switch Module Assembly (-0N designates number of switches)
HFC-BPC01-08**	8-inch Single Loop Controller Backplane
HFC-BPC01-19	19-inch Controller Backplane
HFC-BPE01-19	19-inch Expanded Controller Backplane
HFC-FPC06**	Front Panel Controller Card
HFC-PCC06**	Peripheral Communication Controller Card

Designation	Function
HFC-MA**	Hardware M/A Station Assembly
ECS-B232**	Fiber-optic Repeater PCB Board

* Cards under development (Not in qualification system)
** Cards undergo qualification process but will be dropped from consideration.

5.1.3 Redundant Controller Arrangement

A redundant HFC-6000 controller is composed of two HFC-SBC06 controllers and an HFC-DPM06 (Dual-Ported Memory) card which are installed in adjacent card slots. The two controllers have identical system software and the same application program installed. DIP switches on the controllers and on the DPM card provides the mechanism for setting hardware configuration options and for selecting the software mode of operation. The DPM provides the hardware interface for passing current system status from the primary controller to the secondary controller.

Each of the two HFC-SBC06 controller cards has three onboard processors, and each processor has its own private memory array and system-level software. Each processor performs a dedicated function and operates independently of the other two:

- Master Processor. The master processor is a Pentium processor. This processor provides overall system control and runs the application program.

- PCC Processor. The Peripheral Communication Controller processor controls two ICL links consisting of traces on the backplane. The processors are capable of communicating with up to 53 I/O cards mounted in this and expander racks.

- CPC Processor. The Communication Protocol Controller processor controls two token-ring links that constitute the interface of the controller with the Test C-Link. This Test C-Link function is not included in the scope of the qualification report.

Following initial application of power or following hardware reset, both controllers begin operation by running a set of diagnostic routines. The first controller to complete all internal diagnostic tests successfully becomes primary, and the other controller becomes secondary. Throughout subsequent operation, the primary controller runs all I/O scans, control status broadcasts to the C-Link, process the application program, and copy system status to the DPM array. The secondary copies system status from DPM to its local public memory, listen to activity on the C-Link, and process the application program, but it does not run regular I/O scans or broadcast data to the C-Link. If the primary controller ceases normal operation, an internal watchdog detects the failure and triggers failover to the secondary. Because the copy of system status in public memory of the secondary is at most 1 second old at the time failover occurs, the secondary is capable of taking over primary control with minimum disruption to the process.

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5.1.4 I/O Cards Assemblies

The hardware design for each I/O card assembly includes identical hardware for redundant slave ICL ports, microprocessor, and LED status displays; only the specific hardware interface with the field equipment differs from one module to the next. Similarly, the onboard software is composed of common modules for initialization and ICL support. However, the software for each card type provides a scan algorithm that provides specific support for the hardware interface on that card. The following naming convention has been established to permit unique identification of each I/O card type in the HFC-6000 product line.

Name Format HFC – (a)(b)(c)(d) N

HFC Identifies the product line series

(a) Identifies basic card types
A – Analog
D – Digital
C – Special Function

(b) Identifies primary card function
I – Input
O – Output
C – Combination of both input and output

(c) Identifies number of channels on the card
4 – Four channels total
8 – Eight channels total
16 – 16 channels total
32 – 32 channels total
33 – Two 120-vac output channels, 12 48-vdc DI channels
34 – Two 125-vdc output channels, 12 48-vdc DI channels
35 – One 120-vac output channel, 12 48-vdc DI channels
36 – Four AI channels, four AO channels (4- to 20-mA)
38 – Four AI channels, four AO channels (0- to 10-v)

(d) Identifies specific signal characteristics

A – 120 vac
B – 125 vdc
C – 24 vdc
D – 48 vdc
E – 0 to 10 v (analog)
F – 4 to 20 mA (analog)
G – 250 vdc
H – 220 vdc
I – SOE DI
J – Form C Relay Contact
K – Pulse
L – Thermocouple
M – 100-ohm RTD
N – 200-ohm RTD
P – 2000-ohm potentiometer input
Q – Special Function

N Designates assemblies that have been dedicated for nuclear projects

5.1.5 Test C-Link Hardware

The Test C-Link is a redundant, bi-directional fiber-optic data highway that enables data transfer throughout the system. The Test C-Link was not qualified as part of the qualification program. However, it was used as part of the qualification test system. The Test C-Link for the qualification system consisted of two nodes that enabled communication with the PC workstations via a HIFR.

5.1.6 ICL Hardware

The physical arrangement of the ICL (intercommunication link) takes two forms. When a master controller is connected to one or more expansion I/O racks in the same cabinet, the serial ICL traces of the controller chassis are connected with corresponding traces on the expansion racks. When the controller is connected to a local I/O cabinet, a fiber-optic transmitter/receiver pair provides the ICL interface between the main controller and the I/O chassis. The method used to communicate with the local I/O cards is identical to that used with the cards in the master controller and expander I/O card files. As a result, the same PCC processor can communicate with both local and remote I/O cards in any combination.

5.1.7 Digital Logic Control

Operator interface for digital logic control functions normally consists of one or more discrete inputs and one or more LED outputs. The Test Specimen included three forms of HMI for digital logic: the CSM, the flat panel display, and interactive graphics of the JCRT. However, these HMI interfaces are not included in the scope of the qualification report.

NON-PROPRIETARY

5.1.8 Analog Logic Control

The flat panel display, M/A stations, and JCRT graphic meterface displays provided the HMI for analog control functions. However, these HMI interfaces are not part of the Test Specimen being qualified and are not included in the scope of the qualification report. Data received during the scan cycles is stored in local memory, and that data is transferred to the main controller over the ICL during the regular I/O scans of the HFC-SBC06.

5.1.9 Test Specimen System Power Distribution

The HFC-6000 product line includes both a separate power supply rack and modular power supplies that can be installed in individual logic chassis. Test Specimen had a power supply rack to provide operating power to the four racks that represent the main portion of the controller hardware. The power supply rack produces redundant +24 and +48-vdc outputs. The +24-vdc power lines were diode auctioneered on each card in the chassis to produce onboard logic power. The +48-vdc power was used to supply excitation voltage for external relay contacts and for field transducers. The +24-vdc power was referenced to a common instrument ground; a DIP switch option permits selection of either isolated or common configurations for the excitation power on an individual IO card basis. When isolated excitation voltage is used, the system should include provisions to detect ground fault conditions.

5.2 Test Equipment (Not Being Qualified)

The qualification system included a non-class 1E workstation, an automated tester, C-Link communication and an isolator hub that are all not part of the Test Specimen. That workstation had the HFC suite of software for the EWS and JCRT PC workstations installed. The EWS and JCRT PC workstations constitute a standard software installation for most HFC control systems and provide comprehensive utilities and tools for status monitoring, system control, testing, and maintenance of the overall control system installation. An HFC Plant Automated Tester (HPAT) automated tester workstation was also be included as part of the overall test configuration for the Test Specimen. This assembly is a special unit designed to support automated testing of HFC control systems. Both the PC workstation and the HPAT unit were connected to the C-Link through the isolator hub.

5.2.1 EWS Workstation

The EWS workstation is a suite of software utilities that support the development and maintenance of application software, system maintenance, diagnostics, and fault isolation for HFC control systems. This workstation is a standard part of HFC control system installations, but it normally operates offline from the overall system. This workstation provides the utilities needed to perform the following functions:

- Build the database for the qualification system.
- Build the TSAP.
- Perform code-level test and verification of the TSAP.

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- Install and configure the TSAP in the qualification system controller.
- Perform system-tuning functions for the TSAP.
- Build the application program for the HPAT remote controller.
- Monitor and record system performance during the qualification tests.

5.2.2 JCRT Workstation

The JCRT workstation is the normal operator interface for HFC control systems. It is equipped with a suite of software utilities that provide interactive graphics, alarm displays, overall system status displays, historical logging, and data archiving functions. The interactive graphics displays provide software controls for entering command inputs for both digital and analog control loops with or without the touch screen function. Such command inputs can operate in parallel with physical control modules, or they can be used to replace existing mechanical controls. The operator can choose to have multiple displays operating simultaneously or to vector from one display to another based on status messages that appear on screen. In addition, the historical archiving software provides the capability of generating a regular log of system point values. The resulting database provides an archive that can be used for generating the plant operation reports required by the NRC. In the Test Specimen, the JCRT provided a superset of the functions provided by the flat panel display, but it could not be used to modify system tuning parameters.

5.2.3 System Tester/Simulator

The system tester/simulator consisted of a PC workstation, a non-redundant ECS-1200 controller, and an ECS-1200 I/O rack with the ECS-series card types needed to exercise the I/O channels installed in the Test Specimen. The PC workstation had automated test software installed along with the complete suite of EWS and JCRT software utilities. The ECS controller had an application program installed to provide specific simulations for the field hardware controlled by the TSAP. This arrangement supported all phases of dynamic testing, including functional verification of system operation and simulation of failure conditions.

5.3 Test Specimen (Equipment Being Qualified)

The Master Configuration List is a software test log that contains a listing of specific modules, component serial numbers, and cables that were included in Test Specimen. The component serial numbers are included in this listing to ensure traceability of all modules included in the Test Specimen. In the event of a module failure during testing, the MCL is updated to identify the replacement module. A record of the module that failed and the nature of the failure are included in the report for the test affected, and a summary of all failures included as part of the final test report.

The detailed configuration and arrangement of the Test Specimen is provided by engineering drawings, which are listed in the MCL. The MCL also provides a comprehensive listing of the software installed on each circuit card, including I/O module processing software, PCC processor software, CPC processor software, main processor software, and the TSAP. The workstations and test equipment required to conduct the tests are not part of the Test Specimen, but the software installed on the PCs is identified in the MCL. In addition, the HPAT application program, which will run the automated tests for the Test Specimen, is controlled and listed in the MCL.

6.0 BASELINE TESTING

Baseline testing/pre qualification Operability and Prudency testing was performed on the HFC-6000 Test Specimen to obtain measured test results to be used to define and/or calculate the applicable accuracy and time response baselines against which qualification test results will be compared.

In addition to the Baseline testing performed to establish the HFC-6000 performance baseline, a set of "one-time" tests was also performed in the development of the test configuration control system. These tests are generally described as the following: 1) Application Objects Test 2) Burn-in Test and 3) System Setup and Checkout tests (References 3.3, 3.4 and 3.5).

Figure 6-1 shows the basic testing sequence that was generally followed for baseline/pre qualification and qualification testing.

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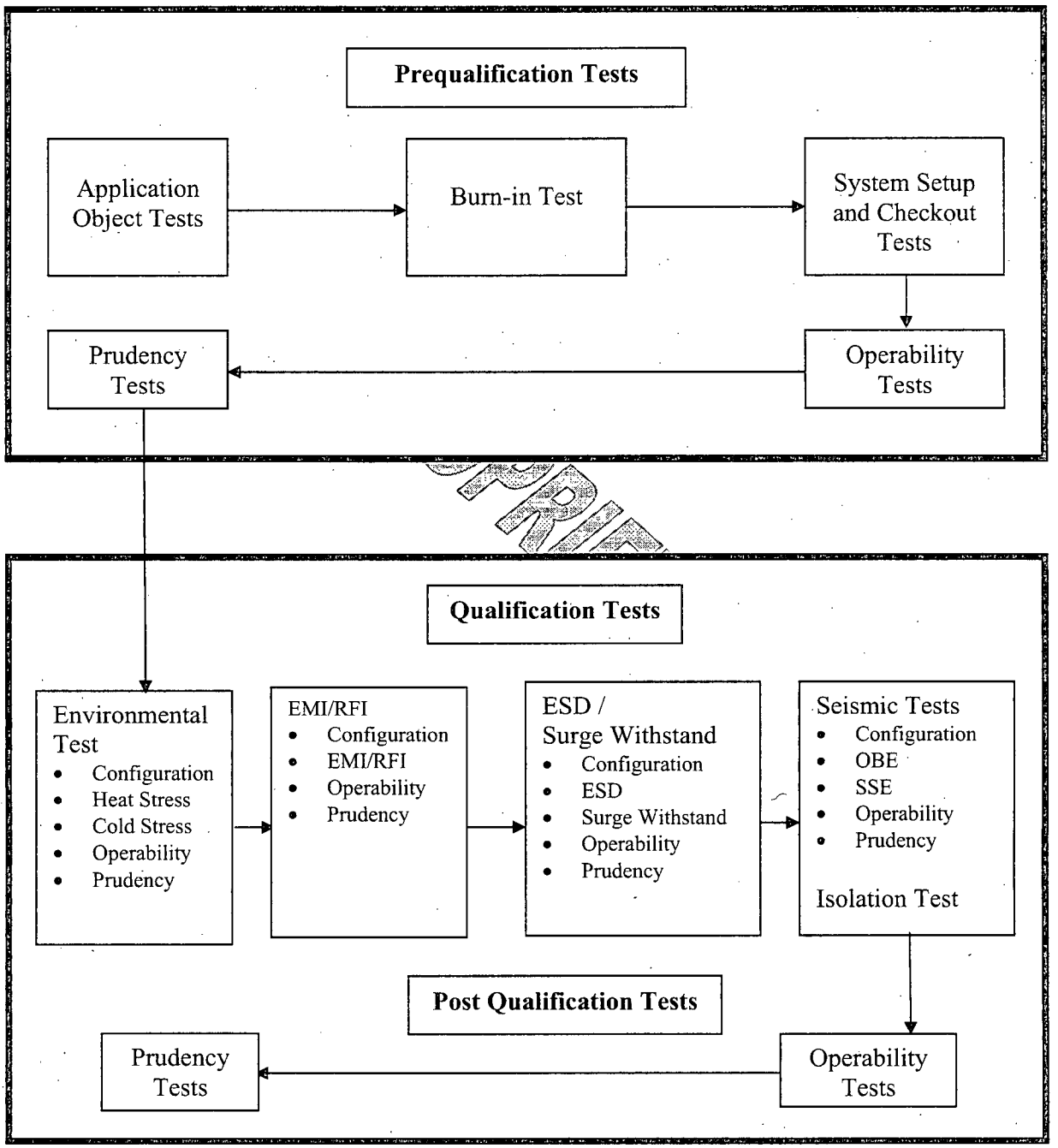

Figure 6-1. Overall Test Sequence.

6.1 APPLICATION OBJECT TEST (ATP0402, Rev. A)

6.1.1 Purpose and Scope of Application Software Object Test

The Application Object Test provides comprehensive testing of software objects that have a direct impact on the application code or that can be accessed by application code while it is running on the HFC-SBC06 controller. Such objects are designated as application software objects (ASO). The scope of testing included both functional operation and exception conditions for the following ASOs:

- Processing algorithms (called CQ4 blocks) used for analog control functions.
- Mathematical operations executed directly by the application code without calling a CQ4 block.
- Boolean operations executed directly by the application code.

Peer-to-peer communication used in HFC Universal Communication Protocol (UCP) is part of the system software. Thus, it was not tested in ASO testing. The major software tool – Equation Compiler, is tested separately. During compilation of the application object, the compiler generates error reports if any errors occur. Any compiling errors will be identified before the object code to be executed in the controller is generated. Only the object code successfully compiled is downloaded via the UCP into the controller to be executed. During the download of the object code, the memory for the object code is write/read protected until the download action is finished. Therefore, the software for the compiler tool, peer-to-peer communication or UCP communication, and the execution of the object code are fully isolated. The successful testing of the ASO verifies the peer-to-peer communication and the compiler communication were successfully achieved during the test setup.

The following software objects or functions were excluded from the scope of testing because they are both external to the application code and inaccessible to it:

- Initialization and internal status monitoring functions of the controller.
- Runtime diagnostics and component fault detection.
- The regular scan of I/O points, including M/A stations and CSMs.
- Dynamic Database (DDB) broadcast of data over the C-link.

The Application Software Objects Test Plan, ATP0402 (Reference Section 3.1), was developed following references in the EPRI TR-107330 specification (Reference Section 3.1).

6.1.2 Results

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6.1.3 Anomalies

6.2 BURN-IN TEST (TP0410, Rev. B)

The circuit card assemblies for HFC-6000 control system (Test Specimen) were run in a normal operating environment for a minimum period of 352 hours prior to system integration. The purpose of this test was to detect any early-life failures of component circuit cards. The scope of the test included two and a half times the total number of cards required for the complete Test Specimen. Circuit card assemblies not included in the initial configuration of the Test Specimen were reserved as spares to be used as replacements for any card that failed during the subsequent qualification tests.

6.2.1 Results

6.2.2 Anomalies

No anomalies were reported for the modules that passed the burn-in test.

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6.3 SYSTEM SETUP AND CHECKOUT TESTS (TP0401, Rev. A)

The System Setup and Checkout Tests were performed to verify that the project specified hardware, wiring and communication cabling had been installed and that communication had been established over each communication link, prior to the TSAP Validation Test.

Included in the scope of this testing were the following activities:

- Verify that all project specified equipment / hardware had been received, functionally tested, and set-up per project documents
- Verify correct software was installed in Test Specimen, HPAT, HPAT PC Workstation
- Verify correct installation for all interconnection wiring.
- Verify that C-Link communication had been established
- Verify that all HFC-6000 PCBs (Printed Circuit Boards) I/Os were functional and communicating with SBC-06 controller
- Verify functional operation of TSAP and automated tests

- This test procedure constitutes part of the prequalification testing for the HFC-6000 control system. These tests were developed to document the baseline performance of the control system Test Specimen prior to the start of the qualification testing.

6.3.1 Results

6.3.2 Anomalies

6.3.3 Summary

All assemblies met the acceptance criteria for the set-up and check-out test upon completion of the procedure.

6.4 OPERABILITY TEST (TP0402, Rev. B)

A specially configured HFC-6000 Test Specimen was configured for generic qualification as a commercially available control system for safety-related applications in nuclear power plants. The following set of Operability tests was performed following completion of the tests described in Sections 6.1, 6.2, and 6.3.

The purpose of these tests was to establish the performance baseline for the system. This performance baseline was then used as the basis for evaluating system performance during and/or following each of the qualification tests required by the EPRI standard.

- **Accuracy Test** - This test developed a baseline to compare against the accuracy and linearity of the analog I/O modules observed during the qualification tests.
- **Response Time Test** – This test measured the response time for discrete and analog inputs.
- **Discrete Input Operability Test** - This test verified the capability of discrete input channels to detect a transition in the input signal being monitored.
- **Discrete Output Operability Test** - This test verified the capability of discrete output channels to operate reliably within its specified loading conditions.
- **Communication Operability Test** – This test verified reliable data transfer over the ICL, C-Link, and serial interfaces with external devices - Control Switch Module (CSM) and M/A stations. Although the C-Link, CSM, and M/A stations are not part of the Qualification Report, they were present during the testing.
- **Timer Test** – This test developed the baseline for the timer function accessible to the TSAP.
- **Failover Operability Test** – This test demonstrated correct operation of the failover function.

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- **Loss of Power Test** – This test demonstrated correct response of all I/O channels to loss of source power followed by reapplication of power to the system.

- **Power Interruption Test** – This test demonstrated the capability of the power modules to sustain system operation during a temporary (40-ms transient) power interruption.

- **Power Quality Tolerance Test** – This test was developed to demonstrate the capability of the Test Specimen to continue normal operation over a range of source power voltages and frequencies. The Power Quality Tolerance test was not a regular part of the Operability tests; it was required during the high temperature phase of the environmental test and after the completion of the seismic test only.

6.4.1 Results

6.4.2 Anomalies

Test Specimen performed as expected except for the following anomalies:

- Manual 4-20 ma AI Channel Accuracy (See Appendix Section A.2)

- Type 100 Ohm RTD Card Accuracy (See Appendix Section A.4)

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- Manual Pulse Input Card (See Appendix Section A.5)

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- Automated Analog Accuracy Test (See Appendix Section A.6)

- Digital Response Time Measurement (See Appendix Section A.7)

- TSAP Analog Response Time Test (See Appendix Section A.8)

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- Discrete Output Operability Test (See Appendix Section A.10)

- Communication Operability Test (See Appendix Section A.11)

- Timer Test (See Appendix Section A.12)

- Failover Operability Test (See Appendix Section A.13)

- Power Interrupt Test (See Appendix A.15)

NON-PROPRIETARY

6.4.3 Summary

The Pre Qualification Operability Tests, as supplemented by the Post-Qualification Operability tests, provided baseline data for comparison to the results of many of the same tests performed during and after the qualification tests.

6.5 PRUDENCY TEST (TP0403, Rev. C)

An HFC-6000 Test Specimen was configured for generic qualification as a commercially available control system for safety-related applications in nuclear power plants. The Prudency testing consisted of the following set of tests.

The entire Prudency test was conducted during the pre qualification phase of testing to establish a performance base line. During subsequent qualification tests, the Burst of Events (BOE) and the other tests were repeated at various points to identify any performance degradation from the performance baseline.

- **Burst of Events Test** - This test consisted of the simultaneous activation of a significant proportion of input and output channels in accordance with EPRI TR-107330 paragraph 5.4.A. This test was automated and was typically run as a continuous background operation for selected qualification tests.

- **Serial Port Failure Test** – The Test Specimen has two redundant serial communication links. For each redundant link, this test imposed three simulated failures on one cable at a time: link open, transmit line shorted to ground, and transmit line shorted to receive line.

- **Serial Port Noise Test** - This test introduced a white noise signal on each of the serial links one port at a time.

- **Fault Simulation Test** – This test covered introduction of a simulated failure condition to trigger failover from the primary to the secondary controller. The intent of this test was covered by the Failover Operability Test (TP0402), and has not been duplicated in this test.

- Throughout the Prudency test, the ac power source for the Test Specimen was set to supply input power at 90 vac and 57 Hz.

6.5.1 Results

6.5.2 Anomalies

Overall performance of the Test Specimen met expectations except for the following anomalies:

- Digital Input/Output BOE Test (See Appendix Section B.2)

- Analog BOE Test (See Appendix Section B.3)

- Serial Port Failure Tests – ICL Failure (See Appendix Section B.4)

NON-PROPRIETARY

- Serial Port Noise Test (See Appendix Section B.4)

NON-PROPRIETARY

6.5.3 Summary

The Pre Qualification Prudency Tests, as supplemented by the Post-Qualification Prudency tests, provided baseline data for comparison to the results of many of the same tests performed during and after the qualification tests.

7.0 ACCEPTANCE CRITERIA

The initial acceptance criteria are defined in the specific Operability and Prudency Test Procedures (References 3.6 and 3.7). The acceptance criteria as stated in the test procedures were developed based on EPRI TR-107330, and the HFC design specifications and they did not specifically consider the HFC-6000 equipment configuration or HPAT Test System, and their interactions and limitations. This is consistent with section 5.0 of the Operability Test Procedure (Reference 3.6) which states "A preliminary set of results obtained during the prequalification phase of testing will establish baseline performance characteristics for the Test Specimen and TSAP. Subsequent performance of the operability tests during the qualification tests will disclose any deterioration from the baseline performance caused by the environmental stress conditions."

The test results achieved during "baseline testing" are generally the standard against which the other tests (environmental, seismic, etc.) will be evaluated. Those tests will focus only on any "changes" in system performance attributable to the test environment.

Where equipment performance did not meet the acceptance criteria initially defined in the specific Operability and Prudency Test Procedures, evaluations were performed to determine the reason (e.g. procedural, test setup, improper specification, equipment limitations, etc.) and the findings and analysis are included in the detailed baseline test sections of this report (Appendices A & B).

8.0 SUMMARY

A specific HFC-6000 control system (Test Specimen) was configured for generic qualification as a commercially available control system for safety-related applications in nuclear power plants. A prescribed set of Operability and Prudency tests was performed following completion of application object testing, burn-in, system integration, and TSAP validation.

The results of those tests, as supplemented by certain post-qualification tests, established the baseline for the system. This performance baseline was then used for evaluating the system performance during and/or following each of the qualification tests.

NON-PROPRIETARY

HFC-6000 Control System

ERD111 – Control System Qualification Project

Baseline Testing Summary Report
TS901-000-22

Rev B

NON-PROPRIETARY

APPENDIX A

OPERABILITY TESTS

A.1 General

The purpose of this attachment is to document the results of the Accuracy Tests in Section 4.1 of the Operability Test Procedure TP0402, Rev. B. The acceptance criteria against which the Operability Tests results are evaluated are provided in Section 5.0 of the test procedure.

A.2 Manual 4-20 mA AI Channel Accuracy (Section 4.1.1)

The purpose of this test was to provide a manually conducted baseline accuracy determination for the Analog Input (AI) channel under test in the Test Specimen. The test configuration is shown in Figure A.2-1. This baseline data will be compared against data from the same test performed at the completion of the qualification program to determine the degree to which system performance was impacted by being stressed up to and even beyond its normal end of life state.

A static step analog algorithm (Figure A.2-2) was generated by HPAT logic and fed into an Analog Output (AO) channel in the HPAT, which was wired to a 4-20 mA AI channel under test in TSAP as shown in Figure A.2-1. Table A.2-1 shows the analysis of the test data and the calculated accuracy. Column 2 (labeled "Input to AI Card") represents the AO signal as measured with a multimeter; this signal is fed directly into the AI channel under test. Column 3 (labeled "Output from AI Card") is the digital data taken at the output of the AI card converted to a 4-20 mA scale. Column 4 shows the resultant accuracy of the AI channel under test calculated as 100%*(Column 3 – Column 2)/20. It should be noted that the AI card contains a moving average algorithm which acts as a filter on the output of this card.

NON-PROPRIETARY

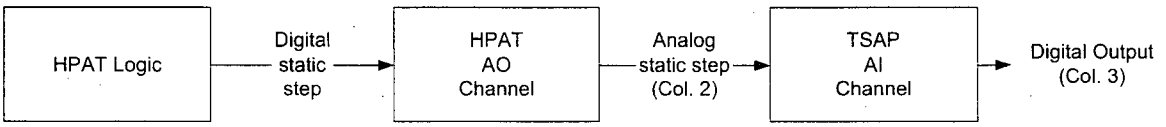


Figure A.2-1. AI Channel Test Configuration.

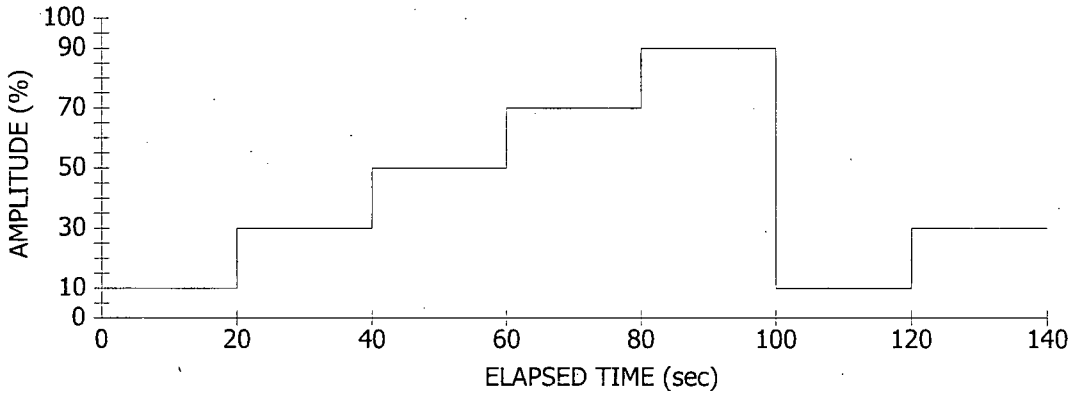


Figure A.2-2. Algorithm for 4- to 20 mA Analog Channel Accuracy Test.

Table A.2-1. AI Channel Accuracy Data.

Static Step (4-20 mA equivalent)	Input to AI Card	Output from AI Card	AI Channel Accuracy (% of difference)
10%			
30%			
50%			
70%			
90%			

Table A.2-2. AI Channel Re-Calibration Data AI16F Board, Serial # 31030007, Channel 1.

Static Step (4-20 mA equivalent)	Input to AI Card (mA)	Output from AI Card (mA)	AI Channel Accuracy (% of difference)
10%			
30%			
50%			
70%			
90%			

A.3 4-20 mA AO Channel Accuracy (Section 4.1.2)

The purpose of this test was to provide a manually conducted accuracy determination for the Analog Output (AO) channel under test in the Test Specimen. The test configuration is shown in Figure A.3-1. This baseline data will be compared against data from the same test performed at the completion of the qualification program to demonstrate that system performance was not unacceptably impacted by being stressed up to and even beyond its normal end of life state.

A static step analog algorithm (Figure A.2-2) was generated by TSAP logic and fed into an AO channel under test. Table A.3-1 shows the analysis of test data and calculation of accuracy for a 4-20 mA AO channel. Column 2 (labeled "Input to AO Card") represents the expected value for the AO channel under test. Column 3 (labeled "Output from AO Card") represents the analog 4 – 20 mA signal as measured with a multi-meter. Column 4 shows the resultant accuracy of the AO channel under test calculated as the absolute value of 100%*(Column 3 – Column 2)/20.

The accuracy measurement taken as described shows that the AO card accuracy was well within the 0.1% acceptance criterion for the module.

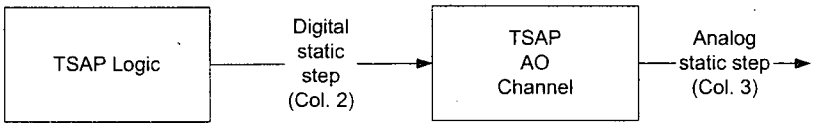


Figure A.3-1. AO Channel Test Configuration.

Table A.3-1. AO Channel Accuracy Data.

Static Step (4-20 mA equivalent)	Input to AO Card (mA)	Output from AO Card (mA)	AO Card Accuracy (% of difference)
10%			

Static Step (4-20 mA equivalent)	Input to AO Card (mA)	Output from AO Card (mA)	AO Card Accuracy (% of difference)
30%			
50%			
70%			
90%			

Non-Proprietary

A.4 Type 100 Ohm RTD Card Accuracy (Section 4.1.4)

The purpose of this test was to provide a manually conducted accuracy determination for the RTD Input channels under test in the Test Specimen. See Figure A.4-1 for a schematic diagram of the test configuration. The RTD card under test is calibrated from 0 °C to 700 °C. A Beta Calibrator ("RTD Input Device") which is accurate to within ±0.25 °C is used to generate temperature input to three of the eight RTD input channels (channels 1, 2, & 8). The actual readings from the card are compared with the inputs to calculate accuracy for each RTD channel. This baseline data will be compared against data from the same test performed at the completion of the qualification program to demonstrate that system performance was not unacceptably impacted by the environmental stress conditions.

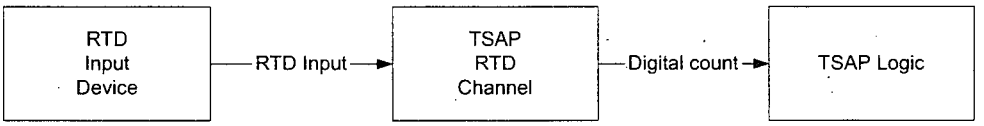


Figure A.4-1. RTD Channel Test Configuration.

Table A.4-1. RTD Channel Accuracy Data.

Input (°C)	Channel 1		Channel 2		Channel 8	
	Output (°C)	Accuracy (% of difference)	Output (°C)	Accuracy (% of difference)	Output (°C)	Accuracy (% of difference)
70						
210						
350						
490						
630						

Proprietary

A.5 Manual Pulse Input Card (Section 4.1.5)

The purpose of this test was to provide a manually conducted accuracy determination for the Pulse Input Card under test in the Test Specimen. This baseline data will be compared against data from the same test performed at the completion of the qualification program to demonstrate that system performance was not unacceptably impacted by being stressed up to and even beyond its normal end of life state.

NON-PROPRIETARY

Table A.5-1. Pulse Input Channel Accumulate Mode Accuracy Data.

Input Frequency		Total Count at 300 Seconds				
			Prescaler = 1		Prescaler = 100	
Nominal (Hz)	Measured (Hz)	Expected Count	Measured Count	Accuracy (%)	Measured Count	Accuracy (%)
50	49.73					
5,000	4,981					
10,000	10,005					
15,000	14,980					
19,500	19,450					

NON-PROPRIETARY

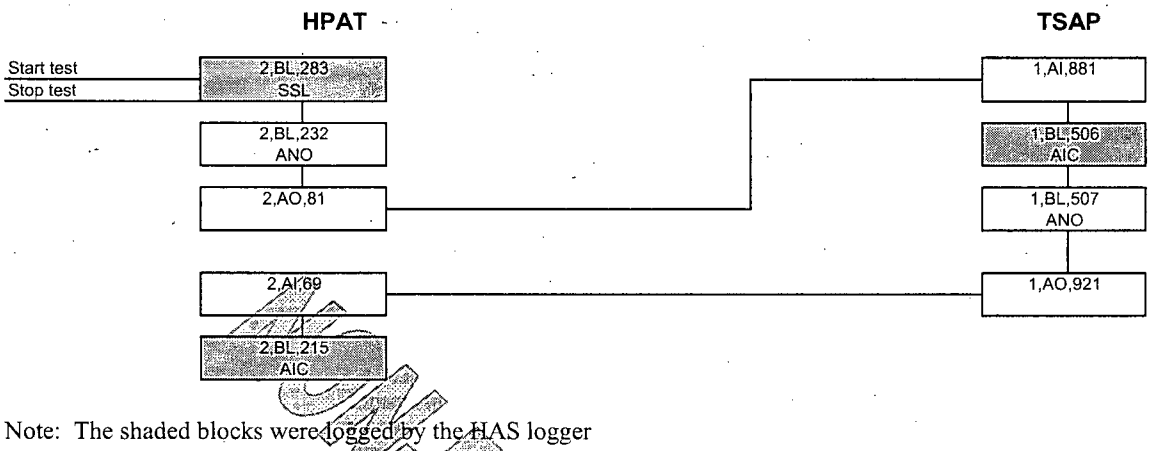
Table A.5-2. Pulse Input Channel Rate Mode Accuracy Data.

Input Frequency (Hz)		8-Bit Mode Measured Frequency				12-Bit Mode Measured Frequency		
Nominal	Measured	8 bit Image	Calculated Frequency Range Min. (Hz)	Calculated Frequency Range Max. (Hz)	Accuracy (%)	12-bit Image	Calculated Frequency (Hz)	Accuracy (%)
50	49.73							
600	594.1							
5,000	4,981							
10,000	10,005							
15,000	14,980							
19,500	19,460							

A.6 Automated Analog Accuracy Test (Section 4.1.6)

The automated test sequence was executed after the manual test sequences during prequalification testing, and then it was repeated before, during, and after selected qualification tests. The purpose of the prequalification test was to provide a baseline to compare against the tests performed at the other times listed above. This baseline data will be compared against data from the same test performed at the completion of the qualification program to demonstrate that system performance was not unacceptably impacted by the environmental stress conditions.

The TSAP configuration, established for the automated AI channel test as prescribed in Section 4.1.6.1, is shown below in Figure A.6-1. The Automated Test Sequence was then run as prescribed in Section 4.1.6.2 and the Historical Archiving System (HAS) logger was activated for the test.



Note: The shaded blocks were logged by the HAS logger

Figure A.6-1. AI Card Automated Accuracy Test Configuration.

The results of the test are shown in Figures A.6-2 and A.6-3. Figure A.6-2 shows the digital step function that was applied to the HPAT analog output card at 2,BL,283 where it was logged. This digital signal was converted to a 4 – 20 ma analog signal and supplied to the analog input card under test. The card converted the analog input signal to a digital signal where it was available for logging at 1,BL,506. This digital signal was converted to a 4 - 20 ma output signal and supplied to the HPAT analog input card at 2,AI,69. This analog input was converted to a digital output signal at 2,BL,215 where it was logged by the HAS.

The purpose of this test was to develop a baseline for the accuracy of the analog input card as measured at 1,BL,506. This baseline data will be compared against data from the same test performed throughout the qualification program to demonstrate the system performance was not unacceptably impacted by the various qualification tests. Although the acceptance criteria were specified to be 0.1%, this accuracy is not critical to the objectives of the test, and is considered to be acceptable. The critical item is the repeatability of the data.

NON-PROPRIETARY

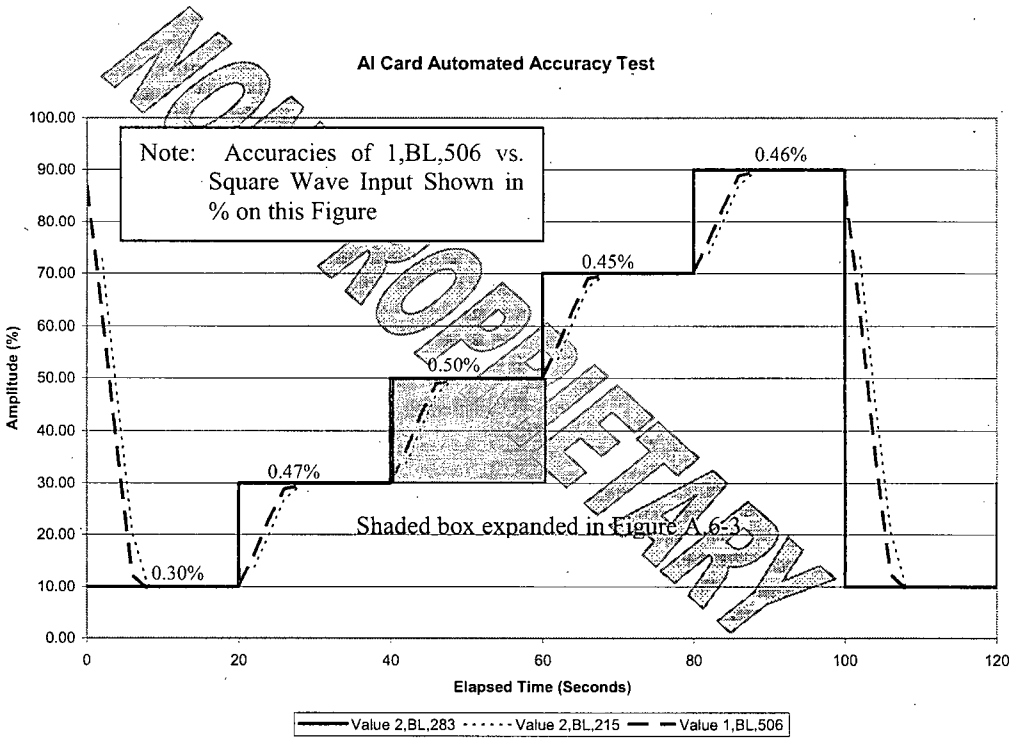


Figure A.6-2. AI Card Automated Accuracy Test Wave Forms.

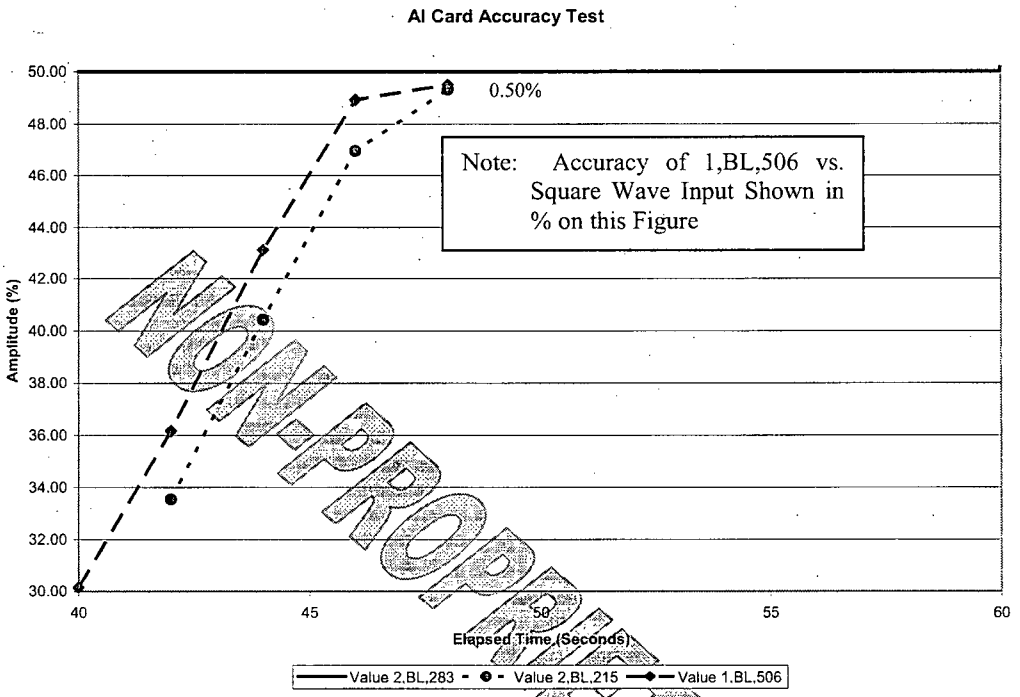


Figure A.6-3. AI Card Automated Accuracy Test – Expansion of Shaded Box in Figure A.6-2.

NON-PROPRIETARY

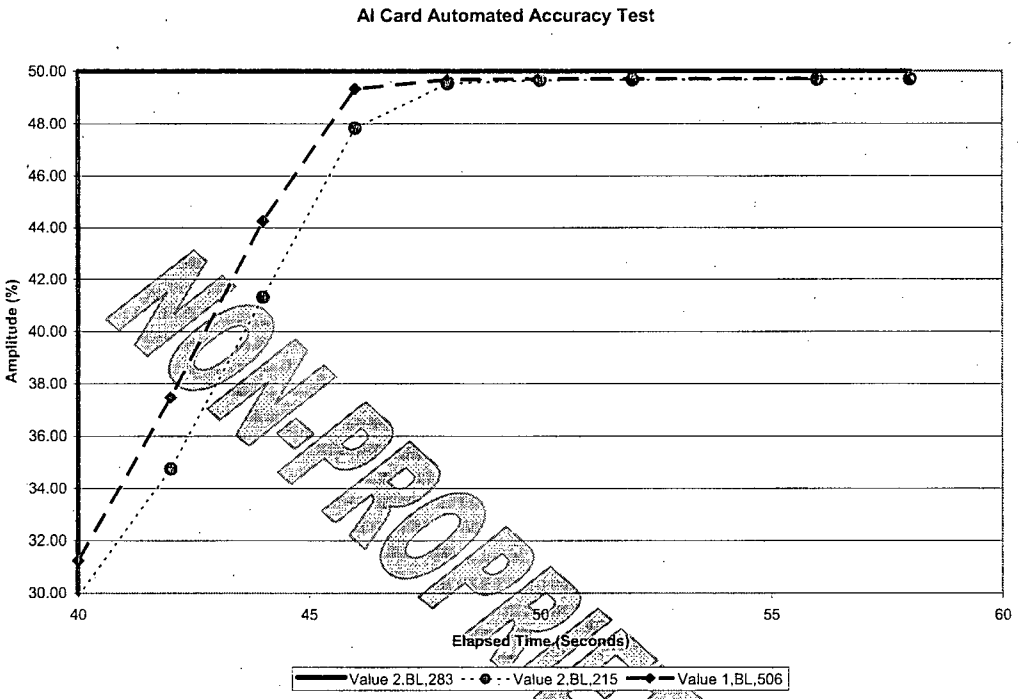


Figure A.6-4. AI Card Automated Accuracy Test – Post-Qualification Data with 1 Second Time Sampling.

NON-PROPRIETARY

The configuration for the automated AO channel test as prescribed in Section 4.1.6.1 is shown below in Figure A.6-5. The Automated Test Sequence was then run as prescribed in Section 4.1.6.2 and the HAS logger was activated for the test.

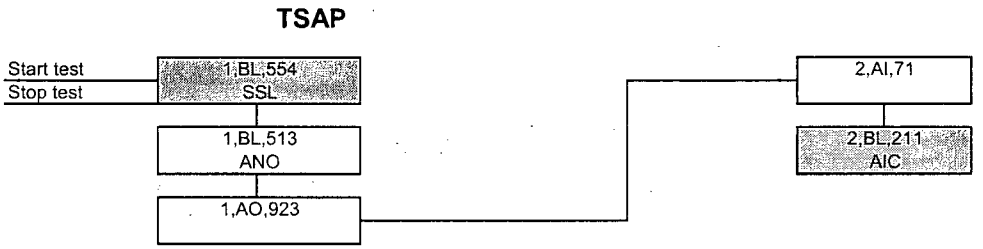


Figure A.6-5. AO Card Automated Accuracy Test Configuration.

The results of the test are shown in Figure A.6-6. A digital step function generated in the TSAP was applied to the AO Test Specimen at 1,BL,554 where it was logged. This digital signal was converted to a 4 – 20 ma analog signal and supplied to an analog input card in the HPAT. The card converted the analog input signal to a digital signal at 2,BL,211 where it was logged by the HAS.

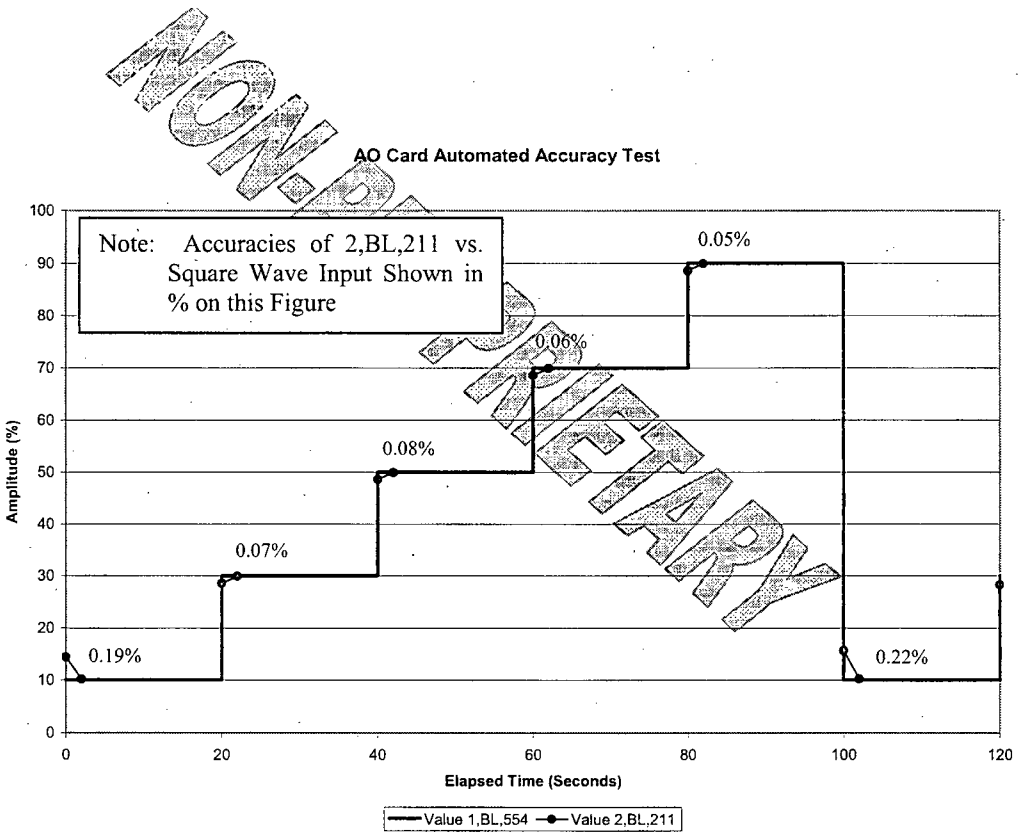


Figure A.6-6. AO Card Automated Accuracy Test Wave Forms.

The RTD and Pulse Card channels were configured for automatic logging by the HAS logger in Section 4.1.6.1. A summary of these setups and the initial logged values is provided below. The purpose of these tests was to develop baselines for the accuracy of each card. This baseline data will be compared against data from the same tests performed throughout the qualification program to demonstrate that system performance was not unacceptably impacted by the various qualification tests. The critical item is the demonstrated repeatability of the data.

RTD Channels -

Pulse Count Channels -

NON-PROPRIETARY

A.7 Digital Response Time Measurement (Section 4.2.1)

The purpose of this test was to use the average equation cycle time and measured values for digital response to measure both the stability of the processing cycles and the response time of the digital processing logic. The resulting response time measurement will include the time required for the following processing steps:

- Input filtering and signal conditioning
- Input processing by the I/O card processor
- Transfer over the internal system ICL to the controller
- Two processing cycles of the equation interpreter algorithm having a minimum of 2000 simple logic elements
- Transfer over the internal system ICL to the DO card
- Output processing of the DO processor
- Operation of the output relay.

The HPAT application provides a free-running square wave that is not synchronized with the operation of the TSAP. The output from this logic controls the input to 1,DI,628, and this input drives a simulated trip memory at point 2,DI,232. The simulated trip memory location will be set

on the FALSE-to-TRUE transition of 1,DI,628, and it will be reset when 1,DI,628 returns to a FALSE state. This test measures the time response of the setting and resetting of this trip memory.

In addition, the TSAP provides a round-robin discrete input/output/input/output program pattern composed of seven DI channels and seven DO channels as shown in Figure A.7-1. The first DI channel controls the first DO channel, and that signal is physically connected to the next DI channel in sequence. The last DO signal is then fed back to the first DI channel, and a NAND gate in the link from the first DI to the first DO permits the test engineer to start or stop the test from the JCRT workstation. When the test is disabled, the memory image of all seven DI and DO points in the chain will have a stable TRUE state, and the trip memory will remain static. When the test is first enabled, the first DO point will become FALSE, and this state will propagate through the chain with each successive processing cycle. Once this state is fed back to the first DI point, each point will exhibit a square wave pattern that is TRUE for seven processing cycles and FALSE for seven processing cycles. This circuit was added to provide a means of generating a large amount of data for statistical analysis in order to obtain an independent verification of the response time and the response time variation.

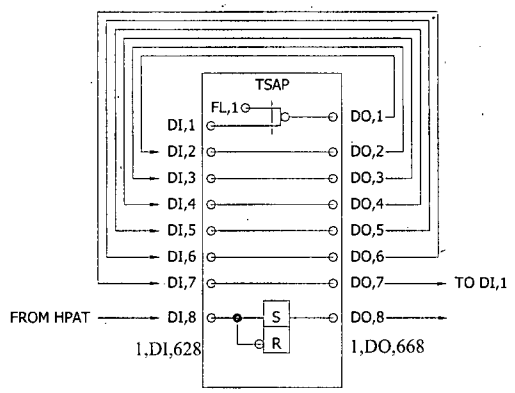


Figure A.7-1. TSAP Algorithm for Digital Response Test.

Finally, a TSAP equation cycle counter at HAS log point 1,CO,50 was monitored in the general time period of this test as required by the test procedure. This counter increments one count each time a TSAP equation cycle is completed. The HAS logs snapshots of the time stamp and total accumulated count every one or two seconds. Contiguous snapshots were gathered over approximately 7 minutes. The average equation cycle time was determined as 89 milliseconds by dividing the number of elapsed seconds by the total equation cycle count in that time period.

Manual Test Execution:

Table A.7-1. Manual Measurement of Digital Response Time from Post-qualification Test.

	Free-Running Square Wave Period (s)	Response Time: 1,DO,668-1,DI,628 (ms)
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
Average		
STD		

NON-PROPRIETARY

Automated Test Execution:

SOE logger is used to record the digital transition time for the automated response test. For the direct response measurement, the input signal 1,DI,628 was configured as 4,DI,8, whereas the output signal 1,DO,668 was configured as 4,DI,9. For the cascaded digital response measurement, signals of DO,1 to DO,7 shown in Figure A.7-1 were configured to be logged as from 4,DI,1 to 4,DI,7 respectively.

Table A.7-2. Automated Digital Response Time Measurements from Pre Qualification Test.

Test	Direct Measurement	Cascaded Measurement					
	4,DI,16 (9)-4,DI,8 (s)	4,DI,3-4,DI,2 (s)	4,DI,4-4,DI,3 (s)	4,DI,5-4,DI,4 (s)	4,DI,6-4,DI,5 (s)	4,DI,7-4,DI,6 (s)	4,DI,1-4,DI,7 (s)
Pre Q							

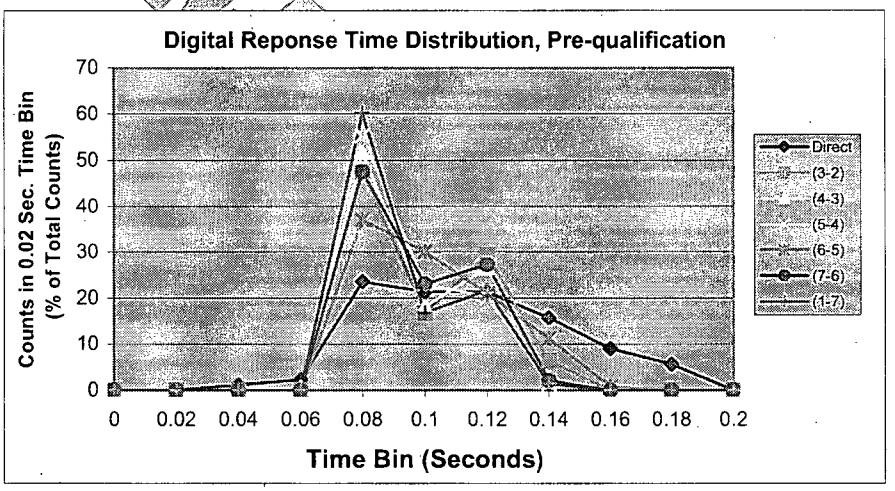


Figure A.7-2. Distribution of Digital Response Time During Pre Qualification Test.

A.8 TSAP Analog Response Time Test (Section 4.2.2)

General:

The manual analog response time test was first conducted on Feb. 17, 2004 between 5:56 and 6:03 PM as part of the TSAP Validation Test (TP0408, paragraph 2.4.2.2.2). The automated analog accuracy test first was run on Feb. 18 2004 between 12:36 to 12:41 AM. Because the manual analog response time test sequence of the Operability test would produce the same results as those obtained just a few hours before, the test engineers decided not to repeat that test sequence. The purpose of the manual test was to provide a direct measurement of signal characteristics by means of oscilloscope screen captures, and those screen captures would provide the basis for evaluating both the results of the initial automated test and each subsequent execution of the automated test.

TSAP Analog Response Time Test:

The test data generated during the manual test sequence consisted of direct oscilloscope screen captures of the analog trigger signal (1,AI,883) and the simulated trip output signal (1,DO,401). The analog trigger signal was originally designed to be a 0.5-Hz free running square wave (1 second at 45% of span and 1 second at 55% of span) generated by the HPAT. While the test is running, this trigger signal is routed to the TSAP AI point, and that input triggers a trip signal when it reaches 50% of span. Figure A.8-1 illustrates the logic algorithm used to produce the output signal. The trip signal controls a DO channel, and the measured response time consists of the time delay from the step transition of the AI signal to the low-to-high transition of the DO signal.

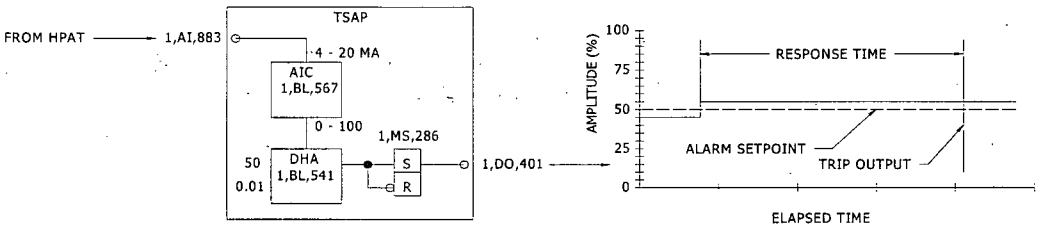


Figure A.8-1. Analog Response Time Test Algorithm.

The original design concept proved not to be effective due to the slow response of the HFC-AI16F assembly. The firmware for this board includes a 100-sample moving average as part of its processing algorithm for each input channel. As a result, the algorithm introduces a significant delay in the transition all of its input signals, and the AI image failed to reach the trip point before the end of 1 second. Consequently, the original algorithm was modified to increase the time period for each level to 10 seconds (10 seconds high, 10 seconds low). The resulting waveform consisted of a free-running square wave with a total design period of 20 seconds. The test algorithm was implemented only in the main controller of the Test Specimen.

Analog Response Time Test:

Table A.8-1 lists the various I/O and log points involved in the analog response time test. In addition to these points, the digital response time test points and the Equation Cycle Counter provide the basis for establishing the processing cycle time of the main controller of the Test Specimen. (Refer to the test report for digital response time and logged data for 1,CO,50. Corresponding elements were not configured for the single loop controller.)

Table A.8-1. Data Points for the Analog Response Time Test.

Point ID	Function	Log Point
1,CO,50	Equation Cycle Counter provides direct count of processing cycles per second.	HAS – 1,CO,50
1,AI,883	Analog Trigger Signal controls the trigger input to the Test Specimen trip logic.	HAS - 1,BL,567
1,DO,401	Simulated Trip Output provides the output signal to be used for measuring the analog response time.	SOE – 4,DI,10 HAS – 1,MS,286 HAS – 2,DI,161

Manual Test Execution:

The analog response time for the main controller was measured manually by connecting channel 1 of a dual trace oscilloscope to 1,AI,883 and channel 3 to 1,DO,401. The analog response time was then established by taking screen captures of the leading and trailing edges of the two signals. A total of six leading edge screen captures and four trailing edge screen captures were taken. (Figures A.8-2 and A.8-3 provide a sample of the leading and trailing edge waveforms; Figure A.8-4 provides an explanation of the parameters displayed on the screen.) Table A.8-2 lists the time delays obtained directly from the data on the screen captures and the average of response for the two transitions. The total period of the trigger signal and the resulting trip output signal were not measured at this time, but the trigger signal and the trip output signal were measured in the automated response time tests.

Table A.8-2. Manual Measurement of Analog Response Time from Pre Qualification Test.

Leading Edge Transition		Trailing Edge Transition	
Time	Measured Delay	Time	Measured Delay

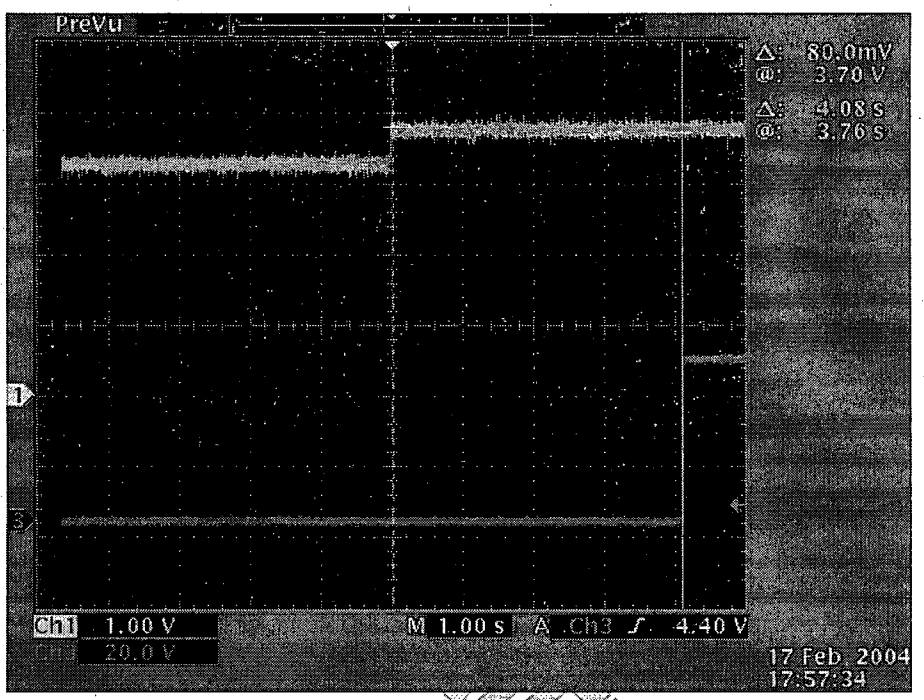


Figure A.8-2. Analog Response Leading Edge.

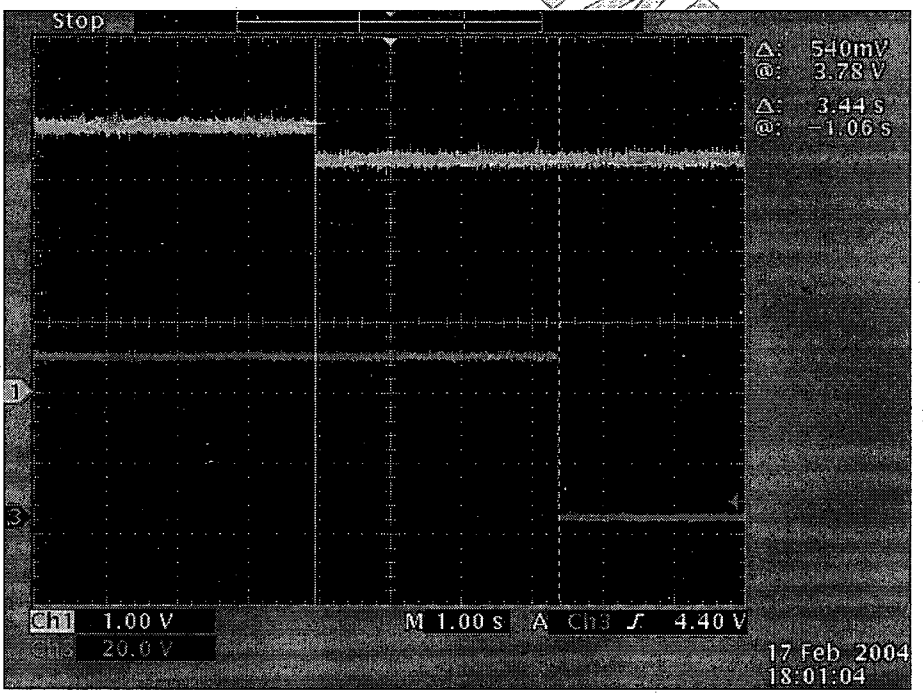


Figure A.8-3. Analog Response Trailing Edge.

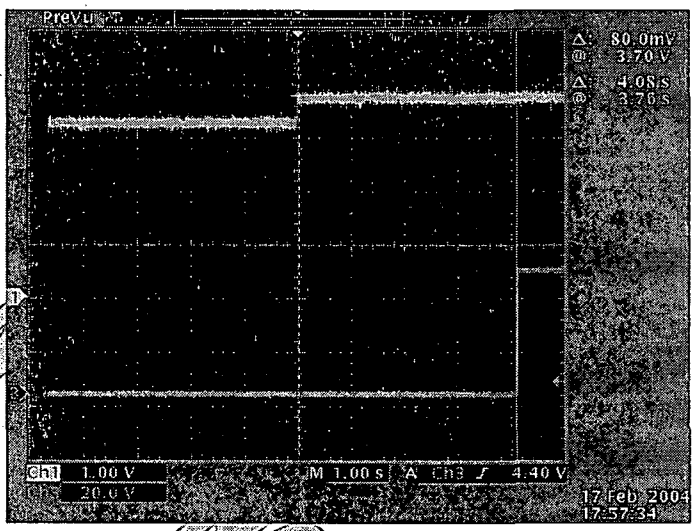


Figure A.8-4. Oscilloscope Display Parameters.

PROPRIETARY

Table A.8-3. Equation Interpreter Processing Cycles.

Total No. of cycles logged:	131		
Maximum No.		**Minimum cycle time**	
Minimum No.		**Maximum cycle time**	
Average No.		**Average cycle time**	
Deviation from the mean		**Deviation from the mean**	

NON-PROPRIETARY

Automated Test Execution:

Table A.8-4. Automated Analog Response Time Test Results from Pre Qualification Test.

Average period of trip waveform:			
Average set period		Average reset period	
AVERAGE DEVIATION FROM THE MEAN		Average deviation from the mean	

Conclusions:

NON-PROPRIETARY

A.9 Discrete Input Operability Test (Section 4.3)

The purpose of this attachment is to document the results of the Discrete Input Operability Test in Section 4.3 of the Operability Test Procedure TP0402, Rev. B. The acceptance criteria for all of the Operability Test are provided in Section 5.0.

This test was conducted during the pre qualification phase of testing to establish a performance baseline. The baseline data will be compared against the data from the same test preformed at the completion of the qualification program.

The Discrete Input Operability test demonstrates the capability of each type of discrete input channel to detect a transition in the signal being monitored. In order to accomplish this, DI channels under test are subjected to an input signal whose voltage level is controlled by a manual rheostat. During the test, the set voltage level and the reset voltage level for each DI channel type were measured.

One channel of each DI card type to qualify is tested for the following tests while the card is operating in the Test Specimen chassis:

- Set Voltage Threshold - is the lowest voltage level that the DI image is switched from off to on.
- Maximum Input Voltage - is the maximum voltage level the DI channel was proven to remain stable.
- Dropout Voltage (reset voltage level) - is the voltage level that the DI image is switched from on to off and remained reset.
- The voltage to the DI channel was dropped from the reset voltage level to 0 to prove the channel remains reset.
- Each DI channel being tested was turned on to prove input signal isolation.

NON-PROPRIETARY

Table A.9-1. Discrete Input Operability Test Results From In-house Test for Seismic Retest.

Test	Card Type Under Test											
	DI16I				DC34				DC33			
	1	2	3	Average	1	2	3	Average	1	2	3	Average
Set Voltage Threshold (V)												
Maximum Input Voltage (V)												
Dropout Voltage (V)												

NON-PROPRIETARY

A.10 Discrete Output Operability Test (Section 4.4)

The purpose of this attachment is to document the results of the Discrete Output Operability Test in Section 4.4 of the Operability Test Procedure TP0402, Rev. B. The acceptance criteria for all of the Operability Tests are provided in Section 5.0.

The Discrete Output Operability test demonstrated the capability of each type of discrete output channel to operate within its specified range of loading conditions. In order to accomplish this, the channel under test was energized while connected to a simulated field load that imposes maximum loading on the channel. The test demonstrated the capability for individual channels to sustain such maximum loading conditions without failure and without affecting operation of adjacent channels. The test was conducted during the pre qualification phase of testing to establish a performance baseline and after completion of the environmental stress tests to detect any deterioration from that level of that performance. It was not repeated before, during, and after any of the other qualification tests.

Relay DO Channel Operability Test (Section 4.4.1)

Table A.10-1. Relay DO Output Characteristics.

Card Type Under Test	
Output Channel Rating	
Contact Resistance (Average of 4 channels)	
Test Load Applied	
Each Channel Switches Under Load	

NON-PROPRIETARY

120 VAC DO Channel Operability (Section 4.4.2)

This test was executed on 1,DO,441 and 1,DO,442 (rack 2 slot 11) of an HFC-DC33 card. 1,DO,441 and 1,DO,442 were connected to the set and reset coils respectively of relay CR2 of the HPAT. These channels were controlled by the simulated valve control logic TO09, and the Burst of Events algorithm was used to control the two relay output channels. (Refer to TP0403. Relay CR2 is driven automatically by the BOE test.)

A variable power source was connected to a terminal block connected to two relays on the DC33. The variable power source was set to 90.0 ± 0.5 VAC at 47 Hz and 130.0 ± 0.5 VAC at 63 Hz to verify that the DO channels operated correctly over this range of voltages and frequencies. Screen captures from an oscilloscope were used to record these values. The simplified test setup provided in Figure A.10-1 was the setup for testing the DC33 DO channels.

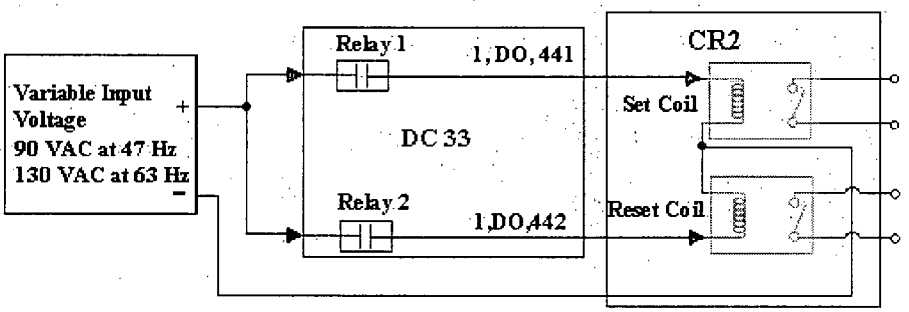


Figure A.10-1. DC 33 Setup for Discrete Output Testing.

NON-PROPRIETARY

Table A.10-2. 120 Vac Output Channel Parameters.

Parameter	Set Coil Circuit	Reset Coil Circuit
Coil Resistance		
Supply voltage set to 90.0 ± 0.5 vac at 47 Hz		
Peak off-on response voltage		
Peak in-rush current		
Steady-State output (rms)		
On state voltage drop		
Peak reverse EMF		
Off state leakage		
Supply voltage set to 130.0 ± 0.5 vac at 47 Hz		
Peak off-on response voltage		
Peak in-rush current		
Steady-State output (rms)		
On state voltage drop		
Peak reverse EMF		
Off state leakage		

NON-PROPRIETARY

125 VDC DO Channel Test (Section 4.4.3)

This test was executed on 1,DO,321 and 1,DO,322 (rack 1 slot 5) of an HFC-DC34 card. 1,DO,321 and 1,DO,322 were connected to the set and reset contacts respectively of relay CR1 of the HPAT. These channels were controlled by the simulated valve control logic TO6, and the Burst of Events algorithm was used to control the two relay output channels. (Refer to TP0403. Relay CR1 is driven automatically by the BOE test.)

A variable power source was set to 90.0 VDC and 140.0 VDC to verify that the DO channels operated correctly over this range of voltage. Screen captures from an oscilloscope were used to record the output signals from the DO channels. Next, the power was removed from the solenoid circuit, and the oscilloscope was used to measure the leakage current. The simplified test setup provided in Figure A.10-10 was the setup for testing the DC34 DO channels.

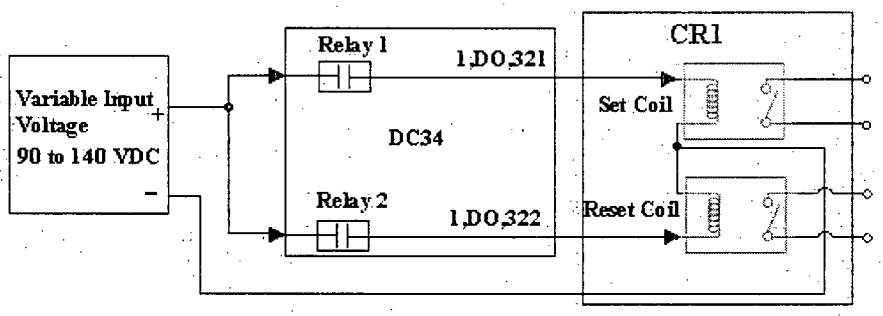


Figure A.10-10. DC34 Setup for Discrete Output Testing.

UNCONTROLLED PROPRIETARY

Data was collected to verify the operating voltage range, the minimum in-rush current capacity, on state voltage drop, current leakage, and steady state current. The operating voltage range was verified by setting the minimum input to 90 VDC and the maximum was set to 140 VDC. The on state voltage drop was determined by finding the voltage drop across each DC34 relay with voltage applied. Current leakage was the current from each relay on the DC34 while each relay was off with voltage applied. The steady state current was the measured current through the set and reset coils of CR1 with the DO channel ON.

Screen captures are recorded from an oscilloscope during the pre-qualification test that should have provided the following results for the DC34:

- Peak response signal on activation of the solenoid circuit.
- Steady state output signal.
- Peak reverse EMF on deactivation of the solenoid circuit.
- Off-state leakage signal.

Table A.10-3. 125 VDc Output Channel Parameters.

Parameter	Set Coil Circuit	Reset Coil Circuit
Coil Resistance		
Supply voltage set to 90.0 ± 0.5 vdc		
Peak off-on response voltage		
Peak in-rush current		

Steady-State output		
On state voltage drop		
Peak reverse EMF		
Off state leakage		
Supply voltage set to 140.0 ± 0.5 vdc		
Peak off-on response voltage		
Peak in-rush current		
Steady-State output		
On state voltage drop		
Peak reverse EMF		
Off state leakage		

NON-PROPRIETARY

A.11 Communication Operability Test (Section 4.5)

The Communication Operability Test was conducted during the prequalification phase of testing and then repeated before, during and after each qualification test. The purpose of the prequalification test was to provide a baseline to compare against the tests performed at the other times listed above. This comparison is to be done to demonstrate that the system communication performance was not unacceptably impacted by the qualification test stress conditions.

The HFC-6000 control system includes two internal communication networks. Intercommunication links (ICL) enable communication between the controller and all configured I/O modules for a particular controller. Redundant C-Link channels enable communication between a remote controller and attached workstation PCs, other remote controllers, or with external equipment. However, the C-Link channels and the associated equipment are not part of the scope of the Qualification Report.

This test will use link error counters to provide a basis for evaluating the quality of communication on these links. The overall test method will consist of recording the count value of the error counters at the start and end of a test period and interpreting the total accumulated error count as the measure of communication reliability. During prequalification or post qualification test phase, a set of automatic tests (accuracy, response and BOE test) was run to provide background activity for the communication test. The ICL link error counters can be read through an HFC software utility – Memory Editor and screen captures were made for the ICL link error counters. The system controller maintains an ICL error counter for each I/O module that communicates with that controller through an ICL. Whenever the system controller resets, all the ICL error counters will be reset to 0. Whenever an I/O module resets, its corresponding ICL error counter will increase rapidly. ICL error counter rolls over at 32767, i.e. $7FFF_H$.

NON-PROPRIETARY

ICL Error Counters

Table A.11-1. ICL Error Counters During Post Qualification Test.

Station	Card Type	Start Count	End Count	Count Diff	Start Time	Stop Time	Duration
Remote 1							
0							
1							
3							
5							
6							
7							
9							
9							
10							
10							

Station	Card Type	Start Count	End Count	Count Diff	Start Time	Stop Time	Duration
Remote 1							
16							
17							
19							
20							
22							
23							
24							
25							
26							
36							
37							
38							
39							
40							
48							
49							
50							
51							
52							
53							
54							
56							
57							
58							
59							
60							
Remote 3							
0							
1							
2							

UNCONTROLLED

A.12 Timer Test (Section 4.6, 4.6.1, 4.6.2)

The timer function within the controller is based on an integral clock that generates an interrupt every 10 ms, and the timer service routine updates the status of every "on-state" timer (TI point used in the application) at regular intervals based on the time base selection:

- Every 100 ms for a second time base (or 0.1 sec)
- Every 6 seconds for a minute time base (or 0.1 min)
- Every 6 minutes for an hour time base (or 0.1 hr).

All timers operate using multiples of 0.1 of the selected time base. The minimum preset value for a TI point is 0.1, and the maximum preset value is timer 5555.9. When executing the TSAP, the controller loads the timer preset value into the timer structure during each execution cycle of the Equation Interpreter. When the control input to a timer becomes true, the remote starts decrementing the timer value by 0.1 at the regular interval appropriate for its time base until the control input either becomes false or the timer value has been decremented to 0.0. Each TI point controls two output functions labeled GT and LT on the symbols shown in Figure A.12-1. The definitions for these output functions are as follows:

- GT – If the control input remains true until the preset value decrements to 0.0, the timer output becomes true. The timer output then remains true until the control input becomes false.

- LT – When the control input becomes true, the timer output becomes true. The timer output then and remains true until either the preset value decrements to 0.0 or the control input becomes false, whichever occurs first.

Figure A.12-2 illustrates a time line for processing a TI point having a preset value of $4\Delta T$, where ΔT is 0.1 of the selected time base. Because processing cycles of the Equation Interpreter are not synchronized with the regular interrupts for the timer service routine, the interval from execution of the timer start process to the first execution of the timer service routine is less than ΔT, and a finite delay exists after the TI value decrements to zero before the timer stop process executes. As a result, the effective time period defined by the timer function is

$$P = 4\,\Delta T - T1 + T2$$

Thus the total deviation from the preset value is represented by T2 – T1, which could be negative, positive, or zero for any particular instance. The maximum theoretical deviation exists when T1 is 0 or when T2 is zero. For the HFC-6000 system the maximum deviation for each time base is as follows:

- ±100 ms for second time base
- ±6 sec for minute time base
- ±6 min for hour time base.

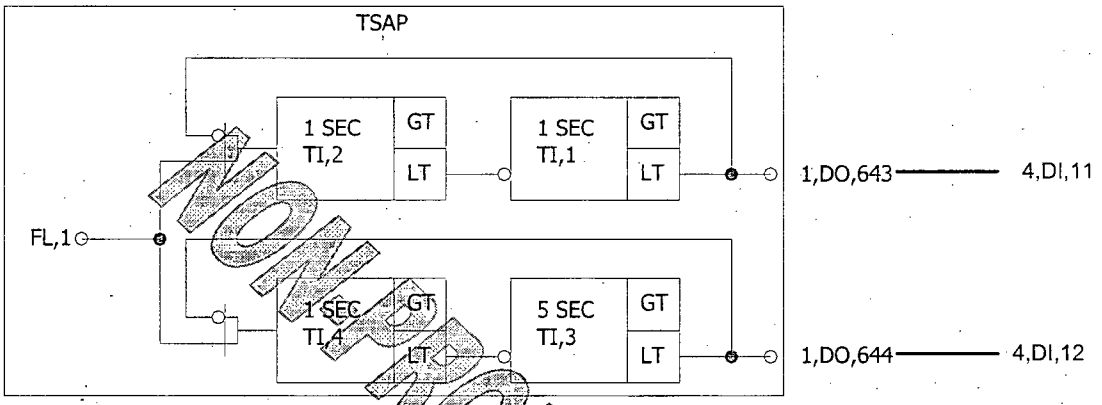


Figure A.12-1. TSAP Timer Test

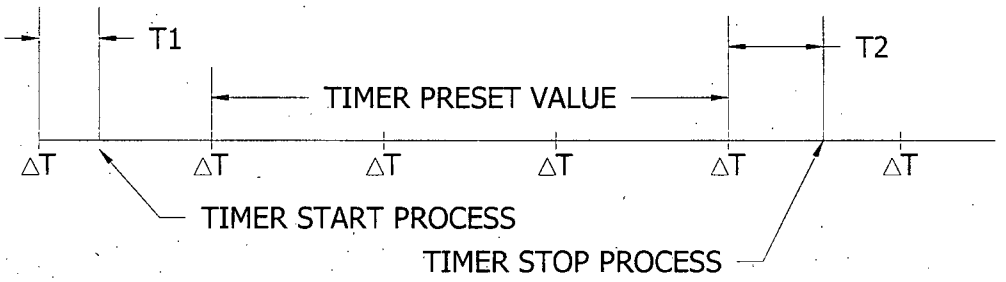


Figure A.12-2. HFC-6000 Timer Processing Function

The purpose of this test was to verify the accuracy of the timer function accessible to the TSAP. The timer test is based on logic completely contained within the TSAP. This logic consists of four pulse timers configured to control two separate free-running square waveforms, as illustrated in Figure A.12-1. The output from one set of timers is on for 1 second and off for 1 second; the waveform from the second set is on for 5 seconds and off for 1 second. The two output signals drive two separate DO channels: 1,DO,643 and 1,DO,644. This arrangement allows the direct measurements with an oscilloscope. During qualification testing, the outputs from the two DO channels are routed to separate SOE input channels of the HPAT to permit automatic recording of the signal transitions. 4,DI,11 and 4,DI,12 are the corresponding SOE logging points.

The timer test acceptance criteria (Section 5.0) specify that the timer accuracy shall vary by no more than ±1% of preset value or ±3 scan cycles. The measurements taken in the test configuration described above record the transitions of DO signals controlled from the memory image of the TI points. This does not measure the transitions of the timer periods directly, but the ICL transfer and the operation of the DO module introduce a uniform offset to the timer transitions. This test does test the way in which the timer function impacts any process under control.

Manual Timer Test (Section 4.6.1)

NON-PROPRIETARY

Table A.12-1. Manual Timer Test Results from Post Qualification Test.

	4,DI,11 (1 s On 1 s Off)			4,DI,12 (5 s On 1 s Off)		
Measurement	Period (s)	ABS Deviation (ms)	ABS Deviation (%)	Period	ABS Deviation (ms)	ABS Deviation (%)
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
Average						

Automated Timer Test (Section 4.6.2)

Table A.12-2 Automatic Timer Test Result from the Post Qualification Test.

		Preset Value (s)	Duration (s)	Duration Deviation (%)	Duration Jitter (%)	Period (s)	Period Deviation (%)	Period Jitter (%)
4,DI,12	ON							
	Number of Measurements							
	OFF							
	Number of Measurements							
4,DI,11	ON							
	Number of Measurements							
	OFF							
	Number of Measurements							

NON-PROPRIETARY

A.13 Failover Operability Test (Section 4.7)

The purpose of this test was to verify proper failover of the redundant controllers. The baseline data will be compared against other data from the same tests performed at the completion of the qualification program to demonstrate that the system performance was not unacceptably impacted by being stressed up to and beyond its normal operating state.

The HFC-6000 control system includes redundant controllers and redundant power supplies. The redundant controllers share a Dual-Ported Memory (DPM) assembly that provides the mechanism for transferring system status from the primary to the secondary controller.

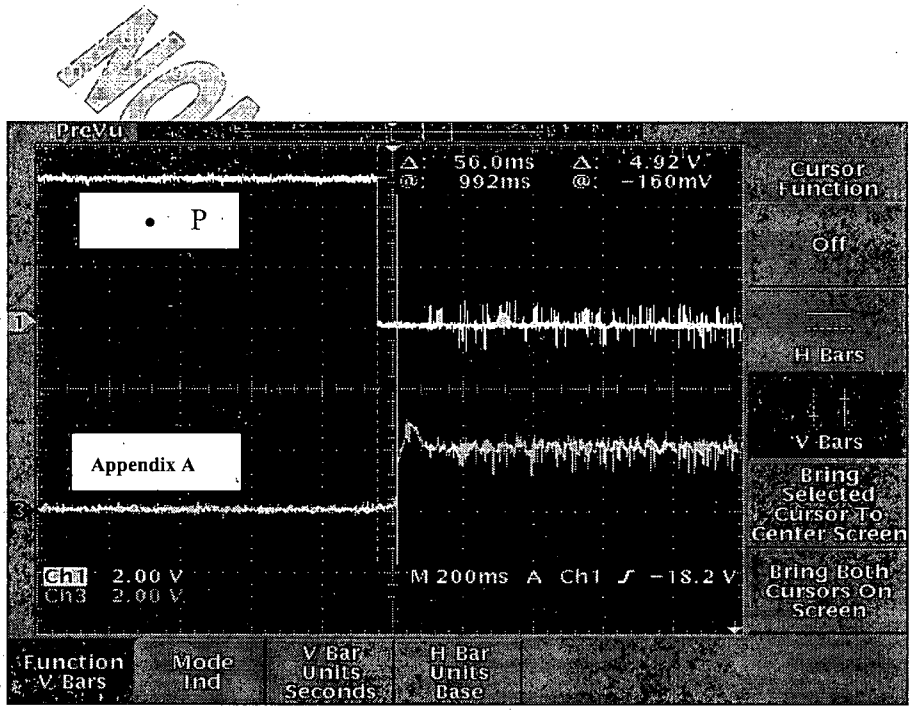


Figure A.13-1 Failover Delay

After recording the failover delay, the affects of failover were monitored on the analog controls loops. Channel 1 of the oscilloscope was connected to 2,AI,29 and channel 3 of the oscilloscope was connected to 2,AO,41. Then the failover button was pushed on the DPM and a screenshot was captured. Acceptance criteria states, the analog control circuits will not exhibit more than a .5% transient shift in the final output signal. Figure A.13-2 below shows the screen capture from the post-qualification test, no disruption occurred.

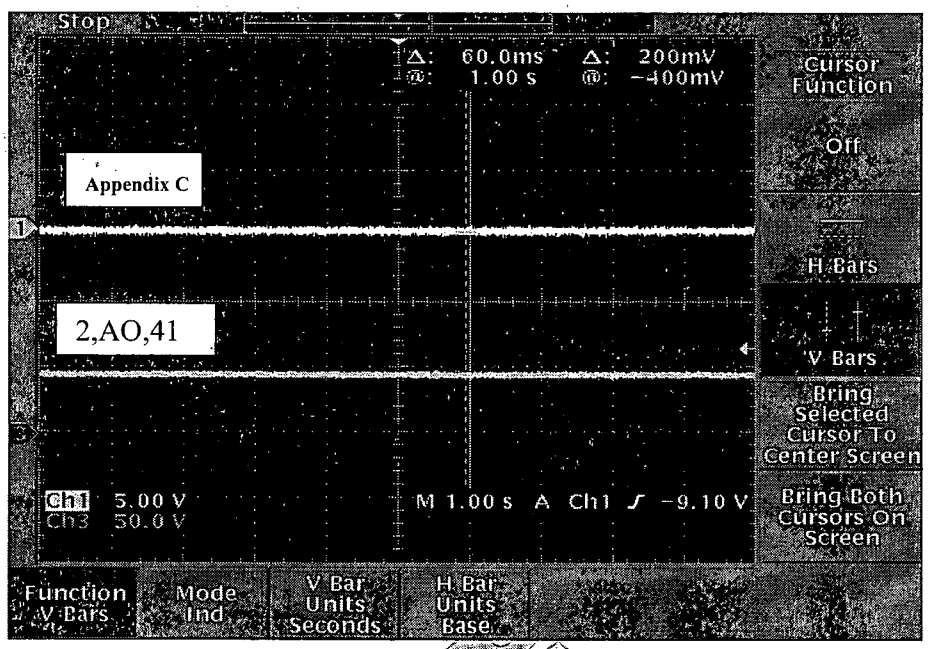


Figure A.13-2 Analog Control Loops

ETARY

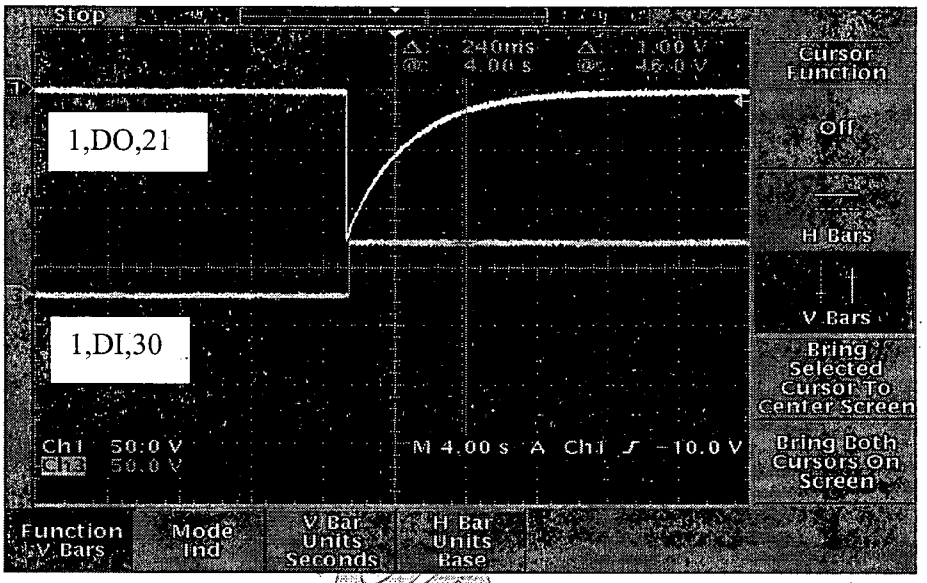


Figure A.13-3 Digital Control Loops

PROPRIETARY

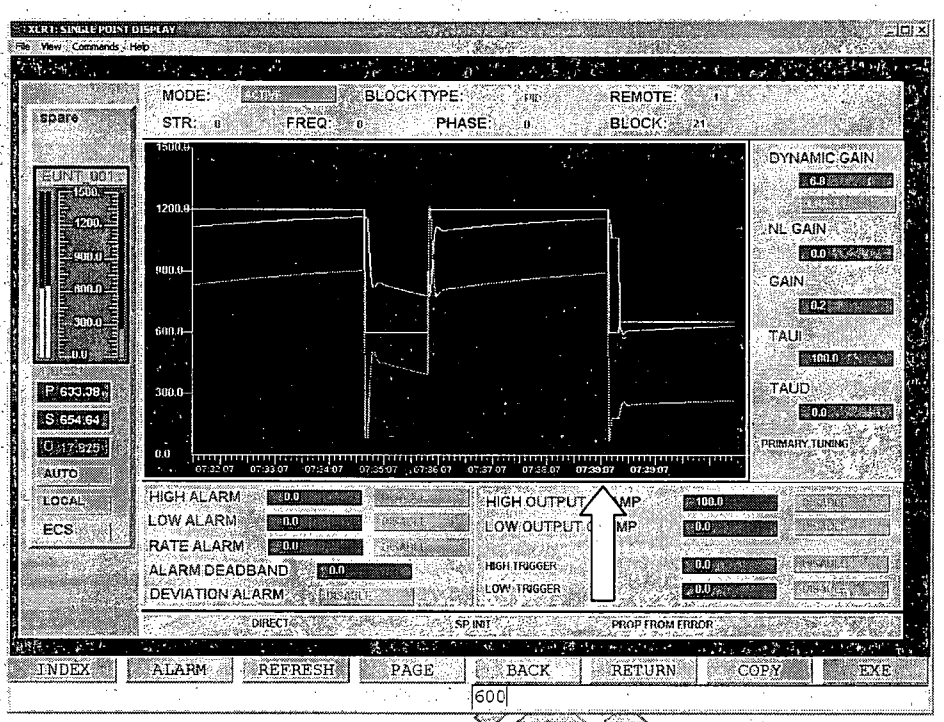


Figure A.13-4. Transition with Failover in Process.

PRELIMINARY

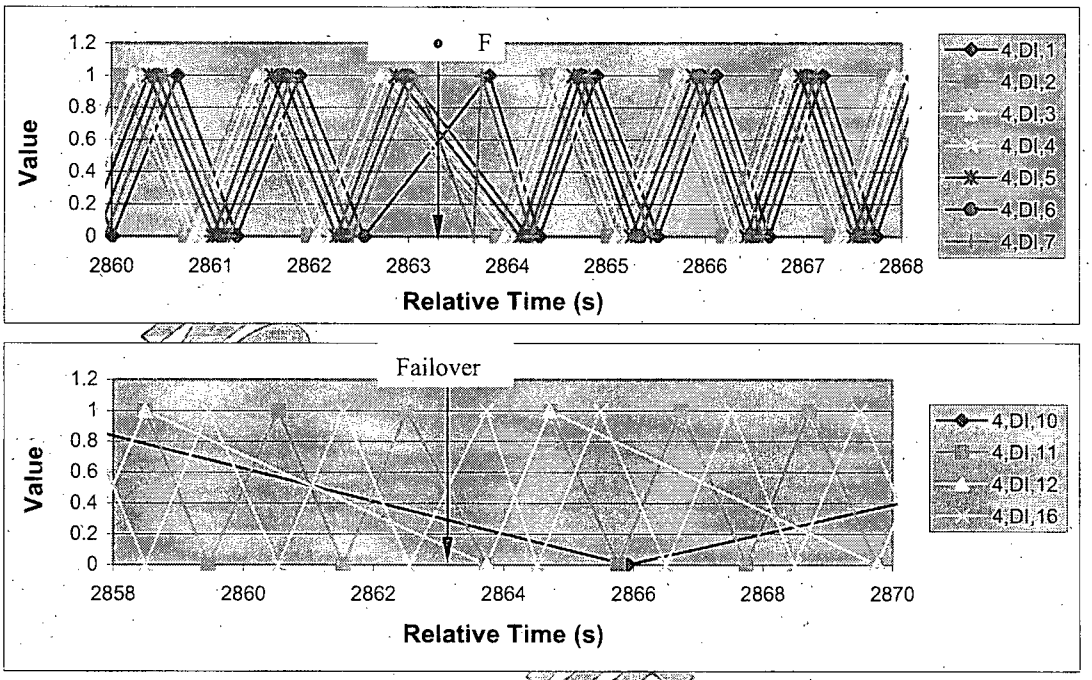


Figure A.13-5. DO (Logged as SOE Input Points) Points During Failover.

Table A.13-1. DO State Transition Time Before, During, and After Failover.

	4,DI,1	4,DI,2	4,DI,3	4,DI,4	4,DI,5	4,DI,6	4,DI,11	4,DI,12	4,DI,16
Before FO									
During FO									
After FO									

A.14 Loss of Power Test (Section 4.8)

The purpose of this test was to demonstrate that all I/O channels transition to default power-off states when power is removed and then hold these states following restoration of power until after system initialization is complete, at which time normal operation resumes.

During this test, power is removed from the Test Specimen for a minimum period of 30 seconds, and then power is restored. While power is out, points are checked to verify DO channels are de-energized, AO channels are open, and power output channels are open. After restoring the AC power to the Test Specimen, the output channels remain disabled while initialization is in progress

and once initialization is complete, the automated tests resume automatically without any additional intervention. Data from post qualification test were used to assess the system performance during power loss test since the data from pre qualification test were not preserved.

NON-PROPRIETARY

Table A.14-1. Loss of Power Manual Data.

Verification Criteria	Points Tested
AO channels are open (0 mA output)	
Power Outputs are open (120Vac, 125Vdc)	
DO channels are de-energized	

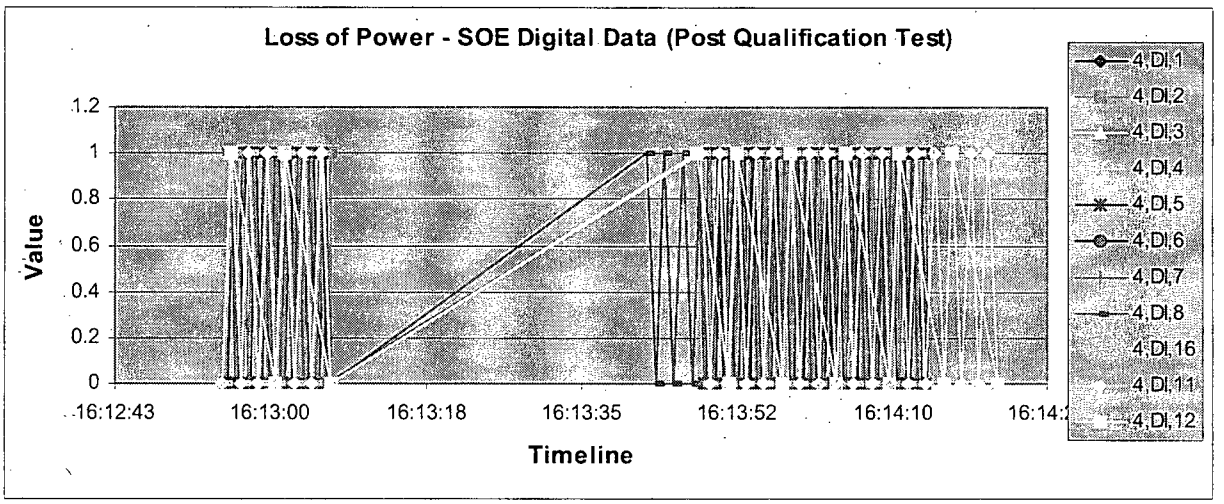


Figure A.14-1. Digital Data from SOE Logger from Loss of Power Test During Post Qualification Test.

NON-PROP

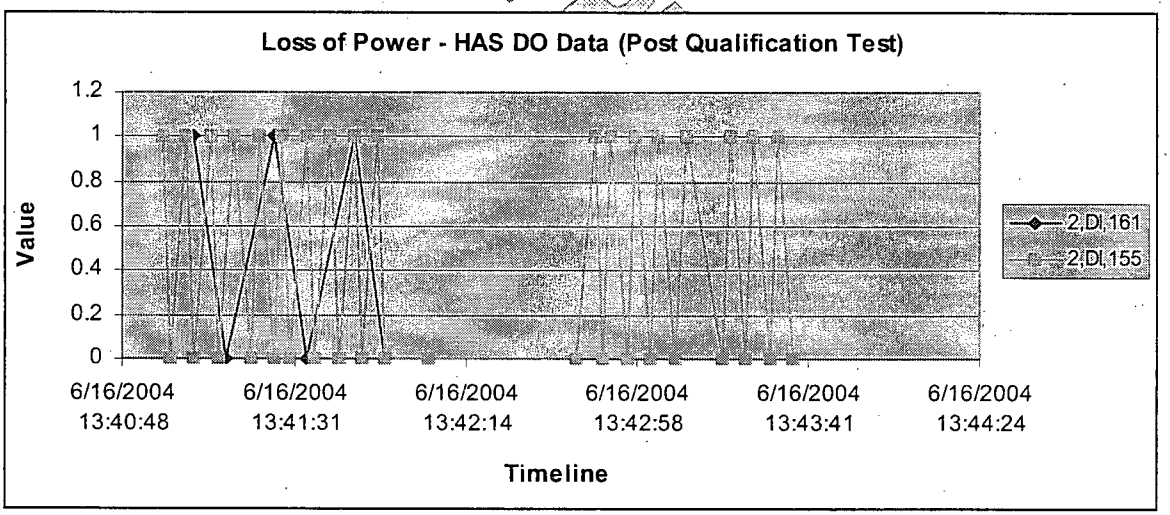


Figure A.14-2. Digital Data from HAS Logger During Loss of Power Test of Post Qualification Test.

Table A.14-2. Equation Processing Cycle Time During Loss of Power Test of Post Qualification Test.

Tag Name	Time Stamp	Value	Cycles/Second	Description	status
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					
1,CO,50					

NON-PROPRIETARY

Three different sources of analog data were monitored during this test:

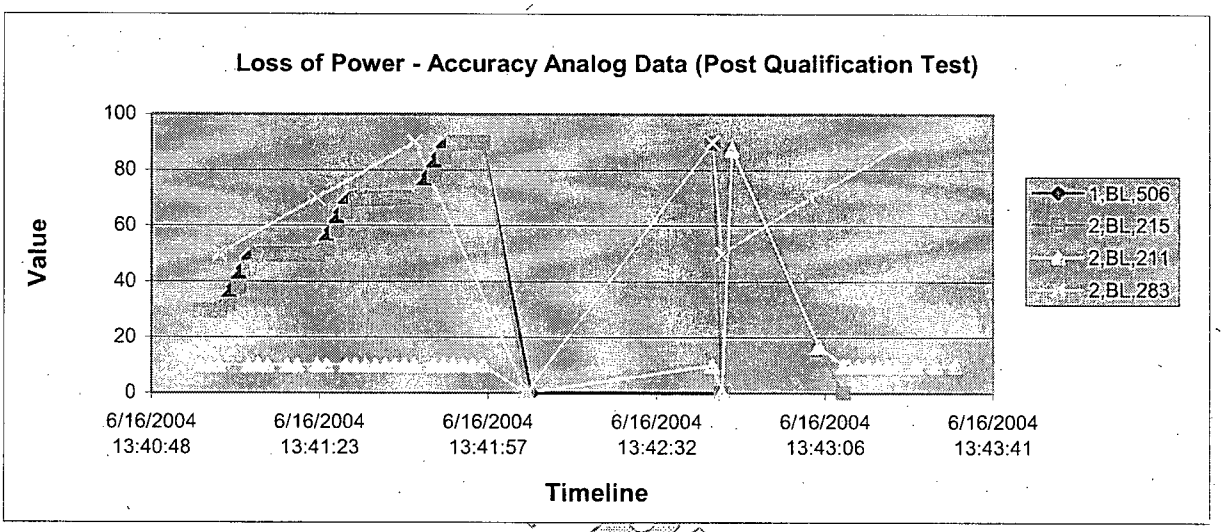


Figure A.14-3. Analog Data During Loss of Power Test from Post Qualification Test.

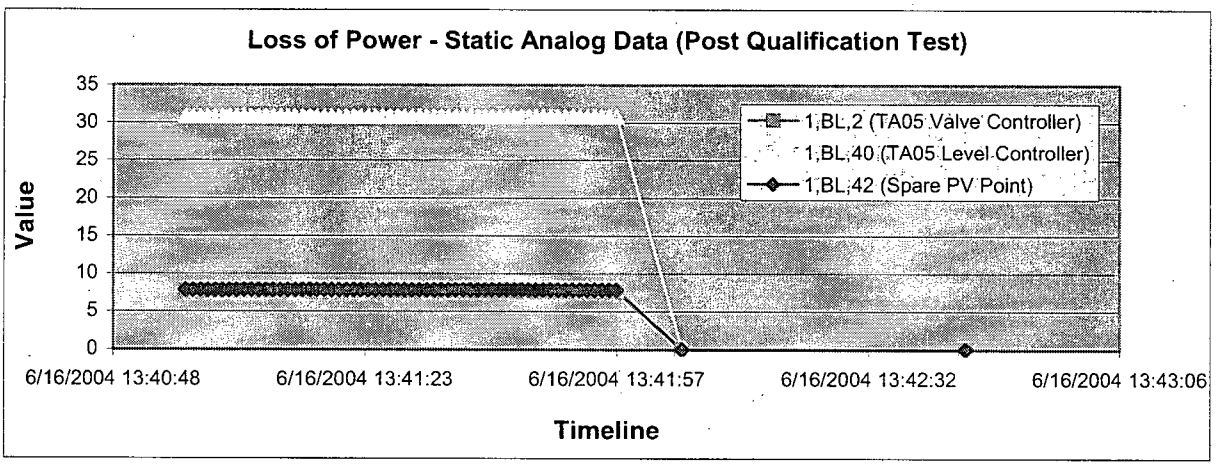


Figure A.14-4. Static Analog Data During Loss of Power Test from Post Qualification Test.

NON-PROPRIETARY

A.15 Power Interruption Test (Section 4.9)

This test was intended to demonstrate the performance of a control system channel with a single power supply during the switchover from one ac power source to another. The test configuration presumed a single power supply with a primary power source and a backup power source available with an automatic switchover. The expected transfer delay was 40 ms and the control system was expected to maintain control during the interruption. For this test, the power source to the Test Specimen was connected to a timer relay which was configured to interrupt power flow to the Test Specimen for a fixed interval of 40 ms. A set of automatic tests - accuracy, response and timer test, was run to provide background activity for the power interruption test. The power interruption was introduced twice, first time with all power supply modules in the Test Specimen in place, and second time with half of the power supply modules down.

The EPRI test requirements document states that if redundant power supplies are provided, then the supplies shall be protected so that undervoltage, overvoltage, shorts to ground, and other faults in one supply do not prevent the alternate supply from operating as designed. The HFC design employs redundant power sources and diode auctioneering to isolate the parallel power rails from one another to meet the above requirement. The results of single power supply testing described below demonstrated that one power supply is sufficient to run the system without interruption in the event of the loss of the redundant supply. However, a single power supply is not required to sustain controller operation during a power interruption when redundant power supplies are provided.

With Redundant Power Supply

- <u>Analog Accuracy Signals</u>

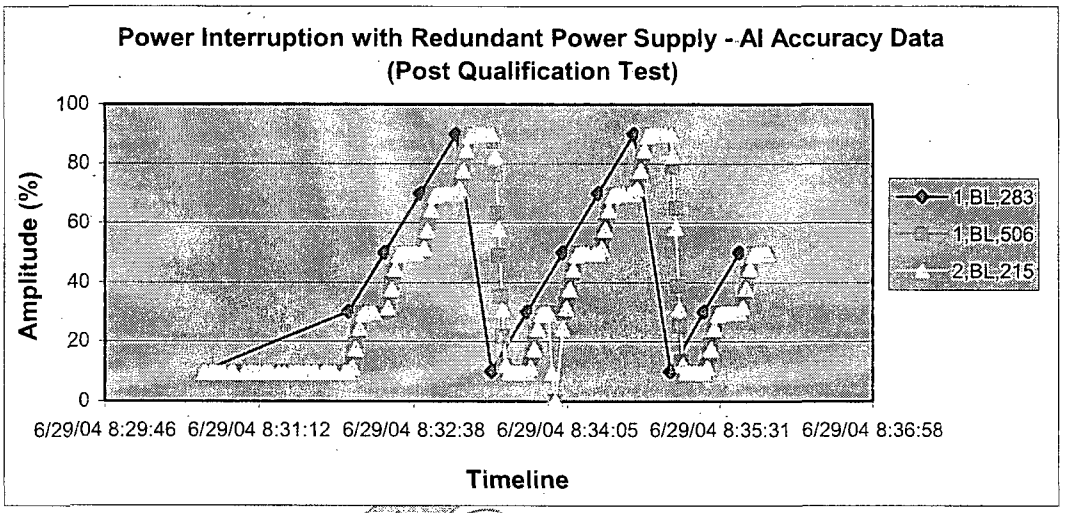


Figure A.15-1. AI Accuracy Signals During Power Interruption with Redundant Power Supply.

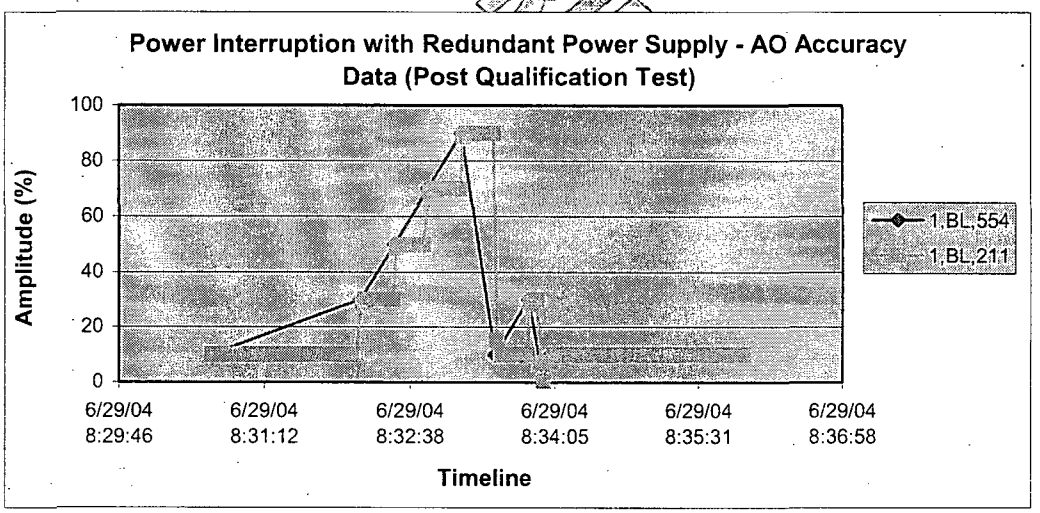


Figure A.15-2. AO Accuracy Signals During Power Interruption with Redundant Power Supply.

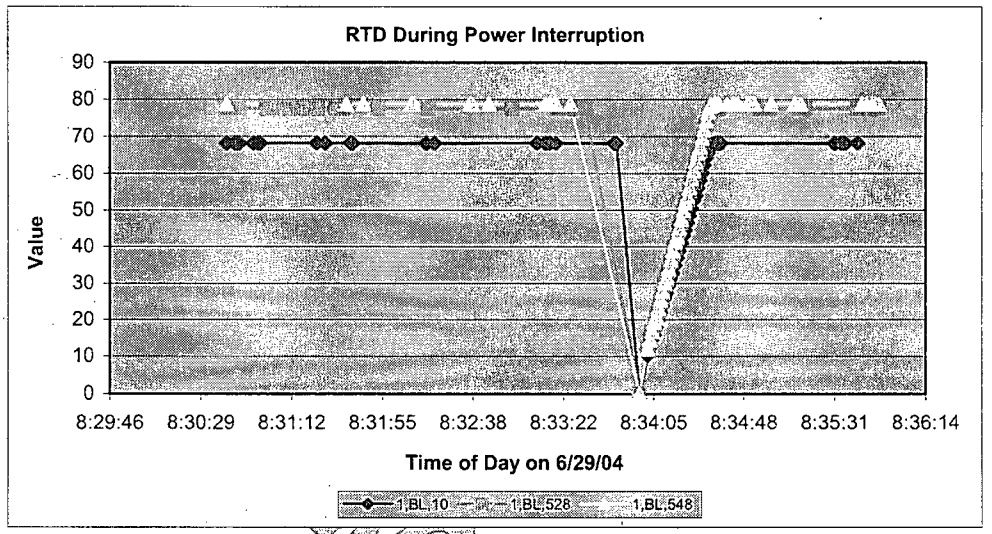


Figure A.15-3. RTD Accuracy During Power Interruption Test with Redundant Power Supply.

NON-PROPRIETARY

- Static Analog Signals

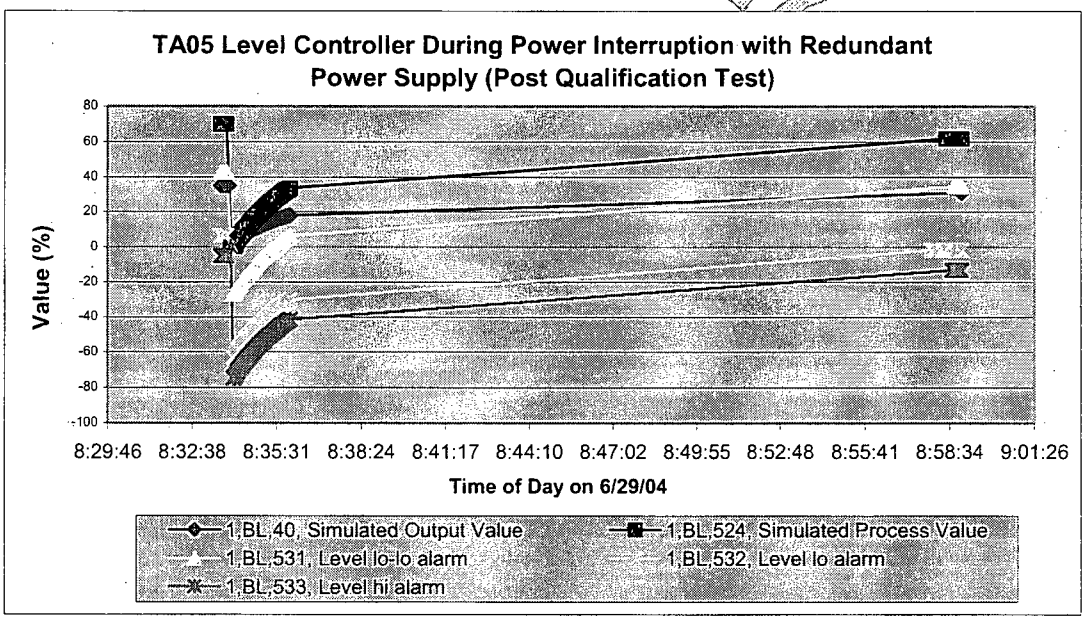


Figure A.15-4. TA05 Level Controller During Power Interruption Test with Redundant Power Supply.

With Single Power Supply

- Analog Accuracy Signals

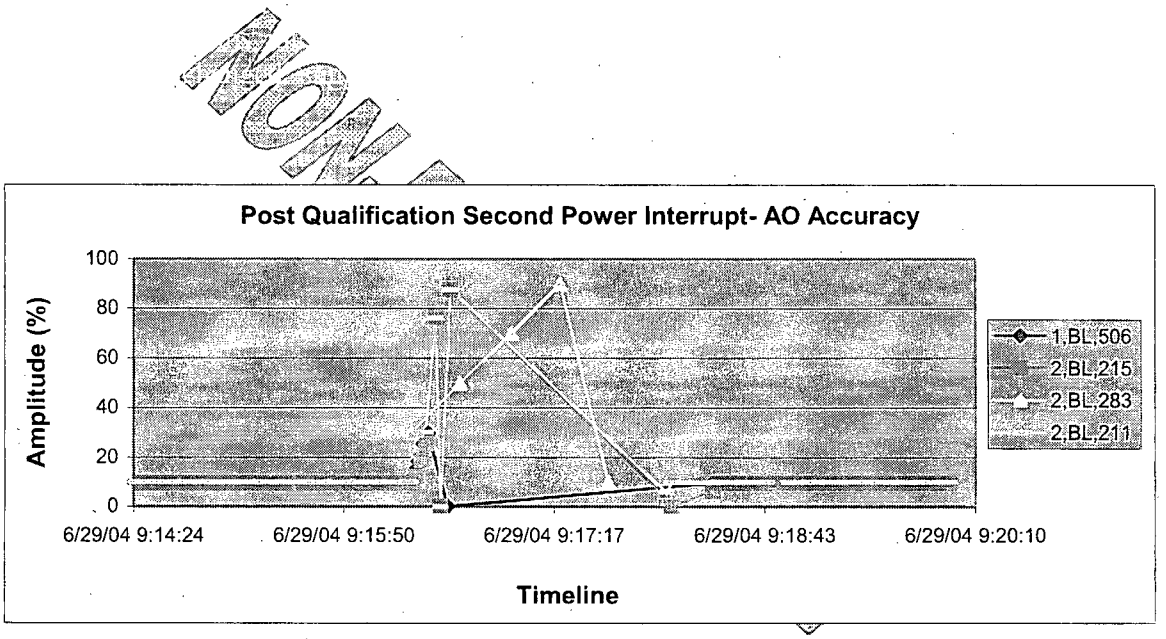


Figure A.15-5. Analog Accuracy Signals During Power Interruption Test with Single Power Supply.

Table A.15-1. Equation Processing Cycle Time During Power Interruption Test.

Tag Name	Time Stamp	Value	Description	Counts	Duration	Cycles /Second
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						

Tag Name	Time Stamp	Value	Description	Counts	Duration	Cycles /Second
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						
1,CO,50						

Non-Proprietary

- Digital Output Data

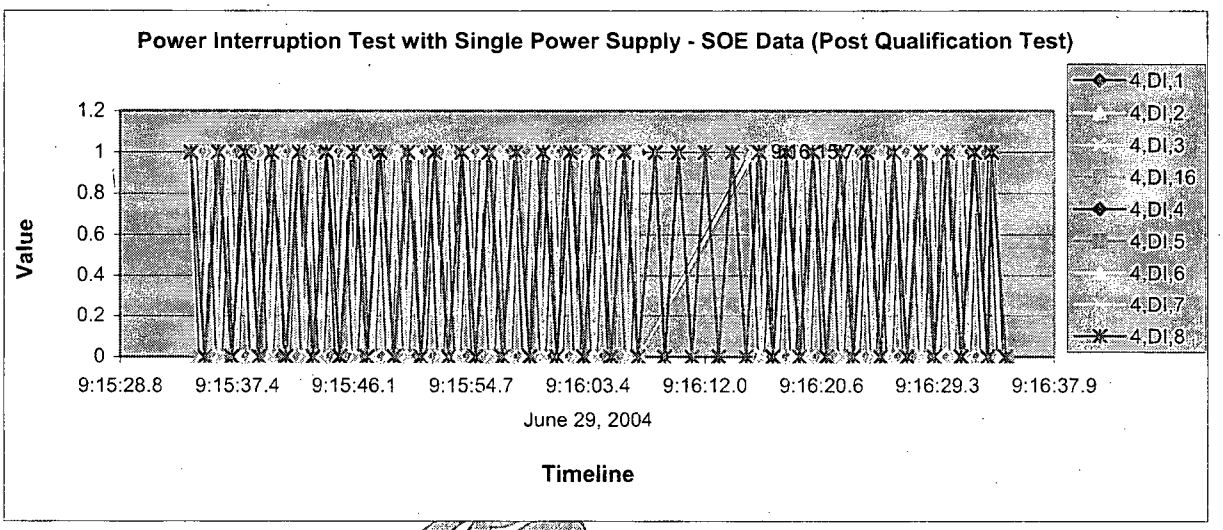


Figure A.15-6. Digital Data from SOE Logger During Power Interruption Test with Single Power Supply.

PROPRIETARY

Application to Nuclear Safety System

- Summary

- Conclusion

HFC-6000 Control System

ERD111 – Control System Qualification Project

Baseline Testing Summary Report
TS901-000-22

Rev B

NON-PROPRIETARY

APPENDIX B

PRUDENCY TESTS

B.1 General

The purpose of this attachment is to document the results of the Baseline Prudency Tests in Section 4.1 of the Prudency Test Procedure TP0403, Rev. C.

The Prudency Tests are a set of tests which were designed to exercise the Test Specimen under extreme loading conditions to provide a prequalification performance baseline. During subsequent qualification testing and post qualification testing applicable sections of this testing would be repeated to identify any performance degradation from the performance baseline. The Prudency Test consists of Burst of Events (BOE) test, Serial Port Failure test, Serial Port Noise test and Fault Simulation test. The test data is captured and recorded by the Sequence of Events (SOE) system and the Historical Archiving System (HAS). The SOE system has a faster response time but is limited by only being capable of capturing digital data, and in its data storage capacity.

The Burst of Events (BOE) section of the Prudency test was configured to impose a large number of operations on the HFC-6000 Test Specimen simultaneously to provide a high level of processing activity equivalent that specified in EPRI TR-107330.

The HFC-6000 Prudency Test Steps 4.1 through 4.2.2 were performed prior to shipping the Test Specimen to Wyle Laboratories for qualification testing. However, most of the test data generated during these tests was overwritten due to a misunderstanding by the test personnel of the limitations of the SOE data storage capacity. While the loss of this earliest baseline data was unfortunate, it does not present a significant problem in the analysis of the Test Specimen performance data. The baseline Prudency Test and each of the subsequent Prudency Tests are evaluated against stated acceptance criteria in the test procedures. A significant performance degradation occurred only when or if the Test Specimen's performance fell outside of the defined requirements for system performance. At that point an evaluation was required to determine the significance of the problem, and its potential impacts. Depending upon the evaluation of the degradation and its causes, the possible outcomes could range from revising the acceptance criteria and/or equipment performance specifications, to modification of the equipment design and repeating the tests affected.

For the analog potion of the BOE test, a square waveform was used with a frequency of 0.5 Hz (one second on, one second off) with the amplitude going from 10% to 90% of the card input range.

Certain pieces of baseline Prudency Test baseline data, while not specifically required in order to demonstrate that the HFC-6000 equipment is qualified, would have been worthwhile having to support some of the data analysis. Therefore, in addition to the qualification and post qualification Prudency Testing, for which data was available, supplemental testing was performed on specific equipment and other data sources (e.g. incoming inspection reports) were assembled to compensate for the baseline data loss.

The Serial Port Failure section of the Prudency test was configured to test the Redundant Intercommunication Links (ICL) that enable communication between the HFC-SBC06 controller and all other cards associated with a particular remote.

The Serial Port Noise test is designed to superimpose a white noise signal on the transmit and receive signal lines of each serial port. When the pre qualification test was done, execution of this test was not required during any phase of the qualification tests. Therefore, it was decided not to include this testing in the baseline testing, Instead, it was performed after the equipment had returned from Wyle labs.

B.2 Digital Input/Output BOE Test (Section 4.1.2)

The setup for this test procedure was performed in Sections 4.0 through 4.1.1.2. The following digital channels were toggled once per second:

- 9 DI channels (48-vdc excitation voltage)
- 4 120 vac DO channels
- 2 125 vac channels
- 23 relay output channels

Control signals for this BOE input were provided by the HPAT to the TSAP. The TSAP responded to these control signals and generated the required driving signals to command the concurrent cycling of the TSAP input and output channels listed above.

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Table B.2-1. Digital BOE Abnormal Transitions in the Pre Qualification Test.

			Transition Time Duration (Seconds)						
Time Stamp (AM on 2/18/04)			4,DI,30	4,DI,29	4,DI,28	4,DI,27	4,DI,26	4,DI,25	4,DI,24
H	M	S							
2	25	27.2							
2	25	30.1							
2	25	43.5							
2	25	44.1							
2	26	11.1							
2	26	15.1							
2	26	15.1							
2	26	18.2							
2	26	19.1							
2	26	23.1							
2	26	23.1							
2	26	59.1							
Total Number of Transitions									
Total Number of Contact Bounce Events									
Total Number of Anomalies									
Anomaly%									

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B.3 Analog BOE Test (Section 4.1.2)

General

The analog burst of events (BOE) test consists of a free-running analog square wave signal that switches between 10% and 90% of full span with a 10-second dwell time at each level. (The original test design required a 1-second dwell time in accordance with requirements of EPRI TR-107330, but this was changed to 1.5 seconds to ensure reliable HAS logging. During the initial execution of the automated tests, this preset time was changed to 10 seconds due to the response time of the AI modules.) The test algorithm operates as part of the HPAT application (remote 2) and drives six 4- to 20-mA AO channels. Five of these AO channels are wired to separate AI channels of the main controller of the Test Specimen (remote 1), and one of the signals was wired to an AI channel of the single-loop controller (remote 3). However, the single-loop controller (remote 3) is not part of the Qualification Report. The TSAP for both remote 1 and remote 3 provided logic to loop these analog signals back to separate AO channels, and the resulting signals were returned to the HPAT.

The BOE test algorithm was configured so that it could be started and stopped by command input from the HPAT workstation PC. When the test was disabled, all six analog BOE AO signals remained static at 90% of span. When the test was enabled, the test algorithm began operating, and the test signal traversed a closed loop from the HPAT to the Test Specimen and back to the HPAT. The HAS logger, which operates on the HPAT workstation, was configured to log the driving signal of the BOE algorithm, four of the Test Specimen AI signals, and the corresponding four AO signals (Table B.3-1). Because the HAS logger can only access data available from DDB broadcasts on the C-Link, individual BL points provided the actual data that was recorded.

TSAP Logic Configuration for Analog BOE – Remote 1

The main Test Specimen controller received analog BOE signals at five separate AI channels, and each of these input signals was processed by a separate AIC block. Three of these inputs were logged by the HAS, and one (1,AI,882) was used to drive an AO channel (1,AO,922). The main Test Specimen also received the analog BOE algorithm via the C-Link as a digital image, and this digital image was used to drive four additional AO channels. All four of these AO channels were routed to AI channels of the HPAT, and two of these channels were logged by the HAS for the analog BOE test.

Table B.3-1. Data Points for the Analog Prudency Test.

PT ID	Description	Log Point
HPAT		
Main Test Specimen Controller		
Single Loop Controller Chassis		

Test Result Analysis – AI BOE Test Results for Remote 1

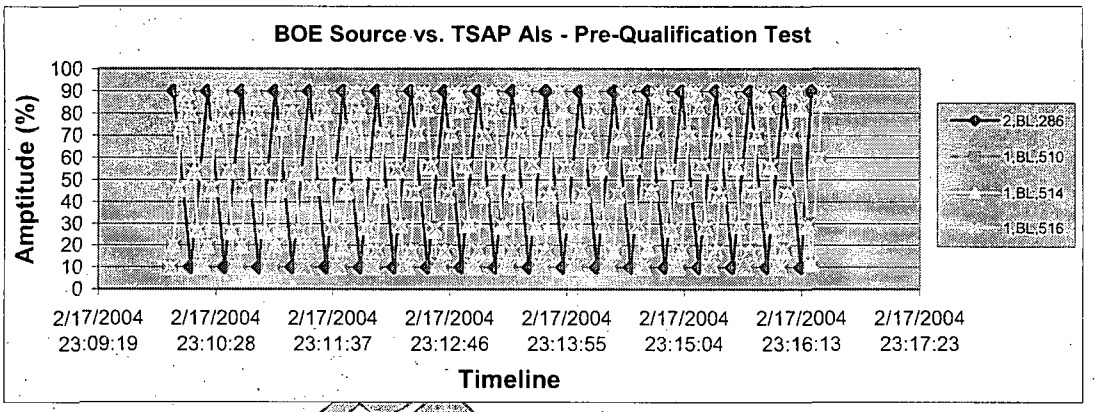

Figure B.3-1. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 During the Pre Qualification Test.

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Table B.3-2. TSAP AI Channel Readings and Deviations from BOE Source Signal During the Pre Qualification Test.

	1,AI,882 (1,BL,510)	1,AI,884 (1,BL,514)	1,AI,901 (1,BL,516)
10% Measurement (%)			
Deviation From 10% (%)			
Num of Measurements			
90% Measurement (%)			
Deviation From 90% (%)			
Num of Measurements			

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Test Result Analysis – AO BOE Test Results

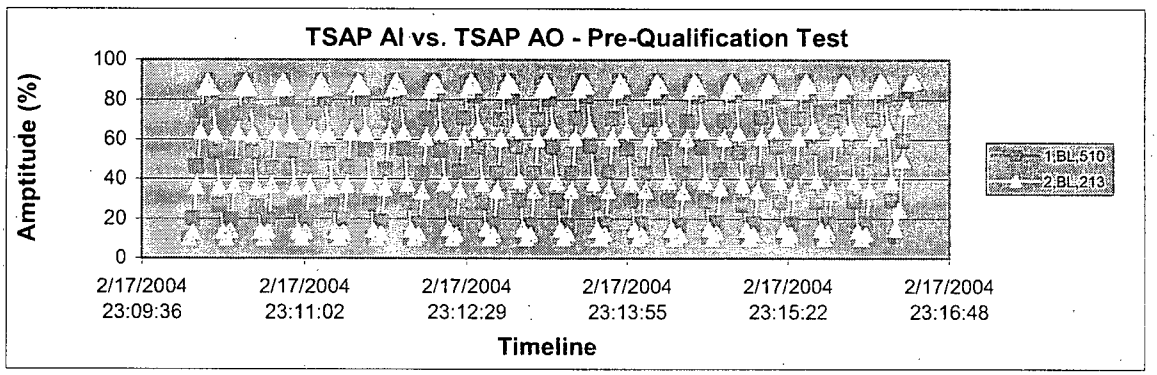

Figure B.3-2. Logged TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213).

Table B.3-3. TSAP AOs and Corresponding TSAP AIs in Remote1 During the Pre Qualification Test.

	1,AI,882 (1,BL,510)	1,AO,922 (2,BL,213)	Deviation (2,BL,213 vs. 1,BL,510)
10% Measurement (%)			
Number of Measurements			
90% Measurement (%)			
Number of Measurements			

Evaluation – Effect of HAS logger on Test Results

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Table B.3-4. TSAP AI Signals in Post-qualification Test.

	1,AI,882 (1,BL,510)	1,AI,884 (1,BL,514)	1,AI,901 (1,BL,516)
10% Measurement (%)			
10% Deviations (%)			
Num of Measurements			
90% Measurement (%)			
90% Deviations (%)			
Num of Measurements			

Table B.3-5. TSAP AO Signals versus TSAP AI Signals in Post-qualification Test.

	1,BL,510	2,BL,213	Deviation (2,BL,213 vs. 1,BL,510)
10% Measurement (%)			
Number of Measurements			
90% Measurement (%)			
Number of Measurements			

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B.4 Serial Port Failure Tests (Section 4.2)

The Serial Port Failure test section of the Prudency test is configured to test the redundant Intercommunication Link (ICL) that enables communication between the HFC-SBC06 and all other modules associated with a particular remote.

The objective of the Serial Port Failure Test is to demonstrate that a hardware failure on a single serial link will have no adverse impact on the steady-state operation of the controller.

The test for the ICL was to impose failure conditions on one of the redundant pair.

ICL Failure Test (Section 4.2.2)

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Serial Link Noise Test (Section 4.3.2)

B.5 Fault Simulation Test (Section 4.3.3)

The Fault Simulation Test covers introduction of a simulated condition to trigger failover from the primary to the secondary controller. Demonstration of the failover function is covered by the Failover Operability test in the Operability Test Procedure (TP0402). Therefore, this test was not intended to be run as a part of the Prudency Test Procedure (TP0403).

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HFC-6000 Control System

ERD111 – Control System Qualification Project

Environmental Testing Summary Report

TS901-000-23

Rev B

Effective Date	9/26/07
Author/Title	Jonathan Taylor/Charles Musick
Reviewer/Title	John A. Stevens
Approval/Title	Terrence A. Gerardis

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Date	Revision	Author	Changes
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11/08/04	A.	B. Han	Release
9/25/07	B	J. Taylor/ C. Musick	Revised Scope of Topical Report

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1.0 PURPOSE

HFC is generically qualifying its HFC-6000 control system for nuclear safety-related applications in U.S. nuclear power plants. The approach taken for this qualification effort is based on the guidance provided in EPRI-TR-107330, Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants.

This document specifically addresses the Environmental Testing segment of the qualification testing program.

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2.0 SCOPE

2.1 Definition of the test setup and environmental qualification testing performed by Wyle Laboratories for the HFC-6000 Control System test specimen.

2.2 Evaluation of Operability and Prudency testing performed before/during/after Environmental Testing against baseline testing results.

2.3 Identification of any performance degradation from the Baseline Operating and Prudency testing performed.

3.0 REFERENCES

3.1	TS901-000-22	HFC6000 Baseline Testing Summary Report
3.2	TP0402	Operability Test Procedure
3.3	TP0403	Prudency Test Procedure
3.4	VV0414	Master Configuration List
3.5	50043-1	Test Procedure Environmental and Seismic Testing of an HFC-6000 Control System (Wyle)
		Test Report Environmental and Seismic Testing of an HFC-6000 Control System (Wyle)
3.6	TP0404	HFC-6000 Control Systems, ERD111- Control System Qualification Environmental Stress Procedure

4.0 HFC-6000 ENVIRONMENTAL QUALIFICATION DESCRIPTION

The environmental stress test is one of a battery of tests mandated by EPRI TR-107330 to qualify a commercially available PLC for safety-related applications in a nuclear

power plant. This test exposes a specially configured HFC-6000 control system (Test Specimen) to extremes of temperature and humidity, Figure 4-1, in order to induce accelerated aging of functional components.

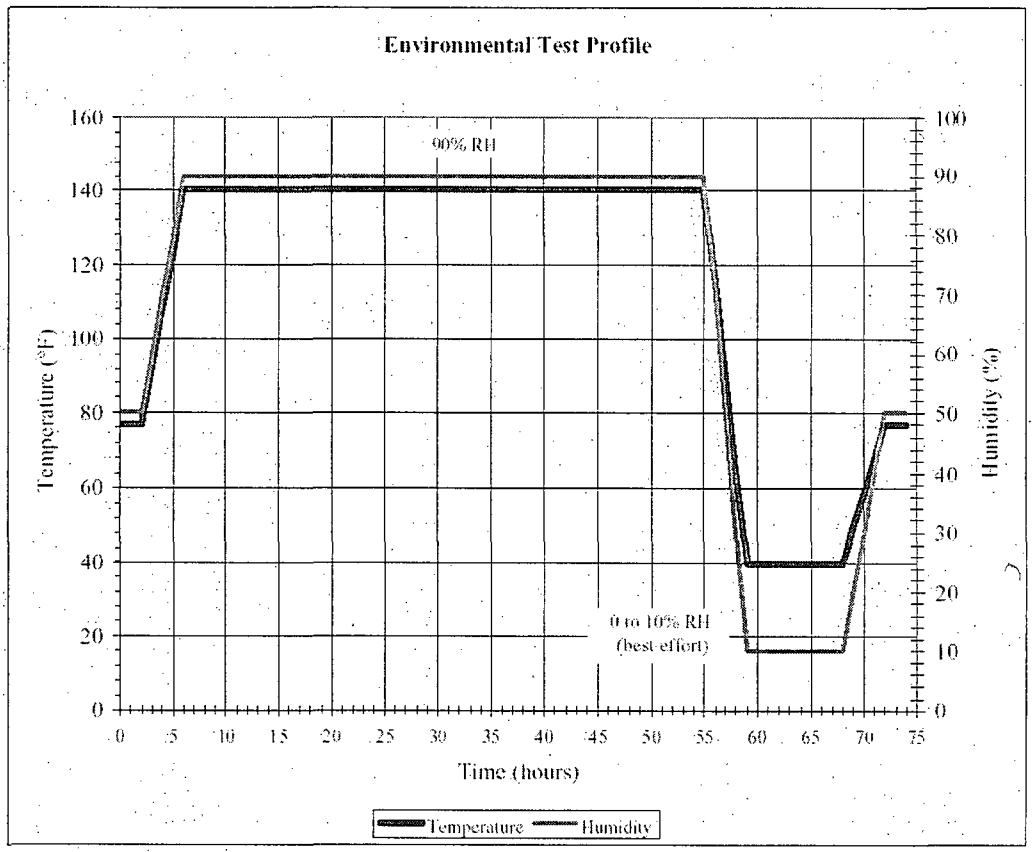

Figure 4-1. Environmental Test Profile

This testing was accomplished by enclosing the Test Specimen in an environmental test chamber in accordance with the HF Controls test procedure at Wyle Laboratories. The Test Specimen was running a Test System Application Program (TSAP) throughout the test period, and its operation was monitored continuously by an automated test controller located outside the test chamber. In addition, comprehensive functional tests were conducted before, after, and at specified points during the stress testing. The results of these tests are used to identify any deterioration in functional performance of the Test Specimen.

5.0 - HFC-6000 ENVIRONMENTAL TEST SETUP DESCRIPTION

The Test Specimen and HPAT both were shipped to Wyle housed in portable cabinet assemblies. The Test Specimen was installed inside the environmental test chamber; the HPAT cabinet and monitoring equipment was located outside the test chamber.

The test specimen was unpacked, inspected, and assembled in the environmental test chamber during the period from 1:00 PM to 5:30 PM on 2/19/04. The following set up was also performed by HFC test personnel:

- Installed rack-to-rack and rack-to-panel cables
- Installed communication wiring between the Test Specimen and the HPAT
- Mounted I/O cables to the connectors on the back of each rack.
- Routed I/O cable from the environmental test chamber to the HPAT.
- Routed power cables from the ac power source to the Test Specimen.
- Verified I/O cable installation.
- The temperature and humidity sensors were positioned in accordance with TP0404 paragraph 3.5.2.

Spare I/O cards were installed in all unused slots of the test specimen chassis. These cards were powered up and were subjected to the environmental stress conditions, but they were not scanned by the controller. Should a failure have occurred during any phase of qualification test, these spare cards could have been used as immediate replacements without disrupting the overall test.

EPRI TR-107330 paragraph 6.3.3 requires a static test during the environmental stress test consisting of the following:

- A minimum of half of all DO relay channels shall be set on and loaded to their rated current; the remainder of the DO relay channels shall be off.

- All of the AO channels shall be set between 50% and 66% of full scale.

  All of the static DO and AO points were preset as required except those used for automated operability or prudency test.

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6.0 ENVIRONMENTAL TESTING

Figure 5-1 shows the basic testing sequence that was followed for the environmental stress testing. Refer to Wyle Laboratories test report for detailed environmental measurement records.

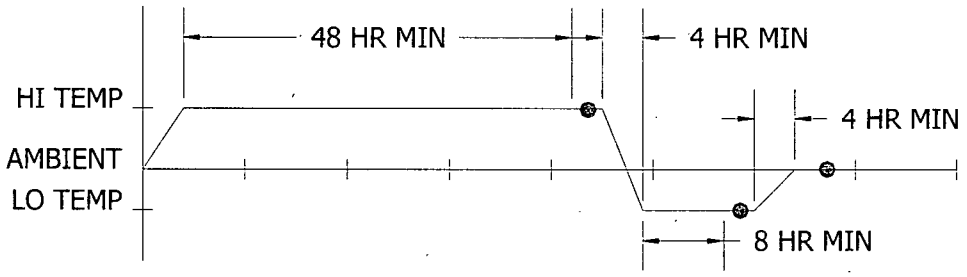

Figure 6-1. Environmental Test Sequence

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Before the environmental testing, a set of pre tests was conducted to verify that the equipment was fully functional. Then the environmental stress test was performed, consisting of 4 major phases:

- 140°F Heat Test: A minimum 48-hour period with the ambient temperature at 140° ± 5° F and a relative humidity (RH) of 90% ± 5% (noncondensing).
- Ramp down period: A transition period of 4 hours during which the ambient temperature was reduced to 40° ± 5° F with 0% to 10% RH (noncondensing).
- 40°F Cold Test: A minimum 8-hour period with the ambient temperature at 40° ± 5° F with 0% to 10% RH (noncondensing).
- Ambient Room Temperature: A transition period of 4 hours during which the test chamber was brought back to ambient room temperature and humidity.

Table 5-1 shows a list of the minimum Operability and Prudency tests needed to be conducted during each environmental test phase.

Table 6-1. Required Tests for Different Environmental Test Phrases

Environmental Test Phases	HFC Tests
Pre-Environmental Test	BOE, Accuracy, Response, Timer
Environmental Test	
At the end of 140°F and 95% RH	BOE, Accuracy, Response, Timer, Discrete Input, Discrete Output, Communication, Power Quality
At the end of 40°F and 5% RH	Accuracy, Response, Timer, Discrete Input, Discrete Output, Communication
Post Test (room ambient temperature)	BOE, Accuracy, Response, Discrete Input, Discrete Output, Communication, Timer

7.0 TEST EVALUATION

The test results achieved during "baseline testing" are generally the tolerance limits against which the qualification tests (environmental, seismic, etc.) will be evaluated. The problems with test methods, test data, etc will not be revisited in detail in these reports. The focus will only be on any "changes" in system performance attributable to the qualification test environment.

6.1 PRE TESTS

6.1.1 General Descriptions

The purpose of the pretest sequence (TP0404 paragraph 4.1) is to verify that the Test Specimen is fully operational prior to the start of the environmental test. During the pre tests, all of the automated Operability tests were run for a minimum period of 5 minutes. The automated Prudency BOE test was run for 5 minutes. Communication was verified.

6.1.2 Acceptance Criteria

- Preliminary operability and prudency tests results shall remain within the tolerance limits listed in documents TP0402 and TP0403. Any deviation from baseline results established during prequalification testing shall be identified and recorded.

6.1.3 Results

6.1.4 Anomalies

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7.2 ENVIRONMENTAL STRESS TESTS

7.2.1 General Descriptions

The environmental stress tests include a 140°F heat test, a transitional ramp down period, and a 40°F cold test. The operability and prudency tests were conducted at the end of 140°F, at the end of 40°F, and at ambient temperature.

7.2.2 Acceptance Criteria

- Operability test results shall remain within the tolerance limits established during baseline testing. Any deviation from baseline results established during prequalification testing shall be identified and recorded.

- BOE test results shall remain within the tolerance limits established during baseline testing. Any deviation from baseline results established during prequalification testing shall be identified and recorded.

- Static DO channel tests – Neither energized relay channels nor deenergized channels shall exhibit any spurious transitions.

- Static AO channel tests – No AO channel shall change by more than 0.05% from its set value throughout the test period.

- If any alarm condition is detected during the environmental stress test, the alarm state shall not affect overall functional operation of the Test Specimen or TSAP.

- A random failure of any module will not be considered a failure of the environmental test if the control system continues overall functional operation. A failed module may be replaced with a spare module without impacting the integrity of the test. If the replacement module is taken from one of the spare slots of the Test Specimen, no increase in the test period will be required. If the replacement module is not taken from one of the spare slots, then the test period shall be increased by a minimum of 1 hour.

- If liquid condensation forms on the Test Specimen during the transition from one environmental condition to another, the condensation may be removed without impacting the overall test results.

7.2.3 Results

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7.2.4 Anomalies

-

NON-PROPRIETARY

-

NON-PROPRIETARY

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8.0 SUMMARY

The environmental test results show that the overall HFC6000 control system met all acceptance criteria except for the anomalies listed below:

- One of the SBC06 controllers failed during the test, evidently because of a power drop in the Wyle power source. This failure did not impact the tests and underscored the functional capabilities of the redundant architecture of the main Test Specimen controller.
- The indicated temperature values associated with RTD input channels changed during the test because the resistance of the loaded resistors changed with temperature variation.
- Due to loss of data, accuracy of RTD and AI cards was not able to be verified under the environmental stress conditions. Applications requiring these accuracies may need additional project specific testing for confirmation.

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9.0 ABBREVIATIONS AND ACRONYMS

The following abbreviations and acronyms are used in this test report and are unique to the environmental test.

BOE	Burst of Events
HAS	Historical Archiving System
HIFR	Host Interface Remote
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
FPC	Flat Panel Display Controller
SOE	Sequence of Events

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Appendix A

PRE-ENVIRONMENTAL TESTS

A.1 GENERAL

This attachment is to document the results of the Pre-Environmental Operability Tests and Prudency Tests in Section 4.1 of the Environmental Stress Test Procedure TP0404, Rev. C. The acceptance criteria against which the pre results are evaluated are provided in Section 5.0 of the test procedure. The purpose of the preliminary operability and prudency tests is to verify that the system is fully functional. Test results shall remain within the tolerance limits established by the baseline testing, as listed in Attachment A of Baseline Testing Summary Report. Any deviation from baseline results established during prequalification testing will be identified and recorded.

The automated operability and burst of events prudency tests were run three different times (8:57 AM, 9:35 AM, and 11:57 AM) on 2/20/04. During the first two executions of the tests, a hardware problem was detected and then corrected. The final execution of the test was accomplished without problem. The operability tests performed are Accuracy, Response, and Timer tests.

During the test, alarm status was monitored and examined. All alarm states being reported represented known conditions.

A.2 AUTOMATED AI ACCURACY (SECTION 4.1)

AI Accuracy card AI16F in rack 4 slot 5 of the test specimen cabinet exhibited power up problems and was replaced before start of environmental test. Since the baseline criteria were established with the original card and the future tests will be run with the new card, the baseline criteria had to be replaced with results from the new card. Manual testing was not performed with the new card, so the automated test results taken during pre-environmental test were used as the basis for evaluation of future tests. Therefore, the results from this pre-environmental test for AI accuracy were used as the new baseline criteria for evaluating AI accuracy test results during environmental test as well as EMI/RFI tests and any other tests.

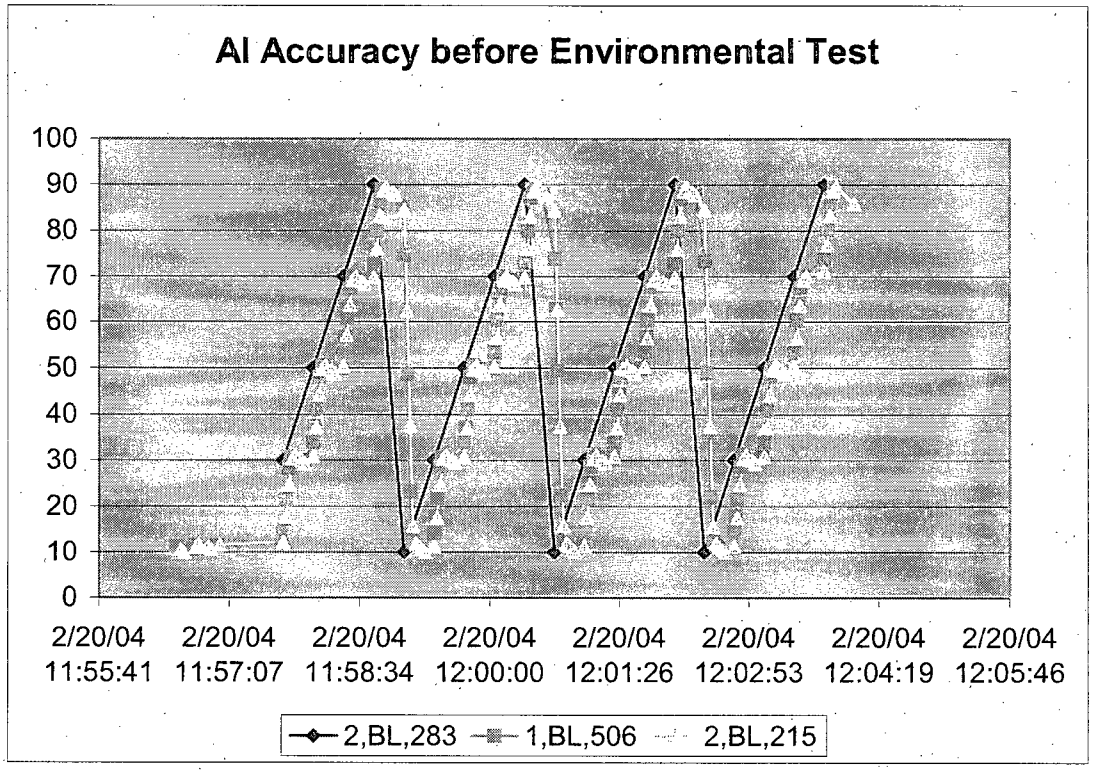


Figure A.2-1. **AI Accuracy Before Environmental Test.**

Table A.2.1. **AI Accuracy before Environmental Test.**

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
1.BL,506					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
2.BL,215					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

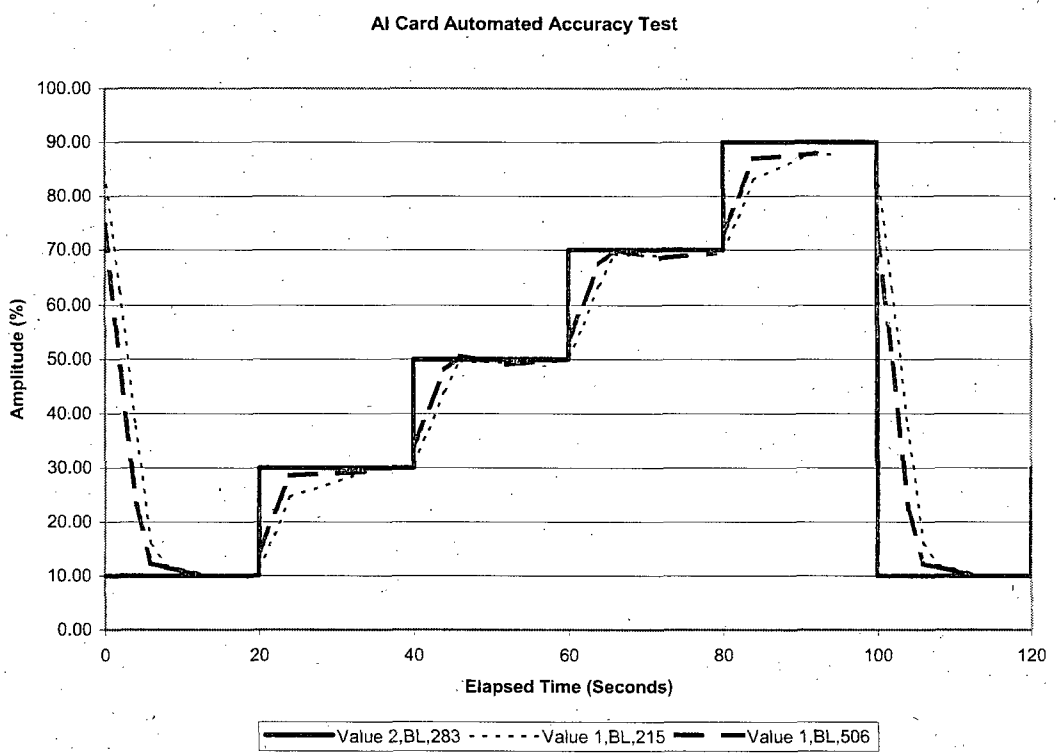


Figure A.2-2. AI Overshoot Pattern.

Table A.2.2. AI Overshoot Pattern.

Tag Name	Time Stamp	Value	Delay
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			

Tag Name	Time Stamp	Value	Delay
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			
1,BL,506			

A.3 AUTOMATED AO ACCURACY (SECTION 4.1)

Table A.3.1. AO Accuracy Test – Pre-Qualification.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
2,BL,211					

The following table and chart shows the automated AO accuracy testing results during pre-environmental phase. These test results are within the baseline tolerance limits.

Table A.3.2. AO Accuracy Test – Pre-Environmental.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
2,BL,211					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

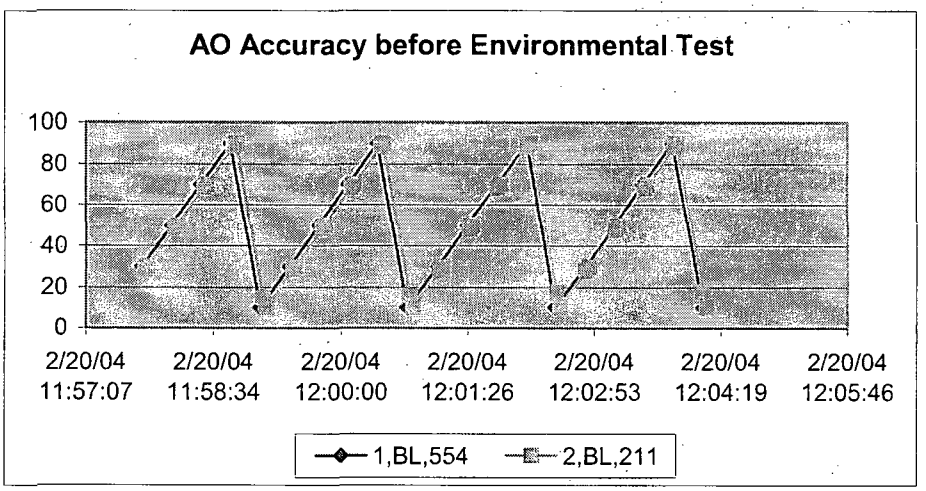


Figure A.3-1. AO Accuracy before Environmental Test.

A.4 RTD ACCURACY (SECTION 4.1)

Table A.4.1. RTD at Pre-Qualification.

Tag Name	Expected Value (%)	HAS Logged Data (%)
1,BL,10		
1,BL,528		
1,BL,546		
1,BL,548		

Table A.4.2. RTD at Pre-Environmental.

Tag Name	Time Stamp	Value (%)	Description
1,BL,10			
1,BL,528			
1,BL,546			
1,BL,548			

A.5 DIGITAL RESPONSE TIME TEST (SECTION 4.1)

A.6 TSAP ANALOG RESPONSE TIME TEST (SECTION 4.1)

A.7 COMMUNICATION TEST (SECTION 4.1)

A.8 TIMER TEST (SECTION 4.1)

A.9 DIGITAL BOE TEST

The baseline testing results are as follows:

- Every transition was detected.
- Each transition occurred within 1.0 ± 0.15 sec.

Table A.9.1. Digital BOE Transitions in the Pre-Environmental Stress Test.

Time Stamp			4,DI,30	4,DI,29	4,DI,28	4,DI,27	4,DI,26	4,DI,25	4,DI,24
H	M	S							
8	3	18							
8	4	52							
Total Number of Transitions									
Total Number of Contact Bounce									
Total Number of Anomalies									

A.10 ANALOG BOE TEST

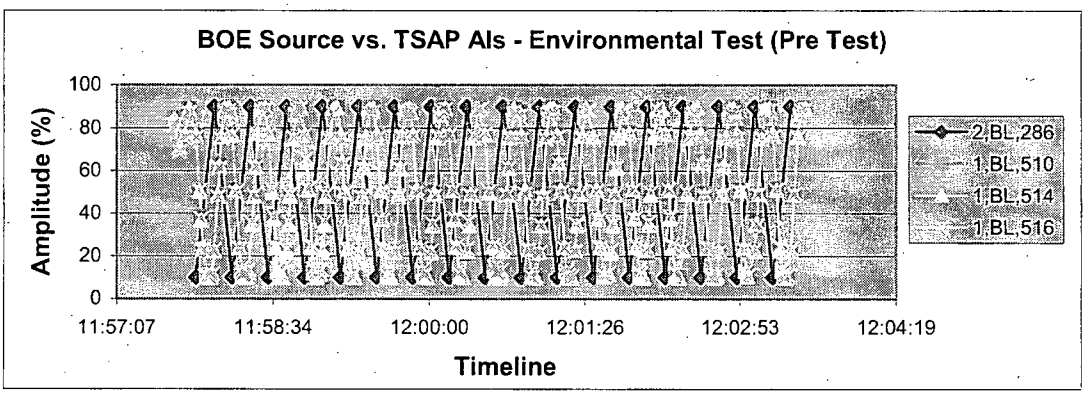


Figure A.10-1. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 in the Pre Environmental Test.

Table A.10-1. TSAP AI Channel Readings and Deviations from BOE Source Signal in Pre Environmental Test.

	1,AI,882 (1,BL,510)		1,AI,884 (1,BL,514)		1,AI,901 (1,BL,516)	
	Test 1	Test 2	Test 1	Test 2	Test 1	Test 2
10% Measurement						
10% Deviations						
Num of Measurements						
90% Measurement						
90% Deviations						
Num of Measurements						

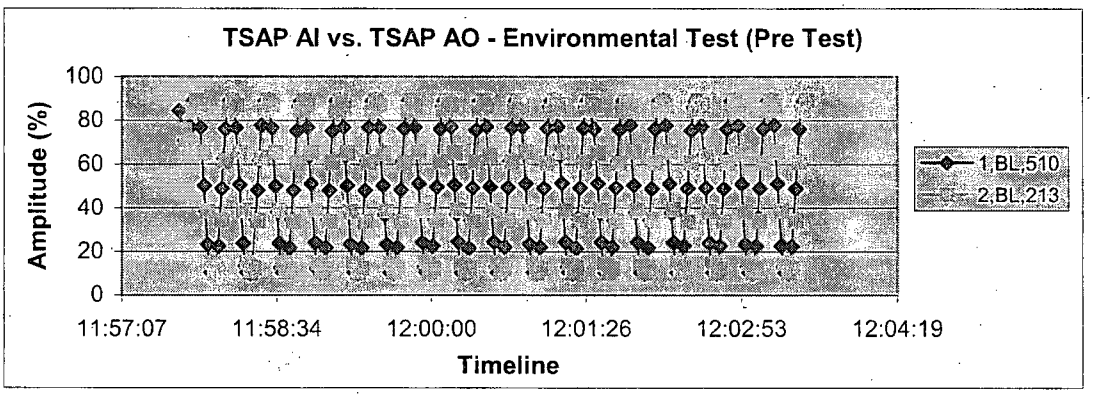


Figure A.10-2. Logged TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) in the Pre Environmental Test.

Table A.10-2. TSAP AOs and the Corresponding TSAP AIs in Remote1 in the Pre Environmental Test.

	1,AI,882 (1,BL,510)	1,AO,922 (2,BL,213)	Deviation (2,BL,213 vs. 1,BL,510)
10% Measurement			
Number of Measurements			
90% Measurement			
Number of Measurements			

HFC-6000 Control System

ERD111 – Control System Qualification Project

Environmental Testing Summary Report

Appendix B

Environmental Stress Test and Post Tests Operability Tests

B.1 GENERAL

This attachment is to document the results of the Operability tests and Prudency tests during and after Environmental Stress Test as stated in Section 4.2 of the Environmental Stress Test Procedure TP0404, Rev. C. The acceptance criteria against which the test results are evaluated are provided in Section 5.0 of the test procedure.

The purpose of the Operability tests and Prudency tests during and after Environmental stress is to verify that system performance was not impacted unacceptably by the elevated temperature, cold temperature, or transition from one temperature to another. Test results shall remain within the tolerance limits established by the baseline testing, as listed in Attachment A of Baseline Testing Summary Report as updated by the attached Pre-Environmental Tests. Any deviation from these established baseline results will be identified and recorded.

The door of the environmental chamber was closed at 1:00 PM on 2/20/04 to start ramp up to the elevated temperature and humidity conditions. The environmental stress test was run at Wyle Laboratories during the period from 1:00 PM on February 20, 2004 through 5:00 PM on February 24, 2004.

The operability tests and prudency tests were conducted at the end of 140°F, at the end of 40°F, and at ambient temperature. The tests include Accuracy, Response, Timer, Discrete Input, Discrete Output, Communication, and Power Quality, digital BOE and analog BOE tests. The requirement for which tests were to be run during each phase of the test is listed in Table 6-1.

No Operability tests were required for the ramping down period. However, during that period, Wyle's power cord breaker that provided power source to the test specimen tripped several times. This is not a failure of Test Specimen equipment. However, as a result of the power cord breaker trip, the entire Test Specimen was powered down. Therefore, additional tests were conducted to demonstrate that the system was restored to full function after power up. The test data for these tests are also evaluated in this appendix.

The post-environmental tests were performed after the environmental chamber was brought back to ambient temperature and humidity. The purpose for conducting the Operability tests and Prudency tests during post-environmental tests period is to verify that the system performance was not impacted after the environmental stress applied to the system. Test results shall remain within the tolerance limits established by the baseline testing as listed in Attachment A of Baseline Testing Summary Report and updated by the attached Pre-Environmental Tests. Any deviation from these established baseline results will be identified and recorded.

B.2 AUTOMATED AI ACCURACY (SECTION 4.2)

B.2.1 At the End of 140°F

Table B.2.1. AI Accuracy at the end of 140°F.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
1,BL,506			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
2,BL,215					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

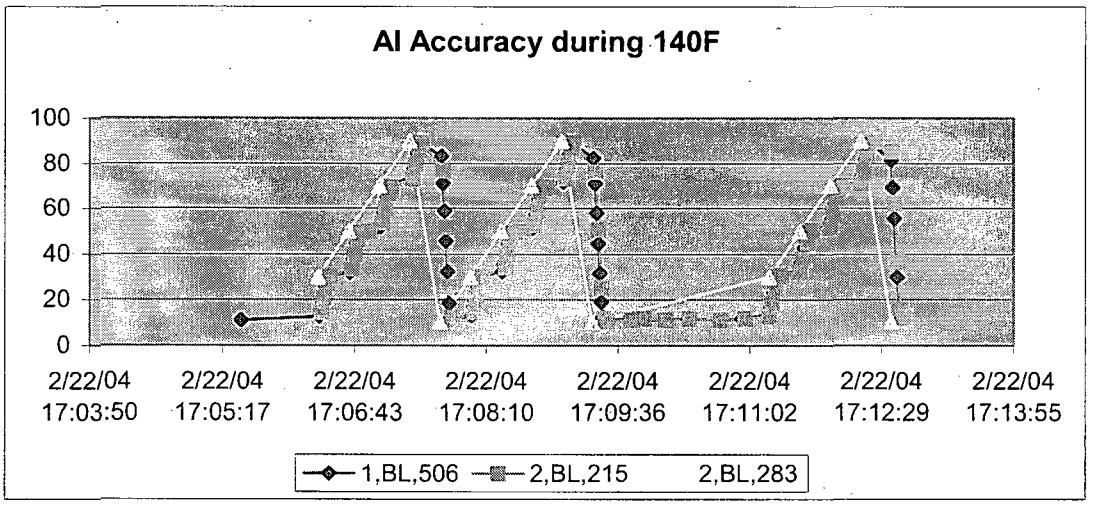


Figure B.2-1. AI Accuracy at the end of 140°F.

B.2.2 During Ramping Down Period

The following charts and tables show AI accuracy tests performed during the ramp down period after Wyle's power cord breaker trips. The logged data was within the tolerance limits.

Table B.2.2. AI Accuracy Test during Ramping Down.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
1,BL,506			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
2,BL,215					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

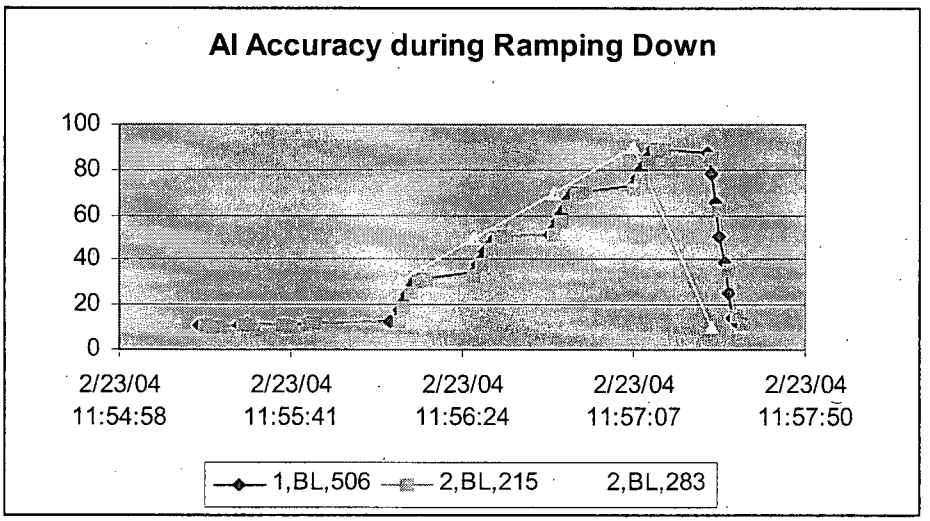


Figure B.2-2. AI Accuracy during Ramping Down.

Table B.2.3. AI Accuracy during Ramping Down 2.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
1,BL,506			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
2,BL,215					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

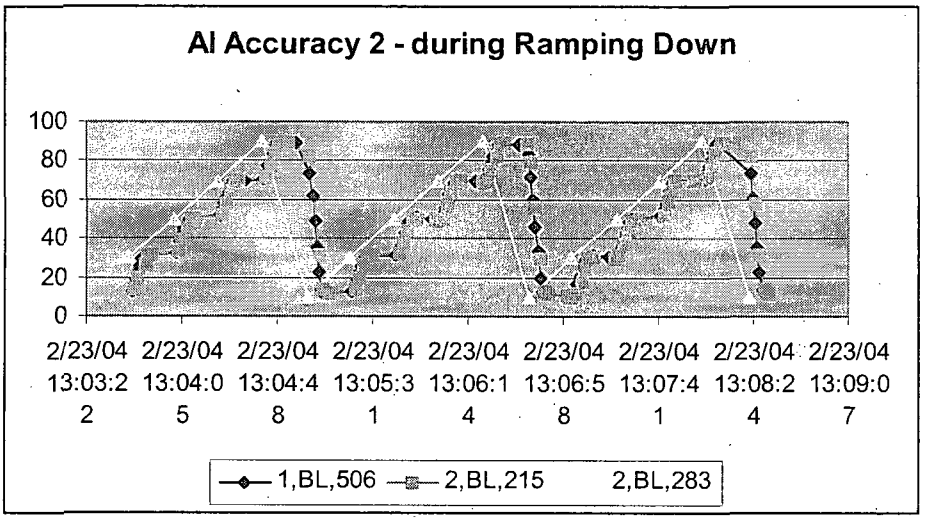


Figure B.2-3. AI Accuracy during Ramping Down.

B.2.3 At the End of 40°F

Table B.2.4. AI Accuracy at the end of 40°F.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
1,BL,506			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
2,BL,215					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

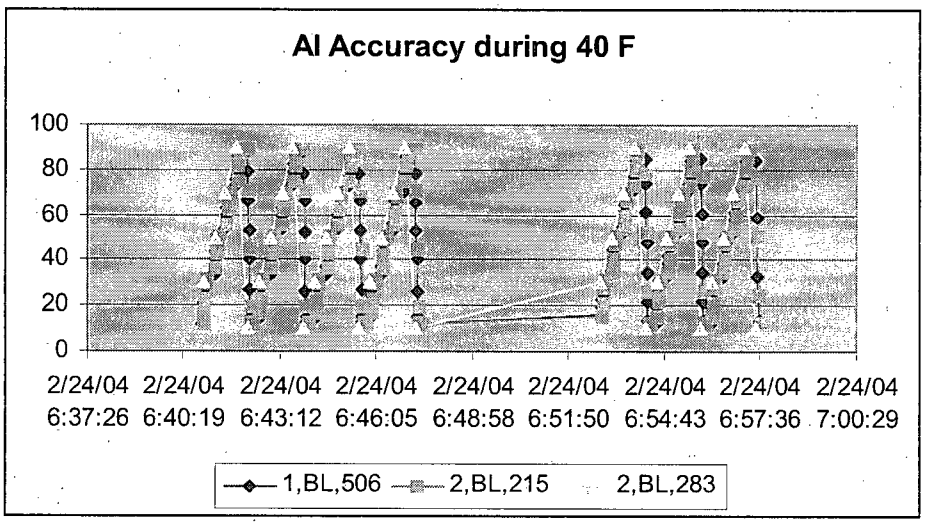


Figure B.2-4. AI Accuracy during 40°F.

B.2.4 At Ambient Room Temperature

The following table and chart shows the automated AI accuracy testing results during post-environmental test phase.

Table B.2.5. AI Accuracy at Ambient Room Temperature.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
1,BL,506			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
2,BL,215					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

Table B.2.6. AI Accuracy at Ambient Room Temperature 2.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
1,BL,506			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
2,BL,215					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

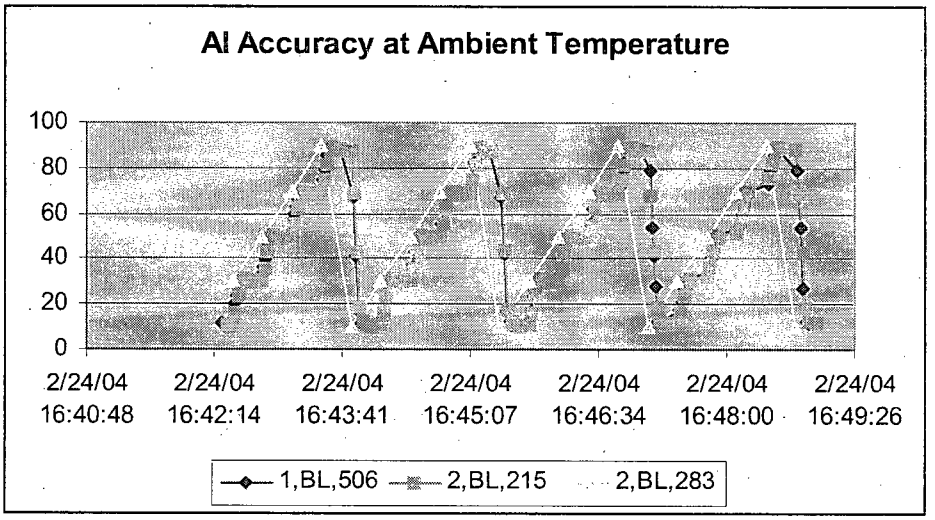


Figure B.2-5. AI Accuracy at Ambient Room Temperature.

B.3 AUTOMATED AO ACCURACY (SECTION 4.2)

The tolerance limits established during pre-qualification test (Attachment A) is ±0.49%.

B.3.1 At the End of 140°F

The following table and chart shows the automated AO accuracy testing results at the end of 140°F heat test phase. The test result 0.22% is within the tolerance limits.

Table B.3.1. AO Accuracy at the end of 140 °F.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
2,BL,211					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

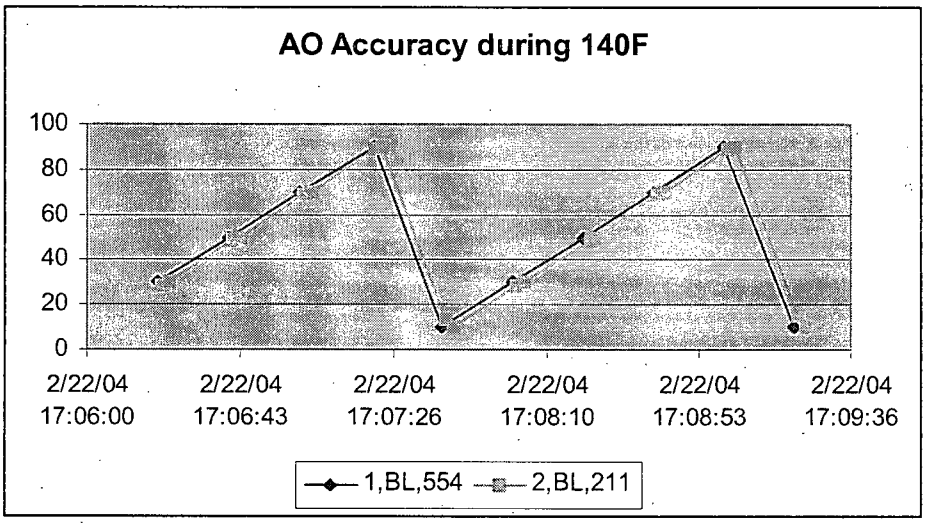


Figure B.3-1. AO Accuracy during 140 °F.

B.3.2 During Ramping Down Period

The following chart and table shows AO accuracy tests performed during the ramp down period after Wyle's power cord trips. The tests were started three times during the temperature ramp down periods; however, the repeated power outages resulted in loss of data for all but one of these tests. The purpose of running this test was to confirm that the Test Specimen had been restored to normal operating condition following these power losses. It was not intended to be part of the scheduled test record.

Table B.3.2. AO Accuracy during Ramping Down.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
2,BL,211					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

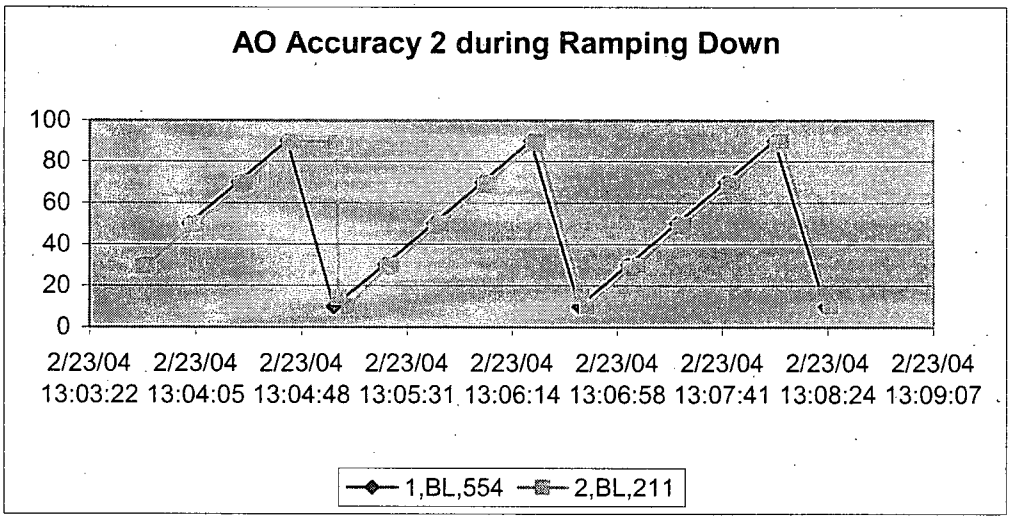


Figure B.3-2. AO Accuracy during Ramping Down.

B.3.3 At the End of 40°F

The following table and chart shows the automated AO accuracy testing results at the end of 40°F cold test phase. The test result 0.20% is within the tolerance limits.

Table B.3.3. AO Accuracy at the end of 40°F.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Deviation (%)
2,BL,211					
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		
			Step Waveform		

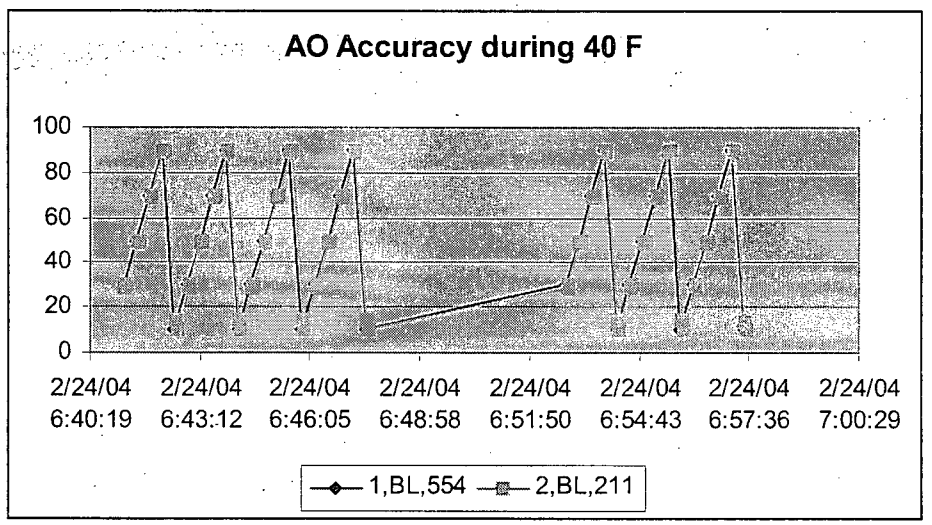


Figure B.3-3. AO Accuracy during 40 °F.

B.3.4 At Ambient Room Temperature

The AO test did not run immediately following the return to ambient temperature because the test signal generator did not operate at that time. However, this test was run and reported as part of the Pre EMI test. The AO accuracy was found to be within the acceptance criteria for that test.

B.4 RTD ACCURACY (SECTION 4.2)

B.4.1 At the End of 140 °F

The following figure shows how the block value related to RTD channels changed during the 48 hours of 140 °F heat test. This change was caused by an increase in the values of the load resisters being used to simulate RTD elements.

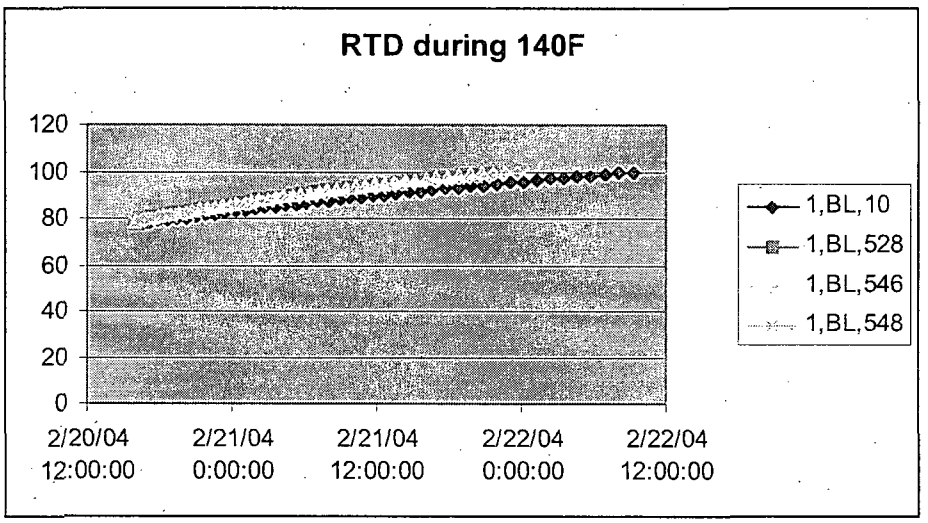


Figure B.4-1. RTD at the end of 140 °F.

Table B.4.1. Resistance Change in Ohms of Loaded Resistors for RTD.

Channel	With Resistor Installed in Terminal Block (Ω)	With Resistor Removed from Terminal Block (Ω)
1		
2		
3		
4		
5		
6		
7		
8		

Table B.4.2. AIC Count Span Changes – RTD Related.

	1,BL,549	1,BL,546	1,BL,528	1,BL,1
Old Count Span				
New Count Span				

B.4.2 During Ramping Down Period

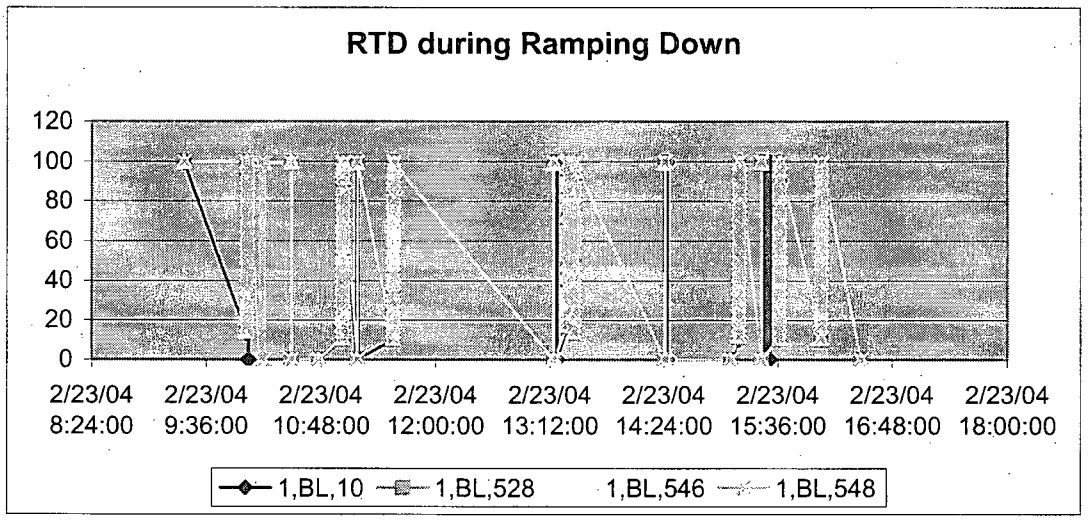


Figure B.4-2. RTD during Ramping Down.

B.4.3 At the End of 40 °F

Table B.4.3. RTD at the end of 40 °F.

Tag Name	Time Stamp	Value	Description
1,BL,10			Simulated RTD Signal
1,BL,528			Simulated RTD Signal
1,BL,546			Simulated RTD Signal
1,BL,548			Output of 1,AI,963

B.4.4 At Ambient Room Temperature

RTD remained the same as in 40 °F degree.

B.5 DIGITAL RESPONSE TIME TEST

The tolerance limits established during baseline testing is as follows:

Table B.5.1. Digital Response during Pre-Qualification.

Measurement Method	Average Response Time (ms)	Standard Deviation (ms)	Comments
Direct Response Time from 1,DI,628 to 2,DI,232			Measures input to output
Discrete I/O 7 Channel Pattern			Measure equation cycle time

B.5.1 At the End of 140 °F

The following table shows digital response time test results for the Environmental Stress Test. The averaged digital response time results from the environmental tests are presented in this table.

Table B.5.2. Digital Response at the end of 140 °F.

Test	(4,DI,16-4,DI,8)	(4,DI,3-4,DI,2)	(4,DI,4-4,DI,3)	(4,DI,5-4,DI,4)	(4,DI,6-4,DI,5)	(4,DI,7-4,DI,6)	(4,DI,1-4,DI,7)
Pre Qualification							
140 °F							
40 °F							
Ambient							

The following figure shows the distribution of digital response time at the end of 140 °F heat test.

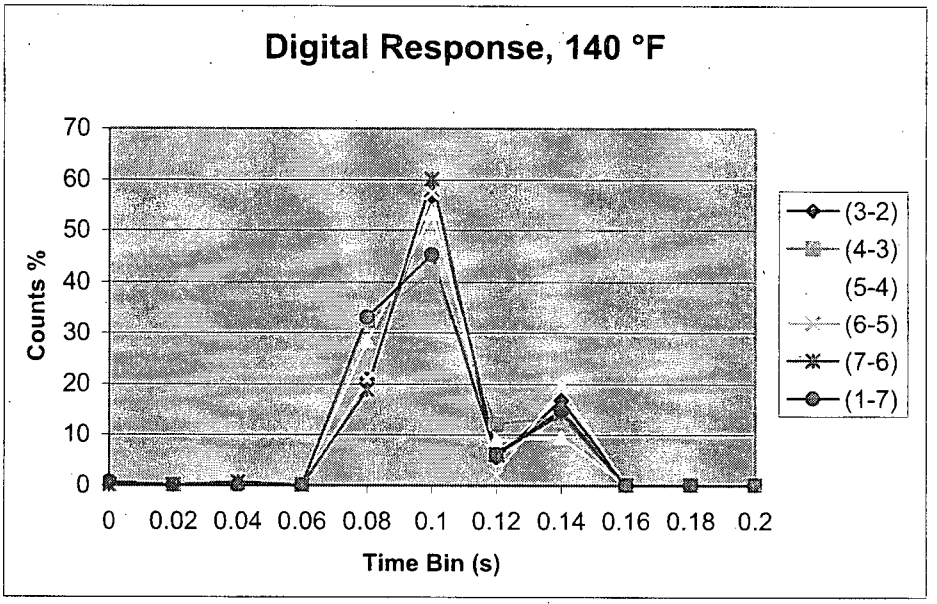


Figure B.5-1. Digital Response at the end of 140 °F.

B.5.2 At the End of 40 °F

The following figure shows the distribution of digital response time at the end of 40°F cold test.

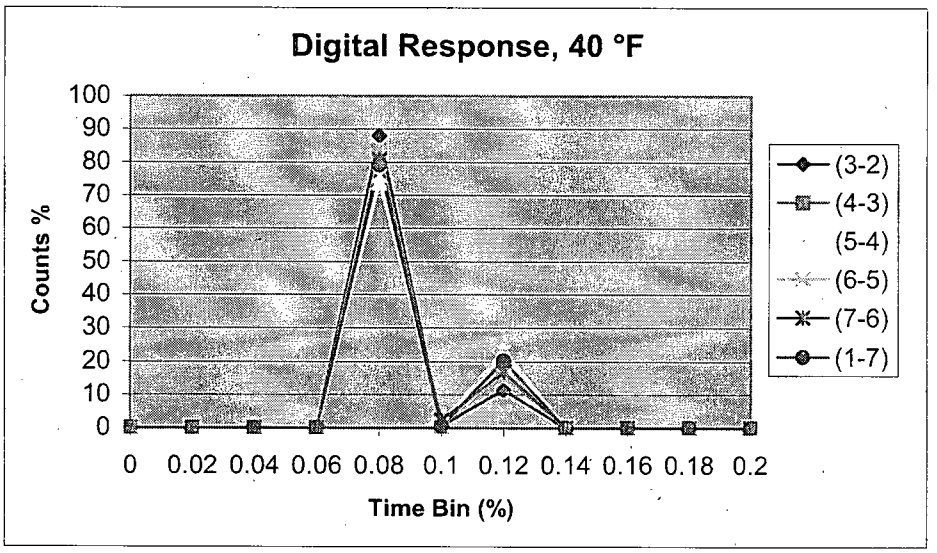


Figure B.5-2. Digital Response Time at 40 °F

B.5.3 At Ambient Room Temperature

The following chart shows the distribution of digital response time during the post environmental test.

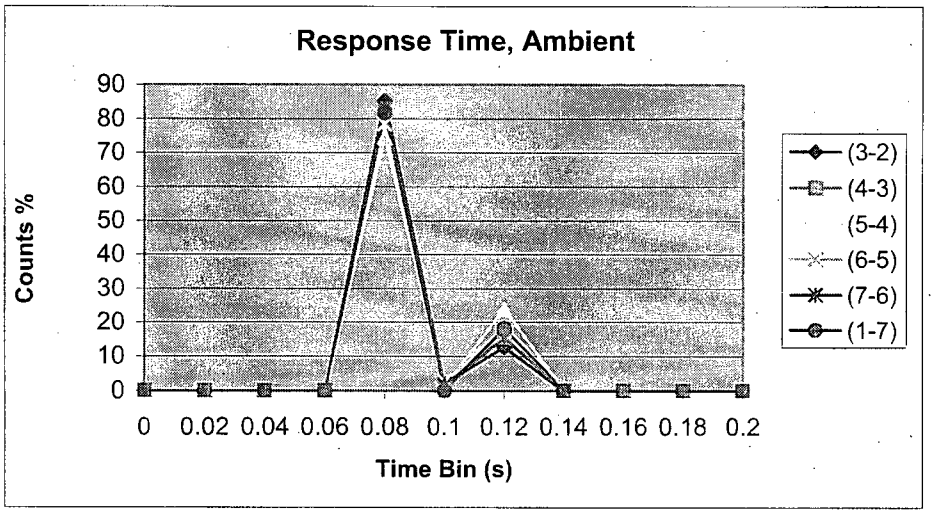


Figure B.5-3. Digital Response Time at Ambient Room Temperature.

Conclusion: The digital response results met the acceptance criteria.

B.6 ANALOG RESPONSE TIME TEST

Table B.6-1 and B.6-2 show baseline testing results for the analog response time test. Half of the data necessary for calculating the response time was not preserved because the SOE data for the output transition from the DO signal was not preserved. However, the analog value data in the TSAP algorithm was preserved and provides a basis of comparison with the baseline data. The value of this data is to indicate if there are any large variations in the processing characteristics of the analog input card and the TSAP due to thermal stress.

Table B.6.1. Analog Response Time Test Result – Prequalification.

Average period of trip waveform:	20.005 seconds		
Average reset period		Average set period	
AVERAGE DEVIATION FROM THE MEAN		Average deviation from the mean	

Table B.6.2. Equation Interpreter Processing Cycles.

Total No. of cycles logged:			
Maximum No.		Minimum cycle time	
Minimum No.		Maximum cycle time	
Average No.		Average cycle time	
Deviation from the mean		Deviation from the mean	

B.6.1 At the End of 140 °F

The operability and prudency tests for the high temperature phase of the environmental test were run from 5:00 PM to 9:00 PM of 2/22/04 after completion of the high temperature and humidity period. The analog response time test was run as part of the other automated tests and then as a background test for the power quality test. Table B.6-3 summarizes the logged results for both of these tests with 1,DO,401 Signal Transition Values.

Table B.6.3. Analog Response at 140 °F.

	Reset Period (s)	Set Period (s)	Total Period (s)
Average			
Deviation			

B.6.2 At the End of 40 °F

According to the master test plan and the Environmental Stress Test Procedure (TP0404), the automated operability tests were to be run after the test specimen had been in the low temperature and humidity environment for a minimum period of 8 hours. However, the test specimen experienced repeated power problems due to tripping of the Wyle power source during the ramp down interval, which extended through the entire day of 2/23/04. Consequently, the automated analog response time tests were actually run three times: once at the end of the ramp down period, and twice the next day before the start of the ramp back up to ambient temperature and humidity. Table B.6-4 presents the results for both executions of the analog response time test for comparison.

Table B.6.4. Analog Response Time Test at 40 °F.

Test		Reset Period (s)	Set Period (s)	Total Period (s)
End of Ramp Down (4:30 PM 2/23/04)	Average			
	Deviation			
End of Low Temperature Period (7:00 AM 2/24/04)	Average			
	Deviation			
End of Low Temperature Period (10:00 AM 2/24/04)	Average			
	Deviation			

B.6.3 At Ambient Room Temperature

The post test was conducted following a 4-hour ramp up to ambient temperature and an additional hour at ambient for system stabilization. The table below lists the results obtained during this period of testing.

Table B.6.5. Analog Response Time at Ambient Room Temperature.

	Reset Period (s)	Set Period (s)	Total Period (s)
Average			
Deviation			

B.6.4 Conclusion

Table B.6.6 below lists the baseline results for the automated analog response time test and the percentage deviation observed during the present test. No large variations are observed in this table.

Table B.6.6. Comparison of Analog Response Time Test Results.

	Baseline Reading (s)	Deviation from Baseline Measurements (%)					
		High Temperature	Power Quality	Low Temperature			Post Test
Set Period							
Reset Period							
Total Period							

B.7 DISCRETE INPUT OPERABILITY TEST

These tests were conducted through various environmental conditions to evaluate the discrete input operability. The tests were performed at 140° F, at 40° F, at ambient temperature, and after seismic stresses.

Each channel cycled the input voltage a total of three times. The acceptance criteria are as follows:

- The DI set voltage level is guaranteed at 20 VDC.
- The maximum input voltage is guaranteed to be 53 VDC.
- The guaranteed dropout voltage is 12 to 15 VDC.

The test results are provided in the following tables.

Table B.7.1. Discrete Input Test at 140 °F.

Test	Card Type Under Test											
	DI16I				DC34				DC33			
	1	2	3	Average	1	2	3	Average	1	2	3	Average
Set Voltage Threshold (V)												
Maximum Input Voltage (V)												
Dropout Voltage (V)												

Table B.7.2. Discrete Input at 40 °F.

Test	Card Type Under Test											
	DI16I				DC34				DC33			
	1	2	3	Average	1	2	3	Average	1	2	3	Average
Set Voltage Threshold (V)												
Maximum Input Voltage (V)												
Dropout Voltage (V)												

Table B.7.3. Discrete Input at Ambient Room Temperature.

Test	Card Type Under Test											
	DI16I				DC34				DC33			
	1	2	3	Average	1	2	3	Average	1	2	3	Average
Set Voltage Threshold (V)												
Maximum Input Voltage (V)												
Dropout Voltage (V)												

The following graphs show the Set Voltage Threshold and the Dropout Voltage:

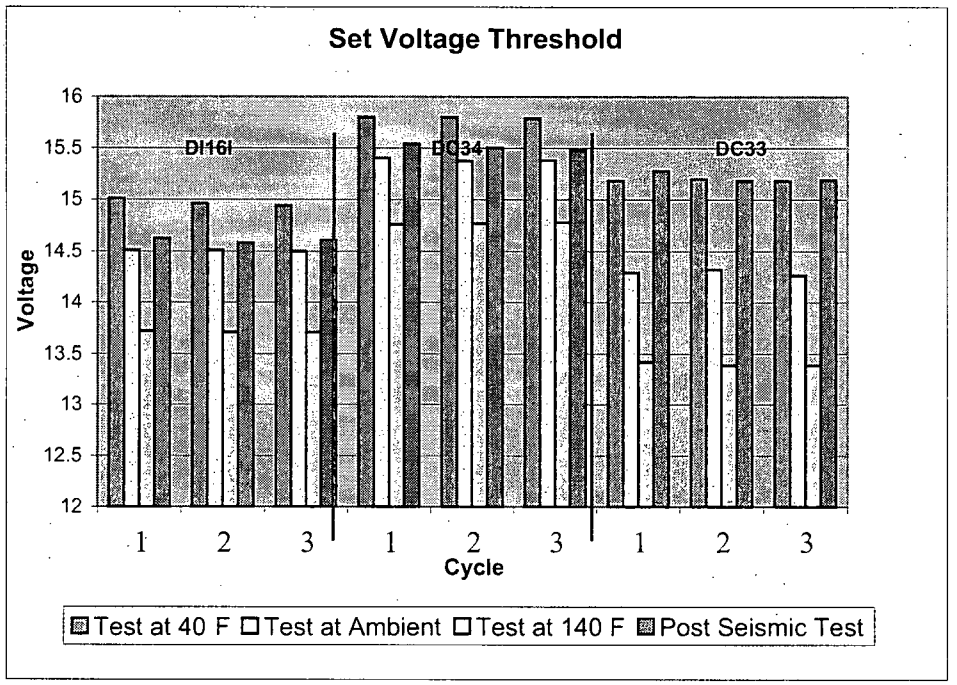


Figure B.7-1. Comparison of Test Results - Set Voltage Threshold.

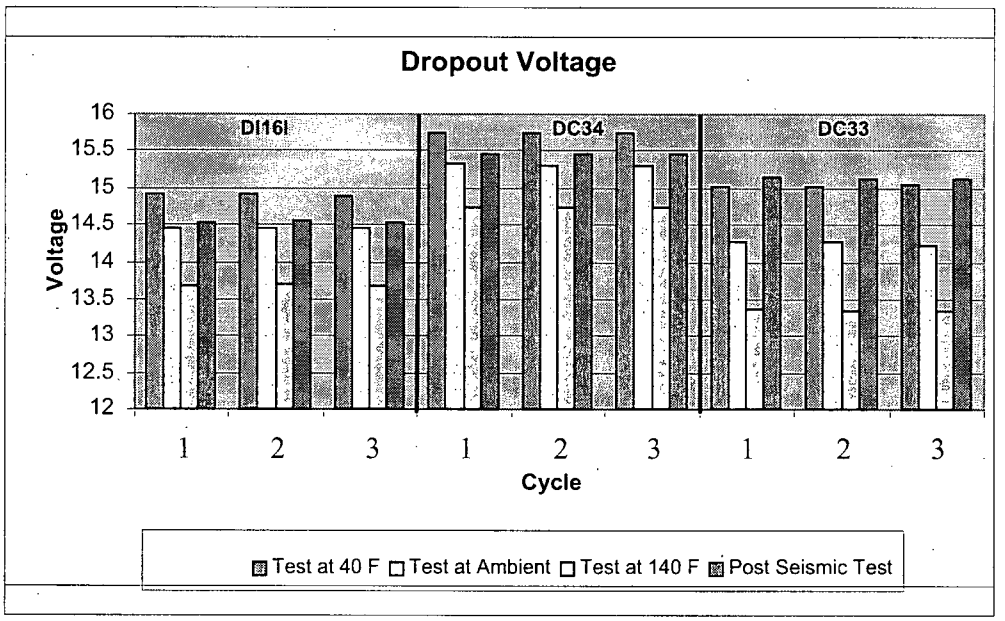


Figure B.7-2. Comparison of Test Results – Dropout Voltage

The DI channels met all of the acceptance criteria for the set voltage level, dropout voltage, and the maximum input voltage through all of the environmental stress. The set voltage was always less than 20 Vdc and the dropout always occurred before the 12 Vdc minimum regardless of the temperature. There was no significant change in the DI channel operation as a result of the environmental stresses. The deviations noted reflect changes in resistance characteristics with temperature. All such changes were within acceptable limits.

B.8 DISCRETE OUTPUT OPERABILITY TEST

The discrete output operability test demonstrates the capability of each type of discrete output channel to operate within its specified range of loading conditions. In order to accomplish this, the channel under test was energized while connected to a simulated field load that imposes maximum loading on the channel. The test demonstrates the capability for individual channels to sustain maximum loading conditions without failure and without affecting operation of adjacent channels. The discrete output operability test was conducted while the system was at 40° F, 140° F, and ambient temperature.

B.8.1 Relay DO Channel Operability Test (Section 4.4.1)

The operability test of the 48 VDC relay DO channels was conducted on a selected HFC-DO8J module. Table B.8-1 lists the results of the measurements taken.

Table B.8.1. DO Channels During Environmental Temperature Test.

Test	Temperature	Channel Tested				Average	Each Channel Switches Under Load
		1	2	4	5		
Contact Resistance (Ω)	140 °F						
	40 °F						
	Ambient						
Test Load Applied (Amps)	140 °F						
	40 °F						
	Ambient						

The relays for the DO channels were specified to operate at 5 Amps at 30 VDC for resistive load. Throughout all testing, the DO channels remained operational with a maximum current load above 9 A at 48 VDC, exceeding the specified requirement. Relay performance and contact characteristics are not significantly impacted by thermal stress within the limits of this test.

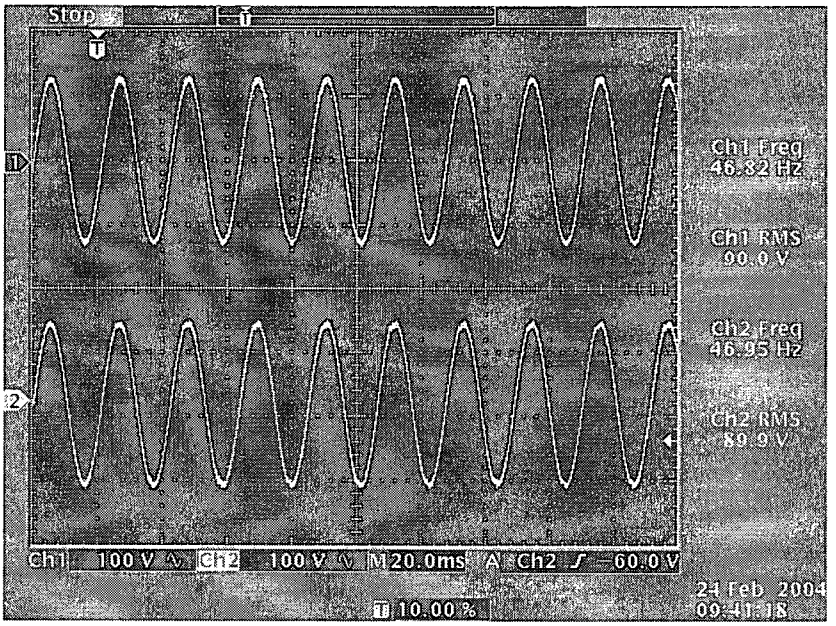
B.8.2 120 VAC DO Channel Operability (Section 4.4.2)

The values in the table below record the resistance of the external set and reset coils connected to the 120 VAC DO channels of the HFC-DC33 selected for test. This relay was not physically located inside the environmental chamber.

Table B.8.2. DC33 Set and Reset Coil Resistance.

Test	Set Coil Resistance (Ω)	Reset Coil Resistance (Ω)
40 °F		
140 °F		
Ambient Temperature		
Average		

The following figures are examples of the screen captures of the output response signal across the set and reset coils. Values were taken from these screen captures to produce the tabulated results. It should be noted that values obtained from screen captures establish bounds but cannot be considered precise.

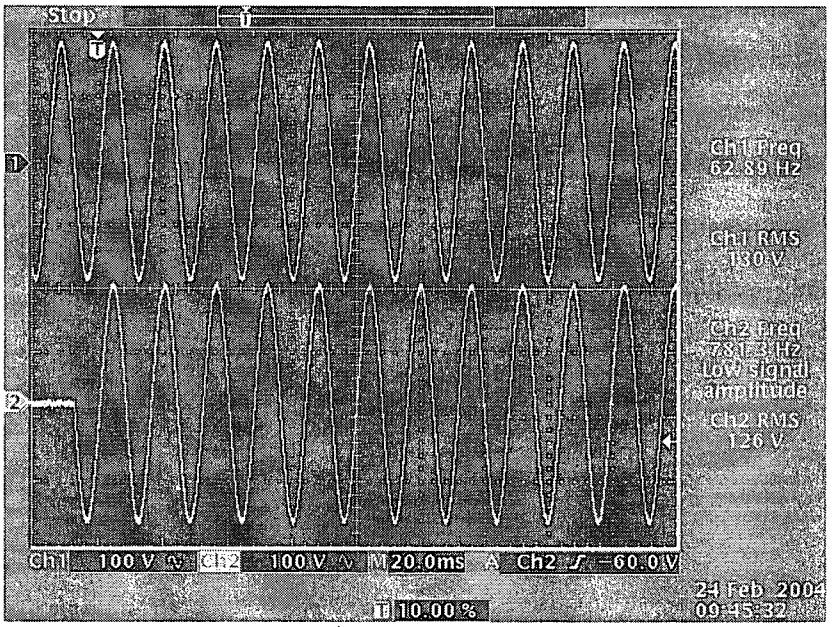


90.0 Vrms

89.9 Vrms

Figure B.8-1. DC33 40 °F Test at Set Coil with Input Voltage Set to 90 VAC at 47 Hz.

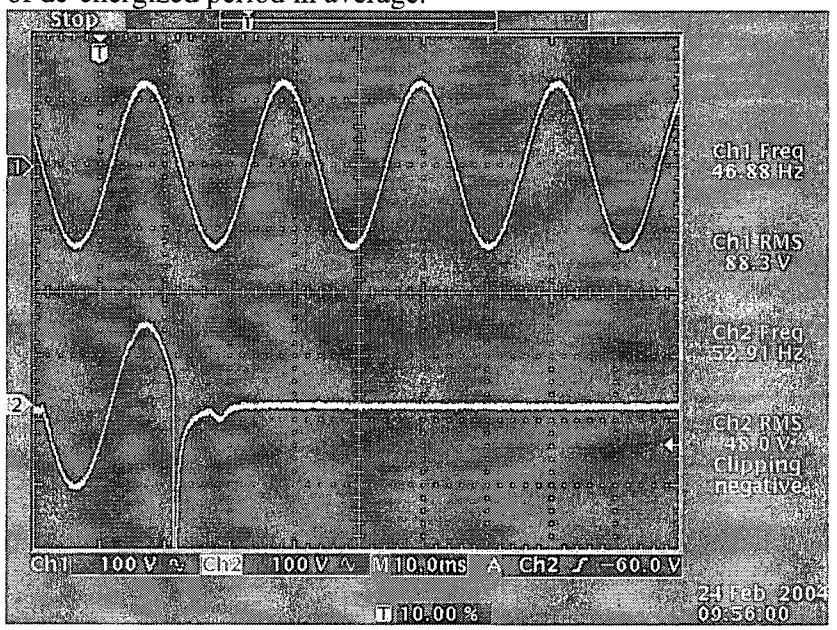
130 V



127.26 V

Figure B.8-2. DC33 40 °F Test at Set Coil with Input Voltage Set to 130 VAC at 63 Hz.

For 127.26 waveform, note that the indicated voltage is too low because it includes part of de-energized period in average.



88.3 Vrms

<~20 Vpp >= ~240
88.375 84.84
Reverse EMF > -200 V peak

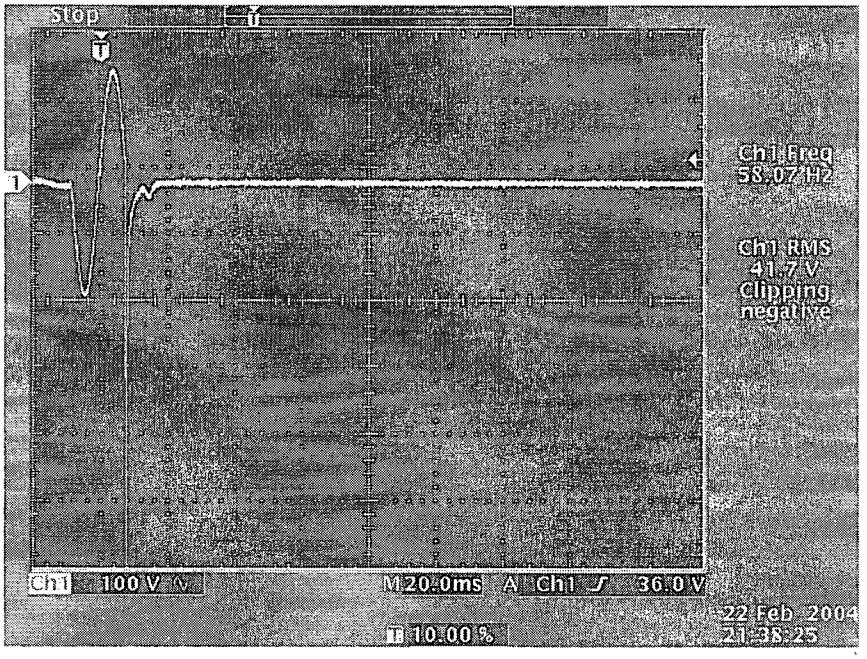
Figure B.8-3. DC33 40 °F Test at Reset Coil with Input Voltage Set to 90 VAC at 47Hz.

Table B.8.3. DC33 Set Coil Output Response Signal During 40 °F Temperature Test.

Set coil and input set to 89.9 VAC at 47 Hz **Off state leak 34.6 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 79.16 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 78.74 Ω)	
On state voltage drop	
Set coil and input set to 130 VAC at 63 Hz **Leakage 64.9 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 79.16 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 78.74 Ω)	
On state voltage drop	
Reverse EMF >200 V (clipped)	

Table B.8.4. DC33 Reset Coil Output Response Signal During 40 °F Temperature Test.

Reset coil and input set to 88.3 VAC at 47 Hz **Off State Leak 15.4 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 439.79 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 439.79 Ω)	
On state voltage drop	
Reset coil and input set to 128 VAC at 63 Hz **No leakage value was measured because probe came disconnected**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 439.79 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 439.79 Ω)	
On state voltage drop	



Reset
Vpp ~ 330
Vrms ~ 116.7

Reverse EMF
>580 V

Figure B.8-4. DC33 140 °F Test at Reset Coil- Input Voltage Set to 120 VAC at 58 Hz.

Table B.8.5. DC33 Set Coil Output Response Signal During 140 °F Test.

Set coil and input voltage not recorded 120 V 60 HZ	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 79.16 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 79.16 Ω)	
On state voltage drop	
Set coil and input voltage not recorded 130 V 63 HZ	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 79.16 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 79.16 Ω)	
On state voltage drop	
No reverse EMF. Off state leak not measured	

Table B.8.6. DC33 Reset Coil Output Response Signal During 140 °F Test.

Reset coil and input voltage not recorded **Off state leakage not measured**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 439.79 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 439.79 Ω)	
On state voltage drop	
Reverse EMF > 580 V	
Reset coil and input voltage not recorded	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 439.79 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 439.79 Ω)	
On state voltage drop	
Reverse EMF >240 V (clipped)	

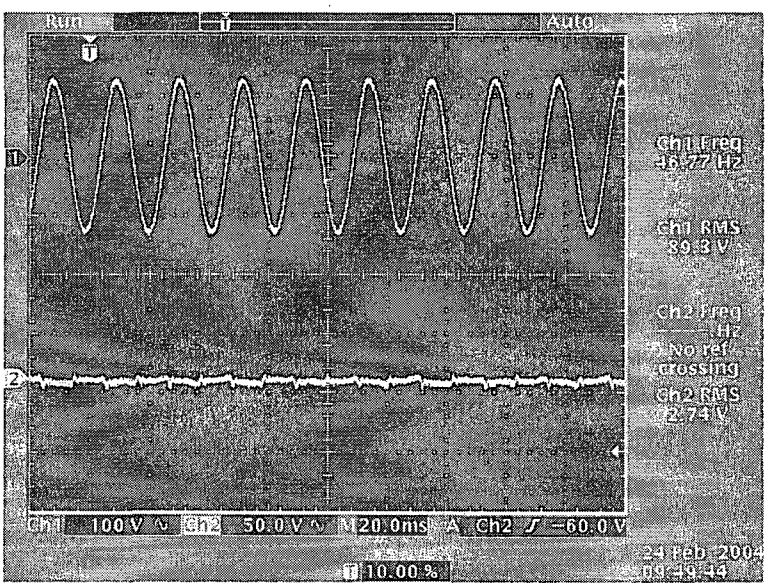
Table B.8.7. DC33 Set Coil Output Response Signal During Ambient Test.

Set coil and input set to 90.6 VAC at 47 Hz **Leakage was not captured**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 79.16 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 79.16 Ω)	
On state voltage drop	
Set coil and input set to 130 VAC at 63 Hz **Leakage 2.00 V 25.3 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 79.16 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 79.16 Ω)	
On state voltage drop	

Table B.8.8. DC33 Reset Coil Output Response Signal During Ambient Test.

Reset coil and input set to 90.4 VAC at 63 Hz **Off state leakage not captured for low voltage**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 439.79 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 439.79 Ω)	
On state voltage drop	
Reset coil and input set to 129 VAC at 63 Hz **Leakage 7.17 V 16.3 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 439.79 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 439.79 Ω)	
On state voltage drop	
Reverse EMF 580 V	

The following shows the off state leakage current:



2.74 Vrms

Figure B.8-5. DC33 40 °F Set Coil Off State Leakage Current- 90 VAC at 47 Hz.

The following test results of the discrete 120 VAC output operability test met the acceptance criteria:

- The output was required to operate at the minimum of 90 VAC at 47 Hz and the maximum of 130 VAC at 63 Hz. The set and reset relay operation was tested

with 90 VAC at 47 Hz and 130 VAC at 63 Hz, which showed it met the acceptance criteria. It was not tested at 140° F at 90 VAC due to power trip problem. If the low voltage capability is necessary for a specific project, a project specific test may need to be run.

- Must support in rush up to 2 A as a minimum. The input voltage was set to 130.32 VAC with the steady state current across the set coil at 2.35 Amps during post seismic testing. Therefore, the card was tested at 0.35 Amps above the minimum in-rush current capacity as required.

- Must support steady state current up to 0.5 A as a minimum. The maximum steady state current of 2.35 Amps was noted to be through the set coil circuit when the input voltage was 130 VAC. This was within the 10 Amp capacity of the DC33 card and demonstrated acceptable performance of the DC33 at this current level. .

- The output was required to have less than 2 VAC on state voltage drop at the maximum voltage and current levels. Measurements did not provide precise values but maximum limits of <3.5 Vrms under all conditions. Based on an evaluation of the components used in the design of the assembly, this on state voltage drop is considered acceptable.

- The off state leakage current which was measured ranged from 15.4 to 64.9 mA. It was not captured in several instances; however, that data was not significant to the overall performance of the module. These values are greater than the acceptance criterion of 2 ma and greater than those sited in baseline report, but are well within the limit (<80% of set current) specified by EPRI. See Section 10 of the Baseline Report for a more detailed explanation of why these results are acceptable.

Conclusions:

Overall the capability of the DC33 module to control a 120 VAC relay was not adversely impacted by temperature stress.

B.8.3 125 VDC DO Channel Test (Section 4.4.3)

The values in the table below were the set and reset coil resistances used to calculate the current levels for the DC34. The average resistance value was used because relay was outside the environmental chamber.

Table B.8.9. DC34 Set and Reset Coil Resistance.

Test	Set Coil Resistance (Ω)	Reset Coil Resistance (Ω)
140 °F		
40 °F		
Ambient Temperature		
Average		

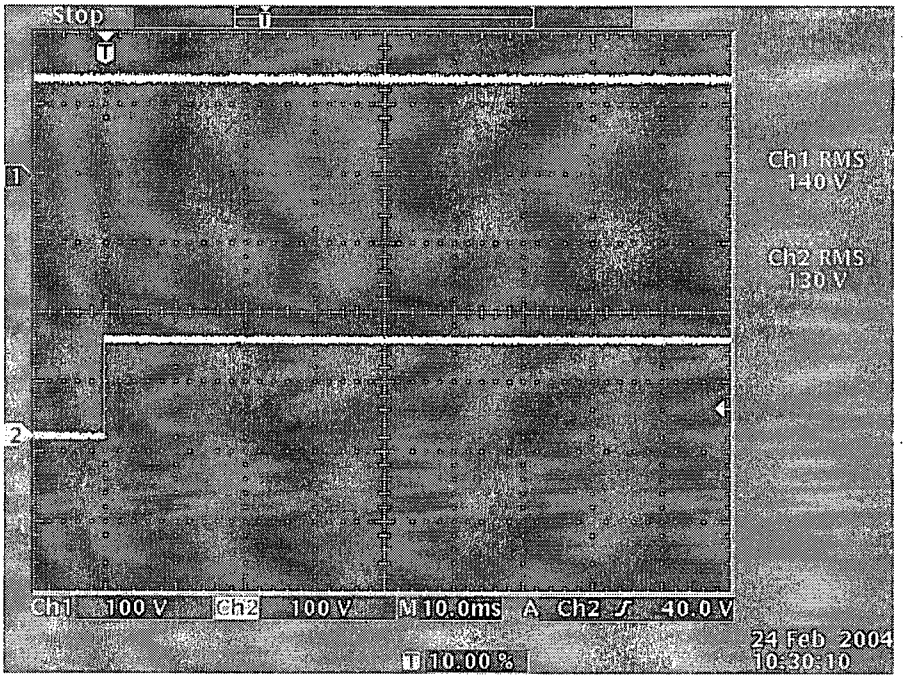
The values in the table were the set and reset coil resistances used to calculate the current levels for the DC33. The following tables provide the results from the oscilloscope screen captures:

Table B.8.10. DC34 Set Coil Output Response Signal During 140 °F Test.

Set coil and input voltage was not recorded	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 1002.7 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 1002.7 Ω)	
On state voltage drop	
Set coil and leakage was not recorded	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 1002.7 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 1002.7 Ω)	
On state voltage drop	

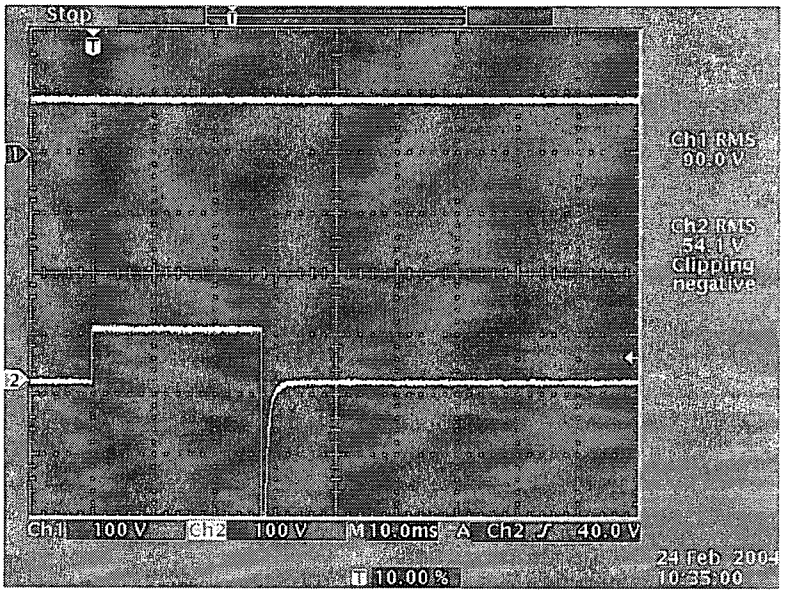
Table B.8.11. DC34 Reset Coil Output Response Signal During 140 °F Test.

Reset coil **Reverse EMF >570 V**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 454.9 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 454.9 Ω)	
On state voltage drop	
Reset coil **Reverse EMF >570 V**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 454.9 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 454.9 Ω)	
On state voltage drop	



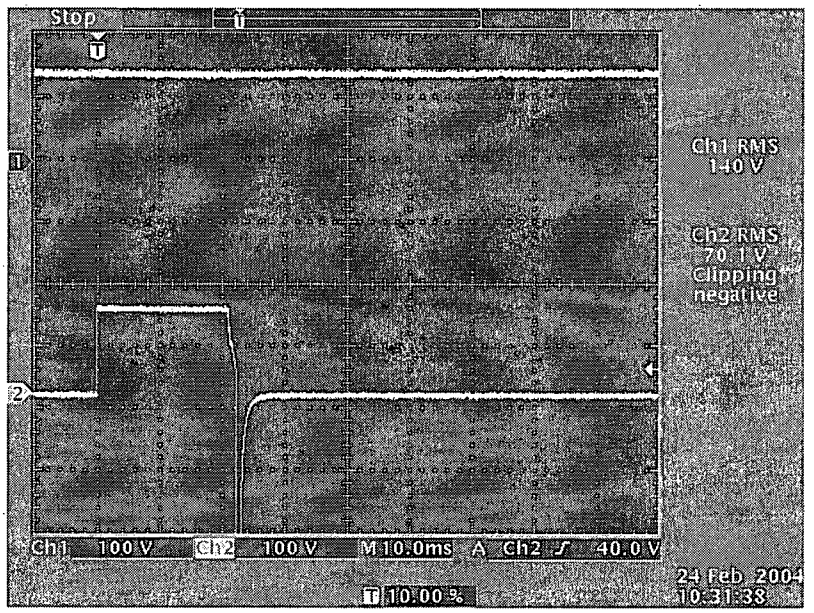
>=135V

Figure B.8-6. DC34 40 °F Test at Set Coil with Input Voltage Set to 140 VDC.



Peak >=89 V
Reverse >200

Figure B.8-7. DC34 40 °F Test at Reset Coil with Input Voltage Set to 90 VDC.



Peak ~ 135V

Reverse EMF >200 V

Figure B.8-8. DC34 40 °F Test at Reset Coil with Input Voltage Set to 140 VDC.

Table B.8.12. DC34 Set Coil Output Response Signal During 40 °F Temperature Test.

Set coil and input set to 89.9 VDC **Off state leakage 1.79 V 1.8 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 1002.7 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 1002.7 Ω)	
On state voltage drop	
Set coil and input set to 140 VDC **Leakage 1.44 V 1.4 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 1002.7 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 1002.7 Ω)	
On state voltage drop	

Table B.8.13. DC34 Reset Coil Output Response Signal During 40 °F Temperature Test.

Reset coil and input set to 90 VDC **Offstate leakage 2.15 V 4.7 mA Reverse EMF >200 V**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 454.9 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 454.9 Ω)	
On state voltage drop	
Reset coil and input set to 140 VDC **Off state leakage 2.17 V 4.8 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 454.9 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 454.9 Ω)	
On state voltage drop	

Table B.8.14. DC34 Set Coil Output Response Signal During Ambient Test.

Set coil and input set to 90.2 VDC **Off state leak 1.32 V 1.3 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 1002.7 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 1002.7 Ω)	
On state voltage drop	
Set coil and input set to 140 VDC **Offstate leak 1.3 V 1.3 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 1004 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 1004 Ω)	
On state voltage drop	

Table B.8.15. DC34 Reset Coil Output Response Signal During Ambient Test.

Reset coil and input set to 89.6 VDC **Reverse EMF >220 V leak 1.62 V 3.56 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 454.9 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 454.9 Ω)	
On state voltage drop	
Reset coil and input set to 140 VDC **Reverse EMF > 220 V leak 1.66 V, 3.65 mA**	
Peak Response signal on activation of solenoid circuit	
Peak in-rush current (resistance= 454.9 Ω)	
Steady-state output	
Maximum steady-state current (resistance= 454.9 Ω)	
On state voltage drop	

The reset coils showed a reverse EMF pulse upon deactivation throughout all of the environmental tests except the test at ambient temperature. Detection of reverse EMF varies with the way the signals were measured. Observation is not significant.

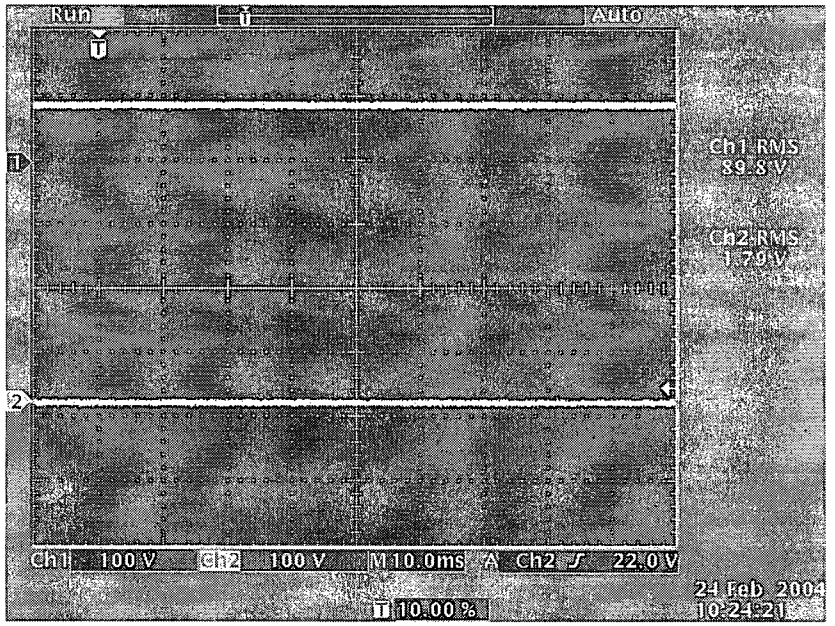


Figure B.8-9. DC34 40 °F Test at Set Coil Off State Leakage Current- 90 VDC.

The following test results of the discrete 125 VDC output operability test met the acceptance criteria:

- The output was required to operate at the minimum of 90 VDC and the maximum of 140 VDC. Test verified acceptable performance over required voltage range.

- The channel was required to support up to 2 A of current as a minimum. Instantaneous current occurred with a reverse EMF of 570 VDC for a current level of 1.25 A. The onboard hardware is rated for 11 A. The interface cabling demonstrated the ability to carry > 9A.

- The channel was required to support a steady state current of 0.5 A as a minimum. The test demonstrated up to 0.3 A. The hardware is rated to 11 A. The interface cabling demonstrated the ability to carry > 9A.

- The output was required to have less than 2 VDC on state voltage drop at the maximum voltage and current levels. For the 140 °F and ambient temperature cases, this criterion was met. For the 40 °F case, the data record confirmed that the results were less than 5 V, but the resolution of the measurement was not fine enough to confirm that the 2 VDC acceptance criterion was met. There was no adverse impact of the potentially higher on state voltage drop at 40 °F because the relay continued normal operation. Since it was not under environmental stress as

the Test Specimen was, the control function continued to operate normally. If this is a critical item for a specific project, a project specific test may need to be run to confirm compliance with the acceptance criterion.

- The results are consistent with the baseline results.

Conclusions:

The capability of the DC34 module to control a 125 VDC was not impacted or degraded by temperature stress.

B.9 COMMUNICATION OPERABILITY

B.9.1 Ramp Down Period

The communication operability test on the ICL was performed manually by checking the ICL error counters over a period of 8 minutes. The following table shows the test results:

- AI4K cards showed errors. These modules consistently reported a station error due to a known internal software error. The software error read a status input incorrectly, resulting in a nuisance alarm which had no other impact on the test results. This error has subsequently been corrected.

- The error counters indicate that all cards for Rack 2 had problems. On the testing log, it says that at 2/23/04 3:30, some loose connectors were found on the rear of the TSAP. They were then pushed back in. (This showed on Wyle's log event 47-55.) After that, rack 2 started communicating as demonstrated by the 40 °F case in Table B.9.2 and subsequent tests. Since the Communication Operability Test was not required to be run during the Ramp Down Period, this problem had no impact on the test results.

Table B.9.1. ICL Error Counters – Ramp Down Period

Station	Card Type	Start Count	End Count	Count Difference	Start Time	Stop Time	Duration	Comments
Remote 1							d-h-m-s	
0	KPD16							
1	KPD16							
3	KPD16							
5	KDI16							
6	KDO8							
7	KDO8							
16	KDI16	13FC	15BA	446				
17	KPD16	1003	1186	387				
19	KDI16	0FAB	10E9	318				
20	KPD16	0FDA	114C	370				
22	KDI16	102D	1197	362				

Station	Card Type	Start Count	End Count	Count Difference	Start Time	Stop Time	Duration	Comments
23	KDO8	0FDD	1143	863				
24	KDO8	0FBB	10D5	830				
25	KDI16	1437	15C5	398				
26	KPD16	FF4	1187	323				
36	KDI16							
37	KDI16							
38	KDO8							
39	KDO8							
40	KDO8							
48	KAIO							
49	KAO8							
50	KAIO							
51	KAIO							
52	KAI16							
53	KAI16							
54	KAO8							
56	KAI8							
57	KAIO							
58	KAI8							
59	KAI8							
60	KAI8							

B.9.2 40 °F Cold Test

For the ICL error counters, only the AI4K card showed errors. The reasons are the same as explained before and can be disregarded.

Table B.9.2. ICL Error Counters at 40 °F.

Station	Card Type	Start Count	End Count	Count Difference	Start Time	Stop Time	Duration	Comments
Remote 1								
0	KPD16							
1	KPD16							
3	KPD16							
5	KDI16							
6	KDO8							
7	KDO8							
16	KDI16							
17	KPD16							
19	KDI16							
20	KPD16							
22	KDI16							
23	KDO8							
24	KDO8							
25	KDI16							

Station	Card Type	Start Count	End Count	Count Difference	Start Time	Stop Time	Duration	Comments
26	KPD16							
36	KDI16							
37	KDI16							
38	KDO8							
39	KDO8							
40	KDO8							
48	KAIO							
49	KAO8							
50	KAIO							
51	KAIO							
52	KAI16							
53	KAI16							
54	KAO8							
56	KAI8							
57	KAIO							
0	KAI8							
0	KAI8							
60	KAI8							

B.9.3 At Ambient Room Temperature

During the Ambient Temperature test, the Communication Operability test was performed at 2/14/04 4:42 for about 5 minutes. The following table shows the ICL error counters at ambient room temperature. Only the AI4K card shows errors. The reasons are the same as explained before and can be disregarded.

Table B.9.3. ICL Error Counters at Ambient Room Temperature.

Station	Card Type	Start Count	End Count	Count Difference	Start Time	Stop Time	Duration	Comments
Remote 1							d-h-m-s	
0	KPD16							
1	KPD16							
3	KPD16							
5	KDI16							
6	KDO8							
7	KDO8							
16	KDI16							
17	KPD16							
19	KDI16							
20	KPD16							
22	KDI16							
23	KDO8							
24	KDO8							
25	KDI16							

Station	Card Type	Start Count	End Count	Count Difference	Start Time	Stop Time	Duration	Comments
26	KPD16							
36	KDI16							
37	KDI16							
38	KDO8							
39	KDO8							
40	KDO8							
48	KAIO							
49	KAO8							
50	KAIO							
51	KAIO							
52	KAI16							
53	KAI16							
54	KAO8							
56	KAI8							
57	KAIO							
0	KAI8							
0	KAI8							
60	KAI8							

B.10 TIMER TEST

The timer function is controlled by the main processor OS. The timers controlled two DO images - that data was transferred via the ICL to a DO8J module, and the resulting signals were routed to the SOE interface via a cable assembly.

Tables B.10.1, B.10.2 and B.10.3 summarize the SOE data for the timer test accumulated during the environmental tests. The parameters listed in the tables are defined as follows:

Preset Value	Set timer interval in application program in seconds
Duration	Measured on/off time in seconds
Duration Deviation	The averaged deviation of the observed timer interval expressed as a percentage value.
Duration Jitter	The averaged difference between successive timer intervals expressed as a percentage value.
Period	Total measured period of signal waveform in seconds
Period Deviation	The averaged deviation of the measured waveform period expressed as a percentage.

Period Jitter The averaged difference of successive periods from the preset value expressed as a percentage.

B.10.1 At the end of 140 °F

The following table shows the result of the Timer test at the end of 140 °F heat test.

Table B.10.1. Timer Test at 140 °F.

		Preset Value	Duration (s)	Duration Deviation (%)	Duration Jitter (%)	Period (s)	Period Deviation (%)	Period Jitter (%)
4,DI,12	ON							
	Number of Measurement							
	OFF							
	Number of Measurement							
4,DI,11	ON							
	Number of Measurement							
	OFF							
	Number of Measurement							

Timer performance remains within the tolerance level identified in the Baseline Testing Summary Report, Section A.12.

B.10.2 At the end of 40°F

The following table shows the result of the Timer test at the end of 40 °F cold test.

Table B.10.2. Timer Test at 40 °F.

		Preset Value	Duration (s)	Duration Deviation (%)	Duration Jitter (%)	Period (s)	Period Deviation (%)	Period Jitter (%)
4,DI,12	ON							
	Number of Measurement							
	OFF							
	Number of Measurement							
4,DI,11	ON							

	Number of Measurement							
	OFF							
	Number of Measurement							

B.10.3 At Ambient Room Temperature

The following table shows the timer test results at Ambient room temperature.

Table B.10.3. Timer Test at Ambient Room Temperature.

		Preset Value	Duration (s)	Duration Deviation (%)	Duration Jitter (%)	Period (s)	Period Deviation (%)	Period Jitter (%)
4,DI,12	ON							
	Number of Measurement							
	OFF							
	Number of Measurement							
4,DI,11	ON							
	Number of Measurement							
	OFF							
	Number of Measurement							

Conclusions:

- No disruption in the timer waveform was observed during any of the environmental tests.
- All timer periods remained within the theoretical tolerance limit established in the baseline report.

B.11 POWER QUALITY TOLERANCE TEST (TP0402 SECTION 4.10)

The power quality tolerance test was not a regular part of the operability test. It was conducted at the end of the high temperature phase of the environmental stress test, and after completion of the SSE seismic test. Execution of this test was not required before, during, or after the other qualification tests.

The Test Specimen being qualified has one set of redundant power supply modules for the HFC-6000 chassis. This test verified the capability of the power supplies to continue providing adequate operating power to the control system under varying conditions of source power quality.

B.11.1 Acceptance Criteria

The acceptance criteria for power quality test is as follows:

- While source power was between 90 to 150 VAC and 57 to 63 Hz, the output voltage level produced by the power supply remained within ±0.1% of its set-point level.
- No power supply dropout alarm occurred while the source power was within the specified range.
- The undervoltage protection tripped the power supply output and the power supply produced a system status alarm.
- The overvoltage protection trips the power supply output and the power supply produces a system status alarm.
- The power supply recovers from overvoltage and undervoltage conditions.

Table B.11.1. Initial Power Module Voltage.

Power Module	Voltage
24-V Module A	24.015 VDC
24-V Module B	24.026 VDC
48-V Module A	48.041 VDC
48-V Module B	48.036 VDC

The power quality test utilized a variable AC power source with an output tolerance of ±1 VAC and ±1 Hz to power up the power supplies. The two output power supplies have a voltage output rating of 24 and 48 VDC. A multimeter was used to monitor the output voltage level produced by each power supply.

Initially, the automated accuracy, response time, and timer operability tests were enabled to provide a minimum set of dynamic operations.

B.11.2 Test Evaluation

The power quality test was performed after the high temperature phase of the environmental stress test. It was started on 8:10 pm and ended at 8:19 pm, 2/22/04. However, the output terminals of the 24 and 48 VDC power supplies were not readily accessible during the environmental testing, and the voltages were not measured. Therefore the first criterion was not evaluated. This is not deemed to be a problem because the scope of testing is within the manufacturer's range of operation for the modules used. If demonstration of proper performance within a system environment is necessary, additional project specific testing may be needed.

The variable AC source was set to 90 VDC at 60 Hz, but after one minute, the power cord circuit breaker tripped because the 11 Amp AC current was too much current for the cord. (The power cord and circuit breaker were not a part to the HFC-6000 system.) This caused the TSAP to power down.

The variable AC source was then set to 250 VAC at 63 Hz. The power cord did not fail and the TSAP continued to function. The system continued to operate properly through the power quality test, except for the brief power interruption due to the trip in the power cord.

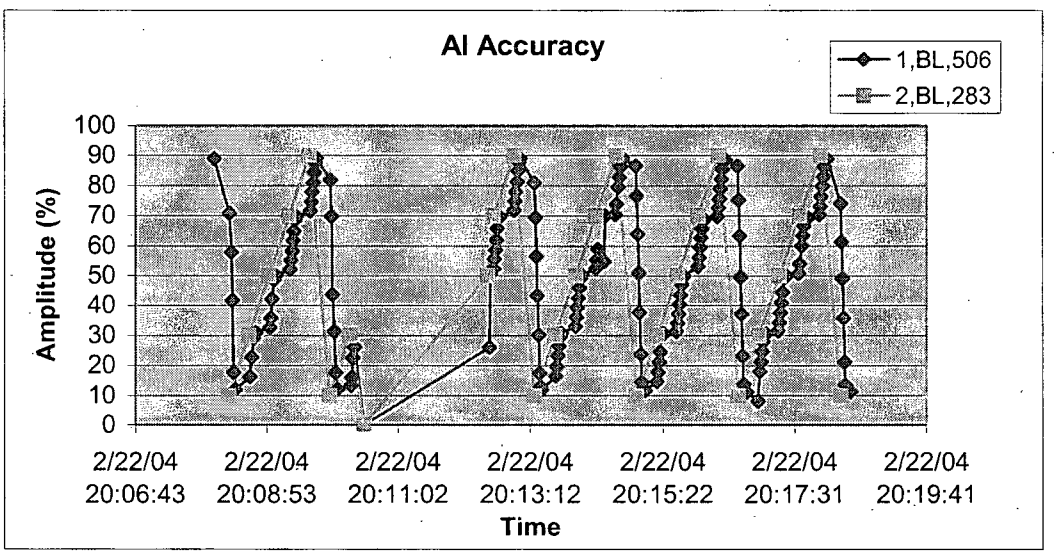


Figure B.11-1. AI Accuracy Waveforms during Power Quality Test.

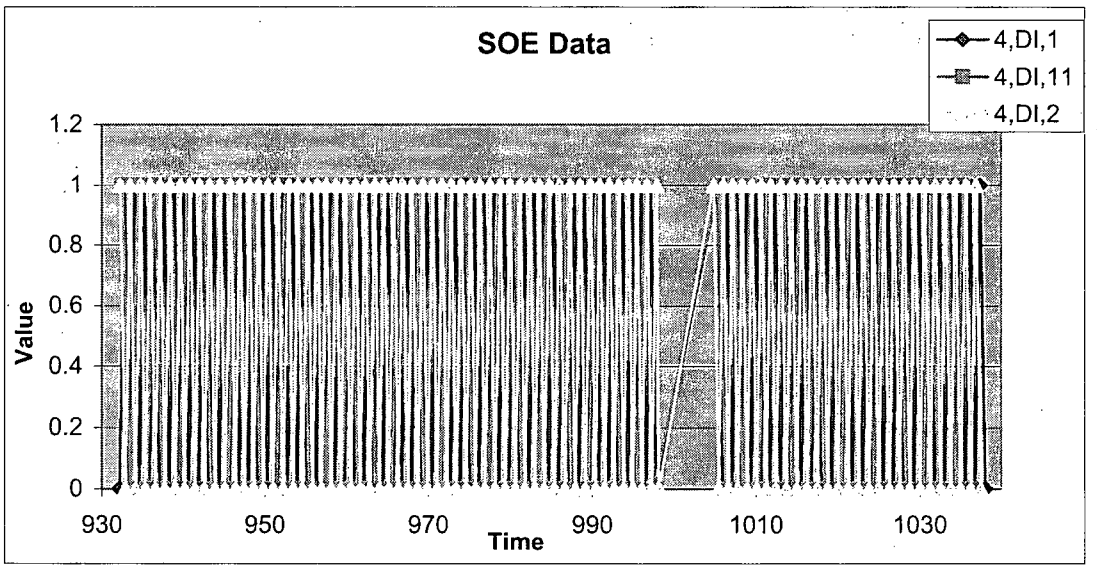


Figure B.11-2. SOE Logged Points during Power Quality Test.

The following table shows the response time during Power Quality Test during Environmental Stress Test. They are within the tolerance limits of baseline testing.

Table B.11.2 Power Quality Test Response Time

Test	Reset Period (s)	Set Period (s)	Total Period (s)
Automated Response Time Test			
Power Quality Test Background Test			

HFC-6000 Control System

ERD111 – Control System Qualification Project

Environmental Testing Summary Report

Appendix C

Environmental Stress Test and Post Tests – Prudency Test

C.1 GENERAL

This attachment is to document the results of the Prudency Tests during and after the Environmental Stress Tests as stated in Section 4.2 and 4.3 of the Environmental Stress Test Procedure TP0404, Rev. C. The acceptance criteria against which the results are evaluated are provided in Section 5.0 of the test procedure.

The purpose of the prudency tests during and after Environmental stress is to verify that the system performance was not impacted significantly by the elevated temperature, cold temperature, or transition from one temperature to another. Test results shall remain within the tolerance limits established by the baseline testing, as listed in Attachment A of Baseline Testing Summary Report. Any deviation from baseline results established during prequalification testing will be identified and recorded.

The prudency tests were conducted at the end of 140 °F, at the end of 40 °F, and at ambient room temperature. The tests include digital and analog BOE tests.

C.2 DIGITAL BOE TEST

C.2.1 At the end of 140 °F Period

It was confirmed that every transition was detected for all seven logged digital channels (4,DI,24 to 4, DI,30) by analyzing the SOE data from the 140 °F environmental stress test. Analysis of the alarm status files indicate that no link alarm condition was detected for the DI cards used for this test.

Abnormal transitions and the corresponding timestamps for all 7 logged digital channels are listed in Table C.2-1. The abnormal transition at the end of the test, i.e., at around 16:58:37 PM, happened to all monitored digital channels. This anomaly is caused by the perturbation from stopping the BOE test and thus should not be counted as the transition exceptions. The numbers in red represents the transition times of relay contact bounce. Ten contact bounces occurred for channel 4,DI,26 during the test period, compared to two occurrences for channel 4,DI,26 during the pre-qualification test.

Excluding the occurrences of contact bounces and abnormal transitions caused by the stopping of BOE test, all the rest of transitions meet the acceptance criteria, which is in line with the pre-qualification test.

Table C.2.1. Digital BOE Abnormal Transitions in the 140 °F Environmental Stress Test.

Time Stamp			4,DI,30	4,DI,29	4,DI,28	4,DI,27	4,DI,26	4,DI,25	4,DI,24
H	M	S							
16	57	45							
16	57	45							
16	57	57							
16	57	57							

16	58	11							
16	58	11							
16	58	13							
16	58	13							
16	58	23							
16	58	23							
16	58	37							
Total Number of Transitions									
Total Number of Contact Bounce									
Total Number of Anomalies									

C.2.2 At the end of 40 °F Period

Analysis of SOE data from the 40 °F environmental stress test verifies that every transition was detected for all seven logged digital channels (4,DI,24 to 4, DI,30). No link alarm condition was detected for the DI cards used in the test.

Table C.2-2 lists the abnormal transitions and the corresponding timestamps for all 7 logged digital channels. The numbers in red represent the transition times of relay contact bounce. Two contact bounces occurred for channel 4,DI,30 during the test period, compared to two occurrences for channel 4,DI,24 and two for 4,DI,26 during the pre-qualification test.

Excluding the occurrences of contact bounces, all the rest of transitions meet the acceptance criteria, which is in line with the pre-qualification test.

Table C.2.2. Digital BOE Abnormal Transitions in the 40 °F Environmental Stress Test.

Time Stamp			4,DI,30	4,DI,29	4,DI,28	4,DI,27	4,DI,26	4,DI,25	4,DI,24
H	M	S							
9	59	43							
9	59	43							
Total Number of Transitions									
Total Number of Contact Bounce									
Total Number of Anomalies									

C.2.3 At Ambient Room Temperature

C.3 ANALOG BOE TEST

C.3.1 At the End of 140 °F

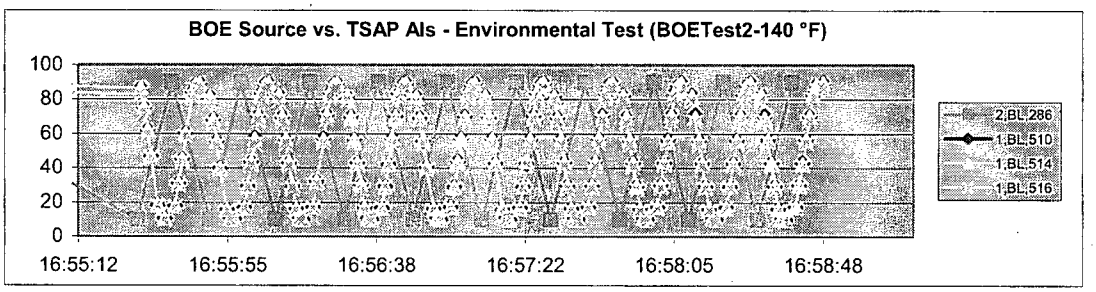


Figure C.3-1. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 in the 140 °F Environmental Stress Test.

Table C.3.1. TSAP AI Channel Readings and Deviations from BOE Source Signal in 140 °F Environmental Stress Test.

	1,AI,882 (1,BL,510)	1,AI,884 (1,BL,514)	1,AI,901 (1,BL,516)
10% Measurement			
Deviation From 10%			
Num of Measurements			
90% Measurement			
Deviation From 90%			
Num of Measurements			

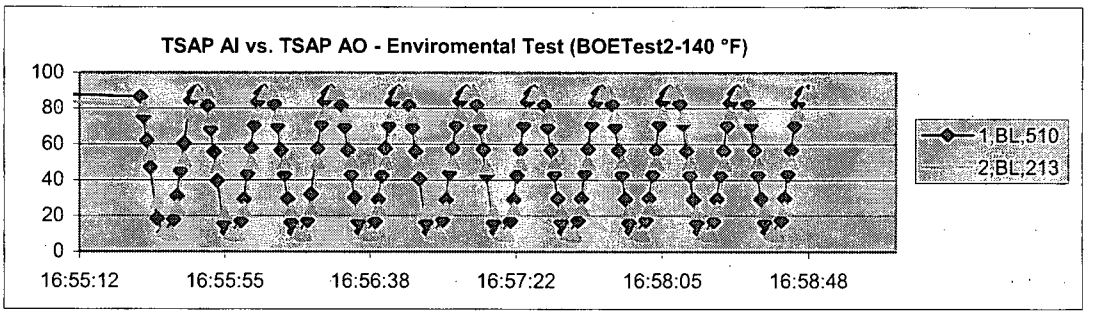


Figure C.3-2. Logged TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) in the 140 °F Environmental Stress Test.

Table C.3.2. TSAP AOs and the Corresponding TSAP AIs in Remote1 in the 140 °F Environmental Stress Test.

	1,AI,882 (1,BL,510)	1,AO,922 (2,BL,213)	Deviation (2,BL,213 vs. 1,BL,510)
10% Measurement			
Number of Measurements			
90% Measurement			
Number of Measurements			

C.3.2 At the End of 40 °F

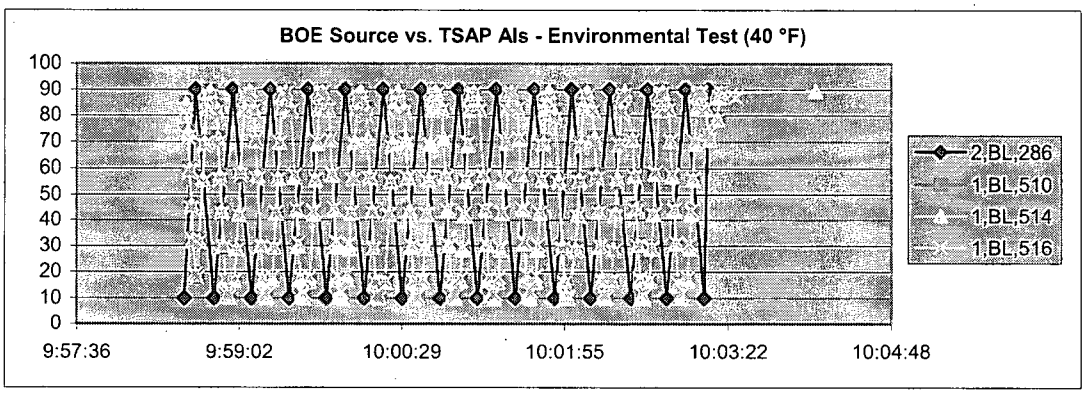


Figure C.3-3. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 in the 40 F Environmental Stress Test.

Table C.3.3. TSAP AI Channel Readings and Deviations from BOE Source Signal in the 40 °F Environmental Stress Test.

	1,AI,882 (1,BL,510)	1,AI,884 (1,BL,514)	1,AI,901 (1,BL,516)
10% Measurement			
Deviation From 10%			
Num of Measurements			
90% Measurement			
Deviation From 90%			
Num of Measurements			

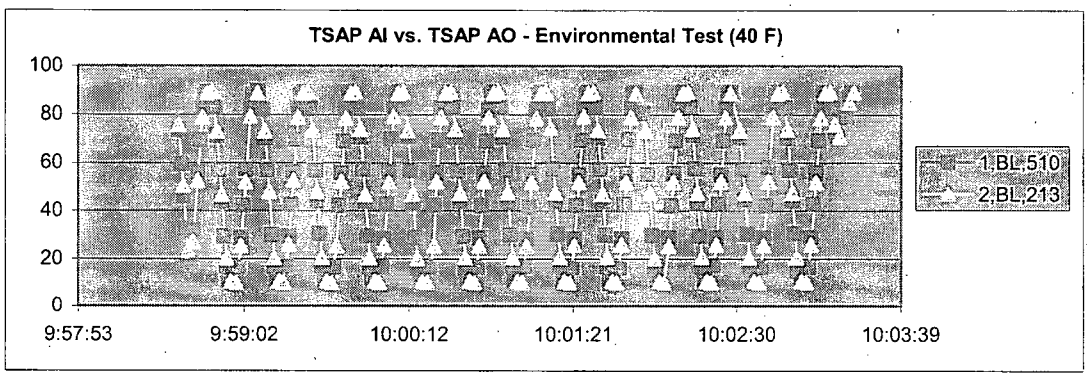


Figure C.3-4. Logged TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal(1,AO,922, 2,BL,213) in the 40 °F Environmental Stress Test.

Table C.3.4. TSAP AOs and the Corresponding TSAP AIs in Remote1 in the 40 °F Environmental Stress Test.

	1,AI,882 (1,BL,510)	1,AO,922 (2,BL,213)	Deviation (2,BL,213 vs. 1,BL,510)
10% Measurement			
Number of Measurements			
90% Measurement			
Number of Measurements			

C.3.3 At Ambient Room Temperature

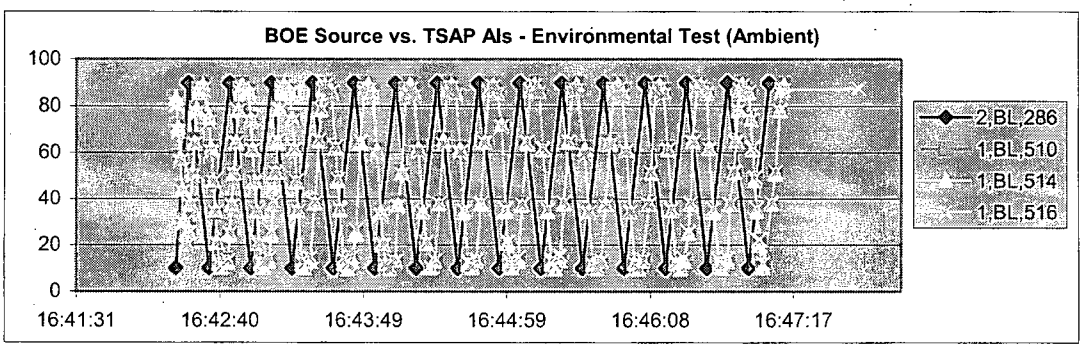


Figure C.3-5. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 in the Post Environmental Stress Test.

Table C.3.5. TSAP AI Channel Readings and Deviations from BOE Source Signal in the Post Environmental Stress Test.

	1,AI,882 (1,BL,510)	1,AI,884 (1,BL,514)	1,AI,901 (1,BL,516)
10% Measurement			
Deviation From 10%			
Num of Measurements			
90% Measurement			
Deviation From 90%			
Num of Measurements			

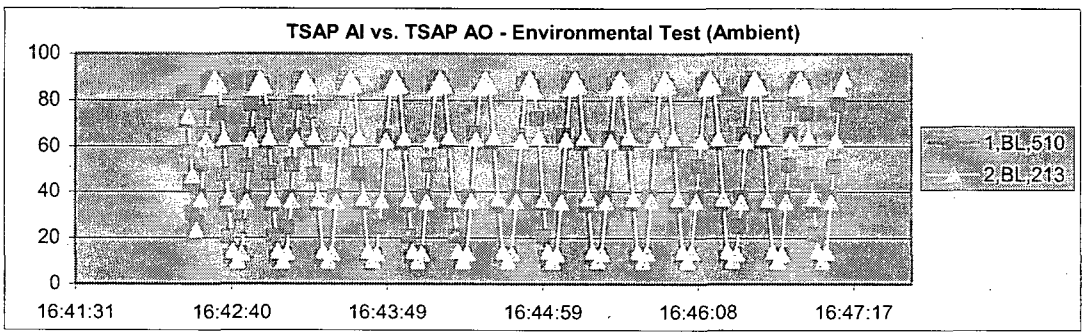


Figure C.3-6. Logged TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal(1,AO,922, 2,BL,213) in the Post Environmental Stress Test.

Table C.3.6. TSAP AOs and the Corresponding TSAP AIs in Remote1 in the Post Environmental Stress Test.

	1,AI,882 (1,BL,510)	1,AO,922 (2,BL,213)	Deviation (2,BL,213 vs. 1,BL,510)
10% Measurement			
Number of Measurements			
90% Measurement			
Number of Measurements			

HFC-6000 Control System

ERD111 – Control System Qualification Project

Environmental Testing Summary Report

Appendix D

Environmental Stress Tests - Static Tests

D.1 GENERAL

The environmental stress test was run at Wyle Laboratories during the period from 1:00 PM on February 20, 2004 through 5:00 PM on February 24, 2004. Automated prudency and operability tests were scheduled to be run prior to the start of the temperature ramp up, after a minimum period of 48 hours at the high temperature level (140° F and 95% RH), after a minimum period of 8 hours at the low temperature level (40° F and 5% RH), and after a return to ambient temperature. Between the periods while the automated tests were running, the system was logging internal status and the value of static data points. The static data points consisted of a set of analog and digital points (TP0405 Tables 1 and 2) that had been set to fixed states during the pretest period. The specific points that were to be logged are listed in bold in Tables 1 and 2 of TP0405. The internal status points consist of the first 2000 FL points in each remote that are reserved for system use. These flags are typically configured for broadcast and are used to control system-level alarms.

D.2 STATIC POINT TEST DATA

D.2.1 Pretest

The static points test consisted of 58 DO channels and 29 AO channels. Most of the DO channels were controlled either by the digital BOE test (half on, half off) or by one of the simulated control loops. However, a small number of spare DO channels were configured by using the memory editor to directly set or clear the memory image for that point. The analog channels were controlled by the following sources:

- Analog accuracy test (fixed at 10% when test was disabled).
- Analog BOE test (fixed at 90% where test was disabled).
- Simulated analog loop (set manually from the HPAT interface).
- RTD input channel (input simulated by a fixed resistor).

In each case, the channels were expected to remain static while the automated tests were disabled. Both the SOE and HAS were used to log the static points data. Table D.2-1 lists the static points that were logged and identifies the source of logged data. All of the digital static points were hard wired to inputs of the HPAT with selected points being logged both by the SOE and the HAS. All analog points were logged by the HAS only. Half of the analog points were hard wired to input points of the HPAT and logged from an HPAT AIC block; the remainder of the static points were logged from a processing block within the TSAP. One of the analog points had two sources of logged data.

Table D.2.1. Log Points for Static Data.

Static Point	Data Source	Log Point	
Digital Data			
1,DO,383	Digital BOE	2,DI,141 4,DI,17	Logged by both SOE and HAS
1,DO,385	Digital BOE	4,DI,18	Logged by SOE only
1,DO,387	Digital BOE	4,DI,19	Logged by SOE only

1,DO,401	Analog Response Time	2,DI,161 4,DI,10	Logged by both SOE and HAS
1,DO,402	Digital BOE	4,DI,33	Logged by SOE only
1,DO,403	Digital BOE	4,DI,34	Logged by SOE only
1,DO,646	Timer Test	4,DI,20	Logged by SOE only
1,DO,648	Digital BOE	4,DI,28	Logged by SOE only
1,DO,668	Digital Response Time	2,DI,232 4,DI,9	Logged by both SOE and HAS
1,DO,682	Digital BOE	4,DI,29	Logged by SOE only
1,DO,684	Digital BOE	4,DI,30	Logged by SOE only
1,DO,686	Digital BOE	4,DI,31	Logged by SOE only
1,DO,688	Digital BOE	4,DI,32	Logged by SOE only
Analog Static Points			
1,AO,801	TA05	1,BL,41	Signal controlled by simulated closed analog loop. Log point is the ANO block controlling the AO channel.
1,AO,843	Analog BOE	2,BL,201	Log point is the AIC block receiving the signal back from test specimen.
1,AO,861	1,BL,31	1,BL,31	Signal controlled by simulated closed analog loop. Log point is the ANO block controlling the AO channel.
1,AO,921	AI Accuracy	2,BL,215	Log point is AIC block receiving the signal back from the test specimen.
1,AO,922	Analog BOE	2,BL,213	Log point is AIC block receiving the signal back from the test specimen.
1,AO,923	AO Accuracy	1,BL,554 2,BL,211	Both TSAP ANO block and HPAT AIC block logged.
1,AO,924	Analog BOE	2,BL,209	Log point is AIC block receiving the signal back from the test specimen.
1,AO,981	TA05	1,BL,40	Signal controlled by simulated closed analog loop. Log point is the SSL block controlling signal selection.
1,AO,983	1,AI,963	1,BL,548	Signal controlled by RTD input channel. Log point is ANO block controlling the AO channel.
1,AO,984	TA05	1,BL,43	Signal controlled by simulated closed analog loop. Log point is the ANO block controlling AO channel.
3,AO,61	Analog BOE	2,BL,291	Log point is AIC block receiving the signal back from the test specimen.

D.2.2 High Temperature Period

Ramp up to the high temperature level extended from 1:00 PM to 4:37 PM on 2/20/04, and the high temperature static interval continued until 4:50 PM on 2/22/04. Both the digital and the analog static points were configured at the start of the ramp up period and logged throughout this interval.

D.2.2.1 Digital Static Points

D.2.2.2 Analog Static Points

D.2.2.2.1 Simulated Closed Control Loop

D.2.2.2.2 Analog BOE Channels

Table D.2.2. Analog BOE Channels during Ramping Up Period.

Data Source	Log Point	Average Value	Deviation from Mean
1,AO,843	2,BL,201		
1,AO,922	2,BL,213		
1,AO,924	2,BL,209		
3,AO,61	2,BL,291		

D.2.2.2.3 Analog Accuracy Channels

. The following chart summarizes the results of the logged records during ramp up.

Table D.2.3. Analog Accuracy Channels during Ramping Up Period

Data Source	Log Point	Average Value	Deviation from Mean
1,AO,921	2,BL,215		
1,AO,923	1,BL,554		
	2,BL,211		

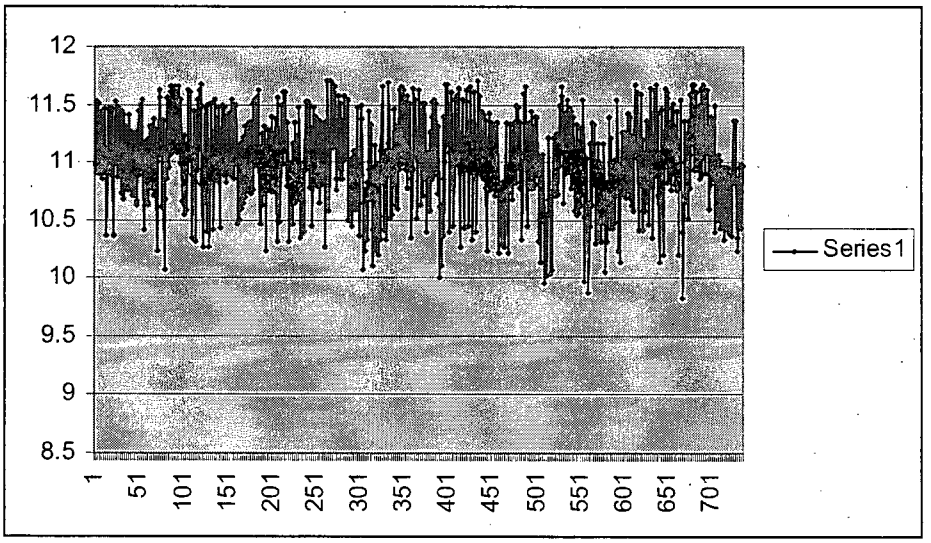


Figure D.2-1. 1,BL,215 Log Values.

D.2.2.2.4 RTD Input

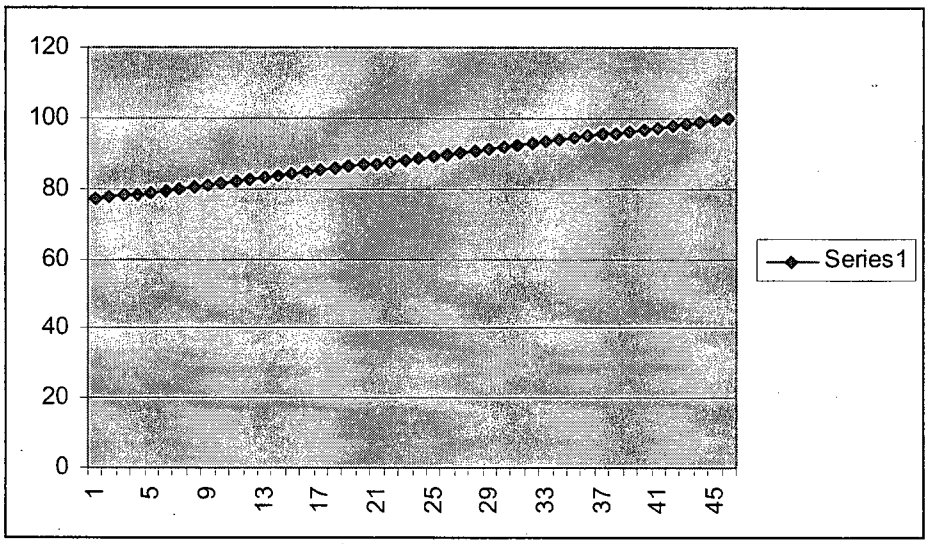


Figure D.2-2. RTD Input Value During 2/20/04.

D.2.3 Ramp to Low Temperature Test Period

D.2.4 Low Temperature Test Period

D.2.5 Return to Ambient Period

D.3 ALARM POINT STATUS

HFC control systems include an alarm server utility that monitors every DDB broadcast and examines the status of every point listed in an alarm configuration table. Certain data point types (MS, DI, DO, and BL) include a quality word that contains alarm status data in addition to the point value. The alarm server logs these points whenever their alarm status changes. Each FL point consists of a single data bit without quality word. When FL points are included in the alarm configuration table, the alarm server logs every logic transition. The total alarm log includes seven fields that permit the user to identify the date, time, point type, and overall status of the points in the log. This data is presented on a formatted display screen of the operator workstation and also recorded in a buffer file that is stored in the job directory in the folder for Remote 0. Each buffer file contains the alarm activity for a single 24-hour period, and these files are retained in the job directory as a historical record of alarm activity and system status.

D.3.1 Link Status

Table D.3.1. Station Alarms During the Environmental Test.

Module Type	Station	2/20	2/21	2/22	2/23	2/24
HFC-DC34	0					
HFC-DC34	1					
HFC-DC34	3					
HFC-DI16I	5					
HFC-DO8J	6					
HFC-DO8J	7					
HFC-DI16I	16					
HFC-DC33	17					
HFC-DI16I	19					
HFC-DC34	20					
HFC-DI16I	22					
HFC-DO8J	23					
HFC-DI16I	24					
HFC-DI16I	25					
HFC-DC33	26					
HFC-DI16I	36					
HFC-DI16I	37					
HFC-DO8J	38					
HFC-DO8J	39					
HFC-DO8J	40					
HFC-AO8F	49					
HFC-AI16F	52					
HFC-AI16F	53					
HFC-AO8F	54					
HFC-AI8M	56					
HFC-AI4K	58					
HFC-AI4K	59					
Nominal number of scan cycles during 24-hour period: 864,000						

D.3.2 System Status Flags

Not all of the system status flags specifically represent alarm conditions, but they can be used to generate system level alarms for display on the operator workstation. Table D.3-2 lists the total number of records logged in the alarm files for selected system status flags during the environmental test. The functions of these flags are as follows:

- A/B Primary – True state indicates that controller A is primary; false state indicates that controller B is primary. A transition indicates either controller reset or failover.
- Secondary in Standby – True state indicates that the secondary controller is operating normally, not primary, and available for failover. If any of these conditions is not satisfied, the flag will be reset to false.
- EQ Drops Good – True status indicates that the transfer of digital status data from the primary to the dual-ported memory (DPM) occurred without error. Equation drops normally occur once per second.
- CQ4 Drops Good - True status indicates that the transfer of analog status data from the primary to the DPM occurred without error. Equation drops normally occur once per second.
- FL,1081 thru FL,1088 – This is a status byte that defines overall status of the secondary controller. The byte value must be 77H for failover to be enabled.
- Secondary Subordinates OK – True status indicates that the two secondary processors on the secondary controller are operating normally (no mailbox timeout).
- Hardware Port OK

Table D.3.2. System Status Flags During the Environmental Test.

Flag ID	Name	2/20	2/21	2/22	2/23	2/24
FL,1048	A/B Primary					
FL,1049	Secondary in Stby					
FL,1081	EQ Drops Good					
FL,1082	CQ4 Drops Good					
FL,1083	IOC List Good					
FL,1085	EQ Valid					
FL,1086	CQ4 Valid					
FL,1087	DB Equalized					

FL,1088	Secondary Subordinates OK					
FL,1090	Hardware Port OK					
Nominally, 86,000 DPM drops occur over a 24-hour period.						

The significance of these flag transitions is as follows:

D.4 CONCLUSIONS

The essential time line for test events is shown in Table D.4-1. The essential acceptance criteria for the Digital Static Points Tests, Analog Static Points Tests and System Alarms and Status Flags tests are as follows:

- Static DO channel tests – Neither energized relay channels nor deenergized channels exhibit any spurious transitions.

- Static AO channel tests – No AO channel changes by more than 0.05% from its set value throughout the test period. (Note: The deadband of the HAS logger was

set to 0.5%, so deviations of 0.05% cannot be observed. Also, this parameter was taken from EPRI TR-107330 paragraph 4.6.4, which does not apply to the environmental stress test.)

- If any alarm condition is detected during the environmental stress test, the alarm state shall not affect overall functional operation of the Test Specimen or TSAP.

Table D.4.1. Test Time Segments.

Time Period	Activity
1:00 PM 2/20/04 to 5:00 PM 2/20/04	Environmental test enclosure closed at 1:00 PM. Ramp up to the high temperature and humidity levels occurs over a four-hour period.
5:00 PM 2/20/04 to 4:50 PM 2/22/04	High temperature and humidity period. No significant disruptions noted; static point status logged.
5:00 PM 2/22/04 to 9:00 PM 2/22/04	Operability and Prudency tests run. Static point values are not significant during this period.
9:00 PM 2/22/04 to 9:00 AM 2/23/04	No clear indication of disruption. Static data logged during this period.
9:00 AM 2/23/04 to 6:00 PM 2/23/04	Log of 1,CO,50 and system status flags show at least 8 periods of instability. Each of these correlates directly with power trips caused by overload of the Wyle power cord. The power trips and the subsequent execution of automated tests to verify restoration of test specimen operation invalidates the static point logs during this period.
6:00 PM 2/23/04 to 6:30 AM 2/24/04	Low temperature and humidity stress period. Log of 1,CO,50 indicates stable operation, but one of the two controllers was not running.
6:30 AM 2/24/04 to 10:00 AM 2/24/04	Operability and Prudency tests run. Static point values are not significant during this period.
10:00 AM 2/24/04 to 2:20 PM 2/24/04	Ramp up to ambient and temperature stabilization.
2:20 PM 2/24/04 to 5:00 PM 2/24/04	Operability and Prudency tests run. Static point values are not significant during this period.

D.4.1 Digital Static Points Test Results

No spurious transition was detected for any of the digital static points during any phase of the test.

D.4.2 Analog Static Points

D.4.2.1 Simulated Closed Loop Channels

Two of the logged output channels were controlled directly by PID blocks and two were controlled by the closed loop feedback from the HPAT. During the high temperature phase of the test, the two channels controlled directly by PID blocks were fixed at their setpoint value and did not deviate from that value by more than the deadband of the HAS logger. The two channels controlled by the feedback loop both drifted up to fixed values

and then remained static. Because the feedback signal is not directly related to the setpoint value of the source signal, a quantitative evaluation of the signal deviation is not significant.

Following the power trips that occurred at the end of the high temperature period and during the ramp down interval, the analog values were not reset to their initial states. Consequently, the logged data for these points is not meaningful for the remainder of the environmental test.

D.4.2.2 Analog BOE Channels

The four analog BOE channels included in the test all maintained stable values that varied by less than the preset deadband of the HAS. The points that were logged exhibited a degree of stability that was within ± 0.05% of full span, but the absolute value of each channel deviated from the signal source value by more than this amount, as shown below. However, these parameters remained stable and exhibited no drift in excess of the HAS deadband through the test period. In addition, the logged values were consistent with the values observed for the corresponding points as measured in the baseline analog prudency test.

Table D.4.2. Static Analog BOE Points.

Signal	Average Value	% Deviation from Signal Source
1,AO,843		
1,AO,922		
1,AO,924		
1,AO,61		
Note: Deviation value is based on % of full span.		

D.4.2.3 Analog Accuracy Channels

Two channels controlled by the analog accuracy algorithm were included among the static channels. HAS records of static data for both channels were obtained for both channels during the ramp up period, and both values correspond to those that were obtained for the same blocks during the baseline prequalification tests. The percent deviation from the source signal is shown below.

Table D.4.3. Static Analog Accuracy Tests.

Signal	Average Value	% Deviation from Signal Source
1,AO,921		
1,AO,923		
Note: Deviation value is based on % of full span.		

No values were logged for 1,AO,921 after the ramp up period, indicating that it did not change by more than the HAS deadband value. The HAS did record numerous values for 1,AO,923 during the high temperature phase. Over this interval, its average value was 10.99, or 0.99% (% of full span) above the source signal, and the standard deviation of the sampled records was 0.41. During the low temperature and ambient phases of the

test, no records for this point were logged, indicating that it did not change by more than the HAS deadband. This difference indicates the impact of the elevated temperature on the analog circuitry on the AI module.

D.4.2.4 RTD Input Channel

The log of records from the RTD input channel exhibits a gradual, but uniform increase in the reported value. The RTD input signals were simulated with eight matched resistors having a fixed starting resistance of 130.00 ± 0.25 ohms. During the course of the environmental stress test, the effective value of all eight resistors increased by about 10 ohms, as shown below. This increase in resistance was sufficient to simulate a temperature greater that the 100° C span of the AIC blocks configured for the RTD channels. Consequently, these channels reported an over range error and did not return to normal operation after completion of the environmental test. The overall span configured for the AIC blocks processing the RTD inputs were subsequently increased prior to the start of EMI/RFI testing, and this action returned the module to normal indications for all channels.

Table D.4.4. Resistance Value of Loaded Resistors for RTD after Environmental Test.

Original value	Resistance value after environmental stress test							
130.00 ± 0.25	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
	141.22	139.52	139.93	139.23	139.23	139.80	138.43	139.90

The results obtained provide reasonable confidence that the RTD input module will perform reliably in the presence of thermal stress, but the fact that the input signal changed eliminates the resulting AO signal from being considered a static point.

D.4.3 System Alarms and Status Flags

The link alarm flags indicate that some of the modules exhibited some degree of sensitivity to elevated temperature. The level of disruption introduced into the ICL communication by the elevated temperature was insignificant (less than 200 failures to respond out of 864,000 poll messages per day). All of the modules returned to normal operation during the cold phase of the test, and no station alarm occurred thereafter.

Overall operation of the controllers was not significantly impacted by the thermal stress. The entire system was disrupted by the power problems during 2/23/04, but this was not a planned or intended part of the stress test. Controller B failed to complete initialization after the cause of the power problem was identified and corrected for reasons that have not been specifically identified. Controller A continued operating so that the subsequent dynamic and static tests were not impacted. Failure of a single controller does not constitute failure of the test as a whole.

D.4.4 Overall Assessment

The acceptance criteria for the static points are as follows:

- Static DO channel tests – Neither energized relay channels nor deenergized channels exhibit any spurious transitions.

- Static AO channel tests – No AO channel changes by more than 0.05% from its set value throughout the test period.

The Test Specimen met that acceptance criteria for the test except for the following minor considerations:

- Failure of controller B following the last power cycle had no impact on the performance of the system during the low temperature phase and or subsequent qualification testing. This will not be considered a failure of the environmental stress test.

- The repeated power trips caused by the Wyle power drop did disrupt several of the tests, but it did not have any material impact on evaluating the overall test results. Occurrence of these trips and the resulting disruptions do not constitute a failure of the test as a whole.

- The inputs to the RTD channels did exhibit thermal sensitivity, but the module did not exhibit any instability. All indications are that the observed deviations were caused by the simulation resistors, which changed value during the test and did not return to their original value following completion of the test.

- There was no indication of any change in the analog output values; however, the HAS deadband exceeded the tolerance stipulated by the EPRI specification. Applications necessitating demonstration of the higher accuracy in the EPRI specification may need additional project specific testing.

HF Controls

DOOSAN HF CONTROLS CORPORATION

NON-PROPRIETARY

HFC-6000 Control System

ERD111 – Control System Qualification Project

EMI/RFI, ESD and SWC Testing Summary Report

TS901-000-25

Rev B

Effective Date	09/26/07
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1.0 PURPOSE

HFC is generically qualifying its HFC-6000 control system for nuclear safety-related applications in U.S. nuclear power plants. The approach taken for this qualification effort is based on the guidance provided in EPRI-TR-107330, Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants.

This document specifically addresses the Electromagnetic Interference (EMI), Electrostatic Discharge (ESD), and Surge Withstand segments of the qualification testing program.

2.0 SCOPE

2.1 Definition of the test setup and EMI/RFI qualification testing performed by Wyle Laboratories for the HFC-6000 Control System product line.

2.2 Evaluation of Operating and Prudency testing performed before/during/after EMI/RFI Testing to identify any performance degradation from the pre-qualification Baseline Operating and Prudency testing performed at HFC.

2.3 Definition of the test setup and ESD qualification testing performed by Wyle Laboratories for the HFC-6000 Control System product line.

2.4 Evaluation of Operating and Prudency testing performed before/during/after ESD Testing to identify any performance degradation from the pre-qualification Baseline Operating and Prudency testing performed at HFC.

2.5 Definition of the test setup and Surge Withstand testing performed by Wyle Laboratories for the HFC-6000 Control System product line.

2.6 Evaluation of Operating and Prudency testing performed before/during/after Surge Withstand Testing, to identify any performance degradation from the pre-qualification Baseline Operating and Prudency testing performed at HFC.

3.0 REFERENCES

3.1	TS901-000-22	HFC6000 Baseline Testing Summary Report
3.2	TP0402	Operability Test Procedure
3.3	TP0403	Prudency Test Procedure
3.4	VV0414	Master Configuration List
3.5	50044-10	Test Procedure Environmental and EMI Testing of an HFC-6000 Control System (Wyle)

3.6	50044-01	Test Report Environmental and EMI Testing of an HFC-6000 Control System (Wyle)
3.7	TP0407	HFC-6000 Control Systems, ERD111- Control System Qualification EMI/RFI Test Procedure
3.8	TP0409	HFC-6000 Control Systems, ERD111- Control System Qualification ESD Test Procedure
3.9	TP0406	HFC-6000 Control Systems, ERD111- Control System Qualification Surge Withstand Test Procedure

4.0 HFC-6000 EMI. ESD. AND SURGE WITHSTAND QUALIFICATION DESCRIPTION

The HFC-6000 control system (Test Specimen) is designed to operate in a wide variety of industrial applications, fossil power plant, and nuclear power plant applications. The control system hardware may be installed both in an electrical equipment room and at various other locations near the equipment under control. The control system hardware and the field equipment both generate electromagnetic radiation (noise). Potentially the operation of this equipment is susceptible to degradation or failure due to such noise. In the installation environments, the potential exists for exposure of sensitive electronic components to high voltage electrostatic discharges. Power, electrical I/O signal lines, and hardwired communication cables may also be exposed to high amplitude transient signals. Acceptable levels of EMI/RFI susceptibility, radiation limits, ESD immunity, and surge withstand are defined in EPRI TR-102323 (later revised by NUREG 1.180 Rev 1).

Testing was performed in accordance with HFC EMI/RFI Test Procedure, HFC ESD Test Procedure, HFC Surge Withstand Test Procedure and Wyle EMI Test Procedure. Test results are recorded in the Wyle EMI Test Report, and in the individual HFC Test Procedures.

Wyle Labs test technicians conducted the following specific tests:

- Radiated Susceptibility Test – RS103
- Conducted Susceptibility Test – CS101 and CS114
- Radiated Emissions Test – RE101 and RE102
- Conducted Emissions Test – CE101 and CE102
- Electrostatic Discharge (ESD) Test
- Surge Withstand Capability (SWC) Test

Wyle test personnel conducted the individual test sequences and an HFC test engineer monitored overall performance of the HFC-6000 Test Specimen.

5.0 HFC-6000 EMI, ESD AND SURGE WITHSTAND TEST SETUP DESCRIPTION

The HFC-6000 Test Specimen consists of several modular chassis, a power supply rack, a flat panel display, CSMs and M/A stations for simulated control loops, communication hardware, and mechanical support structures. The flat panel display, CSM, and M/A station are not within the scope of the qualification project. The electrical interference testing began after the environmental stress test was complete. The Test Specimen hardware was set up in the Test Chamber with the HPAT physically located outside. Electrical, communication, and power cables were reconnected, and pre testing performed in accordance with the test procedures.

6.0 EMI/RFI, ESD AND SURGE WITHSTAND TESTING

Testing was performed in accordance with HFC EMI/RFI Test Procedure, HFC ESD Test Procedure, HFC Surge Withstand Test Procedure and Wyle EMI Test Procedure. All test results are recorded in the Wyle EMI Test Report, and in the individual HFC Test Procedures. The following sections summarize the testing performed and the results.

6.1 Radiated Susceptibility Test – RS103

The HFC-6000 Control System was subjected to RS103 Radiated Susceptibility Test, with radiated electric field of 10 V/m and frequency range of 10 KHz to 1 GHz. The test was executed twice. Once with the antenna positioned at the front center of the Test Specimen and once with the antenna at the rear center.

According to the Wyle test report, the Test Specimen exhibited immunity to the test signal except for one DC33 card which went into an alarm state while the interference signal was being broadcast from the rear (exposed side) of the Test Specimen. Other DC33 cards in the Test Specimen had no problem during the RS103 tests.

Summary of Susceptibility Effects:

During the test period, an alarm occurred for a DC33 card at station 26 (rack 2, slot 11). It alarmed at 490 MHZ of Front Horizontal Test, and about 16 MHZ of Front Vertical Test. This DC33 card was functioning properly during the Rear Horizontal and Rear Vertical Tests. There is one other DC33 card in the test specimen and it performed its control function normally throughout the RS103 test period without going into an alarm state.

Conclusion:

The DC33 card was shown to be capable of performing its function successfully during execution of the RS103 test.

6.2 Conducted Susceptibility Test – CS101 and CS114

6.2.1 CS101

The HFC-6000 Control System was subjected to the CS101 Susceptibility Test. This test injected a test signal 6.3 Vrms having a frequency range of 30 Hz to 50 kHz range on all power lines.

The DC33 card that was replaced after the RS103 test failed during the CS101 test. The HFC-6000 Control System was not susceptible to interference signals injected onto the input power lines after this card was replaced.

6.2.2 CS114

The HFC-6000 Control System was subjected to CS114 Susceptibility Test, in the 50 kHz to 400 MHz range, on all power lines. A decision was made during the test program due to time constraints for the test chamber to not run the injection of the test signal on the I/O cables.

A detailed summary of the disruptions is as follows:

Conclusion:

Tests were completed and the results were recorded and analyzed as defined above.

6.3 Radiated Emissions Test – RE101 and RE102

6.3.1 RE101

The HFC-6000 Control System was monitored in accordance with the RE101 Radiated Emissions Test procedure to measure the magnetic field emissions in the range from 30 HZ to 100 KHZ.

The radiated emissions from the HFC-6000 Control System were within the specified limits over the entire frequency range.

6.3.2 RE102

The Wyle test report contains an evaluation of the HFC-6000 radiated emissions relative to the criteria in EPRI TR-102323-R1 to measure the electric field emissions from 10 KHZ to 1 GHZ. Separate test runs were conducted with horizontal and with vertical antennas positioned 1 meter from the front and 1 meter from the rear of the Test Specimen. Subsequently, HFC has re-evaluated the emissions relative to the guidance in Regulatory Guide 1.180-Revison 1. The results below are based on this reevaluation.

The following is a list of conditions that exhibited some degree of emissions deviations during the tests:

During the RE102 test the findings are as follows;

- The radiated emissions detected from the front antenna position did not exceed the revised limits.
- Of the 18 points detected by the rear vertical antenna, at most 2 points exceed the revised limits by a maximum of 0.9 dB, or approximately 1%.
- Of the 57 points detected by the rear horizontal antenna, at most three points exceed the revised limits by a maximum of 2.5 dB, or approximately 3.7%.

Conclusion:

All of the excessive emissions readings were taken from the rear of the cabinet. Two of the spikes have been isolated to the Flat Panel Display and the Flat Panel Controller, which are not included in the scope of this report; the remainder have not been isolated to specific components. There was no metal shielding at the rear of the Test Specimen to block RFI generated by system components. A completed system will be completely enclosed in a cabinet that will provide such shielding. Substantially the same components have been qualified in such a cabinet during the development for the Ulchin nuclear power plant, and the HFC-6000 control system will be qualified in equivalent cabinet structures on a project by project basis. The Ulchin EMI/RFI test data is documented in the HFC documentation files.

6.4 Conducted Emissions Test – CE101 and CE102

6.4.1 CE101

The CE101 Conducted Emission Test was performed on the HFC6000 Test Specimen to measure emissions in the range of 30 Hz to 50 kHz range on all power leads.

The conducted emissions on all power lines were within the specified limits.

6.4.2 CE102

The CE-102 Conducted Emissions Test was performed on all power leads of the HFC-6000 Test Specimen to measure emissions in the range from 50 KHZ to 400 MHZ.

The conducted emissions of HFC-6000 Control System were within the specified limits with the following notation:

> The 120 VAC High lead exceeded the limit at 110.2 KHz by 8.0 dBμV, and the Neutral lead exceeded the limit at 110.2 KHz by 7.0 dBμV. (Reference 3.7, Notice of Anomaly No. 4).

However, USNRC Regulatory Guide 1.180 Rev 1, which was obtained after execution of the test, revises the conducted emissions envelope so that the above point is no longer in excess of the allowable limit. Consequently there are no anomalies in the frequency range covered by CS102.

6.5 Electrostatic Discharge (ESD) Test

The HFC-6000 Control System was subjected to an ESD test of 8 kV contact and 15 kV air ESD discharges to specified components of the Test Specimen as well as 8 kV contact to the Vertical Coupling Plane (VCP) around the perimeter of the Test Specimen. Table 1 list all the individual components subjected to the ESD testing.

Table 1. ESD Test Points

Component	Location	Discharge Type
Controller and I/O Chassis	At the top, bottom and each side of the controller chassis, expansion chassis, and single loop chassis	Contact
	The front surface of bezel for each of the different circuit board types	Contact
	Controller A power toggle switch	Contact
	HFC-FPC06 power/reset toggle switch	Contact
	DPM failover pushbutton switch	Air
	One of the two C-Link connector shells for controller A	Air
Power Supply Chassis	Top, bottom and both sides of chassis frame	Contact
	Module A 24-vdc power supply front panel	Contact
	Module A 48-vdc power supply front panel	Contact
	Single loop power bracket	Contact
	Single loop power switch	Air

It is noted that the single loop controller, HFC-FPC06 plat panel controller, and C-Link are not included in the qualification project, however they were used as injection points for the ESD contact for the test specimen.

The HFC-6000 Control System did not exhibit any functional susceptibility to the ESD pulses and experienced no permanent damage due to application of the ESD test wave form. During application of ESD pulses to I/O cards, the specific module tested appears to have had a single ICL communications error during application of the pulses. This had no functional impact on control system performance.

6.6 Surge Withstand Capability (SWC) Test

The HFC-6000 Control System was subjected to an SWC test using both Combination and Ring Waveforms.

The EPRI specification defines 14 different categories for surge testing, of which the following 7 are applicable to the HFC Test Specimen:

1. Between AC+ and AC- terminals for power supply group A of the redundant pair (EPRI TR-107330, 4.6.2.A)

2. Between AC+ and G terminals for power supply group A of the redundant pair (EPRI TR-107330, 4.6.2.B)

3. Between AC- and G terminals for power supply group A of the redundant pair (EPRI TR-107330, 4.6.2.C)

4. Across 1,DO,441 contact A29 to contact A28 (120-vac DO channel) in both the ON and OFF states (EPRI TR-107330, 4.6.2.F)

5. Between common connections of discrete inputs where a common is shared by two or more I/O points (EPRI TR-107330, 4.6.2.G). The following specific channels were be tested:

6. Between the power supply G terminal and the common for discrete inputs for both ON and OFF states (EPRI TR-107330, 4.6.2.H). The following specific channels were tested:

7. Between the power supply G terminal and the common for analog I/O channels (EPRI TR-107330, 4.6.2.I). The following specific channels were tested:

Specific acceptance criteria for each component subjected to the surge waveforms shall be as follows:

- Application of surge waveform shall not damage any other module, component, or channel other than those specific modules or circuits under test.
- Channels or modules other that the one under test continue to operate within normal accuracy limits for those modules during and after application of the test waveform.
- Failure of the particular channel or circuit under test will not be considered a failure of the Test Specimen if the circuit (e.g., power module) is redundant, if the failure does not disrupt overall operation of the Test Specimen, or the failure does not propagate to other channels or circuits.

The Test Specimen met all acceptance criteria as listed above. Some components were damaged as the result of the test pulses, but those damages were limited to the specific components under test and the remainder of the system continued operating normally before, during, and after application of the test waveform. The failures noted in the Wyle test report affected only those components under test and did not propogate to other modules.

Conclusion

The HFC-6000 Test Specimen satisfactorily met all of acceptance criteria for surge testing. Some components were damaged as the result of the test pulses; but that damage was limited to the specific components under test, and the remainder of the system continued operating normally.

7.0 SUMMARY

7.1 EMI/RFI Test

Radiated Susceptibility (RS103)

The Test Specimen exhibited immunity to the test signal except for one DC33 card which went into an alarm state in two tests.

There was one other DC33 card in the Test Specimen and it performed its control function normally throughout the test without going into an alarm state. Therefore, the DC33 card was shown to be capable of performing its function successfully during execution of the test. The DC33 card which had gone into the alarm state was found to be defective and was replaced in further tests.

Low Frequency Conducted Susceptibility (CS101)

The HFC-6000 Control System was not susceptible to the 30 Hz to 50 kHz interference signals injected onto the input power lines once the DC33 card referenced in Section 6.1 above was replaced.

High Frequency Conducted Susceptibility (CS114)

The HFC-6000 Control System was subjected to CS114 Susceptibility Test, in the 50 kHz to 400 MHz range, on all power lines.

Low Frequency Radiated Emissions (RE101)

The HFC-6000 Control System was monitored in accordance with the RE101 Radiated Emissions Test procedure to measure the magnetic field emissions in the range from 30 HZ to 100 KHZ. All radiated emissions were within the specified limits over the entire frequency range.

High Frequency Radiated Emissions (RE102)

An evaluation was performed of the HFC-6000 radiated emissions from horizontal and vertical antennas positioned one meter from the front and one meter from the rear of the Test Specimen. The purpose of the test was to measure the electric field emissions from 10 KHZ to 1 GHZ relative to the criteria in EPRI TR-102323-R1. Subsequently, HFC has re-evaluated the emissions relative to the guidance in Regulatory Guide 1.180-Revison 1. The results below are based on this reevaluation:

- The radiated emissions detected from the front antenna position did not exceed the revised limits.
- Of the 18 points detected by the rear vertical antenna, at most 2 points exceed the revised limits by a maximum of 0.9 dB, or approximately 1%.
- Of the 57 points detected by the rear horizontal antenna, at most 3 points exceed the revised limits by a maximum of 2.5 dB, or approximately 3.7%.

All of the excessive emissions readings were taken from the rear of the cabinet. Two of the spikes have been isolated to specific hardware components; the remainder have not. There was no metal shielding at the rear of the Test Specimen to block RFI generated by system components. A completed system will be fully enclosed in a cabinet that will provide such shielding. Substantially the same components have been qualified in such a cabinet during the development for the Ulchin nuclear power plant, and the HFC-6000 control system will be qualified in equivalent cabinet structures on a project by project basis. The Ulchin EMI/RFI test data is documented in the HFC documentation files.

Low Frequency Conducted Emissions (CE101)

The CE101 Conducted Emission Test was performed on the HFC6000 Test Specimen to measure emissions in the range of 30 Hz to 50 kHz range on all power leads. The conducted emissions on all power lines were within the specified limits.

High Frequency Conducted Emissions (CE102)

The CE-102 Conducted Emissions Test was performed on all power leads of the HFC-6000 Test Specimen to measure emissions in the range from 50 KHZ to 400 MHZ. Based on the acceptance criteria in USNRC Regulatory Guide 1.180 Rev 1, there are no anomalies in the frequency range covered by CS102.

7.2 ESD Test

The HFC-6000 Control System was subjected to an ESD test of 8 kV contact and 15 kV air ESD discharges to specified components of the Test Specimen as well as 8 kV contact to the Vertical Coupling Plane (VCP) around the perimeter of the Test Specimen. The Test Specimen did not exhibit any susceptibility to the ESD pulses and experienced no permanent damage due to application of the ESD test waveform.

7.3 Surge Withstand Capability (SWC) Test

The HFC-6000 Control System was subjected to an SWC test using both Combination and Ring Waveforms. The HFC-6000 Test Specimen satisfactorily met all of the acceptance criteria for surge testing. Some components were damaged as the result of the test pulses; but that damage was limited to the specific components under test, and the remainder of the system continued operating normally.

8.0 ABBREVIATIONS AND ACRONYMS

EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FPD	Flat Panel Display
HFC	HF Controls
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
I/O	Input/Output
RFI	Radio Frequency Interference
SWC	Surge Withstand Capability
TSAP	Test System Application Program
VCP	Vertical Coupling Plane

Non-Proprietary

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NON-PROPRIETARY

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NON-PROPRIETARY

HFC-6000 Control System

ERD111 – Control System Qualification Project

EMI Testing Summary Report

NON-PROPRIETARY

Appendix A

Operability and Prudency Tests

A.1 GENERAL

This attachment is to document the results of the Operability Tests and Prudency Test performed during the process of the EMI/RFI, ESD, and Surge Withstand qualification tests. The acceptance criteria against which the test results are evaluated were stipulated in the respective test procedures. Operability test and Prudency test results shall remain within the tolerance limits established by the baseline testing, as listed in Attachment A of Baseline Testing Summary Report. Any deviation from baseline results established during pre-qualification testing will be identified and recorded.

All the automated operability tests and prudency tests were run for about 5 minutes. These tests include AI Accuracy Test, AO accuracy test, RTD accuracy test, Pulse Input accuracy test, Digital Response time test, Analog Response Time test, Communication Test, Timer Test, Digital BOE test and Analog BOE test.

NON-PROPRIETARY

A.2 4-20 MA AI ACCURACY TEST

The tolerance limits for the automated AI accuracy test established in the pre-qualification test are shown in the Table A.2.1. Because deviations are introduced by the 100 cycle moving average function in the AI card combined with the asynchronous operation of the HAS logger, the AI accuracy during the Wyle qualification test will be checked against the baseline results instead of against the acceptance criteria.

A.2.1 Pre EMI/RFI Test

The automated AI accuracy test results from pre EMI/RFI test are presented in Table A.2-1 and Figure A.2-1. The results listed in the table were the calculations from one of the AI input test cycles. All but one measurement, i.e., 1.92% at 10% level, were within the tolerance limits. This result is consistent with the results from the post environmental test which was the test immediately proceeding the pre EMI/RFI test.

Table A.2.1. AI Accuracy from Pre EMI/RFI Test.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1.BL,506					
	3/3/04 8:30:38	11.92	Step Waveform	10.00	1.92
2,BL,215					

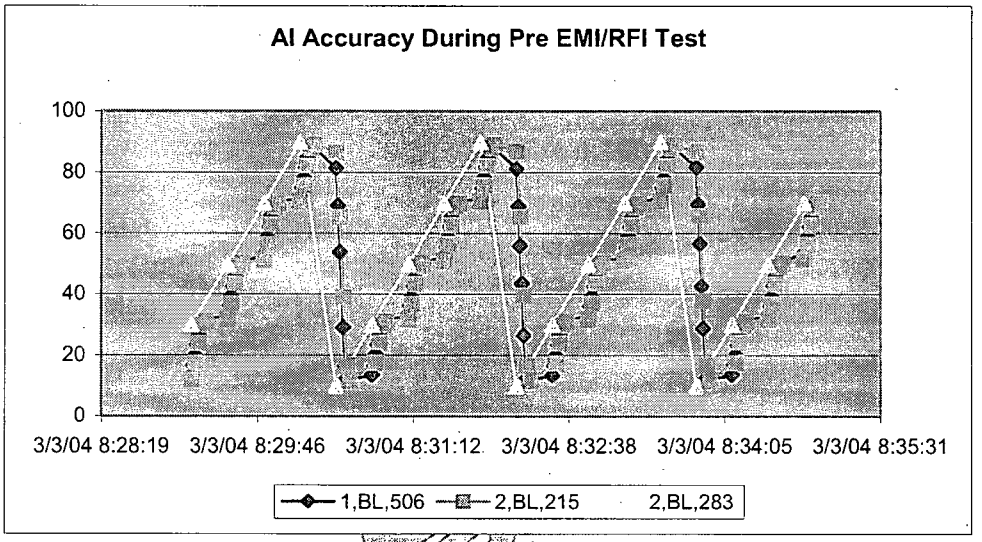

Figure A.2-A.2-1. AI Accuracy from Pre EMI/RFI Test.

A.2.2 Before Conducted Susceptibility Test

The automated AI accuracy testing results from the operability test performed before the conducted susceptibility test was performed are presented in Table A.2-2 and Figure A.2-2. The results listed in the table were the calculations from one of the AI input test cycles. Although at this time, measurements were out of the tolerance limits at both 10% and 30% levels, the accuracy of 1.05% at 30% level only barely missed the 1.04% limit.

Table A.2.2. AI Accuracy Before Conducted Susceptibility Test.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1,BL,506					
2,BL,215					

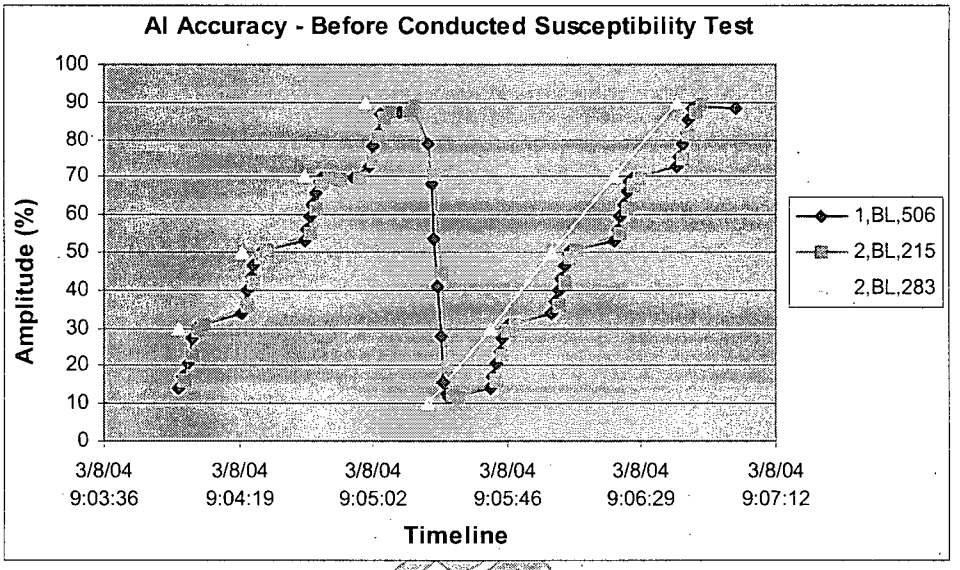

Figure A.2-A.2-2. AI Accuracy Before Conducted Susceptibility Test.

PROPRIETARY

A.2.3 Pre ESD Test

The automated AI accuracy testing results from pre ESD test are presented in Table A.2-3 and Figure A.2-3. The results listed in the table were the calculations from one of the AI input test cycles. Similar to Pre Susceptibility test, measurements were out of the tolerance limits at both 10% and 30% levels, though the accuracy of 1.11% at 30% level is only slightly higher than the 1.04% limit.

Table A.2.3. AI Accuracy During Pre ESD Test.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1,BL,506					
2,BL,215					

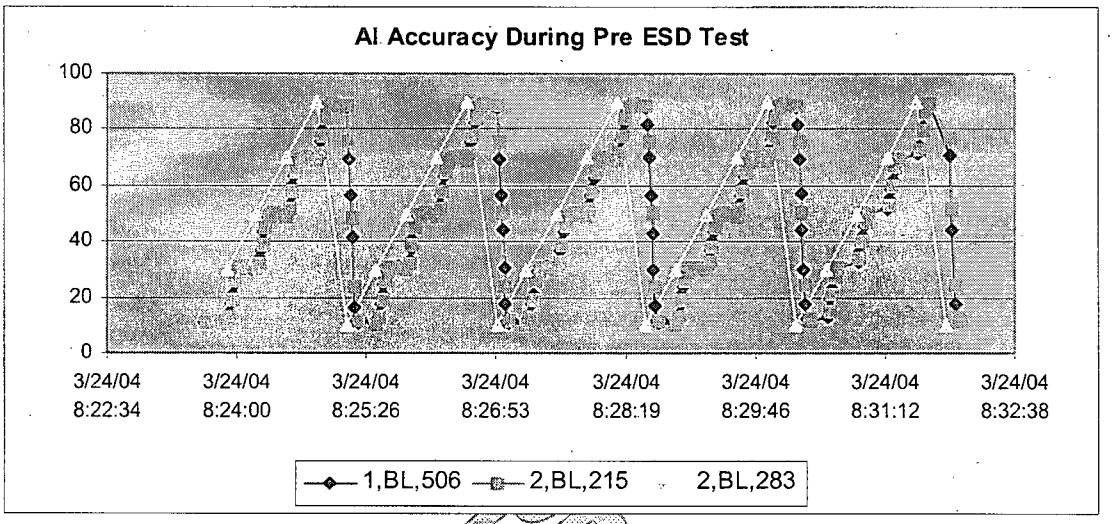

Figure A.2-A.2-3. AI Accuracy During Pre ESD Test.

PROPRIETARY

A.2.4 Pre Surge Withstand Test

The automated AI accuracy testing results from pre Surge Withstand test are presented in Table A.2-4 and Figure A.2-4. The results listed in the table were the calculations from one of the AI input test cycles. Similar to Pre EMI test, all but one measurement, i.e., 1.21% at 10% level, were within the tolerance limits. This result is consistent with the results from the post environmental test.

Table A.2-4. AI During Pre Surge Withstand Test.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1,BL,506					
2,BL,215					

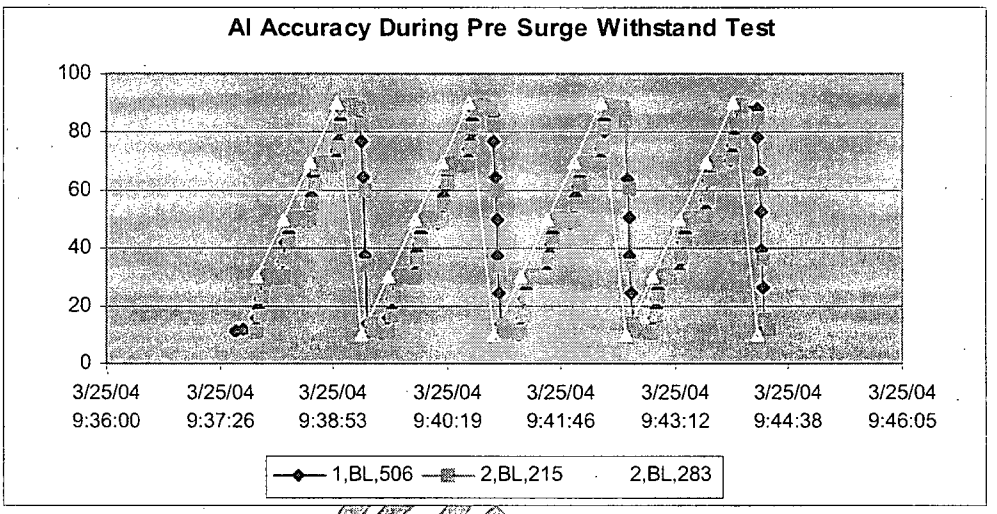

Figure A.2-A.2-4. AI Accuracy During Pre Surge Withstand Test.

PROPRIETARY

A.2.5 During Surge Withstand Test

Table A.2-5. AI Accuracy after Performing Combination Signal Surge Test and AC36 Replacement.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1,BL.506					
2,BL.215					

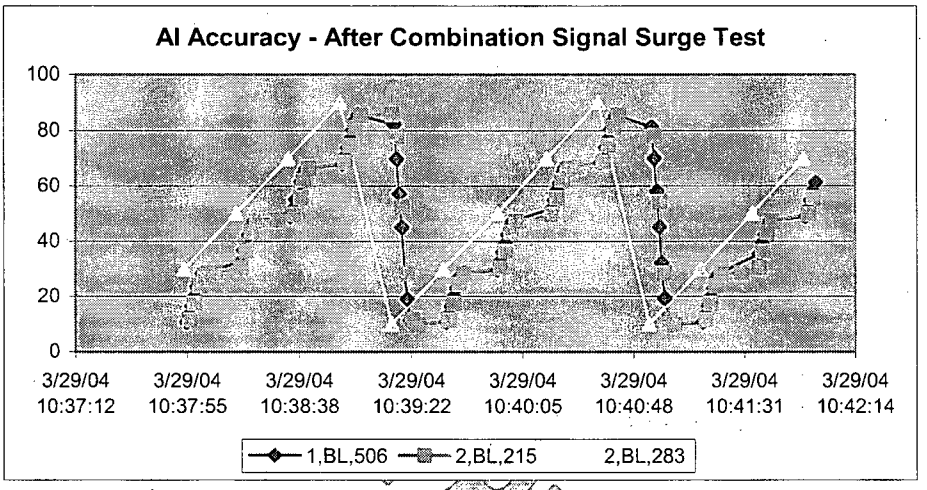

Figure A.2-A.2-5. AI Accuracy after Performing Combination Signal Surge Test and AC36 Replacement.

Table A.2-6. AI Accuracy after Applying TSAP Ringwaves.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1.BL,506					
2.BL,215					

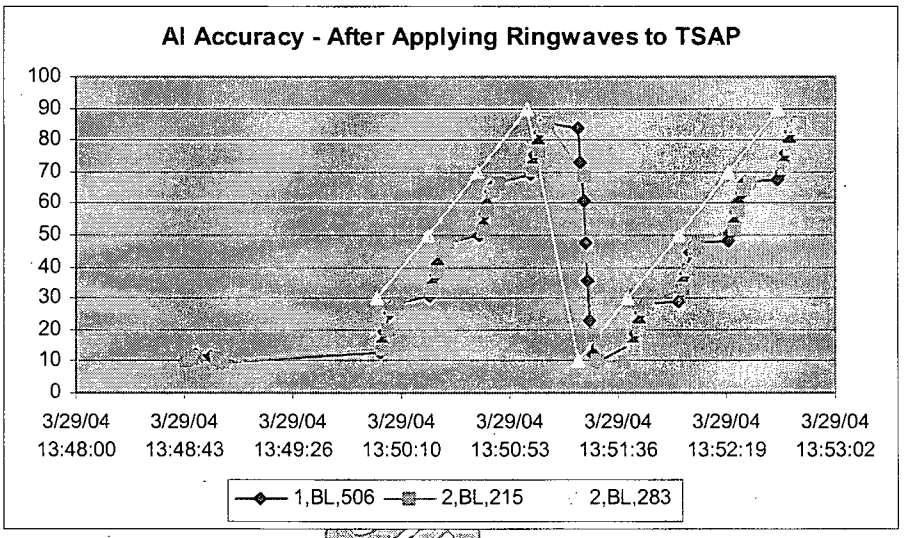

Figure A.2-A.2-6. AI Accuracy After Applying TSAP Ringwaves.

Table A.2-7. AI Accuracy after Applying SLC Ringwaves.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1,BL,506					
2,BL.215					

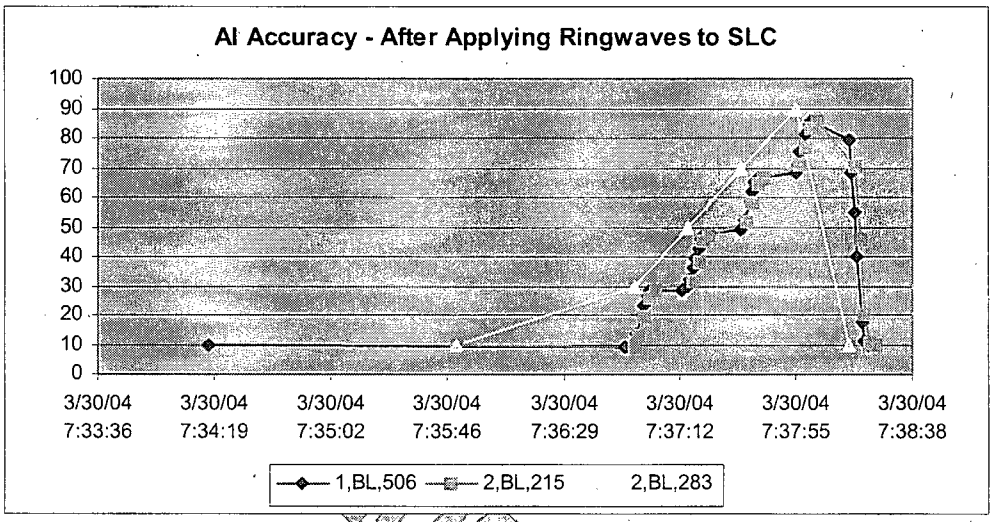

Figure A.2-A.2-7. AI Accuracy After Applying SLC Ringwaves.

PROPRIETARY

Table A.2-8. Last Time AI Okay in Surge Withstand

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1,BL,506					

Table A.2-9. First Indication of Significant Deviation in AI in Surge Withstand

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1,BL,506					

NON-PROPRIETARY

A.3 4-20 MA AO ACCURACY TEST

The baseline tolerance limits for the AO accuracy established from the pre-qualification test is ±0.49%.

A.3.1 Pre EMI Test

AO automated test data was not available in the pre EMI test. The reason is due to the TSAP limitation for the automated AO test as explained in Environmental Test Report. Table A.3-1 and Figure A.3-1 show the automated AO accuracy testing results from the operability test performed before the radiated Emission test which proceeded any other EMI/RFI tests. The test results are within tolerance limits.

Table A.3-1. AO Accuracy Test before Radiated Emission Test.

Tag Name	Time Stamp	Value (%)	Description	AO (%)	Accuracy (%)
2,BL,211					

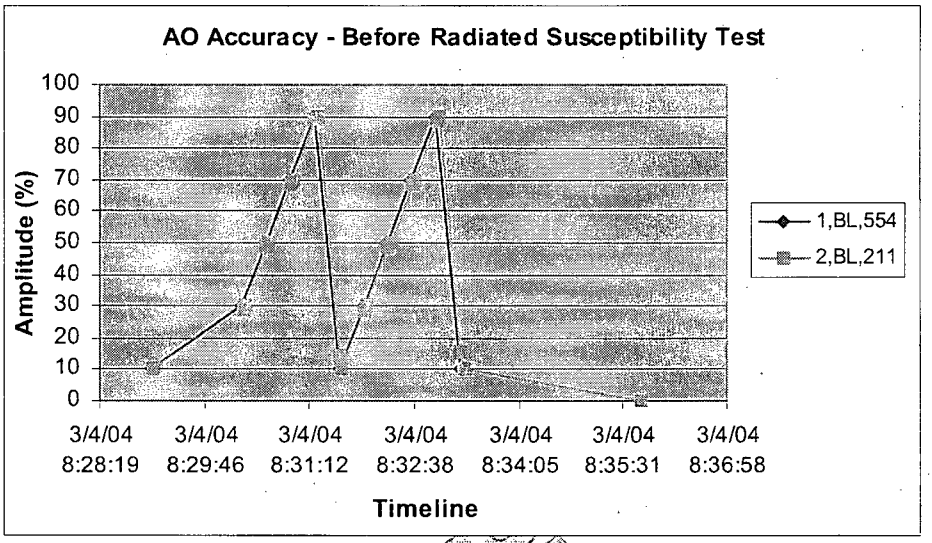

Figure A.3-1. AO Accuracy before Radiated Emission Test.

A.3.2 Pre ESD Test

Table A.3-2 and Figure A.3-2 show the automated AO accuracy testing results from the pre ESD test. The test results are within the tolerance limits.

Table A.3-2. AO Accuracy from Pre ESD Test.

Tag Name	Time Stamp	Value (%)	Description	AO (%)	Accuracy (%)
2,BL,211					

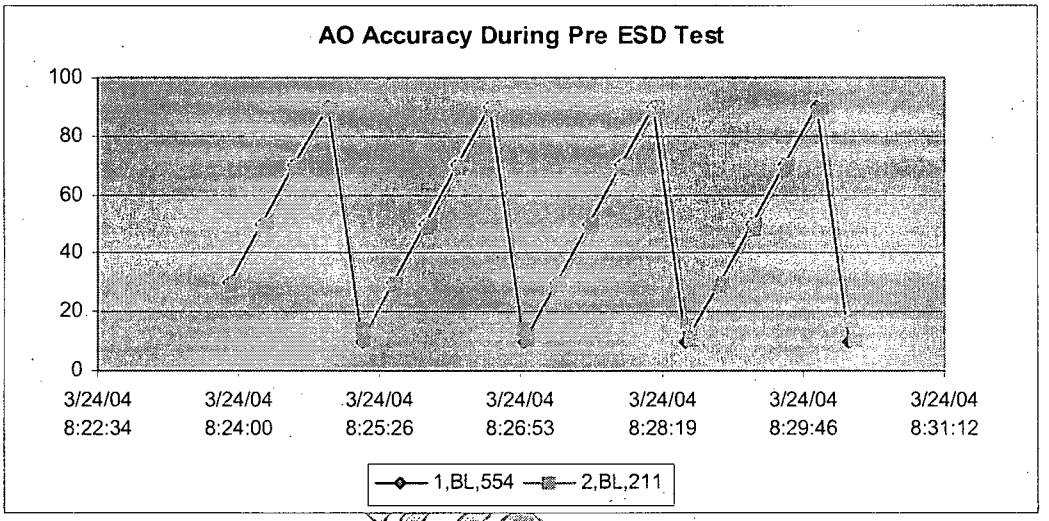

Figure A.3-2. AO Accuracy from Pre ESD Test.

PROPRIETARY

A.3.3 During Surge Withstand Test

Table A.3-3 and Figure A.3-3 show the automated AO accuracy testing results from the operability test performed after performing combination signal surge test and AC36 replacement. The test results are within tolerance limits.

Table A.3-3. AO Accuracy after Performing Combination Signal Surge Test and AC36 Replacement.

Tag Name	Time Stamp	Value (%)	Description	AO (%)	Accuracy (%)
2,BL,211					

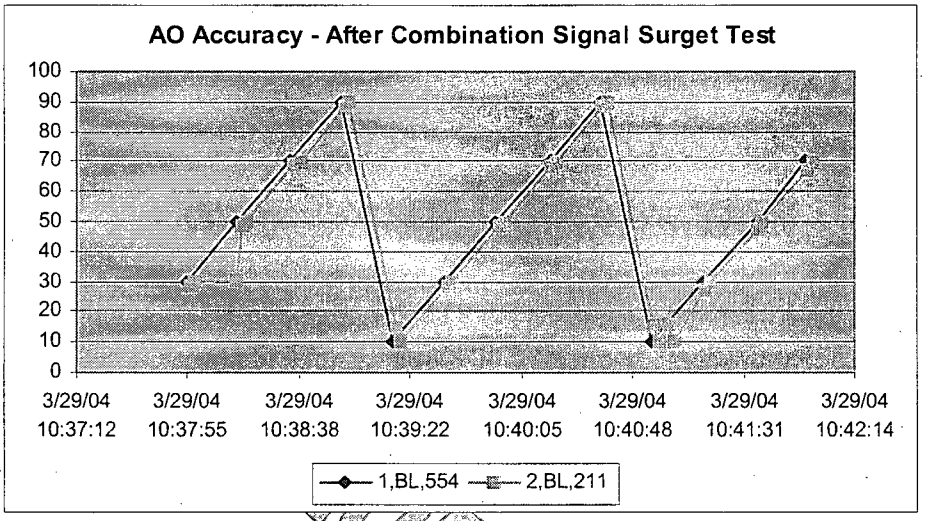

Figure A.3-3. AO Accuracy after Performing Combination Signal Surge Test and AC36 Replacement.

Table A.3-4 and Figure A.3-4 show the automated AO accuracy testing results from the operability test performed after performing ringwaves to TSAP. The test results are within tolerance limits.

Table A.3-4. AO Accuracy after Applying TSAP Ringwaves.

Tag Name	Time Stamp	Value (%)	Description (%)	AO (%)	Accuracy (%)
2,BL,211					

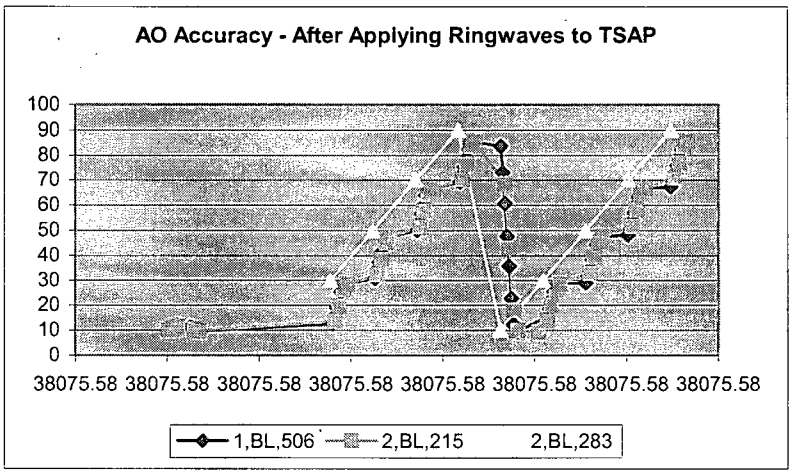

Figure A.3-4. AO Accuracy after Applying TSAP Ringwaves.

A.4 100 OHM RTD CARD

A.4.1 Pre EMI

The blocks related with RTD did not change in value through all the EMI tests. This is consistent with the results from environmental tests.

A.4.2 During Susceptibility

RS103 radiated susceptibility test was conducted on 3/8/04. Figure A.4-1 through A.4-4 shows value of RTD during this test.

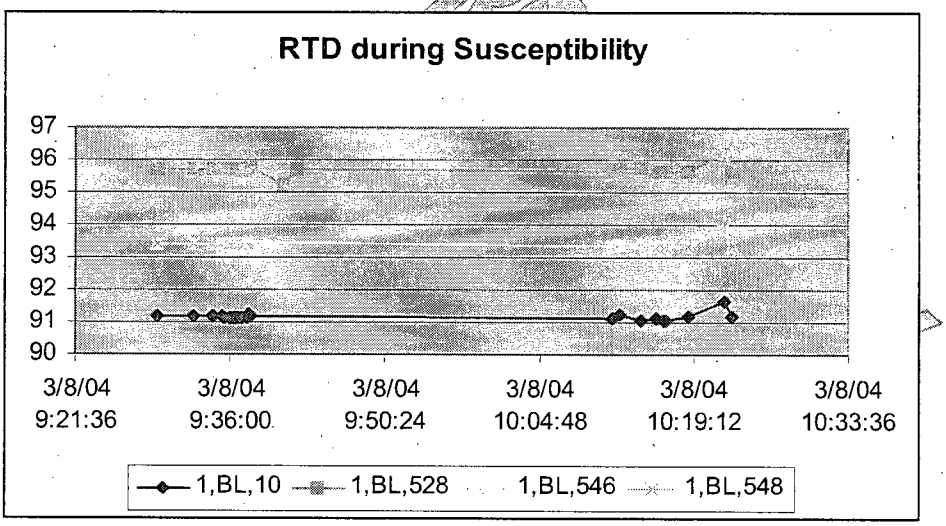

Figure A.4-1, RTD - Vertical Front 10 KHZ - 200 MHZ and Horizontal Front 30 MHZ - 200 MHZ

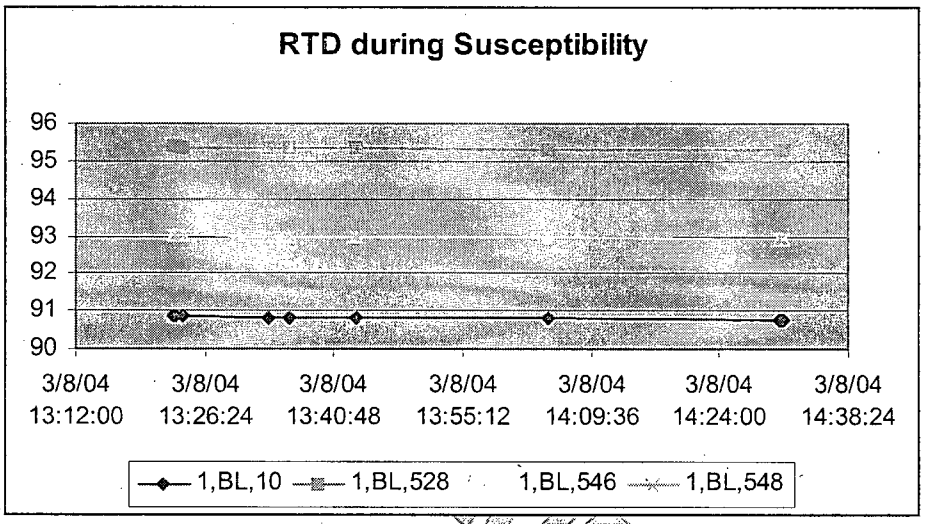

Figure A.4-2. RTD – Vertical Front 900 KHZ – 1.6 MHZ, 6.3 MHZ – 200 MHZ, 6 MHZ – 10 MHZ

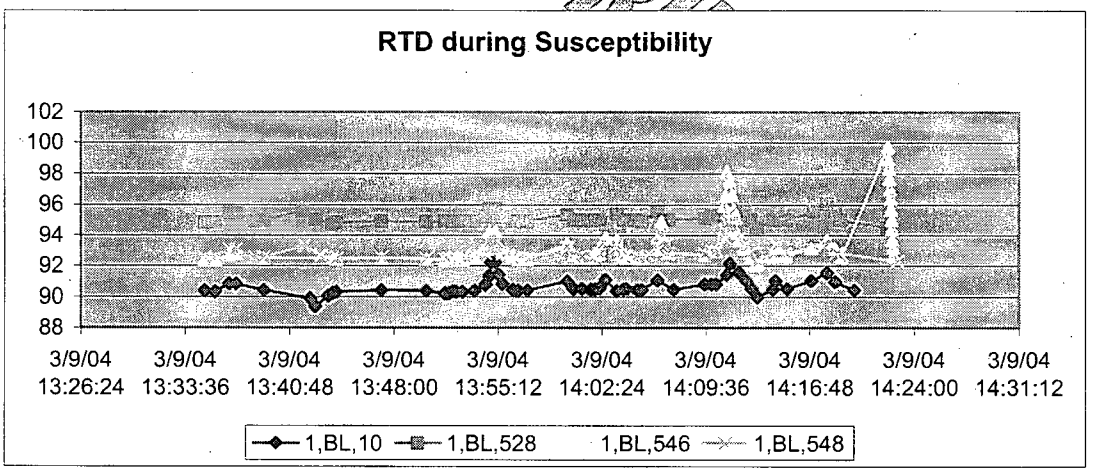

Figure A.4-3. RTD – 50 KHZ – 400 MHZ

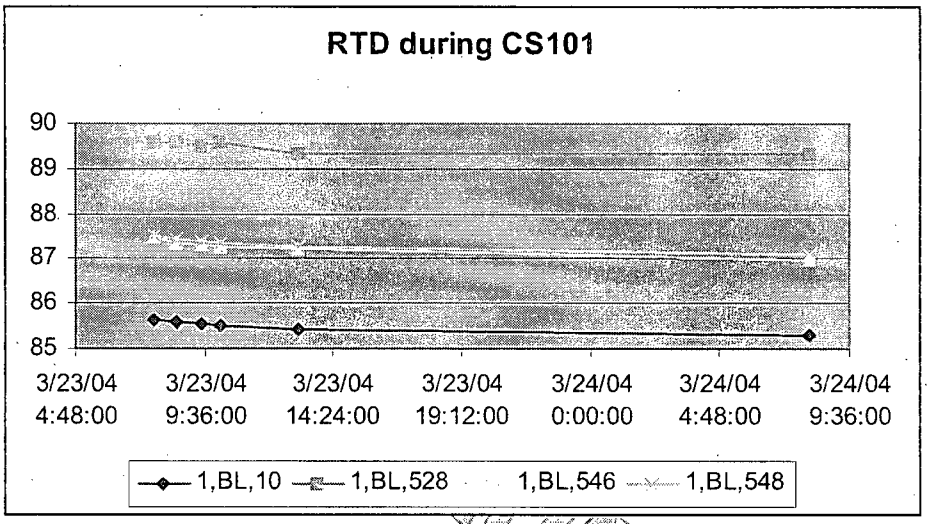

Figure A.4-4. RTD during CS101.

A.4.3 Pre ESD

There was no logged data in the HAS output for the RTD, which means that the output did not change by more than 0.5%.

A.5 PULSE INPUT CARD

Table A.5-1. Pulse Input During Pre EMI Test

Tag Name	Time Stamp	Value	Description
1,BL,535			
1,BL,557			

During the tests, the pulse input value was not logged in the HAS output, which means that the change of the values is no more than 0.5%.

A.6 ICL COMMUNICATION OPERABILITY TEST

A.6.1 During Radiated Susceptibility Test (1) – 03/05/04

Screen captures were taken for ICL error counters at the start and at the end of the radiated susceptibility test on 3/5/04, from 8:41 AM to 4:50 PM. Six modules in rack 2 showed some errors as listed in Table A.6-1. Refer to the conclusions at the end of Section A.6 for an explanation of the ICL communication errors tabulated in Tables A.6-1 through A.6-12.

Table A.6-1. ICL Error Counter During Radiated Susceptibility Test (1).

ICL Communication Error Counters – 03/05/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
0	KAI8				
0	KAI8				
60	KAI8				

Non-Proprietary

A.6.2 During Radiated Susceptibility Test (2) – 03/08/04

Screen captures were taken for ICL error counters at the start and at the end of the radiated susceptibility test on 3/8/04, from 9:30 AM to 3:14 PM.

Table A.6-2. ICL Errors During Radiated Susceptibility Test (2).

ICL Communication Error Counters – 03/08/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
0	KAI8				
0	KAI8				
60	KAI8				

Non-Proprietary

A.6.3 During Conducted Susceptibility Test (1) – 03/09/04

Screen captures were taken for ICL error counters at the start and at the end of the conducted susceptibility test on 3/9/04, from 1:09 PM to 3:58 PM, during which 50 KHZ -400 MHZ at 95% signal strength was applied on the AC power bundle powering the TSAP.

From 3:58 PM to 4:41 PM, 50 KHZ -100 MHZ at 71% signal strength was applied on AC power bundle.

Table A.6-3. ICL Error Counters During Conducted Susceptibility Test (1) – 50 KHZ - 400 MHZ at 95%.

ICL Communication Error Counters – 03/09/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
0	KAI8				
0	KAI8				
60	KAI8				

Table A.6-4. ICL Error Counters During Conducted Susceptibility Test (1) – 50 KHZ-100 MHZ at 71%.

ICL Communication Error Counters – 03/09/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
0	KAI8				
0	KAI8				
60	KAI8				

NON-PROPRIETARY

A.6.4 During Conducted Susceptibility Test (2)– 03/10/04

Screen captures were taken for ICL error counters at the start and at the end of the conducted susceptibility test on 3/10/04, from 8:04 AM to 10:55 AM, during which 100-400 MHZ at 71% signal strength was applied on the AC power bundle powering the TSAP.

From 11:31 AM to 3:23 PM, 50 KHZ to 400 MHZ at 100% signal strength was applied on AC power hot wire powering the TSAP

From 3:24 PM to 4:47 PM, 50 KHZ to 400 MHZ at 75% signal strength was applied to the AC power hot wire powering the TSAP.

NON-PROPRIETARY

Table A.6-5. ICL Error Counters During Conducted Susceptibility Test (2) – 100-400 MHZ at 71%.

ICL Communication Error Counters – 03/10/04					
Station	**Card Type**	**Start Count**	**End Count**	**Count Diff**	**Comments**
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				

0	KAI8				
0	KAI8				
60	KAI8				

Table A.6-6. ICL Error Counters During Conducted Susceptibility Test (2) – 50 KHZ – 400 MHZ at 100%

ICL Communication Error Counters – 03/10/04					
Station	**Card Type**	**Start Count**	**End Count**	**Count Diff**	**Comments**
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
0	KAI8				
0	KAI8				
60	KAI8				

Table A.6-7. ICL Error Counters During Conducted Susceptibility Test (2) – 50 KHZ –400 MHZ at 75%

ICL Communication Error Counters – 03/10/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
0	KAI8				
0	KAI8				
60	KAI8				

NON-PROPRIETARY

A.6.5 During Conducted Susceptibility Test (3) – 03/11/04

Screen captures were taken for ICL error counters at the start and at the end of the conducted susceptibility test on 3/11/04, from 7:40 AM to 9:26 AM, during which 100-400 MHZ at 75% signal strength was applied on the AC power hot wire powering the TSAP.

Table A.6-8. ICL Error Counters During Conducted Susceptibility Test (3) – 100-400 MHZ at 75%.

ICL Communication Error Counters – 03/11/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
0	KAI8				
0	KAI8				
60	KAI8				

Non-Proprietary

A.6.6 During Conducted Susceptibility Test (4)– 03/23/04

Screen captures were taken for ICL error counters at the start and at the end of the conducted susceptibility test on 3/23/04, from 7:52 AM to 8:15 AM, during which CS 101 test was performed on TSAP hot wire.

From 8:35 AM to 9:11 AM, CS 101 test was conducted on TSAP low wire. The screen capturing results showed that no errors occurred as shown in Table A.6-10.

Table A.6-9. ICL Error Counters – CS101, TSAP High Wire.

ICL Communication Error Counters – 03/23/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
58	KAI8				
59	KAI8				
60	KAI8				

PROPRIETARY

Table A.6-10. ICL Error Counters – CS101, TSAP Low Wire.

ICL Communication Error Counters – 03/23/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
58	KAI8				
59	KAI8				
60	KAI8				

Non-Proprietary

A.6.7 During ESD Test – 03/24/04

Screen captures were taken for ICL error counters at the start and at the end of the ESD test on 3/24/04, from 8:42 AM to 4:15 PM

Table A.6-11. ICL Error Counters During ESD Test.

ICL Communication Error Counters – 03/24/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
0	PCC03				
0	PCC03				
0	PCC06				
0	PCC06				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
58	KAI8				
59	KAI8				
60	KAI8				

NON-PROPRIETARY

A.6.8 During Surge Withstand Test

Screen captures were taken for ICL error counters at the start and at the end of the Surge Withstand test on 3/25/04, from 9:41 AM to 3:08 PM.

Table A.6-12. ICL Error Counters During Surge Withstand Test.

ICL Communication Error Counters – 03/25/04					
Station	Card Type	Start Count	End Count	Count Diff	Comments
Remote 1					
0	KPD16				
1	KPD16				
3	KPD16				
5	KDI16				
6	KDO8				
7	KDO8				
16	KDI16				
17	KPD16				
19	KDI16				
20	KPD16				
22	KDI16				
23	KDO8				
24	KDO8				
25	KDI16				
26	KPD16				
36	KDI16				
37	KDI16				
38	KDO8				
39	KDO8				
40	KDO8				
48	KAIO				
49	KAO8				
50	KAIO				
51	KAIO				
52	KAI16				
53	KAI16				
54	KAO8				
56	KAI8				
57	KAIO				
58	KAI8				
59	KAI8				
60	KAI8				

Conclusions:

The ICL communication test was executed during each of the EMI/RFI susceptibility, ESD, and surge withstand tests. A total of 12 tests were run on the Test Specimen with the test duration lasting up to eight hours, depending on the type of test being executed. The method of test execution consisted of taking a screen capture of the ICL error counters before the start of the test run and then again after completion of the test run. The difference between the error counter value represents the total number of ICL errors detected for a particular I/O module throughout the course of the test run. (The error counter consisted of a single 16-bit binary count field without carry that rolls over from FFFFH to 0000H.) The following conclusion have been drawn from a detailed examination of the accumulated data:

NON-PROPRIETARY

A.7 TIMER TEST

The timer function is controlled by the main processor OS. The timers controlled two DO images - that data was transferred via the ICL to a DO8J module, and the resulting signals were routed to the SOE interface via a cable assembly.

Tables A.7.1 and A.7.2 summarize the SOE data for the timer test accumulated during the Pre-EMI/RFI and Pre-ESD tests. The parameters listed in the tables are defined as follows:

Preset Value	Set timer interval in application program in seconds
Duration	Measured on/off time in seconds
Duration Deviation	The averaged deviation of the observed timer interval expressed as a percentage value.
Duration Jitter	The averaged difference between successive timer intervals expressed as a percentage value.
Period	Total measured period of signal waveform in seconds
Period Deviation	The averaged deviation of the measured waveform period expressed as a percentage.
Period Jitter	The averaged difference of successive periods from the preset value expressed as a percentage.

NON-PROPRIETARY

A.7.1 Pre EMI/RFI

The results from automated timer test during the pre EMI/RFI test are listed in Table /A,7-1. The number listed in the table is the average result of 16-18 measurements for the 4,DI,12 (5 second on and 1 second off waveform) and 51-53 measurements for the 4,DI,11 (1 second on and 1 second off waveform).

Table A.7-1. Automatic Timer Test Result from the Pre EMI-RFI Test.

		Preset Value (s)	Duration (s)	Duration Deviation (%)	Duration Jitter (%)	Period (s)	Period Deviation (%)	Period Jitter (%)
4,DI,12	ON	5						
	Number of Measurement							
	OFF	1						
	Number of Measurement							
4,DI,11	ON	1						
	Number of Measurement							
	OFF	1						
	Number of Measurement							

NON-PROPRIETARY

A.7.2 Pre ESD Test

The results from automated timer test during the pre ESD test are listed in Table /A,7-2. The number listed in the table is the average result of 16-18 measurements for the 4,DI,12 (5 second on and 1 second off waveform) and 53-55 measurements for the 4,DI,11 (1 second on and 1 second off waveform).

Conclusions:

- No disruption in the timer waveform was observed during either the Pre-EMI/RFI or the Pre-ESD tests.
- All timer periods remained within the theoretical tolerance limit established in the baseline report.

Table A.7-2. Automatic Timer Test Result from the Pre ESD Test.

		Preset Value (s)	Duration (s)	Duration Deviation (%)	Duration Jitter (%)	Period (s)	Period Deviation (%)	Period Jitter (%)
4,DI,12	ON	5						
	Number of Measurement							
	OFF	1						
	Number of Measurement							
4,DI,11	ON	1						
	Number of Measurement							
	OFF	1						
	Number of Measurement							

NON-PROPRIETARY

A.8 DIGITAL BOE TEST

A.8.1 Pre EMI/RFI

SOE data from the pre EMI/RFI test was analyzed. By analyzing the alarm reports throughout the EMI-RFI test, it is concluded that no link alarm condition was detected for the DI cards whose channels were logged by SOE logger.

Table A.8-1. Digital BOE Abnormal Transitions in the Pre EMI/RFI Test.

Time Stamp			Transition Time Duration (Seconds)						
H	M	S	4,DI,30	4,DI,29	4,DI,28	4,DI,27	4,DI,26	4,DI,25	4,DI,24
8	39	56.5							
8	39	56.5							
Total Number of Transitions									
Total Number of Contact Bounce									
Total Number of Anomalies									

NON-PROPRIETARY

A.8.2 Pre ESD

Analysis of the logged data records has confirmed that every transition was detected for all seven logged digital channels (4,DI,24 to 4, DI,30). No link alarm condition was recorded for the digital modules processing the BOE signals during the ESD test.

As shown in Table A.8-2, neither abnormal transition nor contact bounce was detected throughout the entire pre-ESD test.

Table A.8-2. Digital BOE Abnormal Transitions in the Pre-ESD Test.

Time Stamp			Transition Time Duration (Seconds)						
H	M	S	4,DI,30	4,DI,29	4,DI,28	4,DI,27	4,DI,26	4,DI,25	4,DI,24
Total Number of Transitions									
Total Number of C00ontact Bounce									
Total Number of Anomalies									

A.8.3 Pre Surge Withstand

This test was performed; however, no SOE or HAS data is available. The power supply output voltages were recorded to be within tolerance. The test procedure as written was based on the assumption that the equipment would be reassembled immediately prior to this test. However; the equipment had been reassembled in the test area for the EMI/RFI testing several days earlier and operability and prudency tests had been run at that time. As a result, this test was not needed for the purpose of verifying Test Specimen operability.

A.9 ANALOG BOE TEST

The analog burst of events (BOE) test consists of a free-running analog square wave signal that switches between 10% and 90% of full span with a 10-second dwell time at each level. The waveforms during the various tests are shown in Figures A.9.1 through A.9.6 and the associated readings and deviations are presented in Tables A.9.1 through A.9.6.

NON-PROPRIETARY

A.9.1 Pre EMI/RFI

The waveforms of TSAP analog inputs at remote 1 and that of the driving BOE signal during the pre EMI/RFI are depicted in Figure A.9-1. The TSAP AI signals are seen to correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table A.9-1 lists the averaged readings and deviations of 15 measurements for these HAS logged AI signals at 10% and 90% levels. The averaged deviations at 10% for 1,BL,510 and 1,BL,514 meet the 0.32% acceptance criteria, which is in line with the pre environmental results.

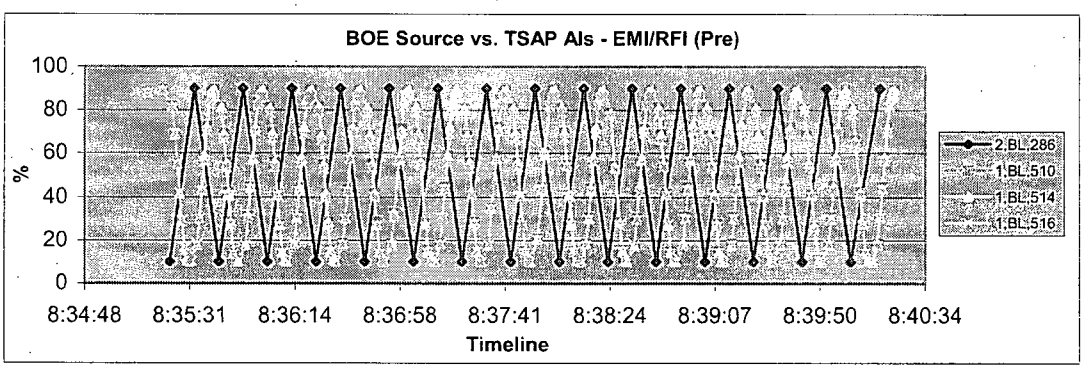

Figure A.9-1. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 in the Pre EMI/RFI Test.

Table A.9-1. TSAP AI Channel Readings and Deviations from BOE Source Signal in Pre EMI/RFI Test.

	1,AI,882 (1,BL,510)	1,AI,884 (1,BL,514)	1,AI,901 (1,BL,516)
10% Measurement (%)			
Deviation From 10% (%)			
Num of Measurements			
90% Measurement (%)			
Deviation From 90% (%)			
Num of Measurements			

PROPRIE

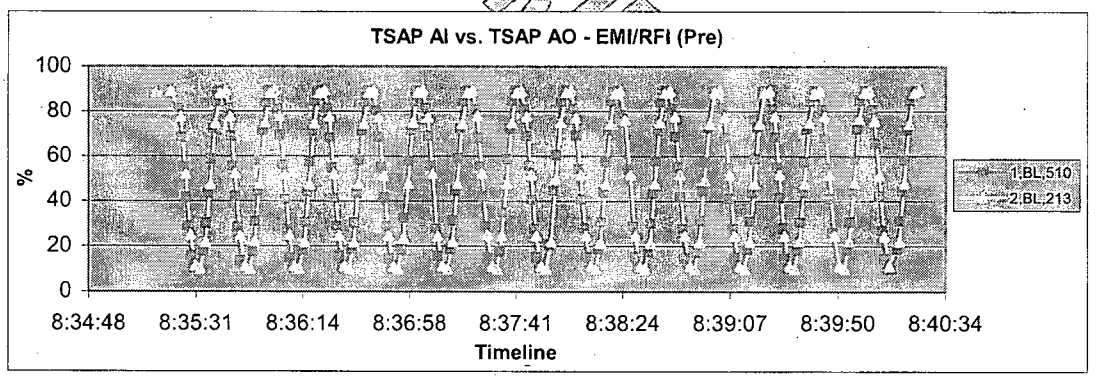

Figure A.9-2. Logged TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) in Pre EMI/RFI Test.

Figure A.9-2 shows the waveforms for HAS logged TSAP AO (2,BL,213) versus its corresponding TSAP AI (1,BL,510) during the pre EMI/RFI test. The AO image duplicates the AI image at each transition. The averaged readings and deviations for these two analog signals at 10% and 90% levels are listed in Table A.9-2. Deviations of 2,BL,213 from 1,BL,510 at both 10% and 90% levels meet the 0.3% acceptance criteria, which is in line with pre-qualification results. More specifically, the deviations in pre EMI/RFI test are 0.119% at 10% and 0.047% at 90% level, a significant reduction from 0.276% at 10% and 0.274% at 90% level from pre-qualification test.

Table A.9-2. TSAP AOs and the Corresponding TSAP AIs in Remote1 in the Pre EMI/RFI Test.

	1,AI,882 (1,BL,510)	1,AO,922 (2,BL,213)	Deviation (2,BL,213 vs. 1,BL,510) (%)
10% Measurement (%)			
Number of Measurements			
90% Measurement (%)			
Number of Measurements			

PROPRIETARY

A.9.2 Pre ESD

The waveforms of TSAP analog inputs at remote 1 and that of the driving BOE signal during the pre ESD are depicted in Figure A.9-3. The figure shows that the TSAP AI signals correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table A.9-3 lists the averaged readings and deviations of 19-20 and 21 measurements for these HAS logged AI signals at 10% and 90% levels respectively.

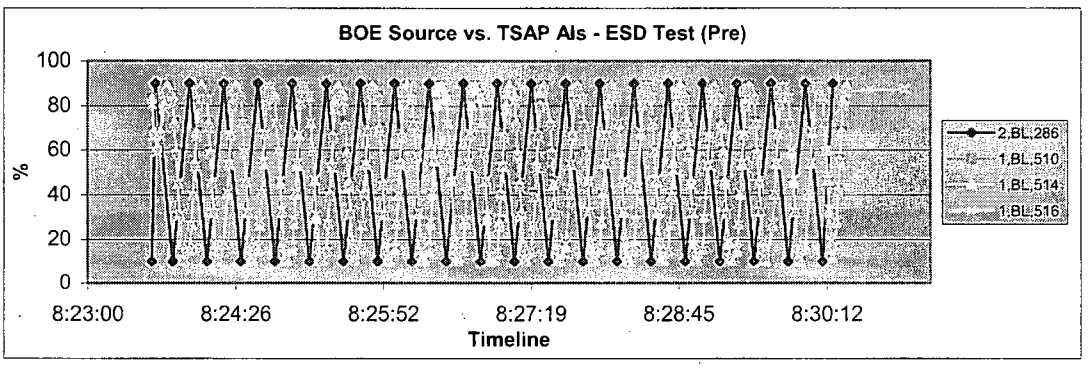

Figure A.9-3. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 in the Pre ESD Test

Table A.9-3. TSAP AI Channel Readings and Deviations from BOE Source Signal in Pre ESD Test

	1,AI,882 (1,BL,510)	1,AI,884 (1,BL,514)	1,AI,901 (1,BL,516)
10% Measurement (%)	10.082± 0.033	10.051± 0.034	10.972 ± 0.673
Deviation From 10% (%)	0.083 ± 0.030	0.056 ± 0.024	0.972 ± 0.673
Num of Measurements	19	19	20
90% Measurement (%)	89.260 ± 0.034	89.176 ± 0.065	87.555 ± 0.778
Deviation From 90% (%)	0.740 ± 0.034	0.824 ± 0.065	2.445 ± 0.778
Num of Measurements	21	21	21

Proprietary

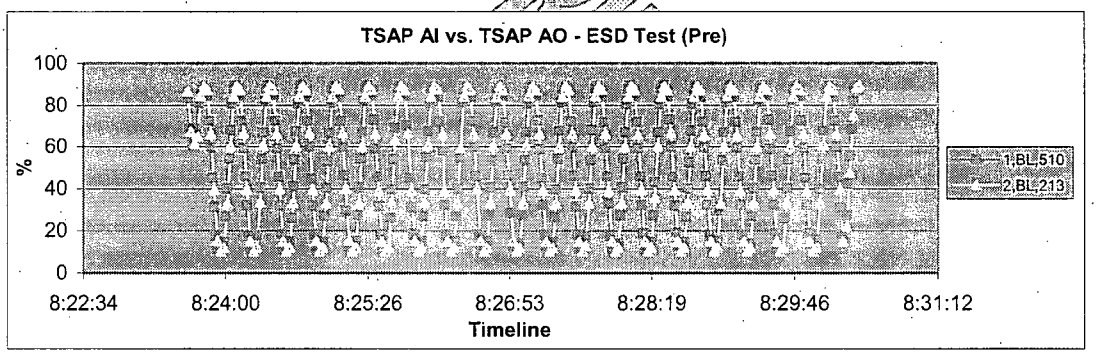

Figure A.9-4. Logged TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) in Pre ESD Test.

Figure A.9-4 shows the waveforms for HAS logged TSAP AO (2,BL,213) versus its corresponding TSAP AI (1,BL,510) during the pre ESD test. The figure shows that the AO image duplicates the AI image at each transition. The averaged readings and deviations for these two analog signals at 10% and 90% levels are listed in Table A.9-4.

Table A.9-4. TSAP AOs and the Corresponding TSAP AIs in Remote1 in the Pre ESD Test.

	1,AI,882 (1,BL,510)	1,AO,922 (2,BL,213)	Deviation (2,BL,213 vs. 1,BL,510) (%)
10% Measurement (%)			
Number of Measurements			
90% Measurement (%)			
Number of Measurements			

NON-PROPRIETARY

A.9.3 Pre Surge Withstand

The waveforms of TSAP analog inputs at remote 1 and that of the driving BOE signal during the pre surge withstand are depicted in Figure A.9-5. The TSAP AI signals are seen to correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table A.9-5 lists the averaged readings and deviations of 17 and 18 measurements for these HAS logged AI signals at 10% and 90% levels respectively.

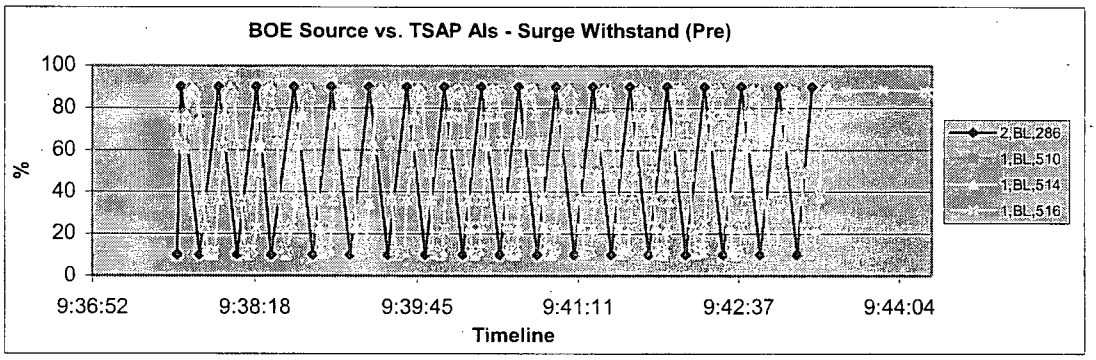

Figure A.9-5. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 in the Pre Surge Withstand Test.

Table A.9-5. TSAP AI Channel Readings and Deviations from BOE Source Signal in Pre Surge Withstand Test.

	1,AI,882 (1,BL,510)	1,AI,884 (1,BL,514)	1,AI,901 (1,BL,516)
10% Measurement (%)			
Deviation From 10% (%)			
Num of Measurements			
90% Measurement (%)			
Deviation From 90% (%)			
Num of Measurements			

UNPROPRI

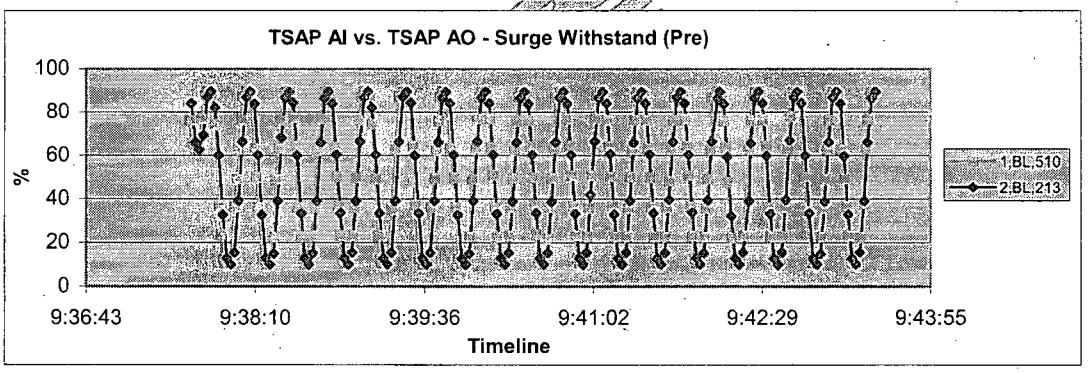

Figure A.9-6. Logged TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) in Pre Surge Withstand Test.

Figure A.9-6 shows the waveforms for HAS logged TSAP AO (2,BL,213) versus its corresponding TSAP AI (1,BL,510) during the pre surge withstand test. The figure shows that the AO image duplicates the AI image at each transition. The averaged readings and deviations for these two analog signals at 10% and 90% levels are listed in Table A.9-6.

Table A.9-6. TSAP AOs and the Corresponding TSAP AIs in Remote1 in the Pre Surge Withstand Test.

	1,AI,882 (1,BL,510)	1,AO,922 (2,BL,213)	Deviation (2,BL,213 vs. 1,BL,510)
10% Measurement (%)	10.101 ± 0.225	9.965 ± 0.019	0.227 ± 0.133
Number of Measurements	17	17	17
90% Measurement (%)	89.367 ± 0.209	89.366 ± 0.027	0.180 ± 0.080
Number of Measurements	18	18	18

Conclusion:

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Appendix B

Susceptibility Test Alarm Analysis

B.1 GENERAL

The susceptibility tests include the following:

- Radiated EMI/RFI Susceptibility Test: RS103. The frequency range for the radiated test signal is from 10 KHZ to 1 GHZ. The overall test will be divided into several frequency ranges with a different signal source and antenna for each frequency range. Each test will be executed twice: one with the antenna positioned at front center of the Test Specimen and once with the antenna at rear center.

- Conducted Low Frequency EMI/RFI Susceptibility Test: CS101. Test signals between 30 HZ and 50 KHZ were injected directly into power leads of the Test Specimen. Two tests were executed: one for power module A of the redundant power supply and one for the non-redundant power supply of the single-loop rack.

- Conducted High Frequency EMI/RFI Susceptibility Test: CS114. Test signals between 50 KHZ and 400 MHZ were inductively coupled into power leads and selected I/O cables of the test specimen as shown in Table B.1-1.

Table B.1.1. Conducted High Frequency Susceptibility Test Cases.

Test Case	Cable	Description
1	Power source A	120-vac power source for redundant power module A
2	Power source	120-vac power source for single-loop power supply
3	01-2-7	I/O cable to HFC-DI16I digital input card
4	01-2-9	I/O cable to HFC-DO8J digital output card
5	01-4-9	I/O cable to HFC-AI8M RTD input card
6	01-4-5	I/O cable to HFC-AI16F analog input card
7	01-4-7	I/O cable to HFC-AO8F analog output card
8	01-4-12	I/O cable to HFC-AI4K pulse input card
Note: The status of one or more I/O points for test cases 3 through 8 are monitored by the Operability and Prudency BOE trends.		

A portion of the Operability and Prudency Tests were run and monitored for signs of susceptibility. The susceptibility test was run from 3/5/04 to 3/12/04 and then from 3/22/04 to 3/23/04.

The acceptance criteria for susceptibility is as follows:

EPRI TR-102323-R1 Appendix B Paragraphs 3.1 and 3.2 and Wyle Test Procedure 50044-10 list the maximum signal strength for each of the susceptibility tests. Each test will be run at 100% of the indicated signal strength. Lack of susceptibility is demonstrated by the following acceptance criteria:

NOTE

Objective demonstration of these criteria will be provided by the alarm process function and results of the Operability and Prudency BOE tests that will be running while the test signals are being injected to the Test Specimen.

- All Test Specimen microprocessors continue to function normally.
- Transfer of I/O data over serial links is not disrupted.
- Serial communication links exhibit no increase in communication error rates.
- Discrete I/O channels exhibit no spurious transitions.
- Analog I/O channels do not change by more than 3% while the EMI/RFI signal is being applied.

If a susceptibility condition is detected at the maximum signal level, the susceptibility threshold shall be identified and recorded.

The system alarms files were evaluated and compared with the test log book. If any anomalies were not recorded in the test log book, they were added to the test log. Then the anomalies were categorized by the related modules in order to identify components that are susceptible to test conditions.

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B.2 RS103

The test results of RS103 show that Test Specimen met acceptance criteria with one exception. The specific deviation is as follows:.

- The DC33 card at station 26 (rack 2, slot 11) went into alarm at 490 MHZ of Front Horizontal Test and about 16 MHZ of Front Vertical Test. It was functioning properly during the Rear Horizontal and Rear Vertical Tests. There are other DC33 cards in the Test Specimen, and none of them had any problem during the RS103 test.

Tables B.2-1, B.2-2, B.2-3 show the RS103 susceptibility test results. Any single module failure is noted by an "X" mark in the "No" column.

Table B.2-1. RS103 Test Results – Front Horizontal.

Susceptibility Data Analysis								
RS103								
Measurement Point: Front Horizontal								
Test MHZ	Frequency	Deleted	Deleted	Deleted	System Functioning		Susceptibility Threshold Level For Others	Comments

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Table B.2-2. RS103 Test Results – Front Vertical.

Susceptibility Data Analysis						
RS103						
Measurement Point: Front Vertical						
Test Frequency MHZ	**Deleted**	**Deleted**	**Deleted**	**System Functioning**	**Susceptibility Threshold Level For Others**	**Comments**

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Table B.2-3. RS103 Test Results – Rear Vertical and Rear Horizontal.

Susceptibility Data Analysis								
RS103								
Measurement Point: Rear Vertical								
Test Frequency MHZ		**Deleted**	**Deleted**	**Deleted**	**System Functioning**		**Susceptibility Threshold Level For Others**	**Comments**
					Yes	**No**	**V/m**	

Test Frequency MHZ				System Functioning		Susceptibility Threshold Level For Others	Comments
				Yes	No	V/m	

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B.3 CS114

Detailed analysis of results indicate that the Test Specimen exhibited some degree of susceptibility to conducted test signals for most of the frequencies ranges. Specific areas of susceptibility were as follows:

- RTD input card went into alarm sometimes during the CS114 test for the test specimen.
- DC33 at station 26 went into alarm during High Lead /Hot Wire test for test specimen.

Table B.3-1 and Table B.3-2 show the CS114 susceptibility test results. Column 2 and 3 present the results for the whole system, i.e., any individual module's failure is considered that the system failed. Columns 4 and 5 present the results for the rest of the system.

Non-Proprietary

Table B.3-1. CS114 on Test Specimen.

Susceptibility Data Analysis										
CS114										
High/Return Bundle										
Test Frequency MHZ	**Whole System Functioning**		**Susceptibility Threshold Level**	**TC Functioning**		**C-Link Functioning**		**Other System Functioning**		**Comments**
	Yes	**No**	**V/m**	**Yes**	**No**	**Yes**	**No**	**Yes**	**No**	
High Lead / Hot Wire										
Test Frequency MHZ	**Whole System Functioning**		**Susceptibility Threshold Level**	**TC Functioning**		**C-Link Functioning**		**Other System Functioning**		**Comments**
	Yes	**No**	**V/m**	**Yes**	**No**	**Yes**	**No**	**Yes**	**No**	

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B.4 CS101

The test results of CS101 show that the test specimen was not susceptible to the interference signals injected onto the input power lines. System alarms files have been reviewed and no anomalies were identified. DC33 at station 26 was in alarm at the beginning. It was later swapped with the DC33 card at station 27. The test was rerun and there were no more alarms from the DC33.

B.5 DETAILED ALARM ANALYSIS

A detailed alarm analysis was performed of the alarm records to identify the test in process and the specific source of the alarm.

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Appendix C

ESD and Surge Withstand Test Alarm Analysis

C.1 GENERAL

ESD test was conducted on 3/24/04.
Surge Withstand test was conducted from 03/25/04 to 03/29/04.

C.2 ESD TEST

The alarm file on 3/24/04 was analyzed and compared with test log. No abnormal events were identified.

C.3 SURGE WITHSTAND TEST

The alarm files for surge withstand tests were analyzed and compared with test log as shown in Table C.3-1. Most of alarms are due to test signals applied to test specimen. No abnormal events were identified in the alarm files.

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Table C.3-1. Surge Withstand Test Log and Alarms.

Date	Time	Event Description	Alarms
	(9:22 am)		
3/25/04	9:57am		
3/25/04			
3/25/04	12:50pm		
3/25/04	2:40pm		
3/25/04	3:19pm		
3/25/04	3:48pm		
3/25/04	4:13pm		

	(8:41:00 AM)		
3/26/04			
3/26/04	9:00am		
3/26/04	9:30am		
3/26/04	11:25am		
3/26/04	11:55am		
	(12:03 pm)		
3/26/04	12:41pm		
3/26/04	1:25pm		
3/26/04	1:41pm		
3/26/04	1:50pm		
	(2:00 pm)		
3/26/04	3:30pm		
3/26/04	3:45pm		

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3/29/04	9:00am		
3/29/04	10:58am		
3/29/04	11:08am		
3/29/04	11:19am		
3/29/04	11:28am		
3/29/04	11:39am		
3/29/04	11:50am		
3/29/04	12:45pm		
3/29/04	12:55pm		
3/29/04	1:06pm		
3/29/04	1:17pm		
3/29/04	1:28pm		
3/29/04	1:38pm		
3/30/04	7:30am		
3/30/04	9:23am		
3/30/04	10:12am		
3/30/04			
3/30/04	10:43am		
3/30/04	11:01am		
3/30/04	11:14am		
3/30/04	11:26am		
3/30/04	1:07pm		

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The summary is as follows:

Combination Wave Test signal

Surge test for I/O channels. Three pulses applied to each channel under test.

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Ring Wave Test signal

NON-PROPRIETARY

HF Controls

DOOSAN HF CONTROLS CORPORATION

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HFC-6000 Control System

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Isolation Testing Summary Report

TS901-000-28

Rev B

Effective Date	09/15/2007
Author/Title	Allen Hsu/William Gill
Reviewer/Title	John A. Stevens
Approval/Title	Terrence A. Gerardis

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Revision History

Date	Revision	Author	Changes
9/23/04	0	B. Han	Initial Draft
10/15/04	1	B. Han	Added new channel to channel test results
11/9/04	A	B. Han	Release
8/15/07	B	A.Hsu/W.Gill	Revised Scope of Topical Report

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1.0 PURPOSE

HFC is generically qualifying specific components of the HFC-6000 control system for nuclear safety-related applications in U.S. nuclear power plants. The approach taken for this qualification effort is based on the guidance provided in EPRI-TR-107330, Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants.

2.0 SCOPE

- The scope of this Isolation Testing Report Summary includes Class 1E isolation. Non-Class 1E isolation will be addressed on a plant specific basis.
- Definition of the test setup and Isolation qualification testing performed by HFC on the HFC-6000 Control System product line.
- Evaluation of test log notes recorded during the isolation testing to identify any performance degradation of test specimen.
- Evaluation of Operating and Prudency test results obtained during the Isolation Test to identify any performance degradation from the Baseline test results.

3.0 ABBREVIATIONS AND ACRONYMS

BOE	Burst of Events
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
HAS	Historical Archiving System
HFC	Doosan HF Controls
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
I/O	Input/Output
RFI	Radio Frequency Interference
SWC	Surge Withstand Capability
TSAP	Test System Application Program
vac	AC voltage
VCP	Vertical Coupling Plane
vdc	DC voltage

4.0 REFERENCES

TS901-000-22	HFC6000 Baseline Testing Summary Report (Rev. B)
TP0402	Operability Test Procedure
TP0403	Prudency Test Procedure
VV0414	Master Configuration List
TP0411	HFC-6000 Control Systems, ERD111- Control System Qualification Isolation Test Procedure

5.0 HFC-6000 ISOLATION QUALIFICATION DESCRIPTION

The term "channel" and "channel to channel" in this section of the report means a "port" on an I/O card and "port to port" interactions on the I/O card. I/O cards have multiple channels.

The HFC-6000 hardware may be installed both in an electrical equipment room and at various other locations near the equipment under control. When I/O chassis are physically located in a remote location with respect to the controller hardware, they will be connected to the controller by means of a dedicated fiber-optic communication link. This link will provide the mechanism for ensuring physical and electrical isolation between the remote I/O modules and the controller.

This document covers specific testing to demonstrate two categories of isolation:

- A fault on one channel of an I/O module will not effect the operation of other channels on the same module.
- A fault on one channel of an I/O module will not effect the operation of other modules in the system.

Test signals were applied to I/O channels to verify channel-to-channel isolation level requirements and acceptance criteria are met. During the tests, HAS data was recorded for automated tests (accuracy, response, BOE), and specific static points were monitored to detect any deviation caused by the applied test signals. For a number of the tests, 250 VDC and 600 vac was applied to each channel under test, and overall system response monitored for any disruption, interruption in automated waveforms, or unexpected transitions. Due to limitations of the high power fault test generator, certain tests were conducted with a current capacity power source with a 283 vac fault.

Acceptance criteria for Class 1E are:

- No channel-to-channel interference.
- No other module affected

If a channel successfully met the criteria for Class 1E isolation at the high voltage limit, no further test was executed for that channel type. If a channel failed to meet the Class 1E isolation acceptance criteria at the high voltage limit, the magnitude of the test signal was reduced to a lower level such that successful channel-to-channel and channel to module isolation was obtained once the channel passed this lower level test, then the magnitude of the test signal was progressively increased in order to determine the maximum level of isolation that the module could provide.

The minimum acceptable level of channel-to-channel and channel to module isolation for normal operation differs for each card type. The following list presents the minimum acceptable level of isolation for modules of the HFC-6000 Test Specimen on a channel-to-channel or group-to-group basis.

- ±30 v peak for AI channels on a group basis
- 100 v peak for 48 vdc discrete inputs on a group basis
- 40 vdc for pulse input channels on a group basis
- 600 v peak applied for 30 seconds for 120-vac discrete output channels on a group basis
- 600 v peak applied for 30 seconds for 125-vdc discrete output channels on a group basis
- 600 vac and 250 vdc applied for 30 seconds for AO channels
- Twice the nominal output voltage for discrete output channels and serial I/O channels on a group basis

This isolation test refers to demonstration of electrical isolation of Class 1E control equipment The tests were to run to determine the degree of isolation between one Class 1E module and other Class 1E modules in that safety channel; and the degree of isolation between I/O channels on the selected I/O cards. The initial signal levels used for this test were as follows:

- 600 vac or 283 vac applied for 30 seconds
- 250 vdc applied for 30 seconds

For those initial tests that did not meet the acceptance criteria the tests were repeated at lower voltage levels.

6.0 HFC-6000 ISOLATION TEST SETUP DESCRIPTION

The HFC-6000 Test Specimen consists of several modular chassis, a power supply rack, for simulated control loops, communication hardware, and mechanical support structures in the form of an open frame. The Test Specimen was assembled at HFC for pre-qualification testing and then disassembled for shipment to Wyle labs for stress tests.

At the completion of the stress test the Test Specimen and reassembled at HFC for the Isolation tests. The equipment was set up and the electrical, communication, and power cables were reconnected, and pre testing performed in accordance with Reference 3.5. The set-up consisted of 4

remotes: TSAP was Remote 1, HPAT was Remote 2, Single Loop Controller was Remote 3, and Remote 4 was used to record SOE data. The HPAT contains a memory editor program that allows the user monitor adjacent channels and cards during each test.

Throughout the Isolation testing, the test engineer recorded data in a variety of ways. The HAS logger was running to record the data on adjacent channels and automated tests running in the background. SOE data was recorded from Digital I/O cards and it records at a higher rate than the HAS logger. The test log book was used by the test engineer to record the dates and times of each test and all results seen during the test. This logbook will be referred to many times in the test results to describe observances and also to fill in gaps when HAS or SOE data was not available. The last record of data is found at the end of the test procedure TP0411. This record was initialed and dated by the test engineer. Throughout the test results below all these methods will be mentioned to provide a description of the performance of the test specimen during Isolation testing.

7.0 ISOLATION TESTING

Isolation testing was performed in accordance with HFC Isolation Test Procedure (Reference 3.5), and the results of that test are covered in this report. A representative I/O channel from each type of I/O module in the test specimen was exposed to the indicated level of test signals.

The following channels were tested and results included in this test report:

4 to 20 mA AI:

RTD input:

48-vdc discrete input:

Pulse input channels:

4-20 mA analog output:

Solid-state ac discrete output:

Solid-state dc discrete output:

Relay discrete output:

8.0 TEST EVALUATION

8.1 *Results*

8.1.1 4-20 mA AI

Test results of a channel on an AI16F card shows that HFC-AI16F board meets the Class 1E01 acceptance criteria

- for test signals at 250 vdc and 283 vac with no module other than the module under test being affected
- for test signals of 250 vdc 40 vac with no channel other than the channel being affected

8.1.2 RTD Input Channel

Test results of a channel on an AI8M card shows that the AI8M module meets the acceptance criteria

- for test signals at 250 vdc and 600 vac with no module other than the module under test being affected
- for test signals of 250 vdc and 283 vac with no channel other than the channel being affected

8.1.3 48 vdc Discrete Input Channel

Test results of a channel on an HFC-DC34 card (station 20) in test specimen passed both the 250 VDC and 600 VAC tests without channel-to-channel effects or module to module effects.

Test results of a channel on an HFC-DC33 card showed no adverse channel-to-channel effects or module-to-module effects during tests at 250 vdc and 283 vac.

Test results of a channel on an HFC-DI16I card showed no adverse channel-to-channel effects or module-to-module effects during either test at 250 vdc or 600 vac.

8.1.4 Pulse Input Channel

Test results of a channel on an HFC-AI4K card showed no adverse channel-to-channel or module to module effects during tests at 250 vdc or 600 vac. .

8.1.5 Analog Output Channel

Test results of a channel on an HFC-AO8F card showed no adverse channel-to-channel or module to module effects during tests at 250 vdc or 600 vac.

8.1.6 AC Discrete Output Channel

Test results of a channel on an HFC-DC33 card showed no adverse channel-to-channel effects or module-to-module effects during either test at 250 vdc and 283 vac.

8.1.7 DC Discrete Output Channel

Test results of a channel on an HFC-DC34 card showed no adverse channel-to-channel effects or module-to-module effects during either test at 250 vdc and 283 vac.

8.1.8 Relay Discrete Output Channel

Test results of a channel on an HFC-DO8J card showed no adverse channel-to-channel effects or module-to-module effects during tests at 250 vdc and 600 vac.

8.2 *Anomalies*

When applied 600 vac voltages to the AI4K card under test (station 58) DI16I card (station 36) in another rack also reported alarm at that time.

Resolution: The DI16I card was located a relatively long distance from the AI4K in a different rack. The alarm is considered random and independent of the DI16I test.

9.0 SUMMARY

The analog output channel on HFC-AO8F, discrete input channel on HFC-DC34, discrete output on HFC-DO8J, discrete input channel on DI16I and pulse input channel on HFC-AI4K passed all Class 1E requirements with 600 vac and 250 vdc applied. While several cards experienced destructive failure of the test channel, adjacent channels and modules showed no adverse effects. These tests met the acceptance criteria.

Discrete input and output channel on HFC-DC33, discrete output channel on HFC-DC34 DC Discrete Output passed Class 1E requirements and no channel to channel interference requirements with 283 vac and 250 vdc applied.

The card HFC-AI16I passed no module to module interference criteria with 283 vac and 250 vdc applied. It passed no channel to channel interference with up to 40 vac applied, which result in damage to the test channel but no other channels were affected.

The card HFC-AI8M passed no module to module interference criteria with 600 vac and 250 vdc applied. It passed no channel to channel interference with up to 280 vac applied, which result in damage to the test channel but no other channels were affected.

Certain cards were only tested to 283 vac due to limitations of the HFC test equipment. These cards are analog input channel on AI16F, discrete input and discrete output channels on DC33, and discrete output channel on DC34.

Doosan HFC has concluded that all modules that are part of the qualification testing have completed successful isolation testing.

HFC-6000 Control System

ERD111 – Control System Qualification Project

Isolation Testing Summary Report

TS901-000-28
Ref B

Appendix A

Test Results Evaluation

Non-Proprietary

A.1 GENERAL

This attachment provides a detailed evaluation of results for the isolation test cases.

A.2 1E01 AND ISO1 TESTING

For the current input (4 to 20 mA) AI16F module, 600 vac and 250 vdc was applied to the test channel for 30 seconds.

A.2.1 Channel under Test: 1,AI,894 (HFC-AI16F)

Channel 1, AI,894 experienced test voltages on 4/22/04 at the HF Controls facility between 2-3pm. At 2:26pm, a 250 vdc signal was applied for 30 seconds to the channel. Other channels were monitored both manually and recorded through HAS logger.

At the time of testing, HAS was logging data on an adjacent channel 1,AI,889, this channel is monitored through 1,BL,510, 1,BL,514, and 1,BL,516 signals. The data for these channels can be seen in Figure A.2-1 below, and shows no signs of disturbance from the channel under test.

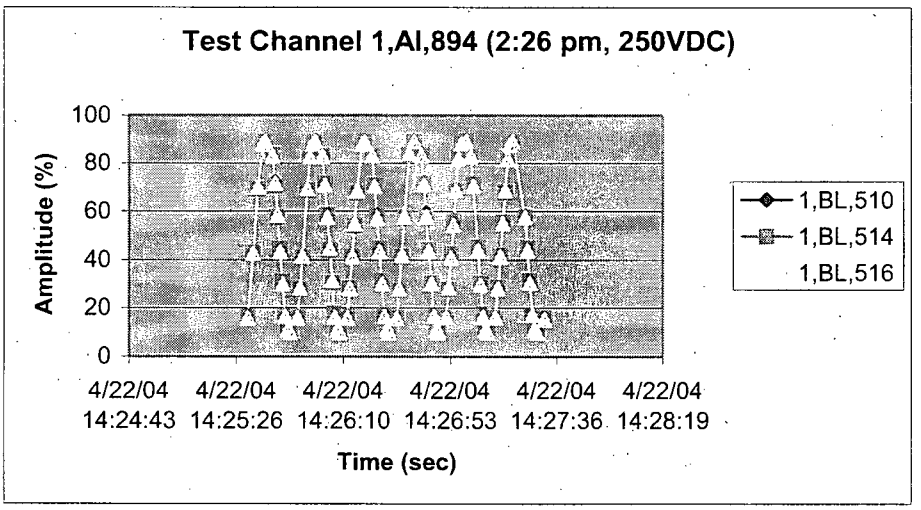

Figure A.2- 1, **1,AI,894 No Disturbance at 250 vdc Test.**

At 2:39pm, a 150 vac test signal was applied to channel 1,AI,894. The HIPOT fault test generator unit tripped at this point due to limitation of the test device. Later on 6/4/04 at 3:09pm, a 283 vac was applied to the card and the following observations recorded;

1) All channel outputs changed to FFFF indicating the I/O card lost communications.

Since the adjacent channels on the card under test were affected by the 283 vac signal, HFC concluded that the HFC-AI16 card needs to go through additional ISO1 testing to evaluate channel to channel interactions.

By looking at the Accuracy data taken from other cards during the same 283 vac time period and witnessing no disturbances on these other cards, HFC verified that no other cards other than the card under test were affected. In summary, other channels on the module being tested were disrupted, but no other module was disrupted. Further channel to channel testing would be required for the AI card.

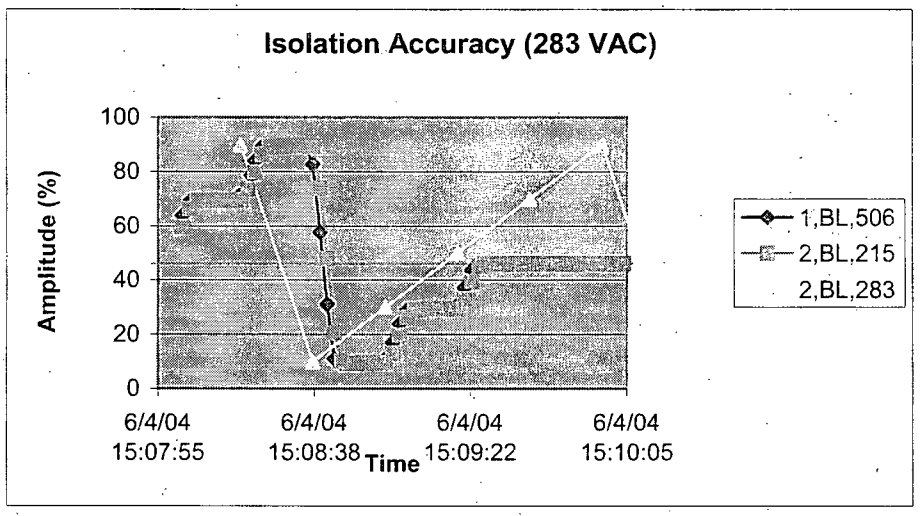

***Figure A.2- 2,* 1EO1 Accuracy Data.**

1,BL,506 is associated with 1,AI,881 and used for the AI accuracy test. The data from Figure A.2-2 shows that channel AI,881 was affected when the 283 vac fault was applied. No malfunctions of other modules in the system were observed. Alarm files on 4/22/04 are listed in Table A.2-1 and show that at 14:18, several channels from the AI16F card had alarms for a few minutes. Then at 14:32, those channels had alarm again. No other modules in the system showed alarms. The time ranges match the testing periods. So, for the application of the 283 vac fault, HFC can conclude that in both conditions, channels on the same card were affected, but no adjacent modules were affected.

***Table A.2- 1.* Alarms during Isolation Test on AI16F AI.**

TIME	NAME	DESCRIPTION	VALUE
14:18:49	1,FL,69	LINK 0 STATION 52 FAIL	1
14:18:52	1,FL,69	LINK 0 STATION 52 FAIL	1
14:18:59	1,FL,69	LINK 0 STATION 52 FAIL	1
14:19:02	1,FL,69	LINK 0 STATION 52 FAIL	1
14:19:05	1,FL,69	LINK 0 STATION 52 FAIL	1
14:19:08	1,FL,69	LINK 0 STATION 52 FAIL	1
14:19:10	1,FL,69	LINK 0 STATION 52 FAIL	1
14:19:53	1,FL,69	LINK 0 STATION 52 FAIL	1
14:19:57	1,FL,69	LINK 0 STATION 52 FAIL	1
14:20:03	1,FL,69	LINK 0 STATION 52 FAIL	1
14:20:05	1,FL,69	LINK 0 STATION 52 FAIL	1
14:20:07	1,FL,69	LINK 0 STATION 52 FAIL	1

TIME	NAME	DESCRIPTION	VALUE
14:20:10	1,FL,69	LINK 0 STATION 52 FAIL	1
14:20:12	1,FL,69	LINK 0 STATION 52 FAIL	1
14:31:56	1,FL,69	LINK 0 STATION 52 FAIL	1
14:33:22	1,FL,69	LINK 0 STATION 52 FAIL	1
14:33:32	1,FL,69	LINK 0 STATION 52 FAIL	1

On 10/12/04, 30 vac test signal was applied to the channel for 30 seconds. The channel was working normally, and there were no affects on other channels. Subsequently, 40 vac resulted damage to 1,AI,894's resistor R73, but there was no affect on other channels. The test at 40 vdc met the acceptance criteria of no channel to channel interaction as Figure A.2-3 shows the operation of two adjacent channels and there were no disruption to these channels during the test. The test at 40 vdc met the acceptance criteria of no channel to channel interaction.

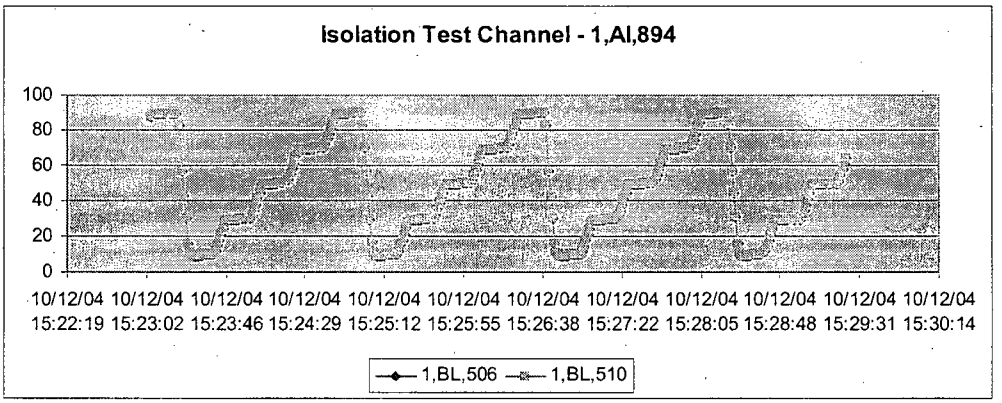

Figure A.2- 3, Adjacent Channels to 1,AI,894 at Channel-to-Channel Isolation Test

The data shows that the Class 1E01 testing meets the acceptance criteria that no other modules were affected at 250 vdc and 283 vac; and no other channels on a single module were affected at 250 vdc and 40 vac.

A.3 1E02 AND ISO2 TESTING

A.3.1 Channel under Test: 1,AI,965 (HFC-AI8M)

On 4/22/04 at 3:22 pm, 250 vdc was applied to 1,AI,965 for a thirty second period. Adjacent channels were monitored through memory editor on the HPAT. Adjacent AI8M channels and other modules were monitored on the diagnostic window. Neither failures nor disturbances were detected during testing.

On 4/22/04 at 3:31 pm, 600 vac was applied to 1,AI,965 for a thirty second period. All channels were seen changing in memory editor, verifying the 600 vac affected adjacent channels on the same card. No other modules were affected. HFC concluded that additional testing for the vac faults was required.

Figure A.3-1 shows the adjacent RTD channel value changes during those periods. The RTD values did not change by more than 0.5 % from 4/22/21 until 3:25 on 4/22/04. This shows that 250 vdc had no affect on these channels. The figure shows that 600 vac at 3:31 pm had affects on all these channels.

Alarm files as in Table A.3-1 shows that channels on the same card reported alarms at 15:23 and then at 15:30.

Subsequent to the 600 vac test, progressively increasing fault signals up to 240 vac test signal were applied to the test channel for 30 second on 10/12/04. The channel continued to perform normally and there were no affect to other channels. The 280 vac resulted in fuse F5 on the channel under test blowing out, but there was no affect on other channel effects. This fuse failure is acceptable.

The data shows that Class 1E02 testing meets the acceptance criteria that no other module was affected at 250 vdc and 600 vac, and no other channel to channel affects occurred at 250 vdc and 280 vac. All acceptance criteria were met at these fault levels.

The HFC-AI8M board meets the Class 1E02 acceptance criteria of no other module affected and no channel-to-channel interference.

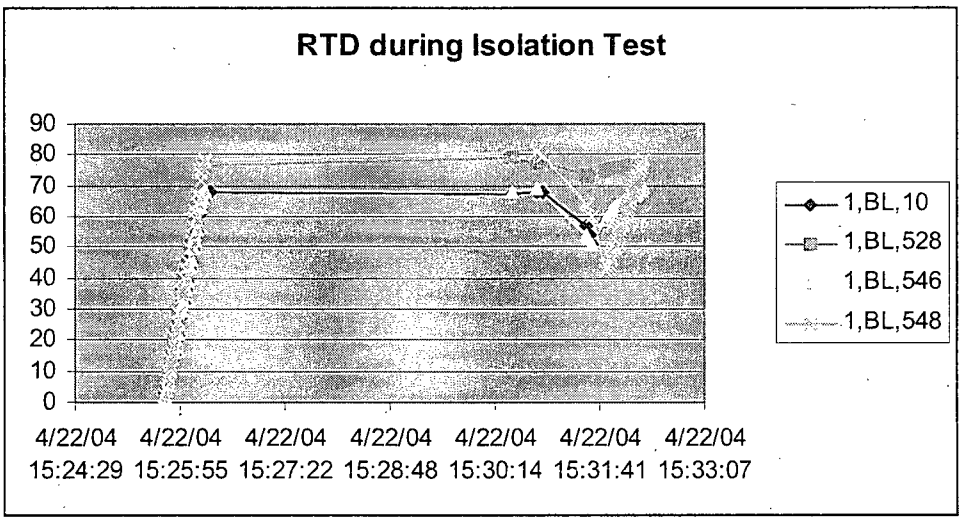

Figure A.3- 1, **RTD Channels during Isolation Test.**

Table A.3- 1. **Alarms during Isolation Test on RTD card.**

TIME	NAME	DESCRIPTION	VALUE
15:23:11	1,FL,73	LINK 0 STATION 56 FAIL	1
15:23:12	1,BL,10	AIC AI,962 AI8M 1-4-9 FL,73	68.12
15:23:12	1,BL,528	AIC AI,961 AI8M 1-4-9 FL,73	77.18
15:23:12	1,BL,546	AIC AI,968 AI8M 1-4-9 FL,73	68.92
15:23:12	1,BL,549	AIC AI,963 AI8M 1-4-9 FL,73	78.65
15:30:18	1,FL,73	LINK 0 STATION 56 FAIL	1
15:30:19	1,BL,10	AIC AI,962 AI8M 1-4-9 FL,73	68.12
15:30:19	1,BL,528	AIC AI,961 AI8M 1-4-9 FL,73	77.2
15:30:19	1,BL,546	AIC AI,968 AI8M 1-4-9 FL,73	68.98
15:30:19	1,BL,549	AIC AI,963 AI8M 1-4-9 FL,73	78.73
15:30:43	1,FL,73	LINK 0 STATION 56 FAIL	1
15:30:43	1,BL,10	AIC AI,962 AI8M 1-4-9 FL,73	67.55
15:30:43	1,BL,528	AIC AI,961 AI8M 1-4-9 FL,73	78.2
15:30:43	1,BL,546	AIC AI,968 AI8M 1-4-9 FL,73	68.04
15:30:43	1,BL,549	AIC AI,963 AI8M 1-4-9 FL,73	78.55
15:30:49	1,FL,73	LINK 0 STATION 56 FAIL	1
15:30:52	1,FL,73	LINK 0 STATION 56 FAIL	1
15:31:33	1,BL,528	AIC AI,961 AI8M 1-4-9 FL,73	73.04
15:31:33	1,BL,546	AIC AI,968 AI8M 1-4-9 FL,73	52.51
15:31:33	1,BL,549	AIC AI,963 AI8M 1-4-9 FL,73	63.69

A.4 1E06 AND IS06 TESTING

A.4.1 Channel under Test: 3,DI,32 (HFC-DC34)

On 4/22/04 at 3:55 pm, 250 vdc was applied to 3,DI,32 for thirty-four seconds. The logbook indicates that the input resistor was burned on the channel under test. No affects on adjacent channels were noticed by observing the Memory Editor screen. No HAS data logging was configured for this card. On 4/22/04 at 4:24 pm, 600 vac was applied to 3,DI,32 for a thirty second period. Again, no affects were noted. No alarms were observed during this test period.

This card passed both the 250 vdc and 600 vac tests without channel-to-channel affects or module to module effects. This card passed both 1E06 and ISO6 testing.

A.4.2 Channel under Test: 1,DI,325 (HFC-DC34)

On 4/22/04 at 4:30 pm, 250 vdc was applied to 1,DI,325 for thirty seconds. The logbook indicates that no affects were seen. HAS data was recorded during this period and shows no affects. The HAS data monitored channel 1,DI,329 and is shown in Figure A.4-1 below. There are no disturbances during the thirty-second period except the last point which occurred after testing had completed.

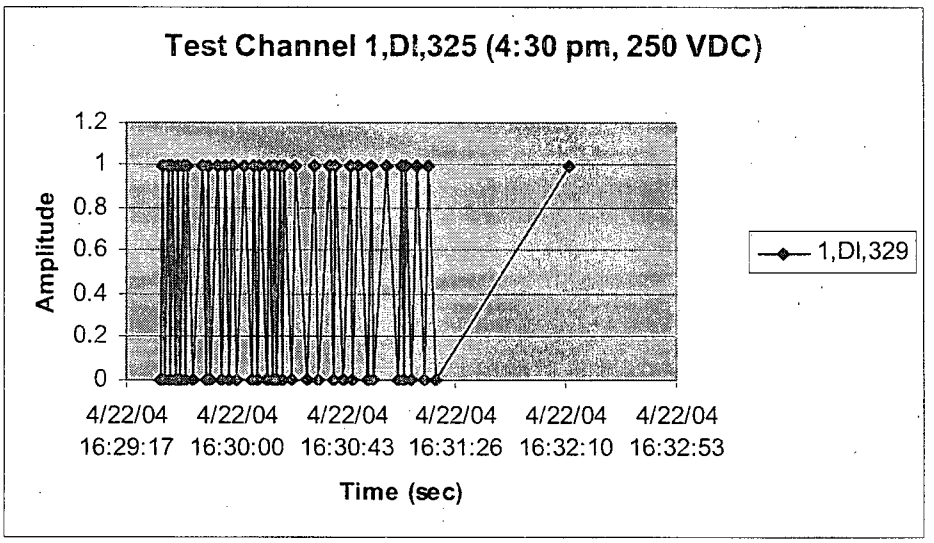

Figure A.4- 1, **No Disturbances During 250 vdc Test.**

On 4/22/04 at 4:36 pm, 600 vac was applied to 1,DI,325 for a thirty second period. Again, no affects were noticed. The HAS data taken during this test is in Figure A.4-2.

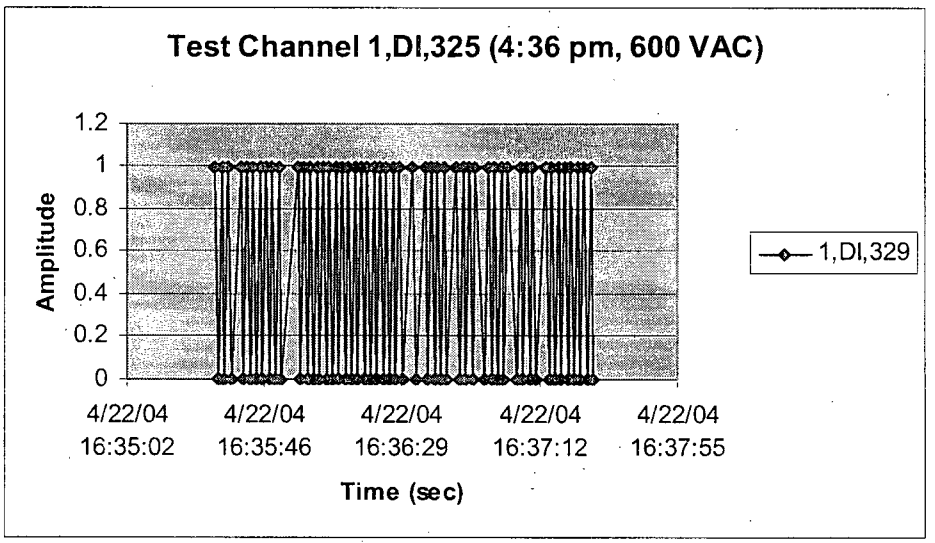

Figure A.4- 2, **No Disturbances during 600 vac.**

Table A.4- 1. **Alarms during Isolation Test for 1,DI,325.**

TIME	NAME	DESCRIPTION	VALUE
16:31:16	1,FL,37	LINK 0 STATION 20 FAIL	1

During the test period, only this card (station 20) went into alarm because the board was removed momentarily to observe input channel components and the board was then reinstalled. This alarm is a normal expected occurrence.

The HFC-DC34 passed both the 250 vdc and 600 vac tests without channel-to-channel or module to module effects. This card passed both 1E06 and ISO6 testing.

A.4.3 Channel under Test: 1,DI,265 (HFC-DC33)

On 4/22/04 at 4:42 pm, 250 vdc was applied to 1,DI,265 for thirty seconds. The logbook recorded no adverse affects during the test. HAS data was recorded during this period and shows no affects. The HAS data monitored channel 1,DI,269 and is shown in Figure A.4-3 below. There are no thirty-second periods of disturbances seen in the data.

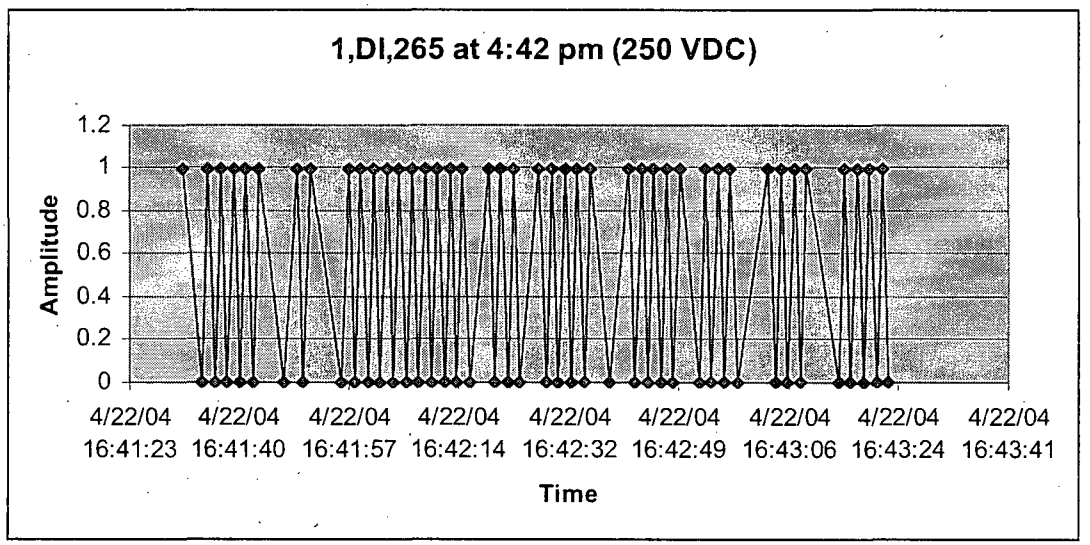

Figure A.4- 3, **No Disturbances at 250 vdc.**

On 4/22/04 at 4:47 pm, 600 vac was intended to be applied to 1,DI,265 for a thirty second period. However using the HIPOT fault generator tester, only 28 vac was applied before the HIPOT tripped. The test was repeated later at 5:27 pm on 5/26/04 using the Variac transformer to apply 283 vac for thirty seconds. No affects on adjacent channels were noticed. No alarms were noted during the test period. The HAS data shown in Figure A.4-4 was taken during the 4:47 pm time period.

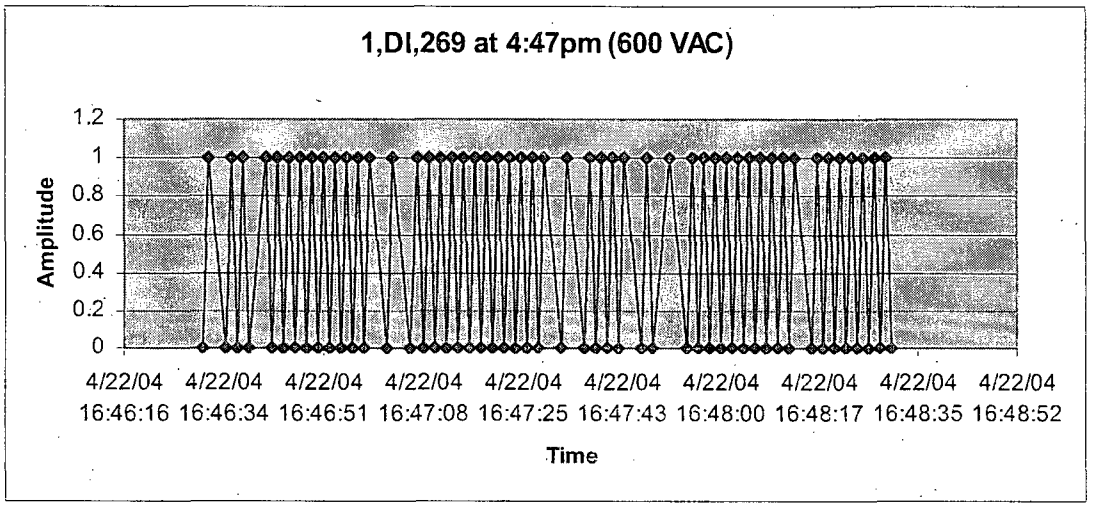

Figure A.4- 4, **No Disturbances at 600 vac.**

The HFC-DC33 card showed no adverse affects during either test so it passed 1E06 and ISO6 for 250 vdc and 283 vac.

A.4.4 Channel under Test: 1,DI,311 (HFC-DI16I)

On 4/22/04 at 5:19 pm, 250 vdc was applied to 1,DI,311 for thirty seconds. The logbook recorded no adverse affects. No HAS data was configured to be logged for monitoring this channel.

On 4/22/04 at 5:24 pm, 600 vdc was applied to 1,DI,311 for thirty seconds. The logbook recorded no adverse affects.

The alarm file shows only the DI16I card went into alarm because the board was removed momentarily for inspection. This alarm is a normal expected occurrence No other modules were affected.

Table A.4- 2. **Alarm Records during Testing of 1,DI,311.**

TIME	NAME	DESCRIPTION	VALUE
17:18:03	1,FL,36	LINK 0 STATION 19 FAIL	1
17:21:14	1,FL,36	LINK 0 STATION 19 FAIL	1

The DI16I card passed both the 250 vdc and 600 vac tests with no channel to channel or module to module effects. The HFC-DI16I card met the 1E06 and ISO6 acceptance criteria.

A.5 1E07 AND ISO7 TESTING

A.5.1 Channel under Test: 1,AI,1021 (HFC-AI4K)

On 4/23/04 at 9:10 am, 250 vdc was applied to 1,AI,1021 for thirty seconds. The logbook recorded no adverse affects. HAS data was not recorded during this period.

On 4/23/04 at 9:18 am, 600 vac was applied to 1,AI,1021 for thirty seconds. The logbook recorded no adverse affects. HAS data was not recorded during this period.

Examination of alarm log files showed no system alarm during the test period.

The HFC-AI4K showed no adverse channel-to-channel affects and no other modules were affected during test at 250 vdc and 600 vac. The AI4K module passed 1E07 and ISO7 acceptance criteria.

A.6 1E08 AND ISO8 TESTING

A.6.1 Channel under Test: 1,AO,822 (HFC-AO8F)

On 10/13/04 at 9:33 am, 600 vac test signal was applied to 1,AO,822 for thirty seconds. Fuse F8 (1,AO,822 fuse) failed. There were no affects on other channels or other modules. The fused was replaced and the channel starts working again. The test passed the acceptance criteria for the 600 vac test.

At 9:51 am, 250 vdc was applied to the channel for thirty seconds. The fuse F8 failed again. There was no affect on other channels and no affects on other modules.

The AO8F card met the channel to channel and module to module acceptance criteria for the tests at 250 vdc and 600 vac.

The HFC-AO8F passed both 1E08 and ISO8 acceptance criteria.

A.7 1E09 AND ISO9 TESTING

A.7.1 Channel under Test: 1,DO,262 (HFC-DC33)

On 4/26/04 at 10:37 am, 250 vdc was applied to 1,DO,262 for thirty seconds. The logbook recorded no adverse affects. No HAS data was configured to be logged for monitoring this point.

On 4/26/04 at 10:45 am, using the HIPOT tester, only 79 vac could be applied before tripping the tester. Therefore, on 5/27/04 at 9:40 am, the Variac Transformer was used to apply 283 vac for thirty seconds. No affects on adjacent channels were noticed. No impact on other modules was noticed. The DO channel under test was operable, however some burnt traces were noticed on the card under test.

No alarms were reported during the testing period.

The DC33 card met the channel to channel and module to module acceptance criteria for tests at 250 vdc and 283 vac.

The HFC-DC33 met the 1E09 and ISO9 acceptance criteria.

A.8 1E010 AND ISO10 TESTING

A.8.1 Channel under Test: 1,DO,82 (HFC-DC34)

On 4/23/04 at 10:55 am, 250 vdc was applied to 1,DO,82 for thirty seconds. The logbook recorded no adverse affects. HAS data recorded at that time supports this statement by showing the adjacent channel 1,DO,81 monitored through 1,DI,89 in Figure A.8-1 below.

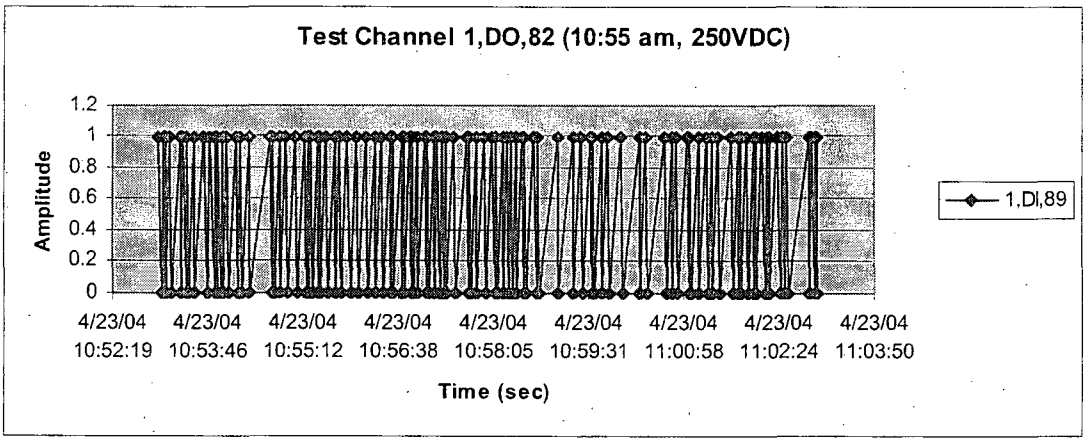

Figure A.8- 1, **No Disruption at 250 vdc.**

On 4/23/04, only 192 vac was reached before tripping the HIPOT tester. Therefore, on 6/1/04 at 3:57 pm, 283 vac was applied using the Variac Transformer. During the test the DO point remained on until the 283 vac source tripped after several seconds. The adjacent DO channel was not disturbed. It is noted that diode D13 was shorted after testing.

No alarms were reported during the testing period.

The adjacent channels and no other modules were affected.

The HFC-DC34 met the channel to channel and module to module 1E010 and ISO10 acceptance criteria for 250 vdc and 283 vac.

A.9 1E012 AND ISO12 TESTING

A.9.1 Channel under Test: 3,DO,56 (HFC-DO8J)

On 4/23/04 at 10:29 am, 250 vdc was applied to 3,DO,56 for thirty seconds. The logbook recorded no adverse effects. No HAS data was configured to be logged to monitor this point.

On 4/23/04, 600 vac was applied to the test channel. No adverse effects were noticed.

No alarms were reported during the testing period.

The HFC-DO8J met the channel to channel and module to module 1E012 and ISO12 acceptance criteria at 250 vdc and 600 vdc.

HF CONTROLS CORPORATION

HFC-6000 Control System

ERD111 – Control System Qualification Project

Post Qualification Testing Summary Report

TS901-000-29

Rev B

NON-PROPRIETARY

Effective Date	10/16/07
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9/23/04	0	X. Li	Initial Draft
10/12/04	1	X. Li	Result summary, C-Link and ICL SOE data added
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11/10/04	A	X. Li	Rev A Release
10/16/07	B	J Taylor/ R Musick	Revised Scope of Topical Report

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1.0 PURPOSE

HFC is generically qualifying its HFC-6000 control system for nuclear safety-related applications in U.S. nuclear power plants. The approach taken for this qualification effort is based on the guidance provided in EPRI-TR-107330, Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants.

This document specifically addresses the Post Qualification Test segment of the qualification testing program. This test was performed after the equipment was returned from Wyle the first time.

2.0 SCOPE

- Evaluation of Operability and Prudency tests performed during the post qualification testing to identify any performance degradation from the Operability and Prudency results established in the Baseline Report (TS901-000-22).
- Evaluation of all anomalies detected during the course of the Post Qualification test.

3.0 REFERENCES AND ACRONYMS

3.1 References

TS901-000-22	HFC6000 Baseline Testing Summary Report
TP0402	Operability Test Procedure
TP0403	Prudency Test Procedure
VV0414	Master Configuration List
Manual	Hand-written HFC Test Log

3.2 Acronyms

BOE	Burst of Events
DDB	Dynamic Database
HAS	Historical Archiving System
HFC	HF Controls
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
PLC	Programmable Logic Controller
RTD	Resistance Temperature Detector
SOE	Sequence of Events
TSAP	Test System Application Program

4.0 POST QUALIFICATION TEST DESCRIPTION

The Post Qualification Test is a repeat of the Operability and Prudency testing that was performed during the Pre-Qualification Test. This test was performed following the return of the equipment from Wyle after the first seismic test. Refer to the Baseline Report (TS901-000-22) for the test description.

5.0 POST QUALIFICATION TEST SETUP

The Post Qualification Test is a repeat of the Operability and Prudency testing that was performed during the Pre-Qualification Test. Refer to the Baseline Report (TS901-000-22) for the test setup. It should be noted that the HAS logger configuration was modified before the start of the post qualification test. More specifically, the deadband for the logging was changed from 0.5 to 0.0 so that any change in the value of the configured points would trigger the logging of the points. In addition, DDB request tables for TSAP and HPAT were also modified to eliminate unnecessary points from the DDB broadcast. This latter change was made to ensure that the entire DDB broadcast would be completed once every second. The detailed changes are listed in Table 1.

Table 1. Modification of DDB Request Tables for TSAP and HPAT During Post Qualification Test.

Point ID	Number of Points Broadcasted			
	TSAP (Remote 1)		HPAT (Remote 2)	
	Old	New	Old	New
DI	1500	800	7000	300
DO	1500	800	7000	300
FL	20000	3000	20000	3000
CO	8000	200	100	100
MS	1000	500	500	300
DF	1000	0		
BL	1370	600	1370	400
TI	0	150		

6.0 POST QUALIFICATION TEST SEQUENCE

6.1 System Setup and Checkout Tests

6.1.1 General

An abbreviated System Setup and Checkout Test was performed at HFC after the test specimen was returned from the Wyle Laboratory test facility after the first seismic test, prior to Post qualification testing performed at HFC. This testing was to verify that the equipment was functioning, that all interconnecting wiring had been installed correctly, and that communication had been established before starting the Post Qualification Test.

6.1.2 Results

This test was run and all equipment was configured as required.

6.1.3 Anomalies

Any anomalies that were found were resolved prior to completion of the procedure.

6.1.4 Summary

All assemblies met the acceptance criteria for the set-up and check-out test upon completion of the procedure.

6.2 Operability Test

6.2.1 General

The HFC-6000 control system (Test Specimen) was configured for generic qualification as it was for the baseline testing, and Post Qualification Operability Testing was performed to evaluate system performance against the baseline testing (Appendix PQ.A).

6.2.2 Results

- All applicable operability tests, with the exception of the Power Quality Tolerance Test, were performed at the HFC site after completion of the first round of qualification tests at Wyle Laboratories. The results of these tests are documented in Appendix PQ.A.

- Manual AO accuracy test results are within the 0.1% acceptance range and are consistent with pre qualification test results.

- Manual pulse card accumulate mode test results demonstrate a significant improvement over those from pre-qualification test. More specifically, the accuracy was 0.00%-0.227% at prescaler 1 and was 0.001%-0.065% for prescaler 100, compared to pre-qualification results of 0.156%-1.139% at prescaler 1 and 0.127%-1.093% at prescaler 100.

- Manual pulse card rate mode test measurements from 8-bit mode are in line with pre-qualification test results. However, measurements from 12-bit mode show significant improvement over pre-qualification test at low frequency range: 0.005% vs. 1.79% at 50 Hz, and 0.005% vs. 0.294% at 600 Hz.

- Automated AO results were well within the acceptance range and are consistent with pre-qualification test.

- Manual and automated analog response time results from the post qualification test deviate less than 10% from the pre-qualifications results.

- Discrete input operability test demonstrated that DI channels met all of the acceptable criteria for the set voltage level, dropout voltage, and the maximum input voltage.

- Results for other operability tests are presented in Section 6.4 or related sections of Baseline Report (TS901-000-22).

6.2.3 Anomalies

- Manual AI Accuracy Test: The post qualification test was conducted with a replacement card, serial number 31030007. The test result did not meet the 0.1% acceptance criteria, which is in line with pre-qualification results. However, AI deviations in post qualification test are generally higher than those obtained from baseline measurements: 0.202%-0.588% vs. 0.148-0.322%.

  Resolution: The card was found out to be out of calibration. After being recalibrated, the same channel was retested, and the results met the 0.1% acceptance criteria. Larger deviation in the post qualification test may be the results of the adverse effect of the stress tests on the AI cards.

- RTD Manual Test: Channel 8 was not tested because it was having a bad contact. Neither channel 1 nor channel 2 met the 0.1% acceptance criteria over their operating range. By contrast, in the pre-qualification test, channel 1 met the 0.1% criteria, whereas channel 2 did not meet the criteria over the entire temperature range.

  Assessment: The simulation resistors changed value during the environmental test and the terminals were damaged by the seismic test. In addition, connecting and disconnecting wires from the terminals can change contact resistance by more than 1 ohm, which will produce more than 0.1% change in indicated temperature.

- Automated AI Accuracy Test: A different AI card was used during the post qualification test. Although the deadband of HAS logger was changed from 0.5 to 0.0 in the post qualification test, the AI accuracy results are still outside the acceptance range of 0.1%. Nonetheless, post qualification results do improve over the pre-qualification results although two different AI cards were used in these tests. Post qualification results also show apparent trend of lower deviations with higher input signal levels.

  Assessment: The out of range accuracy is due to the following factors:

  - It is likely that the card was not calibrated to 0.1% accuracy over the entire operating range prior to this test,
  - The deviation of the AI channel being monitored includes the inaccuracy factors of an AO channel in the HPAT and the AI channel in the Test Specimen.
  - The 100 cycle moving average function in the AI card in conjunction with the input filter on the AI card prevent the AI image from reaching the actual input value for approximately 10 seconds. During this process, the image value is constantly changing

- The AI accuracy test waveform consisted of a step signal with the analog value held at a set value for 20 seconds at each step. The HAS logged data once every 2 seconds, and this operation was in no way synchronized with the test waveform. Consequently, the archive does not preserve any way of precisely correlating a data point from one execution of the test with a data point from another execution of the same test.

- Automated RTD Test: In post qualification test, 1,BL,528 and 1,BL,548 show higher temperature readings, but 1,BL,10 shows lower temperature reading than the corresponding pre-qualification results.

  Assessment: The simulation resistors changed value during the environmental test and the terminals were damaged by the seismic test. In addition, connecting and disconnecting wires from the terminals can change contact resistance by more than 1 ohm. Both factors could have contributed to the deviations.

- Automated Digital Response Test: 1) A wiring inconsistency was identified: in pre-qualification test, the HPAT square waveform was wired to 4,DI,9; it was rewired to 4,DI,16 in post qualification test. 2) The response time from direct measurement did not meet the 100 ms acceptance criterion. 3) Post qualification measurements also displayed a significantly larger standard deviation

  Resolution: 1) The wiring error did not affect the proper execution of the test. 2) Although direct response time measurement was larger than 100 ms, it deviated less than 10% from the pre-qualification result. 3) A larger standard deviation may be a sign of system degradation from the stress tests.

6.2.4 Summary

Due to data missing or other reasons in the pre-qualification test, a number of post qualification operability results were used to supplement the Baseline Report (TS901-000-22). For those operability tests that were available in the pre-qualification test, the corresponding results from the post qualification test clearly showed an adverse effect of the stress tests on the system operability performance.

6.1 Prudency Test

6.3.1 General

The HFC-6000 control system (Test Specimen) was configured for generic qualification as it was for the baseline testing, and Post Qualification Prudency Testing was performed for evaluating system performance against the baseline testing (Appendix PQ.B).

6.3.2 Results

- All applicable prudency tests, with the exception of the Serial Link Noise Test and Fault Simulation Test, were performed at the HFC site after equipment shipped back from Wyle labs. The results of these tests are documented in Appendix PQ.B.

- The averaged deviations at 10% for all three AIs vs. BOE source signal meet the 0.32% acceptance criteria, which is consistent with pre-qualification results.

- Results for other Prudency tests are either included in Section 6.5 or related sections of Baseline Report (TS901-000-22).

6.3.3 Anomalies

- Digital BOE Test: 1) A wiring inconsistence was identified: the digital BOE points logged during the pre-qualification and Wyle tests were 4,DI,24 to 4,DI,30; however, they were changed to 4,DI,28 to 4,DI,36 in the post qualification test. 2) A total of 6 contact bounces from 4 channels occurred during the test period, a moderate increment from four occurrences during the pre-qualification test.

  Resolution: 1) The wiring error did not affect the system performance evaluation since one point is sufficient to provide a proper evaluation of system digital BOE performance; 2) The fact that no contact bounces were detected during the seismic retest, which was conducted after the post qualification test, demonstrated that the higher occurrences of contact bounces can be treated as random events. Refer to test report TS901-000-35 for the digital BOE results in the seismic retest.

- Digital BOE Test: 6 abnormal transitions were recorded: one occurred at 8:25:29.46 AM from channel 4,DI,28, the other five occurred 64 ms later for channels 4,DI,28, 4,DI,30, 4,DI,31, 4,DI,33, 4,DI,34.

  Assessment: Observations from SOE data: the abnormal transition at 8:25:29.46 AM, i.e., 1.8545 s transition, was immediately followed by another abnormal transition and a contact bounce and the other five abnormal transitions were short transitions of ~60 ms and they were all immediately followed by a contact bounce except for 4,DI,30.

- Analog BOE Test: In the assessment of BOE source signal versus the TSAP AI signals, it was found that for the 90% level signal, 1,BL,510 and 1,BL,514 were within 0.32% BOE source signal, whereas 1,BL,516 was not. By contrast, in pre qualification test all three AI signals deviated more than 0.32% from the BOE source signal at 90% level.

  Resolution: HAS deadband was set to 0 versus 0.5 used in pre qualification test. In addition, a different AI card that involved 1,BL,510 and 1,BL,514 was used in the post qualification test. The improved accuracy could be the result of combination of these two factors.

- Serial Link Noise Test and Fault Simulation Link Test were not performed during the post qualification test.

  Assessment: Serial Link Noise Test was performed during the in-house test for the seismic retesting program. Refer to Seismic Retest In-house Retesting Summary Report (TS901-000-34) for more detail. The Fault Simulation Link Test was covered by the Failover Operability Test.

6.3.4 Summary

BOE results were generally in line with the baseline test, with the exception of the occurrence of 5 abnormal transitions in the digital BOE test.

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APPENDIX PQ.A

OPERABILITY TESTS

PQ.A.1 General

The purpose of this attachment is to document the results of the Post Qualification Operability Tests which were performed following the return of the equipment from the first round of tests at Wyle. The Post Qualification Test is a repeat of the Operability and Prudency testing that was performed during the Pre-qualification Testing.

For ease of comparison to the Post Qualification test results, this appendix is organized to follow the same section numbering as in the Baseline Report Appendix A (Operability Test) and Appendix B (Prudency Test), adding PQ (e.g. Appendix PQ.A) to distinguish the Post Qualification. If a section is not applicable to the Post Qualification testing the section numbering will be maintained with that section being indicated as "Not Applicable".

There are areas where the Post Qualification test results and analysis have to be used to supplement missing or insufficient Pre-qualification testing data. Where the Post Qualification data and analysis is used in the Baseline section of the report it will not be repeated in the Post Qualification test results and that section will be marked "Refer to the applicable Section of the Baseline report".

PQ.A.2 Manual 4-20 mA AI Channel Accuracy (Section 4.1.1)

The original AI16F card used for AI accuracy test during qualification was damaged by the Isolation Test. The post qualification test was conducted with a replacement card, serial number 31030007. As a replacement, this card was placed in a spare slot of TSAP and thus went through all the Wyle qualification test process. The manual test results are shown in Table PQ.A.2-1.

The test results are out of the 0.1% acceptance criteria. The table shows that the deviations became higher at higher signal input levels, which is consistent with the baseline results. In order to determine why the card exceeded the acceptance limits, the card was subjected to a calibration test and found to be out of calibration. After being recalibrated, the same channel was retested, and the results are shown in Table PQ.A.2-2. It is clear that the results met the 0.1% acceptance criteria, and the magnitude of deviation is not a function of the signal input levels.

Results in Table PQ.A.2-1 also indicate that the AI accuracy during the post qualification test were less accurate than the baseline results established from pre-qualification test. However, it should be noted that the pre-qualification and post qualification AI tests were performed on different cards.

Table PQ.A.2-1. Manual AI Channel Accuracy Data – Post Qualification.

Static Step (4-20 mA equivalent)	Input to AI Card (mA)	Output from AI Card (mA)	AI Channel Accuracy (% of difference)
10%			
30%			
50%			
70%			
90%			

Table PQ.A.2-2. Manual AI Channel Re-Calibration Data

AI16F Board, Serial # 31030007, Channel 1.

Static Step (4-20 mA equivalent)	Input to AI Card (mA)	Output from AI Card (mA)	AI Card Accuracy (% of difference)
10%			
30%			
50%			
70%			
90%			

PQ.A.3 4-20 mA AO Channel Accuracy (Section 4.1.2)

Manual AO accuracy test results during post qualification phase are listed in Table PQ.A.3-1. It is clear that the results are within the 0.1% acceptance range and are consistent with pre-qualification test results. Notably, the magnitude of AO measurement deviation decreased with the increment of output AO signal level. For example, at 10% level, deviation averaged at 0.025%, whereas deviation averaged at 0% at 90% level.

Table PQ.A.3-1. Manual AO Channel Accuracy Data – Post Qualification.

Static Step (4-20 mA equivalent)	Input to AO Card (mA)	Output from AO Card (mA)	AO Card Accuracy (% of difference)
10%			
30%			
50%			
70%			
90%			

PQ.A.4 Type 100 Ohm RTD Card Accuracy (Section 4.1.4)

The manual RTD accuracy test results from channels 1 and 2 during post-qualification phase are listed in Table PQ.A.4-1. Channel 8 was not tested because it was having a bad contact. It is clear from the table that neither channel met the 0.1% acceptance criteria except for the readings at 210 °C for channel 1, which was a degradation from pre-qualification results where channel 1 met the 0.1% criteria at all temperature levels, although channel 2 met the criteria only at certain temperature levels. Results in Table PQ.A.4-1 also show an apparent trend of larger deviations at higher temperature levels with the exception of at 210 °C. By contrast, the deviations were consistent at different temperature levels in the pre-qualification test.

Table PQ.A.4-1. Manual RTD Channel Accuracy Data – Post Qualification.

Input (°C)	CH1			CH2		
	AI Count	°C	Accuracy (% difference)	AI Count	°C	Accuracy (% difference)
70						
210						
350						

490						
630						

PQ.A.5 Manual Pulse Input Card (Section 4.1.5)

The manual pulse input card accuracy test results for accumulate mode are listed in Table PQ.A.5-1. There are no acceptance criteria regarding the pulse card accuracy defined in the test procedure. However, the test results demonstrate a significant improvement over those from pre-qualification test. More specifically, the accuracy was 0.00%-0.227% at prescaler 1 and was 0.001%-0.065% for prescaler 100, compared to pre-qualification results of 0.156%-1.139% at prescaler 1 and 0.127%-1.093% at prescaler 100.

Table PQ.A.5-1. Manual Pulse Input Card Accuracy Data (Accumulate Mode) – Post Qualification.

Input Frequency		Indicated Rate						Accuracy (%)	
		Prescaler Value = 1			Prescaler Value = 100				
Nominal (Hz)	Measured (Hz)	Recorded Start Count	Recorded Final Count	Calculated Rate (Hz)	Recorded Start Count	Recorded Final Count	Calculated rate (Hz)	Prescaler = 1	Prescaler =100
50	49.8022								
5000	4985.7								
10000	10002.8								
15000	14978.8								
195000	19459.1								

The manual pulse input card accuracy test results for rate mode with 8 bit and 12 bit configurations are shown in Table PQ.A.5-2. There are no acceptance criteria defined in the test procedure for pulse card rate mode accuracy test. Measurements from 8-bit mode are in line with pre-qualification test results. However, measurements from 12-bit mode show significant improvement over pre-qualification test at low frequency range: 0.005% vs. 1.79% at 50 Hz, and 0.005% vs. 0.294% at 600 Hz.

Table PQ.A.5-2. Manual Pulse Input Card Accuracy Data (Rate Mode) – Post Qualification.

Input Frequency (Hz)		8 bit					12 bit		
Nominal	Measured	8 Bit Image	8 Bit Image	Calculated Frequency	Calculated Frequency	Accuracy (%)	12 Bit Image	Calculated Frequency	Accuracy (%)
50	49.817								
600	594.91								
5000	4986.4								
10000	10004.9								
15000	14981.1								
19500	19461								

PQ.A.6 Automated Analog Accuracy Test (Section 4.1.6)

The test data logged by HAS logger for automated AI accuracy test are shown in Table PQ.A.6-1. This automated logging system incorporates the HPAT's AO channel's inaccuracy. It is clear that although the deadband of HAS logger was changed from 0.5 to 0.0 in the post qualification test, the AI accuracy results are still outside the acceptance range of 0.1%. As a comparison, the results from pre-qualification test are listed in Table PA.A.6-2. Obviously, post qualification results do improve over the pre-qualification results although two different AI cards were used in these tests. Post qualification results also show apparent trend of lower deviations with higher input signal levels.

Table PQ.A.6-1. Automated AI Accuracy Test – Post Qualification.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1,BL,506					
2,BL,215					

Table PQ.A.6-2. Automated AI Accuracy Test – Pre Qualification.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
1,BL,506					
2,BL,215					

Table PQ.A.6-3 shows the automated AO accuracy test results from post qualification test. It is clear that the results were well within the acceptance range and are consistent with pre-qualification test.

Table PQ.A.6-3. Automated AO Accuracy Test – Post Qualification.

Tag Name	Time Stamp	Value (%)	Description	Expected (%)	Accuracy (%)
2,BL,211					

Table PQ.A.6-4 lists RTD accuracy test results during post-qualification phase. 1,BL,528 and 1,BL,548 show higher temperature readings, but 1,BL,10 shows lower temperature reading than the corresponding pre-qualification results. This deviation is probably caused by the resistance change of the resistors from the stress test as well as the contact resistances change from the rewiring process. Resistors were used to simulate RTD inputs to the card during the automated RTD accuracy test.

Table PQ.A.6-4. Automated RTD Accuracy Test – Post Qualification.

Tag Name	Average (°C)	Pre-qualification Result (°C)	Difference (°C)
1,BL,10			
1,BL,528			
1,BL,548			

PQ.A.7 Digital Response Time Measurement (Section 4.2.1)

Manual Test Execution

Refer to Baseline Report (TS901-000-22).

Automated Test Execution

Results of automated digital response time test during the post qualification test are listed in Table PQ.A.7-1. For sake of comparison, corresponding results from pre qualification test are also included in the table. It should be noted that due to a wiring inconsistency, in pre-qualification test, the HPAT square waveform was wired to 4,DI,9, whereas in post qualification test, it was rewired to 4,DI,16. Direct digital response time measurement averages at 112 ± 78 ms, compared with 104 ± 27 ms from the pre-qualification test. It is clear that the response time from direct measurement does not meet the 100 ms acceptance criteria, but deviates less than 10% from the pre-qualification result. However, the post qualification measurements display a significant larger standard deviation. The indirect (cascaded) digital response time measurements average between 88 and 93 ms with standard deviation ranging from 17 to 47 ms, which meets the criterion and deviates less than 10% from the pre-qualification results. Similar to the pre-qualification results , the digital response time from the direct measurement is approximately 20 ms longer than the results from measurements of the cascaded tests. This difference is caused by the experimental setup in which the direct measurement linkage undergoes one extra I/O scan relative to the number of scans for the cascaded tests.

Table PQ.A.7-1. Digital Response Time from Pre-qualification and Post Qualification Test.

Test	Direct Measurement	Cascaded Measurement					
	4,DI,16 (9)-4,DI,8 (s)	4,DI,3-4,DI,2 (s)	4,DI,4-4,DI,3 (s)	4,DI,5-4,DI,4 (s)	4,DI,6-4,DI,5 (s)	4,DI,7-4,DI,6 (s)	4,DI,1-4,DI,7 (s)
Pre Q	0.104 ± 0.027						
Post Q	0.112 ± 0.078						

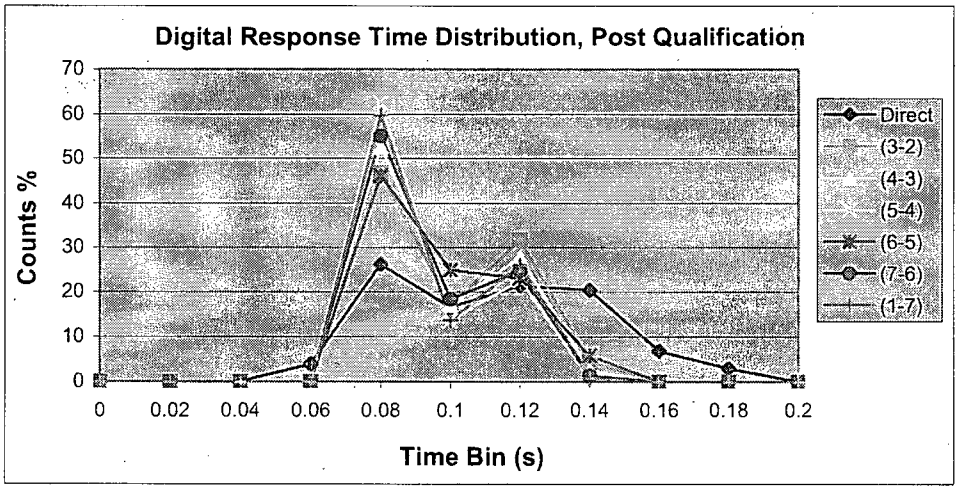

Figure PQ.A.7-1. Distribution of Digital Response Time During the Post Qualification Test.

Figure PQ.A.7-1 plots the distribution pattern of the digital response time measurements during the post qualification test. Similar to the pre-qualification results, the results from different measurement methods display different distribution patterns: the response time from the direct measurement method spans a larger timeframe and is also more evenly distributed; by contrast, the results from the cascaded test method span over a smaller timeframe and are more concentrated at a few time bins. For example, in direct response time measurement, the counts % for time bins 60-80 ms, 80-100 ms, 120-100 ms, and 140-120 ms are roughly the same, whereas in cascaded tests more than 90% of counts are located at three time bins: 60-80 ms (~50-60%), 100-120 ms (~20-30%), and 100-80 ms (~15%).

PQ.A.8 TSAP Analog Response Time Test (Section 4.2.2)

Manual Test Execution

The results from manual analog response time measurement during the post qualification test are listed in Table PQ.A.8-1. 1,AI,883 is the analog step signal, and 1,DO,401 is the simulated trip output from 1,AI,883. The leading edge response time of 4.054 s represents a slight decrement from the pre-qualification result of 4.11 s. On the other hand, the trailing edge response time of 3.542 s represents a slight increment from the pre-qualification result of 3.43 s. In both cases, the post qualification results deviate less than 10% from the pre-qualifications results.

Table PQ.A.8-1. Manual Analog Response Time Measurement Data During Post Qualification Test.

	1,AI,883 Period (s)	1,AI,883 High Duration (s)	1,AI,883 Low Duration (s)	Leading Edge Response Time (s)	Trailing Edge Response Time (s)	1,DO,401 Active Period (s)
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
Average						
STD						

Automated Test Execution

The automated analog response time results from post qualification test are listed in Table PQ.A.8-2. The data were obtained by processing the SOE data of TSAP simulated trip output signal (1,DO,401), which was logged as 4,DI,10. The results deviate less than 10% from those from pre-qualification test. More specifically, the periods for trip waveform, Set, and Reset are 20.01s, 10.454 s, 9.553 s respectively, compared with 20.005 s, 10.716 s, 9.289 s in the pre-qualification test.

Table A.8-2. Automated Analog Response Time Test Results from Post Qualification Test.

4,DI,10	Trip Waveform Period (ON, s)	Trip Waveform Period (OFF, s)	Set Period (s)	Reset Period (s)
1				
2				
3				
4				
5				
6				
Average				
STD				

PQ.A.9 Discrete Input Operability Test (Section 4.3)

The discrete input operability test results are listed in Table PQ.A.9-1. Each channel under test cycled the input voltage a total of three times.

Table PQ.A.9-1. Discrete Input Operability Test Results from Post Qualification Test.

Test	Card Type Under Test											
	DI16I				DC34				DC33			
	1	2	3	Average	1	2	3	Average	1	2	3	Average
Set Voltage Threshold (V)												
Maximum Input Voltage (V)												
Dropout Voltage (V)												

It is clear from the table that the DI channels met all of the acceptance criteria for the set voltage level, dropout voltage, and the maximum input voltage as specified in Section A.9 of Appendix A of the Baseline Testing Summary Report (TS-901-22). There was no significant change in the DI channel operation compared to the pre-qualification results, though set voltage threshold readings for DI16I and DC33 were slightly lower in post qualification test.

PQ.A.10 Discrete Output Operability Test (Section 4.4)

Refer to Section A.10 of Baseline Report (TS901-000-22).

PQ.A.11 Communication Operability Test (Section 4.5)

ICL Error Counters

Refer to Section A.11 of Baseline Report (TS901-000-22).

PQ.A.12 Timer Test (Section 4.6, 4.6.1, 4.6.2)

Manual Timer Test (Section 4.6.1)

Refer to Section A.12 of Baseline Report (TS901-000-22).

Automated Timer Test (Section 4.6.2)

Refer to Section A.12 of Baseline Report (TS901-000-22).

PQ.A.13 Failover Operability Test (Section 4.7)

Refer to Section A.13 of Baseline Report (TS901-000-22).

PQ.A.14 Loss of Power Test (4.8)

Refer to Section A.14 of Baseline Report (TS901-000-22).

PQ.A.15 Power Interruption Test (Section 4.9)

Refer to Section A.15 of Baseline Report (TS901-000-22).

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APPENDIX PQ.B

PRUDENCY TESTS

PQ.B.1 General

The purpose of this attachment is to document the results of the Post Qualification Prudency Tests in Section 4.1 of the Prudency Test Procedure TP0403, Rev. C. These tests were performed following the return of the equipment from the first round of tests at Wyle. The test descriptions and acceptance criteria are provided in Appendix B of the Baseline Testing Summary Report (TS901-000-22).

PQ.B.2 Digital Input/Output BOE Test (Section 4.1.2)

Due to a wiring inconsistency, the digital BOE points logged during the pre-qualification and Wyle tests were 4,DI,24 to 4,DI,30, but changed to 4,DI,28 to 4,DI,36 in the post qualification test.

By analyzing the alarm reports throughout the prudency BOE test, it is concluded that no link alarm condition was detected for the DI cards whose channels were logged by SOE logger. SOE data from the post qualification test was analyzed. All abnormal transitions and the associated timestamps are listed in Table PQ.B.2-1. The abnormal transition at the end of the test, i.e., at around 8:26:11 AM, happened to all monitored digital channels. This anomaly is caused by the perturbation from stopping the BOE test and thus should not be counted as the irregular transition. The numbers in shade represent transition times of contact bounces. A total of 6 contact bounces from 4 channels occurred during the test period, a moderate increment from four occurrences during the pre-qualification test.

Table PQ.B.2-1. Digital BOE Abnormal Transitions in the Post Qualification Test.

Time Stamp	Transition Time Duration (Seconds)								
	4,DI,28	4,DI,29	4,DI,30	4,DI,31	4,DI,32	4,DI,33	4,DI,34	4,DI,35	4,DI,36
08:25:22.6317									
08:25:22.6318									
08:25:29.4614									
08:25:29.5253									
08:25:29.5262									
08:26:11.2303									

Excluding the occurrences of contact bounces and abnormal transitions caused by the stopping of BOE test, there were a total of 6 abnormal transitions. The first one occurred at 8:25:29 AM from channel 4,DI,28. The transition time of 1.8545 s represents a 85.45% higher than the preset value of 1 s, which is significantly greater than the 15% acceptance criteria. Noticeably, this transition was followed immediately by another abnormal transition (0.0639 s) and one contact bounce (0.0009 s).

The other five abnormal transitions occurred approximately 60 ms after the 1.8545 s transition for channels 4,DI,28, 4,DI,30, 4,DI,31, 4,DI,33, 4,DI,34. They were all followed by a contact bounce except 4,DI,30. Since this test ran for 1 minute and all 6

abnormal transitions occurred within 60 ms, it is likely that the abnormal trasitions were caused by a common disruption to the system. No transition was missing and no link alarms were reported during the test. Therefore, excluding the abnormal transitions probably caused by a common system disruption, the test met the acceptance criteria.

PQ.B.3 Analog BOE Test (Section 4.1.2)

The BOE waveform is generated by 2,BL286 in the HPAT, and this signal is used to control five AO channels (2,AO,82; 2,AO,84; 2,AO,85 (not logged); 2,AO,86; and 2AO,87). These AO channels were routed to corresponding AI channels of the Test Specimen (1,AI,882; 1,AI,884; 1,AI901; 1,AI,902; and 1,AI,902). Because the AI image is not directly accessible for logging, each input was mapped to an AIC block in the TSAP, and the resulting block value was logged by the HAS. In addition, the value for 1,AI,882 was mapped through the TSAP to the output image for 1,AO,922, and the resulting signal was routed to 2,AI,70, producing a closed loop.

The waveforms of TSAP analog inputs at remote 1 and that of the driving BOE signal during the post qualification test are depicted in Figure PQ.B.3-1. The TSAP AI signals duplicate each transition of the BOE source signal, and the three AI images exhibit the same characteristics. In each cycle, the values closest to 10% and 90% were extracted from HAS data for 1,BL,510, 1,BL,514, and 1,BL,516. These values have been averaged and presented in Table PQ.B.3-1. The averaged deviations at 10% for all three AI channels meet the 0.32% acceptance criteria, which is consistent with pre-qualification results. However, the values are significantly smaller than pre-qualification results: 0.010% vs. 0.188% for 1,BL,510, 0.055% vs. 0.232% for 1,BL,514, and 0.165% vs. 0.298% for 1,BL,516. At the 90% level, 1,BL,510 and 1,BL,514 meet the 0.32% criteria whereas 1,BL,516 does not, an improvement from pre-qualification test where all three AI signals deviate more than 0.32% from the BOE source signal at 90% level. It should be noted that during the post qualification test, the HAS deadband was changed to 0% from 0.5% and the AI card processing the 1,AI,882 and 1,AI,884 channels was replaced with a spare card. The improvement over the baseline results is likely caused by the combination of these two changes. The AI card processing the remaining AI channels was not changed, and its performance had changed little from that of the baseline result.

AIC block 1,BL,510 served as the source of the BOE signal returned from the test specimen back to the HPAT (1,AO,922 to 2,AI,70). Figure PQ.B.3-2 shows the image of 1,AI,70 as processed by 1,BL,213. As before, the HPAT image tracks each transition of the source signal. In each cycle, the values closest to 10% and 90% were extracted from HAS data, averaged, and the resulting values are listed in Table PQ.B.3-2. Deviations of 2,BL,213 from 1,BL,510 meet the 0.3% acceptance criteria at both 10% and 90% levels, which is consistent with pre-qualification results.

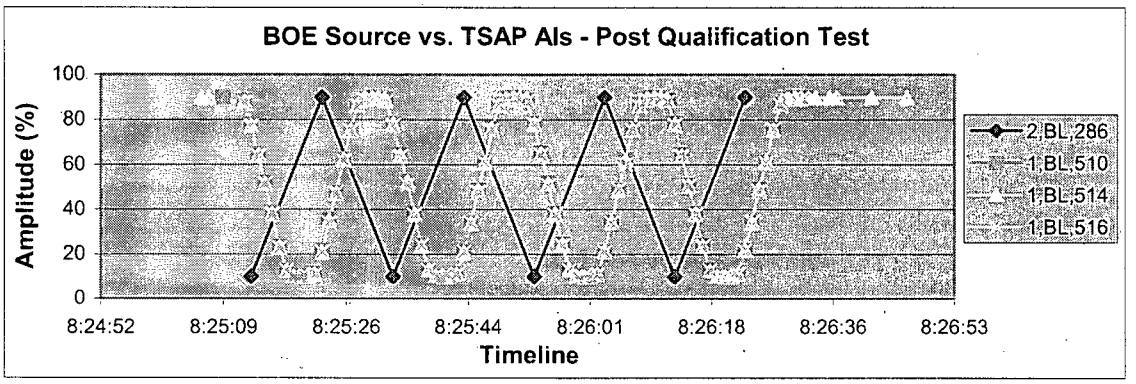

Figure PQ.B.3-1. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 in the Post Qualification Test.

Table PQ.B.3-1. TSAP AI Channel Readings and Deviations from BOE Source Signal in Post Qualification Test.

	1,AI,882 (1,BL,510)	1,AI,884 (1,BL,514)	1,AI,901 (1,BL,516)
10% Measurement (%)			
Deviation From 10% (%)			
Num of Measurements			
90% Measurement (%)			
Deviation From 90% (%)			
Num of Measurements			

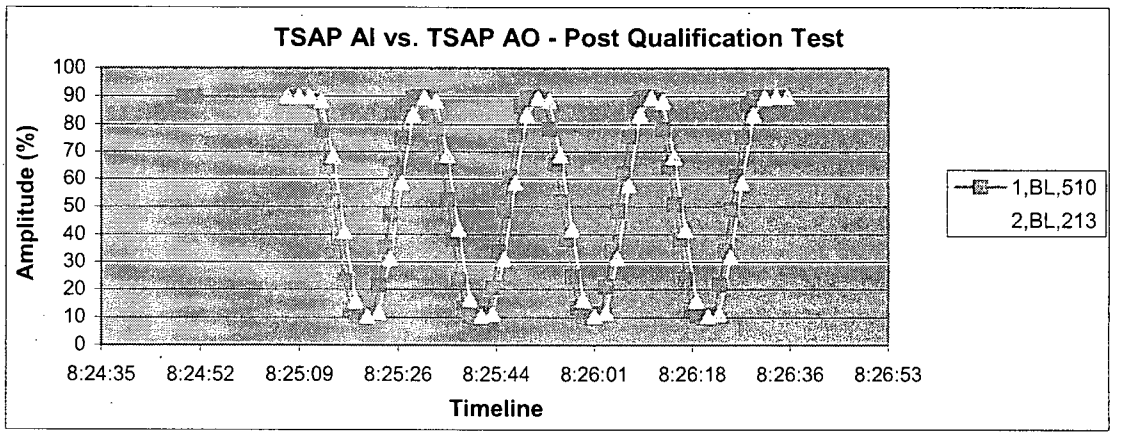

Figure PQ.B.3-2. TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) in the Post Qualification Test.

Table PQ.B.3-2. TSAP AOs and the Corresponding TSAP AIs in Remote1 in the Post Qualification Test.

	1,AI,882 (1,BL,510)	1,AO,922 (2,BL,213)	Deviation (2,BL,213 vs. 1,BL,510) (%)
10% Measurement (%)			
Number of Measurements			
90% Measurement (%)			
Number of Measurements			

PQ.B.4 Serial Port Failure Tests (Section 4.2)

PQ.B.4.1 ICL Failure Test (Section 4.2.2)

Abnormal transitions and the corresponding timestamps for logged digital channels during the ICL failure test are listed in Table B.4-1. The abnormal transitions occurred during the test of shorting the TX pin to RX pin appeared at the end of the test. They were caused by the perturbation from stopping the BOE test. All other transitions occurred within 0.85-1.15 s.

Table B.4-1. Digital BOE Abnormal Transitions from ICL Failure Test of In-house Test for Seismic Retest.

	Time Stamp			4,DI,28 Transition (s)	4,DI,29 Transition (s)	4,DI,30 Transition (s)	4,DI,31 Transition (s)	4,DI,32 Transition (s)	4,DI,33 Transition (s)	4,DI,34 Transition (s)	4,DI,35 Transition (s)	4,DI,36 Transition (s)
Breakout												
Normal												
TX Pin Float												
Short Ground												
Short RX Pin												
Regular Cable												

PQ.B.5 Serial Link Noise Test (Section 4.3.2)

This test was not required to be executed as part of the post testing sequence.

PQ.B.5 Fault Simulation Test (Section 4.3.3)

Not Applicable, see Section B.5 of Baseline Report (TS901-000-22).

HF Controls

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NON-PROPRIETARY

HFC-6000 Control System

ERD111 – Control System Qualification Project

Summary Report for Burn-in Test, Setup and Checkout Test, TSAP Validation Test

TS901-000-30

Rev B

Effective Date	09/15/07
Author/Title	Allen Hsu/William Gill
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1.0 PURPOSE AND SCOPE

The purpose of this report is to provide the performed on the HFC-6000 control system (Test Specimen). The tests include PCB burn-in test, system set-up and check-out, and TSAP validation test. These prequalification tests serve to validate that the test specimen meets the hardware and system application criteria before the first execution of the Operability and Prudency tests which provides a system performance baseline for subsequent qualification tests.

This report describes the types of tests performed, provides a summary of the test results, and evaluates those results based on the acceptance criteria.

2.0 REFERENCES

2.1 INDUSTRY STANDARDS

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants

2.2 RELATED PLANS AND PROCEDURES

TN0401	Master Test Plan
VV0414	Master Configuration List
TP0410	Burn-in Test Procedure
TP0401	Integration (Setup and Checkout) Procedure
TP0408	TSAP Validation Test Procedure

2.3 HFC INTERNAL STANDARDS AND PROCEDURES

QPP 5.1	Review and Approval of Quality Documents
QPP 11.1	Test Control
WI-ENG-003	Configuration Management
WI-ENG-205	Develop Software/Firmware Test Procedure
372000-43	WIN_EWS User's Guide

2.4 REFERENCE DOCUMENTS

700907-01	Schematic Wiring Diagram, TSAP
700909-01	System Arrangement, Controller-FOT Configuration
700916-01	Power Distribution, TSAP Configuration
700910-01	TSAP Card Layout
700910-02	HPAT Card Layout
700912-01	TSAP System Assay
700912-01	TSAP Configuration – System Assay
700715-00	I/O Wiring Schematic Diagram – Cover Sheet

700715-01	I/O Wiring Schematic Diagram – Digital Inputs (2 sheets)
700715-02	I/O Wiring Schematic Diagram – Digital Outputs
700715-03	I/O Wiring Schematic Diagram – Analog Inputs
700715-04	I/O Wiring Schematic Diagram – Analog Outputs
700715-05	I/O Wiring Schematic Diagram – Digital Combination
700715-06	I/O Wiring Schematic Diagram – Analog Combination
700715-07	I/O Wiring Schematic Diagram – Single Controller
700916-01	Power Distribution – TSAP Configuration (2 sheets)
700901-09	TSAP Requirements Specification
700901-10	HPAT Requirements Specification
700907-01	TSAP Logic Diagram
700908-01	HPAT Logic Diagram
ASC0401	TSAP Program Listing
ASC0402	HPAT Program Listing

2.5 SPECIAL TERMS, ABBREVIATIONS, AND ACRONYMS

BOM	Bill of Material
EWS	Engineer Workstation
HPAT	HFC Plant Automatic Tester
FOT	Fiber-Optics Transmitter
JCRT	Java CRT
OIS	Operator Interface System
PCB	Printed Circuit Board
TSAP	Test Application which is a synthetic application program to be used for qualification testing

3.0 BURN-IN TEST

The burn-in test requires a minimum period of 352 cumulative hours of operation. The purpose of this test is to detect any early-life failures of components and circuit cards. During the test period, all cards under test must remain in a normal operating state. Only those cards that pass the burn-in test will be placed into inventory for subsequent use as part of the HFC-6000 Test Specimen.

3.1 PCB CARDS TESTED

The following circuit card assemblies were included in the burn-in test.

Table 3. 1. **HFC-6000 Modules Included in the Burn-in Test**

Module Type	Description
HFC-ILR06	I/O Link Repeater/Terminator
HFC-SBC06	Main Controller Card
HFC-DPM06	Dual-Ported Memory
HFC-DI16I	16-Channel Digital Input and SOE Card
HFC-DO8J	8-Channel Relay Output Card

HFC-DC33Q	Special Function Card (120 vac output)
HFC-DC34Q	Special Function Card (125-vdc output)
HFC-AI4K	4-Channel Pulse Input Card
HFC-AI16F	16-Channel Analog Input Card
HFC-AC36F	8-Channel AI, 8-Channel AO Card
HFC-AO8F	8-Channel Analog Output Card
HFC-AI8M	8-Channel 100 Ohm RTD Input Card

3.2 ACCEPTANCE CRITERIA

The card edge LEDs for each card under test indicates normal operation of the card during the test interval and is an indication of the successful operation of the card during the burn-in test.

3.3 TEST RESULTS

The assemblies under burn-in test were verified periodically every day and the status was logged into an electronic database. All assemblies under burn-in test reached the minimum 352 cumulative hours of operation without failure.

3.4 CONCLUSION

All assemblies except HFC-FPC06 passed the 352 cumulative burn-in test without failure.

4.0 SET-UP AND CHECK-OUT TEST

The purpose of this procedure is to verify that the project specified hardware, wiring, and communication cabling has been installed correctly and that communication has been established over each communication link prior to performing TSAP Validation Test.

4.1 TEST SEQUENCES

Included in the scope of these tests are the following activities:

- Verify that all project specified equipment / hardware has been received, functionally tested, and set-up per project documents.
- Verify correct software is installed in Test Specimen, HPAT, and OIS/EWS.
- Perform a continuity test for all interconnection wiring.
- Verify that C-Link communication has been established.
- Verify that all HFC-6000 I/O modules are functional and communicating with SBC-06 controller.

4.2 ACCEPTANCE CRITERIA

The overall method used for verifying correct hardware component installation and functional operation consisted of highlighting the relevant engineering drawing(s) as each item was verified to be operating correctly.

4.2.1 Equipment / Hardware

1. All hardware components and communication cables depicted on the BOM and drawing 700912-01 have been highlighted.
2. All Test Specimen's PCBs depicted on drawing 700910-01 have been highlighted.
3. All HPAT's PCBs depicted on drawing 700910-02 have been highlighted.

4.2.2 Continuity Test

1. All circuits depicted on drawing 700916-01 have been highlighted
2. All circuits depicted on drawing 700909-01 have been highlighted
3. All external (field) wiring circuits on drawings 700715-00 thru 700715-07 have been highlighted
4. Drawing and BOM 700912-01: BOM Mark Numbers: 4,19,28,33,40 and 50 have been highlighted

4.2.3 I/O Functional Test

1. Digital Inputs: All digital inputs channels on the Loop Schematics have been highlighted.
2. Digital Outputs: All digital outputs channels on the Loop Schematics have been highlighted.
3. Analog Input (0-20 mAdc): All analog inputs (0-20 mAdc) channels on the Loop Schematics have been highlighted.
4. Analog Outputs: All analog outputs (0-20 mAdc) channels on the Loop Schematics have been highlighted.
5. RTD Input (100 Ohm Platinum): All RTD inputs channels on the Loop Schematics have been highlighted..
6. Pulse Input: All pulse input channels on the Loop Schematics have been highlighted.

4.3 TEST RESULT

- Equipment / Hardware

  BOM and Drawing 700912-01, Drawing 700910-01, Drawing 700910-02 were verified and signed off by test engineers.

- Continuity Test

  Continuity checks were performed on Drawings 700916-01, 700909-01, 700715-00 through 700715-07, Drawing and BOM 700912-01, and Drawing 700916-02 and test logs were signed off.

- I/O Functional Test

  All digital and analog IO cards were tested individually. See attached Excel file for test results for analog cards.

4.4 CONCLUSION

Test results have met all acceptance criteria for set-up and check-out test. Test results for analog cards are shown in Table 5.2 and Table 5.3. These results and the analog accuracy test results from subsequent baseline testing are used for comparison to accuracy results from future stress testing.

5.0 TSAP VALIDATION TEST

A synthetic application program, TSAP, installed in the test specimen includes sample control logic for power plant processes as well as logic to support automated qualification testing.

5.1 TEST SEQUENCE

The overall validation test is accomplished in two stages: source code verification, and system functional test. During source code verification, the content of the source code text files are validated against the logic diagrams from which they were created. During the functional test, the application code is installed in the controller, and functional operation of the Operability tests, Prudency Burst of Events test, and simulated control loops are verified to be correct. The test sequence includes the following activities:

- **Source Code Verification** – The source code file generated by the HFC One-Step utility program is examined line by line and compared with the graphic representation of logic diagrams 700907-01, 700907-02, and 700908-01.

- **Loop Logic Test** – This test verifies functional operation of the logic for each sample control loop based on the algorithm in the TSAP logic diagrams.

- **Operability Test Support** - This test verifies functional operation of the TSAP code designed to support Operability testing and verifies that the test design produces the expected data. The automated Operability tests are controlled by application code installed in the HPAT. Execution of this test excludes automated logging of test results, which is to be accomplished during the first execution of the subsequent Operability tests.

- **Prudency Test Support** - This test verifies functional operation of the TSAP code designed to support the automated Prudency tests. The automated Prudency tests are controlled by application code installed in the HPAT. Execution of this test excludes automated logging of test results, which is to be accomplished during the first execution of the subsequent Prudency tests.

5.2 ACCEPTANCE CRITERIA

Acceptable results for the TSAP are based on the verification of the specific conditions listed in Table 5.1.

***Table 5. 1.* TSAP Acceptance Criteria.**

Source Code Verification	
	All point types and point designations match those in the logic diagrams.
	All logic connections traced from point to point match the connections shown in the logic diagrams.
	All timer preset values match those shown in the logic diagrams.
	All internal block structures contain the values shown in the logic diagrams.
Accuracy Tests	
	JCRT interface enables test engineer to start/stop the automated accuracy test.
	All AI and AO channels listed for the automated accuracy test exhibit the test waveform while the test is enabled.
	Response time of the system to each step is sufficient to permit accurate recording of the AI and AO channel performance.
	RTD AI channel configured and responds to simulated input.
	Pulse card configured with one channel pair in Rate mode and the other channel pair in Accumulate mode.
	Both pulse card inputs respond to simulated input signal.
Digital Response Time Algorithm	
	JCRT interface enables test engineer to start/stop automated response time test algorithms.
	While digital response time test is running, the TSAP algorithm produces a free running square wave composed of 7 DI channels and 7 DO channels.
	Free-running TSAP algorithm permits accurate measurement of average cycle time for the Equation Interpreter (plus jitter).
	HPAT algorithm produces a free-running 0.5 Hz square wave.
	The HPAT algorithm drives a simulated trip memory in the TSAP. The input transition to the resulting output transition permits accurate measurement of system digital response time (plus jitter).
Analog Response Time Algorithm	
	JCRT interface enables test engineer to start/stop automated response time test algorithms.
	The HPAT algorithm produces a free running 0.5 Hz analog square wave that switches between 45% and 55% of span.

	The TSAP algorithm provides an alarm block to trigger a simulated trip memory.
	The duration from input transition to trip memory output permits accurate measurement of system analog response time (plus jitter).
Operability Timer Test	
	JCRT interface enables test engineer to start/stop automated time test algorithms.
	TSAP provides four timers that produce two free-running square waves while the test is enabled.
	Test waveforms enable direct measurement of periods for 1-second and 5-second timers (plus jitter).
TSAP Special Functions	
	1,DO,647 provides a 1 Hz heartbeat display that provides a visual indication that the Test Specimen Equation Interpreter is running.
	1,CO,50 increments once each Equation Interpreter processing cycle. This running count provides a precise indication of processing speed during any fixed period of time.
	The TSAP monitors status of each power supply. Failure of any power supply triggers a common power monitor alarm.
Burst of Events Test	
	JCRT interface enables test engineer to start/stop automated burst of events test algorithms.
	HPAT controls two digital bursts of events 0.5 Hz square waves that are 180 degrees out of phase.
	HPAT controls an analog burst of event 0.5 Hz square wave that switches between 10% and 90% of span.
	While test is running, all points listed in Table 5 exhibit activity. When test is disabled, all of these points remain static.
Simulated Digital Control Loops	
	JCRT provides display interface for controlling inputs to the control loop and for monitoring overall loop status, including alarm conditions.
	TSAP functional response to each DI channel connected to the internal logic verified for both TRUE and FALSE logic states.
	TSAP control of each DO channel connected to internal logic verified based on logic input states.
	TSAP control of alarm status verified based on simulated alarm conditions.
Simulated Analog Control Loops	
	JCRT provides display interface for controlling inputs to the control loop and for monitoring overall loop status, including alarm conditions.
	In Manual mode, M/A station permits manual control of the loop output variable.
	HPAT algorithm provides closed-loop simulation of an external process.
	After tuning is complete, the closed loop simulation enables the loop to reach a balanced state while operating in Auto mode without oscillation.

5.3 TEST RESULT

- **Source Code Verification**

  The TSAP source code was verified to assure the functional requirements were correctly implemented. All deviations were documented and corrected. The corrections were verified.

- **Accuracy Tests**

  Manual accuracy tests during the TSAP validation test are listed in Tables 5.2, 5.3, 5.4, 5.5, and 5.6. The main purpose of these tests was to validate the TSAP functionality.

Table 5. 2. **AI Accuracy Test During TSAP Validation Test.**

Test Signal (%)	AI Test Algorithm 1,BL, 506 Count Value		Calculated Signal (%)		Accuracy (%)	
	Test 1	Test 2	Test 1	Test 2	Test 1	Test 2
10	9073	9059	9.612	9.558	-0.388	-0.442
30	14306	14306	29.575	29.575	-0.425	-0.425
50	19539		49.538		-0.462	
70	24795	24797	69.588	69.596	-0.412	-0.404
90	30036		89.582		-0.418	

Table 5. 3. **AO Accuracy Test During TSAP Validation Test.**

Test Signal (%)	AO Test Algorithm 2,BL,211 Count Value		Calculated Signal (%)		Accuracy (%)	
	Test 1	Test 2	Test 1	Test 2	Test 1	Test 2
10	9170	9169	9.982	9.978	-0.018	-0.0220
30	14416	14419	29.994	30.006	-0.00565	0.00580
50	19660	19657	49.999	49.988	-0.00076	-0.0122
70	24907	24895	70.016	69.970	0.0156	-0.0302
90	30148	30149	90.009	90.013	0.009	0.0128

Table 5. 4. **Type 100 Ohm RTD Accuracy Test During TSAP Validation Test.**

Input (°C)	Expected Count	AI Image	Accuracy (%)
10	468	492	0.0732
200	9362	9376	0.0427
500	23405	23400	-0.0153

Table 5. 5. **Pulse Card Accuracy Test During TSAP Validation Test (Rate Mode, 12-bit Resolution).**

Input Signal		Indicated Rate		
Nominal (kHz)	Measured Frequency (kHz)	Measured	Expected Value	Accuracy (%)
3	2.987	612	611.588	0.0673
7	6.976	1429	1428.34	0.0465

Table 5. 6. **Pulse Card Accuracy Test During TSAP Validation Test (Accumulate Mode).**

Input Signal		Accumulated Count Over 300 Seconds (Prescaler Value =10)									
		Pulse Card from Rack 4 Slot 11					Pulse Card from Rack 4 Slot 12				
Nominal (Hz)	Measured Frequency (Hz)	Start Count	Final Count	Difference	Expected	Accuracy (%)	Start Count	Final Count	Difference	Expected	Accuracy (%)
300	296.9	384	9268	8884	8907	-0.258224	754	9680	8926	8907	0.2133154
1100	1097.1	4949	37966	33017	32913	0.315985	3072	34800	31728	32913	-3.6004011

- **Digital Response Time Algorithm**

  The digital response time of the TSAP is defined below;

  Period of free-running square wave signal: 2.0 s
  Calculated average equation cycle time: 91 ms
  Average response time based on one processing cycle: 104 ms
  Average response time based on two processing cycles : 146 ms

- **Analog Response Time Algorithm**

  The analog response time of the TSAP is defined below;

  Period of free-running analog square wave signal: 20 s
  Duration that analog signal is at 55% of output span: 10 s
  Duration that analog signal is at 45% of output span: 10 s
  Average response time based on one processing cycle: ~4.1 s
  Average response time based on two processing cycles: ~4.15 s
  Delay from trailing edge of analog signal to inactive transition of DO: 3.5 s

  It should be noted that during the initial execution of the test algorithm, the 1 second time preset was found to be too fast for the analog response of the Test Specimen. Consequently, the total time period was changed to produce a 45% output for 10 seconds and a 55% output for 10 seconds.

- **Operability Timer Test**

  The test was performed according to test procedure. The screen captures part of the test data was lost during test. The loss of this data does not have a significant impact on the overall assessment of the test results since other test data was available to perform the required analyses and reach conclusions.

- **TSAP Special Functions**

  All TASP special functions were tested and signed off properly by the test engineer against the acceptance criteria. BOE timer preset values of 1 second, 1.5 seconds, and 10 seconds were used to produce the response curve for the TSAP.

- **Burst of Events Test**

  All BOE related functionalities were tested and signed off properly by the test engineer against the acceptance criteria.

- **Simulated Digital Control Loops**

  Each simulated digital control loop was tested and signed off properly by the test engineer against the acceptance criteria.

- **Simulated Analog Control Loops**

  Each simulated analog control loop was tested and signed off properly by the test engineer against the acceptance criteria.

5.4 CONCLUSION

The TSAP validation results demonstrated that the TSAP source code generated from the One-step program development tool reflects the logics depicted in the control schematics. Operability test and Prudency test results showed that the response time and accuracy of I/O (both analog and digital) cards fall within the acceptable range. The timer test algorithm was tested and verified. TSAP special functions test, simulated digital and analog control loops test verified that the functions in TSAP correctly execute the controls described in control schematics.

HF Controls

HF CONTROLS CORPORATION

NON-PROPRIETARY

HFC-6000 Control System

ERD111 – Control System Qualification Project

Seismic Retest In-house Testing Summary Report

(Update of Pre-Qualification Tests)

TS901-000-34

Rev B

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11/8/04	2b	X. Li	Reformat Table of Contents
11/10/04	A	X. Li	Rev A Release
9/28/07	B	A Hsu/W Gill	Revised Scope of Topical Report

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1.0 PURPOSE

HFC is generically qualifying its HFC-6000 control system for nuclear safety-related applications in U.S. nuclear power plants. The approach taken for this qualification effort is based on the guidance provided in EPRI-TR-107330, Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants.

This document describes the in-house pre-qualification testing that was performed in preparation for the seismic retesting program. As such, it establishes the baseline data for use during and after the seismic retest. Also included is the update of the Burn-In Test for new modules and the Set-up and Check-out Procedure for the equipment.

An initial baseline was developed for the first set of qualification tests and is reported in the Baseline Testing Summary Report (TS901-000-22, Rev B). However, some of this equipment was damaged and replaced during the subsequent qualification tests which necessitated the development of the new baseline described in this report.

2.0 SCOPE

- Evaluation of Operability and Prudency tests performed during the in-house test for seismic retesting program.
- Evaluation of all anomalies detected during the course of the in-house test for seismic retest.

3.0 REFERENCES AND ACRONYMS

3.1 REFERENCES

TP0408B	Test Specimen Validation Test Procedure
TP0402	Operability Test Procedure
TP0403	Prudency Test Procedure
VV0414	Master Configuration List

3.2 ACRONYMS

BOE	Burst of Events
DDB	Dynamic Database
HAS	Historical Archiving System
HFC	HF Controls
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
PLC	Programmable Logic Controller
RTD	Resistance Temperature Detector
SOE	Sequence of Events
TSAP	Test System Application Program

4.0 TEST DESCRIPTION

The Burn-In, Setup and Checkout, Operability, and Prudency Tests which were performed in-house prior to the seismic retest are a repeat of the testing that was performed during the original Pre-Qualification Test. Refer to the Baseline Report for the test description.

5.0 TEST SETUP

Although the in-house seismic retest was a repeat of the Pre-Qualification testing as described above, the configuration for SOE logging and HAS logging was modified to reduce the number of points to be logged. Refer to the respective test procedures for the detailed changes. Similar to post qualification test, the HAS deadband and DDB broadcast table were also modified as stated in the post qualification test report.

6.0 TEST SEQUENCE

6.1 APPLICATION OBJECT TEST (ATP0402, REV A)

Not applicable to the in-house seismic retest.

6.2 BURN-IN TESTS (TP0410, REV A)

Any new or replacement modules or hardware for the seismic retest underwent 352 hours of cumulative burn-in process.

6.3 TEST SPECIMEN VALIDATION TEST (TP0408, REV B) AND INTEGRATION (SETUP AND CHECKOUT) PROCEDURE (TP0401)

6.3.1 General

The Test Specimen Validation Test and the Integration (Setup and Checkout) Procedure were performed in-house at HFC prior to the seismic retest. This testing was performed to verify proper hardware and software configuration, proper component assembly, and overall integration following reconfiguration in preparation for the seismic retest.

6.3.2 Results

These tests were performed and all equipment was configured as required.

6.3.3 Anomalies

Any anomalies that were found were resolved prior to completion of the procedure.

6.3.4 Summary

The Test Specimen and the test equipment were all configured as required upon completion of these procedures.

6.4 OPERABILITY TEST

6.4.1 General

The HFC-6000 control system (Test Specimen) was configured for the repetition of seismic test, and in-house operability testing was performed to establish a system performance baseline against which the system operability performance during the Wyle seismic retest could be compared.

6.4.2 Results

- All applicable operability tests were performed at the HFC site and the detailed data analysis and conclusions of these tests are documented in Appendix A. See the Baseline Testing Summary Report (TS901-000-22) for a description of these tests.

- Manual AI accuracy test results are within the 0.1% acceptance range. The results were within a range of -0.02% to +0.07%.

- Manual AO accuracy test results are within the 0.1% acceptance range. The results were within a range of +0.01% to +0.03%.

- Manual pulse card accumulate mode accuracy are within ±0.1% at all input frequencies from both 1 and 100 prescaler tests except at 195 kHz from the prescaler = 100 test where the accuracy was +0.42%.

- Manual pulse card rate mode accuracy are well within ±0.1% when the card was operated at 12 bit mode, and the measurements are within range when the card was operated at 8 bit mode.

- Automated AI results are within the 0.1% acceptance range. The results were within a range of -0.012% to +0.07%.

- Automated AO results are well within the 0.1% acceptance range. The results were within a range of 0.000% to +0.013%.

- Automated RTD tests were established as follows: 1,BL,10 = 72.93 °C, 1,BL,528 = 79.95 °C, 1,BL,548 = 79.25 °C.

- Automated pulse card test showed rate mode measurement was within range and accumulate mode had an accuracy of –0.025% over 28 minutes and 11 seconds period.

- Automated digital response time results: 100 ± 30 ms (direct measurement) and 91 ± 18 ms (cascaded measurement).

- Manual analog response time results (redundant configuration): leading edge response time: 4.145 second; trailing edge response time: 3.303 second.

- Automated analog response time results (redundant configuration): leading edge response time: 4.0 second; trailing edge response time: 4.0 second.

- Discrete input operability test demonstrated that DI channels met all of the acceptable criteria for the set voltage level, dropout voltage, and the maximum input voltage.

- The Discrete Output operability test demonstrated that each of the modules continued to operate reliably over the required voltage range and to support the required current loads. Each channel demonstrated the capability of switching reliably under load without arcing or displaying contact bounce.

- There were no ICL errors in the Test Specimen during the in-house test.

- Manual timer test data showed that deviation for 5 second timer was within 1% acceptance range.

- Automated timer test data showed that deviation for 5 second timer was within 1% acceptance range.

- Failover results show that no disruption occurred to analog output signal during the failover process and the maintenance failover has no effect on the operation of digital control loop. As for the digital I/O, no invalid DI or DO transition was detected during the entire failover process.

- Power loss test results show that for both dynamic and static analog outputs, the signals remained at their power-off state until the power was returned; similarly, the digital output signals remained at their de-energized state until the power was recovered.

- During the power quality test, the two power modules A and B from TSAP met the ±1% acceptance criterion at both the low voltage and high voltage tests, For the low voltage test, the TSAP dropped out at 66.4 Vac, and the power supply recovered from the undervoltage condition automatically. However, since the undervoltage condition brought down the entire system, no system status alarm was logged after the power trip. At high voltage test, no system trip was observed up to the limit of the power source: 275 Vac. Lastly, no power supply dropout alarm occurred while source power was within the specified range (90-150 Vac and 57-63 Hz).

6.4.3 Anomalies

6.4.4 Summary

The main purpose of the in-house operability test for seismic retest was to establish a system operability performance baseline. Test results have demonstrated that the system met the acceptance criteria in all tests except for the analog and digital response times and the failures from power interruption test. Nonetheless, the analog and digital response times remain consistent with the system response time performance characteristics established in the baseline report (TS901-000-22).

6.5 PRUDENCY TEST

6.5.1 General

The HFC-6000 control system (Test Specimen) was configured for the repetition of seismic test, and in-house prudency testing was performed to establish a system performance baseline against which the system prudency performance during the Wyle seismic retest could be compared.

6.5.2 Results

- All applicable prudency tests, with the exception of the Fault Simulation Test, were performed at the HFC. The results of these tests are documented in Appendix B.

- The points logged during the digital BOE test were 4,DI,28, 4,DI,32, 4,DI,33, 4,DI,34, 4,DI,35. SOE data demonstrated that all digital transitions occurred within 0.85-1.15 s. Analysis of alarm file showed no link alarm condition for DI card related to digital BOE test.

- TSAP AI signals track SOE source signal at each transition and the deviations from the source signal are less than ±0.32% at both 10% and 90% levels for both 1,BL,510 and 1,BL,516. It should be noted that the accuracy calculation used 9.694% and 89.306% measured straightly from HPAT outputs rather than the algorithm levels of 10% and 90%.

- TSAP AI/AO analysis showed that TSAP AO (2,BL,213) tracked TSAP AI (1,BL,510) at each transition, and the deviation was less than 0.30% at 10% level (0.115%), but was more than 0.30% at 90% level (0.327%).

- ICL failure test showed that no abnormal digital transitions were detected other than the ones caused by the start or stop of the BOE test. All other normal transitions occurred within 0.85-1.15 s. Analog BOE analysis demonstrated that no apparent deviation or disruption from the normal condition was seen in the fault conditions.

- During the serial link noise test, two abnormal transitions occurred during the ICL link noise test with one long transition (1.3354 s) followed immediately by one short transition (0.6094 s). All other transitions occurred within 0.85-1.15 s. Analog BOE analysis demonstrated that no apparent deviation or disruption from the normal condition was seen in the fault conditions in the ICL serial link.

6.5.3 Anomalies

6.5.4 Summary

The main purpose of the in-house prudency test for seismic retest was to establish a system prudency performance baseline. Test results have demonstrated that the system met the acceptance criteria in all tests except for the larger than 0.30% deviation of TSAP AO from TSAP AI at 90% level and the two abnormal digital transitions during the ICL link noise test.

7.0 TEST EVALUATION

The Test Specimen performance either matched or exceeded the system performance established in the baseline report (TS901-000-22)

HFC-6000 Control System

ERD111 – Control System Qualification Project

Seismic Retest In House Testing Summary Report
(Update of Pre-Qualification Operability Tests)

TS901-000-34

Rev B

APPENDIX A

OPERABILITY TESTS

A.1 GENERAL

This attachment covers manual and automated accuracy tests defined in test procedure TP0402. Both manual and automated tests were performed on at least one channel for every type of analog circuit included in the test specimen. The purpose of these tests was to establish a baseline for comparison with system performance during and after the seismic test runs.

A.2 MANUAL 4-20 MA AI CHANNEL ACCURACY

Table A.2-1 summarizes the manual AI accuracy test results during in-house test for seismic retest. It is clear that the results meet 0.1% acceptance criteria. The value listed in the **True Level** column represents the actual signal level presented to the input of the TSAP AI channel. This is the value that should be used as the basis of evaluation for the logged automated test results.

Table A.2-1. Manual AI Channel Accuracy Data from In-house Test for Seismic Retest.

Static Step (4-20 mA equivalent) (%)	Input to AI Card		Output from AI card		AI Channel Accuracy (% of difference)
	Measured Test Signal (mA)	True Level (%)	Indicated TSAP Level (%)	Calculated Signal (mA)	
10					
30					
50					
70					
90					

A.3 MANUAL 4-20 MA AO CHANNEL ACCURACY

Table A.3-1 shows the manual AO accuracy test results during in-house test for seismic retest. The results meet 0.1% acceptance criteria.

Table A.3-1. Manual AO Channel Accuracy Data from In-house Test for Seismic Retest.

Static Step (4-20 mA equivalent) (%)	Input to AO Card (mA)	Output from AO Card (mA)	AO Card Accuracy (% of difference)
10			
30			

Static Step (4-20 mA equivalent) (%)	Input to AO Card (mA)	Output from AO Card (mA)	AO Card Accuracy (% of difference)
50			
70			
90			

Because the automated test requires the HPAT to record the values from the TSAP AO channel, the HPAT AI image for each step level was also recorded during this test. These images provide correction factors for evaluating the results of the automated AO accuracy test, as indicated in Table A.3-2.

Table A.3-2. Development of Correction Factor for Automated AO Test.

Algorithm Level (%)	Expected Signal Level(mA)	Ave. HPAT Signal Image (%)	Image Accuracy (%)	Apparent Signal Level (mA)	Deviation (mA)
10					
30					
50					
70					
90					

A.4 TYPE 100 OHM RTD CARD ACCURACY

Table A.4-1 shows manual RTD accuracy test results during the in-house test for seismic retest.

Table A.4-1. Manual RTD Channel Accuracy Data from In-house Test for Seismic Retest.

Input (°C)	Expected Value	Ch1		Ch2		Ch8	
		Measured Value	Accuracy (%)	Measured Value	Accuracy (%)	Measured Value	Accuracy (%)
70							
210							
350							
490							
630							

Table A.4-2. Manual RTD Channel Accuracy Data after Recalibration.

Input (°C)	Expected Value	Ch1		Ch2		Ch8	
		Measured Value	Accuracy (%)	Measured Value	Accuracy (%)	Measured Value	Accuracy (%)
70							
210							
350							
490							
630							

A.5 MANUAL PULSE INPUT CARD ACCURACY TEST

The general operating parameters of pulse input card are listed in Table A.5-1, and the following conclusions can be drawn against the acceptance criteria:

- Depending on configuration, the minimum peak pulse voltage varies between 22.6 v and 24.4 v at 100 Hz and a 50% duty cycle.
- The maximum input pulse rate for the 8-bit rate mode is 10 kHz; the maximum input pulse rate for both the 12-bit rate mode and the accumulate rate mode is 20 kHz.
- A 100 μs pulse corresponds to a 10 kHz pulse signal at 50% duty cycle. The module responded to this signal in all configuration modes.
- The module accurately responded to 90% duty cycle at 100 Hz in 12-bit rate mode. The 8-bit rate mode image became increasingly unstable above a 75% duty cycle.

Table A.5-1. Summary of General Operating Parameters of Pulse Input Card.

	Rate Mode		Accumulate Mode
	8 Bit	12 Bit	
Minimum Input Pulse Amplitude with 50% Duty Cycle (vpp)			
Maximum Input Pulse Amplitude (vpp)			
Minimum Duty Cycle (%)			
Maximum Duty Cycle (%)			
Minimum Rate Input Frequency (Hz)			
Maximum Rate Input Frequency (kHz)			
Maximum Accumulate Count Value			

Table A.5-2 shows manual pulse input card accuracy test results for accumulate mode from in-house test for seismic retest. There is no acceptance criteria specified for the accuracy performance of the pulse card. However, it can be seen that the accumulate mode accuracy are within ±0.1% at all input frequencies from both 1 and 100 prescaler tests except at 195 kHz from 100 prescaler test.

Table A.5-2. Pulse Input Channel Accumulate Mode Accuracy Data from In-house Test for Seismic Retest.

Input Frequency (Hz)		Indicated Rate								Accuracy (%)	
		Prescaler Value = 1				Prescaler Value = 100					
Nominal	Measured	Recorded Start Count	Recorded Final Count	Accumulated Time (s)	Calculated Rate (Hz)	Recorded Start Count	Recorded Final Count	Accumulated Time (s)	Calculated Rate (Hz)	Prescaler = 1	Prescaler =100
50	49.756										
5000	4978.4										
10000	10002										
15000	14977										
195000	19450										

Table A.5-3 shows manual pulse input card accuracy test results for rate mode with 8 bit and 12 bit configurations from in-house test for seismic retest. There is no acceptance criteria specified for the accuracy performance of the pulse card. However, it can be seen that the rate mode accuracy are well within ±0.1% when the card was operated at 12 bit and the measurements were within the range when the card was operated at 8 bit.

Table A.5-3. Pulse Input Channel Rate Mode Accuracy Data from In-house Test for Seismic Retest.

Input Frequency (HZ)		8 bit					12 bit		
Nominal	Measured	8 Bit Image	8 Bit Image	Calculated Frequency	Calculated Frequency	Accuracy (%)	12 Bit Image	Calculated Frequency	Accuracy (%)
50	49.752								
600	594.454								
5000	4978.5								
10000	10003								
15000	14977.3								
19500	19450.3								

A.6 AUTOMATED ANALOG ACCURACY TEST

A.6.1 AI Automated Test

Table A.6-1 shows the test data logged by HAS logger for AI accuracy test from the in-house test for seismic retest. It is clear that the results are within the acceptance criteria of ±0.1% and will serve as the baseline for AI automated test results from Wyle seismic test.

Table A.6-1. Automated AI Accuracy Test from In-house Test for Seismic Retest.

Tag Name	Algorithm Level (%)	Corrected Level (%)	Averaged Logged Value (%)	Accuracy (%)
1,BL,506				
	10			
	30			
	50			
	70			
	90			
2,BL,215				
	10			
	30			
	50			
	70			

A.6.2 AO Automated Test

Table A.6-2 shows the automated AO accuracy test results. It is clear that the results are within the 0.1% acceptance criteria and will serve as the baseline for AO automated test results from Wyle seismic test.

Table A.6-2. Automated AO Accuracy Test – In-house Test for Seismic Retest.

Tag Name	Algorithm Level (%)	Corrected Level (%)	Averaged Logged Value (%)	Accuracy (%)
2,BL,211				
	10			
	30			
	50			
	70			
	90			

A.6.3 RTD Automated Test

The RTD input signal could not be automated like those for the AI and AO accuracy tests. In order to provide an input value for monitoring, a fixed resistor was connected to each input channel, and the constant current source for each channel produced the voltage drop sensed by each channel. The HAS data for RTD during the automated accuracy test are listed in Table A.6-3. The data would serve as the baseline for the evaluation of RTD performance during the Wyle seismic retest.

Table A.6-3. Automated RTD Accuracy Test – In-house Test for Seismic Retest.

Tag Name	Resistance (Ω)	Average (°C)
1,BL,10	130.52	72.93
1,BL,528	134.20	79.95
1,BL,548	132.83	79.25

A.6.4 Pulse Card Automated Test

The automated test for the pulse card will consist of applying the same signal to two channels. One channel is configured for rate mode, and the other channel is configured for accumulate mode with a prescaler value of 1000. The data from these two channels were logged by HAS logger and the results are listed in Table A.6-4. The pulse card performance in both the rate mode and accumulate mode based on the HAS data is shown in Table A.6-5. In the rate mode measurement, HAS data showed toggling between 0.49% and 0.51% that corresponds to 98 Hz and 100 Hz respectively. Therefore, the input frequency of 100 Hz was within the range. As for the accumulate mode, a calculation based on a 28 minute 11 second period data gave a –0.025% accuracy.

Table A.6-4. HAS Data for Automated Pulse Card Test – In-house Test for Seismic Retest.

Tag Name	Time Stamp	Value (%)	Description
1,BL,535	8/26/2004 1:14:47		Pulse Output Signal
1,BL,535	8/26/2004 1:14:48		Pulse Output Signal
1,BL,535	8/26/2004 1:14:52		Pulse Output Signal
1,BL,535	8/26/2004 1:14:53		Pulse Output Signal
1,BL,535	8/26/2004 1:15:06		Pulse Output Signal
1,BL,535	8/26/2004 1:15:07		Pulse Output Signal
1,BL,535	8/26/2004 1:15:09		Pulse Output Signal
1,BL,535	8/26/2004 1:15:10		Pulse Output Signal
1,BL,535	8/26/2004 1:15:14		Pulse Output Signal
1,BL,539	8/26/2004 1:07:34		Pulse Output Signal
1,BL,539	8/26/2004 1:07:35		Pulse Output Signal
1,BL,539	8/26/2004 1:07:36		Pulse Output Signal
1,BL,539	8/26/2004 1:07:37		Pulse Output Signal
1,BL,539	8/26/2004 1:07:38		Pulse Output Signal
1,BL,539	8/26/2004 1:35:45		Pulse Output Signal
1,BL,539	8/26/2004 1:35:46		Pulse Output Signal
1,BL,539	8/26/2004 1:35:47		Pulse Output Signal
1,BL,539	8/26/2004 1:35:48		Pulse Output Signal
1,BL,539	8/26/2004 1:35:49		Pulse Output Signal

Table A.6-5. Automated Pulse Card Accuracy Test – In-house Test for Seismic Retest.

	Channel 1 (1,AI,1001)	Channel 3 (1,AI,1005)
Configuration		
Input Signal (Hz)		
Indicated Value		
Expected Value		
Error (%)		

A.7 DIGITAL RESPONSE TIME MEASUREMENT

Manual Test Execution

Results of manual digital response time test during in-house test for seismic retest are listed in Table A.7-1. The table contains response measurements for control system configured with single or redundant controllers. Results show that the square waveform period measurement in a redundant system is ~80 ms longer than the corresponding measurement in a single controller system. Similarly, the direct digital response time measurement in a redundant system is significantly longer than in a single controller system: 106.9 ms vs. 72.6 ms. The response time of 106.9 ms does not meet the acceptance criterion of 100 ms, but consistent with the results from baseline report (TS901-000-22).

Table A.7-1. Manual Measurement of Digital Response Time from In-house Test for Seismic Retest.

	Square Waveform Period (s)		Response Time: 1,DO,668-1,DI,628 (ms)	
	Single Controller	Redundant Controllers	Single Controller	Redundant Controllers
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
17				
18				
AVG				
STD				

Automated Test Execution

Results of automated digital response time test during in-house test for seismic retest are listed in Table A.7-2. Digital response time from direct measurement averages at 100 ± 30 ms, and thus meets the 100 ms acceptance criteria. The digital response time from

indirect (cascaded) measurements averages at 91 ± 18 ms, which is within the acceptance range. When the system was configured with single controller, response time from direct measurement is approximately the same as that from the cascaded measurement. In contrast, when system is configured with redundant controllers the response time from direct measurement is ~10 ms longer that the result from cascaded measurement. The cause of this difference is because data equalization between redundant controllers consumes time and results in longer equation cycle time.

Table A.7-2. Automated Digital Response Time from Pre-qualification and from In-house Test for Seismic Retest.

Test	Direct Measurement	Cascaded Measurement
	4,DI,9-4,DI,8 (s)	4,DI,3-4,DI,2 (s)
Seismic Retest (In-house Test, Single Controller)		
Seismic Retest (In-house Test, Redundant Controller)		

Figure A.7-1 plots the distribution pattern of the response time measurements during the in-house test for seismic retest with single controller configuration. It is clear that the distribution patterns for direct and cascaded measurements are similar when the system is configured with a single controller: majority of counts (~80%) are distributed into 0.06-0.08 and 0.08-0.10 time bins.

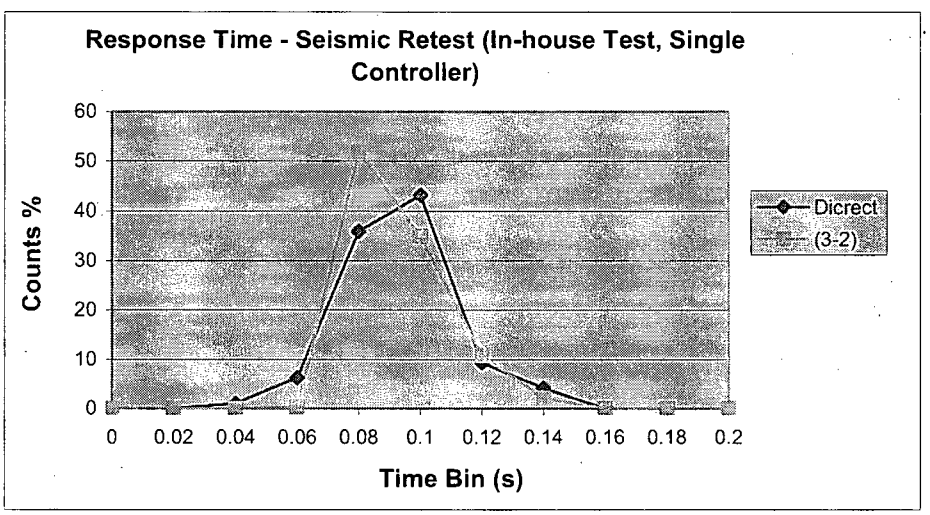


Figure A.7-1. Distribution of Digital Response Time from In-house Test for Seismic Retest With Single Controller Configuration.

Figure A.7-2 plots the distribution pattern with redundant controller configuration. The result is similar to that of the pre-qualification test: the response time from the direct measurement spans a larger timeframe and is also more evenly distributed; whereas the

results from the cascaded tests span over a smaller timeframe and are also much less evenly distributed. For example, in direct response time measurement, the counts % for time bins 60-80 ms, 80-100 ms, 100-120 ms, and 120-140 ms are roughly the same, in contrast to cascaded tests where counts are located at these three time bins: 60-80 ms (~60%), 80-100 ms (~5%), and 100-120 ms (~35%).

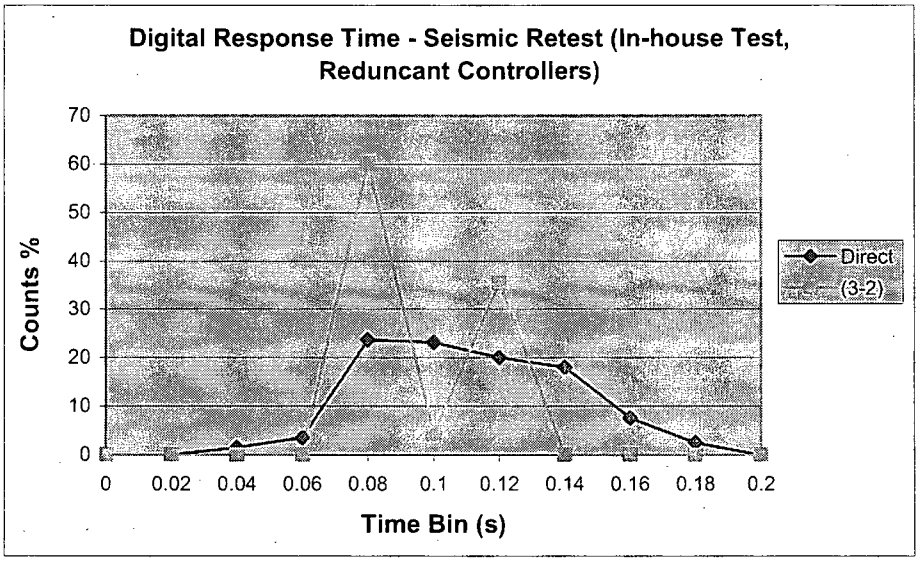


Figure A.7-2. Distribution of Digital Response Time from In-house Test for Seismic Retest With Redundant Controller Configuration.

A.8 TSAP ANALOG RESPONSE TIME TEST

Manual Test Execution

The results from manual measurement of analog response time during the in-house test for seismic retest are listed in Table A.8-1. 1,AI,883 is the analog step signal, and 1,DO,401 is the simulated trip output from 1,AI,883. The leading edge response time averages at 4.145 second and the trailing edge response time averages at 3.303 second.

Table A.8-1. Manual Measurement of Analog Response Time from In-house Test for Seismic Retest.

	1,AI,883 Period (s)	Leading Edge Response Time (s)	Trailing Edge Response Time (s)	1,DO,401 Active Period (s)
1				
2				
3				
4				
5				
6				
7				

	1,AI,883 Period (s)	Leading Edge Response Time (s)	Trailing Edge Response Time (s)	1,DO,401 Active Period (s)
8				
9				
10				
11				
12				
13				
14				
15				
16				
Average				
STD				

Automated Test Execution

The automated analog response time results from in-house test for seismic retest are listed in Table A.8-2 and Table A.8-3. The data were obtained by processing the SOE data of TSAP simulated trip output signal (1,DO,401), which was logged as 4,DI,10. The averaged periods for trip waveform, Set, and Reset with redundant controller configuration are 20.003 s, 10.808 s, and 9.198 s respectively. There is no noticeable difference for automated analog response time measurements when system is configured with single or redundant controller(s).

Table A.8-2. Automated Analog Response Time Test Results from In-house Test for Seismic Retest With Single Controller Configuration.

	Trip Waveform Period (ON)	Trip Waveform Period (OFF)	Set Period (s)	Reset Period (s)
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
AVG				
STD				

Table A.8-3. Automated Analog Response Time Test Results from In-house Test for Seismic Retest with Redundant Controller Configuration.

	Trip Waveform Period (ON)	Trip Waveform Period (OFF)	Set Period (s)	Reset Period (s)
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
AVG				
STD				

In addition to the SOE data as presented above, HAS logger also preserved data related to the analog response time test. More specifically, in the modified HAS configuration table for seismic retest, free running waveform that toggles between 45% and 55% from HPAT was logged as 2,BL,228, the corresponding TSAP AI signal was logged as 1,BL,567, and the trip output from TSAP was logged as 2,DI,161. The analog response time is obtained by taking the time differences from when 2,BL,228 transitions to when 2,DI,161 transitions. The results are listed in Table A.8-4. The data for 1,BL,567 in the table represents the time when the block rose above 50% or fell below 50%. It is clear that the automated analog response time was very consistent throughout the test. Leading edge response time is the same as the trailing edge response time. The 4.0 second response time is comparable to the manual test results in which the leading edge response time was measured as 4.1 seconds and the trailing edge response time was measured as 3.3 seconds.

Table A.8-4. Automated Analog Response Time Test Results from In-house Test for Seismic Retest with Redundant Controller Configuration.

2,BL,228		1,BL,567		2,DI,161		Analog Response	
Time Stamp	Value	Time Stamp	Value	Time Stamp	Value	Leading Edge Response (s)	Trailing Edge Response (s)
12:06:02							
12:06:12							
12:06:22							
12:06:32							
12:06:42							
12:06:52							
12:07:02							
12:07:12							

2,BL,228		1,BL,567		2,DI,161		Analog Response	
Time Stamp	Value	Time Stamp	Value	Time Stamp	Value	Leading Edge Response (s)	Trailing Edge Response (s)
12:07:22							
12:07:32							
12:07:42							
12:07:52							
12:08:02							
12:08:12							
12:08:22							
12:08:32							
12:08:42							
12:08:52							
12:09:02							
12:09:12							
12:09:22							
12:09:32							

A.9 DISCRETE INPUT OPERABILITY TEST

The discrete input operability test results are listed in Table A.9-1. Each channel under the test cycled the input voltage a total of three times. The measurements were taken under ambient temperature.

Table A.9-1. Discrete Input Operability Test Results from In-house Test for Seismic Retest.

Test	Card Type Under Test								
	DI16I			DC34			DC33		
Set Voltage Threshold (V)									
Maximum Input Voltage (V)									
Dropout Voltage (V)									

It is clear from the table that the DI channels under test met all of the acceptable criteria for the set voltage level (20 v at 25 °C), dropout voltage (12-15 v at 25 °C), and the maximum input voltage (53 v at 25 °C).

A.10 DISCRETE OUTPUT OPERABILITY TEST

This test measured operating characteristics of relay output channels, 120-vac output channels, and 125-vdc output channels for conformity with specified limits and tolerances.

A.10.1 Relay Output Operability

One HFC-DO8J relay output module was selected for test, and the contact resistance for each relay channel was measure with an ohmmeter. The observed resistance ranged from 0.60Ω to 0.74Ω. In contrast, the average contact resistances measured during the prequalification execution of the same test was 0.58Ω, indicating a degree of deterioration caused by cumulative operating cycles. Four test channels were loaded with a current in excess of 9.4 A at 120 vac and then switched under load. Each test channel successfully opened without indication of arcing.

Acceptance criteria for relay channels are that the relay will operate successfully for a resistive load with a current level of 5 A at 30 v. Each channel tested met the acceptance criteria. Observed parameters for the relay channels remained essentially unchanged from those measured during the prequalification test, except that the average contact resistance had increased by 0.07 ohm.

A11.2 120 vac Output Operability

The test was executed on two output channels of a selected HFC-DC33 module. The specified acceptance criteria for such channels are as follows:

- Functional range is 90.0 ± 0.5 vac at 47 Hz up to 130.0 ± 0.5 vac at 63 Hz
- 2 A minimum in-rush capacity
- Up to 0.5 A steady-state current capacity
- 2 vac maximum on-state voltage drop at 0.5 A
- Supports off-state continuity monitoring for the external relay coil

The test was conducted by supplying ac power to the module under test via a variable power supply and then enabling/disabling the output channel. During each transition, the power source signal and the output voltage of the channel under test were captured on an oscilloscope, and the relevant measurements were taken from the oscilloscope screen captures. Table A.10-1 summarizes the test results obtained for this module.

The module continues to perform within all acceptance criteria, except the on-state voltage drop appears to exceed the 2.0 v limit based on the data provided by the oscilloscope screen captures. These values are deceptive, because the oscilloscope produced averaged rms values over the entire range of the sample, and the amplitude of the DO channel switched during that period. Measurements taken directly from the screen are less precise, but they indicate that the voltage drop through the module remained within limits.

Table A.10-1. 120 Vac Output Channel Parameters.

Parameter	Set Coil Circuit	Reset Coil Circuit
Coil Resistance		
Supply voltage set to 90.0 ± 0.5 vac at 47 Hz		
Peak off-on response voltage		
Peak in-rush current		
Steady-State output (rms)		
On state voltage drop		
Peak reverse EMF		
Off state leakage		
Supply voltage set to 130.0 ± 0.5 vac at 47 Hz		
Peak off-on response voltage		
Peak in-rush current		
Steady-State output (rms)		
On state voltage drop		
Peak reverse EMF		
Off state leakage		

The acceptance criteria for in-rush current and steady-state current load are 2.0 A and 0.5 A, respectively. One measurement for peak in-rush current was 2.33 A, and one value for steady-state current was 1.62 A, indicating that the module can support the minimum current levels. The solid state relay is rated for a steady-state current of up to 10 A and a peak surge current of more than 60 A. The relay DO test demonstrated that the interface cable can support a steady-state current in excess of 9 ADC, as the system can support the minimum current level specified.

The coil monitoring circuit supplies a leakage current of between 2% and 4% of the amount required to energize the relay. The EPRI specification requires that leakage be less than 2 mA or less than 80% of the minimum current needed to energize the attached relay. The latter limit is maintained by the coil continuity circuit.

A.10.3 125 vdc Output Operability

The test was executed on two output channels of a selected HFC-DC34 module. The specified acceptance criteria for such channels are as follows:

- Functional range is 90.0 ± 0.5 vdc to 140.0 ± 0.5 vdc
- 2 A minimum in-rush capacity
- Up to 0.5 A steady-state current capacity
- 2 vdc maximum on-state voltage drop at 0.5 A
- Supports off-state continuity monitoring for the external relay coil,

This test was conducted in the same manner as the 120-vac test using a variable dc power source. Table A.10-2 summarizes the results obtained for the 125-vdc output channels.

Table A.10-2. 125 Vdc Output Channel Parameters.

Parameter	Set Coil Circuit	Reset Coil Circuit
Coil Resistance		
Supply voltage set to 90.0 ± 0.5 vdc		
Peak off-on response voltage		
Peak in-rush current		
Steady-State output		
On state voltage drop		
Peak reverse EMF		
Off state leakage		
Supply voltage set to 140.0 ± 0.5 vdc		
Peak off-on response voltage		
Peak in-rush current		
Steady-State output		
On state voltage drop		
Peak reverse EMF		
Off state leakage		

The characteristics observed correspond to those obtained during the original baseline test. The acceptance criteria stipulate that the module be capable of supporting an in-rush current up to 2 A and a steady state current of up to 0.5 A as a minimum. The maximum current level observed during the test was 308 mA (890 ma for reverse EMF) due to the characteristics of the attached relay. The control circuit for this module is rated for 11 A at 25 °C with a derating down to 6.8 A at 100 °C. In addition, the interface circuitry has been shown to support current levels above 9 ADC by the relay DO test.

Requirements and characteristics for the coil monitoring circuit of the 125-vdc channels are identical to those for the 120-vac output channels.

HFC concludes that these modules satisfactorily meet the functional requirements for these DO channel types.

A.11 COMMUNICATION OPERABILITY TEST

The Communication Operability Test was run for about 5 minutes on 9/7/04.

- **ICL Error Counters**

Screen captures were taken for ICL error counters at the start and at the end of the test. None of the cards in the Test Specimen showed errors.

Table A.11-1. ICL Error Counters During Communication Test of In-house Test for Seismic Retest.

Station	Card Type	Start Count	End Count	Count Diff	Start Time	Stop Time	Duration	Comments
Remote 1							*d-h-m-s*	
0	KPD16							
1	KPD16							
3	KPD16							
5	KDI16							
6	KDO8							
7	KDO8							
16	KDI16							
17	KPD16							
19	KDI16							
20	KPD16							
22	KDI16							
23	KDO8							
24	KDO8							
25	KDI16							
26	KPD16							
36	KDI16							
37	KDI16							
38	KDO8							
39	KDO8							
40	KDO8							
48	KAIO							
49	KAO8							
50	KAIO							
51	KAIO							
52	KAI16							
53	KAI16							
54	KAO8							
56	KAI8							
57	KAIO							
58	KAI8							
59	KAI8							
60	KAI8							

A.12 TIMER TEST

A.12.1 Manual Timer Test

Table A.12-1 lists the period measurements for free running waveforms 4,DI,11 (1 second on timer + 1 second off timer) and 4,DI,12 (5 second on timer + 1 second off wave timer) from manual timer test. ABS stands for absolute. The results show that 4,DI,12 had a larger absolute deviation than 4,DI,12: 31.8 ms vs. 17.8 ms. Nonetheless, the averaged period deviations for both waveforms are less than 1%, and within the

theoretical characteristics of the timer function as described in the baseline report (TS901-000-22).

Table A.12-1. Manual Timer Test Result for Combined Timers from In-house Test for Seismic Retest.

	4,DI,11 (1 s On 1 s Off)			4,DI,12 (5 s On 1 s Off)		
Measurement	Period (s)	ABS Deviation (ms)	ABS Deviation (%)	Period (s)	ABS Deviation (ms)	ABS Deviation (%)
1						
2						
3						
4						
5						
Average						

Measurements on the durations of 1 second timer (ON) for 4,DI,11, and 5 second timer (ON) for 4,DI,12 were also performed and the results are listed in Table A.13-2. It is clear that 1 second timer and 5 second timer have similar absolute deviations and jitters: 23.2 ms vs. 27.2 ms for deviation and 42.2 ms vs. 47.3 ms for jitter. On the other hand, the jitter% for 1 second timer is about 5 times larger than that of 5 second timer: 5.0% vs. 0.95%. The difference is caused by the smaller duration of 1 second timer.

Table A.12-2. Manual Timer Test Results for Individual Timers from In-house Test for Seismic Retest.

	1 s Timer (ON)				5 s Timer (ON)			
Measurement	Duration (s)	ABS Deviation (ms)	ABS Jitter (ms)	ABS Jitter (%)	Duration (s)	ABS Deviation (ms)	ABS Jitter (ms)	ABS Jitter (%)
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								
13								
14								
15								

	1 s Timer (ON)				5 s Timer (ON)			
Measurement	Duration (s)	ABS Deviation (ms)	ABS Jitter (ms)	ABS Jitter (%)	Duration (s)	ABS Deviation (ms)	ABS Jitter (ms)	ABS Jitter (%)
16								
17								
18								
19								
Average								

A.12.2 Automated Timer Test

The results from automated timer test during the in-house test for seismic retest are listed in Table A.12-3. The number listed in the table is the average results of 28-29 measurements for the 4,DI,12 and 51-53 measurements for the 4,DI,11. The data would serve as the baseline for the evaluation of timer performance during the Wyle seismic retest.

Table A.12-3. Automatic Timer Test Result from In-house Test for Seismic Retest.

		Preset Value (s)	Duration (s)	Duration Deviation (%)	Duration Jitter (%)	Period (s)	Period Deviation (%)	Period Jitter (%)
4,DI,12	ON	5						
	Number of Measurement							
	OFF	1						
	Number of Measurement							
4,DI,11	ON	1						
	Number of Measurement							
	OFF	1						
	Number of Measurement							

A.13 FAILOVER OPERABILITY TEST

Figure A.13-1 is the screen capture from the failover test when switching off the power of controller A (controller A was running as the primary). A delay of 56 ms is recorded from High-to-Low transition for signal PRI _B/ to Low-to-High transition for signal SANE_A/. Similarly, Figure A.13-2 is the screen capture from the failover test when switching off the power of controller B (controller B was running as the primary). A delay of 39.2 ms is recorded from High-to-Low transition for signal PRI _A/ to Low-to-

High transition for signal SANE_B/. The difference in the time delay is due to the fact that the power cycle was not synchronized with internal operations of the controller. The controller that was primary disabled its PRI/ signal as soon as power dropped below the low level limit of its onboard power monitor, causing the secondary to take over as

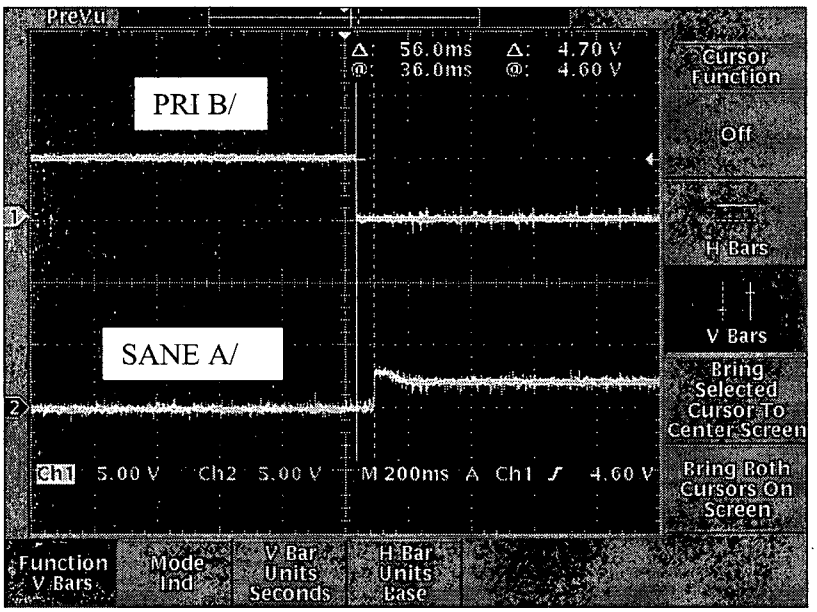


Figure A.13-1. Failover When Controller A Was Primary from In-house Test for Seismic Retest.

primary. However, the SANE/ signal of the former primary remained active until power dropped out entirely. Because processing of PRI status occurs at a single point during the processing cycle, the relative duration between the transitions will vary, depending on when the power level drops.

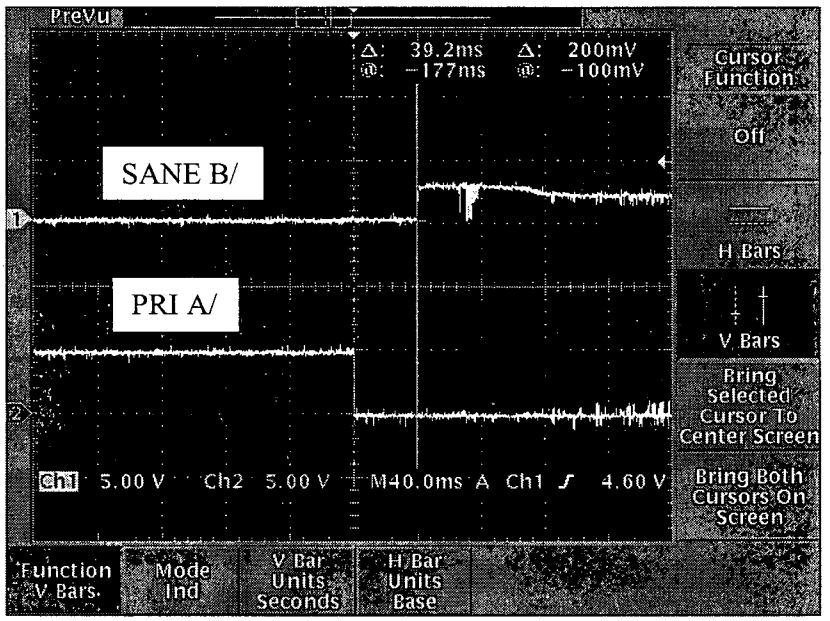


Figure A.13-2. Failover When Controller B Was Primary from In-house Test for Seismic Retest.

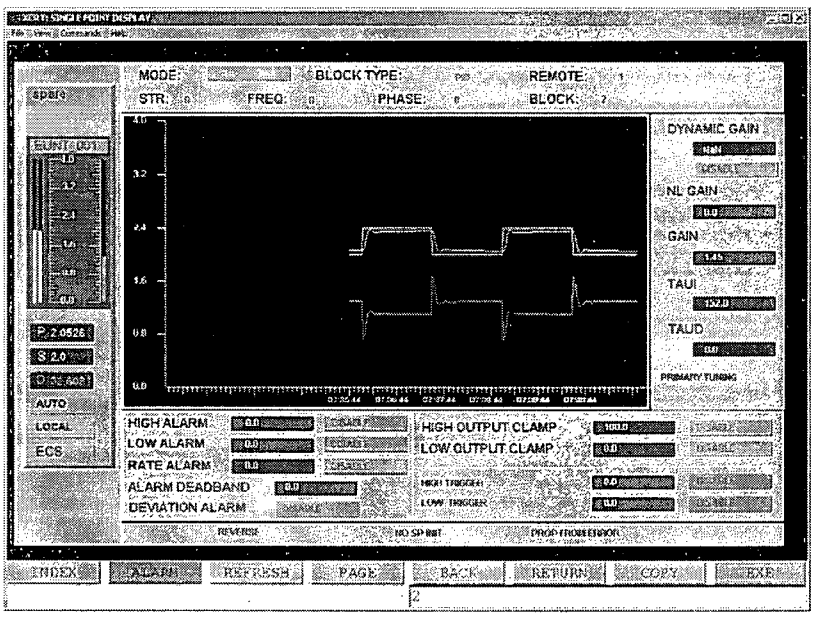


Figure A.13-3. Effect of Maintenance Failover on Analog Control Loop from In-house Test for Seismic Retest.

Figure A.13-3 shows the effect of maintenance failover (MF) on the analog control loops. The first two transitions had no failover and the last two transitions included failover. It is clear that no disruption occurred to analog output signal during the failover process. Figure A.13-4 shows the effect of maintenance failover on the digital control loops. The maintenance failover was initiated after triggering the slow close process. The duration

from the Low-to-High change of signal 1,DI,30 to the High-to-Low change of signal 1,DI,21 was measured as 5.00 second, which demonstrates that maintenance failover has no effect on the operation of digital control loop.

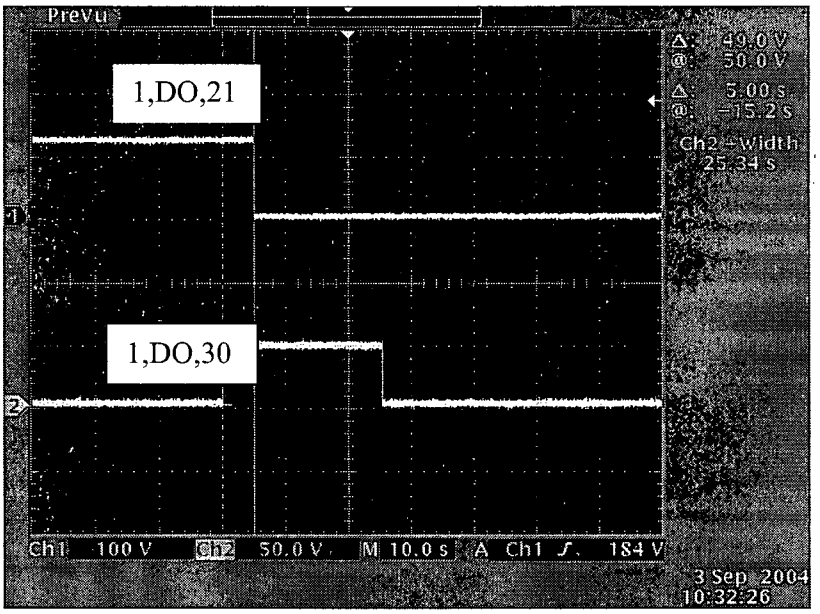
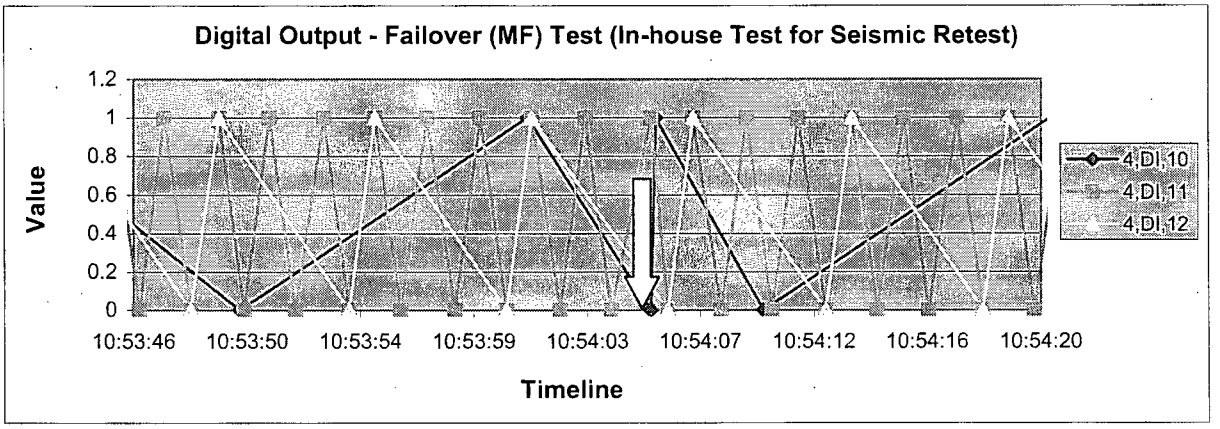


Figure A.13-4. Effect of Maintenance Failover on Digital Control Loop from In-house Test for Seismic Retest.

Figure A.13-5 illustrates transitions of DO data during the maintenance failover: arrows mark the moment when MF was introduced. No invalid transition was detected during the entire failover process. This had been validated by inspecting the SOE and HAS reports from failover test and no state transitions for static points were recorded throughout the failover test period. The representative state transition time for the DO points before, during and after failover is listed in Table A.13-1. Longer transitions period is observed during the failover process except 4,DI,10. A shorter transition time followed the failover for 4,DI,9, 4,DI,11. On the other hand, transition time recovered to the pre failover level for 4,DI,2, 4,DI,3, 4,DI,10, and 4,DI,12 after the failover. 4,DI,8 was not impacted by the failover because it was an output from HPAT.



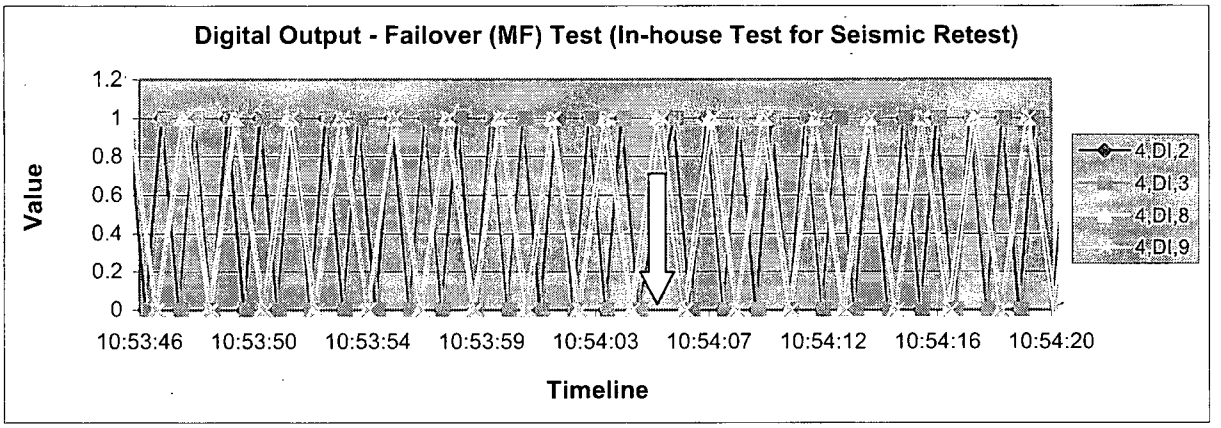


Figure A.13-5. Transition of Digital Points During Maintenance Failover.

Table A.13-1. DO State Transition Time Before, During, and After Maintenance Failover.

	4,DI,2	4,DI,3	4,DI,8	4,DI,9	4,DI,10	4,DI,11	4,DI,12
Before FO							
During FO							
After FO							

A.14 LOSS OF POWER TEST

Figures A.14-1, A.14-2 illustrate the response of the analog output signals during the loss of power test of in-house test. 1,BL,40 (1,AO,981) is a static signal from the TA05 level controller, 1,BL,504 (1,AO,841) is a static signal from the TA05 flow controller, and 2,BL,203 (1,AO,983) is a uncontrolled spare RTD point. It can be seen that for both dynamic and static analog outputs, the signals remained at their power-off state (0%) until the operation restarted. In this test, no failsafe state was detected by HAS logger for

neither 2,BL,211 or 2,BL,215. The transient nature of failsafe state was discussed in Section A.14 of Baseline Report (TS901-000-22).

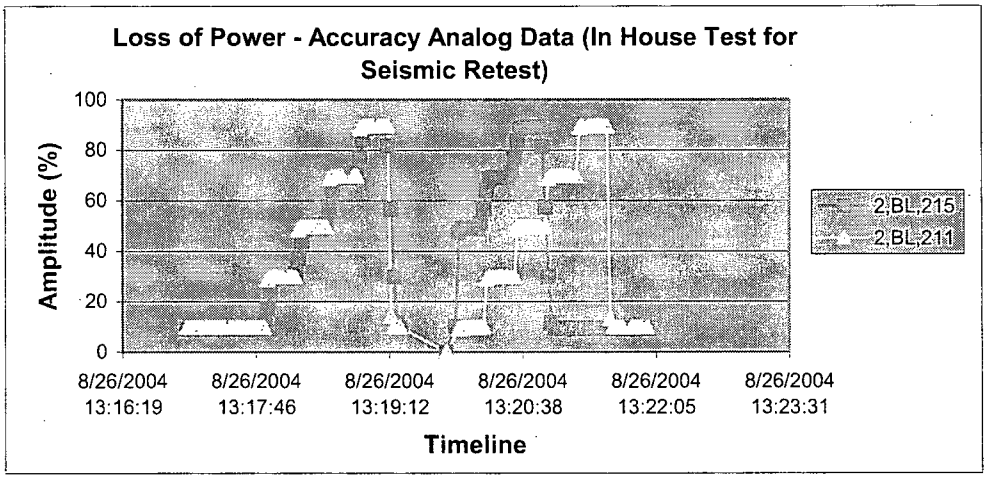


Figure A.14-1. Analog Data During Loss of Power Test from In-house Test for Seismic Retest.

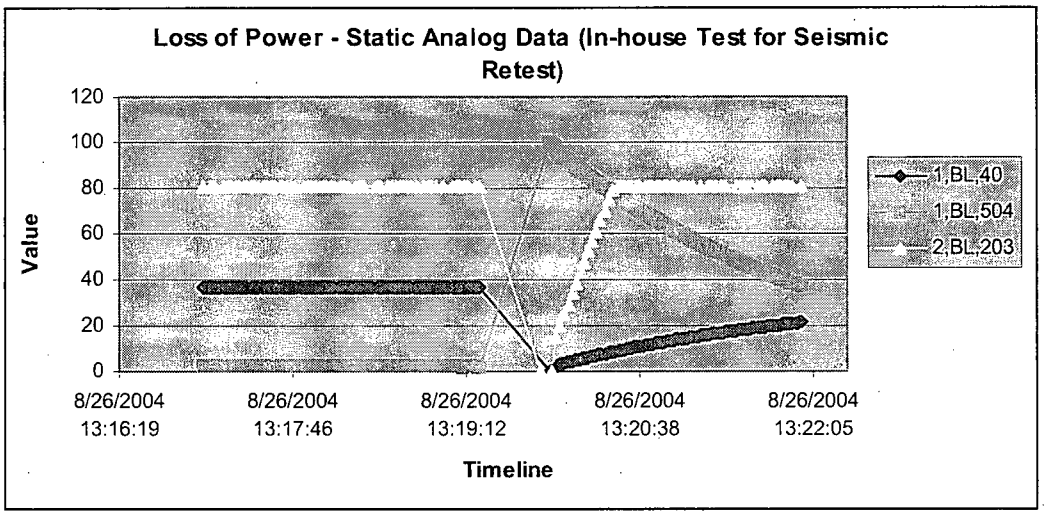


Figure A.14-2. Static Analog Data During Loss of Power Test from In-house Test for Seismic Retest.

Figure A.14-3 illustrates the effect of power loss on the digital points as logged by the SOE. During power loss period, digital points from TSAP (4,DI,2, 4,DI,3, 4,DI,9, 4,DI,10, 4,DI,11, and 4,DI,12) transitioned to their deenergized state of 0 (false) as expected, and no further transition was logged until power was restored. The reason why 4,DI,8 (HPAT output for digital response time test) was not logged is because the excitation power for this signal came from the TSAP. As a result, when power was cut off from the TSAP, the power for this signal was also cut off. It came back earlier than the other points because the relay channel controlling this signal resides in the HPAT,

therefore no TSAP scanning was required. After the power was restored, the log of all digital data resumed with the next point transition to 1 (true), because SOE logger records only changes in state. As shown in the figure, 4,DI,8 resumed activity several cycles earlier than the rest of SOE logged digital points.

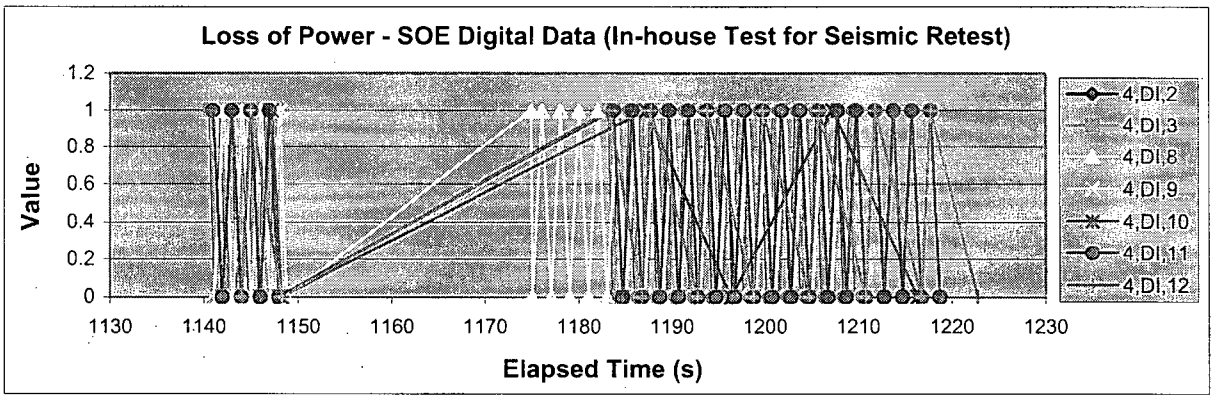


Figure A.14-3. Digital Data from SOE Logger During Loss of Power Test of In-house Test for Seismic Retest.

Figure A.14-4 illustrates the effect of power loss on the digital points as logged by HAS logger. 2,DI,161 (1,DO,401) is the trip output signal from analog response time test and 2,DI,155 (1,DO,647) is the uncontrolled TSAP logic. Due to the loss of C-Link after power was cut, HAS logger could not record the transition to the deenergized state of "0". However, the HAS data did show that on return of the power the initial state of these two points were at "0" as expected.

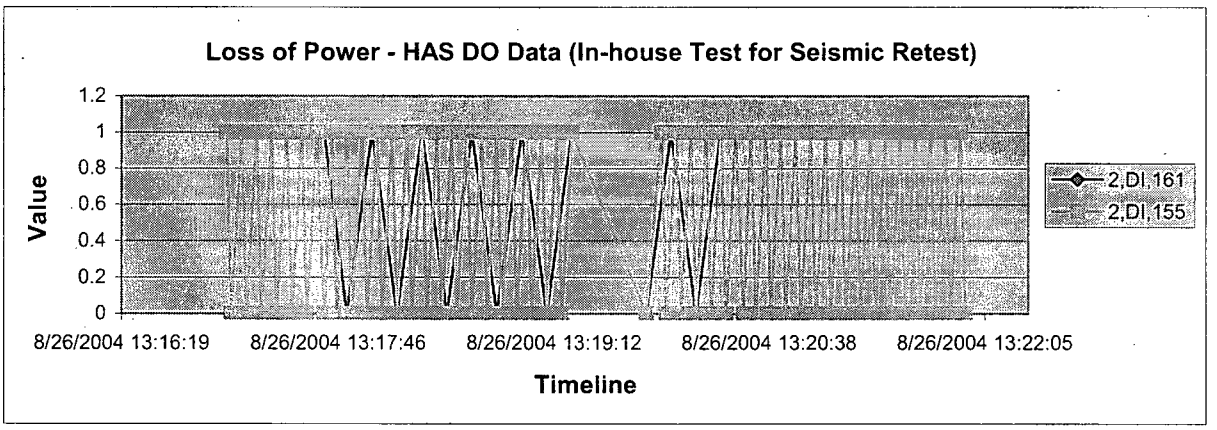


Figure A.14-4. Digital Data from HAS Logger During Loss of Power Test of In-house Test for Seismic Retest.

A.15 POWER INTERRUPTION TEST

Selective analog accuracy test signals and static analog points throughout the entire power interruption test were plotted in Figures A.15-1, A.15-2, and A.15-3. The first, third and fourth of the four disruptions shown in these figures corresponds to one power interruption test. There were no background tests running during the first power interruption. The second disruption at around 14:11:28 PM seemed to be a C-Link disruption, as demonstrated by the loss of DDB data for 1,Bl,506 and RTD cards, as well as spotty DDB for 2,BL,211. After the second power interruption test, a disruption for digital points appeared at around 14:18:27 as shown in Figure A.15-4. Analog accuracy test seemed to stop running after this disruption (Refer to 1,BL,506 and 2,BL,211 in Figure A.15-1) . In contrast, the digital responses continued to run after the disruption. Analog accuracy returned after the third power interruption test.

Figure A.15-4 demonstrates that the static points during the power interruption test did not meet the acceptance criteria which specifies a maximum 5% output drift for the static AO channels. Each time when power interruption was introduced, 1,BL,1 (simulated process valve) jumped to value 4 then slowly drifted back to its static value of 1.

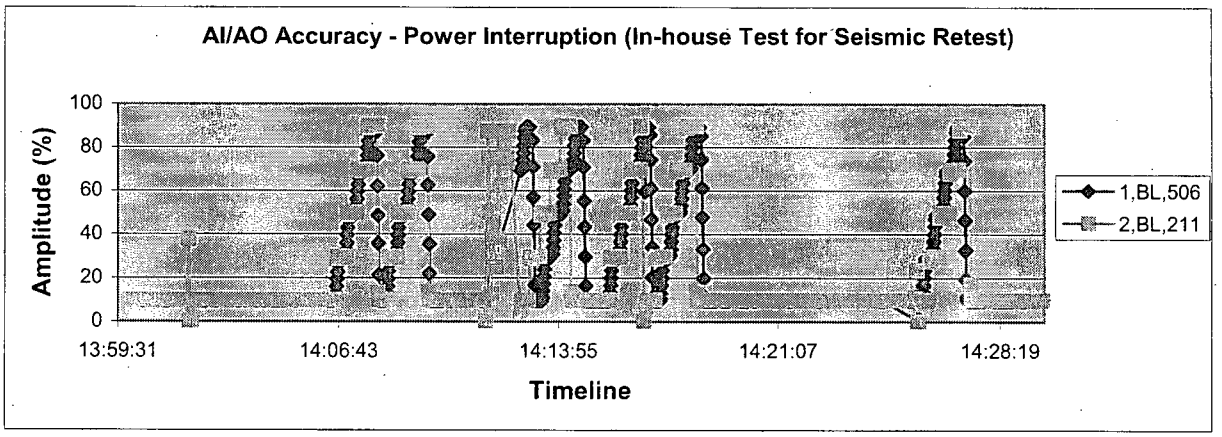


Figure A.15-1. AI/AO Signals During Power Interruption Test of In-house Test for Seismic Retest.

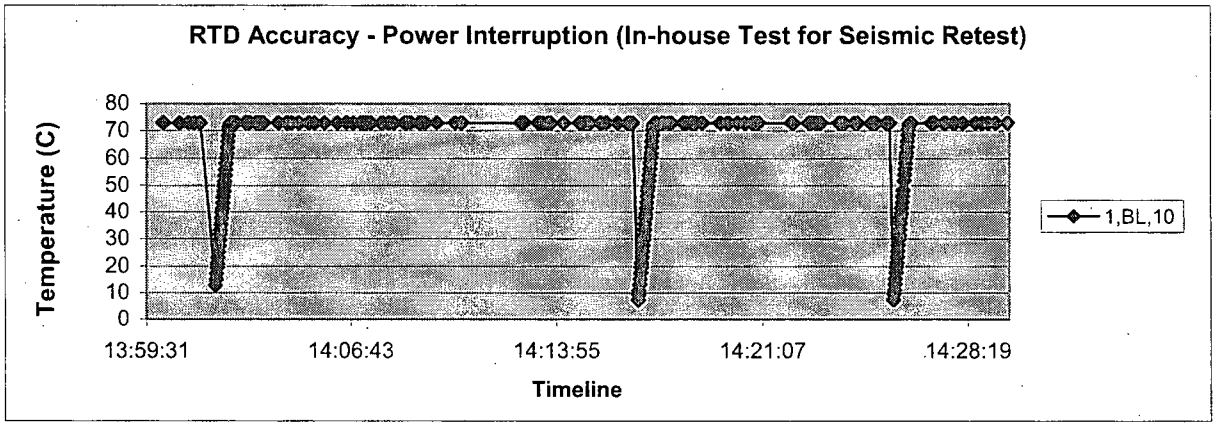


Figure A.15-2. RTD Signal During Power Interruption Test of In-house Test for Seismic Retest.

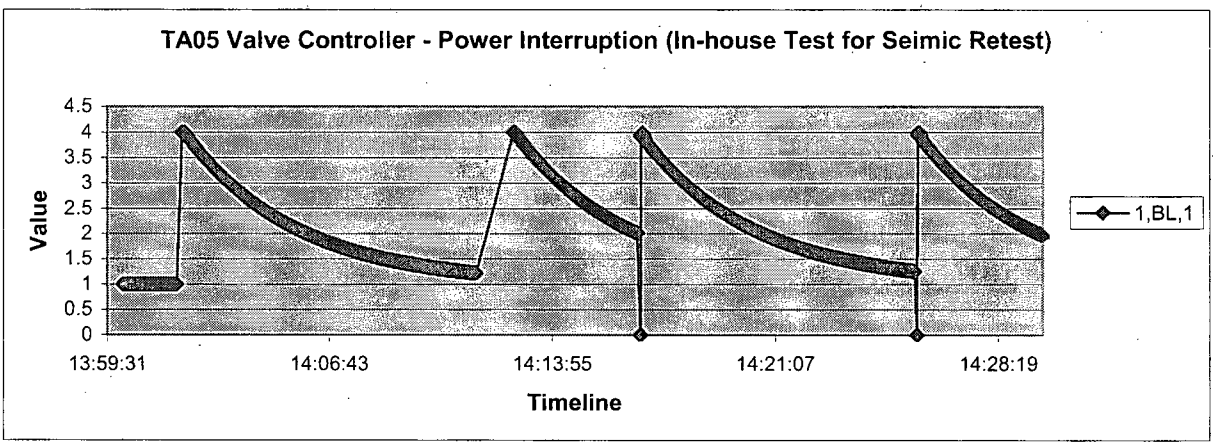


Figure A.15-3. Static Point During Power Interruption Test of In-house Test for Seismic Retest.

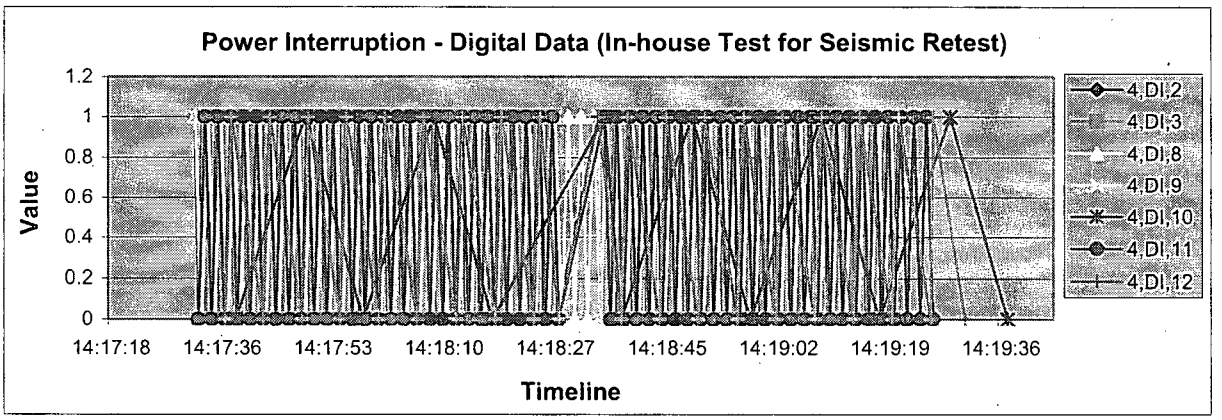


Figure A.15-4. Digital Data During Power Interruption Test of In-house Test for Seismic Retest.

A.16 POWER QUALITY TOLERANCE TEST

The power quality tolerance test results during in-house test for seismic retest are listed in Table A.16.1. The two power modules A and B from TSAP meet the ±1% acceptance criteria at both the low voltage and high voltage tests. At low voltage test, both TSAP and SLC dropped out at 66.4 Vac, and the power supply recovered from the undervoltage condition automatically. However, since the undervoltage condition brought down the entire system, no system status alarm was logged after the power trip. At high voltage test, no system trip was observed up to the limit of the power source: 275 Vac. Lastly, by inspecting the HAS data for power supply alarm flags, it is concluded that no power supply dropout alarm occurred while source power was within the specified range (90-150 Vac and 57-63 Hz).

Table A.16.1. TSAP and SLC Power Quality Tolerance Test Results from In-house Test for Seismic Retest.

Power Feed	Power Module A				Power Module B				Single-Loop Module			
	24-vdc	Deviation (%)	48 vdc	Deviation (%)	24 vdc	Deviation (%)	48 vdc	Deviation (%)	24 vdc	Deviation (%)	48 vdc	Deviation (%)
120 vac 60 Hz												
90 vac 57 Hz												
90 vac 63 Hz												
90 vac 63 Hz												
< 60 vac												
120 vac 60 Hz												
150 vac 57 Hz												
150 vac 63 Hz												
150 vac 63 Hz												
> 270 vac												
120 vac 60 Hz												

Figures A.16-1 and A.16-2 demonstrates the analog responses throughout the low voltage test. Notice a system dropout occurred at around 9:36:51 AM and the automatic system recovery at around 9:38:14 AM. Also notice that in Figure A.16-1, TSAP AO outputs 2,BL,211 and 2,BL,215 had a spike before settling down when system recovered from the power trip. Figure A.16-3 shows the digital response throughout the low voltage test. As expected, all TSAP digital outputs (4,DI,2, 4,DI,3, 4,DI,9, 4,DI,10, 4,DI,11, and 4,DI,12) went down to zero when power trip occurred. However, similar to what happened during the loss of power test, 4,DI,8, the free running waveform from HPAT for digital response time test, showed similar disruption although it dropped to zero later but recovered earlier than the TSAP DO points.

Figures A.16-3 and A.16-4 demonstrates the analog responses throughout the high voltage test. Notice that there is no system disruption during the entire test period.

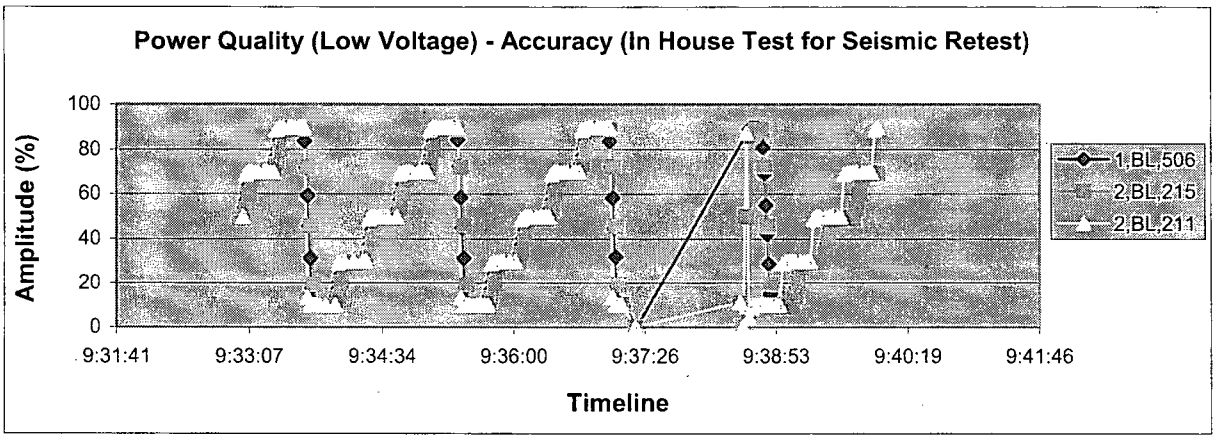


Figure A.16-1. Analog Data During Low Voltage Power Quality Tolerance Test of In-house Test for Seismic Retest.

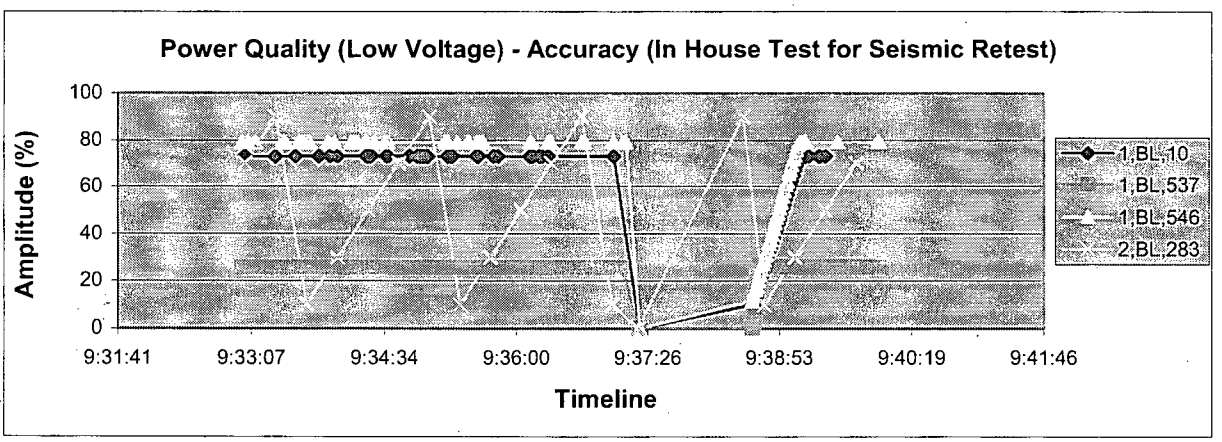


Figure A.16-2. Analog Data During Low Voltage Power Quality Tolerance Test of In-house Test for Seismic Retest.

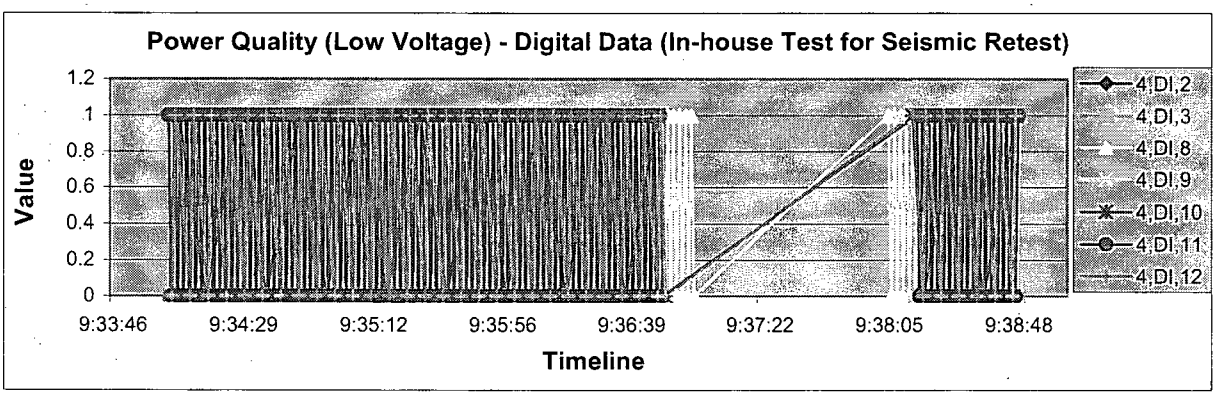


Figure A.16-3. Digital Data During Low Voltage Power Quality Tolerance Test of In-house Test for Seismic Retest.

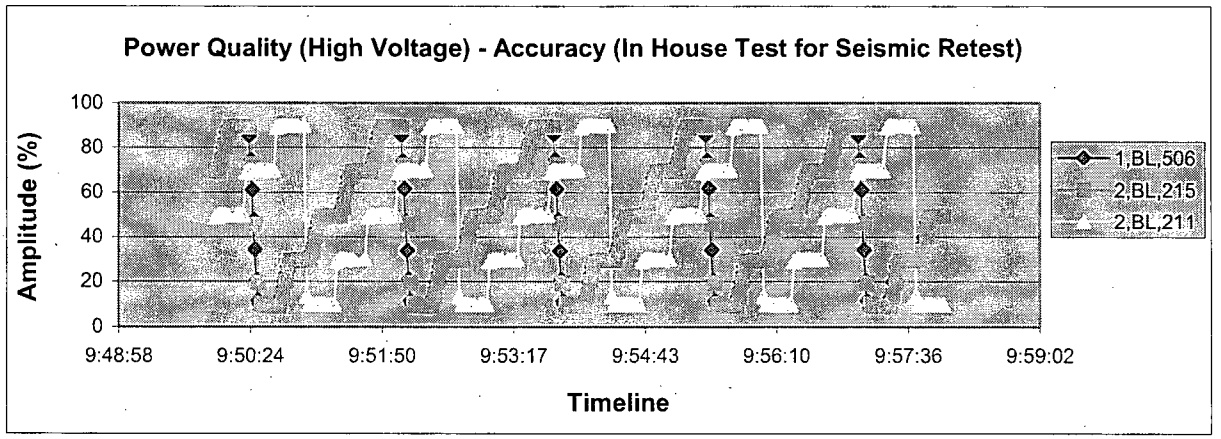


Figure A.16-4. Analog Data During High Voltage Power Quality Tolerance Test of In-house Test for Seismic Retest.

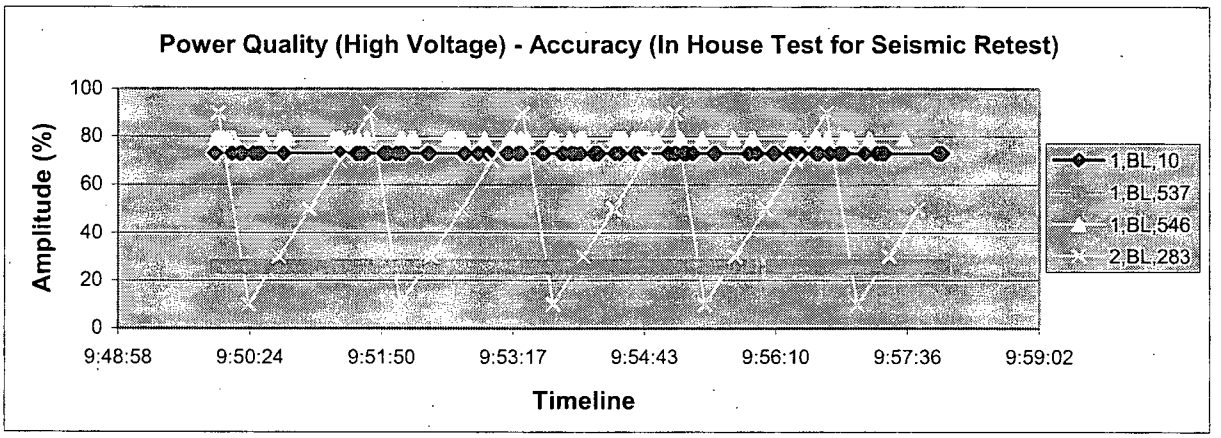


Figure A.16-5. Analog Data During High Voltage Power Quality Tolerance Test of In-house Test for Seismic Retest.

HFC-6000 Control System

ERD111 – Control System Qualification Project

Seismic Retest In-House Testing Summary Report
(Update of Pre-Qualification Prudency Tests)

TS901-000-34

Revision B

APPENDIX B

PRUDENCY TESTS

B.1 GENERAL

The purpose of this attachment is to document the results of the Post Qualification Prudency Tests in Section 4.1 of the Prudency Test Procedure TP0403, Rev. C.

B.2 DIGITAL INPUT/OUTPUT BOE TEST

The points logged during the digital BOE test were 4,DI,28, 4,DI,32, 4,DI,33, 4,DI,34, 4,DI,35. SOE data demonstrated that all digital transitions occurred with 0.85-1.15 s.

B.3 ANALOG BOE TEST

The waveforms of TSAP analog inputs at remote 1 and that of the BOE source signal during the in-house test of seismic retest are depicted in Figure B.3-1. It is clear from the figure that the TSAP AI signals correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table B.3-1 lists the averaged readings and deviations of 15 measurements for these HAS logged AI signals at 10% and 90% levels.

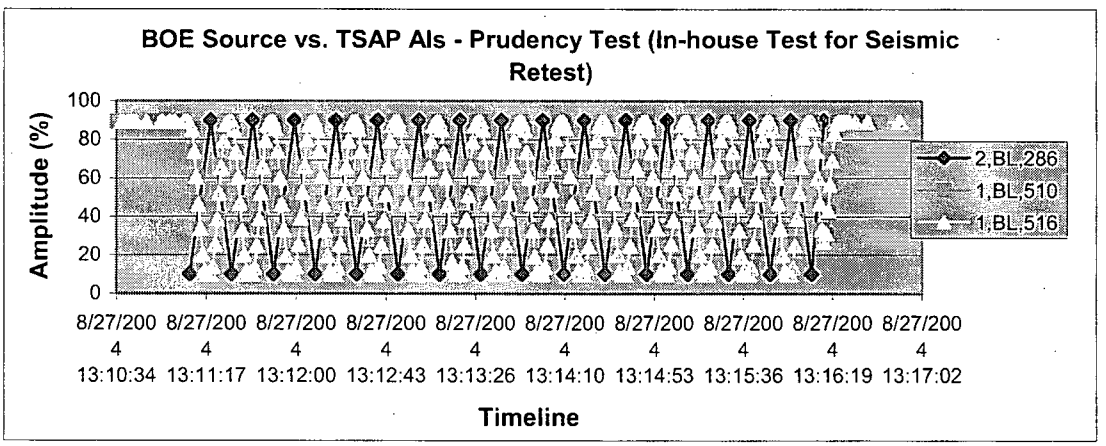


Figure B.3-1. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from In-house Test for Seismic Retest.

Table B.3-1. TSAP AI Channel Readings and Deviations from BOE Source Signal from In-house Test for Seismic Retest.

	1,AI,882 (1,BL,510)		1,AI,901 (1,BL,516)	
	With Correction	No Correction	With Correction	No Correction
10% Measurement (%)				
Deviation From 10% (%)				
Num of Measurements				
90% Measurement (%)				
Deviation From 90% (%)				
Num of Measurements				

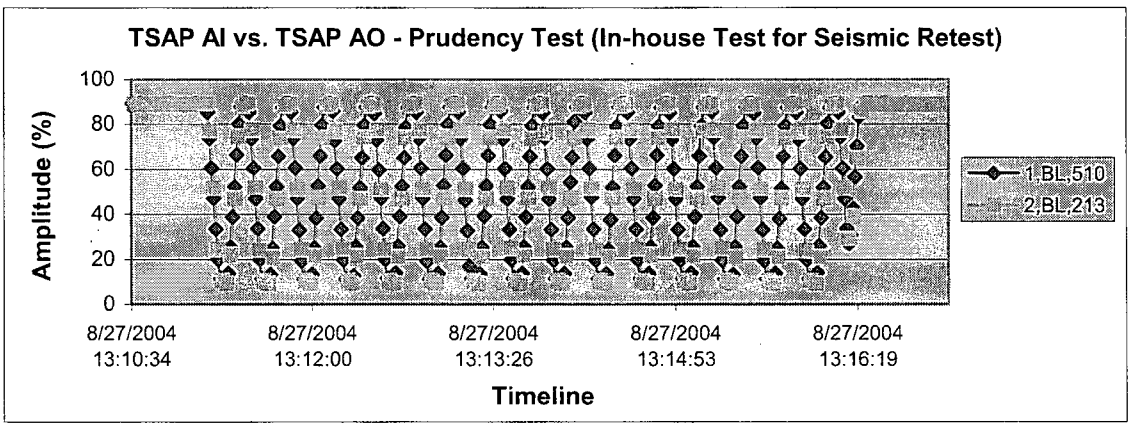


Figure B.3-2. TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) from In-house Test for Seismic Retest.

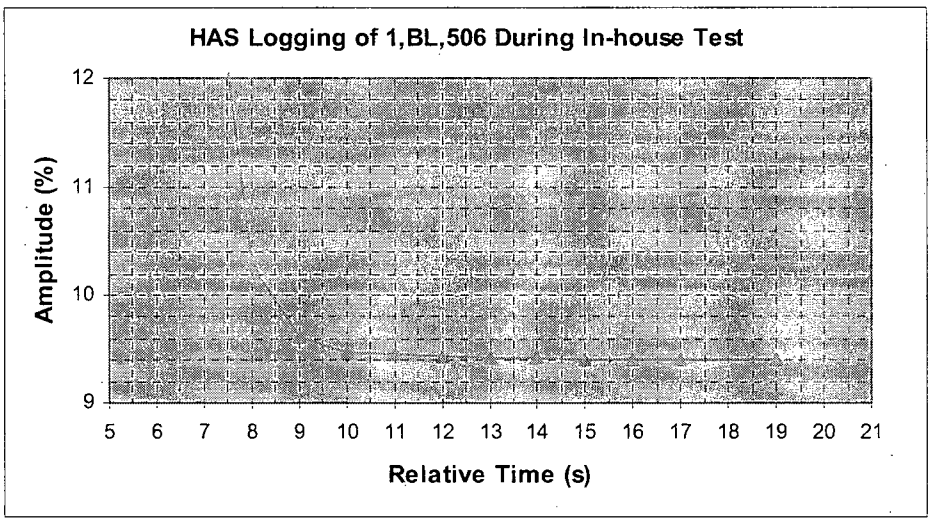


Figure B.3-3. Analog Input Signal of 1,BL,506 During the In-house Accuracy Operability Test.

Table B.3-2. TSAP AOs and the Corresponding TSAP AIs in Remote1 from In-house Test for Seismic Retest.

	1,AI,882 (1,BL,510)		1,AO,922 (2,BL,213)	Deviation (1,BL,213 vs. 1,BL,510)	
	With Correction	No Correction		With Correction	No Correction
10% Measurement (%)	9.689 ± 0.005	9.995 ± 0.020	9.575 ± 0.011	0.115 ± 0.008	0.421 ± 0.017

	1,AI,882 (1,BL,510)		1,AO,922 (2,BL,213)	Deviation (1,BL,213 vs. 1,BL,510)	
	With Correction	No Correction		With Correction	No Correction
Number of Measurements	15	15	15	15	15
90% Measurement (%)	89.261 ± 0.003	89.261 ± 0.003	88.934 ± 0.008	0.327 ± 0.006	0.327 ± 0.006
Number of Measurements	15	15	15	15	15

B.4 SERIAL PORT FAILURE TESTS

B.4.1 ICL Failure Test

Abnormal transitions and the corresponding timestamps for logged digital channels during the ICL failure test are listed in Table B.4-1. No abnormal transitions were detected with normal breakout cable and with pin1 of TX shorting one RX line. The abnormal transitions occurred during other stages of the C-Link failure test all appeared at the end of respective test. They were caused by the perturbation from stopping the BOE test. All other transitions occurred within 0.85-1.15 s.

Table B.4-1. Digital BOE Abnormal Transitions from ICL Failure Test of In-house Test for Seismic Retest.

	4,DI,28		4,DI,32		4,DI,33		4,DI,34		4,DI,35	
	Time Stamp	Transition (s)	Time Stamp	Transition (s)	Time Stamp	Transition (s)	Time Stamp	Transition (s)	Time Stamp	Transition (s)
Breakout Normal										
TX Pin Float										
Short Ground										
Short RX Pin										
Regular Cable										

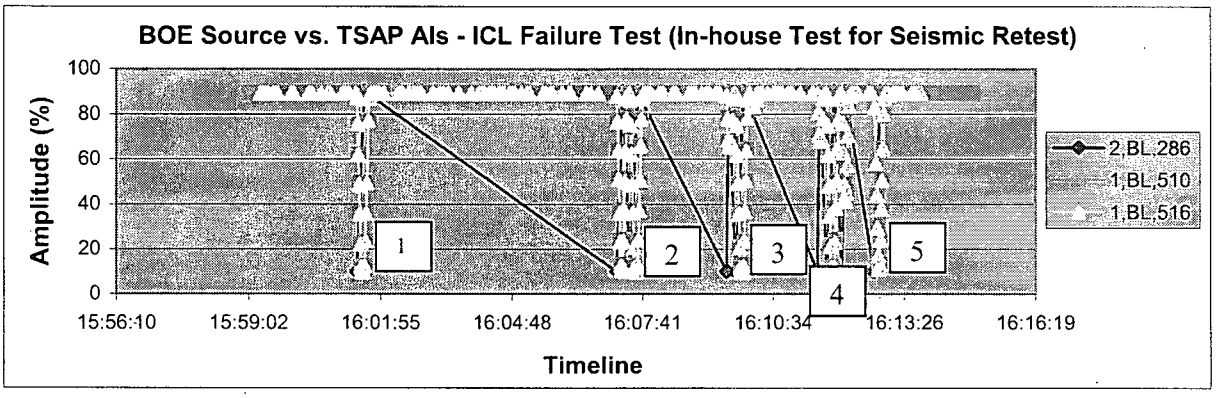


Figure B.4-1. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 During ICL Failure Test of In-house Test for Seismic Retest.

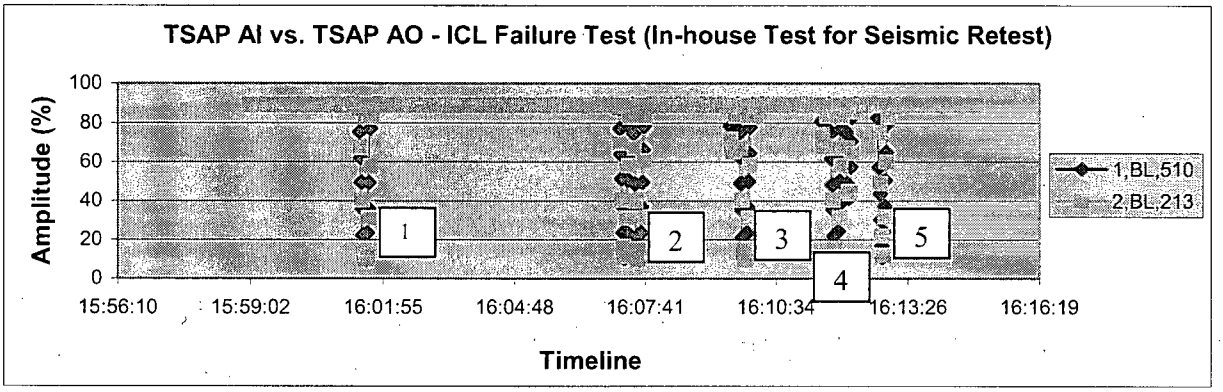


Figure B.4-2. TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) During ICL Failure Test of In-house Test for Seismic Retest.

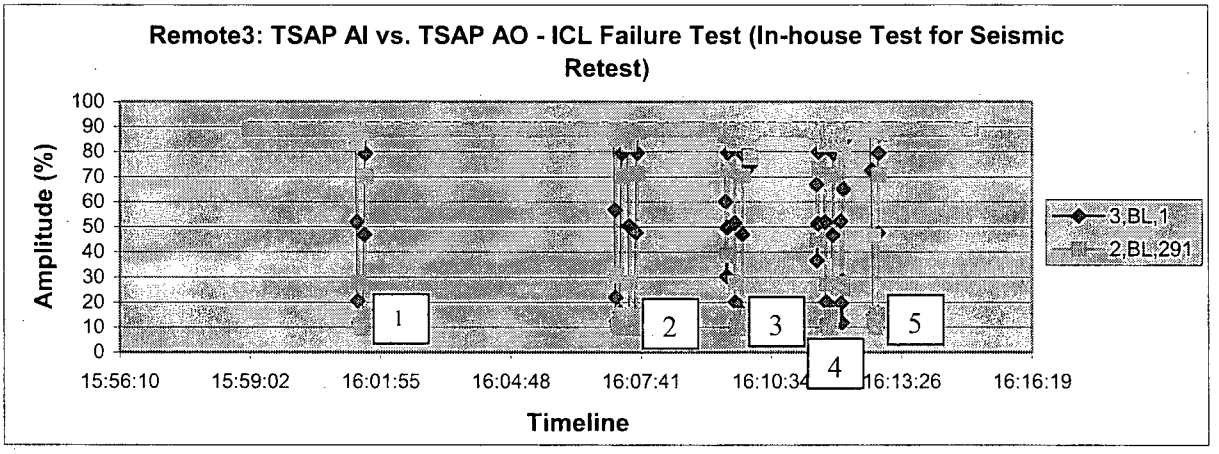


Figure B.4-3. Single Loop Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO During ICL Failure Test of In-house Test for Seismic Retest.

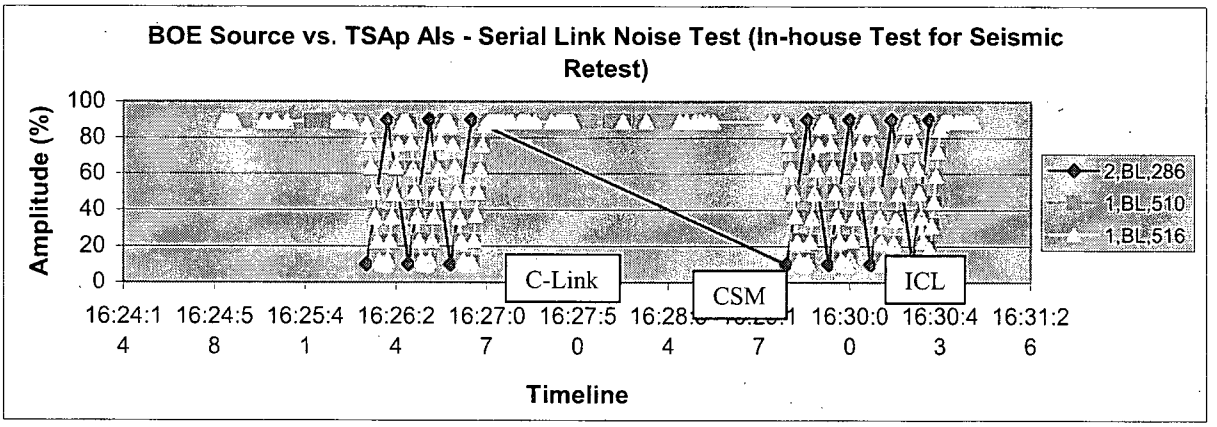
B.5 SERIAL LINK NOISE TEST

Serial link noise test was performed on 9/3/2004 from 2:26 PM to 4:31 PM.

Table B.5-1. Digital BOE Abnormal Transitions from Serial Link Noise Test of In-house Test for Seismic Retest.

	4,DI,28		4,DI,32		4,DI,33		4,DI,34		4,DI,35	
	Time Stamp	Transition (s)	Time Stamp	Transition (s)	Time Stamp	Transition (s)	Time Stamp	Transition (s)	Time Stamp	Transition (s)
C-Link Noise										
ICL Noise										
CSM Link Noise										

Analog BOE test results during the serial link noise test are demonstrated in Figures B.5-1, B.5-2, and B.5-3. It is apparent from the figures that there are no apparent disruptions throughout the entire serial link noise test.



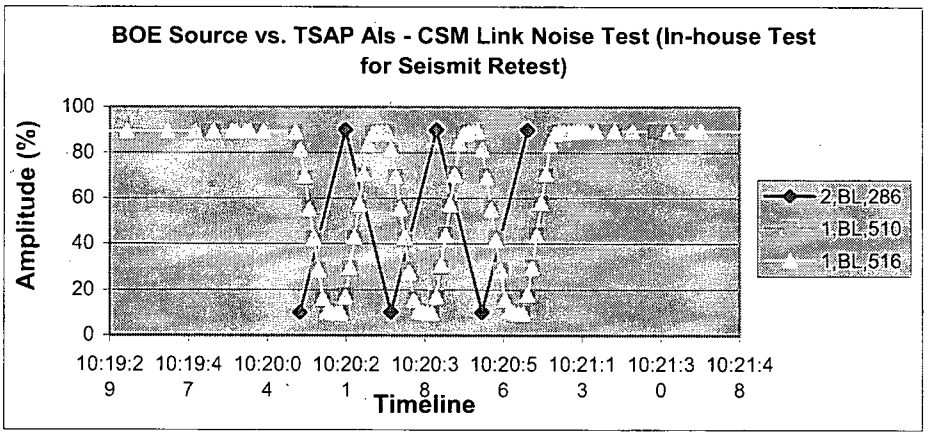
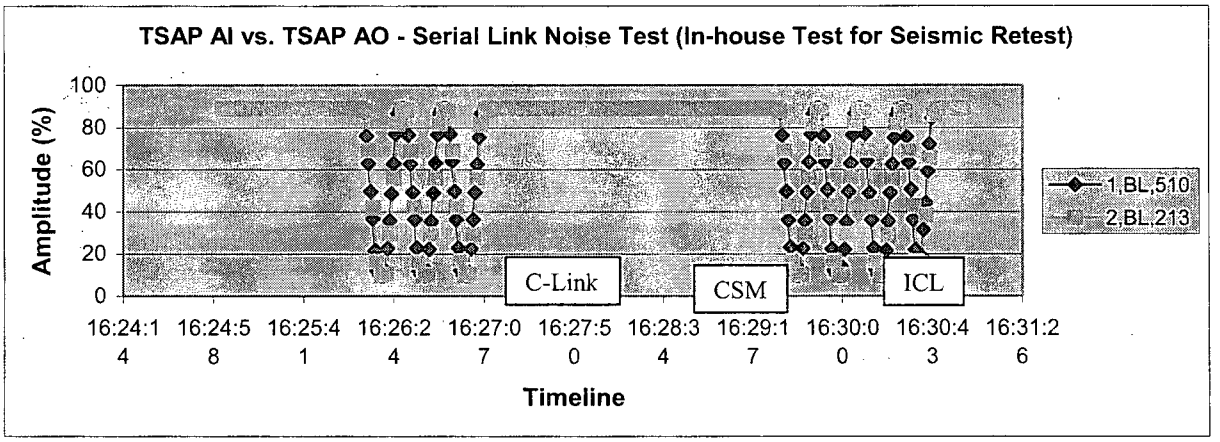


Figure B.5-1. BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from In House Test of Seismic Retest.



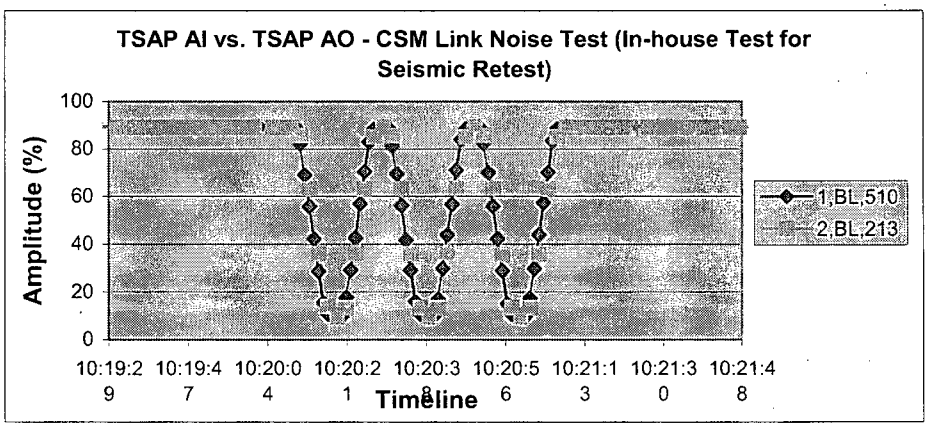
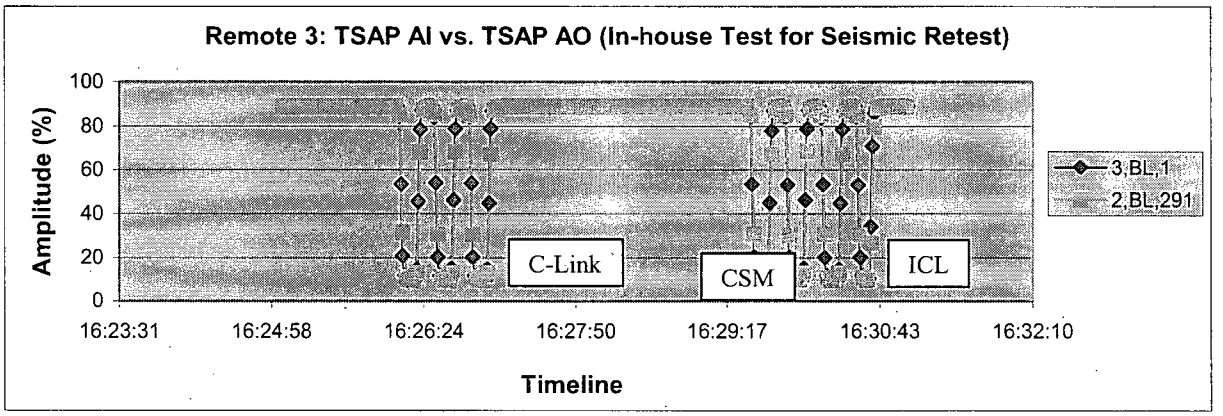


Figure B.5-2. TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) from In House Test of Seismic Retest.



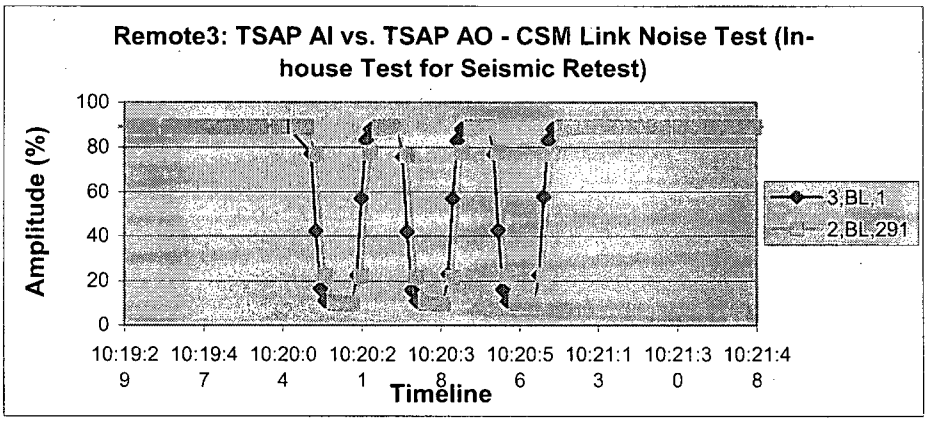


Figure B.5-3. Single Loop Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO from In House Test of Seismic Retest.

B.6 FAULT SIMULATION TEST

N/A.

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HFC-6000 Control System

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Seismic Testing Summary Report

TS901-000-35

Rev B

NON-PROPRIETARY

Effective Date	09/15/07
Author/Title	Allen Hsu/William J Gill
Reviewer/Title	John A. Stevens
Approval/Title	Terrence A. Gerardis

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Revision History

Date	Revision	Author	Changes
10/14/04	0	B. Han	Initial Draft
10/19/04	1	X. Li	Modify Power Loss and Power Interrupt
10/25/04	2	X. Li	Add new BOE Analysis Contents
11/8/04	3	X. Li	Incorporate Review Changes, Layout Changes
11/10/04	A	X. Li	Rev A Release
9/15/2007	B	A.Hsu/W.Gill	Revised Scope of Topical Report

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1.0 PURPOSE

HFC is generically qualifying its HFC-6000 control system for nuclear safety-related applications in U.S. nuclear power plants. The approach taken for this qualification effort is based on the guidance provided in EPRI-TR-107330, Generic Requirement Specification for Qualifying Commercially Available PLC for Safety-Related Applications in Nuclear Power Plants.

The Seismic test was initially performed at Wyle. The first test was performed on 4/2/2004 and 4/3/2004. During analysis of the initial seismic test data, the Test Specimen experienced several anomalies and a fault in the data recorder resulted in a loss of significant data.. As a consequence, HFC decided to repeat the entire seismic test. The Seismic tests were conducted a second time at Wyle on 9/22/2004 and 9/23/2004. This second test is often referred as "Seismic Test 2" in this report.

This document specifically addresses results of the Seismic Testing segment (i.e. Seismic Test 2) of the qualification testing program.

2.0 SCOPE

- Define the test setup and Seismic Qualification tests performed by Wyle Laboratories.
- Evaluate the Operating and Prudency testing performed before/during/after the Seismic Qualification test to identify any performance degradation from the Baseline Operating and Prudency testing performed.
- Evaluate any anomalies detected during the course of the Seismic Qualification tests.
- The tests included a low amplitude resonance search, five OBEs, one SSE, and post testing inspection and Operability and Prudency testing.

3.0 REFERENCES AND ACRONYMS

3.1 REFERENCES

TS901-000-34	HFC6000 Seismic Retest In House Testing Summary Report
TP0402	Operability Test Procedure
TP0403	Prudency Test Procedure
TP0405	Seismic Test Procedure
TP0408B	Test Specimen Validation Test Procedure
VV0414	Master Configuration List
50043	"Test Procedure for Seismic Testing of one HFC-6000 Control System" (Wyle Laboratories)
	Hand-written HFC Test Log

50043	Test Procedure for Seismic Testing of one HFC-6000 Control System (Wyle Laboratories)
51378-1	Test Report "Environmental and Seismic Testing of an HFC-6000 Control System" (Wyle Laboratories)
700911-01	HFC-6000 Seismic Test Equipment Layout

3.2 ACRONYMS

BOE	Burst of Events
HAS	Historical Archiving System
HIFR	Host Interface Remote
HPAT	HFC Plant Automated Tester
ICL	Intercommunication Link
M/A	Manual/Automatic
OBE	Operating Basis Earthquake
RRS	Required Response Spectrum
SOE	Sequence of Events
SSE	Safety Shutdown Earthquake

4.0 HFC-6000 SEISMIC QUALIFICATION DESCRIPTION

Seismic testing exposes a specially configured HFC-6000 control system (Test Specimen) to a set of dynamic spectra designed to simulate five Operating Basis Earthquakes (OBEs) and a Safe Shutdown Earthquake (SSE). The dynamic spectra consisted of tri-axial, random, multi frequency waveforms that were transmitted to the Test Specimen by means of hydraulic actuators attached to a Seismic Simulator Table. Figure 1 illustrates the OBE and SSE spectra recommended by EPRI TR-107330 and the actual spectra used due to the limitations of the Wyle test fixture. The overall scope of testing consisted of the following phases:

- Initial setup and pre-qualification testing for equipment
- Low amplitude resonance search to identify critical frequencies below 100 Hz
- Five OBE
- One SSE
- Post seismic test inspection and Operability and Prudency tests.

A preliminary resonance test was conducted to determine if the Test Specimen components had any resonant frequencies within the RRS. The test was conducted by Wyle test personnel by imposing a low level sinusoidal sweep. If one or more resonant frequencies were detected, the Test Response Spectrum (TRS) was to be centered on the resonant frequency that produced the maximum response in the Test Specimen. Overall requirements for the resonance search were governed by IEEE 344.

Wyle personnel conducted the dynamic seismic tests using the TRS established as the result of the resonance sweep test in accordance with Wyle Test Procedure 50043. Wyle personnel performed five tests based on the OBE RRS and one test based on the SSE RRS. The response spectrum of the Test Specimen was reported for 0.5%, 1.0%, 2.0%,

3.0%, and 5.0% damping factors. While any particular dynamic test was in progress, an HFC test engineer ran the specified combination of automated tests to verify overall system performance. Following each dynamic test, the entire Test Specimen was examined for mechanical damage. All mechanical damage sustained during testing was recorded and has been reported in detail within this report.

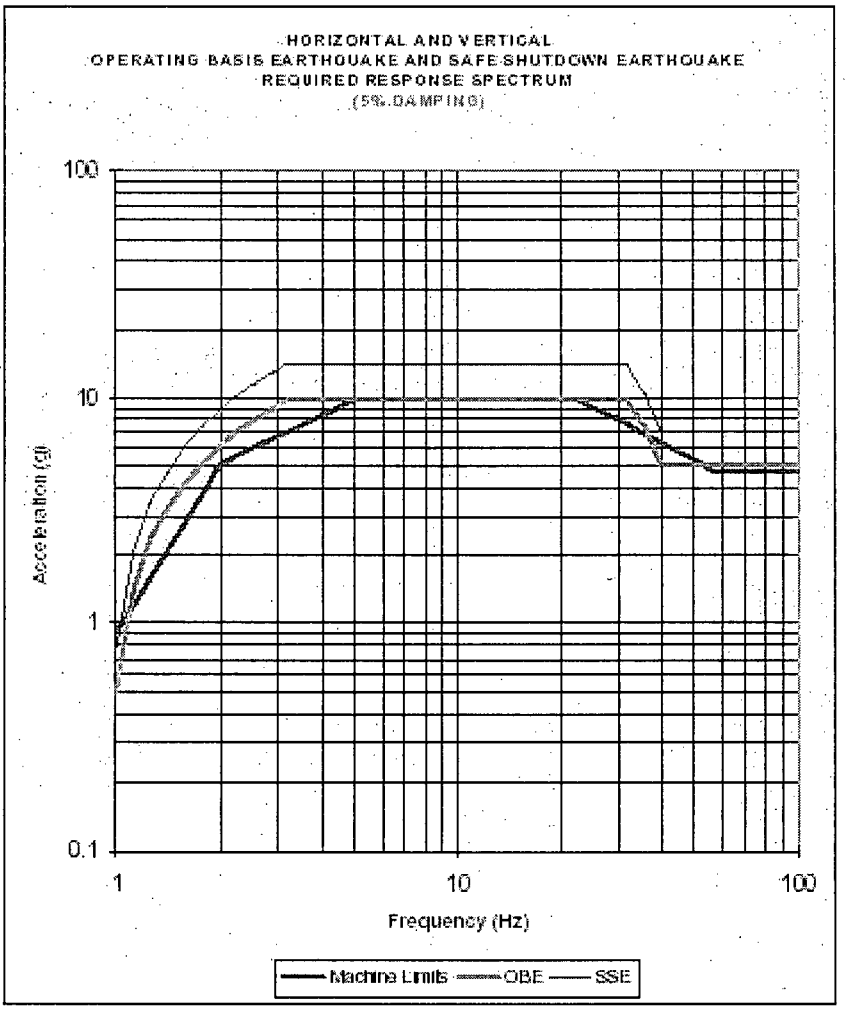

Figure 1. Seismic Test Spectra.

5.0 HFC-6000 SEISMIC TEST SETUP DESCRIPTION

The test setup included a larger spectrum of equipment than the equipment being qualified. The test setup defined in this section of the report includes the entire Test Specimen. The analysis in the remainder of this report is limited to the equipment being qualified.

The Test Specimen was installed in a standard 19-inch equipment cabinet for prequalification testing at HFC. After completion of the prequalification tests, the 19-inch cabinet, HPAT (HFC Plant Automated Tester) cabinet, PC workstation,

interconnecting cables and necessary support equipment was shipped to Wyle Laboratories for execution of the seismic test. The Test Specimen was received at Wyle and mounted on three open frame metal structures (fabricated by Wyle) that had been welded to the surface of the Seismic Simulation Table. (Refer to Wyle Test report 51378-1.) The physical arrangement of the test specimen was as follows:

- One support structure provided the physical mount for Remote 1 consisting of four HFC-6000 chassis, a power supply chassis, and panel-mounted equipment (switch modules and M/A stations). The power supply chassis was positioned at the bottom of the support structure closest to the table surface, and the panel-mounted equipment was located at the top. I/O cables for this remote were connected to the rear of the backplane and secured in place with jack screws. Communication with the HFC-FPD and ECS-B232 modules was accomplished by cables that connected at the front of the controller modules. The switch module, M/A station, FPD, and ECS-B232 are not being qualified.

- The following equipment was mounted on the second support structure:

  - One flat panel display (FPD) was mounted at the bottom of the structure closest to the table surface. The second FPD of the Test Specimen was not included in the seismic test.
  - A panel with two ECS-B232 fiber-optic repeater modules required for the fiber-optic communications link (C-Link) between the HPAT and the Test Specimen.
  - One HFC-FPCB module mounted directly on top of the shake table.

- The third mounting structure provided the physical mount for Remote 3 (single-loop controller), which was mounted inside a separate Hoffman cabinet assembly.

The C-Link and FPCB module are not being qualified.

6.0 SEISMIC TEST SEQUENCE

Table 1 provides the detailed sequence of events associated with the seismic qualification test. The time parameter in the table provides the basis for locating the data associated with each test in the HAS database and in the SOE files. Accurate identification of the test times is critical, because each of the seismic tests lasted no more than 30 seconds.

Table 1. **Seismic Tests Time Ranges.**

Tests	Date	Start	End
Pre Test BOE	9/22/04	9:59 am 10:12 am	10:05 am 10:18 am
OBE1	9/22/04	4:11 pm	4:14 pm
OBE2	9/23/04	8:16 am	8:21 am
OBE3	9/23/04	9:13 am	9:17 am
OBE4	9/23/04	9:38 am	9:41 am
OBE5	9/23/04	9:54 am	9:56 am
SSE	9/23/04	10:27 am	10:30 am
Post Test	9/23/04	12:17 pm	12:22 pm 2:37 pm

The following summarizes the overall sequence for repeat of the seismic test:

1) Assemble Test Specimen on seismic simulator table, and perform TP0408B to verify system operation.

2) Run the automated portions of the Operability and Prudency tests in accordance with TP0405.

3) Run the resonance search test.

4) Run five OBEs and one SSE with background Operability and Prudency tests running.

5) Run the post test sequence defined by TP0405.

7.0 TEST EVALUATION

The Operability and Prudency test results from the "HFC Seismic Retest In-House Testing", performed prior to shipment to Wyle, establish the baseline limits against which the seismic test results will be evaluated.

The test evaluation methods include data analysis of OBEs and SSE data compared with data from;

- HAS and SOE data logged for automatic tests,
- Static point examination,
- System alarm files,
- Examination of testing records recorded by testing personnel,
- Reference to Wyle test reports

The following sections provide descriptions of overall test results, any anomalies that occurred, and resolutions for the anomalies.

7.1 PRE TESTS

7.1.1 General Descriptions

The purpose of the pretest sequence is to verify that the test specimen is fully operational prior to the start of the seismic test. During the pretests, all of the automated Operability tests were run for a minimum period of 5 minutes. The automated Prudency BOE test was run for 5 minutes. Communications with in the Test Specimen and to the test recorders were verified.

7.1.1 Acceptance Criteria

Preliminary Operability and Prudency tests results shall remain within the acceptance limits listed in documents TS901-000-34. Any deviation from baseline results established during in house testing shall be identified and recorded.

7.1.2 Results

Based on the Pre-Test data evaluation it is concluded that the test specimen was correctly reassembled following shipment to Wyle and fully operational before the start of the seismic test except for the single anomaly listed in Section 7.1.3.

Detailed description and evaluation of test results are provided in Attachment A.

7.1.3 Anomalies

The following is a list of anomalies:

- Of the three RTD input channels monitored by HAS through AIC blocks, one was within tolerance limits and two channels were slightly off from baseline tolerance limits.

- Assessment: Probable cause is stray resistances in terminal connections to wiring leads. These resistances can change by one or two ohms when wires are connected and disconnected. The deviations are considered to have negligible impact on the seismic testing and evaluations.

7.2 SEISMIC TESTS

7.2.1 General Descriptions

The main test specimen was subjected to OBE1, OBE2, OBE3, OBE4, OBE5 and SSE tests. Automatic Operability and Prudency tests were run during these testing periods as well as after SSE.

7.2.2 Acceptance Criteria

Overall acceptance criteria for seismic testing are specified in paragraph 4.3.9 of EPRI TR-107730. These criteria are summarized as follows:

- The Test specimen shall meet its performance requirements during and following application of an SSE simultaneously applied in three orthogonal directions. The Test Specimen shall withstand application of the SSE spectrum after application of five OBEs.

- All connections shall remain intact, all modules shall remain fully inserted, and no functional or non-functional parts shall fall off. Tightening fasteners between successive OBEs or before the SSE does not constitute a failure condition.

- Relay contacts shall be capable of changing state from energized to deenergized and from deenergized to energized during application of OBEs and the SSE spectrum. Any spurious changes in state shall not last for longer than 2 ms for both energized and deenergized relays.

7.2.3 Results

The system successfully withstood the SSE after five OBEs seismic tests and continued to function normally. The overall system performance was within acceptable limits. Recorded anomalies and the associated assessments are listed in Section 7.2.4. Detailed descriptions and evaluations of test results are provided in Attachment A.

7.2.4 Anomalies

The followings are a list of anomalies during the tests:

-

8.0 SUMMARY

The system successfully withstood the seismic tests and continued to function normally. The overall system performance was within acceptable tolerance limits except for the anomalies listed below:

- After OBE3, one of the center power supplies came part way out, but power was not lost, and no functional failure was noted. A locking bar will included of all future nuclear plant systems.

- A secondary system controller was lost sometime before or during the SSE. The system was still operating normally with one system controller. Therefore, this does not constitute a failure.

- Two RTD channels slightly deviate from in house testing results. The results during seismic testing are consistent with those in the Pre test. This deviation is typical of stray resistances due to reconnection of signal wires to terminals and not a characteristic of RTD input module.

The recommended correction to the system is as follows:

Install a power supply locking bar or retest the power supplies having an enhanced locking mechanism.

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Appendix A

Operability and Prudency Tests

A.1 GENERAL

This attachment is to document the results of the Operability Tests and Prudency Tests in Pre, During, and Post Seismic tests. The acceptance criteria against which the test results are evaluated are provided in the related test procedures and the seismic baseline test report. The acceptance criteria for the seismic related Operability test and Prudency test results shall remain within the tolerance limits established by the baseline testing, as listed in Attachment A of Baseline Testing Summary Report and as modified by the "Seismic Retest In-house Testing Summary Report". Any deviation from baseline results established during in-house testing will be identified and recorded.

All the automated operability tests and prudency tests were run for approximately 5 minutes during each individual seismic test. These tests include AI Accuracy Test, AO Accuracy Test,, Communication Test, Timer Test, Digital BOE test and Analog BOE test.

The table below lists time ranges for the seismic tests performed. Automated operability tests and prudency tests were conducted during these periods.

Table A.1-1. **Seismic Tests Time Ranges.**

Tests	Date	Start	End
Pre Test BOE	9/22/04	9:59 am 10:12 am	10:05 am 10:18 am
OBE1	9/22/04	4:11 pm	4:14 pm
OBE2	9/23/04	8:16 am	8:21 am
OBE3	9/23/04	9:13 am	9:17 am
OBE4	9/23/04	9:38 am	9:41 am
OBE5	9/23/04	9:54 am	9:56 am
SSE	9/23/04	10:27 am	10:30 am
Post Test	9/23/04	12:17 pm	12:22 pm 2:37 pm

Besides the SOE data and HAS data evaluation as described in the following sections, chatter box charting and system alarm files have been examined. The chatter box charting shows that the automatic tests were operating normally during the seismic tests, and no relay contact bounce was indicated during any seismic test run.

A.2 4-20 MA AI ACCURACY TEST

The tolerance limits for pre test and post test are ±0.1% and for seismic tests are ±0.35%.

A.2.1 Pre Test

AI Accuracy was within tolerance limits as shown in the table below.

Table A.2-1. **AI Accuracy – Pre Seismic Test.**

Expected (%)	Measured (%)	Accuracy (%)
9.424		
29.397		
49.359		
69.331		
89.294		

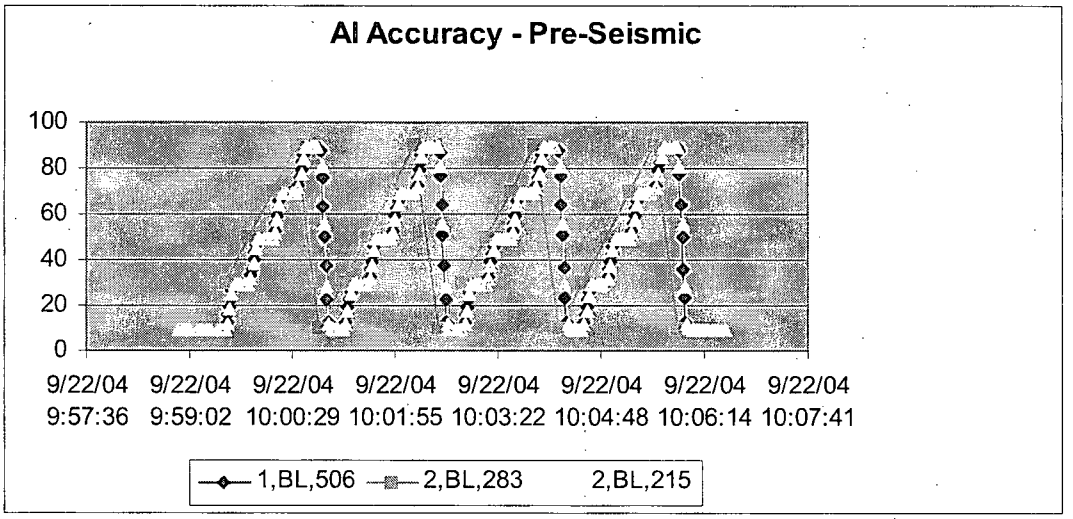

Figure A.2-1. **AI Accuracy – Pre Seismic.**

A.2.2 OBE1

OBE1 was run twice, with power set to 120 vac 60 HZ for the first time and 90 vac 57 HZ for the second time. The data from the second run is used for test results. The AI16F card used for AI accuracy test and analog BOE test apparently went off at the OBE1 first run as shown in the figure below. Shutdown of the module apparently was caused by watchdog timeout and not related to the seismic test. It was not discovered and reset until after OBE2. The card failure has been reported as an alarm as shown in Table A.2-2. As a consequence, there was no data for AI accuracy for OBE1 and OBE2. Figure A.2-2 and Figure A.2-3 illustrates how the AI card associated with 1,BL,506 stop working during OBE1. It should be noted, however, that these alarm conditions were also detected for this card prior to the Wyle seismic retest program. Alarm file on 8/27/04 showed multiple occurrences for these alarm conditions. This loss of AI16F data for OBE1 and OBE2 is not considered significant since data is available for OBS3, OBE4, OBE5 and SSE. AI accuracy for the OBE1 rerun is shown in Figure A.2-3.

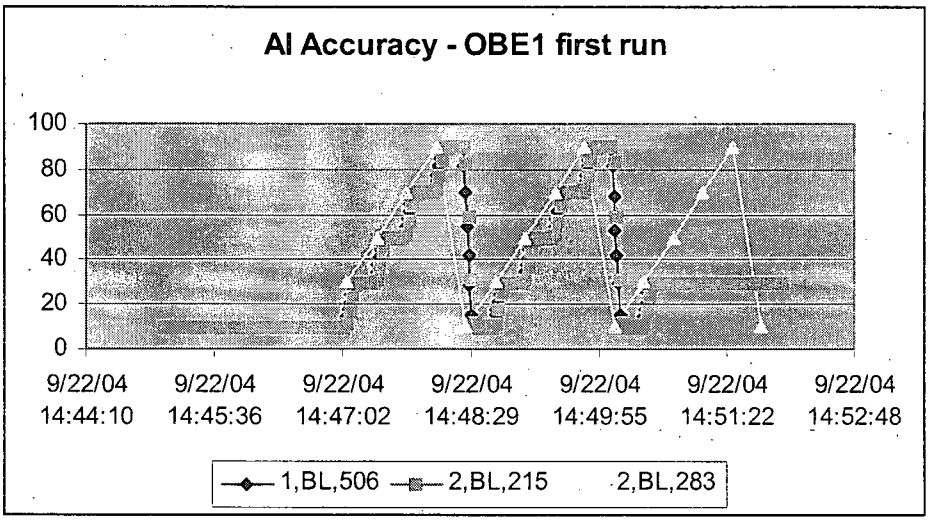

Figure A.2-2. **AI Accuracy – OBE1 First Run.**

Table A.2-2. **Alarms at OBE1 First Run.**

DATE	TIME	NAME	DESCRIPTION	VALUE	EVENT
22-Sep	14:50:35	1,FL,69	LINK 0 STATION 52 FAIL	1	ALARM
22-Sep	14:50:35	1,FL,1044	ANALOG OUT OF RANGE ALM	1	ALARM

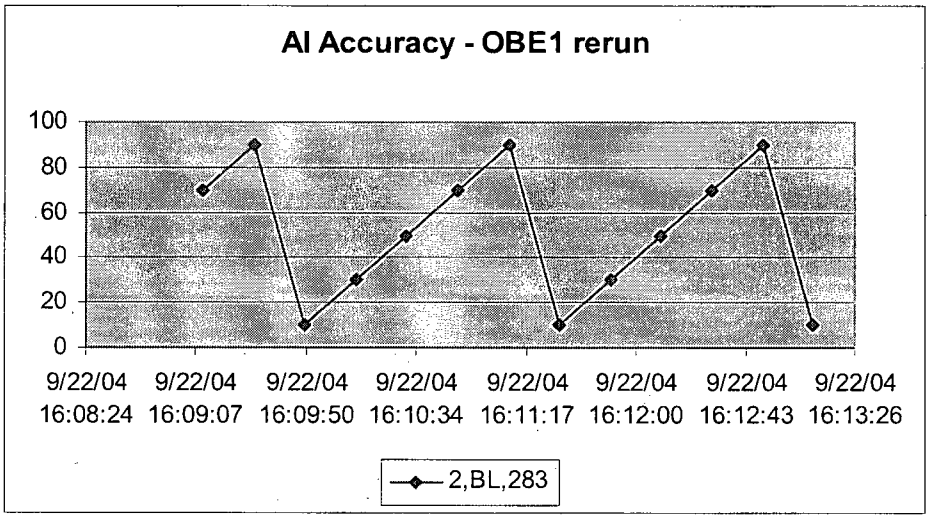

Figure A.2-3. **AI Accuracy – OBE1 Rerun.**

A.2.3 OBE2

No data was available for AI16F as explained in the section above. Figure A.2-4 shows that the AI card associated with 1,BL,506 was not working during OBE2. Table A.2-3 shows that an ICL station alarm existed for this card.

Table A.2-3. **Alarms around OBE2.**

DATE	TIME	NAME	DESCRIPTION	VALUE	EVENT
23-Sep	8:05:53	1,FL,69	LINK 0 STATION 52 FAIL	1	ALARM
23-Sep	8:58:48	1,FL,69	LINK 0 STATION 52 FAIL	1	ALARM

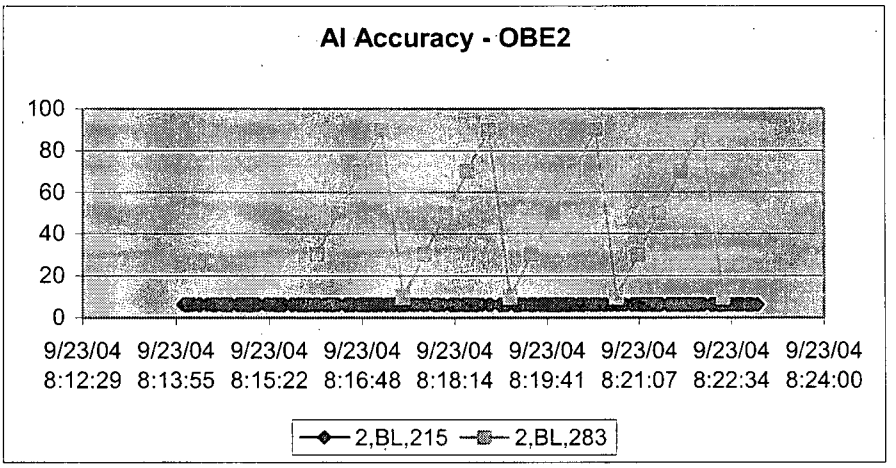

Figure A.2-4. **AI Accuracy – OBE2.**

A.2.4 OBE3

The AI accuracy was within tolerance limits as shown in Table A.2-4. Figure A.2-5 shows the operation of AI accuracy test before, during and after OBE3. When the test was run, the operation was disturbed for about 1 minute and the source signal for the test was not running. After that, the test resumed operation, the test results are within tolerance limits.

Table A.2-4. **AI Accuracy – OBE3.**

Expected (%)	Measured (%)	Accuracy (%)
9.424		
29.397		
49.359		
69.331		
89.294		

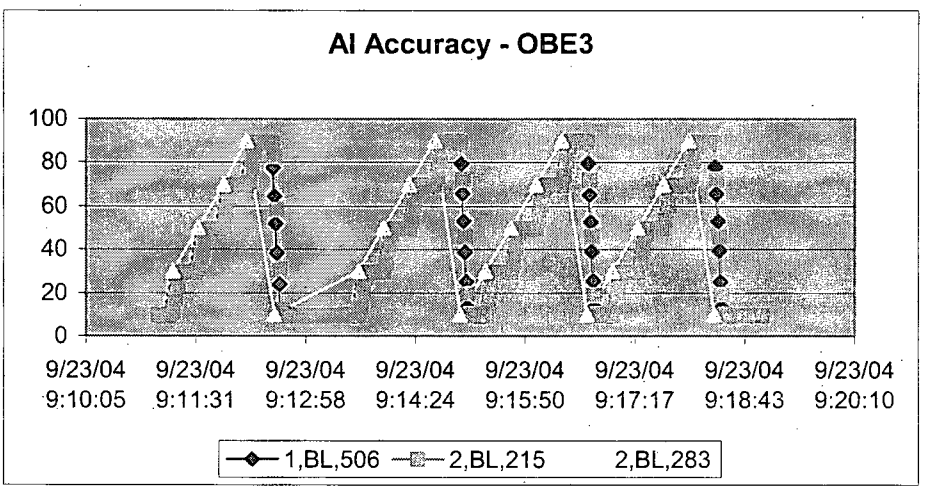

Figure A.2-5. **AI Accuracy – OBE3.**

A.2.5 OBE4

AI accuracy was within tolerance limits as shown in Table A.2-5 and Figure A.2-6.

Table A.2-5. **AI Accuracy – OBE4.**

Expected (%)	Measured (%)	Accuracy (%)
9.424		
29.397		
49.359		
69.331		
89.294		

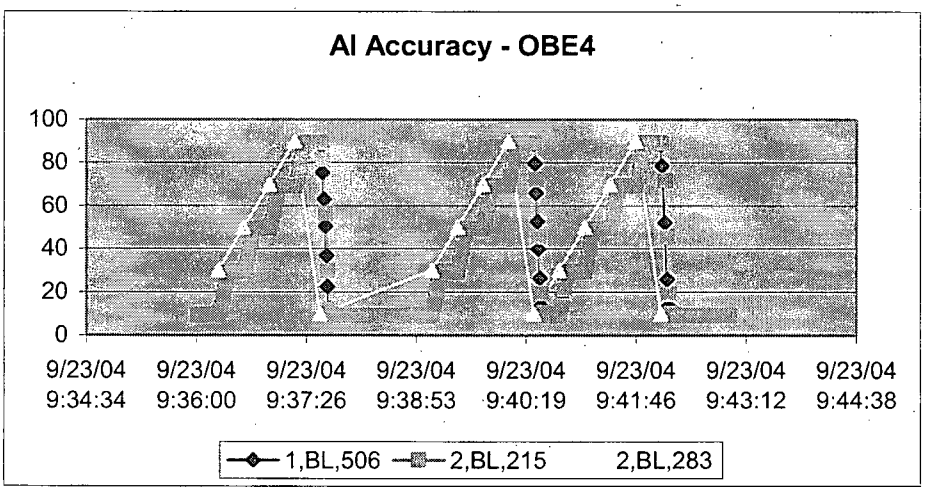

Figure A.2-6. **AI Accuracy – OBE4.**

A.2.6 OBE5

AI accuracy was within tolerance limits as shown in Table A.2-6 and the system was operating normally as shown in Figure A.2-7.

Table A.2-6. **AI Accuracy – OBE5.**

Expected (%)	Measured (%)	Accuracy (%)
9.424		
29.397		
49.359		
69.331		
89.294		

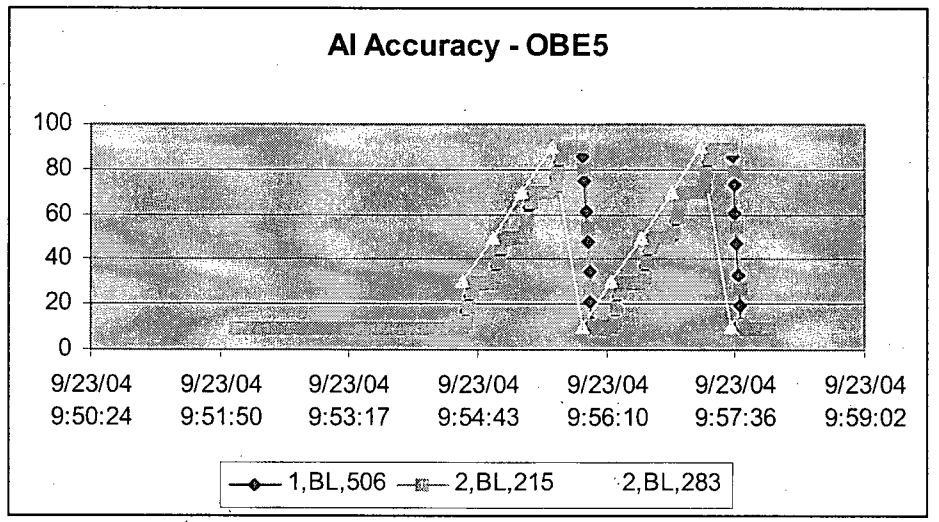

Figure A.2-7. **AI Accuracy – OBE5.**

A.2.7 SSE

The AI accuracy was within tolerance limits as shown in Table A.2-7 and the system was operating normally as shown in Figure A.2-8.

Table A.2-7. **AI Accuracy – SSE.**

Expected (%)	Measured (%)	Accuracy (%)
9.424		
29.397		
49.359		
69.331		
89.294		

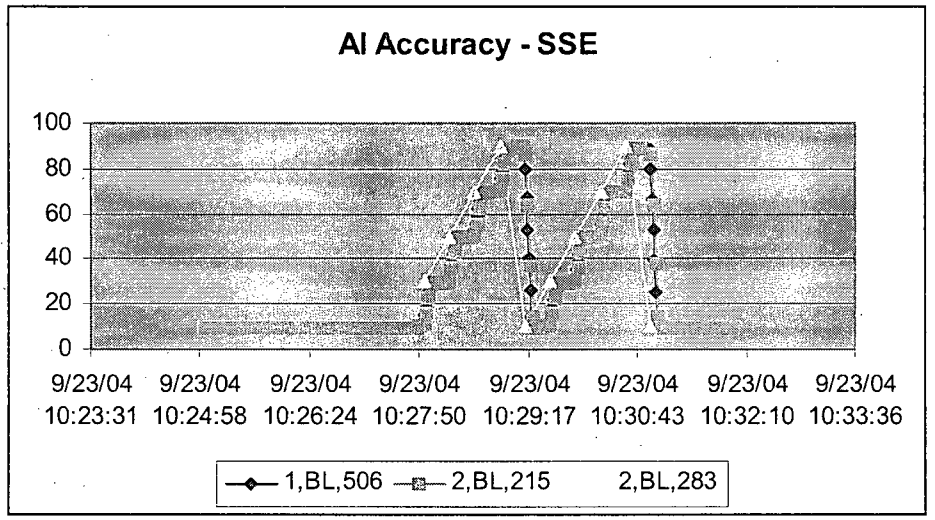

Figure A.2-8. **AI Accuracy – SSE.**

A.2.8 Post Test

The AI accuracy was within tolerance limits as shown in Table A.2-8 and the system was operating normally as shown in Figure A.2-9.

Table A.2-8. **AI Accuracy – Post Seismic.**

Expected (%)	Measured (%)	Accuracy (%)
9.424		
29.397		
49.359		
69.331		
89.294		

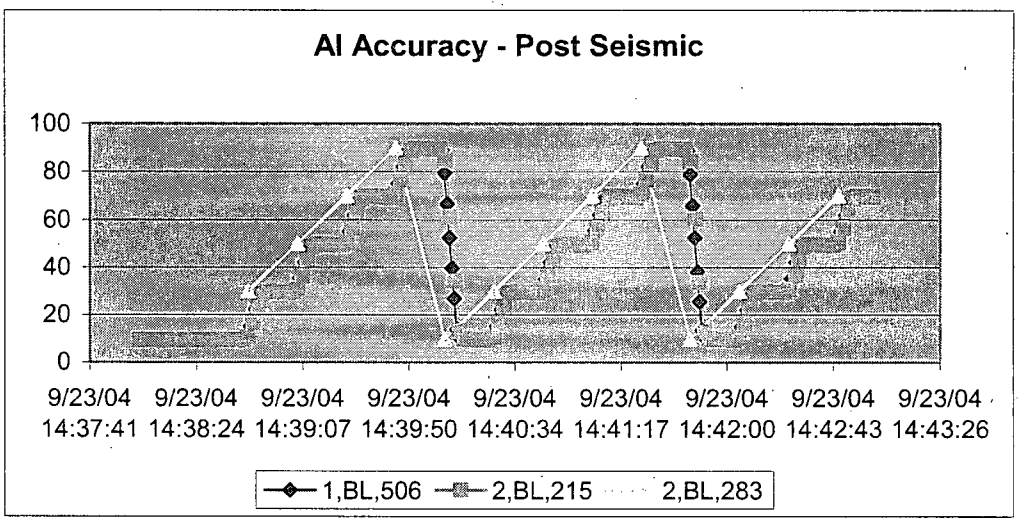

Figure A.2-9. **AI Accuracy – Post Seismic.**

A.3 AO ACCURACY

The tolerance limits for pre test and post test are ±0.1% and for seismic tests are ±0.32%.

A.3.1 Pre Test

AO accuracy was within tolerance limits as shown in Table A.3-1 and the system was operating normally as shown in Figure A.3-1.

Table A.3-1. **AO Accuracy – Pre Test.**

Expected (%)	Measured (%)	Accuracy (%)
9.985625		
29.966875		
49.971875		
69.98125		
89.95625		

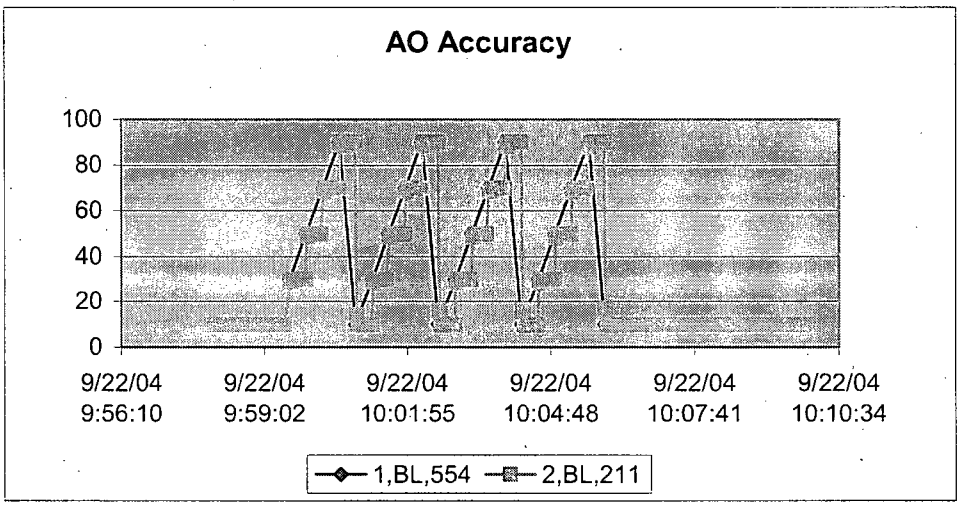

Figure A.3-1. **AO Accuracy – Pre Test.**

A.3.2 OBE1

AO accuracy was within tolerance limits as shown in Table A.3-2 and the system was operating normally as shown in Figure A.3-2.

Table A.3-2. **AO Accuracy – OBE1.**

Expected (%)	Measured (%)	Accuracy (%)
9.985625		
29.96688		
49.97188		
69.98125		
89.95625		

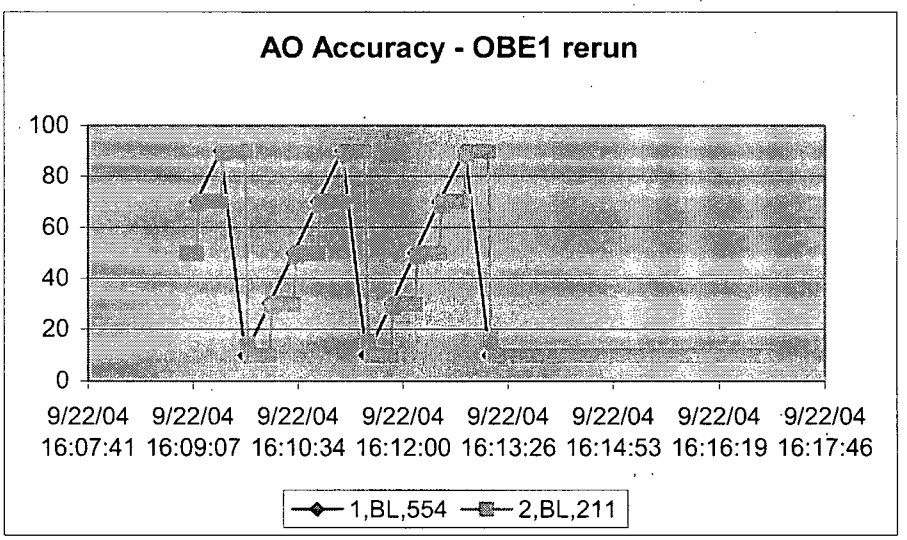

Figure A.3-2. **AO Accuracy – OBE1.**

A.3.3 OBE2

AO accuracy was within tolerance limits as shown in Table A.3-3 and the system was operating normally as shown in Figure A.3-3.

Table A.3-3. **AO Accuracy – OBE2.**

Expected (%)	Measured (%)	Accuracy (%)
9.985625		
29.96688		
49.97188		
69.98125		
89.95625		

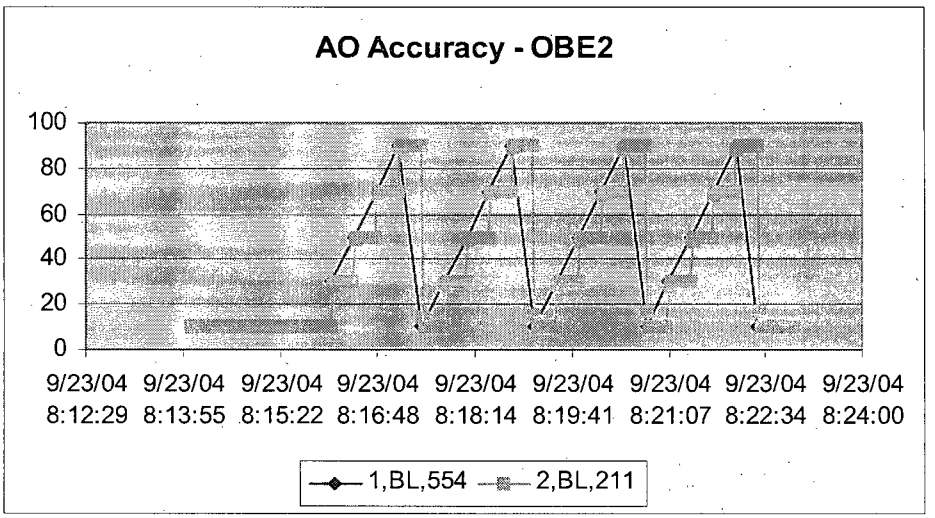

Figure A.3-3. **AO Accuracy – OBE2.**

A.3.4 OBE3

AO accuracy was within tolerance limits as shown in Table A.3-4 and the system was operating normally as shown in Figure A.3-4.

Table A.3-4. **AO Accuracy – OBE3.**

Expected (%)	Measured (%)	Accuracy (%)
9.985625		
29.96688		
49.97188		
69.98125		
89.95625		

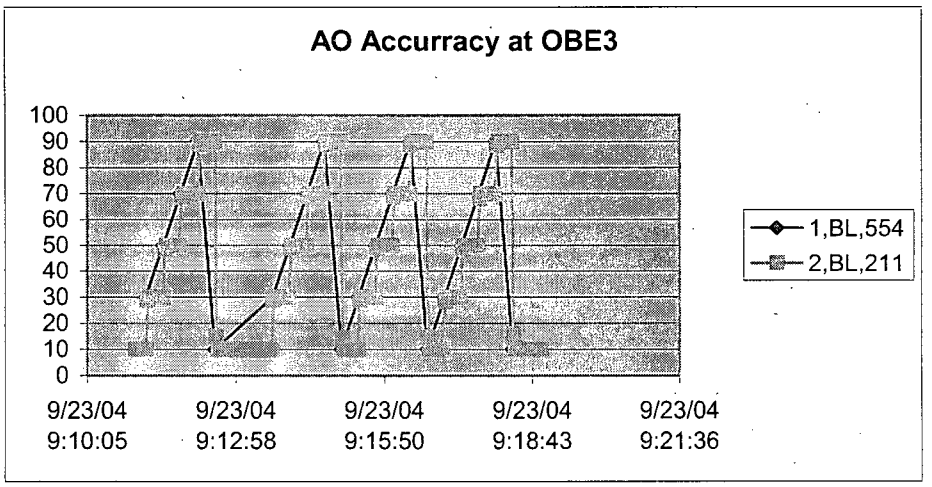

Figure A.3-4. **AO Accuracy – OBE3.**

A.3.5 OBE4

AO accuracy was within tolerance limits as shown in Table A.3-5 and the system was operating normally as shown in Figure A.3-5.

Table A.3-5. **AO Accuracy – OBE4.**

Expected (%)	Measured (%)	Accuracy (%)
9.985625		
29.96688		
49.97188		
69.98125		
89.95625		

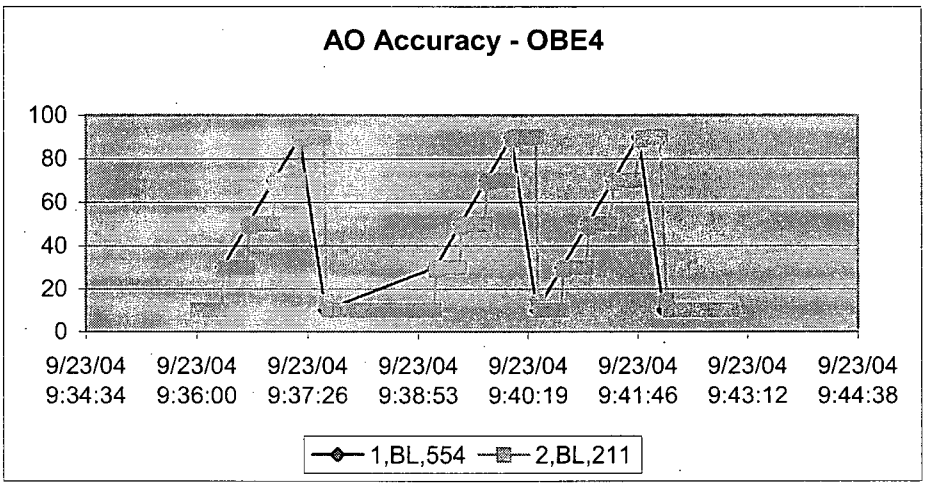

Figure A.3-5. **AO Accuracy – OBE4.**

A.3.6 OBE5

AO accuracy was within tolerance limits as shown in Table A.3-6. and the system was operating normally as shown in Figure A.3-6.

Table A.3-6. **AO Accuracy – OBE5.**

Expected (%)	Measured (%)	Accuracy (%)
9.985625		
29.96688		
49.97188		
69.98125		
89.95625		

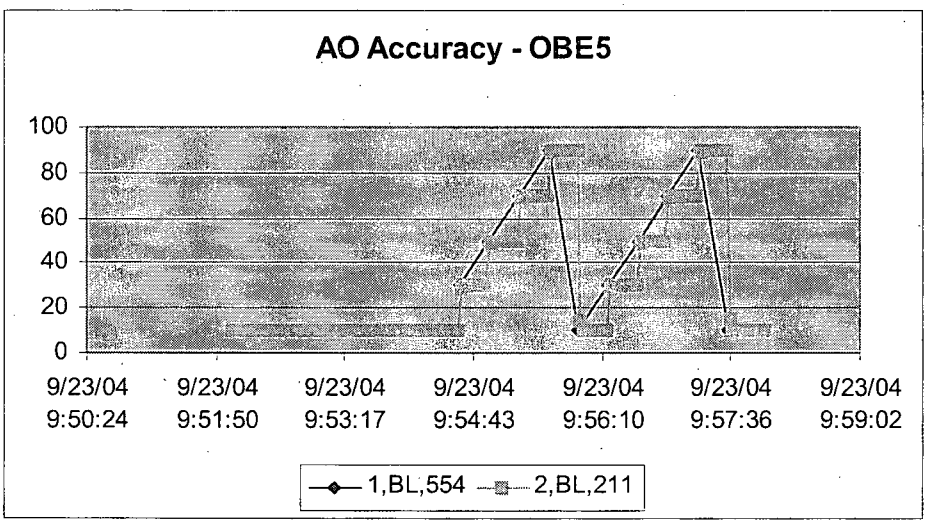

Figure A.3-6. **AO Accuracy – OBE5.**

A.3.7 SSE

AO accuracy was within tolerance limits as shown in Table A.3-7 and the system was operating normally as shown in Figure A.3-7.

Table A.3-7. **AO Accuracy – SSE.**

Expected (%)	Measured (%)	Accuracy (%)
9.985625		
29.96688		
49.97188		
69.98125		
89.95625		

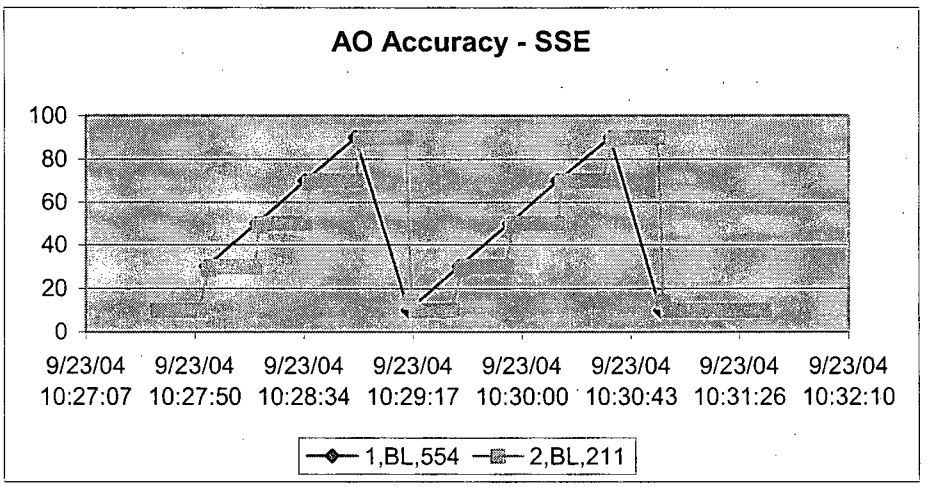

Figure A.3-7. **AO Accuracy – SSE.**

A.3.8 Post Seismic

AO accuracy was within tolerance limits as shown in Table A.3-8 and the system was operating normally as shown in Figure A.3-8.

Table A.3-8. **AO Accuracy – Post Seismic.**

Expected (%)	Measured (%)	Accuracy (%)
9.985625		
29.96688		
49.97188		
69.98125		
89.95625		

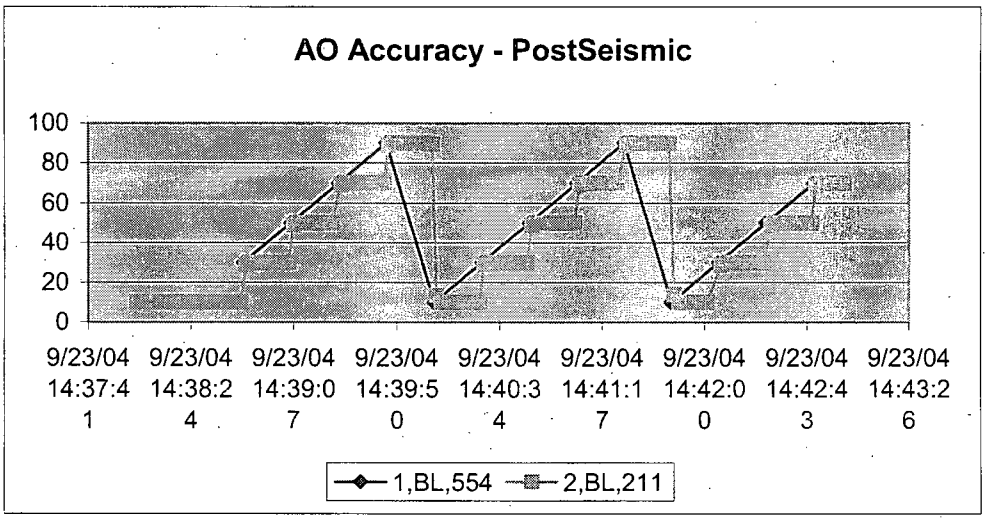

Figure A.3-8. **AO Accuracy – Post Seismic.**

A.4 RTD

The acceptance criteria for RTD qualification test are ±3.6 °F (±2 °C).

A.4.1 Pre Tests

The RTD accuracy was within tolerance limits for 1,BL,528 as shown in Table A.4-1 but slightly off for the other two RTD blocks. Because contact resistance can change each time a terminal is reconnected, the pre seismic baseline test results were used to evaluate RTD performance. These minor deviations are considered insignificant for evaluation of seismic performance.

Table A.4-1. **RTD – Pre Tests.**

	Expected (°C)	Average (°C)	STDEV (°C)	Accuracy (%)
1,BL,10	72.93			
1,BL,528	79.95			
1,BL,546	79.25			

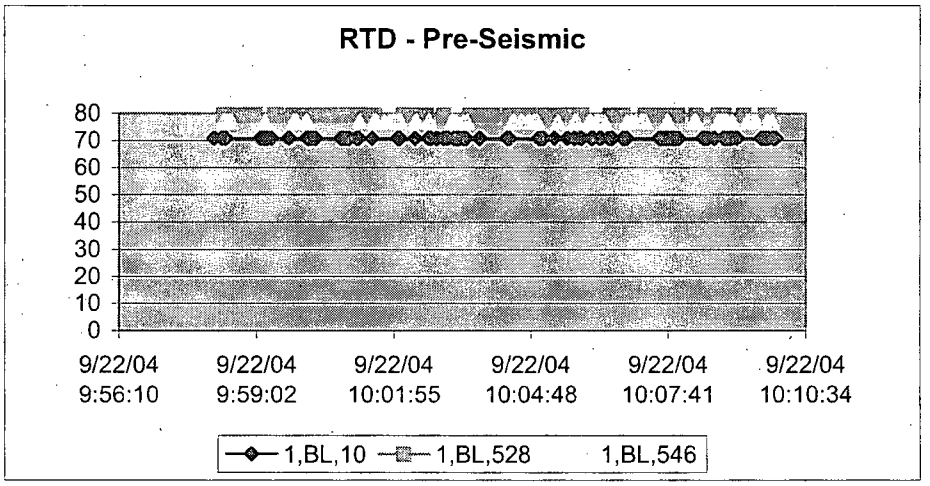

Figure A.4-1. **RTD – Pre Seismic.**

A.4.2 OBE1

The RTD accuracy was within tolerance limits for 1,BL,528 but slightly off for the other two RTD blocks as shown in Table A.4-2. The results are in line with the pre seismic test.

Table A.4-2. **RTD – OBE1.**

	Expected (°C)	Average (°C)	STDEV (°C)	Accuracy (%)
1,BL,10	72.93			
1,BL,528	79.95			
1,BL,546	79.25			

A.4.3 OBE2

The RTD accuracy was within tolerance limits for 1,BL,528 but slightly off for the other two RTD blocks as shown in Table A.4-3. The results are in line with the pre seismic test.

Table A.4-3. **RTD – OBE2.**

	Expected (°C)	Average (°C)	STDEV (°C)	Accuracy (%)
1,BL,10	72.93			
1,BL,528	79.95			
1,BL,546	79.25			

A.4.4 OBE3

The RTD accuracy was within tolerance limits for 1,BL,528 but slightly off for the other two RTD blocks as shown in Table A.4-4. The results are in line with the pre seismic test.

Table A.4-4. **RTD – OBE3.**

	Expected (°C)	Average (°C)	STDEV (°C)	Accuracy (%)
1,BL,10	72.93			
1,BL,528	79.95			
1,BL,546	79.25			

A.4.5 OBE4

The RTD accuracy was within tolerance limits for 1,BL,528 but slightly off for the other two blocks as shown in Table A.4-5. The results are in line with the pre seismic test.

Table A.4-5. **RTD – OBE4.**

	Expected (°C)	Average (°C)	STDEV (°C)	Accuracy (%)
1,BL,10	72.93			
1,BL,528	79.95			
1,BL,546	79.25			

A.4.6 OBE5

The RTD accuracy was within tolerance limits for 1,BL,528 but slightly off for the other two blocks as shown in Table A.4-6. The results are in line with the pre seismic test.

Table A.4-6. **RTD – OBE5.**

	Expected (°C)	Average (°C)	STDEV (°C)	Accuracy (%)
1,BL,10	72.93			
1,BL,528	79.95			
1,BL,546	79.25			

A.4.7 SSE

The RTD accuracy was within tolerance limits for 1,BL,528 but slightly off for the other two blocks as shown in Table A.4-7. The results are in line with the pre seismic test.

Table A.4-7. **RTD – SSE.**

	Expected (°C)	Average (°C)	STDEV (°C)	Accuracy (%)
1,BL,10	72.93			
1,BL,528	79.95			
1,BL,546	79.25			

A.4.8 Post Test

The RTD accuracy was within tolerance limits for 1,BL,528 but slightly off for the other two RTD blocks as shown in Table A.4-8. The results are in line with the pre seismic baseline test.

Table A.4-8. **RTD – Post Test.**

	Expected (°C)	Average (°C)	STDEV (°C)	Accuracy (%)
1,BL,10	72.93			
1,BL,528	79.95			
1,BL,546	79.25			

A.5 PULSE INPUT CHANNELS

The acceptance criteria for both Rate mode and Accumulate mode is 0.1% over the full scale.

A.5.1 Rate Mode Channel

The Pre Test results are used as a baseline to evaluate the test results during seismic tests. The pulse input channel associate with 1,BL,535 was set to Rate mode and the one associated with 1,BL,539 was set to Accumulate mode. Both blocks show a percentage value. The maximum input is 20 KHz. The prescaler value for the Accumulate mode is 1000. The input frequency is 997.6 Hz. The expected value for 1,BL,535 is calculated as 997.6/20,000*100% = 4.988.

	Average (%)	STDEV (%)	Expected (%)	Accuracy (%)
1,BL,535				

During the different seismic test periods and post test, the Rate mode channel was within tolerance limits as shown below.

	Average (%)	STDEV (%)	Expected (%)	Accuracy (%)
1,BL,535				

A.5.2 Accumulate Mode Channel

1,BL,539 Block value change per minute is calculated as follows:

99736*1/1000/16777215 = 5.945E-06.

It changes very slowly. In order to evaluate the performance of the accumulate mode channel during various seismic test, HFC scanned the block values to find a time period that covers the test period and experienced a reading change. For example, during the pre

test, the block value changed to 0.09 at 9:37 and changed to 0.10 at 10:15. The expected reading was calculated as follows:

Expected End Reading = Start Reading + 99736 * Seconds /1000/16777215

The actual reading was then compared with expected readings to obtain accuracy of the input.

Table A.5-1 provides a detailed analysis of performance of the accumulate mode pulse input channel during each seismic test and the results were satisfactory.

Table A.5-1. **Accumulate Mode Pulse Input.**

Test	Test Date	Test Time	Start Reading	Start Time	Period (second)	End Time	Expected Reading	Actual End Reading	Accuracy
Pre Test	9/22/04	9:59 AM							
OBE1	9/22/04	4:11 PM							
OBE2	9/23/04	8:16 AM							
OBE3	9/23/04	9:13 AM							
OBE4	9/23/04	9:38 AM							
OBE5	9/23/04	9:54 AM							
SSE	9/23/04	10:27 AM							
Post	9/23/04	12:17 PM							

The accumulate mode block value remained the same during each seismic test period. The performance evaluated over extended periods of time as listed in Table A.5-1 demonstrated that the pulse card accuracy was not affected after each seismic run.

A.6 ICL COMMUNICATION OPERABILITY TEST

ICL communication tests were performed during pre-tests and post tests. No alarms or failures have been identified by testing personnel. HFC conclude that the communication operability was successful..

A.7 TIMER TEST

The timer function is controlled by the main processor OS and so is not directly susceptible to disruption by seismic stress. The timers controlled two DO images, that data was transferred via the ICL to a DO8J module, and the resulting signals were routed to the SOE interface via a cable assembly. The following failure conditions that might be expected during seismic excitation:

- Loss of power to some portion or all of the test specimen
- Relay contact jitter resulting in false transitions of the timer waveform
- Broken I/O cable wire resulting in loss of signal.

Tables A.7-1 and A.7.2 summarize the SOE data for the timer test accumulated during the seismic tests. The parameters listed in the tables are defined as follows:

Preset Value	Set timer interval in application program in seconds
Duration	Measured on/off time in seconds
Duration Deviation	The averaged deviation of the observed timer interval expressed as a percentage value.
Duration Jitter	The averaged difference between successive timer intervals expressed as a percentage value.
Period	Total measured period of signal waveform in seconds
Period Deviation	The averaged deviation of the measured waveform period expressed as a percentage.
Period Jitter	The averaged difference of successive periods from the preset value expressed as a percentage.

Table 07-1. **Automatic Timer Test Result for 4,DI,12**

4,DI,12		Preset Value	Duration (s)	Duration Deviation (%)	Duration Jitter (%)	Period (s)	Period Deviation (%)	Period Jitter (%)
Baseline	ON	5						
	OFF	1						
Pre Test	ON	5						
	OFF	1						
OBE2	ON	5						
	OFF	1						
OBE4	ON	5						
	OFF	1						
OBE5	ON	5						
	OFF	1						
SSE	ON	5						
	OFF	1						
Post Test	ON	5						
	OFF	1						

Table 0.7-2. **Automatic Timer Test Result for 2,DI,11**

4,DI,11		Preset Value	Duration (s)	Duration Deviation (%)	Duration Jitter (%)	Period (s)	Period Deviation (%)	Period Jitter (%)
Baseline	ON	1						
	OFF	1						
Pre Test	ON	1						
	OFF	1						
OBE2	ON	1						
	OFF	1						
OBE4	ON	1						
	OFF	1						
OBE5	ON	1						
	OFF	1						
SSE	ON	1						
	OFF	1						
Post Test	ON	1						
	OFF	1						

Conclusions

- No disruption in timer waveform was observed during any of the seismic tests.
- All timer periods remained within the theoretical tolerance limit established in the baseline report.

A.8 POWER LOSS OPERABILITY TEST

The purpose of this test was to demonstrate that all I/O channels transition to default power-off states when power was removed and then hold these states following restoration of power until after system initialization is complete, at which time normal operation resumes. This test was executed prior to the seismic test runs and then after completion of the SSE.

A.8.1 Pre Seismic Test

Figure A.8-1 and Figure A.8-2 illustrate the response of the analog output signals during the loss of power test for the pre seismic test. 1,BL,40 (1,AO,981) is a static signal from the TA05 level controller, 1,BL,504 (1,AO,841) is a static signal from the TA05 flow controller, and 2,BL,203 (1,AO,983) is a uncontrolled spare RTD point. For both dynamic and static analog outputs, the signals had a "fail high" spike and quickly returned and remained at their power-off state (0%) until the operation was resumed.

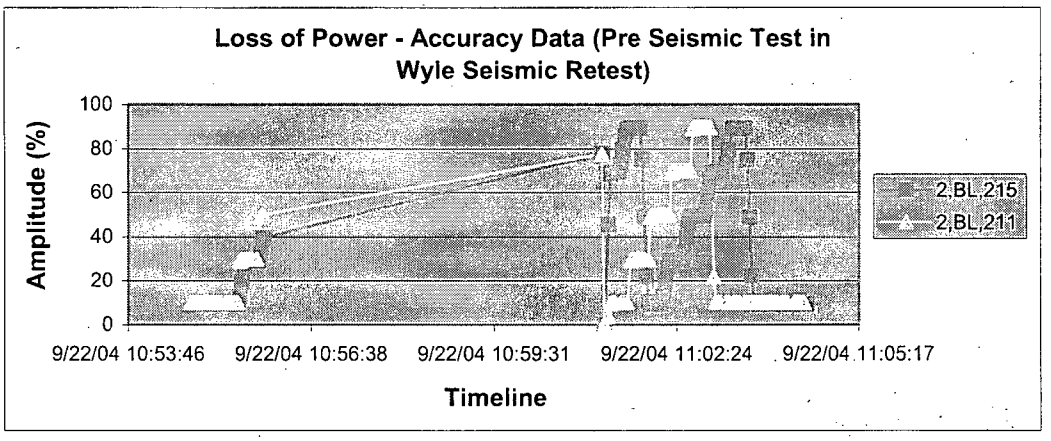

Figure 08-1. **Dynamic Analog Data During Loss of Power Test from Pre Seismic Test in Wyle Seismic Retest.**

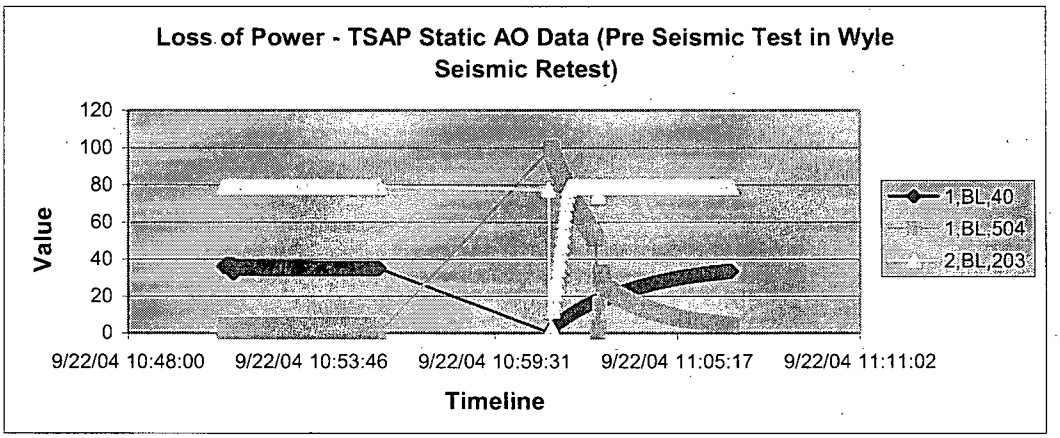

Figure 0.8-2. **Static Analog Data During Loss of Power Test from Pre Seismic Test in Wyle Seismic Retest.**

Figure A.8-3 illustrates the effect of power loss on the digital points as logged by the SOE. During power loss period, digital points from TSAP (4,DI,2, 4,DI,3, 4,DI,9, 4,DI,10, 4,DI,11, and 4,DI,12) transitioned to their default logic state of 0 (false) as expected, and no further transition was logged until power was restored. The reason why 4,DI,8 (HPAT output for digital response time test) was not logged is because the excitation power for this signal came from the TSAP. As a result, when power was cut off from the TSAP, the power for this signal was also cut off. Because the logic state for 4,DI,8 was controlled by the HPAT, the signal was restored as soon as the 48 vdc excitation power became available from the Test Specimen. After the power was restored, all log digital data resumed with the next point transition to 1 (true) because SOE logger logs the transition only when state change occurs. As shown in the Figure A-27, 4,DI,8 resumed activity several cycles earlier than the rest of SOE logged digital points.

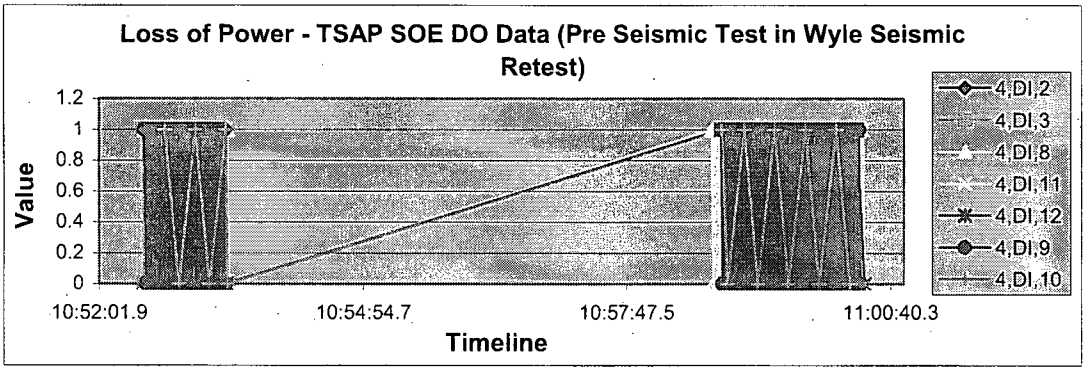

Figure 08-3. **Digital Data from SOE Logger During Loss of Power Test of Pre Seismic Test in Wyle Seismic Retest.**

Figure A.8-4 illustrates the effect of power loss on the digital points as logged by HAS logger during the pre seismic test. 2,DI,161 (1,DO,401) is the trip output signal from analog response time test and 2,DI,155 (1,DO,647) is the uncontrolled TSAP logic. The last HAS logged state for these two points happened to be at the "OFF" state before the power was cut and the test C-Link communication was unavailable. The points remained at that state until the power was recovered and operation was restarted.

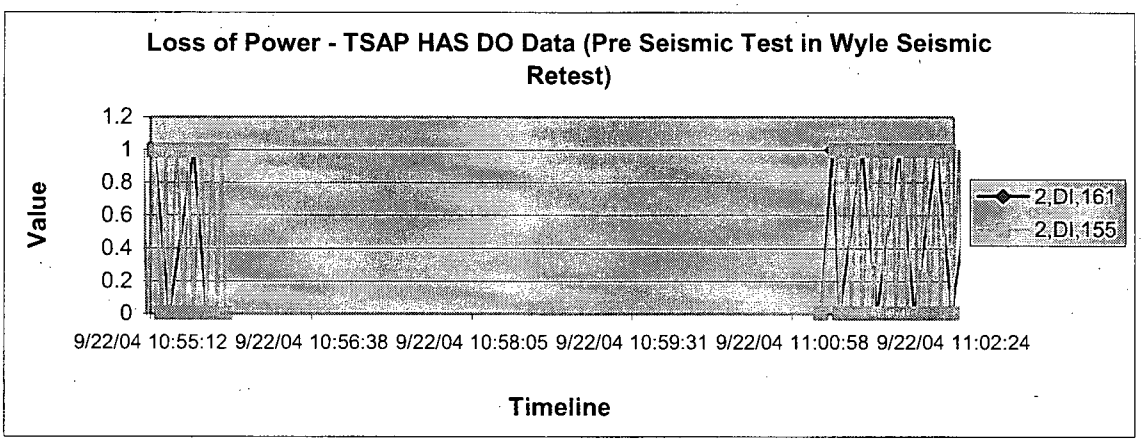

Figure 08-4. **Digital Data from HAS Logger During Loss of Power Test of Pre Seismic Test in Wyle Seismic Retest.**

A.8.2 Post Seismic Test

Figure A.8-5 and Figure A.8-6 illustrate the response of the analog output signals during the loss of power test for the post seismic test. For both dynamic and static analog outputs, the signals remained at their power-off state (0%) until the power was returned. The explanation for the spike seen for AO accuracy test output 2,BL,211 before the restart of the operation was not determined, however due to the short duration and random nature it is considered to be not significant to a seismic event.

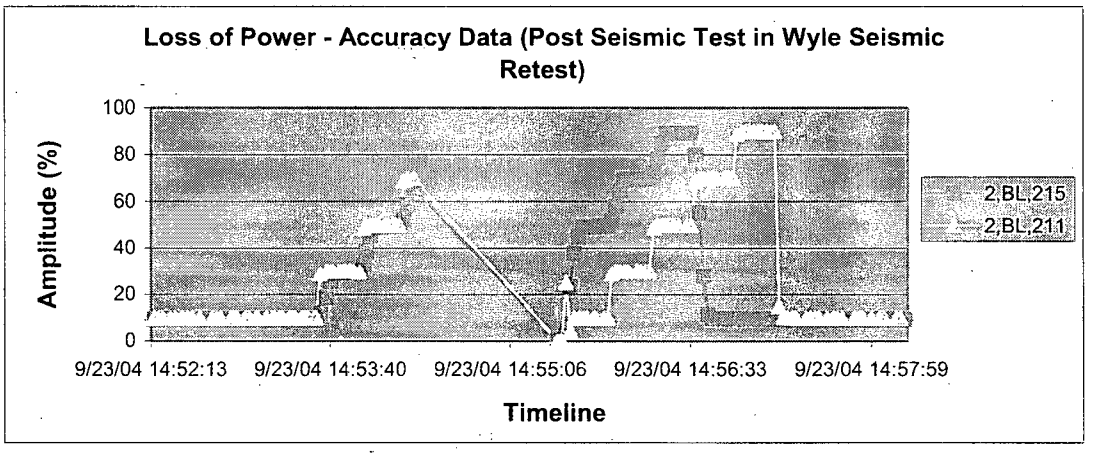

Figure 08-5. **Dynamic Analog Data During Loss of Power Test from Post Seismic Test in Wyle Seismic Retest.**

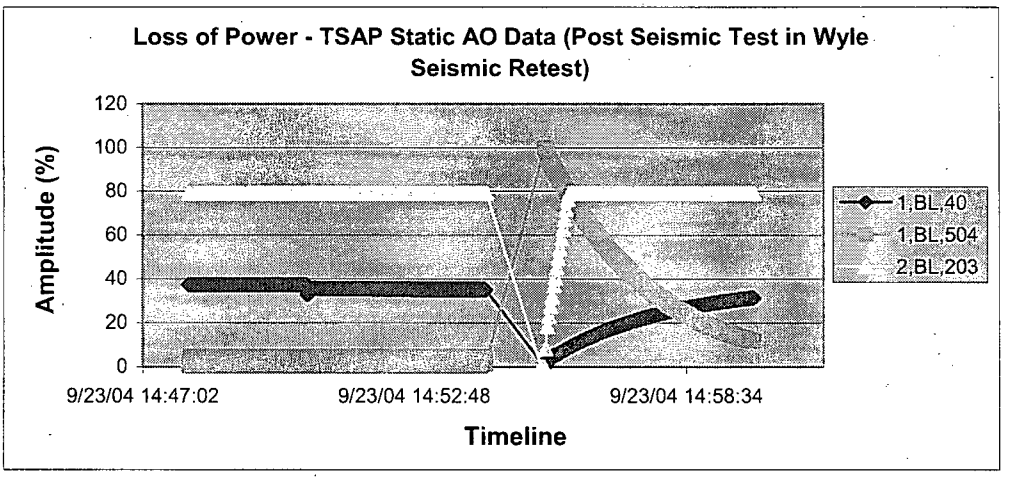

Figure 08-6. **Static Analog Data During Loss of Power Test from Post Seismic Test in Wyle Seismic Retest.**

Figure A.8-7 illustrates the effect of power loss on the digital points as logged by the SOE. During power loss period, digital points from TSAP (4,DI,2, 4,DI,3, 4,DI,9, 4,DI,10, 4,DI,11, and 4,DI,12) transitioned to their default logic state of 0 (false) as expected, and no further transition was logged until power was restored. The reason why 4,DI,8 was not logged is because the excitation power for this signal came from the TSAP. As a result, when power was cut off from the TSAP, the power for this signal was also cut off. Because the logic state for 4,DI,8 was controlled by the HPAT, the signal was restored as soon as the 48 vdc excitation power became available from the Test Specimen. After the power was restored, all log digital data resumed with the next point transition to 1 (true) because SOE logger logs the transition only when state change

occurs. As shown in the figure, 4,DI,8 resumed activity several cycles earlier than the rest of SOE logged digital points.

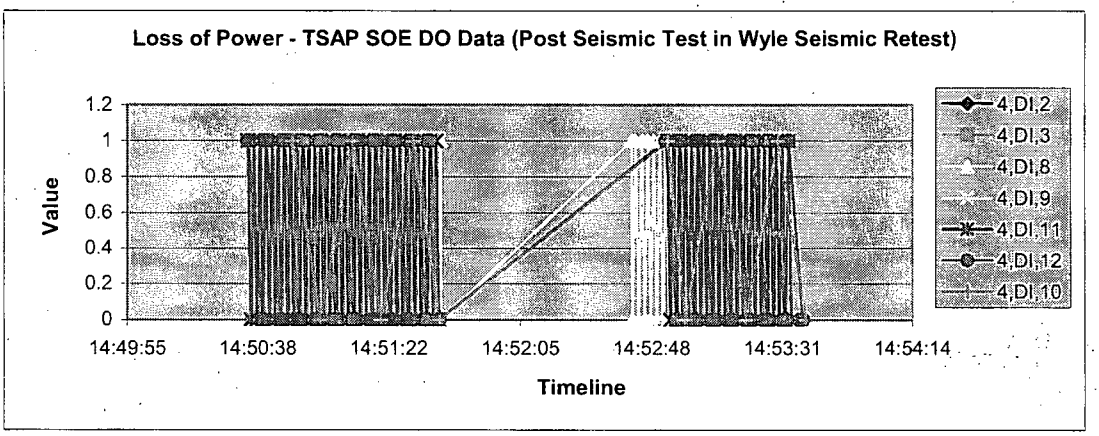

Figure 08-7. **Digital Data from SOE Logger During Loss of Power Test of Post Seismic Test in Wyle Seismic Retest.**

Figure A.8-8 illustrates the effect of power loss on the digital points as logged by HAS logger during the post seismic test. The figure shows that the last state for these two signals were at "1" before the loss of power. This is normal because the test C-Link was lost after power was cut, and due to DDB delays the HAS logger could not have logged that these two points returned to their deenergized state of "0". The HAS data did show that on return of the power the initial state of these two points were at "0" as expected.

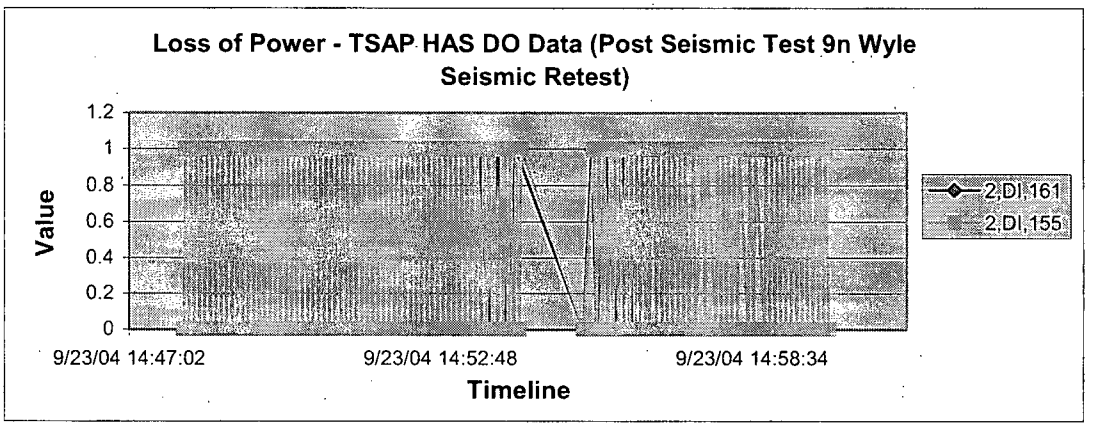

Figure 08-8. **Digital Data from HAS Logger During Loss of Power Test of Post Seismic Test in Wyle Seismic Retest.**

A.9 POWER INTERRUPTION OPERABILITY TEST

The Power Interruption Test was conducted during pre seismic and post seismic testing. This test verified that when a 40 ms power interruption to the Test Specimen was triggered the system responded as follows:

- None of the processors reset
- No static DO channels change state
- None of the static AO channels change their output signal by more than 5%
- Logged parameters of all automated tests remain within tolerance

The power source to the Test Specimen was connected to a timer relay, which was configured to a switch that interrupted power flow to the Test Specimen for a fixed interval of 40 ms. A power interruption was triggered twice. First, the 40 ms power interruption was introduced with all power supply modules in the test specimen. Second, the power interruption was introduced with half of the power supply modules not operable.

To verify the system responded as designed, a series of HAS and SOE automated background tests logged data before, during, and after both power interruptions were introduced. The HAS data recorded included accuracy, response time, Burst of Events (BOE), and the timer.

The static DI and AI logged points corresponded to the static DO and AO points; therefore, the recorded transitions of all static input points were representative of all static output points. The SOE results represented the transition states of all digital static points. TC, RTD, TA05, TO06 thru TO09, and TO05 was the static digital and analog data recorded from HAS.

The static points logged in the HAS ramped up to an initial value. Once the static points reach the initial value, there should have been no transition of more than 5% throughout testing. The SOE logged the dynamic and static digital transitions. In addition, none of the static digital states should change states throughout testing.

A.9.1 Pre Seismic Test

Figures A.9-1, A.9-2, and A.9-3 illustrate the response of the analog signals during the power interruption test of pre seismic test. 1,BL,1 (2,AO,41) is a static signal from the TA05 valve controller. For both the dynamic and static analog outputs, the signals showed that the controller either partially reset or completely reset during the power interruption test. This is discussed further in the main body of this report including the corrective action for the resetting.

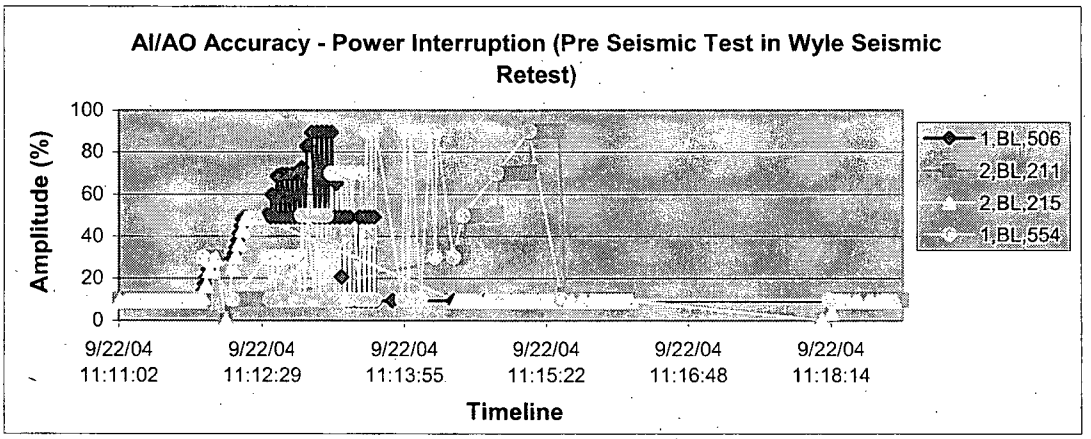

Figure 09-1. **Dynamic Analog Data During Power Interruption Test from Pre Seismic Test in Wyle Seismic Retest.**

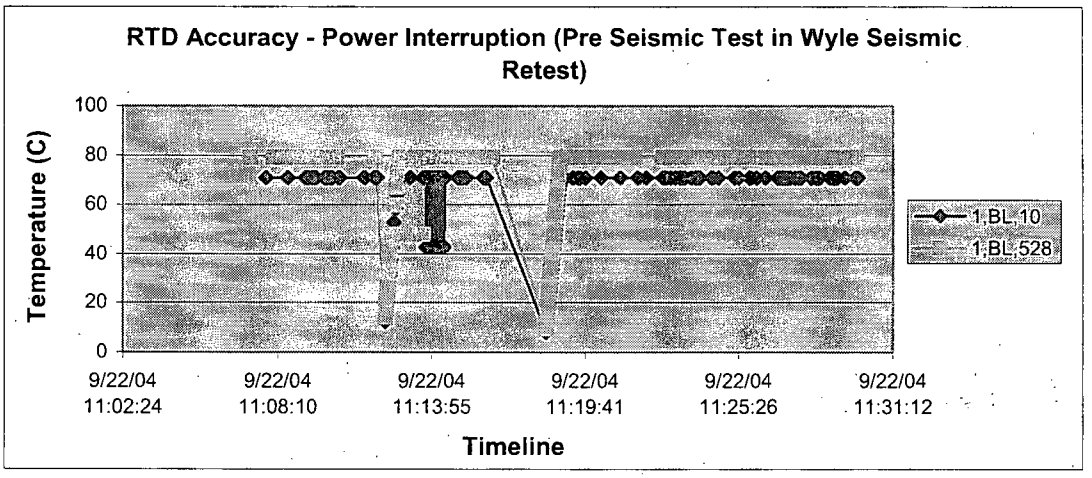

Figure 09-2. **RTD Data During Power Interruption Test from Pre Seismic Test in Wyle Seismic Retest.**

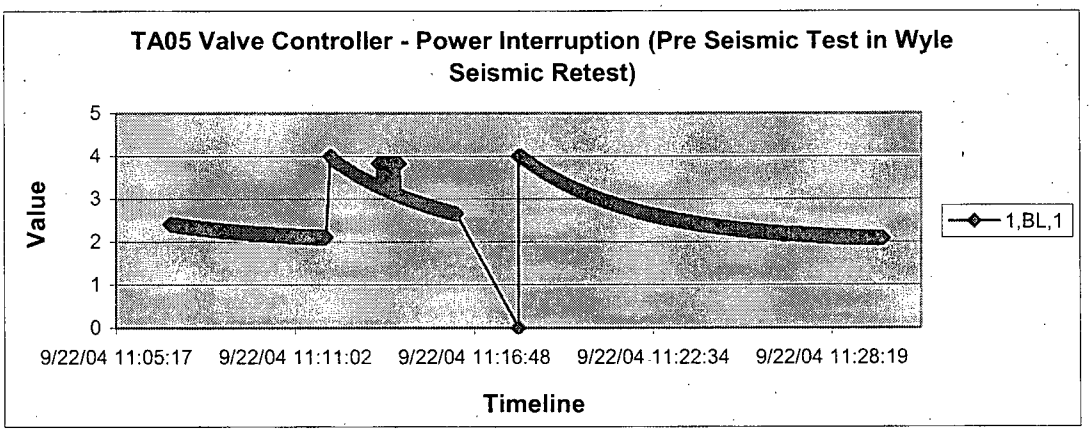

Figure 09-3. **Static Analog Data During Power Interruption Test from Pre Seismic Test in Wyle Seismic Retest.**

Figure A.9-4 illustrates the effect of power interruption on the digital points as logged by the SOE. The 4,DI,8 was not affected by the power interruption to TSAP. The timeframe in SOE data corresponds to the first disruption shown in Figures A.9-1 through A.9-3. The short disruption demonstrates that the power interruption introduced at that particular moment did not bring down the entire system.

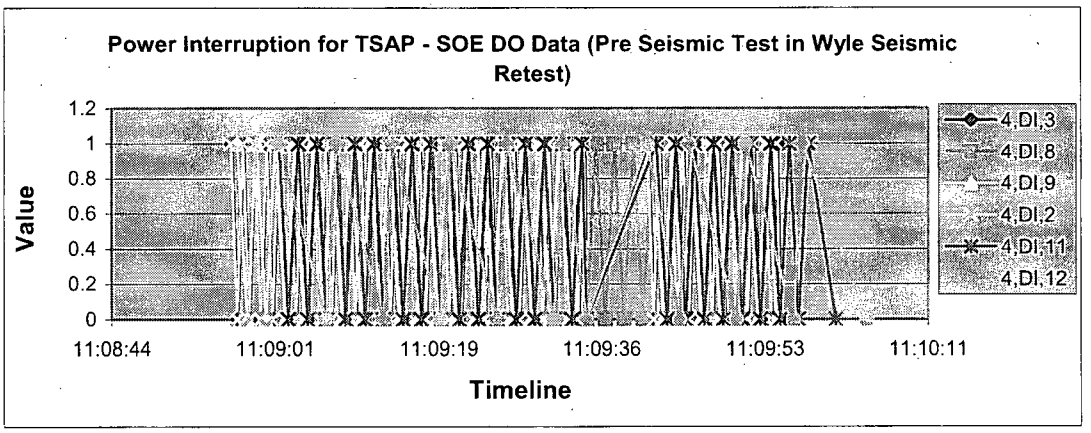

Figure 09-4. **Digital Data from SOE Logger During Power Interruption Test of Pre Seismic Test in Wyle Seismic Retest.**

A.9.2 Post Seismic Test

Figures A.9-5 and Figure A.9-6 illustrate the response of the analog signals during the power interruption test of post seismic test. Similar to pre seismic test, signals from both dynamic and static analog outputs show the controller either partially reset or completely reset during the power interruption test. The seismic stress tests did not alter the system response.

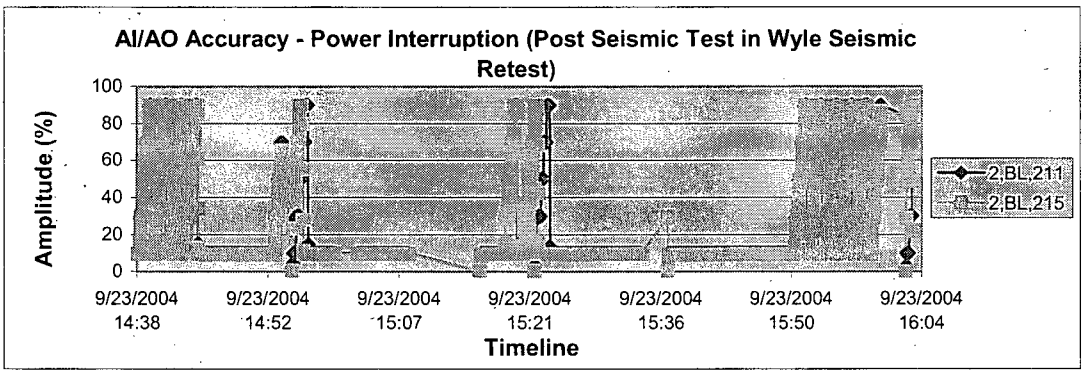

Figure 09-5. **Dynamic Analog Data During Power Interruption Test from Post Seismic Test in Wyle Seismic Retest.**

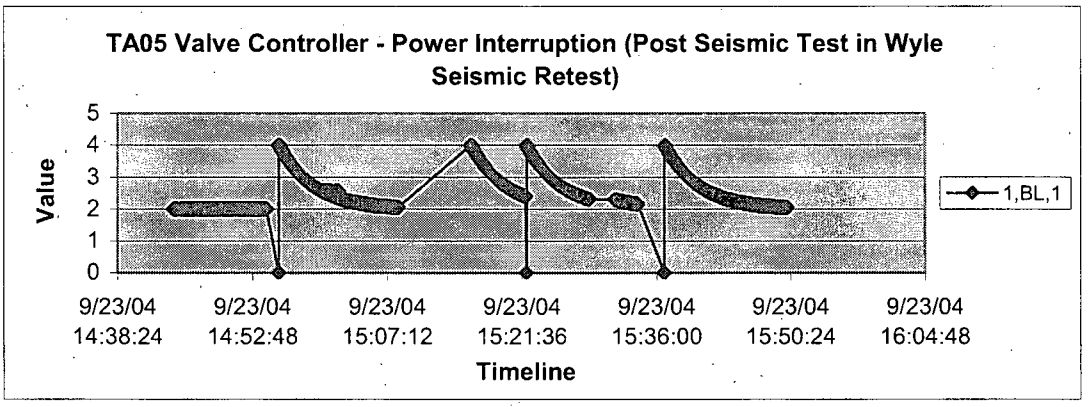

Figure 09-6. **Static Analog Data During Power Interruption Test from Post Seismic Test in Wyle Seismic Retest.**

A.10 POWER QUALITY OPERABILITY TEST

The power quality tolerance test results during the post seismic test are listed in Table A.10-1. The two power modules A and B from TSAP meet the ±1% acceptance criteria at both the low voltage and high voltage tests. At the low voltage test, TSAP dropped out at 77-76 Vac. The power supply recovered from the under voltage condition automatically. Since the under voltage condition brought down the entire system, no system status alarm was logged after the power trip. At high voltage test, no system trip was observed up to the limit of the power source: 276 Vac. Lastly, by inspecting the HAS data for power supply alarm flags, it is concluded that no power supply dropout alarm occurred while source power was within the specified range (90-150 Vac and 57-63 Hz).

Table 010-1. TSAP Power Quality Tolerance Test Results from Post Seismic Test.

Power Feed	Power Module A				Power Module B			
	24-vdc	Deviation (%)	48 vdc	Deviation (%)	24 vdc	Deviation (%)	48 vdc	Deviation (%)
120 vac 60 Hz								
90 vac 57 Hz								
90 vac 63 Hz								
90 vac 63 Hz								
< 60 vac								
120 vac 60 Hz								
150 vac 57 Hz								
150 vac 63 Hz								
150 vac 63 Hz								
> 270 vac (276 vac)								

A.11 DIGITAL BOE TEST

A.11.1 Pre Seismic Test

SOE data from the baseline pre-seismic stress test was analyzed. It is concluded that all transitions were detected for all 5 logged digital channels (4,DI,28, 4,DI,32 through 4,DI,35). By analyzing the alarm reports throughout the seismic test, it is concluded that no link alarm conditions were detected for the DI cards.

All transitions and the associated timestamps are listed in Table A.11-1. The transition at the end of the test at around 10:15:35 AM, happened to all monitored digital channels. This event is caused by the perturbation from stopping the BOE test and thus is not be counted as the irregular transition. This did not impact the validity of the seismic tests.

Excluding the occurrences of the transitions caused by the stopping of the BOE test, all of the rest of the transitions had a transition time that was within acceptance range.

Table 01-1. **Digital BOE Abnormal Transitions in the Pre Seismic Test.**

Time Stamp			Transition Time Duration (Seconds)				
H	M	S	4,DI,28	4,DI,32	4,DI,33	4,DI,34	4,DI,35
10	15	34.79					
Total No. of Transitions							
Total No. of Contact Bounce							
Total No. of Anomalies							

A.11.2 OBE1 Test

SOE data from the OBE1 test was analyzed. It is concluded that all transitions were detected for all 5 logged digital channels (4,DI,28, 4,DI,32 through 4,DI,35). By analyzing the alarm reports throughout the seismic test, it is concluded that no link alarm conditions were detected for the DI cards whose channels were logged by SOE logger.

A.11.3 OBE2 Test

SOE data from OBE2 test was not available. Two of the digital BOE points, 1,DO,385 and 1,DO,387, were logged by the Wyle chatter box. By inspection of the chatter box recorder data, it is concluded that the response time from these two points were within 0.85-1.15 seconds.

A.11.4 OBE3 Test

SOE data from the OBE3 test was analyzed. It is concluded that all transitions were detected for all 5 logged digital channels (4,DI,28, 4,DI,32 through 4,DI,35). By analyzing the alarm reports throughout the seismic test, it is concluded that no link alarm conditions were detected for the DI cards whose channels were logged by SOE logger.

A.11.5 OBE4 Test

SOE data from the pre-seismic stress test was analyzed. It is concluded that all transitions were detected for all 5 logged digital channels (4,DI,28, 4,DI,32 through 4,DI,35). By analyzing the alarm reports throughout the seismic test, it is concluded that no link alarm conditions were detected for the DI cards whose channels were logged by SOE logger.

All transitions and the associated timestamps are listed in Table A.11-2. The transitions occurred at the end of the test, i.e., at around 9:38:18 AM. This anomaly is caused by the perturbation from stopping the BOE test and thus should not be counted as the irregular transition.

Excluding the occurrences of the transitions caused by the stopping of BOE test, all the rest of transitions had a transition time that was within acceptance range.

Table 01-2. **Digital BOE Abnormal Transitions in the OBE4 Test.**

Time Stamp			Transition Time Duration (Seconds)				
H	M	S	4,DI,28	4,DI,32	4,DI,33	4,DI,34	4,DI,35
9	38	18.65					
9	38	19.72					
Total No. of Transitions							
Total No. of Contact Bounce							
Total No. of Anomalies							

A.11.6 OBE5 Test

SOE data from the pre-seismic stress test was analyzed. It is concluded that all transitions were detected for all 5 logged digital channels (4,DI,28, 4,DI,32 through 4,DI,35). By analyzing the alarm reports throughout the seismic test, it is concluded that no link alarm conditions were detected for the DI cards whose channels were logged by SOE logger.

All transitions and the associated timestamps are listed in Table A.11-3. The transition at the end of the test, i.e., at around 9:54:13 AM, happened to all monitored digital channels. This is caused by the perturbation from stopping the BOE test and thus should not be counted as the irregular transition.

Excluding the occurrences of transitions caused by the stopping of BOE test, all the rest of transitions had a transition time that was within acceptance range.

Table 0-3. **Digital BOE Transitions in the OBE4 Test.**

Time Stamp			Transition Time Duration (Seconds)				
H	M	S	4,DI,28	4,DI,32	4,DI,33	4,DI,34	4,DI,35
9	54	13.41					
Total No. of Transitions							
Total No. of Contact Bounce							
Total No. of Anomalies							

A.11.7 SSE Test

SOE data from the SSE test was analyzed. It is concluded that all transitions were detected for all 5 logged digital channels (4,DI,28, 4,DI,32 through 4,DI,35). By analyzing the alarm reports throughout the seismic test, it is concluded that no link alarm conditions were detected for the DI cards whose channels were logged by SOE logger.

A.11.8 Post Seismic Test

SOE data from the post seismic test was analyzed. It is concluded that all transitions were detected for all 5 logged digital channels (4,DI,28, 4,DI,32 through 4,DI,35). By analyzing the alarm reports throughout the seismic test, it is concluded that no link alarm conditions were detected for the DI cards whose channels were logged by SOE logger.

A.12 Analog BOE Test

A.12.1 Pre Seismic Test

The waveforms of TSAP analog inputs at remote 1 and that of the BOE source signal during the pre seismic test of seismic retest are depicted in Figure A.12-1. The TSAP AI signals correlate well with the BOE source signal at each transition and they essentially overlap with one another. Table A.12-1 lists the average readings and the deviation of 15 measurements for these HAS logged AI signals at 10% and 90% levels. The calculation of deviation is based on 9.694% for 10% and 89.306% for 90%. Both 1,BL,510 and 1,BL,516 deviate less than 0.32% from the BOE source signal at both 10% and 90% levels. The magnitude of deviations is comparable to the in-house baseline test results.

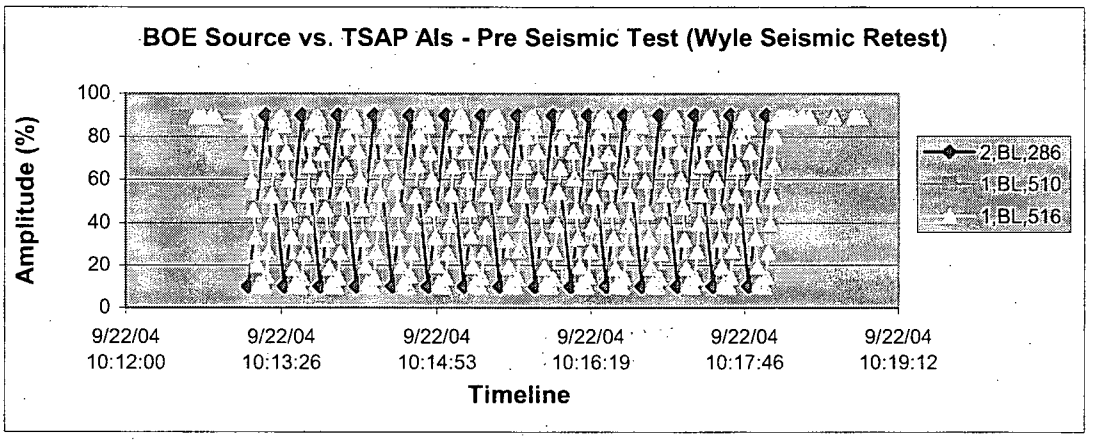

Figure 02-1. **BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from Pre Seismic Test for Seismic Retest.**

Table 02-4. **TSAP AI Channel Readings and Deviations from BOE Source Signal from Pre Seismic Test for Seismic Retest.**

	1,AI,882 (1,BL,510)	1,AI,901 (1,BL,516)
10% Measurement (%)		
Deviation From 10% (%)		
No. of Measurements		
90% Measurement (%)		
Deviation From 90% (%)		
No. of Measurements		

Figure A.12-2 shows the waveforms for TSAP AO (2,BL,213) versus its corresponding TSAP AI (1,BL,510) during the pre seismic test for seismic retest. The AO image duplicates the AI image at each transition. The averaged readings and deviations for these two analog signals at 10% and 90% levels are listed in Table A.12-2. At 10% level, 2,BL,213 deviates from 1,BL,510 by 0.283% and thus meets the 0.3% acceptance criteria. The average deviation at 90% level is 0.383%, which is slightly out of the 0.30% acceptance criteria but is comparable to the in-house baseline result of 0.327%. The higher deviation at 10% level is probably caused by HAS logging issues: 1) Due to a set-up issue for HPAT tester, 2,BL,213 was logged every two seconds (Figure A.12-3), compared to the 1 second logging of 1,BL,510; 2) At different tests, the points logged at each transition cycle differed slightly as listed in Table A.12-3.

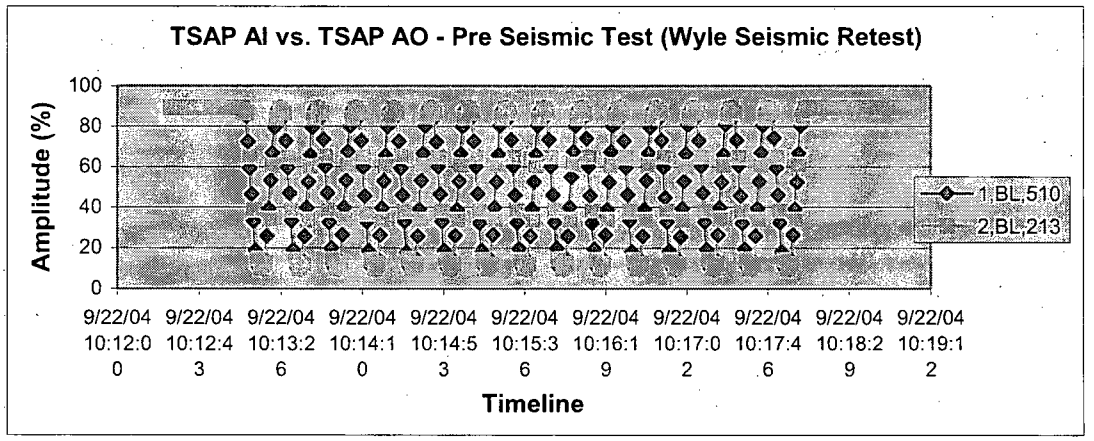

Figure 0-2 **TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) from Pre Seismic Test for Seismic Retest.**

Table 02-5. **TSAP AO and the Corresponding TSAP AIs in Remote1 from Pre Seismic Test for Seismic Retest.**

	1,BL,510	2,BL,213	Deviation (2,BL,213 from 1,BL,510)	3,BL,1	2,BL,291	Deviation (2,BL,291 from 3,BL,1)
10% Measurement						
No. of Measurements						
90% Measurement						
No. of Measurements						

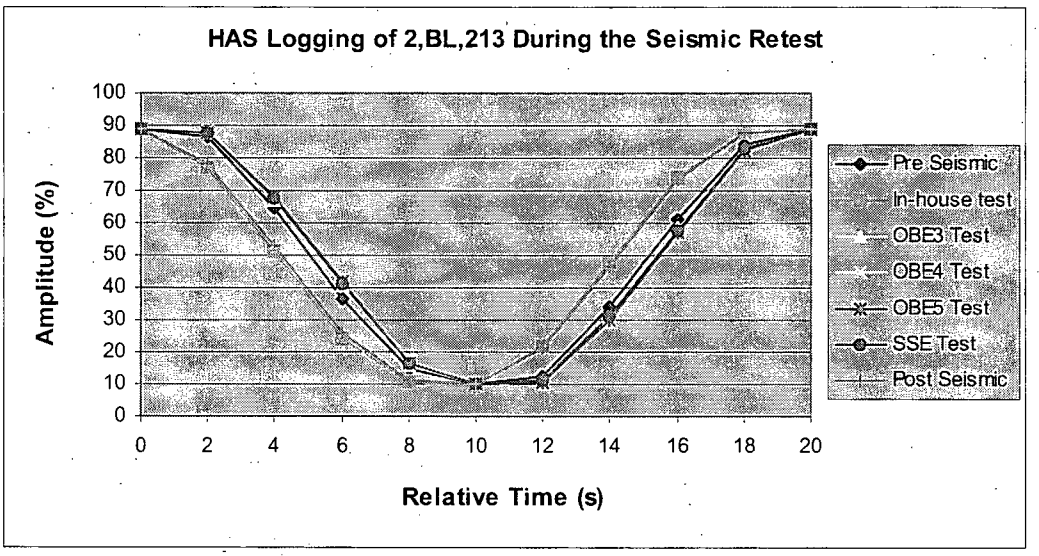

Figure 02-3. **HAS Logging of 2,BL,213 During Different Tests of Seismic Retest.**

Table A.12-3 **Logging Variations of 2,BL,213 During Different Tests of Seismic Retest.**

	In-house Test	Pre Seismic Test	OBE3 Test	OBE4 Test	OBE5 Test	SSE Test	Post Seismic Test
Minimum Reading (%)							
Maximum Reading (%)							

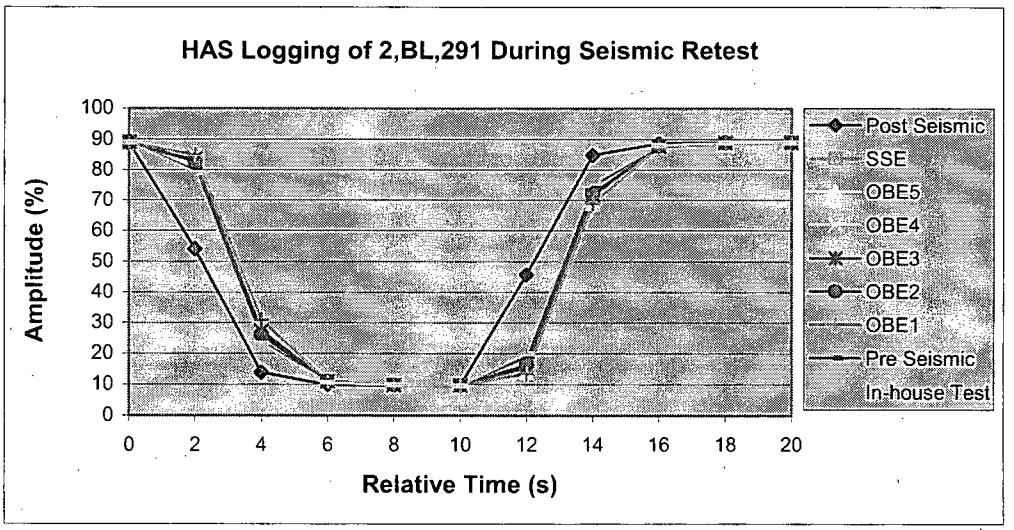

Figure 02-4. **HAS Logging of 2,BL,291 During Different Tests of Seismic Retest.**

Figure A.12-3 shows the response time of 2,BL,213 is greater than 8 seconds, the last point logged for each cycle at both 10% or 90% level may not be the steady-state values, which is the largest source of the deviations. The logging variations at different tests as demonstrated in Table A.12-3 is likely a consequences of HAS logging issues as discussed above. As shown in Figure A.12-4, since the response time of 2,BL,291 is ~6 seconds, the steady-state values were thus logged by HAS. As a result, much better results were obtained for SLC AI/AO test as it is shown in Table A.12-2. Although the SLC is not part of the qualification it was a valid driver of inputs to test the AI/AO cards.

Figure A.12-5 shows the BOE source signal (2,BL,286) versus TSAP AI signal (3,BL,1) as well as the TSAP AO signal (2,BL,291) at single loop controller (remote 3) during the pre seismic test for seismic retest. The 3,BL,1 waveform duplicates the BOE source at each transition and the waveforms for 2,BL,291 and 3,BL,1 track each other at each transition. The averaged readings and deviations of 15 measurements for 3,BL,1 and 2,BL,291 at the 10% and 90% levels are provided in Table A.12-2. The results indicate that 2,BL,291 deviates less than 0.3% from 3,BL,1 at both levels, and the magnitude of deviations is comparable to in-house test results: 0.069% vs. 0.058% at 10%, 0.157% vs. 0.131% at 90%.

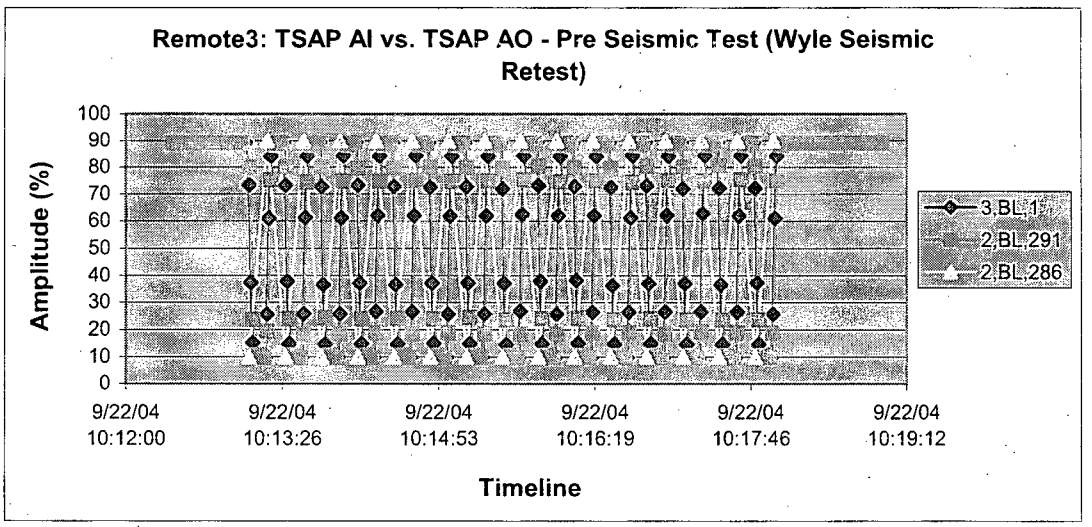

Figure 0-5. ***Single Loop Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO from Pre Seismic Test for Seismic Retest***

A.12.2 OBE1 Test

The waveforms of TSAP analog inputs at remote 1 and that of the BOE source signal during the OBE1 test of seismic retest are depicted in Figure A.12-6. This Figure shows that the TSAP AI signals correlate well with the BOE source signal at each transition and they essentially overlap with one another. Table A.12-4 lists the averaged readings and deviations of 13 and 14 measurements for 1,BL,516 at 10% and 90% levels respectively. The HAS data for 1,BL,510 was lost. The calculation of deviation was based on 9.694% for 10% and 89.306% for 90%. The 1,BL,516 deviate less than 0.32% from the BOE source signal at both 10% and 90% levels. The magnitude of deviations is higher than

the in-house baseline test results at 10% level: 0.040% vs. 0.01%; magnitude at 90% level is comparable: 0.179% vs. 0.096%.

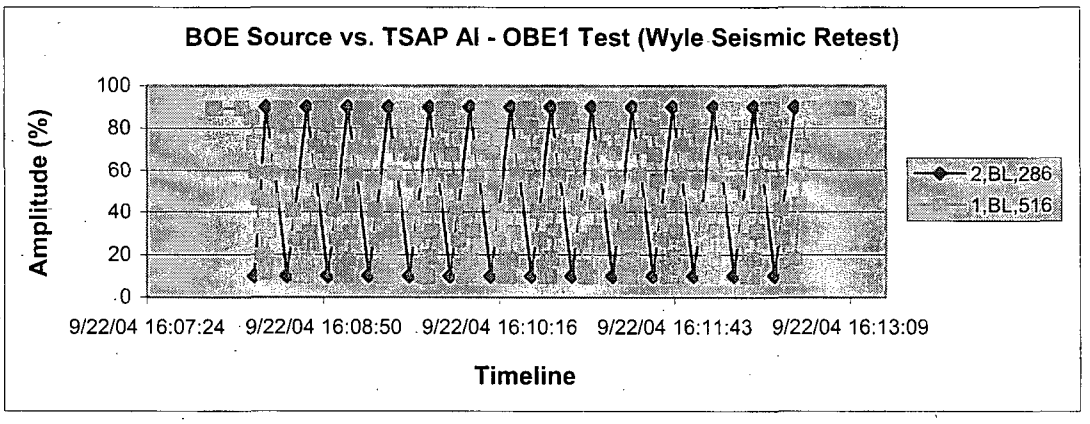

Figure 0-6. **BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from OBE1 Test for Seismic Retest.**

Both 1,BL,510 and 2,BL,213 were not logged during the OBE1 test, therefore the TSAP AI and TSAP AO comparison is not available for Remote 1.

Table 012-4. **TSAP AI Channel Readings and Deviations from BOE Source Signal from OBE1 Test for Seismic Retest.**

	1,AI,882 (1,BL,510)	1,AI,901 (1,BL,516)
10% Measurement (%)		
Deviation From 10% (%)		
Num of Measurements		
90% Measurement (%)		
Deviation From 90% (%)		
Num of Measurements		

Table 012-5. **TSAP AOs and the Corresponding TSAP AIs in Remote1 from OBE1 Test for Seismic Retest.**

	3,BL,1	2,BL,291	Deviation (2,BL,291 from 3,BL,1)
10% Measurement (%)			
No. of Measurements			
90% Measurement (%)			
No. of Measurements			

Figure A.12-7 shows the BOE source signal (2,BL,286) versus TSAP AI signal (3,BL,1) as well as the TSAP AO signal (2,BL,291) at test controller (remote 3) during OBE1 test for seismic retest. The 3,BL,1 waveform duplicates the BOE source at each transition and the waveforms for 2,BL,291 and 3,BL,1 track each other at each transition. The averaged readings and deviations of 13 and 14 measurements for 3,BL,1 and 2,BL,291 at the 10% and 90% levels respectively are provided in Table A.12-5. The results indicate that 2,BL,291 deviates less than 0.3% from 3,BL,1 at both levels, and the magnitude of deviations is comparable to in-house baseline test results: 0.067% vs. 0.058% at 10%, 0.161% vs. 0.131% at 90%.

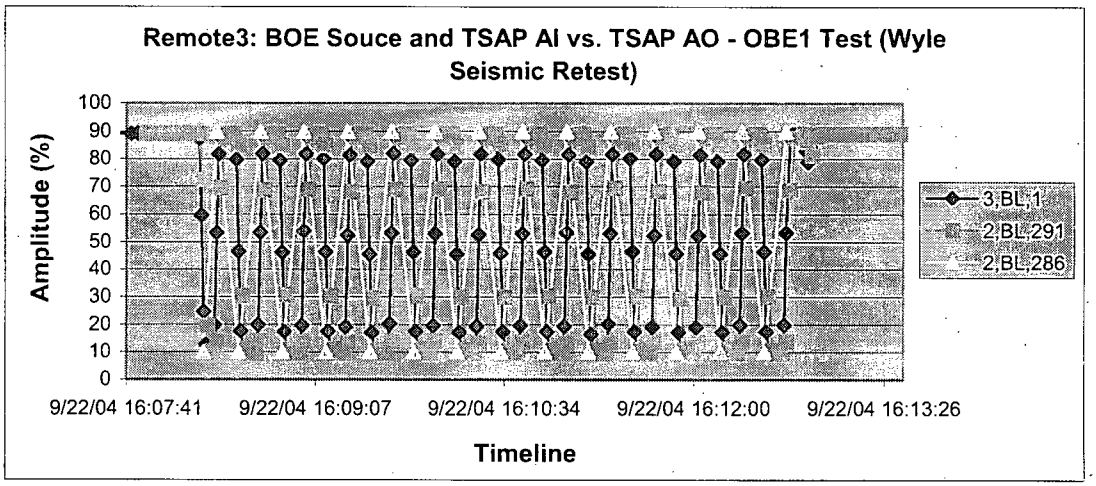

Figure 02-7. **Test Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO from OBE1 Test for Seismic Retest.**

A.12.3 OBE2 Test

The waveforms of TSAP analog inputs at remote 1 and that of the BOE source signal during the OBE2 test of seismic retest are depicted in Figure A.12-8. This Figure shows that the TSAP AI signals correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table A.12-6 lists the averaged readings and deviations of 14 and 15 measurements for 1,BL,516 at 10% and 90% levels respectively. The HAS data for 1,BL,510 was lost. The calculation of deviation is based on 9.694% for 10% and 89.306% for 90%. The 1,BL,516 deviate less than 0.32% from the BOE source signal at both 10% and 90% levels. The magnitude of deviations is higher than the in-house baseline test results at the 10% level: 0.054% vs. 0.01%; the magnitude at 90% level is comparable: 0.134% vs. 0.096%.

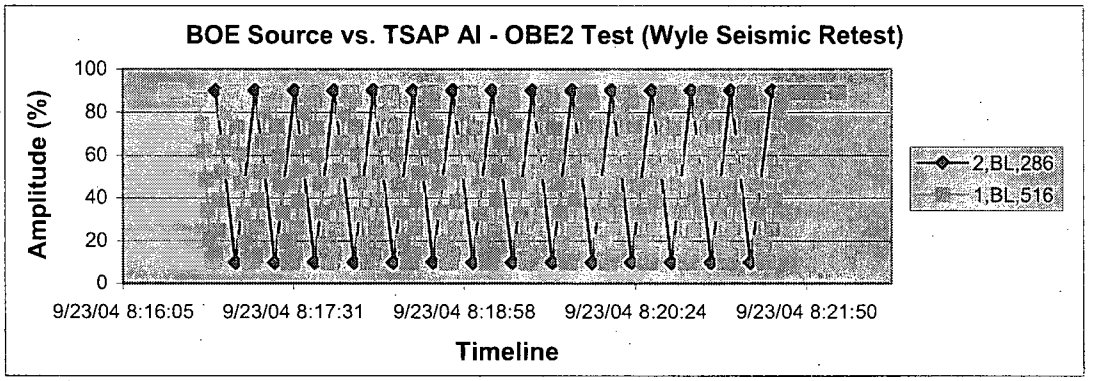

Figure 02-8. **BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from OBE2 Test for Seismic Retest.**

The 1,BL,510 was not logged during the OBE2 test; 2,BL,213 was logged but the values remained constant throughout the test. Therefore the TSAP AI and TSAP AO comparison is not available for Remote 1.

Table 02-6. **TSAP AI Channel Readings and Deviations from BOE Source Signal from OBE2 Test for Seismic Retest.**

	1,AI,882 (1,BL,510)	1,AI,901 (1,BL,516)
10% Measurement (%)		
Deviation From 10% (%)		
No. of Measurements		
90% Measurement (%)		
Deviation From 90% (%)		
No. of Measurements		

Table 02-7. **TSAP AOs and the Corresponding TSAP AIs in Remote1 from OBE2 Test for Seismic Retest.**

	3,BL,1	2,BL,291	Deviation (2,BL,291 from 3,BL,1)
10% Measurement (%)			
No. of Measurements			
90% Measurement (%)			
No. of Measurements			

Figure A.12-9 shows the BOE source signal (2,BL,286) versus TSAP AI signal (3,BL,1) as well as the TSAP AO signal (2,BL,291) at test controller (remote 3) during OBE2 test for seismic retest. The 3,BL,1 waveform duplicates the BOE source at each transition and the waveforms for 2,BL,291 and 3,BL,1 track each other at each transition. The averaged readings and deviations of 15 measurements for 3,BL,1 and 2,BL,291 at the

10% and 90% levels are provided in Table A.12-7. The results indicate that 2,BL,291 deviates less than 0.3% from 3,BL,1 at both levels, and the magnitude of deviations is comparable to in-house test results: 0.067% vs. 0.058% at 10%, 0.154% vs. 0.131% at 90%.

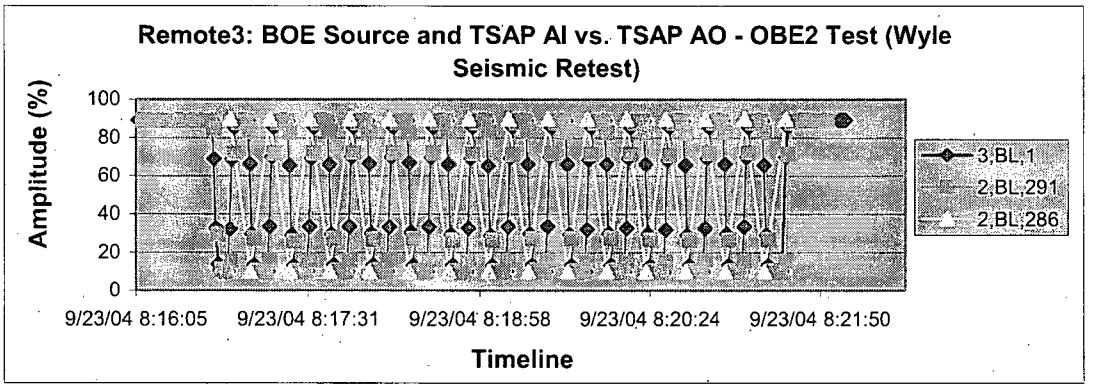

Figure 02-9. **Single Loop Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO from OBE2 Test for Seismic Retest.**

A.12.4 OBE3 Test

The waveforms of TSAP analog inputs at remote 1 and that of the BOE source signal during the OBE3 test of seismic retest are depicted in Figure A.12-10. The figure shows that the TSAP AI signals correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table A.12-8 lists the averaged readings and deviations for 12 measurements for the HAS logged AI signals at 10% and 90% levels. The calculation of the deviation was based on 9.694% for 10% and 89.306% for 90%. Both the 1,BL,510 and 1,BL,516 deviate less than 0.32% from the BOE source signal at both 10% and 90% levels. The magnitude of the deviations is higher than the in-house baseline test results at 10% level: 0.023% vs. 0.005% for 1,BL,510, and 0.049% vs. 0.01% for 1,BL,516; magnitude at 90% level is comparable: 0.069% vs. 0.045% for 1,BL,510, and 0.132% vs. 0.096% for 1,BL,516.

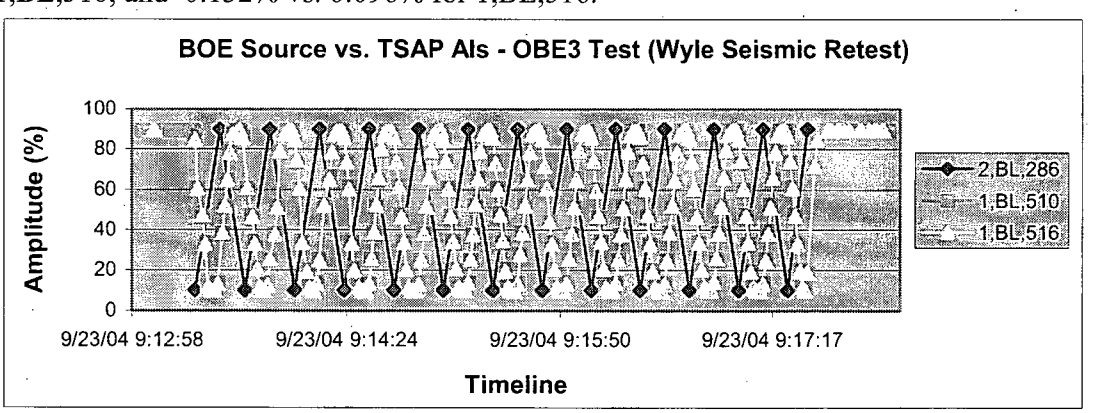

Figure 02-10. **BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from OBE3 Test for Seismic Retest.**

Figure A.12-11 shows the waveforms for TSAP AO (2,BL,213) versus its corresponding TSAP AI (1,BL,510) during the OBE3 test for seismic retest. The figure shows that the AO image duplicates the AI image at each transition. The averaged readings and deviations for these two analog signals at 10% and 90% levels are listed in Table A.12-9. Deviations of 2,BL,213 from 1,BL,510 by 0.283% at both 10% and 90% levels were out of the acceptance range. The deviations at 10% and 90% levels are 0.370% and 0.438% respectively, compared with 0.115% and 0.327% from the in-house baseline test. The increment at 10% is likely caused by the logging issues with HPAT as explained in the Pre Seismic Test.

Table 02-8. **TSAP AI Channel Readings and Deviations from BOE Source Signal from OBE3 Test for Seismic Retest.**

	1,AI,882 (1,BL,510)	1,AI,901 (1,BL,516)
10% Measurement (%)		
Deviation From 10% (%)		
No. of Measurements		
90% Measurement (%)		
Deviation From 90% (%)		
No. of Measurements		

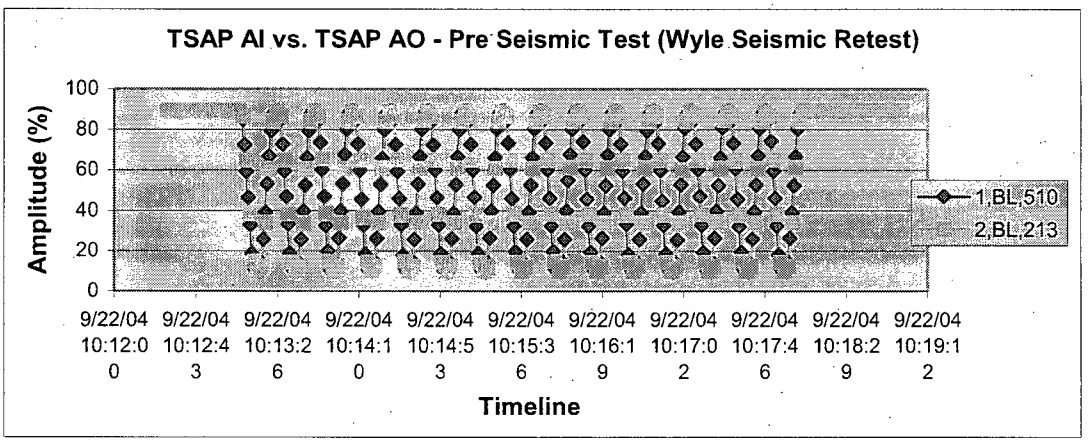

Figure 012-11. **TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) from OBE3 Test for Seismic Retest.**

Table 02-9. **TSAP AOs and the Corresponding TSAP AIs in Remote1 from OBE3 Test for Seismic Retest.**

	1,BL,510	2,BL,213	Deviation (2,BL,213 from 1,BL,510)	3,BL,1	2,BL,291	Deviation (2,BL,291 from 3,BL,1)
10% Measurement						
No. of Measurements						
90% Measurement						
No. of Measurements						

Figure A.12-12 shows the BOE source signal (2,BL,286) versus TSAP AI signal (3,BL,1) as well as the TSAP AO signal (2,BL,291) at test controller (remote 3) during the OBE3 test for seismic retest. The 3,BL,1 waveform duplicates the BOE source at each transition and the waveforms for 2,BL,291 and 3,BL,1 track each other at each transition. The averaged readings and deviations of 12 measurements for 3,BL,1 and 2,BL,291 at the 10% and 90% levels are provided in Table A.12-9. The results indicate that 2,BL,291 deviates less than 0.3% from 3,BL,1 at both levels, and the magnitude of deviations is comparable to in-house baseline test results: 0.062% vs. 0.058% at 10%, 0.139% vs. 0.131% at 90%.

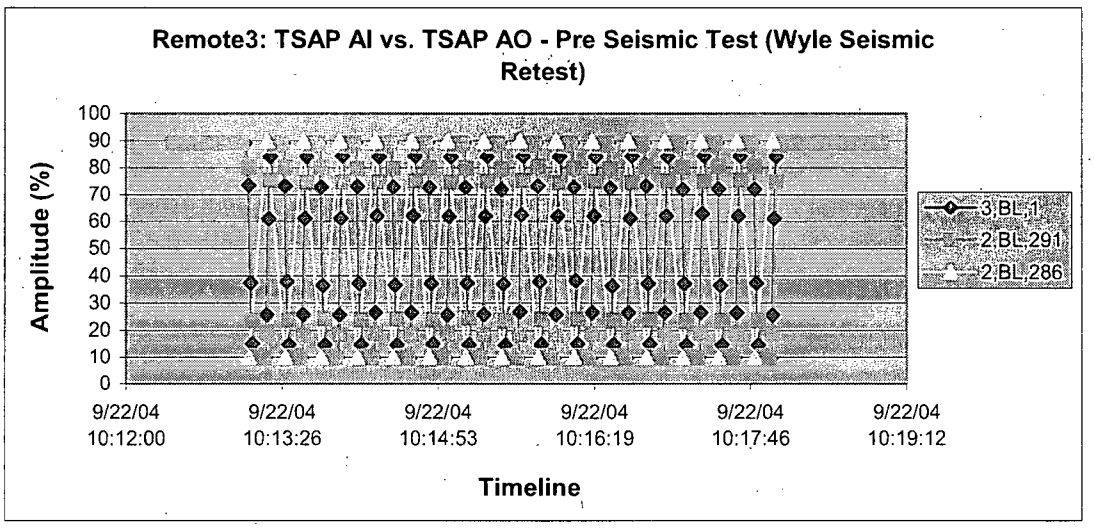

Figure 02-12. **Test Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO from OBE3 Test for Seismic Retest.**

A.12.5 OBE4 Test

The waveforms of TSAP analog inputs at remote 1 and that of the BOE source signal during the OBE4 test of seismic retest are depicted in Figure A.12-13. The figure shows

that the TSAP AI signals correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table A.12-10 lists the averaged readings and deviations of 6 measurements for the HAS logged AI signals at 10% and 90% levels. The calculation of deviation was based on 9.694% for 10% and 89.306% for 90. Both 1,BL,510 and 1,BL,516 deviate less than 0.32% from the BOE source signal at both 10% and 90% levels. The magnitude of deviations is higher than the in-house baseline test results at 10% level: 0.028% vs. 0.005% for 1,BL,510, and 0.046% vs. 0.01% for 1,BL,516; magnitude at 90% level is comparable: 0.078% vs. 0.045% for 1,BL,510, and 0.133% vs. 0.096% for 1,BL,516.

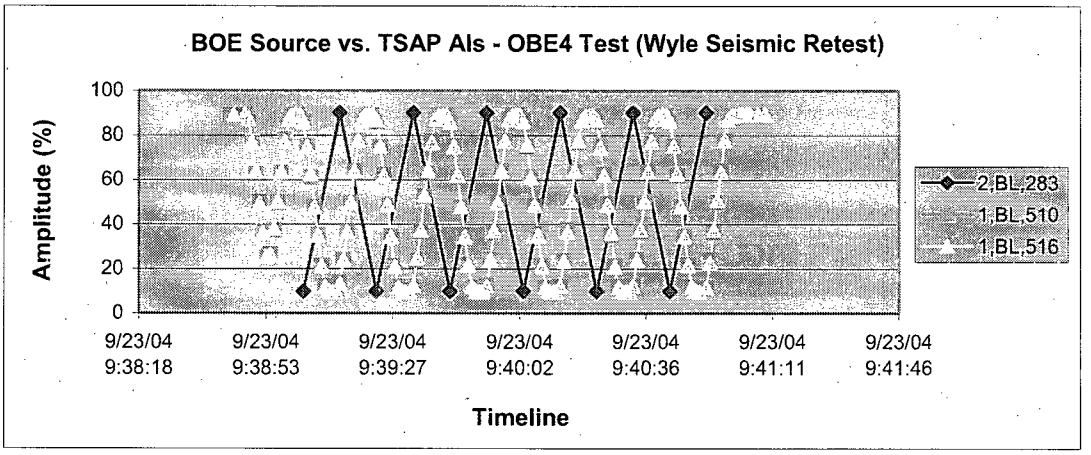

Figure 02-13. **BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from OBE4 Test for Seismic Retest.**

Figure A.12-14 shows the waveforms for TSAP AO (2,BL,213) versus its corresponding TSAP AI (1,BL,510) during OBE4 for seismic retest. The figure shows that the AO image duplicates the AI image at each transition. The averaged readings and deviations for these two analog signals at 10% and 90% levels are listed in Table A.12-11. Deviations of 2,BL,213 from 1,BL,510 by 0.283% at both 10% and 90% levels were out of the acceptance range. The deviations at 10% and 90% levels are 0.430% and 0.483% respectively, compared with 0.115% and 0.327% from the in-house test. The increment at 10% is likely caused by the logging issues with HPAT as explained in the Pre Seismic Test.

Table 02-10. **TSAP AI Channel Readings and Deviations from BOE Source Signal from OBE4 Test for Seismic Retest.**

	1,AI,882 (1,BL,510)	1,AI,901 (1,BL,516)
10% Measurement (%)		
Deviation From 10% (%)		
No. of Measurements		
90% Measurement (%)		
Deviation From 90% (%)		
No. of Measurements		

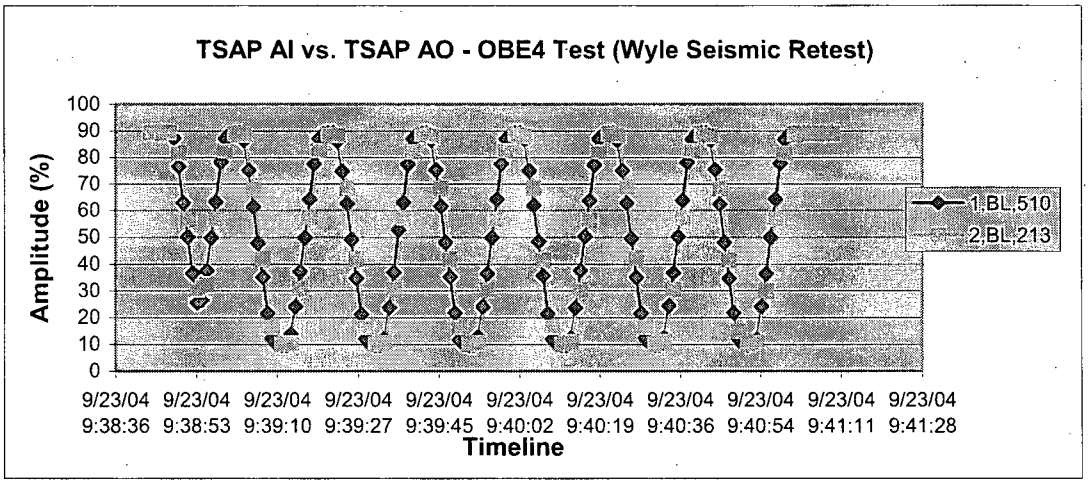

Figure 02-14. **TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) from OBE4 Test for Seismic Retest.**

Table 02-11. **TSAP AOs and the Corresponding TSAP AIs in Remote1 from OBE4 Test for Seismic Retest.**

	1,BL,510	2,BL,213	Deviation (2,BL,213 from 1,BL,510)		3,BL,1	2,BL,291	Deviation (2,BL,291 from 3,BL,1)
10% Measurement							
No. of Measurements							
90% Measurement							
No. of Measurements							

Figure A.12-15 shows the BOE source signal (2,BL,286) versus TSAP AI signal (3,BL,1) as well as the TSAP AO signal (2,BL,291) at the test controller (remote 3) during the OBE4 test for seismic retest. The 3,BL,1 waveform duplicates the BOE source at each transition and the waveforms for 2,BL,291 and 3,BL,1 track each other at each transition. The averaged readings and deviations of 6 measurements for 3,BL,1 and 2,BL,291 at the 10% and 90% levels are provided in Table A.12-11. The results indicate that 2,BL,291 deviates less than 0.3% from 3,BL,1 at both levels, and the magnitude of deviations is comparable to in-house test results: 0.107% vs. 0.058% at 10%, 0.152% vs. 0.131% at 90%.

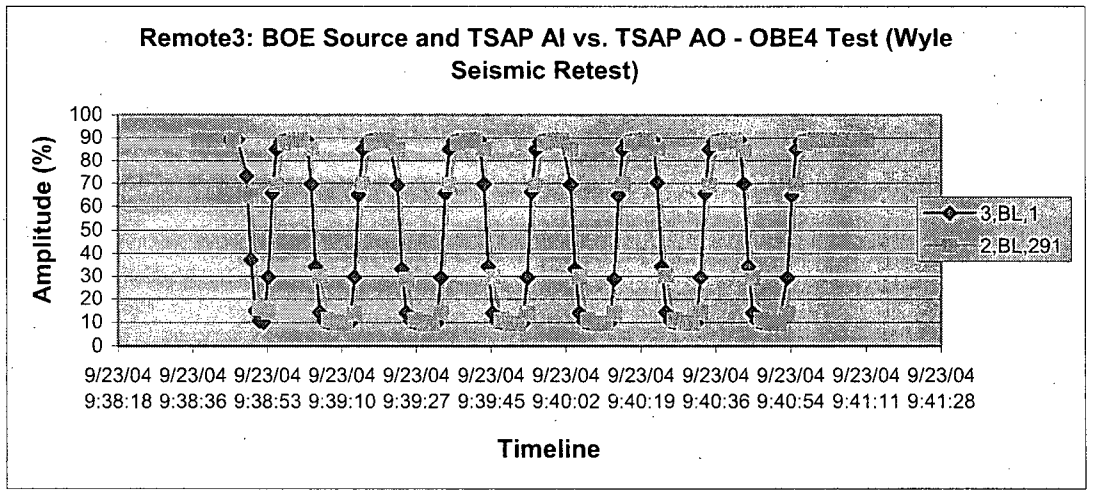

Figure 0-15. **Single Loop Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO from OBE4 Test for Seismic Retest.**

A.12.6 OBE5 Test

The waveforms of TSAP analog inputs at remote 1 and that of the BOE source signal during the OBE5 test of seismic retest are depicted in Figure A.12-16. The Figure shows that the TSAP AI signals correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table A.12-12 lists the averaged readings and deviations of 6 measurements for the HAS logged AI signals at 10% and 90% levels. The calculation of the deviation was based on 9.694% for 10% and 89.306% for 90%. Both 1,BL,510 and 1,BL,516 deviate less than 0.32% from the BOE source signal at both 10% and 90% levels. The magnitude of deviations is higher than the in-house test results at 10% level: 0.019% vs. 0.005% for 1,BL,510, and 0.038% vs. 0.01% for 1,BL,516; magnitude at 90% level is comparable: 0.081% vs. 0.045% for 1,BL,510, and 0.141% vs. 0.096% for 1,BL,516.

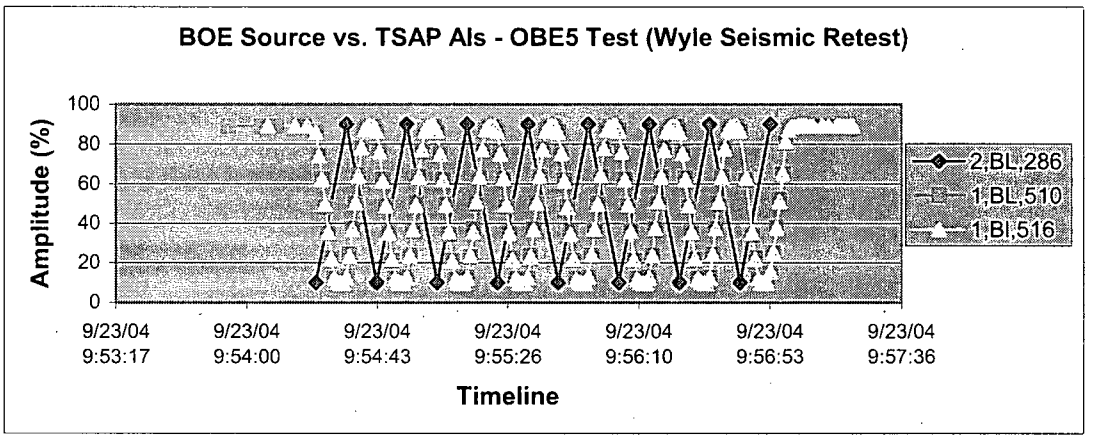

Figure 02-16. **BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from OBE5 Test for Seismic Retest.**

Figure A.12-17 shows the waveforms for TSAP AO (2,BL,213) versus its corresponding TSAP AI (1,BL,510) during OBE5 for seismic retest. The Figure shows that the AO image duplicates the AI image at each transition. The averaged readings and deviations for these two analog signals at 10% and 90% levels are listed in Table A.12-13. Deviations of 2,BL,213 from 1,BL,510 by 0.283% at both 10% and 90% levels were out of the acceptance range. The deviations at 10% and 90% levels are 0.423% and 0.474% respectively, compared with 0.115% and 0.327% from the in-house test. The increment at 10% is likely caused by the logging issues with HPAT as explained in the Pre Seismic Test.

Table 02-12. **TSAP AI Channel Readings and Deviations from BOE Source Signal from OBE5 Test for Seismic Retest.**

	1,AI,882 (1,BL,510)	1,AI,901 (1,BL,516)
10% Measurement (%)		
Deviation From 10% (%)		
No. of Measurements		
90% Measurement (%)		
Deviation From 90% (%)		
No. of Measurements		

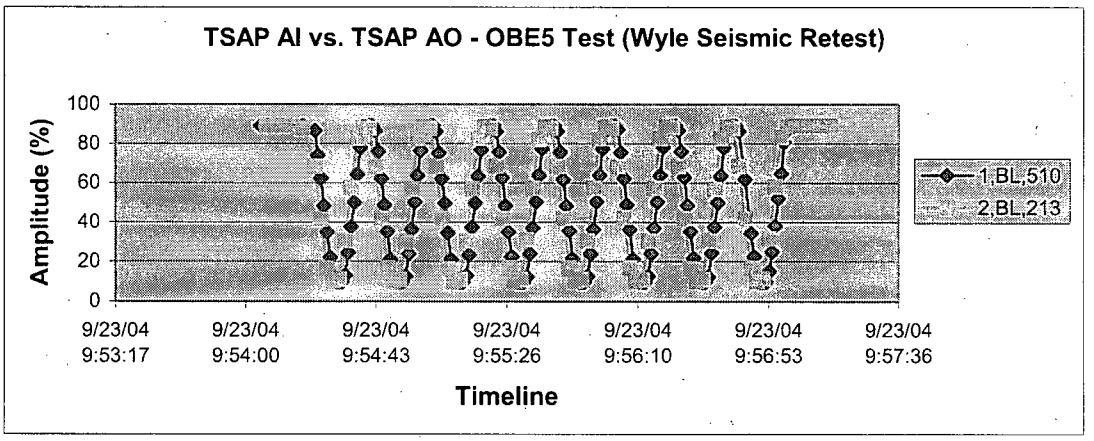

Figure 02-17. **TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) from OBE5 Test for Seismic Retest.**

Table 02-13. **TSAP AOs and the Corresponding TSAP AIs in Remote1 from OBE5 Test for Seismic Retest.**

	1,BL,510	2,BL,213	Deviation (2,BL,213 from 1,BL,510)	3,BL,1	2,BL,291	Deviation (2,BL,291 from 3,BL,1)
10% Measurement						
No. of Measurements						
90% Measurement						
No. of Measurements						

Figure A.12-18 shows the BOE source signal (2,BL,286) versus TSAP AI signal (3,BL,1) as well as the TSAP AO signal (2,BL,291) at single loop controller (remote 3) during the OBE5 test for seismic retest. The 3,BL,1 waveform duplicates the BOE source at each transition and the waveforms for 2,BL,291 and 3,BL,1 track each other at each transition. The averaged readings and deviations of 8 measurements for 3,BL,1 and 2,BL,291 at the 10% and 90% levels are provided in Table A.12-13. The results indicate that 2,BL,291 deviates less than 0.3% from 3,BL,1 at both levels, and the magnitude of deviations is comparable to in-house test results: 0.066% vs. 0.058% at 10%, 0.153% vs. 0.131% at 90%.

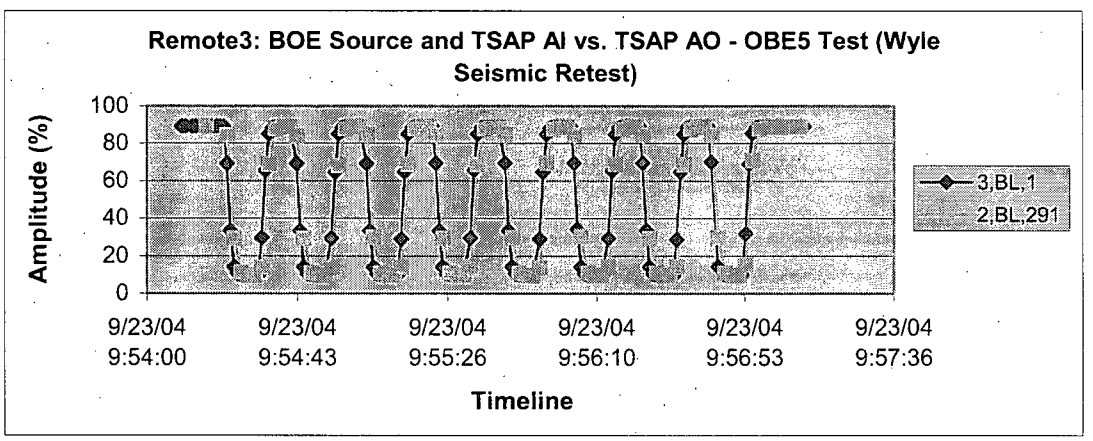

Figure 0-18. **Test Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO from OBE5 Test for Seismic Retest.**

A.12.7 SSE Test

The waveforms of TSAP analog inputs at remote 1 and that of the BOE source signal during the SSE test of seismic retest are depicted in Figure A.12-19. The Figure shows that the TSAP AI signals correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table A.12-14 lists the average readings and deviations of 8 measurements for the HAS logged AI signals at 10% and 90% levels. The

calculation of deviation was based on 9.694% for 10% and 89.306% for 90%. Both 1,BL,510 and 1,BL,516 deviate less than 0.32% from the BOE source signal at both 10% and 90% levels. The magnitude of deviations is higher than the in-house test results at 10% level: 0.019% vs. 0.005% for 1,BL,510, and 0.044% vs. 0.01% for 1,BL,516; magnitude at 90% level is comparable: 0.075% vs. 0.045% for 1,BL,510, and 0.141% vs. 0.096% for 1,BL,516.

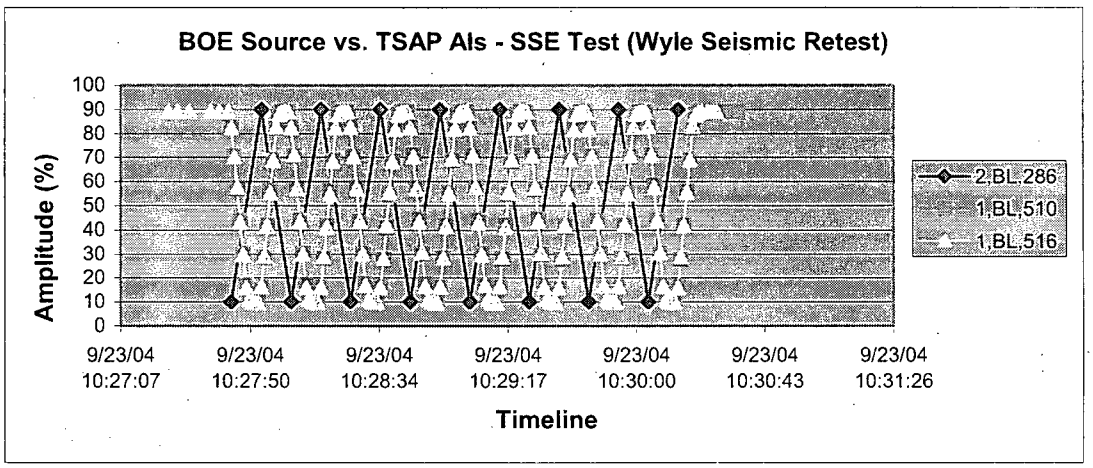

Figure 0-19. **BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from SSE Test for Seismic Retest.**

Figure A.12-20 shows the waveforms for TSAP AO (2,BL,213) versus its corresponding TSAP AI (1,BL,510) during SSE for seismic retest. The Figure shows that the AO image duplicates the AI image at each transition. The averaged readings and deviations for these two analog signals at 10% and 90% levels are listed in Table A.12-15. Deviations of 2, BL, 213 from 1,BL,510 by 0.283% at both 10% and 90% levels were out of the acceptance range. The deviations at 10% and 90% levels are 0.421% and 0.486% respectively, compared with 0.115% and 0.327% from the in-house test. The increment at 10% is likely caused by the logging issues with HPAT as explained in the Pre Seismic Test.

Table 0-14. **TSAP AI Channel Readings and Deviations from BOE Source Signal from SSE Test for Seismic Retest.**

	1,AI,882 (1,BL,510)	1,AI,901 (1,BL,516)
10% Measurement (%)		
Deviation From 10% (%)		
No. of Measurements		
90% Measurement (%)		
Deviation From 90% (%)		
No. of Measurements		

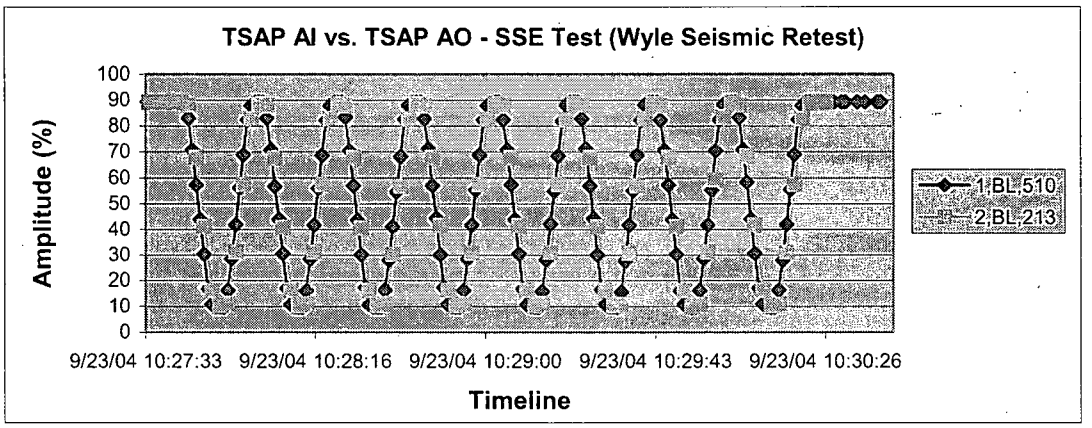

Figure 02-20. **TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) from SSE Test for Seismic Retest.**

Table 02-15. **TSAP AOs and the Corresponding TSAP AIs in Remote1 from SSE Test for Seismic Retest.**

	1,BL,510	2,BL,213	Deviation (2,BL,213 from 1,BL,510)		3,BL,1	2,BL,291	Deviation (2,BL,291 from 3,BL,1)
10% Measurement							
No. of Measurements							
90% Measurement							
No. of Measurements							

Figure A.12-21 shows the BOE source signal (2,BL,286) versus TSAP AI signal (3,BL,1) as well as the TSAP AO signal (2,BL,291) at test controller (remote 3) during the SSE test for seismic retest. The 3,BL,1 waveform duplicates the BOE source at each transition and the waveforms for 2,BL,291 and 3,BL,1 track each other at each transition. The averaged readings and deviations of 8 measurements for 3, BL,1 and 2,BL,291 at the 10% and 90% levels are provided in Table A.12-15. The results indicate that 2,BL,291 deviates less than 0.3% from 3,BL,1 at both levels, and the magnitude of deviations is comparable to in-house test results: 0.064% vs. 0.058% at 10%, 0.151% vs. 0.131% at 90%.

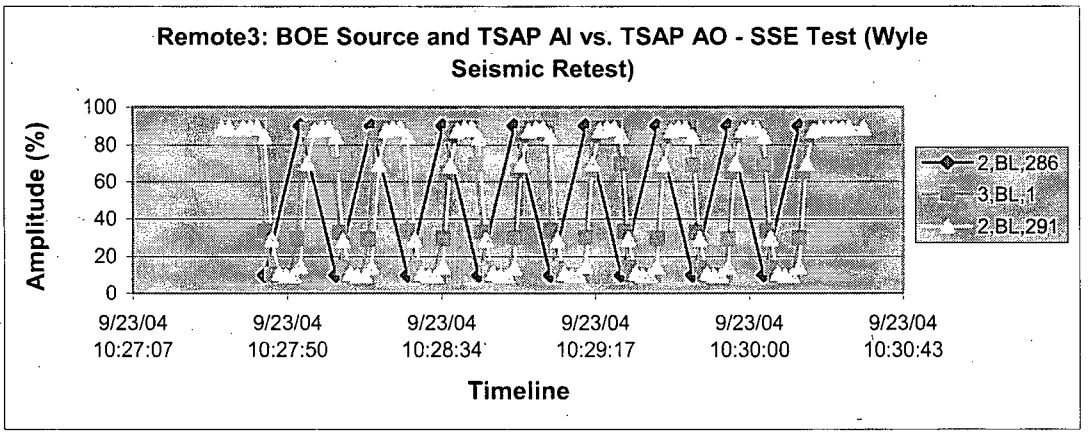

Figure 0-21. **Single Loop Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO from SSE Test for Seismic Retest.**

A.12.8 Post Seismic Test

The waveforms of TSAP analog inputs at remote 1 and that of the BOE source signal during the post seismic test are depicted in Figure A.12-22. The figure shows that the TSAP AI signals correlate well with the BOE source signal at each transition, and they essentially overlap with one another. Table A.12-16 lists the average readings and deviations of 17 measurements for the HAS logged AI signals at 10% and 90% levels. The calculation of deviation was based on 9.694% for 10% and 89.306% for 90%. Both 1,BL,510 and 1,BL,516 deviate less than 0.32% from the BOE source signal at both 10% and 90% levels. The magnitude of deviations is higher than the in-house baseline test results at 10% level: 0.035% vs. 0.005% for 1,BL,510, and 0.063% vs. 0.01% for 1,BL,516; magnitude at 90% level is comparable: 0.074% vs. 0.045% for 1,BL,510, and 0.156% vs. 0.096% for 1,BL,516.

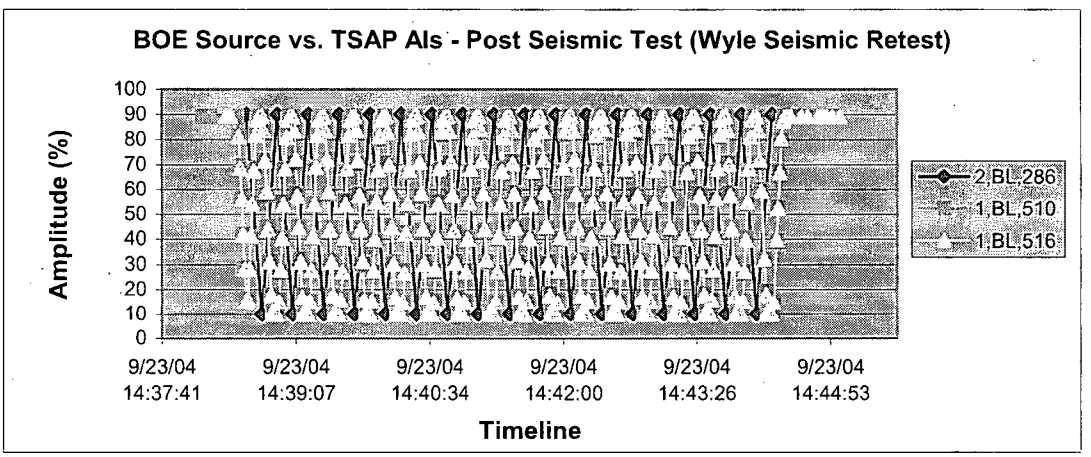

Figure 0-22. **BOE Control Signal versus TSAP Analog Input Signals in Remote 1 from Post Seismic Test for Seismic Retest.**

Figure A.12-23 shows the waveforms for TSAP AO (2, BL,213) versus its corresponding TSAP AI (1,BL,510) during post seismic test for seismic retest. The Figure shows that the AO image duplicates the AI image at each transition. The averaged readings and deviations for these two analog signals at 10% and 90% levels are listed in Table A.12-17. Deviations of 2,BL,213 from 1,BL,510 by 0.283% at both 10% and 90% levels were within the acceptance range. The deviations at 10% and 90% levels are 0.082% and 0.161% respectively, which are less than the in-house test results of 0.115% and 0.327% respectively. The improvement was likely caused by the same HAS logging issue discussed in Pre Seismic Retest.

Table 0-16. **TSAP AI Channel Readings and Deviations from BOE Source Signal from Post Seismic Test for Seismic Retest.**

	1,AI,882 (1,BL,510)	1,AI,901 (1,BL,516)
10% Measurement (%)		
Deviation From 10% (%)		
No. of Measurements		
90% Measurement (%)		
Deviation From 90% (%)		
No. of Measurements		

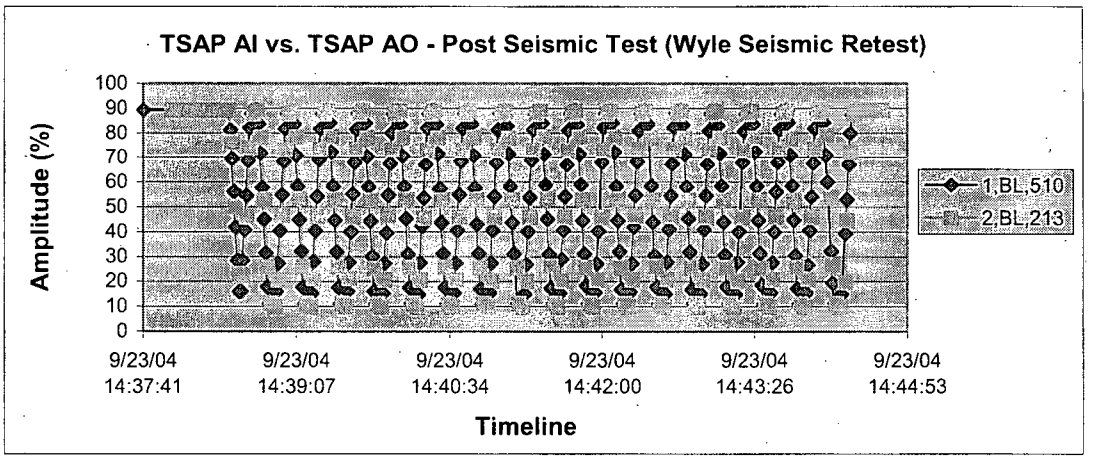

Figure 02-23. **TSAP AI signal (1,AI,882, 1,BL,510) versus Corresponding TSAP AO Signal (1,AO,922, 2,BL,213) from Post Seismic Test for Seismic Retest.**

Table 02-17. **TSAP AOs and the Corresponding TSAP AIs in Remote1 from Post Seismic Test for Seismic Retest.**

	1,BL,510	2,BL,213	Deviation (2,BL,213 from 1,BL,510)	3,BL,1	2,BL,291	Deviation (2,BL,291 from 3,BL,1)
10% Measurement						
No. of Measurements						
90% Measuremen						
No. of Measurements						

Figure A.12-24 shows the BOE source signal (2,BL,286) versus TSAP AI signal (3,BL,1) as well as the TSAP AO signal (2,BL,291) at single loop controller (remote 3) during the post seismic test for seismic retest. The 3,BL,1 waveform duplicates the BOE source at each transition and the waveforms for 2,BL,291 and 3,BL,1 track each other at each transition. The averaged readings and deviations of 8 measurements for 3,BL,1 and 2,BL,291 at the 10% and 90% levels are provided in Table A.12-17. The results indicate that 2,BL,291 deviates less than 0.3% from 3,BL,1 at both levels, and the magnitude of deviations is comparable to in-house test results: 0.069% vs. 0.058% at 10%, 0.136% vs. 0.131% at 90%.

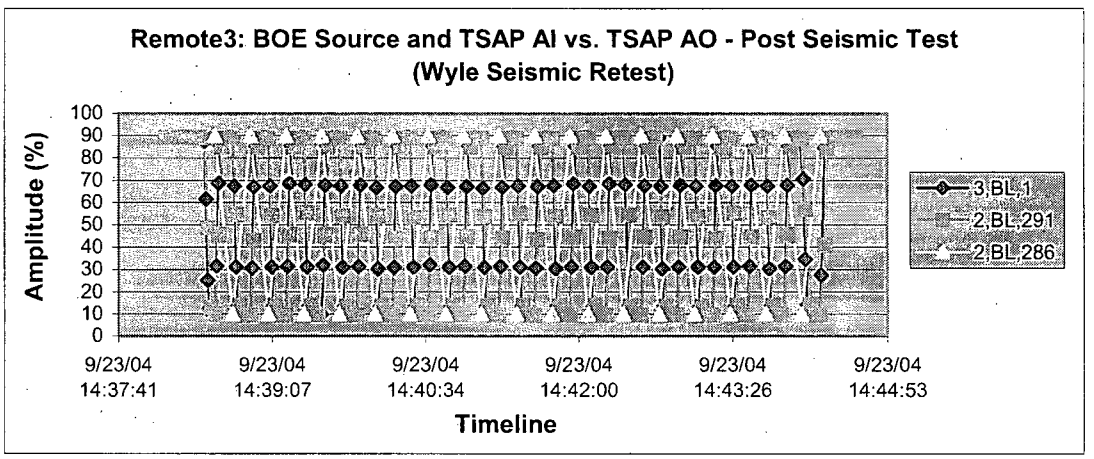

Figure 02-24. **Single Loop Controller Analog BOE Source Signal versus TSAP AI and TSAP AI versus TSAP AO from Post Seismic Test for Seismic Retest.**

HF Controls

HFCONTROLS CONTROL SYSTEM

Class 1E Nuclear Control System

HFC-6000 Product Development Plan
ERD111 US NRC qualification project

NON-PROPRIETARY

VV0401
Rev A
Sept. 2003

Rev	Date	Author	Reviewer	Approval
A	9/28/2003	Allen Hsu	Jonathan Taylor	J.A Stevens

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Revision History

Date	Revision	Author	Changes
10/31/02	0	A. Hsu	Draft
9/28/2003	A	A. Hsu	Change product line and components names

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1.0 PURPOSE AND SCOPE

The HF Controls (HFC) Integrated Safety Control System for nuclear power application is composed of hardware and software from two existing product lines; the AFS-1000 Critical Control System and the ECS-1200 Distributed Control System. Both product lines are mature and have a substantial operating base in fossil, utility and nuclear application. This development plan is to dedicate the technology to an integrated system; HFC-6000 Plant Control System for USNRC qualification program.

The Product Development Plan continues to serve as the primary communication vehicle for development plans and progress. It is a dynamic document during planning, execution and closure phases and is updated when necessary to reflect changes in development scope, constraints, deliverables, tests and progress.

The ERD111 project serves as the US NRC qualification project by using HFC-6000 as Nuclear Safety related control system.

1.1 SCOPE

The qualification system will be composed of four 19-inch card files mounted on an open cabinet frame to simulate cabinet installation. These card files will encompass every feature of the HFC-6000 architecture to be qualified. (This requirement will determine the total number of card files to be included in the test system.) One of these chassis will be configured with redundant controller hardware, the system power supply, and I/O modules linked directly to the controller. Two of the remaining card files illustrated in Figure 1 will be linked directly to the controller as expander I/O chassis. The remaining card file (labeled local I/O in Figure 2-1) will contain a power supply module and I/O cards linked to the controller via a fiber-optic communication link. The overall configuration will simulate the hardware arrangement of a redundant remote controller that is physically located in an equipment room and a local I/O chassis that is physically located near the equipment under control.

The controller hardware will support two redundant serial communication links:

1.2 GENERAL ARRANGEMENT

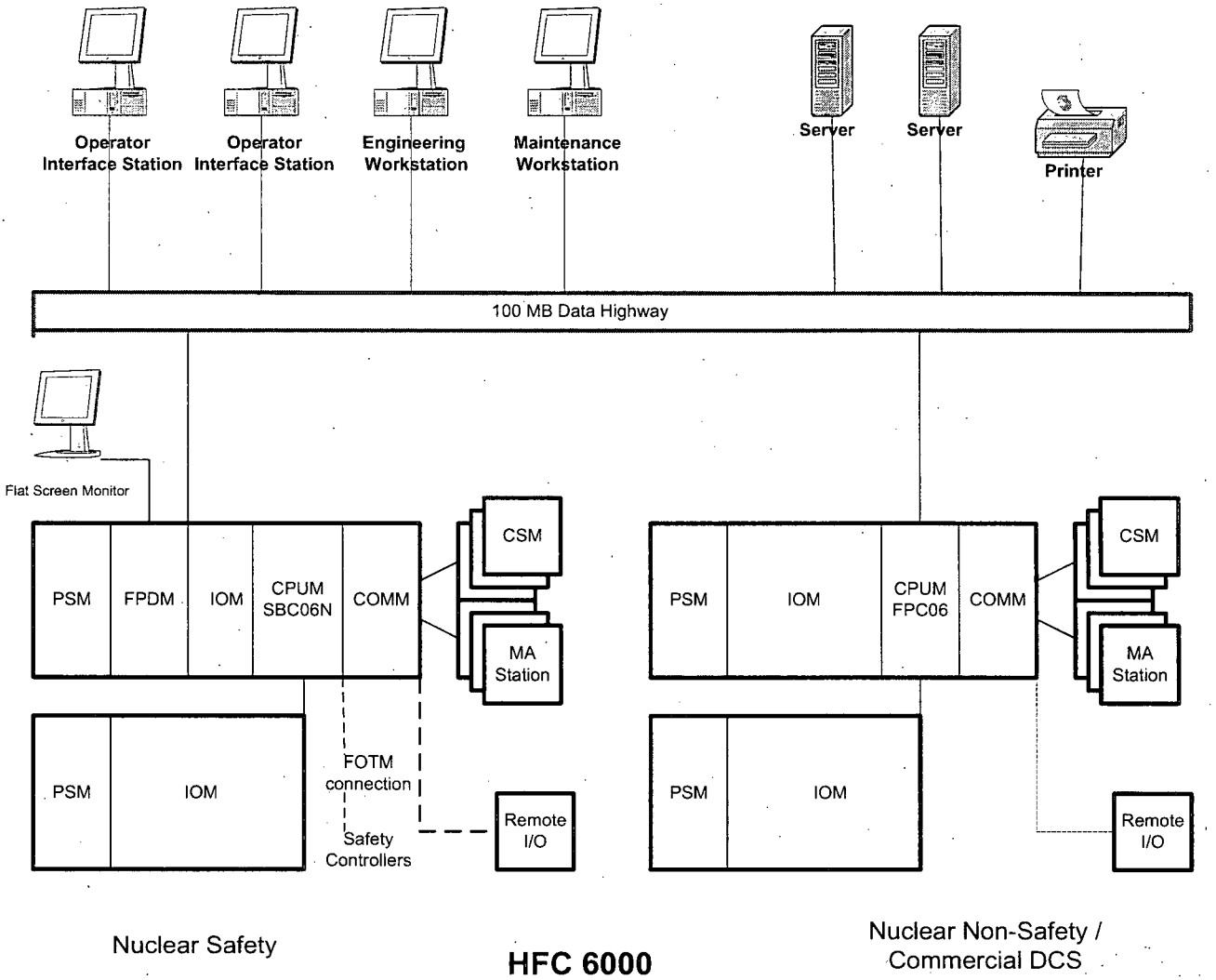


Figure 1, General Arrangement

CPUM	CPU Module for nuclear safety equipment
IOM	I/Os cards family (NQ-series)
COMM	Communication Module
FPDM	Flat Panel Device Module
PSM	Power Supply Module
CSM	Control Switch Modules
MA	Manual/Auto Station

CPUM CPU Module for nuclear safety equipment

Safety equipment
1. Multi-loop controller
SBC06N Redundant multi-loop controller
DPM06N Dual port memory
2. Single-loop controller
SBC04N Single loop controller
Non-safety equipment
ECS06 Multi-loop controller

IOM I/Os cards family
HFC- (a)(b)(c)(d) N
(a) D – Digital, A – Analog, C- Combination
(b) I – Input, O – Output, C – Combination
(c) Number of points 8, 16 or 32
33: 2-120vac outputs,
12-48vdc inputs
34: 2-125vdc outputs
12-48 vdc inputs
35: 1-120vac output
12-48vdc inputs
36: 8 - 4 to 20ma outputs
8 – 4 to 20ma inputs
37: 8 – 0 to 10v outputs
8 – 0 to 10v inputs
(d) Voltage
A – 120vac, B – 125vdc, C – 24vdc, D – 48vdc, E – 0 to 10vdc,
F – 4 to 20ma, G – 250vdc, H – 220vdc, I – 48vdc SOE,
J - Form C contact, K – Pulse, L – Thermocouple, M – RTD 100ohms,
N – RTD 200ohms, P – RTD 2000ohms, Q - special
N – Nuclear

Examples –
DC34N 2 channels 125vdc DO and 12 channels 48vdc DI
DI16DN 16 channels 48vdc Digital Inputs
DC34N 2 channels 125vdc DO and 12 channels 48vdc DI

COMM -
PCC06N CSM, M/A station and RSP channels multiplexer card
ILI06N I/O link Isolator
ILR06N I/O link Repeater/Terminator

FPDM	Flat Panel Device Module	
	FPC06N	Flat Panel Device controller
	FPD06N	Flat Panel Device
PSM	Power Supply Module	
	PSR06N	Rack mounted 24v power supply
	GFD06N	Ground Fault Detector
CSM	Control Switch Modules	
MA	Manual/Auto Station	
FOTM	Fiber Optics Transmitter Module	
	FOT06N	FOT channel boards
	HUB06	Isolation hub

1.3 REFERENCES

In compliance with HFC Quality Manual and Work Instructions, the following Project Specific Documents are to be generated. In HF Controls' compliance with the Software Verification and Validation standards (IEEE 7.4.3.2, 730, 830, 1012, 1074-1995) etc. we have taken a system wide approach and have changed the organization of some of the specified plans. Where the organization of the document has been change from the Standard we have included a cross-reference table.

- VV0401 – Product Development Plan
- VV0402 – Project Quality Plan (PQP-2003-005)
- VV0403 - System Requirements Specification
- VV0405 (WI-ENG-003) - Configuration Management Plan
- VV0404 (WI-ENG-008) - Software QA Plan
- DD0401 - Test System Design Description
- TN0401 - Master Test Plan

The Product Development Plan refers to HF Controls Standard Procedures and Work Instructions for nuclear project which; will be followed to the extent they do not contradict any of the project specific Procedures or Plans listed above.

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Application in Nuclear Power Plants

1.4 ABBREVIATIONS AND ACRONYMS

BIT	Built-in Test
CPC	Communication Protocol Controller
CRC	Cyclical Redundancy Check
CSM	Control Switch Module
DCS	Distributed Control System
EWS	Engineering Workstation
FPD	Flat Panel Device
HFC	HF Controls
HPAT	HFC PCS Automated Tester
ICL	Intercommunication Link
I/O	Input/Output
HFC-6000	HFC Integrated Safety Control System
JCRT	JAVA Compliant CRT Workstation
LAN	Local Area Network
M/A	Manual/Automatic
NRC	Nuclear Regulatory Commission
PCC	Peripheral Communication Controller
PID	Proportional Integral Derivative. A type of analog control algorithm.
RTD	Resistance Temperature Detector
SOE	Sequence of Events
TSAP	Test System Application Program. A "synthetic application" used to check/verify the Control System functionality needed to support the qualification test program.
TTL	Transistor-Transistor Logic

1.5 DEVELOPMENT PROJECT ASSUMPTIONS AND CONSTRAINTS

This section contains a discussion of the project assumptions or factors that affect project decisions. Changes in these assumptions and constraints can affect the project schedule, phases, tasks, resources, etc.

1.5.1 Milestone Schedule

Please refer to the attached HFC-6000 USNRC qualification project master schedule.

1.5.2 Assumptions

- The entire qualification process should be guided through our nuclear consultants Hurst Technologies and Process Design Consultants, Inc.
- The product design process shall follow all requirements from HFC internal business plan. The main focus of this development is to dedicate an integrated control system for NRC qualification, US NPP retrofit projects, NSSS applications and next generation Nuclear Plant Control Systems.
- Base upon the milestone schedule, HFC should complete the test set of modular HFC-6000 chassis by August 1, 2003. The process to merge all existing AFS/ECS product lines in to HFC-6000 family cards shall be executed as continuity phase of this project. So is the cabinet development and arrangement.

2.0 PRODUCT LINE DEVELOPMENT ORGANIZATION

2.1 DEVELOPMENT PROJECT TEAM

The Development Project Team will provide the analytical, functional, organizational, technical and clerical skills necessary to complete the development tasks. It will be a dynamic entity changing to match the project's needs. The Project Manager will be responsible for organizing the Development Project Team and adjusting the participants as the project execution progresses.

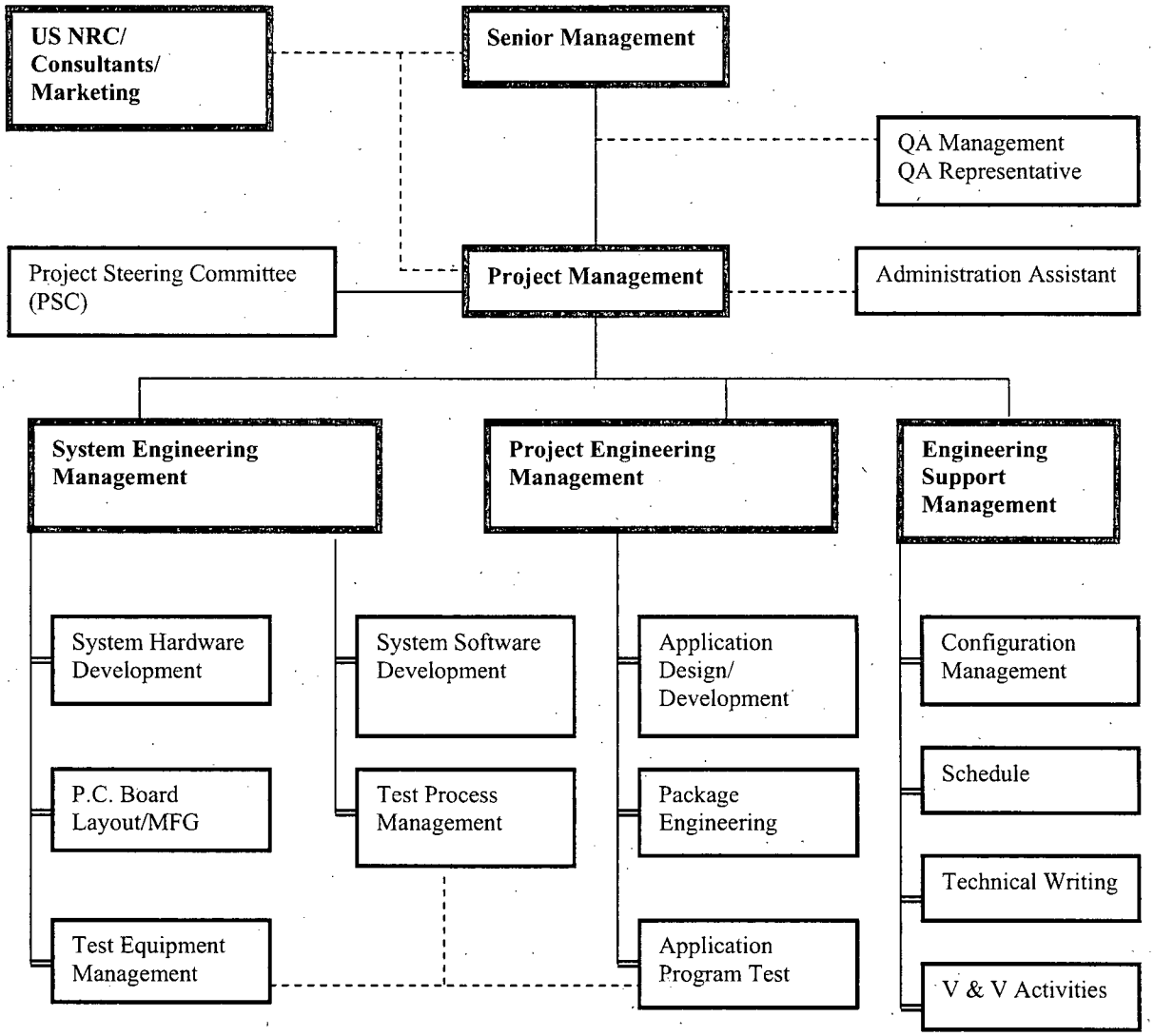


Figure 2, Organization chart with project structure

Where_____ Report channel
------- Communication link
═══ Technical responsibility

During the execution of the project, the Development Project Team will also include full and/or part-time (dedicated or non-dedicated) participation by representation from Hardware and Software Development, manufacturing, operations, purchasing, and system test organizations. The Development Project Team participation shall be in accordance with the project's funding plan as agreed to by the HF Controls Senior Management Team.

2.1.1 Senior Management

The Senior Management of HF Controls will review the project cost, the estimated man-hours and cost to complete and any outstanding issues. The members of the Senior Management Committee are as follows:

- HF Controls' President – Tim McCreary
- HF Controls' Chief Financial Officer – J. H. Choi
- HF Controls' QA Manager – Charles Fisher
- HF Controls' V. P. Engineering – Allen Hsu

2.1.2 Project Manager

The Project Manager for the ERD111 US NRC qualification project is Mr. John Stevens who has prior experience in planning, organizing, and managing projects of this complexity and nature. Mr. Stevens will be responsible for ensuring all project activities are performed and that all processes are completed. The Project Manager will organize and, as required, delegate to other Development Managers/Project Leaders the responsibilities to implement tactical aspects of the project. The responsibilities of the project manager will be in accordance with "Project Management Overview", Procedure WI-ENG-902, to the extent that it does not conflict with this Product Development Plan or any other of the project specific procedures and or plans as referenced above.

2.1.2.1 Authority

The Project Manager has been given the authority to assemble, plan, and execute the Project to insure that the requirements of the HFC Quality Procedures/Work Instructions are met. He has also been delegated the authority to make decisions and commitments regarding schedule, scope, material content, and financial performance (With Management Oversight and direction). This authority is granted by the Company President or Chief Executive Officer for all aspects of this Project.

2.1.2.2 Tasks & Responsibilities

- Oversee changes to the Project schedules, including time and cost estimates
- Secure and manage manpower and resources in all parts of the organization
- Define, organize, schedule and document Project meetings
- Manage the Hardware/Software Engineers, and Project Application Engineer
- Insure that the product delivered meets the project requirements
- Schedule and maintain all Project documentation/publications
- Verify that all Project specific Corrective Actions are addressed and cleared
- Oversee activities of V&V Team
- Maintain and execute the Software Configuration Management plan in according with WI-ENG-003
- Maintain and oversee execution of the System Design Definitions (DD0401)

2.1.3 Engineering Support Manager

The tasks and responsibilities of the Engineering Support Manager are to perform most of the project control functions. He also has been given the authority, tasks and responsibilities of the System Verification and Validation team as fully defined in the System Verification and Validation Plan (WI-ENG-008). To fully carry out the V&V requirements, the Engineering Support Manager shall also coordinate the System Test tasks and responsibilities. Briefly, the tasks and responsibilities for these various functions are as follows:

2.1.3.1 V&V Tasks & Responsibilities

- Generate, maintain and oversee execution of the master test plan.
- Generate and maintain the V & V reports
- Form and manage the V&V team, auditors and schedules for V&V task
- Create, track, administer, maintain, keep records and generate reports associated with reported issues, problems, anomalies and/or V&V Corrective action requests associated with this project
- Insure, monitor and provide reporting associated with V&V tasks and test reports and verify that any anomalies are properly reported
- Insure that the product delivered meets the project requirements
- Verify that all Project specific Condition Reports, Project Change Request and Corrective Actions are addressed and cleared
- Monitoring the laboratory tests and all intermediate testing defined in the master test plan by System Test personnel
- Participate in the V&V plan and audit schedules/reviews by System Test personnel
- Complete and submit all V&V and Quality Assurance documentation
- Verify that all System Test Condition Reports, Project Change Request and Condition Report (CR) are addressed and cleared

2.1.3.2 Other Engineering Support Tasks & Responsibilities

- Establish and maintain Project schedules, including time and cost estimates
- Establish and maintain Project Budgets and Estimate to Complete on Corporate computer system.
- Develop project databases, correspondence, drawing/document logs, Application Loops & I/O, Corrective Actions, etc.
- Define, organize, schedule and document Project meetings assigned by Project Manager
- Manage the Technical writers
- Support SCM record keeping and reporting

2.1.4 Hardware Design Engineer

Tasks & Responsibilities

- Execute the Hardware requirements documents
- Define interaction between hardware and software within the designs
- Assure that the hardware design specifications conform to the SRS (VV0403)

- Assure that the hardware design conforms to the SDD (DD0401)
- Coordinate and participate in the hardware functional testing of the master test plan.
- Participate in Design Reviews
- Participate in V&V reviews
- Complete and submit all V&V and Quality Assurance documentation
- Schedule, create and maintain all hardware documentation/publications
- Verify that all hardware Condition Report (CR) are addressed and cleared

2.1.5 Software Design Engineer

Tasks & Responsibilities

- Maintain the Software requirements documents
- Define interaction between hardware and software within the designs
- Assure that the software design specifications conform to the SRS (VV0403)
- Assure that the software design conforms to the SDD (DD0401)
- Coordinate and participate in the software functional testing of the master test plan
- Participation in Design Reviews
- Participate in V&V reviews
- Complete and submit all V&V and Quality Assurance documentation
- Schedule, create and maintain all software documentation/publications
- Verify that all software Condition Report (CR) are addressed and cleared

2.1.6 Project Engineer

Tasks & Responsibilities

- Maintain and execute the Applications requirements documents
- Assure that the Applications design specifications conform to the SRS (VV0403)
- Assure that the Applications design conforms to the SDD (DD0401)
- Coordinate and participate in the Application functional testing per the SRS (VV0403)
- Participate in Design Reviews
- Participate in V&V plan and audit schedules/reviews
- Complete and submit all V&V and Quality Assurance documentation
- Schedule, create and maintain all Applications documentation/publications
- Verify that all Applications Condition Report (CR) are addressed and cleared

2.1.7 Project Steering Committee

The Project Steering Committee is responsible for providing the administrative and managerial direction for the project and for all system-related development activities, procurement, manufacture, assembly and testing within this product line development plan. Its duties include setting project direction, evaluating project performance against planned performance, assessing all deviations, and prioritizing and resolving project issues. This entity serves as the approval body for all development-related decisions. When necessary this committee may also call on the Senior Management of HF Controls. Upon review by the Project Steering Committee, any questions and/or decisions which in

their judgment is 1) a change in the current development scope, 2) impacts project funding, 3) impacts schedule of equipment deliveries, 4) any issue or problem item which can not be resolved by the committee, or 5) other items requiring approval by HF Controls' Senior Management. The members of the HF Controls Project Steering Committee shall consist of the following:

- Project Director – Allen Hsu
- Project Manager – John Stevens
- Engineering Support – Jon Taylor
- System Engineering – Terry Geraradis and Jim Grisham
- QA Manager – Charles Fisher
- Manufacturing Manager – Tracy Mosley
- Procurement/Material Control Manager – Gregg Redding
- Consultants – Tim Hurst

2.2 QA MANAGEMENT

The authority, tasks and responsibility of the QA Management are defined in the HF Controls Quality Manual and Project Quality Plan (PQP2003-005).

3.0 DELIVERABLES

Table 1 contains the specific component count of hardware modules and assemblies to be included in the test specimen.

Table 1, HFC-6000 Test Specimen Equipment

Quantity	Module Type	Description	Firmware

Third Party Equipment			

Table 2 lists documents that are required for this project.

Table 2, Summary of document list

HFC Doc. Number	**ERD111 Project Documents Description**	**Requirement**
ADS0401	TSAP Design Specification	USNRC Qualification
AFS0401	TSAP Functional Specification	USNRC Qualification
AFS0402	ASOA Functional Specification	USNRC Qualification
ASC0401	TSAP Program listing	USNRC Qualification
ATP0401	TSAP Validation Test Procedure	USNRC Qualification
ATP0402	ASOA Test procedure	USNRC Qualification
ATR0403	TSAP V & V Report	USNRC Qualification
CC0401	Certificate of Conformance	USNRC Qualification
CC0402	QVDL	Project
DD0401	Test System Design Description	USNRC Qualification
DD0402	Test System Arrangement/Wiring Diagram	USNRC Qualification
DD0403	Test System loop Diagram	USNRC Qualification
DD0404	System Drawings	USNRC Qualification
DD0405	System Hardware/Software Configuration	Project
DD0406	System Database Documentation	USNRC Qualification
MN0401	Operator's Manual	USNRC Qualification

MN0402	Programmer's Manual	USNRC Qualification
MN0403	Equipment Maintenance Manual	USNRC Qualification
MN0404	System Installation Manual	Project Internal
MN0405	HFC-6000 Module Selection Guide	Project Internal
MN0406	HFC-6000 Application Guide	USNRC Qualification
SFS0401	Software Functional Specification (OS)	USNRC Qualification
SDS0401	Software Design Specification (OS)	USNRC Qualification
TN0401	Master Test Plan	USNRC Qualification
TN0402	Class 1E/Non Class 1E Test Plan	USNRC Qualification
TP0401	Setup and Checkout Test Procedure	USNRC Qualification
TP0402	Operability Test Procedure	USNRC Qualification
TP0403	Prudence Test Procedure	USNRC Qualification
TP0404	Environmental Test Procedure	USNRC Qualification
TP0405	Seismic Test Procedure	USNRC Qualification
TP0406	Surge Withstand Test Procedure	USNRC Qualification
TP0407	EMI/RFI Test Procedure	USNRC Qualification
TP0408	ESD Test Procedure	USNRC Qualification
TP0409	Burn-in Test procedure	USNRC Qualification
TR0401	Pre-qualification Test Report	USNRC Qualification
TR0402	Equipment Test Report	USNRC Qualification
TR0403	Environment Test Report	USNRC Qualification
TR0404	Seismic Test Report	USNRC Qualification
TR0405	EMI/RFI Test Report	USNRC Qualification
TR0406	Surge Test Report	USNRC Qualification
TR0407	ESD Test Report	USNRC Qualification
TR0408	Safety 1E/Non Safety 1E Isolation Test Report	USNRC Qualification
TR0409	Performance Proof Test Report	USNRC Qualification
TR0410	Final summary Report	USNRC Qualification
TR0411	Topical Report for subtotal	USNRC Qualification
TR0420	Operability Test Reports	USNRC Qualification
TR0421	Prudency Test Reports	USNRC Qualification
TR0422	Setup and Checkout Test Reports	USNRC Qualification
VV0401	Product Development Plan	Project
VV0402	Project Quality Plan	Project (PQP2003-005)

VV0403	System Requirement Specification	Project
VV0404	Software QA Plan/SVVP	HFC Procedure
VV0405	System Configuration Management Plan	HFC Procedure
VV0407	Design Evaluation Reports	Project
VV0408	Reliability/Availability Analysis Report	USNRC Qualification
VV0409	Failure Modes & Effects Analysis	USNRC Qualification
VV0410	Software Qualification Report	USNRC Qualification
VV0411	Accuracy & Setpoint Analysis Report	USNRC Qualification
VV0412	Final Summary Report	USNRC Qualification
VV0413	Topical Report for subtotal	USNRC Qualification
VV0414	Master Configuration List	USNRC Qualification

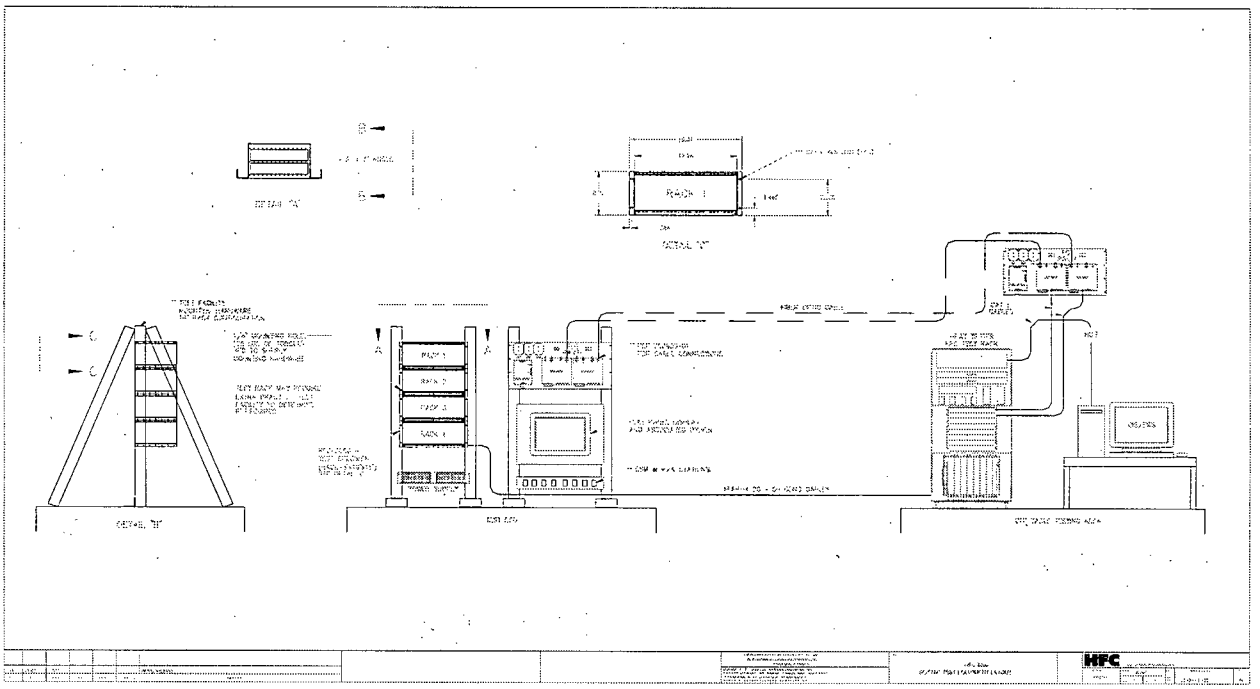
4.0 PROJECT EXECUTION

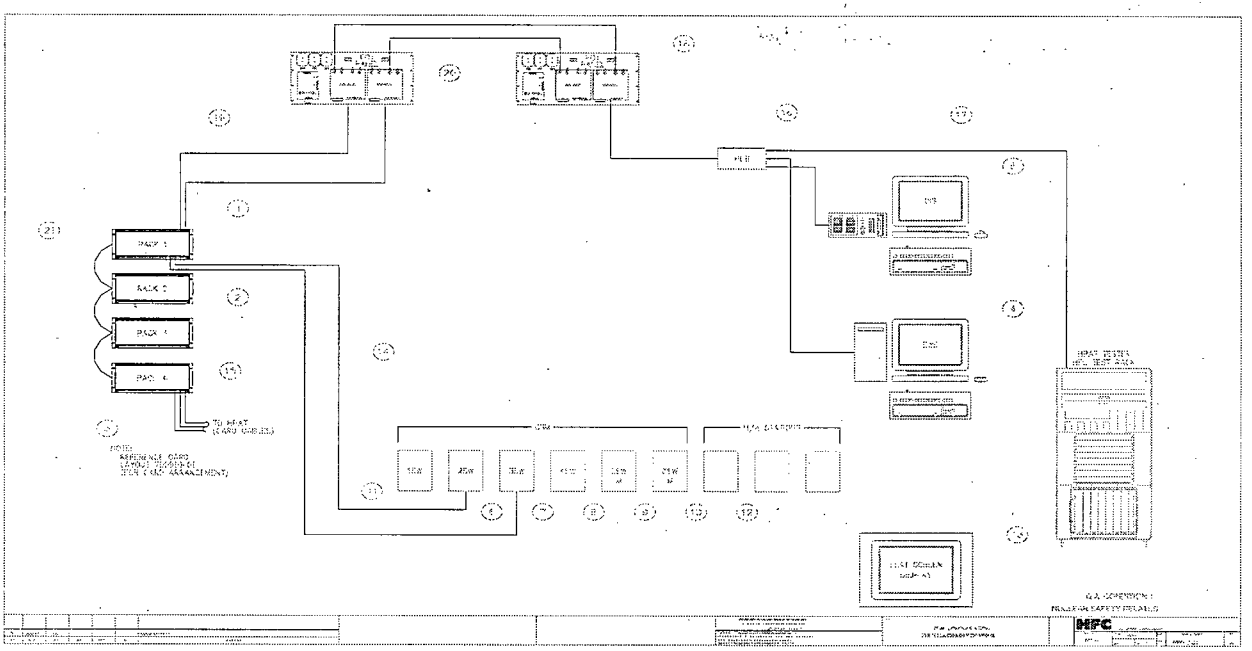
The HF Controls Project Management Life Cycle (PMLC) addresses the project management needs for all HF Controls systems projects. It is applicable to projects that require development of new products or software, and to projects, which utilize existing HF Controls and other company's products and software. The HF Controls PMLC is generally defined in the Project Management Overview Procedure WI-ENG-902 and the supporting Procedures and Work Instructions. The supporting Procedures and Work Instruction are as listed in the Reference section of this Product Development Plan. These will be followed to the extent there are no conflicts with this Product Development Plan and any associated Project specific plans and procedures.

4.1 PROJECT MANAGEMENT OVERVIEW

As described in the Project Management Overview (WI-ENG-902), the Project Manager and other key project leaders were involved in the review of the final requirement, review of the proposed list of deliverables and the associated application engineering, any hardware and software development items, and other technical aspects of the project.

Figure 3, Arrangement drawings of qualification test set (700911_01-0001 & 700912_01-0001)





4.1.1 Project Planning

Upon the development project approval by HFC senior management staff, the Project Execution phase was initiated with the project planning aspects of the Project Life Cycle. The following steps were taken in planning and initiation of the execution of this project within HF Controls.

- Reviewed and updated the qualification proposal and started assigning personnel to the different functional labor groups
- Since this project mainly involves engineering exercise in the first phase, held an internal kick-off meeting among the key engineering personnel and consultants is necessary. At the beginning of second phase (Manufacturing) held internal Kick-off meeting to disseminate preliminary information to other departments that will be affected by this project i.e. Procurement, QA, Manufacturing, System Test, and Service (Project Kick-off Meeting, Work Instruction WI-ENG-916).
- Reviewed Project Risk and their mediation
- Provided Summarized Project Schedule and Manpower loading projections based on the estimate. The summarized schedule provided the major milestones for the project (Project Execution Plan, Work Instruction WI-ENG-912)
- Setup Project Documentation files in accordance with the Product Development Plan.

4.1.2 Project Execution

As the project proceeds through the Project Life Cycle phases of Project planning, requirements definition, design, production, pre-installation testing the other portions of the Project Execution of the Project Overview shall be performed as follows:

- Schedule review meetings & handle NRC interface
- Maintain the Project Master Schedule
- Meet with HF Controls Operations weekly to review schedule with manufacturing and procurement. Any issues with Procurement, Material Control and Manufacturing will be raised, reviewed and resolution discussed.
- Facilitate and review subcontractor meetings for procurement of major project items
- Coordinate the efforts of testing to assure that the requirements of the specifications are being met.
- Review the project monthly with Senior Management of HF Controls regarding the financial aspects, Coordination issues between departments, Estimated cost to complete (ETC), any major outstanding risk issues, etc.

5.0 PROJECT CONTROLS

5.1 PROJECT DOCUMENTATION FILES

Since it is HFC internal project, there is no Project Contractual Documents, Proposal and Cost Sheets, Transmittal and Approval documents, Correspondence, and other documentation of a commercial non-technical nature in accordance with the "Project Documentation Files" Procedure WI-ENG-901.

5.2 CONFIGURATION MANAGEMENT

Project changes during the Project Life Cycle shall be controlled in order to prevent unauthorized and untested changes to hardware and software of the deliverable product. The final product may contain many components such as code modules, user documentation, installation procedures, test cases, requirements documentation, design documentation, planning documents, etc. These are all either interim or final product deliverables. Methods have been established to identify the product components that need to be controlled, when they need to be controlled, and by whom. Change control and reporting methods have been established. The combination of these controlling methods is called Configuration Management, and the System Configuration Management Plan contains the details on how this will be accomplished.

REFERENCE: Systems Configuration Management Plan (SCMP) WI-ENG-003

5.3 DOCUMENT CONTROL

Changes to key project documentation are covered under System Configuration Management Plan (SCMP WI-ENG-003). Members of the project team are to file the documents generated in the directory structure as detailed in the above on the dedicated LAN Drop. The hard copy of documents assigned a HF Controls part Document Number will be stored in PVCS version manager utility. All Project specific documentation will be verified and confirmed to meet the requirements. This review will be conducted by (1) the document creator, (2) one or more members of the Project Steering Committee, (3) by internal audits scheduled and monitored by the V&V Team. Any discrepancies found, at any of the review steps, will be resolved.

5.4 PROBLEMS/ISSUES MANAGEMENT

During the project life cycle, problems, anomalies and issues will arise that must be resolved. If left unresolved, these can greatly impact product quality and severely impact project cost and schedule constraints. HF Controls corrective action and nonconformance program is implemented by QPP 16.1, "Corrective Action Program".

During the design phase of the products, software and engineering deliverables problems and issues will be documented and tracked utilizing the Design and Verification procedure (WI-ENG-001) reviews for those documents. Once the Final Baseline for a document, drawing, software module, or product has been reached, it shall be subject to the following Condition Reporting process. Please refer to System Configuration and Management Plan (WI-ENG-003) for further details on the Final Baseline.

Any member of the Project Team or other involved parties from manufacturing, procurement, customer, vendor etc. may identify any item that is believed to be an issue, concern, Condition or possible problem by entering an Condition Report (CR). After Final Baseline, any of the following, but not limited to the following, may be cause for the generation of an CR:

- Failures
- Faults
- User errors
- Incoming material Non-conforming Material Report
- Engineering Change Request
- Design Problem
- Manufacturing problem
- Process failure
- Procedure violation
- Procedure requiring change
- Training issues
- QA/QC issues
- Documentation issues

5.5 QUALITY MANAGEMENT

5.5.1 Verification & Validation

Quality assurance methods must be used throughout the Project Life Cycle to ensure product quality. The compilation of these methods is a process called Verification & Validation. Verification and Validations will be performed during this project. Please refer to the Systems Verification and Validation Plan (SVVP) (WI-ENG-008) for further guidance on the process and how these will be performed.

5.5.2 Reviews and Audits

Reviews and audits are two of the key methods that are used to verify the quality of product components and the effectiveness of the processes used to produce them. Refer to the Reviews & Audits process in the System Quality Assurance Plan (SQAP) program for further guidance on the process and how these will be performed.

5.5.3 Testing

Testing of product components is one of the key methods used to validate that the finished product complies with the product requirements. Unit, integration, systems and various forms of acceptance testing are usually necessary to validate the product. Testing requires adequate planning, staffing, tool usage and numerous iterations until an adequate level of product quality is achieved. Refer to the master test plan (TN0401) for detailed information on the process and how these will be performed.

5.6

5.7 PROJECT TOOLS

5.7.1 Hardware Development Tools

The following Hardware development tools are used:

- Auto2000 — To generate loop schematic drawings
- CAM350 — To convert Gerber file to DXF format file
- PowerPCB 3.5 — P.C. Board layout design tool
- Power Logic 3.0 — To generate schematic drawings
- Pathwork32 — Tools to work with Digital VAX
- Hardware change management tools
  - PVCS tracker 6.5.02
  - PVCS Version Manager 6.5

The Hardware engineer uses Power Logic to design electronic circuit boards and generate schematic drawings. The P.C. Board design expert uses PowerPCB to develop layout drawings and uses AutoCAD to generate detailed drawing. The Bill of materials then will be entered into Macola Information System, the HF Controls Cooperation database system.

Refer to procedures for hardware development (procedure WI-ENG-101) and P.C. Board design (procedure WI-ENG-102).

5.7.2 Software development tools

The following Software Development tools are utilized:

- Source and executable code development tools
  - DEC3100 Digital MicroVAX
    - Digital EVE editor
    - Intel Cross Assembler, PL/M compiler, linker and locater (x86)
  - PC server
- Source code version control tools
  - Microsoft SourceSafe
  - PVCS Version Manager 6.5
  - Digital CMS/MMS library on Digital DEC3100 MicroVAX
- Software code change management tools
  - PVCS tracker 6.5.02
  - Digital CMS/MMS library on Digital DEC3100 MicroVAX.

The referenced procedures are System Software Functional Specification (procedure WI-ENG-202), Design Specification (procedure WI-ENG-203), and Software Coding procedure (procedure WI-ENG-204).

5.7.3 Application development tools

- AutoCAD 2000
- ECT PromisE CAD tool
- Microsoft Office 2000 suite
- Macola on HF Controls LAN, tools to maintain Bill of Materials
- Application code change management & impact assessment tools
  - PVCS tracker 6.5.02
- HFC One-Step Graphic Editor

Referenced procedure is Application Engineering Design Process (procedure WI-ENG-702).

5.7.4 Change Management

- PVCS tracker 6.5.02
- PVCS Version Manager

And procedure is covered in the HFC Work Instruction WI-ENG-003.

5.8 RESOURCE MANAGEMENT

5.8.1 People Resources

The Project Steering Committee and representatives of Manufacturing, Procurement and Test have reviewed the technical and commercial requirements of the project, the proposal scope and budget estimates for the resources required to perform the various functions of design, development, implementation, procurement, manufacture and testing. The process is discussed in further detail in the Project Management Overview (WI-ENG-912). The project team led by the Project Manager develop a Master Project Schedule including all of the project documentation deliverables, engineering tasks, scope definition tasks, procurement tasks, product development tasks, manufacturing tasks, system testing tasks, V&V reporting tasks, V&V testing tasks etc. The resource requirements for the project are broken down per the functional labor groups with budgeted hours for each group. The functional groups will be allocated to the appropriate tasks of the Master Project Schedule to determine an estimated time-phased manpower loading requirements for the project. The time-phased manpower requirements for this project will be overlaid on the know requirements for other projects and evaluations made by the various department managers as to whether the time-phased manpower requirements for this project can be met with existing staff. If the manpower requirements cannot be met with current staffing then contingency plans are discussed and reviewed by upper management. The various contingency plans in order are as follows:

- Borrowing manpower from other departments
- Outsourcing of Engineered deliverables
- Temporary Labor
- New Hires

Temporary Labor is generally utilized to fill the non-technical resource requirements such as drafting, clerical etc. In each of the above cases, any possible candidates will be evaluated and interviewed first by Human Resources and then by the lead engineer of the appropriate area to ascertain that the individual or firm has the capabilities to perform the work required. In the case of outsourcing Purchasing will perform the initial evaluation of the persons or firm.

Table 3, Summary of operational number list

Operation Number	Operational Category
0011	System Engineering
0012	Hardware Engineering
0013	Software Engineering
0014	Application Engineering
0015	Test Engineering
0016	Package Engineering
0017	Drafting
0018	Project Engineering
0019	Project Management
0100	Production/Manufacturing
0101	Manufacturing Engineering for project
0102	Manufacturing for project
0103	System Testing for project

5.8.2 Physical Resources

To be most effective in the execution of the project a determination was made that all of the project team engineering and support personnel would be located in the same area. Once the initial manpower requirements for the Engineering portion of the project were determined, areas within the building to consolidate the Project Team were evaluated. Since a major portion of the manpower would be required for new product and software development and space and office furniture was available in this area of the building the project team was located in this area. It was decided to have everyone one the Project Team Compatible with Microsoft Windows 2000 and Office 2000.

HF Controls has sufficient floor space in manufacturing test system for this project. Please refer to the master test plan (TN0401) for further details on the facilities available for testing of the equipment and software. Once the time for the manufacturing of the system gets closer we have to evaluate the impact of this project on other projects that, may be sold later.

5.9 COST MANAGEMENT

The Baseline budgets are maintained to include any manpower and material cost changes associated with any agreed to contract scope changes. The Estimated budget is spread

across the duration of the project in accordance with the estimated time-phase manpower requirements of the Master Project Schedule. The estimated budgets will be adjusted as the project proceeds through the life cycle to provide the best estimate of the requirements to complete the project.

6.0 RISK ASSESSMENT

Complete a Risk Assessment in order to identify and communicate areas where the project is vulnerable.

Risk is defined as the probability of deviation from the expected result. Taking risks is a part of doing business in our competitive industry. Many of our great successes, which make us the industry innovator, were originally considered risks. While taking a calculated risk is acceptable, it is *not* acceptable to take a risk without understanding it's magnitude and possible ramifications and without taking necessary steps to manage the risk.

The Risk Assessment will identify potential threats to the project, which may require specific actions. Once the Risk Assessment is complete and the results are known, the Project Team should identify and estimate the necessary activities to reduce the high and medium risk(s) to the lowest practical level. The Project Steering Committee will evaluate the activities and approve the final course of action. Once approved, these activities must be incorporated into the existing Product Development Plan.

Table 4, Project Risk Management Assessment

RISK TYPE	IDENTIFICATION	MITIGATION ACTIONS
Schedule	Schedule impact - The development requirement of resource during the first 6 months, some are contractor or vendor - Tight production schedule	1. Retain key project staff; no reassignment to other projects. 2. The use of tools to automate project processes and to promote staff effectiveness and efficiency. Appropriate tools may allow reduction in staff levels and may improve quality of deliverables. Planning for appropriate tool training. 3. Utilize contractor resource.
Regulatory **Legal** **Safety**	V & V programs Are nuclear safety system standards and regulations requiring legal/contractual constraints that would put the project at risk from a financial or legal liability point of view	1. Adequate up-front product definition of standards and regulations applicable to the work to be performed. – Through V & V programs. 2. The guidance from consultants.
Regulatory **Legal** **Safety**	Configuration & Change Management Are there data safety precautions such as offsite storage, frequent backups, logging, data replication, etc., that would cause the project to be economically or technically unfeasible?	1. Adequate change management of project requirements to ensure requirements do not "creep in" in during the life of the project without being identified. 2. Adequate definition of qualification system and tasks and adequate project quality reviews, inspections and audits to ensure regulatory requirements are being met.

RISK TYPE	IDENTIFICATION	MITIGATION ACTIONS
Technological	Three microprocessor controllers SBC06N is the first time to use three microprocessors on one board with different function.	1. Adequate design review and prototype testing.
	Is more than 20 remotes an issue over C-link?	1. Adequate design review and prototype testing. 48 nodes is limitation for current CPC software.
	Do we need to have MCM any more?	1. To use SBC06N as MCM (MUX communication master)
	Is all the technology needed for the project available for immediate use?	Adequate technology evaluation process, including product and vendor evaluation.
	Is system performance a major requirement?	Prototyping of new technology to ensure feasibility, performance, reliability, usability, etc.
	New development/modify boards - Layout out process	Hire outside contractor for layout work.
	FPD & Driver	Adequate design review and hire outside contractor to design FPD real time drive.
	Power supply	Adequate design review and hire outside contractor to design power supply.
	Qualification Test System - New components - Possible buying components/assembly.	
	New package of modular chassis - Power Supply - Control Switch Modules - New P.C. Board & chassis	

7.0 PROJECT RESOURCE ASSIGNMENT

The following table illustrates the original resource plan for this project. The resource shall be updated in the project master schedule continuously throughout the project.

Table 5, Project Resource Assignments

Tasks	Description	HFC (Hours)		Responsible
		Proposal	Revised	
Test Plan Development	Development initial test plan	12		J. Taylor
	Internal & External review & comments	10		J. Taylor
	Resolve Comments & issue plan	6		J. Taylor
TSAP Development	Define TSAP Application • Functional requirement specification • Logic Diagram • CAD	 60 30 40		 J. Stevens/J. Taylor J. Stevens J. McGregor
	Develop TSAP Software Specification	108		J. Stevens

	Develop TSAP Application Program	120		J. Stevens
	Develop Test Simulator Program	100		J. Taylor
Test System Definition & Development	Define Test System (hardware, software, Arrangement, etc.) • Develop System Description	64		T. Gerardis /J. Taylor
	Develop Test System Configuration & Physical Drawings • Develop Configuration Drawings • Develop Physical Arrangement & Mount Details • Develop Wiring Drawings (loop, Power, Monitoring, etc.) • CAD	36 54 40 60		J. Stevens J. Stevens J. Stevens J. McGregor
	Develop Configuration Management Document	40		A. Hsu
	Develop System Setup & checkout procedure	64		J. Stevens/J. Taylor
Develop Test Procedures	Develop Operability Test	10	90	J. Taylor/A. Han
	Develop Prudency Test	8	72	J. Taylor/A. Han
	Develop Burn-in Test	6	54	J. Taylor/A. Han
	Develop Environment Test	12	108	J. Taylor/A. Han
	Develop Seismic Test	15	135	J. Taylor/A. Han
	Develop Surge Test	12	108	J. Taylor/A. Han
	Develop Isolation (1E to non-1E) Test	20	180	J. Taylor/A. Han
	Develop EMI/RFI Tests	20	180	J. Taylor/A. Han
	Develop ESD Test	12	108	J. Taylor/A. Han
	TSAP Test Procedure (To support V & V)	15	135	J. Taylor/A. Han
Verification & Validation	Review and finalize software QA plan			
	ASOA • Verify ASOA Spec. and programming • Perform ASOA Validation • Prepare ASOA V & V Report	96		S. Yang

	TSAP • Verify TSAP Specification and program • Validate Testing of TSAP • Prepare TSAP V & V Report			
Testing Activities	Development Test Mounting & Data Collection System • Define hardware Requirement & Configuration • Define Data Logging Requirement • Build Test Monitoring System • Configuration & Program System	36 27 50 60		D. Briner/A. Han D. Briner/A. Han D. Briner/A. Han D. Briner/A. Han
	Perform Factory Test • Assemble Test System & Test Setup • Operability • Prudency • Burn-in	487.5		D. Briner and Test Engineers
	Perform special test • Seismic • EMI/RFI • Environment • ESD & Surge Withstand	60 50 40 40		J. Stevens J. Taylor J. Stevens J. Taylor
	Perform Post Qualification Testing Operability, etc.	200		D. Briner and Test Engineer
Analysis	Reliability & availability Analysis Report	160		J. Taylor/A. Han
	Accuracy & Setpoint Report	16		J. Taylor/A. Han
	FMEA	144		M. Hallett
	Radiation Hardness Assessment			
Reports	Develop pre-Qualification Test Report	96		J. Taylor/A. Han
	Develop Environmental Qualification Report	24		J. Stevens
	Develop Seismic Qualification Report	20		J. Stevens
	Develop Surge, ESD and isolation Qualification Report	36		J. Taylor
	Develop EMI/RFI Report	36		J. Taylor

	Develop Final Summary Report	32		J. Taylor
	Develop Topical Report for subtotal	32		J. Taylor
NRC interface & Resolution of Issues	Qualification Kickoff Presentation	20		J. Stevens
	In process Presentation & meetings (2)	32		Engineers
	Subtotal Meeting	30		Engineers
	NRC Audit of HFC	70		C. Fisher/A. Hsu
	Resolve NRC questions & meetings	64		C. Fisher/A. Hsu
Generic Software Qualification	Application Software Objectives Acceptance (ASOA) • Define ASOA Components & Program • Develop ASOA Functional Specification • Develop ASOA Test Procedure	 12 24 24		 J. Stevens J. Stevens J. Stevens
	Operating System Software • Define OS Components & Program • Develop OS Functional Specification • Develop OS Test Procedures	 12 16 16		 T. Gerardis T. Gerardis/A. Han T. Gerardis/A. Han
Project Management & Administration	Project Management	550.4		A. Hsu/J. Stevens
	Administration			
	General Project Expense			
	Travel Expense			
	Test & Test Equipment			
	NRC Review & SER Activities			
	Contingency			
Subtotal		**3586.9**	**4626.9**	
Development Items	16 H/W boards - HFC SBC06N - P.C. Boards layout - Prototype - Integration Test	1600 $5000 per board $5000 per board		Development Team
	Packaging Design HFC-6000	960		
	FPD and Driver	640		
Subtotal		3200		