HF Controls

HFCONTROLS CONTROL SYSTEM

HFC-6000 Control System

Safety-Related Control System Qualification
Test Specimen Design Description

DD0401

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NON PROPRIETARY

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A	4/9/03	Jonathan Taylor	John Stevens	Allen Hsu

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Section 1

GENERAL INFORMATION

1.1 INTRODUCTION

This document provides a detailed description of the hardware components that will make up the HFC-6000 to be presented to the NRC for qualification as a generic controller for safety-related systems.

1.2 REFERENCES

EPRI TR-107330	Generic Requirements Specification for Qualifying a Commercially Available PLC for Safety-Related Application in Nuclear Power Plants
TN0401	Master Test Plan
7000901-01	HFC-6000 Product Line Specification
7000902-01	HFC-SBC06 Controller Design Specification

1.3 ABBREVIATIONS AND ACRONYMS

BIT	Built-in Test
CPC	Communication Protocol Controller
CRC	Cyclical Redundancy Check
CSM	Control Switch Module
DCS	Distributed Control System
EWS	Engineering Workstation
HFC	HF Controls
ICL	Intercommunication Link
I/O	Input/Output
JCRT	Java CRT Workstation
LAN	Local Area Network
M/A	Manual/Automatic
NRC	Nuclear Regulatory Commission
PCC	Peripheral Communication Controller
PID	Proportional Integral Derivative. A type of analog control algorithm.

RTD	Resistance Temperature Detector
SOE	Sequence of Events
TSAP	Test System Application Program. A "synthetic application" used to check/verify the PLC functionality needed to support the qualification test program.

Section 2

COMPONENT OVERVIEW

2.1 GENERAL

HFC has developed and currently markets control systems having two distinctively different architectures. The AFS-1000 architecture is employed primarily for applications that employ single loop control of field equipment from a remote location (low density I/O). The ECS-1200 architecture is employed primarily for DCS applications and provides high density I/O that can be positioned either in a remote control room or physically near the equipment under control. Both architectures are composed of modular components that permit specific configuration of the control system with the level of complexity appropriate for a specific application. HFC-6000 is a new control system product line that incorporates features of both the AFS-1000 and ECS-1200 architectures. Components of this product line will be used to create a fully functional control system complete with system software and a test system application program (TSAP). This control system will constitute the Test Specimen for NRC qualification. Because these components will represent all functions of the HFC-6000 product line, the Test Specimen will permit detailed evaluation of the controller hardware and software without limiting the scope, complexity, or physical arrangement of the control system for any particular installation. A detailed definition of the qualification envelope encompassed by this system will be provided in Section 4 of this document.

2.2 TEST SYSTEM HARDWARE CONFIGURATION

Figure 2-1 illustrates the overall layout of the Test Specimen and indicates the boundary between the safety-related and non-safety-related portions of the system. Only the safety related portion of the system will be subjected to the qualification tests described in the Qualification System Master Test Plan, TN0401.

The Test Specimen will be composed of four 19-inch card chassis mounted on an open cabinet frame to simulate cabinet installation. These card chassis will encompass every feature of the HFC-6000 architecture to be qualified. (This requirement will determine the total number of card chassis to be included in the Test Specimen.) One of these chassis will be configured with redundant controller hardware, the system power supply, and I/O modules linked directly to the controller. Two of the remaining card chassis illustrated in Figure 2-1 will be linked directly to the controller as expander I/O chassis. The remaining card chassis (labeled local I/O in Figure 2-1) will contain a power supply module and I/O cards linked to the controller via a fiber-optic communication link. The overall configuration will simulate the hardware arrangement of a redundant remote controller that is physically located in an equipment room and a local I/O chassis that is physically located near the equipment under control.

The controller hardware will support two redundant serial communication links:

- A redundant Intercommunication Link (ICL) enables direct connection with up to a total of 64 I/O cards (or a maximum of 1024 I/O points), which may be located in the same chassis as the controller, an expander chassis, a local I/O chassis, or a combination of local and remote chassis. When configured to communicate with a local I/O chassis, a redundant fiber-optic link will serve as the communication medium to ensure electrical isolation from non-class 1E equipment.

- A redundant Communication Link (C-Link) provides the communication gateway with external workstations. This network is an Ethernet LAN that employs the TCP/IP protocol to enable data transfer between the controller and PC workstations. When more that one controller is connected to the C-Link, each controller acquires link mastership for a fixed interval in a round-robin sequence. While a particular controller is link master, it can broadcast its accumulated data to the link. Between successive masterships, a controller can receive both broadcast data and specifically addressed UCP messages from the link.

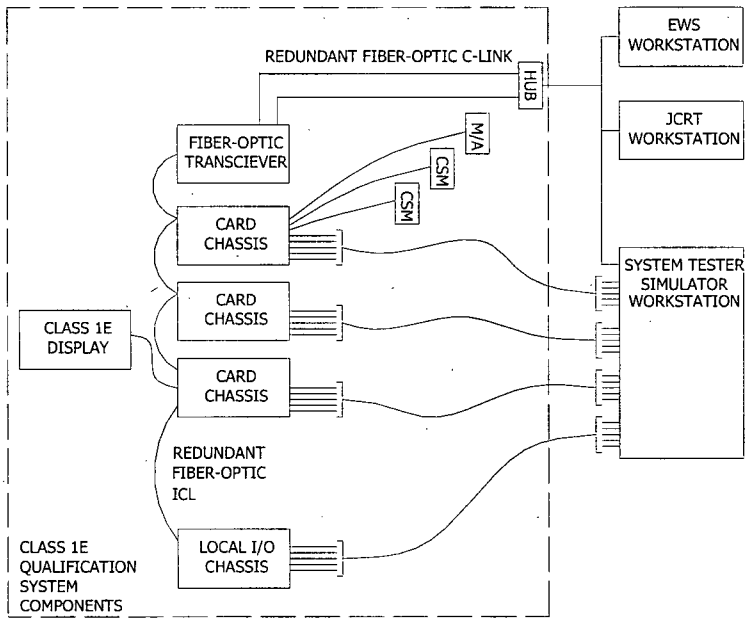

Figure 2-1. Qualification System General Arrangement

2.2.1 MODULAR CARD CHASSIS

The safety-system hardware will be housed in modular card chassis with slots for 14 cards. Each modular card chassis is designed for installation in a standard 19-inch equipment cabinet, to permit direct installation in existing cabinet assemblies. Different backplane assemblies exist for one-loop, two-loop, three-loop chassis, and expander chassis. The controller chassis will include designated slots for redundant controller cards, and a dual-ported memory (DPM) card; all other slots can accept any of the

remaining card types. The expander and local I/O card chassis will be identical. This assembly will not accept the controller or the DPB cards but will accept all other card types. All backplane assemblies will provide traces for the ICL and power lines; connectors on the backplane will provide the interface for connecting field I/O cable harnesses and power source cables. The design will permit either the use of a separate power supply rack or redundant power modules installed in the chassis. The arrangement of all card chassis will be designed to facilitate routing of bundled signals wires from the interface with I/O cards either to a disconnect plug or to individual terminals for the field wiring. Because power distribution and fusing will be integral to each chassis, a retrofit installation can be accomplished by mounting the chassis in an existing cabinet, connecting the power supply to the facility ac power source, and routing the I/O wires to the appropriate field terminals.

2.2.2 CIRCUIT CARD HARDWARE

The qualification system will include at least one example of every module type to be qualified. All hardware designs are based on an architecture that HFC has employed over many years. However, these existing designs will be repackaged using surface-mount hardware to produce a completely modular architecture. The complete set of hardware modules currently planned for the HFC-6000 product line is listed in Table 2-1. The qualification system will include at least one of each card type to be qualified. Additional card types may be added following initial qualification.

Table 2-1. HFC-6000 Product Line Family

Designation	Function

Table 2-1. HFC-6000 Product Line Family (Cont)

Designation	Function

2.2.3 REDUNDANT CONTROLLER ARRANGEMENT

A redundant HFC-6000 controller will be composed of two HFC-SBC06 controllers and an HFC-DPM06 (Dual-Ported Memory) card to be installed in adjacent card slots. The two controllers will have identical system software and the same application program installed.

2.2.4 I/O CARDS ASSEMBLIES

Name Format HFC – (a)(b)(c)(d) N

(a) Identifies basic card types
A – Analog
D – Digital
C – Special Function

(b) Identifies primary card function
I – Input
O – Output
C – Combination of both input and output

(c) Identifies number of channels on the card

16 – 16 channels total
32 – 32 channels total
33 – Two 120-vac output channels, 12 48-vdc DI channels
34 – Two 125-vdc output channels, 12 48-vdc DI channels
35 – One 120-vac output channel, 12 48-vdc DI channels
36 – Eight AI channels, eight AO channels

(d) Identifies specific signal characteristics
A – 120 vac
B – 125 vdc
C – 24 vdc
D – 48 vdc
E – 0 to 10 v (analog)
F – 4 to 20 mA (analog)
G – 250 vdc
H – 220 vdc
I – SOE DI
J – Form C Relay Contact
K – Pulse
L – Thermocouple
M – 100-ohm RTD
N – 200-ohm RTD
P – 2000-ohm potentiometer input
Q – Special Function

2.2.5 C-LINK HARDWARE

2.2.6 ICL HARDWARE

2.2.7 CLASS 1E DISPLAY

2.2.8 DIGITAL LOGIC CONTROL

Operator inputs for digital logic control functions normally consist of one or more discrete inputs and one or more LED outputs. The Test Specimen will include three forms of HMI for digital logic: the CSM, the flat panel display, and interactive graphics of the JCRT. The CSM provides from one to four switch positions, each of which may have display only, switch only, or switch/lamp functions, depending on the specific application. The CSM serves as the primary operator interface with the control system

for control of a single function (motor, valve, relay, etc.) implemented with Boolean logic. The CSMs may be used exclusively for this purpose, or they may be used in parallel with the flat panel display and JCRT.

CSMs having a single switch and/or LED will be connected to the ordinary digital I/O interface of the Test Specimen. All other CSMs will have an RS-485 serial port.

The JCRT software provides the capability of supporting interactive graphics for display of overall system status and enabling overall operator control of the process. Refer to paragraph 2.2.11 for additional information on the JCRT control functions.

2.2.9 ANALOG LOGIC CONTROL

The flat panel display, M/A stations, and JCRT graphic meter face displays will provide the HMI for analog control functions. These functions include selection between auto and manual modes, control of the output value in manual mode, and adjustment of the setpoint value in auto mode. Adjustment of alarm setpoints and PID tuning parameters is a maintenance function, so these parameters will not be accessible from the flat panel display. However, when the controller is in tuning mode, the M/A station can be used to modify and save tuning parameters to flash memory of the master controller.

Each M/A station will include an RS-485 serial port

2.2.10 TEST SPECIMEN SYSTEM POWER DISTRIBUTION

The HFC-6000 product line will include both a separate power supply rack and modular power supplies that can be installed in individual logic chassis. Test Specimen will have a power supply rack to provide operating power to the three racks that represent the main portion of the controller hardware; the local expansion rack will contain the separate modular power supplies. Each power supply will produce redundant +24 and +48-vdc outputs. The +24-vdc power lines will be diode auctioneered on each card in the chassis to produce onboard logic power. The +48-vdc power will be used to supply excitation voltage for external relay contacts and for field transducers. The +24-vdc power will be referenced to a common chassis ground; a DIP switch option will permit selection of either isolated or common configurations for the excitation power.

2.2.11 NON-CLASS 1E EQUIPMENT

The qualification system will include at least one non-class 1E workstation. That workstation will have the HFC suite of software for the EWS and JCRT PC workstations installed. The EWS and JCRT PC workstations constitute a standard software installation for most HFC control systems and provide comprehensive utilities and tools for status monitoring, system control, testing, and maintenance of the overall control system installation. An HPAT automated tester workstation will also be included as part of the overall test configuration for the Test Specimen. This assembly is a special unit designed to support automated testing of HFC control systems and is not actually a part of the Test Specimen. Both the PC workstation and the HPAT unit will be connected to the C-Link through the isolator hub.

2.2.11.1 EWS Workstation

•

2.2.11.2 JCRT Workstation

2.2.11.3 System Tester/Simulator

The system tester/simulator consists of a PC workstation, a non-redundant ECS-1200 controller, and an ECS-1200 I/O rack with the ECS-series card types needed to exercise the I/O channels installed in the Test Specimen. The PC workstation will have automated test software installed along with the complete suite of EWS and JCRT software utilities. The ECS controller will have an application program installed to provide specific simulations for the field hardware controlled by the TSAP. This arrangement will support all phases of dynamic testing, including functional verification of system operation and simulation of failure conditions.

Section 3

TEST SPECIMEN CONFIGURATION

3.1 INTRODUCTION

This section will define the number and type of hardware components to be included in the Test Specimen and provides a detailed summary of operating specifications for each module type.

3.2 TEST SPECIMENT EQUIPMENT

The overall arrangement of the Test Specimen is described in Section 2 of this document. As a minimum, the Test Specimen equipment will be configured to provide the following:

- At least one of each module type to be qualified, including I/O modules, controllers, ancillary devices, and additional modules needed to satisfy requirements of operability and prudency testing.

Table 3-1 contains the minimum component count of hardware modules and assemblies to be included in the Test Specimen. Additional components may be included to support I/O requirements of the particular control logic functions selected for inclusion in the TSAP. The hardware components that make up the HPAT controller and its I/O are excluded from this list.

3.3 COMPONENT SPECIFICATIONS

The following paragraphs provide a summary of functional specifications for the major assemblies included in the Test Specimen. For more detailed information about individual assemblies, refer to the specific detailed design specification for that assembly listed in the related publications.

Later

Table 3-1. HFC-6000 Test Specimen Equipment

Quantity	Module Type	Description	I/O Count Per Module

Section 4

TEST SPECIMEN SOFTWARE

4.1 INTRODUCTION

The software installed on the Test Specimen will include a separate executive program on each I/O card, operating system software installed on the HFC-SBC06, and the TSAP.

4.2 OPERATING SYSTEM SOFTWARE

4.2.1 I/O CARD SOFTWARE

Each I/O card will contain a set of common software modules and an algorithm that controls its particular scan processing function. Specific functions performed by this software will include the following:

4.2.2 MASTER CONTROLLER SOFTWARE

The HFC-SBC-06 controller card will contain three separate processors that will each have a dedicated function. All three programs will use a common operating system, and a set of unique modules for each processor will provide the code to perform the specific tasks for that processor. Major controller functions will be as follows:

4.3 APPLICATION PROGRAM SOFTWARE

4.3.1 TSAP SOFTWARE

The TSAP will reside in nonvolatile memory of both redundant controllers. This software will consist of configuration tables that define the internal architecture of the system and specific analog and digital algorithms for test control system functions. The overall scope of the TSAP will include the following:

4.3.2 HPAT APPLICATION SOFTWARE

The HPAT application will reside in nonvolatile memory of the ECS-1200 controller included as part of the tester assembly. This software will consist of configuration tables that define the internal architecture of the system and specific analog and digital algorithms required to support automated testing of the qualification system. The overall scope of the HPAT will include the following:

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Component Design Specification

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1 Introduction

HFC control cards (system controller cards, communication cards, loop controller cards, and I/O cards) use designs based upon one or more Intel x86 microprocessors. The software running on a microprocessor in an HFC card uses a design that is based upon one of two basic software structures: an architecture centered upon an operating system (OS) kernel, or an architecture using a runtime loop. The OS kernel that is used as one of the basic architectural structures is a standard software component that has been developed and is maintained by HF Controls.

The OS component, together with program tasks and interrupt service routines (ISR), perform card functions and handle hardware interfaces. The OS component is composed of a set of x86 real mode Assembly programs (addressable memory: 1 Megabyte) that are self-contained and not hardware specific. The OS is mainly a task scheduler for use in an environment having multiple tasks each of which operate independently of all other tasks. The OS component consists of two parts, an initialization part and a task scheduling part. As shown in Figure 1, the processor executes its internal initialization immediately after powerup or reset. After completing this process, the software executes its OS initialization one time and then begins executing its task scheduling function. Throughout this phase of operation, a scheduled task takes control, performs its task, and then relinquishes control back to the OS, which then grants control to the next task in sequence.

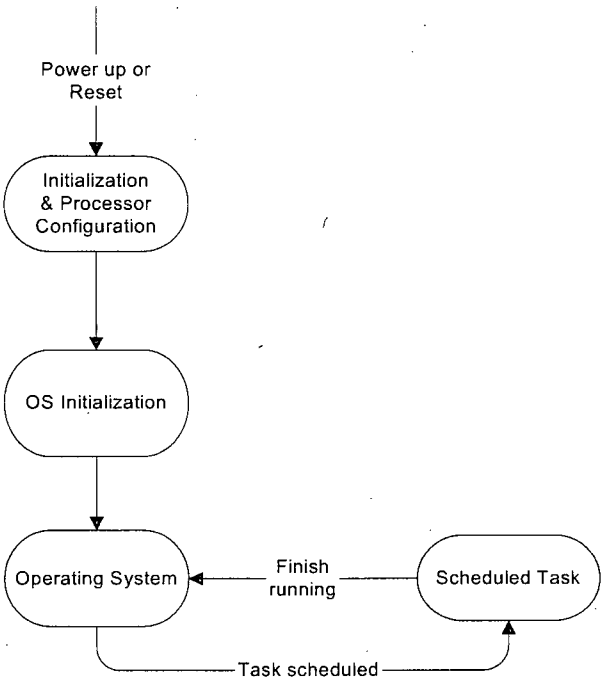

Figure 1 - Operating System Component in a Processor Firmware

The purpose of this document is to serve the needs of software developers, who will use the OS component to build different processor software, and the needs of software maintainers, who modify this component to satisfy new requirements. Subsequent sections of this document provide detailed information about the architecture, interface, design, and implementation of the OS component. Section 3 describes interface layers between the OS component and other software components or modules, as well as the functions provided by the OS component. It also provides descriptions of how to set up the interfaces and use the OS component. Section 4 presents a detailed description of the design and implementation of the component.

2 Functional Description

The real mode OS is the basic kernel of the microprocessor firmware. It starts from the memory address 0FFFF:0000 after the hardware reset (RESET_INT Segment). This OS provides the following functions to allow the microprocessor to perform its defined tasks:

- Initialization: During start up, the initialization part of the OS component executes processor specific initialization sequences to create proper software and hardware environments. These initialization sequences can be implemented individually based on specific hardware characteristics and required functions of that processor. Different initialization routines can be configured for a particular processor and called dynamically by the OS kernel during initialization.

- Tasking: The normal operating mode of a processor consists of sequential execution of the various tasks under control of the OS. The primary task of any remote in a control system consists of executing the application programs for the process(es) under control. Other tasks of a control system remote include communication and diagnostic functions.

- Services: The OS provides a set of service utilities to switch between the OS task scheduling function and the actual execution of the various tasks defined for the processor.

- Synchronization: HFC remotes are designed to support a redundant hardware configuration of controllers. The OS includes features that allow the orderly transfer of control from a primary hardware controller to its backup (secondary) hardware controller. This feature is referred to as synchronization.

The above list presents the major functions performed by the OS component. The functional descriptions provide a context for understanding the operation of the Operating System and how the functions performed by the Operating System work within the overall architecture of a processor firmware. Figure 2 illustrates functional relationships between the OS and the various tasks that it schedules for execution.

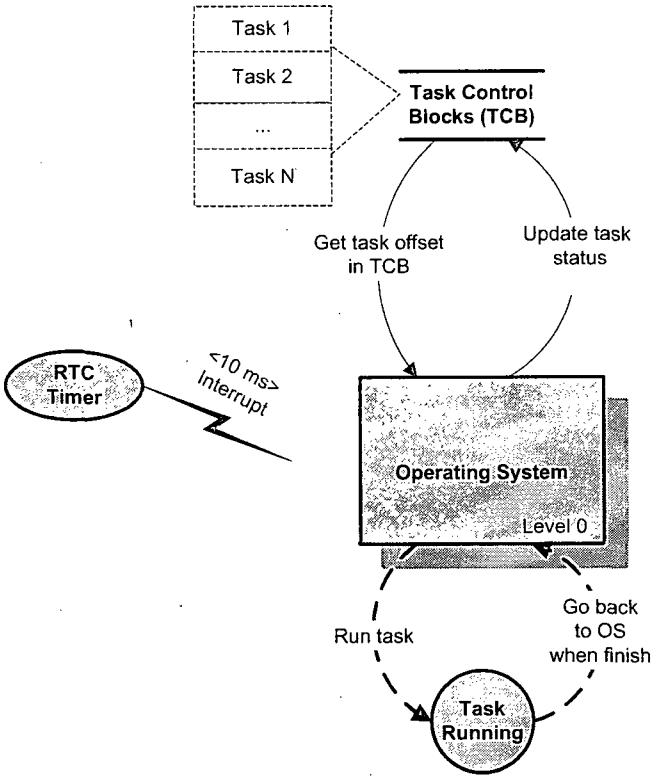

Figure 2 - Component Functional Overview

2.1 Initialization

Upon power up or reset, processor execution begins from the reset vector (RESET_INT located at 0FFFF:0000). From there, it calls the processor initialization routine PROINI to perform processor-related initialization functions.

. Then the OS initialization routine executes the hardware-specific initialization code to create the necessary hardware configuration. After this initialization sequence has been completed successfully, the processor begins regular tasking.

During startup, the initialization part of the OS component initializes its own variables and hardware and software environment particular to that processor by running routines defined in several initialization routine tables (i.e. Interrupts Vectors, Application Program variables and Local Memory Directory for subordinate processors). These tables can be configured in software modules outside the OS component to define the specific initialization routine to call during OS initialization and the list of tasks to run during normal operation for that processor. The OS component calls those configured

initialization routines to set up data structures for the tasks and add the configured tasks to a Task Control Block (TCB).

2.2 Task Scanning

The tasks can be classified into two types according to their configured startup status: an automatic task, which runs continuously after start up; and a dormant task, which runs just once after having been activated. Figure 3 illustrates sequences of status changes for an automatic task and for a dormant task. Automatic tasks are normally background tasks that need to execute their function at regular intervals. Such tasks are used to maintain system timers (mailboxes) or to check for any request coming from the work station. A dormant task performs its function only when it is specifically required. This type of task is used for the Database Manager service task or a message handler.

An automatic task may have any of four status conditions - ACTIVE, DELAY, SUSPENDED, or END. If the TCB for a particular task indicates that its status is DELAY or SUSPENDED, the OS will bypass this task in the current scan. If the TCB entry indicates that the task is in ACTIVE status, the OS will transfer task control to that task, enabling it to execute its function. When the task terminates itself by calling one of OS functions for the termination method required, it returns program control to the OS. Task status is affected by the termination method that it uses.

The OS bypasses any dormant task until some other task request execution of its function. When this occurs, the OS will set its TCB status to ACTIVE and grant control to that task in its proper sequence. When it completes its operation, it changes its status back to dormant, Exits to halt execution, and returns control the OS.

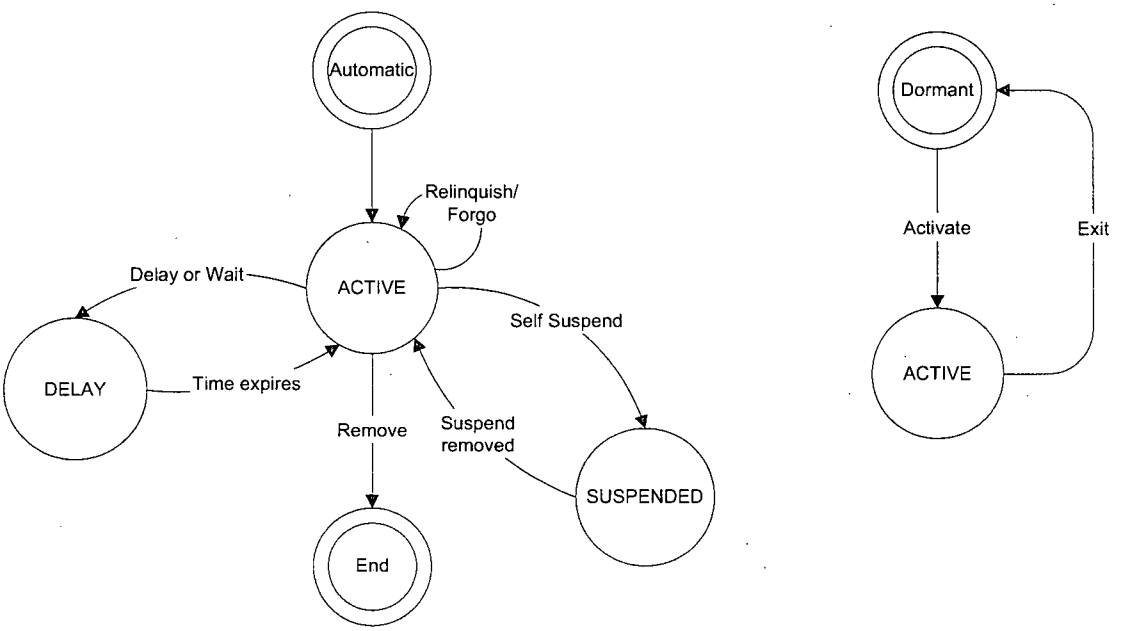

Figure 3 - Status Changes of Automatic Tasks and Dormant Tasks

2.3 Task Scheduling Mechanism

During normal operation, the OS component sequentially scans the TCB list at regular intervals and passes program control to each task in the TCB list that should be scheduled to run. When each task completes execution of its function it returns program control back to the OS component, which then resumes scanning the TCB list for the next active task. In order to ensure reliable transfer of control from the OS to a task and then from the task back to the OS, each task must use one of the OS functions to terminate its execution. While a task is actively performing its function, it can activate a dormant task. When this task returns control to the OS, the OS will execute that previously dormant task the next time it scants its TCB entry. When it completes its function, it will return to dormant status at the time it returns control to the OS. The following subsections describe the OS functions used for task scheduling.

2.3.1 OS Functions for Execution Termination

These functions are normally called at the end of the execution of a task before it returns program control to the operating system. For the multiple processors environment, an "IN SYNC" status bit is used for synchronizing subordinate processors with the Primary/Secondary operating mode of the main processor. If a task provides the same functions regardless of Primary/Secondary status, the task should use OS function that set "IN SYNC" bit. If a task function changes based on Primary/Secondary status, it should use one of the OS functions that does not set the "IN SYNC" bit of the calling task so that the task will be synchronized when the operating mode of the controller changes.

2.3.1.1 Relinquish (RELINQ)

This OS function causes the calling task to relinquish program control, and the OS component will resume TCB list scanning at the point where it left off when the calling task received program control. The end of this function is a jump to the offset pointed to by the OS Re-entry pointer: TSCN_PTR, which is the place where the OS passed program control to this task.

2.3.1.2 Forgo (FORGO)

FORGO function is similar to RELINQ. It also causes the calling task to relinquish program control to the OS component. However, it does not set the "IN SYNC" bit in the TCB entry of that task. The end of this function is also a jump to the offset pointed to by the OS Re-entry pointer: TSCN_PTR.

2.3.1.3 Exit (EXIT)

This OS function causes the calling task to halt execution. It sets the "IN SYNC" bit in the TCB of the calling task to indicate that the task is synchronized with the mode of the controller. The end of this function is a jump to the offset pointed to by the OS Re-entry pointer: TSCN_PTR.

2.3.1.4 Delay (DELA)

This OS function causes the calling task to be delayed by OS component for a specified amount of time (multiple of RTC tick count). An input parameter specifies the RTC tick count of the delay. It sets the "IN SYNC" bit in the TCB of the calling task to indicate that the task in synchronized with the controller operation mode. The end of this function is a jump to the offset pointed to by the OS Re-entry pointer, TSCN_PTR.

2.3.1.5 Wait (TWAIT)

The WAIT function is similar to DELA in that it delays the calling task by a specified multiple of RTC tick counts. However, its function does not set the "IN SYNC" bit in the RTC of the calling task. Tasks requiring mode change synchronization should use this function instead of DELA. The end of function task is a jump to the offset pointed to by the OS Re-entry pointer: TSCN_PTR.

2.3.1.6 Self Suspend (SSUSPE)

This OS function sets "SELF-SUSPEND" and "IN SYNC" bits in the TCB of the calling task. As long as the "SELF-SUSPEND" bit remains set, the OS suspends execution of this task. This function can be used by an event-driven task to suspend itself at a pre-determined point while waiting for a subsequent event to take place. The end of this function is a jump to the offset pointed to by the OS Re-entry pointer: TSCN_PTR.

2.3.1.7 Remove (REMOVE)

This OS function removes the calling task from the TCB list and mark it as removed. The end of this function is a jump to the offset pointed to by the OS Re-entry pointer: TSCN_PTR. Once a task has been removed by this task, it will not be executed gain by the OS.

2.3.2 OS Functions for Task Activation

Two OS functions, Activate (ACTIVA) function and Fast Activate (FAST_ACTIVATE) can be used to activate a dormant task by changing its TCB entry's status word. The only difference between these two functions is that they require different input parameters. The ACTIVATE function requires the task name as its input parameter. The FAST ACTIVATE function requires the offset to the TCB of the task as its input parameter.

2.4 Deterministic task scheduler

Table 1 lists the tasks and task group designations presently defined for processors that run the HFC OS. These tasks can be configured with up to 8 execution sequence groups. Group level 0 is assigned to low priority utility tasks; group level 7 is assigned to the primary function of a remote controller. The OS builds the TCB list based on these sequence groups through the software initialization process. During normal operation, the OS scans the TCB list sequentially. Tasks with the smaller

sequence group numbers are relatively small and are executed quickly. Figure 4 illustrates a controller whose task execution cycle time is set for 100 ms (10 RTC tick times). The function used to start over at the beginning of the TCB list is called a context switch. A context switch will be forced by the OS component at the end of the configured tick time interval. When the OS component detects that it is time to perform a context switch, it starts the TCB scan from the beginning of the TCB list.

. Normally, all tasks will be executed only one time during each context switch interval except the main task for a particular processor. The main task will be executed at least one complete program cycle during each context switch period. A system alarm flag will be set immediately if it fails to complete an entire cycle. A watchdog timer strobe is activated to indicate the health condition of tasks execution in order to provide the sanity signal to the sanity monitoring and failover circuitry.

Table 1. Defined Tasks for Controller Processors

Sequence No.	Tasks	Description	Auto/Dorm	Initial At	Category
Group 0					
Group 0					
Group 0					
Group 0					
Group 0					
Group 0					
Group 0					
Group 0					
Group 4					
Group 4					
Group 5					
Group 7					

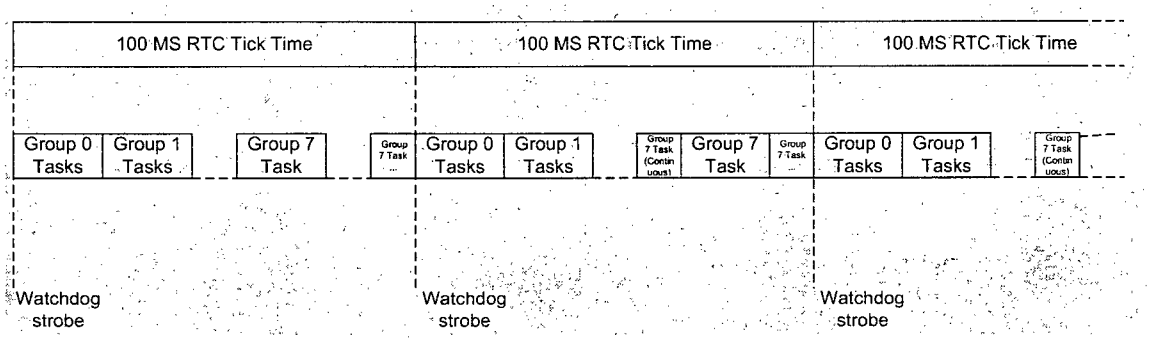

Figure 4 - Deterministic Tasks Scheduler

2.5 Task Status

Each entry in the TCB list includes task status and task attributes. The OS determines whether to execute a task by checking its task status in the TCB entry. A task will be in one of the task status states shown in Table 2 at all times. A task may change the status byte in its own TCB or in that of another task by calling an appropriate OS function.

Table 2 - Task Status

Task Status	Description
DORMANT	Will not be executed
AUTOMATIC / ACTIVATE	Will be executed, starting at the initial entry point
ACTIVE	Will be executed, resuming at the last instruction executed
DELAY	Will be executed after a configurable delay, resuming at the last instruction executed
SUSPENDED	Will not be executed

2.6 Task Execution

During initialization, the status bytes of every TCB in the TCB list should be initialized to either Dormant or Automatic based on the characteristics of the task performed. The OS will not execute any dormant task until its status is changed by another task. It will execute every automatic task starting at its initial entry point.

Each task normally calls an OS function as its last programmed instruction. This OS function terminates execution of the task and returns program control to the OS; it may also update the status byte of the TCB.

2.6.1 Activation

The status of any dormant task can be changed to ACTIVATE by calling an OS function for activation. The OS will then execute the dormant task starting at its initial entry point. If the task's status is already ACTIVE, the ACTIVATE status will be ignored and the task will continue to execute as before.

2.6.2 Termination

Table 3 provides a list of task termination methods. The Exit method is normally used by a dormant task; the other methods are normally used by automatic tasks.

Table 3 - Task Termination Methods

Method	Descriptions
Exit	Tasks status will be changed to DORMANT
Relinquish / Forgo	Tasks will continue to be ACTIVE
Delay / Wait	Task status will be changed to DELAY, and a delay counter initialized.
Self Suspend	Tasks status will be changed to SUSPENDED
Remove	Tasks is removed from the TCB list and will never be executed again

2.7 Message Handling for Communication Processor

2.8 Timing Service

2.8.1 Real Time Clock

An OS Real Time Clock (RTC) routine performs various real-time based functions. For each RTC interrupt, the configurable time based routine queue is scanned. This queue has to be initialized in initialization routines outside the OS component to configure time based routines for the processor's requirements. Each queue entry contains a pointer to the time based routine as well as a frequency counter that defines how many RTC interrupts are required between each execution of the routine.

The RTC routine also calls a hardware dependent macro to execute optional maintenance of a watchdog timer at regular time intervals. Optional OS timers are maintained by the RTC. These OS timers can be used by various tasks as real time counter through the OS_TIMER function.

2.9 Redundancy and Synchronization

In a redundant remote, a controller may be either Primary or Secondary. The Primary controller performs overall status monitoring and coordination for the controller and also

runs the specific application program for the process under control. The Secondary controller functions as a hot spare to take over operation on failure of the Primary controller.

When a controller is operating as part of a redundant remote, problems can develop if some parts of the controller is operating in Primary mode and other parts are operating in Secondary mode. The OS performs a synchronization function at each context switch in order to ensure that all tasks are operating in the same mode as the OS.

The system processor will wait on all of its tasks to be "in synchronization" and then check the processor statuses of all configured subordinate processors. When all processors are "in synchronization", the system processor will then modify the OP_STAT element as "in synchronization", indicating that the controller is now running in synchronization, i.e. all tasks on all processors in the same controller are running in the same Primary or Secondary mode.

3 Component Interface Description

This section describes interfaces to the OS component, OS functions provided by the OS component, how to configure these interfaces during initialization, and how to use OS functions. Figure 5 illustrates the basic interfaces and functions of the OS components.

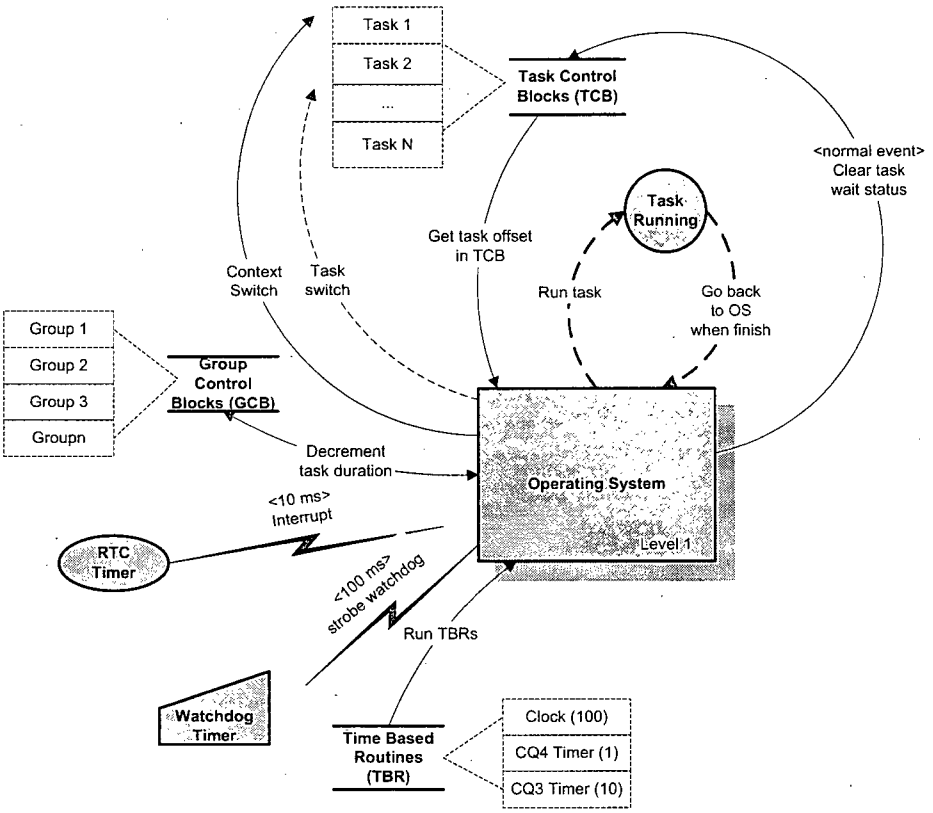

Figure 5 - Overview of OS Interfaces

3.1 Interfaces for OS Initialization and Configuration

A common OS Initialization will be performed during start up. During the OS Initialization, the OS calls every routine listed in several initialization routine tables, which need to be configured in processor specific initialization routines. Different initialization routines are implemented specially according to the hardware characteristics and card functions of the specific processor. The following subsections describe what initialization should be performed or configured for different functions of the OS.

3.1.1 Initialization for Multitasking Scheduling

During operating system initialization, tasks needed for the operation of the card need to be registered with the OS component by placing an entry for each of these task in the TCB list.. These tasks include OS tasks, communication protocol tasks, and processor application tasks. The list of tasks to be added to the TCB list should be configured in processor-specific initialization routines that are separate from the OS.

After all configured tasks are added to the TCB list, the OS initialization routine will rearrange the TCB list linkage according to task priority levels. Tasks with the highest priority level will be listed first in the TCB, followed by tasks with lower priority levels.

When multiple tasks have the same priority level, the task which is registered first is listed first in TCB. Therefore, the ordering of tasks in the TCB is based both on task priority and the order in which the tasks are registered with the OS.

The sequence for registering tasks with the OS is as follows:

- OS Utility Task
- Communication Protocol Tasks
- Processor Specific Application Tasks
- OS Low Priority Tasks

These initialization interfaces are described in paragraphs 3.1.1.1 through 3.1.1.4.

The OS provides two functions that the initialization routines can call to add a task to the TCB list:

- Add Task to TCB function
- Add Channel Communication Task to TCB function

Paragraph 3.1.1.5 describes these two OS functions used to add a task to the TCB list and the data structure that defines a task.

3.1.1.1 Interfaces with the OS Utility Task

The Utility Task is an OS task that can be used to perform various configurable functions. This task is added to the TCB list automatically by the OS, and it is always the first task in the list.

3.1.1.2 Interfaces to Add Communication Channel Tasks

After the Utility Task is added to the TCB list, the OS performs initialization for any configured hardware communication channels. Any specific initialization sequence required to set up the hardware channels and communication protocol tasks need to be implemented separately.

3.1.1.3 Interfaces to Add Processor Specific Application Tasks

After the initialization of communication channels, the OS runs processor-specific initialization routines. These routines are defined in a processor-specific initialization routine table

3.1.1.4 Interfaces to Add Low Priority OS Tasks

As a last part of the task registration sequence, any other configured OS tasks can be added to the TCB list. Since these OS tasks are added at the end, they are normally low priority tasks that don't need to be executed at the beginning of each task scan cycle.

3.1.1.5 OS Functions to Add a Task to TCB List

There are two OS functions that can add a task to the TCB list:

The structure of TASK_ID_STR is described in paragraph 3.1.1.5.1.

The structure of the PACDEF table is described in paragraph 3.1.1.5.2.

3.1.1.5.1 Task ID Structure

The TASK_ID_STR structure is used to define a task to be added to the TCB list by the OS component. The TASK_ID_STR contents are shown in Table 4. The first word indicates task state or status. Bit definitions for the task state word (TSTATE) are listed in Table 5. The second word is task attributes (TATTRB), such as task priority, etc. Bit definitions for TATTRB are listed in Table 6.

Table 4 – TASK_ID_STR Contents

Name	Size (byte)	Description

Table 5 – TSTATE Bit Definitions

Bit	Name	Description	Value
15			
14			
12			
10			
9			
8			
7			
6			
5			

Table 6 – TATTRB Bit Definitions

Bit	Description
2-0	
13-3	
14	
15	

If the option of setting up task duration time and running tasks in a group is going to be used, the group task flag needs to be set for the task attribute word in the task entry ID. Refer to paragraph 2.4 for descriptions of group tasking.

3.1.1.5.2 Packet Definition (PACDEF) Table

The structure of a PACDEF table entry is shown in Table 7. This table will be initialized by OS

Table 7 - Packet Define Table Entry

Name	Size (byte)	Description

3.1.2 Initialization for Time Based Functions

One of the time related functions of the OS is to scan each entry in the Time Based Routine (TBR) table and execute the routine if it is time to run it. Time based routines need to be added to the TBR table during OS initialization.

Table 8 shows the structure of a TBR table entry (TBRDIR_STR).

Table 8 – TBR Table Entry Structure

Name	Size (byte)	Description

The OS also maintains OS timers by decrementing any configured OS timer at each RTC interrupt. These OS timers are software counters stored in an OS timer array (OS_TIMERS). A variable NO_OS_TIMERS defines how many OS timers are configured in the software.

An OS macro can add a timer counter to the OS timer array.

This timer counter will then be configured as an OS timer. At each RTC interrupt, the OS component will decrement the timer counter by one count.

3.2 Interfaces for Real-Time Related functions

An OS RTC routine performs time related functions on a real-time basis, such as executing time based routines (TBR) and maintaining the watchdog timer and optional OS software timers.

A hardware timer is normally set up as a real time clock (RTC) timer and the hardware RTC interrupts will be handled by a processor-specific interrupt service routine. The interrupt service routine should be implemented outside the OS to handle processor specific-hardware interfaces and provide processor-specific functions. This interrupt service routine can call the OS RTC handler (RTC) routine to perform standard time-related functions.

4 Component Architecture and Design Description

This section provides a description of the OS internal architecture, relations, and program control flows among its major routines. These descriptions are for the purpose to serve the needs of software component maintainers for understanding the OS and maintaining its functions and routines. Section 2 and 3 are the preliminary reading required for software maintainers who are not already familiar with OS functions and external interfaces. Section 2 and 3 also set constraints for software maintainers for modifying any part of the design or implementation of the OS. The modified OS should still provide the original functions as described in Section 2 and interfaces as described in Section 3. If any of the OS functions or interfaces is going to be affected by a modification to the OS design or implementation, other software modules that interact with the OS component must be examined to determine if they will remain compatible with one another after implementation of the modification.

The OS component includes the following major routines for its multitasking and process control:

The subsequent paragraphs describe program control flows among the OS routines for major OS functions.

4.1 TCB List Scan

The Sequential Task Scheduler scans the TCB list sequentially and executes each task if the TCB entry indicates that the task should be executed. Before the sequential task scheduler transfers program control to a task, it sets the OS Re-entry pointer to its current execution point. At the end of each task, a Jump instruction returns OS control to the place that is pointed by the OS Re-entry pointer, which is the Sequential Task Scheduler in this case. Therefore, after executing one task, the Sequential Task Scheduler will resume running at the point where it left off and scan the next task in the TCB list.

When the Sequential Task Scheduler executes the task, it sets the controller card's LED to indicate which task is being executed. If any fatal error occurs during execution of the task, the card's LED will freeze with the defined LED sequence for this task. This function is for the purpose of card diagnostics and troubleshooting. Table 9 provides the structure for a TCB table entry (TCB_STR).

Table 9 - Task Control Block Entry

Name	Size (byte)	Description

4.2 RTC Interrupt Handler

When an RTC interrupt occurs, the RTC interrupt service routine will call the RTC handler. The RTC handler will perform time related functions for the card.

The RTC handler will scan each entry in the TBR table (Section 3.1.2), decrement the tick counter and execute each time based routine when the tick count expires. The tick counter is then reset to the initial value for the next time out.

The RTC handler activates the watchdog timer by strobe at regular intervals. It maintains an OS timer array by decrementing each configured OS timer at each RTC interrupt.

The RTC routine decrements delay counters of all tasks in DELAY status. When the delay counter expires, the RTC routine will change the task's TCB entry's task status to ACTIVE.

Then the RTC handler decrements the context switch counter and checks if it is time for a context switch of the TCB scan. If it is time for a context switch, the RTC handler will perform a context switch as described in Section 4.2.1.

If it is not time for a context switch yet, the RTC routine will decrement the optional group tasking timers for the Group Control Blocks (GCB) table, and force a task switch to execute the next task group if the timer expires. Section 4.2.2 provides more descriptions of group task switch. The GCB table is the data structure for managing task groups. A GCB table entry (GCB_STR) structure is shown in Table 10. This table will be set up during OS Initialization according to configurations of group tasking.

Table 10 - Group Control Block Entry

Name	Size (byte)	Description

4.2.1 Context Switch

If it is time for a context switch, the RTC handler will set the TCB Scan Pointer to TCB _Head, which points to the beginning of the TCB list, and it will then pass program control to the Event-Driven Task Queue Scan Routine. The Event-Driven Task Queue Scan Routine will first scan the Event-Driven Task Queue and execute every task queued until the queue is empty, then it will pass program control to the Sequential Task Scheduler. The Sequential Task Scheduler will start running from the point that is pointed to by the TCB Scan Pointer, which is TCB_Head in this case of a context switch.

4.2.2 Task Switch for Group Tasking

If it is time for a task switch of the group tasks, the RTC handler will set the TCB Scan Pointer to the next task in GCB table. Then it passes program control to the Event-Driven Task Queue Scan Routine. The Event-Driven Task Queue Scan Routine will first scan the Event-Driven Task Queue and execute every task queued until the queue is empty, then it will pass program control to the Sequential Task Scheduler. The Sequential Task Scheduler will start running from the point that is pointed by the TCB Scan Pointer, which, in this case of a task switch, is the next task in GCB table.

5 Software Files List

All reference software files are organized in the Digital Code Management System (CMS) library. The list attached here is the complete set of files in that particular CMS library. During the process of software file dedication, the configured files will be extracted from these libraries in order to build the firmware for a configured controller.

5.1 Files from SYS CMS library

File Name:

!!SYSTEM Source files!

5.2 Files from OPS CMS library

!! OPERATING SYSTEM FILES!

5.3 Configuration files

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Common Glossary

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Author/Title ANGELA HAN

Reviewer/Title JONATHAN TAYLOR

Approval/Title STEVE YANG

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Revision History

Date	Revision	Author	Changes
2/25/04	A	B. Han	Initial

Acronyms and Definitions

Terms	*Descriptions*
μ	Micron
A	ampere
A/D	Analog/Digital
AAC	Alternate AC
ac	alternating current
ACE	Abnormal Conditions and Events
ACK	Acknowledge, acknowledgement
ADC	Analog-to-Digital Converter
AGC	automatic gain control
AI	Analog Input
AO	Analog Output
ASCII	American National Standard Code for Information Interchange
ASO	Application Object Test
BCD	Binary-Coded Decimal
BISI	Bypass and Inoperable Status Indication
BIST	Built-in Self-Test
BOE	Burst of Events
BOP	Balance of Plant
BPI	bits per inch
Btu	British thermal unit
C	Celsius; also centigrade
CAN	communication array number
CD	Compact Disk
CF	carry flag
CIB	cable interface buffer
C-Link	Communication link (data highway)
CMR	common-mode rejection
CPC	Communication Protocol Controller, i.e. LAN Controller
CPLD	Complex Programmable Logic Device
CPU	central processing unit
CQ4	Analog control subsystem
CRC	Cyclical Redundancy Check
CRT	Cathode Ray Tube
CSM	Control Switch Module
CVC	Constant Voltage Controller

Terms	*Descriptions*
D/A	digital to analog
DAC	Digital to Analog Converter
dB	deci Bell
dBm	decibel meter
dc	direct current
DCS	Distributed Control System
DDB	Dynamic Database
DGSB	diagnostic status block
DHA	Digital High Alarm
DI	digital input
DIP	Dual In-line Package
DLA	Digital Low Alarm
DMA	Direct Memory Access
DMT	Deadman (watchdog) timer
DO	digital output
DPM	Dual-Ported Memory
DRID	destination remote ID
DSP	Digital Signal Processing
EMI	Electromagnetic Interference
EPROM	Erasable Programmable Read-Only Memory
ESD	Electrostatic Discharge
EUT	Equipment Under Test
EWS	Engineering Workstation
F	Fahrenheit
FIFO	first in first out
FMEA	Failure Modes and Effects Analysis
FOT	Fiber-Optic Transmitter
FPC	Flat Panel Display Controller
FPD	Flat Panel Display
ft	foot
GND	ground
GPI	general purpose interface
H	hexadecimal
HAI	high-level analog input
HAO	high-level analog output
HAS	Historical Archiving System
HEX	hexadecimal
HFC	HF Controls
HIFR	Host Interface Remote
HMI	Human Machine Interface
HPAT	HFC Plant Automated Tester
HSIM	High Speed Interface Module
Hz	Hertz (cycles per second)

Terms	*Descriptions*
I/O	Input/Output
IC	integrated circuit
ICL	Intercommunication Link
ILI	I/O link isolator
ILR	I/O link repeater
ILT	I/O terminator
INIT	initialize
INT	Interrupt
IOC	I/O card
IOIF	I/O Interface
ISR	Interrupt Service Routine
JCRT	Java CRT Workstation
k	1024 binary digits
k	kilo (thousand)
kHz	kilohertz
LAI	low-level analog input
LAN	Local Area Network
lb	pounds
LED	Light Emitting Diode
LLC	Logic Link Control Layer
LOV	Loss of Voltage
LSB	least significant bit
M/A	Manual/Automatic
M/A Station	Manual/Automatic Station
mA	milli Ampere
MAC	Medium Access Control Layer
MCL	Master Configuration List
MFM	Master for a Moment Protocol
mm	millimeter
MMI	Man-Machine Interface
ms	millisecond
MSB	most significant bit
MSS	Maintenance Subsystem
MTP	Master Test Plan
MUX	Multiplex
N	newton
NACK	No Acknowledge, negative acknowledge
NIC	Network Interface Chip
NiCad	nickel-cadmium
NMI	Nonmaskable Interrupt
NRZ	non-return to zero
NSSS	Nuclear Steam Supply System

Terms	*Descriptions*
OBE	Operating Basis Event
OIS	Operator Interface Subsystem
OS	Operating System
OTDR	Optical Time Domain Reflectometer
PAL	programmable array logic
PC	Personal Computer
PCB	Printed Circuit Board
PCC	Programmable Communication Controller
PCS	Plant Control System
PDS	Previously Developed Software
PDU	Protocol Data Units
PID	Proportional-Integral-Derivative
PIP	peripheral interface port
PLC	programmable logic controller
PMS	Plant Monitoring System
PPM	parts per million
PROM	programmable read-only memory
PWR	Pressurized Water Reactor
QA	Quality Assurance
QC	Quality Control
RAM	Random Access Memory
Rf	Radio Frequency
RFI	Radio Frequency Interference
RMS	Root mean square
ROM	Read-Only Memory
RRS	Required Response Spectrum.
RSP	Remote Shutdown Panel
RTC	Real-Time Clock
RTD	Resistance Temperature Detector
RX	receive, receiver
SBC	Single Board Computer
SOE	Sequence of Events
SRS	System Requirements Specification
SSE	Safe Shutdown Earthquake
SSP	System Safety Plan
SSR	solid state relay
STP	System Test Plan
SVVP	System Verification and Validation Plan
SWC	Surge Withstand Capability

Terms	*Descriptions*
T/G	Turbine Generator
T/O	Timeout
TB	Transaction Buffer or Tagged Block in the public memory
TC	Thermocouple
TCB	Task Control Block for Operating System
TCI	thermocouple input
TCP/IP	Transmission Control Protocol/Internet Protocol
Test Specimen	A specific combination of hardware and software components to be subjected to specified test conditions
TID	Total Integrated Dose
TOD	Time of Day
TPM	Tri-Ported Memory
TSAP	Test System Application Program
Tx	Transmit
UART	universal asynchronous receiver/transmitter
UCP	Universal Communication Packet
UL	Underwriters Laboratories
UPS	Uninterruptable Power Supply
USART	universal synchronous/asynchronous receiver/transmitter
vac	volts alternating current
VCP	Vertical Coupling Plane
vdc	volts direct current
VDD	positive power supply terminal
vrms	volts root mean square
w	watt
WT	watchdog timer

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HFC-6000 Product Line

HFC-SBC06-DPM06
Module Detailed Design Specification

DS901-000-01

Rev B

NON-PROPRIETARY

Effective Date	5/15/07
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1. Introduction

This HFC-SBC06 board and HFC-DPM06 board function together as a System Controller Module in a HFC-6000 control system. The overview of the architecture, functions and module structure of the HFC-SBC06 board and HFC-DPM06 board are provided in document MS901-000-01, HFC-SBC06-DPM06 Module Design Specification. The user of this document should be already familiar with document MS901-000-01. This document provides detailed structure and design descriptions on specific parts or features of the HFC-SBC06 board and HFC-DPM06 board, including hardware characteristics and software implementation methods.

2. Hardware Detailed Design for HFC-SBC06

2.1 Module Specification

- Assembly 400417-01 Pentium 100 CPU, CAT5 Connections via front card edge, commercial grade connections
- Assembly 400417-81 Pentium 133 CPU, CAT5 Connections via backplane, industrial grade parts

2.1.1 Environmental Extremes for Reliable Equipment Operations

• Temperature:	0° to 55° C (operating) 0° to 70° C (storage)
• Humidity:	5% to 95% RH, non-condensing

2.1.2 Board Specification

• Supply Voltage	+24 VDC
• Maximum Power Dissipation	18 Watts
• Onboard Clock Rate(s)	
Microprocessor Clock	50 MHz
CPC & ICL Processor Clock:	50 MHz
ICL Bit Rate Clock:	11.0592 MHz
CPC Serial Data Clock:	20 MHz
SOE Master Clock	4.000 MHz

- Mounting Requirements

The HFC-6000 product line includes both 19- and 23-in. controller chassis. Slots 12 and 14 of the 19-in. controller rack are designed to accept HFC-6000 controllers; slots 16 and 18 of

the 23-in rack are designed for controllers. The slot between the two controller positions is designed to accept an HFC-DPM06 assembly.

2.1.3 C-Link - IEEE 802.3 10BASET Communication Links

• Transmission medium	100-Ω twisted pair cable, unshielded 22 to 26 AWG wire
• Maximum segment length	100 meters
• Network specifications	Standard IEEE 802.3 10BASET

The 10BaseT connection can be made either by the front card edge or via the HFC-6000 backplane through the HFC-HUB06.

Installed wired jumpers required to use the front card edge CAT5 connectors J7 and J9:
W10-W11, W13-W14, W16-W17, W19-W20, W22-W23, W24-W25, W28-W29, W31-W32, W34-W35, W37-W38, W39-W40, and W43-W44

Installed wired jumpers required to use the backplane connection with the HFC-HUB06 as the Ethernet interface:
W9-W10, W12-W13, W15-W16, W18-W19, W22-W23, W24-W25, W27-W28, W30-W31, W33-W34, W36-W37, W39-W40, and W43-W44

2.1.4 ICL - EIA RS-485 communication links

• Transmission medium	backplane traces or twisted pair cable
• Signal characteristics	differential signal pair
• Maximum No. of RX/TX on link	32 TX, 32 RX
• Maximum cable length	4000 ft
• Maximum data rate	346 Kbps
• Minimum driver output range	±1.5 V
• Maximum driver output range	±5 V
• Maximum driver short circuit current	250 mA
• TX load impedance	54Ω
• RX input sensitivity	±200 mV
• Maximum RX input resistance	12 KΩ
• RX input voltage range	-7 V to +12 V
• RX logic high level	> 200 mV
• RX logic low level	< 200 mV

2.2 Onboard Power Distribution

2.2.1 Power Distribution

The board receives redundant 24-vdc power feeds from backplane connector P1. The two power feeds are diode auctioneered and routed to transistor switch Q9 at the input of the

onboard power circuitry. Switch S1 in the gate network for transistor Q9 permits the user to enable/disable power distribution to the remainder of the hardware on this board. (Toggleing this switch will force a powerup reset for all onboard microprocessors.) When power distribution is enabled, the combined 24-vdc power line is divided into two branches. One branch is routed to a 5-vdc power regulator that provides operating power for all TTL components on the board. The second branch routed to a 3.3-vdc regulator that provides operating power for the SYS processor and other low-voltage components on the board.

2.2.2 Hardware Reset

The HFC-SBC06 board includes a DS1232 MicroMonitor chip (the SYS Watchdog timer) and a DS1233A EconoReset chip to control hardware reset functions. The MicroMonitor chip monitors the voltage level of the +5-vdc power rail, the state of the onboard reset switch (SW1) and normal cycling of the SYS processor. The EconoReset switch monitors the voltage level of the 3.3-vdc logic power rail connected to the SYS processor and onboard CPLD chips.

When power is first applied to the board, the low state of both logic power rails causes the two chips to hold the RST_IN/ signal at a low level. After logic power increases above 4.5 vdc, the MicroMonitor chip keeps the RST_IN/ signal low for an additional 350 ms to ensure that all transient signals have dissipated before the three processors begin operation. During subsequent operation, the two chips monitor power for a significant drop in the voltage level of the onboard logic power rails.

When the SYS processor begins running the system software, it must supply a low active STROBE/ pulse to the MicroMonitor at regular intervals. If the delay between successive STROBE/ pulses exceeds 1.2 seconds, the MicroMonitor chip automatically activates the RST_IN/ signal to reset all three processors on the card. The operator can initiate reset of all components on the card by toggling the S1 power switch on the board.

2.3 Connector Pinouts

The HFC-SBC06 system controller board has one backplane connector (P1) and two RJ45 connectors for communications ports (J7 and J9). The backplane connector (P1) provides contacts for power, communication with the DPM, and the serial ICL for communication with I/O cards in the controller card rack. The two RJ45 connectors provide the interface with the redundant C-Link. Tables 1 and Table 2 summarize the specific pin assignments for each connector. Three additional JTAG connectors (J3, J4, and J6) are located on the surface of the card. The connector J4 is used for programming of the CPLD chips associated with each of the onboard processors. The connector J3 is used for programming of the flash memory associated with the CPC processor. The connector J6 is used for programming of the flash memory associated with the ICL processor. These ports are not used or accessible during normal operation of the controller.

Table 1. P1 Pin Assignments

Category	Pin	Mnemonic	Pin	Mnemonic
Power				
Serial Bus				
DPM Control				
DPM Address Signals				
DPM Data Signals				
DIP Switch Control				

Category	Pin	Mnemonic	Pin	Mnemonic
DIP Switch Data				
Failover Control				
Ethernet to Backplane Connection				

Table 2. Connector J7 and J9 Pin Assignments

Pin	Name
1	
2	
3	
4	
5	
6	
7	
8	

2.4 SYS Processor Section

2.4.1 I/O Map

The SYS processor, which is a Pentium processor, has no built-in chip select, interrupt controller, I/O ports or timer functions. The SBC6_CHSEL CPLD, in conjunction with the PBUSIF CPLD, provides these functions. This section provides descriptions of decoded address provided by the CPLDs.

Address decoding is accomplished for three blocks of I/O mapped addresses. The first block of addresses range from $F400_H$ to $F4FF_H$ and are used to access internal programmable peripheral registers within the CPLD. The second block of addresses range from 0200_H to $02FF_H$ and are used to access I/O ports included in the CPLD. The third block ranges from 0040_H to $007F_H$ and are used to access the DIP switches and LEDs. Table 3 lists the decoded addresses and their functions.

Table 3. SYS Processor I/O Map

Address Range	I/O **Write** Function	I/O **Read** Function
	Program upper Chip select logic (UCS)	None
	Program middle chip select logic (MCS)	None
	Program lower chip select logic (LCS)	None
	Program page select logic (flash page frame)	None
	Program multiplexed address (flash page latch)	None
	Program memory read/write control	Internal input port (status port)
	Internal output port (control port)	None
	Public memory control enable	None
	Sanity control (watchdog timer port)	
	Maintenance Failover enable	
	LEDs DS3 and DS4	DIPSWITCH 0
	LEDs DS3 and DS4	DIPSWITCH 1
	LEDs DS3 and DS4	DIPSWITCH 2
	LEDs DS3 and DS4	DIPSWITCH 3

The CPLD "PBUSIF" controls a 16 bit data bus. Data from this bus is used to control the multiplexed address logic, the page select logic, the low chip select logic, the middle chip select logic, the upper chip select logic, the memory read/write control logic, and the status of the external LEDs. It is also used to transfer external DIP switch status information, input port information, and interrupt vector information during interrupt acknowledge cycles.

2.4.1.1 I/O Port $F490_H$ – Memory Control and Status Port

The status of data lines 0 through 4 and data lines 6 and 7 are latched during a **write** to I/O address $F490_H$. This latch is used to control various memory read, memory write, and memory select signals. Table 4 defines each of these latches and the data lines that control them.

Table 4. Write Function for $F490_H$

Data Line	Function
0	
1	
2	
3	
4	
6	
7	

By controlling the status of these control latches, different memory devices can be "mapped" to the same address. The status of these latches will determine which type of memory is actually accessed. Mapping both flash and RAM to the same address, enabling RAM write and flash read, and disabling flash write and RAM read, allows all memory writes to modify RAM memory while all memory reads come from flash memory. This allows downloads to

be written to RAM while still running from flash until the downloaded data is verified. Disabling flash allows the SYS processor to initially boot from EPROM, transfer the EPROM contents to code flash, and then execute from code flash.

An IO read to address $F490_H$ will return various input port statuses as defined in Table 5.

Table 5. Status Port

Data Line	Signal
0	
1	
2	
3	
4	
7	

2.4.1.2 I/O Port 200_H – Watchdog Timer Port

The internal output port at address 200_H strobes the hardware watchdog on every IO write to that address. Also the software can cause a failover to the secondary controller by writing a "0" on data bit 0 to this address.

2.4.1.3 I/O Port 210_H – Maintenance Failover Enable/Disable Port

IO address 210_H controls the status of the maintenance failover enable circuit. Writing a "1" on data bit 0 to this address will enable maintenance failover, likewise writing a "0" will disable the maintenance failover feature. Writing a "1" on data bit 0 to IO address $F4A0_H$ will lock the public memory bus access, preventing any other processor from accessing the public memory bus.

2.4.2 Real Time Counter Interrupts

On the -01 assembly, a 50 mHZ clock input to the CPLD (p/n 9093075xx) is divided by 500,000 to create a continuously running timer that generates an interrupt into the SYS processor every 10 msec. On the -81 assembly, the 50 mHz clock is replaced by a 66 mHz and the CPLD (P/N 9093101XX) divides the clock input by 666,000. These timer interrupts are used by the SYS processor for real time control. When the SYS processor receives an interrupt from the CPLD (U36 for both versions of the assembly), it generates an interrupt acknowledge cycle and this CPLD responds to this acknowledge cycle by providing interrupt vector 43_H.

2.5 ICL Processor Section

2.5.1 Interrupt Processing

The ICL 80386EX microprocessor includes an internal interrupt controller that provides input ports for one nonmaskable interrupt (NMI), four levels of external maskable interrupts (INT0/

through INT3/), and internal interrupts from programmable timers and a serial communication controller. The four maskable interrupts, and the NMI interrupt are not used for this application. However, the serial bus interface triggers internal interrupts to coordinate data transfers via the serial transceiver.

2.5.2 ICL Interface

The ICL processor provides two integral serial communication channels (designated channel 0 and channel 1) that can be programmed to support a variety of communication protocols. For the present application, both channels are connected to onboard transceivers that are configured to support RS-485 communication links. The TXD0# and RXD0 ports of the microprocessor are connected to the transceiver for serial channel 0, and the programmable port P1.4 controls the TXEN0 output signal. The TXD1 and RXD1 ports of the microprocessor are connected to the transceiver for serial channel 1, and the programmable port P1.0 controls the TXEN1 output signal. In addition, the card includes three jumper nodes (J5-1, J5-2, and J5-3) that can be used to interlock the TXEN signals with the SANE/ or the PRI/ signals. When the HFC-SBC06 board is used as a redundant controller, a jumper should be installed from node J5–1 to J5–2. This hardware interlock requires the controller chassis to complete its powerup initialization sequence successfully (SANE status TRUE) and become the primary controller before the ICL processor can begin transmitting over its serial link. Removing all jumpers results in a configuration in which the transmit interface remains enabled as long as logic power is present.

2.6 CPC Processor Section

2.6.1 Interrupt Processing

The CPC 80386EX microprocessor includes an internal interrupt controller that provides input ports for one nonmaskable interrupt (NMI), four levels of external maskable interrupts (INT0/ through INT3/), and internal interrupts from programmable timers and a serial communication controller. The CPC processor receives separate interrupts from the two NIC chips. These inputs are routed to interrupt ports INT0/ And INT1/, respectively, to coordinate data transfers between the processor and the Ethernet hardware interface.

2.6.2 Ethernet Interface

The Ethernet interface is implemented by the DP83902 NIC, which is a single VLSI device that includes the Media Access Control (MAC) and Encode/Decode (ENDEC) with AUI interface and 10BASET interface functions in accordance with IEEE 803.2 standards. (The AUI is not used for this application.) The 10BASET transceiver functional block incorporates receiver, transmitter, heartbeat, loopback, jabber detection, and link integrity functions. The integrated ENDEC module allows Manchester encoding/decoding by means of a differential transceiver and phase-lock loop decoder at 10 Mb/sec. This section also includes a collision detector and diagnostic loopback capability.

The CPC processor is connected to hardware for two identical Ethernet channels designated CH0 and CH1. Major components for each channel includes a DPM, serial interface network controller chip (NIC), isolation hardware, and a 20-MHz crystal oscillator (shared by the two channels). A single interrupt signal is routed from each NIC to directly the CPC processor (NIC0_INT to INT2 input port, NIC1_INT to INT1 input port). All other timing and control signals are routed to the CPLD chip, which coordinates all transfers between the NIC and the CPC processor.

2.6.2.1 Interface Configuration

Both Ethernet channels are configured with 10BASET (TPI) physical interfaces; jumper posts W2, W3, W5, and W6 enable the user to configure functional characteristics of the NIC. Following powerup, the hardware circuitry pulls the AUI/TPI port of each NIC low, and logic in the NIC chip enables the TPI interface. TPI interface enables differential RX and TX signal lines with 10BASET interface. Other Ethernet physical interface options are not used and are disabled.

2.6.2.2 CPLD Design for NIC Support

The SBC_386C CPLD supports CPC processor's read and write to the internal registers of the two NIC chips, as well as access the contents of the DPM interface to each NIC chip.

The CPC processor's request to access the internal registers of each NIC is used to synchronize these requests with the acknowledge signals from the NICs. The ready input to the processor is delayed until an acknowledge signal is received from the addressed NIC. This is accomplished through two identical state machines, one for each NIC interface. These state machines detect the CPC processor's request to access that NIC, output the NIC chip select signal, wait for the NIC to respond to the request with an acknowledge, create a properly timed write strobe to the NIC (for write requests), and then release the ready signal to the processor after the proper number of wait states.

The SBC6_386C CPLD uses the CPC processor's NIC-DPM requests, the read strobe, and write strobe to create all of the inputs required by the DPM for each NIC. Table 6 lists the output signals for NIC-DPM.

Table 6. NIC-DPM Control Signals

Description	NIC 0	NIC 1

2.6.2.3 CPC Processor's Control Over NIC

The CPC processor controls overall operation of the Ethernet interface, transfer of data to or from the NIC via DPM, and transfer of data to the main processor via public memory. Following powerup or manual reset, the processor can activate NIC0RST/ (port P1.3) and NIC1RST/ (port P1.2) output signals to disable data reception or transmission at both Ethernet ports. After the controller becomes both sane and primary (SANE/ and PRI/ signals both low), the software can disable the reset signals to permit normal operation of the interface to start.

While normal operation of the NIC is enabled, it activates an interrupt (NIC0_INT or NIC1_INT) to the CPC processor following reception of data from the interface, transmission of data to the interface, or after completion of DMA transfer with DPM. The specific response of the processor to this interrupt depends on current status. The process of reading current status requires the following sequence:

1. Place the NIC in slave mode by pulling the NICX_IO/ signal low.

2. Place the address for a particular register on address lines C_LA01 through C_LA04.

3. Run a bus read cycle with the selected NIC.

Similarly, the processor can use the same sequence for transferring command data to a selected internal register of the NIC. The general sequence of operation necessary for the LAN processor to control operation of the interface is as follows:

1. Access public memory and transfer data to be broadcast to local private memory.

2. Initiate DMA transfer of data from private memory to DPM.

3. Initiate communication with the NIC and identify the starting address of the new data.

4. While the NIC is operating in standalone mode, it controls its access to DPM, encoding of data for transmission to the external link, and status monitoring. Once it completes a commanded operation, it activates its interrupt to the processor.

5. After the NIC completes data reception from the external interface, the CPC processor initiates DMA read from DPM to private memory.

6. After completing the DMA transfer, the processor initiates transfer of the new data through public memory to the main processor.

2.7 SOE Timer

The SOE timer is implemented by a timer with 100 μS resolution contained within the SBC_SHARB CPLD.

3. Hardware Detailed Design Specification for HFC-DPM06

3.1 Module Specification

- Environmental Extremes for Reliable Equipment Operations
  - Temperature: 0° to 55° C (operating)
    0° to 70° C (storage)
  - Humidity: 5% to 95% RH, non-condensing
- Supply Voltage +24 VDC
- Maximum Power Dissipation 5.76 Watts
- Mounting Requirements

All HFC-6000 controller racks contain three slots on the right side of the chassis reserved for controller hardware. The middle slot of the three must contain an HFC-DPM06 assembly.

3.2 Onboard Power Distribution

The card receives redundant 24-vdc power feeds from backplane connector P1. The two power feeds are diode auctioneered and routed to FET switch Q9. The gate input of Q9 is connected to two optical isolators in parallel. Optical isolator U9 is connected to a 5-vdc input signal from controller A, and optical isolator U10 is connected to a 5-vdc input signal from controller B. If a 5-vdc input is available either from controller A or from controller B, one of the two optical isolators will become forward biased. While either optical isolator is forward biased, the gate circuit of the FET passes the input power feed to voltage regulator U5, and the voltage regulator provides +5-vdc operating power to all other hardware on the card. When both controllers are powered down (or missing), the FET becomes cut off, and operating power is removed from all components on this card.

3.3 DIP Switch Status Transfer

Switch configurable data for the HFC-SBC06 board is organized as four data words. The source for one of these data words is physically located on the controller card, and the source for the remaining three is on the HFC-DPM06 card. The data on the HFC-SBC06 SYSTEM CONTROLLER is organized as the high byte of one data word, and each of the inputs from the DPM card is organized as the low byte of a single data word. When the HFC-SBC06 SYSTEM CONTROLLER is configured to operate as a redundant controller, both controller A and controller B read the switch parameters from the DPM card as part of internal configuration following powerup or reset. Each controller employs three control signals (DIPSW0_A, DIPSW1_A, DIPSW2_A; DIPSW0_B, DIPSW1_B, DIPSW2_B) to enable transfer of the configuration data from the DIP switches. Hardware on the DPM card permits both controllers to read configuration data at the same time without causing bus collisions.

Table 7 indicates the content of DIP switch transferred for each combination of DIPSWn signals. As indicated in the table, the last data word contains SANE and PRIMARY status for the other controller. Each controller can read this status byte periodically throughout normal operation. Control signal DIPSW0_A or DIPSW0_B must be active for any of the DIP switch data to be read.

Table 7. Configuration Data Organization

Control Signal States			Data Transfer Enabled
DIPSW0	DIPSW1	DIPSW2	

3.4 Hardware Connections

The HFC-DPM06 has a single backplane connector (P1). Table 8 summarizes the specific pin assignments for this connector. One JTAG connector (J1) is located on the surface of the card. This connector is used for programming the CPLD chip for the DIP switch interface. This port is not used or accessible during normal operation of the controller.

Table 8. P1 Pin Assignments

Category	Pin	Mnemonic	Pin	Mnemonic
Power				
Ground Bus				
DPM Control				
DPM Address Signals				
DPM Data Signals				
DIP Switch Control				

Category	Pin	Mnemonic	Pin	Mnemonic
DIP Switch Data				
Failover Control				

4. Memory Configuration and Access Control

Each processor has their private RAM, flash memory, PROM and has access to the public memory area and the dual ported memory on the HFC-DPM06 board. The CPC processor also has access to the NIC-DPM, the dual ported memory for the NIC.

4.1 Memory Configuration

Figure 1 shows the memory address space architecture. Please note that the addresses are just an example, because the starting addresses, size, and configuration of each memory array are all software configurable.

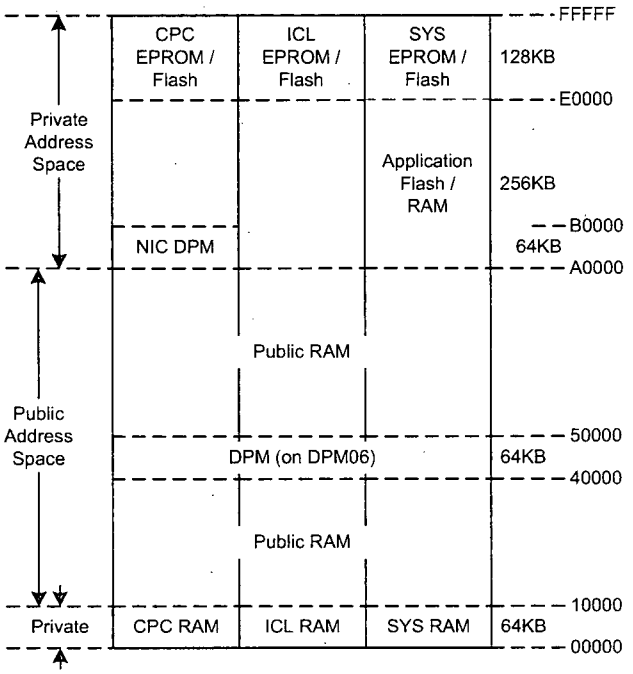

Figure 1. Memory Address Space Architecture

4.1.1 Private Memory Configuration for the SYS Processor

The private memory for the SYS processor is organized into upper, mid, and low memory arrays. The following paragraphs provide descriptions of the private memory configuration of the SYS processor.

- High Memory - The upper bank of private memory can be provided by 256K bytes (128K X 16 bits) of PROM storage or flash memory ending with the address of $FFFFF_H$. This portion of memory provides storage place for the system software. Access to memory in this bank is enabled by the UCS/ chip-select signal. The choice of PROM or flash memory located in the high memory area is determined by the status of jumper J1.

- Mid Memory - An 8-Mbit boot block flash memory chip (512K X 16) serves as the mid memory array. The starting address of mid memory is set by the system software installed in upper memory, and the memory write function is enabled/disabled by onboard switch S2. The flash memory array provides nonvolatile storage for the controller application program, and S2 can be used to prevent online modification of this program.

- Low Memory - The low memory bank provides 8 Mbit of RAM (two 512K X 8 RAM chips). Low memory begins at address 0000:0000 and is configured to permit full word, low byte, or high byte data transfers. The ending address of the low memory array is controlled by the processor. RAM provides temporary storage place for the execution of the system software.

4.1.2 Private Memory Configuration for ICL and CPC Processors

The ICL and CPC processors have the same memory configuration as described in the following paragraphs.

- High Memory - High memory provides up to 256K bytes (128K X 16bits organization) of PROM storage for system software code. The system software code can be transferred to an 8 Mbit (512K X 16 bits) flash memory. Onboard switch SW2 controls the WRITE ENABLE function for all of the flash memory chips. Once the program software has been transferred to flash memory, the processors can be configured to operate from flash rather than PROM.

- Low Memory - Low memory RAM provides an 8 Mbit (two banks of 512K X 8) of volatile memory. Access to RAM is enabled by the CS6#, BLE#, and BHE# signals. RAM provides temporary storage place for the execution of the system software.

4.1.3 Public Memory

The Public Memory on the HFC-SBC06 board provides 8 Mbit (two 512K X 8 bit RAM chips) array of volatile RAM. The public memory array is configured with high and low bytes. As a result, the bus master will have access for high byte, low byte, or full word

read/write transfers. The starting and final address for the array will be software configurable by the SYS processor. This memory area contains all dynamic data that needs to be shared by the three processors on the controller board.

4.1.4 Dual Ported Memory

The DPM array consists of 32 K by 16 bits of volatile RAM configured with high and low bytes in the public memory area. The memory array is physically located on the HFC-DPM06 board in the slot next to the controller (or between two controllers in a redundant configuration).

. The DPM is used for redundant controller configuration to transfer critical information from the primary controller to the secondary controller at regular intervals. An integral memory controller permits simultaneous access by primary and secondary controllers.

4.2 Memory Access Control

The onboard CPLDs provides chip select and control signals for the processors. The CPLDs coordinates bus transfers to local private memory as well as access to the common public memory bus. Figure 2 shows processor bus structure organization.

Each processor has a dedicated data bus connected to its private memory and an interface with the public bus for access to public memory and DPM. All logic components in the common section of the controller are connected to the common public bus. The three processors each use this bus to read current status from public memory and to write status updates to public memory. When the controller is operating in a redundant configuration, the Pentium processor on the primary controller also transfers current status from public memory to the DPM array. Similarly, the Pentium processor on the secondary controller transfers updated status from DPM to its public memory array.

Memory access controls are provided by the CPLDs. CPLDs PBUSIF and SBC6_CHSEL provide chip select and memory access functions for the SYS processor. CPLD SBC6_386C provides these functions to the ICL and CPC processors.

4.2.1 Memory Control Signals for the SYS Processor

Table 9 lists memory control outputs provided by the CPLD for access to different memories for the SYS processor.

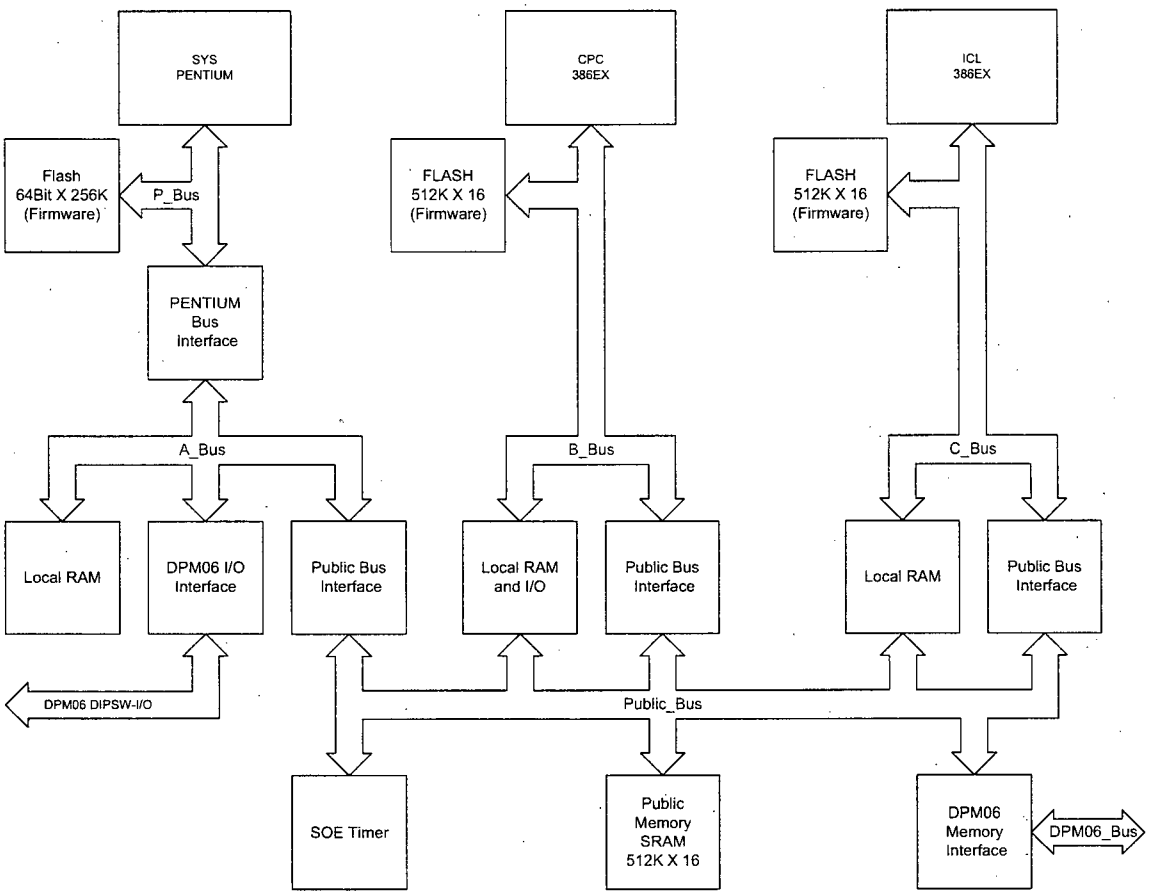

Figure 2. Processor Bus Structure Organization

Table 9. Memory Control Signals for SYS Processor

Signal	Description
EPROM CHIP ENABLE	1) Upper chip select address range if boot strap is installed and EPROM read is enabled (used to boot from EPROM) 2) Middle chip select address range if applications flash is disabled (used when applications is in EPROM).
EPROM READ STROBE	Memory read cycle if EPROM chip enable is active.
CODE FLASH CHIP ENABLE	1)Upper chip select address range if bootstrap is not installed. (Used for normal code execution from code flash) 2) Upper chip select address range if boot strap is installed and code flash write is enabled (used to programming code flash from EPROM when booting from EPROM)
CODE FLASH READ STROBE	All memory read cycles

CODE FLASH WRITE STROBE	Upper chip select address range if code flash write is enabled.
APPLICATIONS FLASH CHIP ENABLE	1) Middle chip select address range if applications flash read is enabled during a memory read cycle (used to read applications program if applications is in flash) 2) Middle chip select address range if applications flash write is enabled during a memory write cycle (used to program applications program into flash)
APPLICATIONS FLASH READ STROBE	1) Memory read cycle if APPLICATIONS CHIP ENABLE is active and applications flash read is enabled.
APPLICATIONS FLASH WRITE STROBE	Memory write cycle if APPLICATIONS CHIP ENABLE is active and applications flash write is enabled.
RAM CHIP ENABLE (LOW BYTE)	1) Low chip select address range is active and low byte enable is active. (used for normal low memory access) 2) Middle chip select address range is active and low byte enable is active if either ram read or ram write is enabled. (used to "overlay" applications flash memory)
RAM CHIP ENABLE (HIGH BYTE)	1) Low chip select address range is active and high byte enable is active. (used for normal low memory access) 2) Middle chip select address range is active and high byte enable is active if either ram read or ram write is enabled. (used to "overlay" applications flash memory)
RAM READ STROBE	1) Memory read cycles to low chip select address range (used for normal memory reads to low memory) 2) Memory read cycles to middle chip select address range if ram read is enabled (used to overlay applications memory)
RAM WRITE STROBE	1) Memory write cycles to low chip select address range (used for normal memory writes to low memory) 2) Memory write cycles to middle chip select address range if ram write is enabled (used to overlay applications memory)
PUBLIC MEMORY SELECT	1) All memory read or write cycles not in any programmed address range.

4.2.2 I/O and Memory Control for the CPC and ICL Processors

The SBC6_386C CPLD supports both ICL and CPC processor's I/O ports and memory control functions.

4.2.2.1 I/O Mapping Through SBC6_386C CPLD

The SBC6_386C CPLD contains an identical control port, the Data Steering Control Register, (DSCR), for each processor. Each processor updates its respective DSCR with an I/O write to address 0080_H. Table 10 lists the functions provided by the DSCR for each processor and the data bus bits that control these functions. These control functions are used to control chip selects, read strobes, and write strobes for the RAM, FLASH, and EPROM memories for the ICL and CPC processors.

Table 10. I/O Mapping for 386EX Processors

DATELINE	FUNCTION

4.2.2.2 Memory Control Signals

The memory control outputs provided for each of the two 80386EX processors are summarized in Table 11.

Table 11. Memory Control Signals for ICL and CPC Processors

Signal	Function

4.2.3 Public Memory and DPM Access

The SBC6_SHARB CPLD provides arbitration for all memory accesses to both onboard public memory and off board dual ported memory. All three processors provide public memory requests into this CPLD. The CPLD determines if the request is for onboard public memory or off board DPM, controls access to the proper memory, and grants access to the requesting processor. If one of the other two processors also request access to the public memory, access is denied to that processor until completion of the memory cycle by the first processor.

The PBUSIF CPLD produces a synchronous ARDY input to the SYS processor, providing support for external ready signals from both public memory accesses and external IO accesses. The SBC6_386C CPLD provides synchronous ready signals to the CPC and ICL processors. Processor ready signals are required by the bus arbitration logic, which holds a requesting processor in wait states until the memory access is granted.

In a redundant controller configuration, CPLDs for both controllers have separate onboard bus arbitration logic that permits any of the onboard processors to access its DPM bus. Once access has been granted, the processor can read or write to a selected location in the DPM array without any possible conflict from the redundant controller.

The DPM arbiter logic on the CPLD has a /DPM BSY status signal to indicate when the memory can be accessed. While the /DPM BSY signal is inactive, any of the processors can access DPM by requesting bus access and running a read or write cycle to an address within the DPM address range. No additional bus arbitration or handshaking is required.

4.2.4 RAM Access Control

The RAM access logic on the CPLD permits firmware to coordinate data transfers between the local RAM and the public memory of the controller. When the microprocessor requires access to its RAM, it places the required address on the address bus (LA01 through LA19) and activates the CS6# chip select. After the address signals have stabilized, the microprocessor activates either the WR# or the RD# to enable either a write or a read transfer. The CPLD chip uses the CS6#, BHE#, and BLE# signals to enable high byte, low byte, or full word transfers from local RAM to the microprocessor.

5. Software Detailed Design Specification

Each processor's system software consists of some standard HFC software components and some hardware specific routines. The design specifications of the standard HFC software components are covered in each component's individual detailed design specification. Refer to Section 5 of the document MS901-000-01 to get a list of component detailed design specifications that are related to the HFC-SBC06 or HFC-DPM06 boards.

This section provides design specification of hardware specific routines or board specific routines, mostly are the initialization processes.

5.1 Initialization Routines

5.1.1 General Initialization Sequence

Each processor on the HFC-SBC06 board goes through a set of initialization sequences before it starts normal operation. These initialization sequences include power up initialization, hardware initialization, processor configuration and UCP Multitasking Operating System initialization.

5.1.1.1 Reset Initialization and Hardware Initialization

Upon power up or reset, the processor automatically begins processing with the instruction pointer set to the last segment address in high memory ($FFFF0_H$), which contains the reset initialization routine. This may be flash memory or the PROM, depending on the processor configuration defined by the jumper settings. The reset initialization defines the entry point to the software. Processor software has an EPROM header at the beginning of the file, and the initialization code must jump over this header for continued program execution.

Functional characteristics of the initialization sequence are similar for all processors. The power-up initialization routine configures chip select registers to define the onboard hardware environment such as memory configuration. If the processor is configured to boot from the PROM, then the software will copy the contents of the PROM to the flash memory and start running from the flash memory.

The module proceeds with hardware-specific initialization for that processor and its peripherals. The module performs initial diagnostic tests, such as RAM Read/Write test and EPROM checksum verification. Any fault detected at this stage of operation is fatal and the program execution will terminate after setting fail indications to the LEDs.

After completion of all preliminary hardware initialization and diagnostics, the initialization software provides different paths for the system processor (SYS processor) and subordinate processors (ICL and CPC processors) to perform their individual processor configuration routines.

5.1.1.2 Processor Configuration

The system processor will initialize public memory and define the controller's configuration. The system processor resets the READY code in the public memory early during the Reset Initialization stage. It reads configuration DIP switches settings and application data in its local memory and sets up configuration data for all subordinate processors in a dedicated area in the public memory, well-known to all processors on board. After the system controller finishes configuration of public memory and becomes SANE, it will set the READY code at the header of the configuration area to indicate completion of the configuration sequence.

The subordinate processors wait till the READY is set in the public memory. After the public memory is ready, the subordinate processors access the public memory and make a local copy of all necessary memory pointers to the public memory and copy other configuration data in their local private memory. Each subordinate processor gets the controller configuration definition in the public memory to build its local copy of all necessary memory pointers. It also goes to its own segment directory in the public memory to get a function code. This function code represents the requested operating mode of the controller by the configuration initialization of the system processor. Two operating modes are supported: Run mode (normal operation), and Self -Test mode.

In the Self-Test mode, the processor performs different kinds of tests based on a request code set up by the DIP switches. The processor stays in the Self-Test mode until the dip switches settings are changed to Run mode. The Run mode is the normal operating mode, and the programs will go to the UCP Multitasking operating system after an OS initialization.

5.1.1.3 UCP Multitasking Operating System Initialization

The UCP Multitasking Operating System is a standard HFC software component. It is mainly a task scheduler that controls the execution of all firmware as well as provides many support functions. During normal operation, the OS component schedules tasks by performing a sequential scan of the defined TCB (task control block) list at regular predefined time intervals, and execute each task in the TCB list if the task's operation status indicates that the task should be executed at that time.

Each processor has unique hardware characteristics and specific functions to fulfill. Various specific initialization routines are required for each processor to set up the hardware and software environment for the operating system to run. These initialization routines are implemented in the processor specific portion of the software. Several initialization routine index tables provide entry to these routines. During the OS initialization, the OS Initialization routine calls these specific initialization routines by going through the initialization routine tables. These initialization routines initializes data structures and adds configured tasks to the TCB list for the OS.

Refer to document MS901-000-01, HFC-SBC06-DPM06 Module Design Specification for the list of configured tasks for each processor on board.

After the initialization for TCB is finished, the OS initialization routine loads the processor's mailbox and marks the processor's status flag to Initialization Done and Online in the dedicated area in the public memory.

The system processor keeps on checking the processor status flag for all configured processors to see if all the processors have finished initialization and online. After all the processors have reported Online and Initialization Done, the system processor will set a SYSTEM_GO flag in the public memory and enters normal operation controlled by the UCP Multitasking operating system. All the subordinate processors, after finding out that the SYSTEM_GO flag is set in the public memory, enters normal operation mode too.

Refer to document DS001-000-01, OS Component Detailed Design Specification for additional information on the OS Component and its initialization interfaces.

In a redundant controller configuration, the failover mechanism determines which controller is primary and which controller is secondary, and the processors on the primary controller start operating in primary mode and the processors on the secondary controller start operating in secondary mode. Refer to document DS001-000-08, Failover Mechanism Component Detailed Design Specification for additional information.

5.1.2 SYS Processor Application Data Initialization

The SYS processor copies application data contained in its flash memory to the public memory or local RAM. The application data includes the following:

- Equations – Application program for control logics
- I/O Configuration Table – ICL I/O Scan Configuration Table for the ICL Processor
- PIP Definition Table – not used for HFC-SBC06
- RQ Table – DDB Filter Table and Broadcast Table for the CPC Processor
- Block Data – Input Data and Intermediate Calculation Data for CQ4 blocks
- Block Value – Output Value and Quality Word for CQ4 blocks

The Equations, Block Data, and Block Value are used for the SYS processor by the Equation Interpreter Component and CQ4 Component. The I/O Configuration Table is used by the ICL processor to perform I/O scan. The RQ Table is used by the CPC processor for DDB broadcasting and processing of DDB data received from the C-Link.

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HFC-6000 Product Line

HFC-6000 I/O Board
Module Detailed Design Specification

DS901-000-02

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Author Angela Han

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1. Introduction

The HFC-6000 I/O boards are sensors and drivers for implementing plant control functions. They provide single-level interfaces to the equipment and devices that run an industrial process. An overview of the architecture and design for standard HFC-6000 I/O boards are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification.

Subsequent sections of this document provide detailed structure and design descriptions of an HFC-6000 I/O board, including common hardware and software characteristics for all I/O boards. The purpose of this document is to present a detailed description of the common methods and strategies used to accomplish the operation and function of a standard HFC-6000 I/O board and the common characteristics of the HFC-6000 I/O boards. The specific detailed design for each individual I/O board is provided by the Module Detailed Design Specification for that board type. The discussion of the operation and function of an HFC-6000 I/O board will be presented using design, implementation, and configuration information.

2. Hardware Detailed Design Specification

HFC-6000 I/O boards share many common hardware characteristics and design strategies. The following is a list of the components that are included in each I/O board and the functions they provide:

- An onboard MicroMonitor IC controls hardware reset at power up or following a microprocessor timeout condition. Switch SW1 permits the operator to initiate a manual reset of the onboard logic.
- A watchdog timer detects a processor timeout condition during normal operation of the system software.
- The microprocessor includes an NMI input port, a variety of internally generated interrupts, and ports for five maskable interrupts (INT0 through INT4).
- Hardwired inputs from the backplane establish the link address.
- Redundant RS-485 serial ports enable communication with external equipment.

Subsequent subsections provide detailed descriptions of these components and how they function.

2.1 Hardware Reset/Initialization Function

An HFC-6000 I/O board provides a DS1232 MicoMonitor chip to control hardware reset functions. The MicroMonitor chip monitors the voltage level of the +5-vdc power rail, the state of the onboard reset switch (SW1), and normal operation of the microprocessor clock,

and it responds to low supply power, manual board resets of SW1, and processor timeout conditions. Any of these conditions will trigger a reset of the 80C188EB microprocessor.

When power is first applied to the board, the low state of the logic power rail causes the MicroMonitor chip to hold a /RESIN signal at a low level. After logic power increases above 4.5-vdc, the MicroMonitor chip keeps the /RESIN signal low for an additional 250 ms to ensure that all transient signals have dissipated before the microprocessor begins operation. During subsequent operation, the chip monitors its inputs for actuation of the RESET switch (SW1) or a significant drop in the voltage level of the onboard logic power rail.

When the microprocessor begins running, CLKOUT pulses are routed from the microprocessor to the MicroMonitor chip. If the microprocessor clock stops running for a period of 1.2 second, the MicroMonitor chip automatically activates the /RESIN signal to reset the microprocessor. If the operator presses the SW1 RESET switch, circuitry on the board causes the MicroMonitor chip to activate the /RESIN signal. When the operator releases the RESET switch, the /RESIN signal remains low for an additional 250 ms before permitting the microprocessor to resume normal operation.

2.2 Watchdog Timer Function

An HFC-6000 I/O board is equipped with a watchdog timer circuit composed of a one-shot and a D-latch. During initial power-up or manual reset, the output from the MicroMonitor chip holds both the one-shot and D-latch in their reset state. When the /RESIN signal assumes a high state, the one-shot can respond to outputs from the microprocessor.

One of the programmable output ports of the microprocessor is routed to the negative trigger input of the one-shot. During normal operation of the onboard software, the microprocessor must produce a low output pulse from this port once every 950 ms to keep the one-shot at a triggered state. While the one-shot remains triggered, the negative output keeps the watchdog LED lit; the positive output enables the transmission function of the redundant serial ports. If the microprocessor stops normally processing its software, the one-shot times out after a period of 950 ms. The resulting transition of the low active output clocks the D-latch, and the low state of the high active output disables transmission over the serial links.

A jumper can be used to disable the Watchdog Timer function. If the jumper is not installed, the D-latch activates a high NMI signal to halt microprocessor operation. As a result, the operator must actuate the RESET switch to initiate hardware reset of the board. If the jumper is installed, the input to the D-latch is pulled low so that the NMI signal will remain disabled following a watchdog timeout. This jumper is used during testing only and should be removed for normal operation.

2.3 INTERRUPT PROCESSING

The 80C188EB microprocessor provides a modular core for processing interrupts and exception conditions. The chip architecture includes an NMI input port, a variety of internally

generated interrupts, and ports for five maskable interrupts (INT0 through INT4). For all I/O boards, the NMI input is controlled by the watchdog timer. The use of maskable interrupts varies, depending on the specific functional requirements of each board type.

2.4 Link Address Data Input Port

The I/O link address port consist of a single 8-bit buffer that maps seven inputs from the backplane to data lines AD0 through AD6. These address signals should be read by the 80C188EB microprocessor during its initialization sequence. The first three data bits correspond to slot select signals SLOT1/, SLOT2/, and SLOT3/, respectively. The remaining four signals correspond to rack select signals RSEL1/ through RSEL4/. The binary status of these 7 address lines are controlled by signals connected to the HFC-6000 I/O board through the backplane, causing the address of the board to be determined by the slot in which it is located.

2.5 Redundant Serial Ports

The 80C188EB microprocessor provides an integral serial communication port that is configured to operate with redundant serial transceivers (designated A and B) and can be programmed to support a variety of communication protocols. For present application, both transceivers are configured to support RS-485 communication links.

The RX (receive) output from both transceivers are connected to the RXD0 input port of the microprocessor, and the TXD0 output from the microprocessor is connected to the TX (transmit) input port of both transceivers. Each transceiver's receive function is controlled by the microprocessor programmable port P1.7. Hardware on the board configures the signal from P1.7 so that the receive function can be enabled for only one transceiver at a time. Programmable output P2.3 controls the transmit function for the transceiver. This output is gated with the high active output from the watchdog timer to prevent spurious transmissions to the link. While the watchdog timer is being triggered, the board can transmit from both transceivers simultaneously.

After power-up and initialization, data reception is always enabled from one of the two transceivers (A or B). When the serial controller in the microprocessor detects activity on the serial link, the RXD0 input to the programmable pin 2.2 of the microprocessor triggers an interrupt. If the newly received message proves to be valid, the software decodes the command code and extracts the data field. After the software has assembled a response message, system software sets the output signal from port P2.3 low to enable transmission. Because one of the two receivers is always enabled, the transmission is automatically echoed back to the RXD0 port of the microprocessor.

2.6 Hardware Connection

All I/O boards are designed with two card-edge connectors (P1 & P2) that mate with corresponding backplane connectors. Signal assignments for P1 are identical for all I/O boards, so that any board can be inserted in any I/O slot of an HFC-6000 chassis. (See table 1.) The P2 connector for each I/O board used the same hardware, but signal assignment are unique

for each board type. Signal assignments for the P2 connector are covered in the detailed design specification for each I/O board type.

Table 1. Connector P1 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic
A1		B1		C1	
A3		B3		C3	
A5		B5		C5	
A6		B6		C6	
A7		B7		C7	
A8		B8		C8	
A9		B12		C9	
A10		B14		C10	
A12		B15		C12	
A14		B16		C14	
A16				C16	

3. Software Detailed Design Specification

Each HFC-6000 I/O board's software will be composed of a set of x86 programs that will handle hardware and software initialization, I/O scan process, communication with the HFC-SBC06 controllers, and self-diagnostic tests functions. The software structure of a standard HFC-6000 I/O board is described in the Module Design Specification. Figure 1 shows the architecture and the major routines in the software for HFC-6000 I/O boards.

The I/O board software consists of the following modules:

- Initialization
  - PCB/Reset Initialization
  - Communication Set Up
- Main Routine
- I/O Scan Routine
- Idle Task – Self Diagnostic Tests
  - RAM Write/Read Test
  - EPROM Test
- Communication Routines
  - Receive Interrupt Service Routine
  - Process Command Routine
  - Create Response Routine
- Timer Interrupt Service Routines

Most of these software modules are common to all I/O boards except those routines that are specific to each board's functions and I/O channels, such as I/O Scan Routine and Process Command Routine. Subsequent subsections provide detailed design descriptions of all the common software modules for the I/O boards.

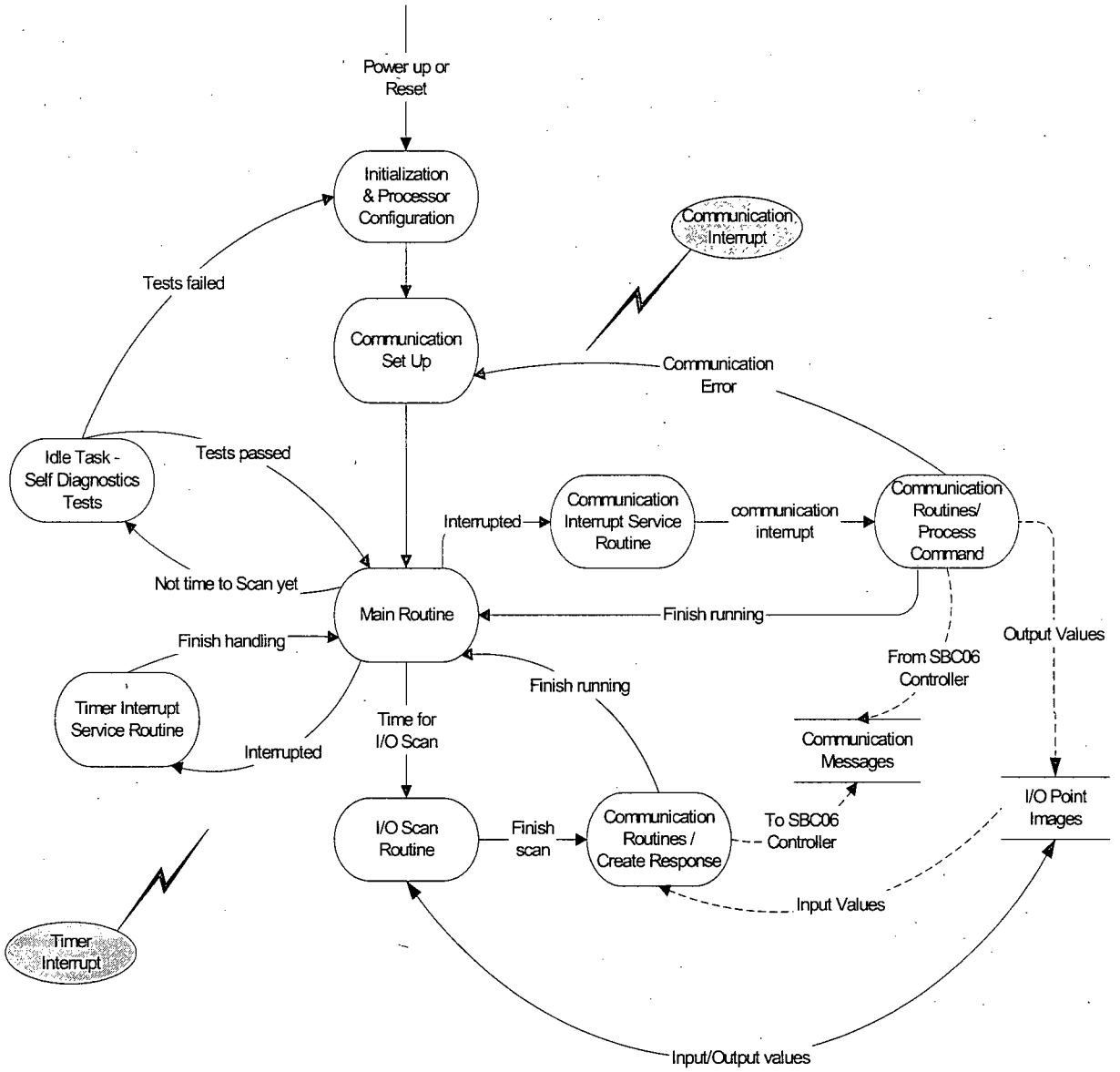


Figure 1. I/O Board Software Architecture

3.1 Initialization Routine

Upon power-up or reset, the microprocessor automatically begins processing with the instruction in the last segment address in high memory, which is the physical location of the first instruction of the initialization routine. The initialization routine configures chip select registers to define the onboard hardware environment, loads configuration parameters into intelligent hardware components, sets control variables to default values, and partitions RAM.

The board executes the power-up tests routine immediately following power up or reset. These tests are composed of a RAM read-write test and an EPROM checksum validation test. Any fault detected at this stage of operation is fatal and terminates program execution. If no errors are detected, the program continues with the initialization by building the interrupt vector table and reading its own link address from an onboard input port.

The Communication Setup subroutine will be called to configure its two serial ports (channel A and channel B) for communication with the HFC-SBC06 controller. The two serial ports are connected to separate ICL links.

At completion of communication setup, the Configure Mode flag is set, and control is transferred to the main routine for normal operation. The configuration mode flag indicates that the board is still under configuration. The Configuration Mode flag is cleared in the Main Routine after completion of the first I/O scan cycle.

3.1.1 Communication Setup

Immediately after completing hardware initialization or after communication timeout, the board enters hunt mode to alternately monitor channel A and channel B for activity. The board will select channel A and listen for activity. If no activity is detected after 150 ms, the board will select channel B and listen for activity. If channel B times out, the software returns to channel A. This monitoring process will be repeated continuously until the board decodes the first valid message with its link address. The channel on which it receives the first message will be configured as the primary link, and the other one will be configured as the backup link.

After detecting activity on one of the two links, the board will enter the active mode. In active mode, the board will begin receiving and processing messages.

The entry point for this module is a procedure call either from the Initialization module or from a Communication ISR module. The exit point returns to the point where this module is called.

3.2 Main Routine

This main routine is configured as a continuous loop that runs two primary functions: an idle task routine and an I/O scan routine. The idle task routine runs a RAM test diagnostic routine as a background task between successive scans. The main routine loops continuously to perform the idle task until an interrupt occurs.

A scan timer ISR is used to control the time interval between successive I/O channel scans. For HFC-6000 systems, this interval is set for 10 milliseconds. When the time interval expires, the interrupt triggers the main routine to stop the idle task and to call the I/O scan process. After I/O scan is finished, the main routine calls a communication function - Create Response module, to transfer the scanned data to response buffer. The board will be set to

idle mode and the main routine resumes the loop to run the idle task until the next interrupt occurs.

The I/O scan process is described in the module detailed design specification for each board type.

The entry point for this module is the Initialization module. As the module is an infinite loop, there is no exit point. The program control will be transferred to an ISR when an interrupt occurs, but it will be transferred back when the ISR is finished.

3.3 Communication Routines

After successful establishment of communication with the controller during the communication setup, the serial interface generates an interrupt to the program each time an Receive activity is detected on the primary link. After the first byte of a new message has been received on the primary serial link, an interrupt will trigger the Receive Interrupt Service Routine.

If the board receives a message while the board is in configure mode, the Receive ISR ignores the command and ends the interrupt because no I/O images are available for transfer to the controller. The Receive ISR also returns without processing if the message address does not match the station address for this board. Otherwise, the board will continue to receive the message and validate the message. After the message is fully received, the specific Process Command Routine for this board is called to process the command. Then the program will set up for the proper response message and start transmitting that message.

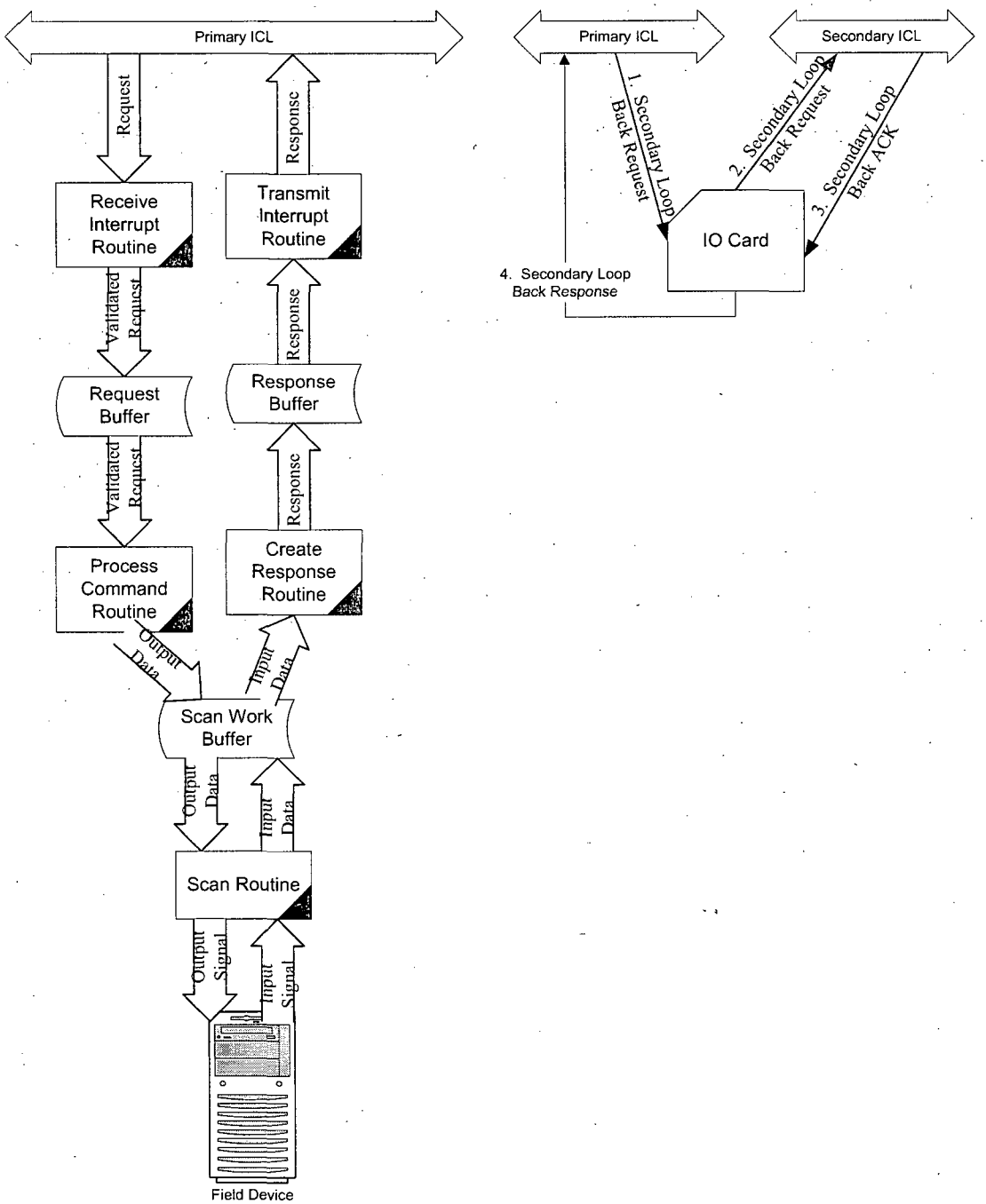
If any error occurs during message reception, the proper error counter will be incremented, and the program will go to the Communication Setup routine to reconfigure the serial links. The communication inactivity timer (timer 0) is used to check inactivity or loopback errors.

The general entry point to the Communication modules is an interrupt from the serial link interface. The exit point is an interrupt return to transfer control back to the main routine.

A loopback test will be performed if the board receives a Secondary Loopback Request message. The program will set the board to loopback mode, and the secondary serial link will be selected as the communication link. Timer 0 will be set up and started. The request message is then transmitted to the secondary controller over the secondary ICL.

If a Secondary Loopback ACK message is received within a fixed timeout interval, the loopback test was successful. The corresponding loopback status and flags will be cleared. If timer 0 times out, the interrupt will branch program control to the Secondary Loopback ACK Timer ISR, and an error code and failure flag will be set. The board will reselect the primary ICL as the normal communication link. The loopback test error will be reported to the primary controller over the primary ICL in a Secondary Loopback Response message.

Figure 2 shows the data flow of data and messages during the normal operation of an HFC-6000 I/O board.



a. Communication Messages b. Secondary Loopback Test

Figure 2. Data Flow

3.3.1 Create Response Routine

The Create Response module creates the response message for each message received from the ICL. The module first determines if a special response message is required. If yes, the special response is created; otherwise, the routine builds the normal response only. The CRC is calculated in working buffer of the I/O Scan process. Two response buffers are used to store response messages. This arrangement ensures that one buffer will be available for constructing a response message.

The module copies either special response data or normal response data from the scan working buffer into the available response buffer, sets the response pointer to this buffer, sets buffer status to "Unavailable" and releases the other response buffer by setting its status to "Available."

The entry point is a routine call from the Main Routine. The exit point returns control to the Main Routine module.

3.4 Timer ISR

Two Timer Interrupts will be configured as part of the common software modules for the I/O boards. These timers will be enabled and disabled in other modules as needed. They have the following Interrupt Service Routines.

3.4.1 Communication Time Out (T/O) ISR

This routine will be triggered by an interrupt generated when a communication inactivity timer times out. It is used to detect communication time out error or secondary loopback test error.

3.4.2 Scan Timer and Watchdog ISR

Timer 2 is used to provide the clock source for the watchdog timer and the scan timer. Each time the required interval has expired, this routine will be triggered to activate a strobe output for the watchdog timer. It will also increment the scan timer, which determines the time interval between successive I/O scans. The I/O scan interval is 10 ms.

4. Software Implementation Descriptions

4.1 Software Programming Language

ASM86 Assembly Language.

4.2 Software Development Tools

Compiler: ASM86

Linker: LINK86

A program, HEX_MOD.exe, developed and being maintained by HFC, takes parameters such as hardware part number, software revision number, etc. and writes them to the binary file generated to be the program file for an I/O board.

4.3 Software Build Files

HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-DO8J Board
Module Detailed Design Specification

Eight Channel Relay
Digital Output Board

NON-PROPRIETARY

DS901-000-03

REV A

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Author Angela Han

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1. Introduction

The HFC-DO8J assembly is an eight-channel relay digital output board. This assembly operates as a standard DO relay board in an HFC-6000 control system. It receives the images of its digital outputs from an HFC-SBC06 system controller at regular intervals, and uses this data to set the on/off status of each output relay.

The overall architectural design of standard HFC-6000 I/O boards are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification.

This document describes the detailed structure and design of the HFC-DO8J board. The design descriptions of the common software modules of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DO8J board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DO8J board is designed to interface eight field outputs to an HFC-6000 control system. It provides eight relay digital output channels. The board receives the image of its digital outputs from the HFC-SBC06 controller board at regular intervals, and uses this data to set the on/off status of each output relay.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification.

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes
  - Temperature: 0° to 55 C° (operating)
    0° to 55 C° (storage)
  - Humidity: 5% to 95%, non-condensing

- Power Requirement
  - External Input Power: +24-vdc, 0.4 A maximum load

- Onboard Clock Rate
  - Microprocessor Clock: 22.1184 MHZ
- Relay contact ratings
  - Up to 30-vdc with 5 A maximum current (resistive load)
  - Up to 250-vac with 5 A maximum current (general use)

3.2 Switches, Jumpers, and LED Indicators

The HFC-DO8J board includes the four card-edge LEDs common to all I/O boards as well as the following components unique to this assembly:

3.2.1 Jumpers

E1-E2 Installed during testing to disable the NMI signal. When the jumper is removed, the D-latch U41-A activates a high NMI signal.

E5-6 Function not currently defined

3.2.2 LED Indicators

DS1-1 Lights when the channel 1 is on
DS1-2 Lights when the channel 2 is on
DS1-3 Lights when the channel 3 is on
DS1-4 Lights when the channel 4 is on

DS2-1 Lights when the channel 5 is on
DS2-2 Lights when the channel 6 is on
DS2-3 Lights when the channel 7 is on
DS2-4 Lights when the channel 8 is on

3.3 ONBOARD POWER DISTRIBUTION

The board receives redundant 24-vdc power feeds from the back plane connector P1. The two power feeds are diode auctioneered, and the resulting 24-vdc output is routed to the following components:

- The onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for logic components on the HFC-DO8J board.
- The combined 24-vdc power line supplies operating power to each of the output relays. A transistor switch in this power line opens whenever the watchdog timer becomes reset.

3.4 Digital Data Output Port

The HFC-DO8J board includes eight relay-controlled DO channels. The ON/OFF image for the eight channels are configured in memory as a single byte of data. During regular scan cycles, the microprocessor copies the DO image from memory to an eight-bit latch, and the resulting output signals from the latch control each DO channel individually.

Each output channel consists of an optocoupler and a mechanical relay with both normally open and normally closed contacts. The optocoupler is configured with a control signal input PTn/ routed from the data output port and the 24-vdc power for the relay. When the digital image for a particular DO channel is ON (PTn/ signal low), the optocoupler becomes forward biased, and 24-vdc power line passes through the optocoupler circuit to the relay coil. While the microprocessor is processing its program code normally, the 24-vdc power line energizes the relay to produce the ON state output. However, if the watchdog timer becomes reset, a transistor switch in the 24-vdc power line opens, removing operating power from all of the relays simultaneously.

3.5 Hardware Connections

The HFC-DO8J board contains board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 back plane. Table 1 lists the pin assignments for connector P1, and Table 2 lists the pin assignments for connector P2. The entries in Table 2 distinguish between normally open (NO) and normally closed (NC) contacts. When the relay is deenergized, continuity exists between its NC contact and its common; when it is energized, continuity exists between its NO contact and its common.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A32		P2-C32	
P2-A31		P2-C31	
P2-A30		P2-C30	
P2-A29		P2-C29	
P2-A28		P2-C28	
P2-A27		P2-C27	
P2-A26		P2-C26	
P2-A25		P2-C25	
P2-A24		P2-C24	
P2-A23		P2-C23	
P2-A22		P2-C22	
P2-A21		P2-C21	
PS-A20		PS-C20	
P2-A19		P2-C19	
P2-A18		P2-C18	
PS-A17		PS-C17	
P2-A16		P2-C16	
P2-A15		P2-C15	
P2-A14		P2-C14	
P2-A13		P2-C13	
P2-A12		P2-C12	
P2-A11		P2-C11	
P2-A10		P2-C10	
P2-A9		P2-C9	

4. Software Detailed Design Specification

The HFC-DO8J board has a total of eight DO channels that provide both normally open and normally closed contacts. The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DO8J board.

4.1 I/O Scan Module

The HFC-DO8J board firmware has an I/O Scan Module like all other I/O boards, but this module has no function, because the board has no input channels.

4.2 Process Command Routine

For normal update messages, this routine reads the one byte output image for eight channels from the command message and transfers that image to output data latch. For UCP diagnostics messages, the routine executes the common processing functions described in HFC-6000 I/O Board Module Detailed Design Specification.

4.3 Data Structure

This section describes the structure of the DO image and provides a list of the programmable ports used in the software.

4.3.1 I/O Scan Data

The DO8J board has eight DO channels. The eight DO images are organized as a single byte in the poll message received from the SBC06 controller as shown below:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1

4.3.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 2. Programmable Ports Used for DO8J Board

Port	Function	Implementation
P1.2		
P1.3		
P1.6		
P1.7		
P2.1		
P2.3		
Port 1 Control Register		

5. Module Implementation Descriptions

5.1 Hardware Schematics

The schematic for the HFC-DO8J board is drawing 400458-01.

5.2 Hardware Components – Bill of Materials

The part number of the HFC-DO8J board is 40045701, and its bill of materials is 400457-01.

5.3 Software Source Code Listing

The HFC-DO8J board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

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HFC-6000 Product Line

HFC-DI16I Board
Module Detailed Design Specification

Sixteen Channel Digital Input Board

NON-PROPRIETARY

DS901-000-04

Rev B

Effective Date	5/7/07
Author	J. Taylor
Reviewer	J. Stevens
Approval	D. Briner

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Revision History

Date	Revision	Author	Changes
11/24/03	0	D. Bynum	Initial
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1. Introduction

The HFC-DI16I assembly is a 16-channel digital input board. This assembly operates as a standard DI board in an HFC-6000 control system. The HFC-DI16I board reads the digital data of its input channels at regular intervals and stores the image in onboard RAM. The HFC-SBC06 controller initiates communication with a configured HFC-DI16I board during its regular scan cycles, and the HFC-DI16I board returns the current digital image for all input channels.

Descriptions and discussions of the architectural and design of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-DI16I board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DI16I board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DI16I board is controlled by an onboard 80C188EB microprocessor and provides an interface for up to 16 digital field inputs for an HFC-6000 control system. The digital inputs received from the field equipment are stored in onboard RAM. The system controller obtains these values from RAM by sending the appropriate poll message to the HFC-DI16I board.

The board can be configured to support sequence of event (SOE) logging for one or more input channels. When the board is configured for SOE logging, poll messages are also used for synchronizing the SOE clock with an external master clock. When SOE logging is enabled the onboard microprocessor reads the value of the SOE timer each time it reads a new DI image. The value of the SOE timer is stored along with the DI image in onboard RAM. The SOE function will be explained in greater detail in section 3.4.

The HFC-DI16I board also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification. The major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Perform reset and initialization of onboard hardware.
- Respond to data transmissions from the HFC-6000 controller.
- Read digital data from each of the 16 DI channels.
- Store the digital image for each channel in onboard memory.
- Perform SOE logging (when function is enabled).

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes

Temperature:	0° to 55° C (operating)
	0° to 70° C (storage)
Relative Humidity:	5% to 95%, non-condensing

- Power Requirements

Interrogation Voltage:	48 volts at 100 mA (maximum)
Logic Level Power:	24-vdc at 0.3 A nominal current

- Onboard Clock Rate

Microprocessor Clock:	22.1184 MHz
SOE Function Clock:	4.0 MHz

3.2 Onboard Power Distribution

The HFC-DI16I board receives two 24-vdc power feeds from the backplane. The two power feeds are diode-auctioneered, and the resulting power line is routed to the input of a 5-vdc voltage regulator (VR1). The output power rail from VR1 supplies logic power for all components on the board.

The board also receives +48-vdc interrogation voltage from the backplane. The input is divided into four separate power rails labeled VINT1 through VINT4. Each power rail is provided with a separate line fuse and provides interrogation power for a group of four input channels. In addition, each of these power rails is also routed to the input of a separate optocoupler. These optocouplers control /VSENS1 through /VSENS4 status signals, which are routed to ports PC0 through PC3 of a programmable port controller. The microprocessor can read the status of the PC port inputs to verify that interrogation voltage is available.

3.3 Interrupt Processing

The 80C188EB microprocessor provides a modular core for processing interrupts and exception conditions. The chip architecture includes a port for an NMI input, ports for five maskable interrupts (INT0 through INT4), and a variety of internally generated interrupts. For this specific board three of the maskable interrupt inputs (INT1 through INT3) are disabled. The maskable interrupt inputs INT0 and INT4 are connected to the logic required to support the SOE function. The watchdog timer controls the NMI input.

3.4 SOE Logic

The SOE logic is composed of two 8-bit comparators, a programmable peripheral controller, and a programmable interval timer. When one or more input points are configured for SOE logging, the microprocessor configures the peripheral controller to retain the most recent image of the 16 DI channels. This image is transferred to 16 output ports of the peripheral controller, and the resulting signals are routed to the two 8-bit comparators. The comparator then compares this image to the current logic state of the 16 input channels. As long as all DI channels remain at the same logic state as that of the most recent image in memory, the

comparator logic holds an INCHG signal at a low state. When the logic state of any DI channel changes from that of its most recent image in memory, the comparator logic sets the INCHG signal high. This signal is routed to the INT4 port of the microprocessor, triggering an interrupt. The service routine corresponding to the INT4 interrupt should perform the following functions.

- It reads the current logic state of all DI channels and transfers that data to memory.
- It reads the current count value of the interval timer.
- It copies the new image of the input channels to the peripheral controller.

The SOE timer consists of a 4.0 MHz crystal oscillator and a programmable interval timer containing three 16-bit counters. The three counters are configured to provide a resolution of 100 μsec over a 24-hour period. When the timer rolls over at the end of the 24-hour period, it activates a CLKOUT signal, which is connected to the INT0 port of the microprocessor. This interrupt can be used to start a clock service routine.

When one or more HFC-DI16I boards are configured for SOE logging, the SOE timer on each board must be synchronized with the system clock to provide reliable results. This function is performed by a master SOE timer in the remote. The controller periodically synchronizes this timer with the remote clock and then downloads this count value to each of the HFC-DI16I boards. The microprocessor on each of the HFC-DI16I boards then downloads that count value to its onboard SOE timer.

3.5 Microprocessor Peripheral Ports

The microprocessor controls the following peripheral ports:

- Digital data input ports
- The 8255 programmable port
- Link address data input port
- Redundant serial port

The link address input port, and the redundant serial port are both common to all I/O board types, and are described in document DS901-000-02. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the three I/O ports.

3.5.1 Digital Input Ports

The 16 DI channels are configured in groups of four with each group sharing a common interrogation voltage supply line. Each DI channel consists of a low-pass RC filter and an optocoupler. The cathode of each optocoupler is connected to one position of two 8-position DIP switches. Each switch position enables hardware configuration of a single DI channel for either common or isolated mode operation. The output section of each optocoupler consists of an optically controlled NPN transistor. Because the emitter of each transistor is connected to ground and the collector controls the DI logic signal, the optocouplers invert all signals received from the field devices.

When a DI channel is configured for common mode operation, interrogation voltage is supplied from the board to the field device, and the return line from the field device is connected to the input channel. Resettable fuses in each of the four interrogation voltage supply lines provide over current protection in groups of four channels each. When the switch or relay contacts for a particular field device closes, the field circuitry returns the interrogation voltage back to the cathode of the associated optocoupler. This condition changes the state of the DI channel to logic TRUE (low active) and causes the board edge LED for that channel to light. When the channel is configured for isolated mode operation, functional characteristics of the input channel hardware are identical, except the external hardware must supply the interrogation voltage.

The logic state of all 16 DI signals are routed to four input buffers. The chip select signal for two of the input buffers is controlled by programmable output P1.2, and the chip select for the other two is controlled by programmable output P1.3. The microprocessor can read the logic state of DI1 through DI8 by running a read cycle with P1.2 pulled low. Similarly, the microprocessor can read the logic state of DI9 through DI16 by running a read cycle with P1.3 pulled low.

3.5.2 The 8255 Programmable Peripheral Interface

The board contains an 8255 programmable peripheral interface that functions as part of the SOE logic. This device includes three programmable 8-bit I/O ports (PA, PB, and PC), an 8-bit interface with the onboard data bus, two address ports, and internal control logic. Programmable port P1.0 of the microprocessor controls the chip select signal (/CS8255) for this device, and the A00 and A01 signals serve as address inputs. While the /CS8255 signal is low, the microprocessor can use the two address signals to access the internal control logic or the data register for one of the three ports. Once a particular register has been accessed, the microprocessor can write configuration data to the control register or read/write data to the selected data register. When the HFC-DI16I board is configured for SOE operation, the microprocessor configures the three programmable ports are as follows:

- PA0 through PA7 function as output channels and contain the most recent image of DI9 through DI16, respectively.
- PB0 through PB7 function as output channels and contain the most recent image of DI1 through DI8, respectively.
- PC0 through PC3 function as input ports and receive the /VSENS1 through /VSENS4 signals. These inputs enable the microprocessor to verify the status of each interrogation voltage rail.
- PC4 and PC5 function as output ports. When both outputs are set high, the clocking function of the SOE timer is enabled; when set low, the SOE timer is disabled.
- PC6 and PC7 are not used.

If the board is not being used for SOE logging, the microprocessor can configure ports PC0 through PC3 to read the status of the interrogation power lines without using the other functions of the chip.

3.5.3 SOE Timer

The board contains a programmable 8254 interval timer that is used for SOE logging. This timer contains three 16-bit programmable timers, an 8-bit interface with the onboard data bus, and control logic. Programmable port P1.1 of the microprocessor controls the chip select signal (/CS8254) for the programmable interval timer, and the A00 and A01 signals serve as address inputs. During read/write cycles to the programmable interval timer, the microprocessor can perform any of the following operations as required:

- Write configuration parameters to a selected counter.
- Enable/disable operation of the interval timer.
- Preset a selected counter to an initial count value.
- Read the current value of a selected counter.

3.6 Controls, Jumpers, and LED Indicators

The firmware determines the overall operating characteristics of the hardware on the HFC-DI16I board. The HFC-DI16I board includes the set of four LEDs common to all I/O board types (DS901-000-02). The board also includes several jumpers, switches, fuses, and LEDs specific to this board. These devices and the functions that they control are as follows:

3.6.1 LEDs

DS1-1	On status indicates that DI channel 1 is at logic 1
DS1-2	On status indicates that DI channel 2 is at logic 1
DS1-3	On status indicates that DI channel 3 is at logic 1
DS1-4	On status indicates that DI channel 4 is at logic 1
DS2-1	On status indicates that DI channel 5 is at logic 1
DS2-2	On status indicates that DI channel 6 is at logic 1
DS2-3	On status indicates that DI channel 7 is at logic 1
DS2-4	On status indicates that DI channel 8 is at logic 1
DS3-1	On status indicates that DI channel 9 is at logic 1
DS3-2	On status indicates that DI channel 10 is at logic 1
DS3-3	On status indicates that DI channel 11 is at logic 1
DS3-4	On status indicates that DI channel 12 is at logic 1
DS4-1	On status indicates that DI channel 13 is at logic 1
DS4-2	On status indicates that DI channel 14 is at logic 1
DS4-3	On status indicates that DI channel 15 is at logic 1
DS4-4	On status indicates that DI channel 16 is at logic 1

3.6.2 Jumpers

E1-E6 Not used.

E9-E12 Not used.

E14-E49 Installed during calibration to disable the NMI signal. When this jumper is removed, the D-latch U41-A activates a high NMI signal.

E13-E15 Function not currently defined.

3.6.3 Switches

SW1 Used to reset the 80C188EB microprocessor.

S1 Used to configure digital inputs 1-8 as isolated or common

S2 Used to configure digital inputs 9-16 as isolated or common

3.6.4 Resettable Fuses

F1–F4 Provide overload protection for the +48-vdc or +24-vdc interrogation voltage supplied for the 16 DI channels.

3.7 Hardware Connections

The HFC-DI16I board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-DI16I and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each DI channel can be configured for either isolated or common operation on an individual basis. Table 2 lists connection requirements for both isolated and common configurations for each channel.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1		P2-C1	
P2-A2		P2-C2	
P2-A3		P2-C3	
P2-A4		P2-C4	
P2-A5		P2-C5	
P2-A6		P2-C6	
P2-A7		P2-C7	
P2-A8		P2-C8	
P2-A9		P2-C9	
P2-A10		P2-C10	
P2-A11		P2-C11	
P2-A12		P2-C12	
P2-A13		P2-C13	
P2-A14		P2-C14	
P2-A15		P2-C15	
P2-A16		P2-C16	
P2-A17		P2-C17	
P2-A18		P2-C18	
P2-A19		P2-C19	
P2-A20		P2-C20	
P2-A21		P2-C21	
P2-A22		P2-C22	
P2-A23		P2-C23	
P2-A24		P2-C24	

Table 2. Input Connection Summary

Channel No.	Type	Interrogation Voltage	Positive Terminal	Negative Terminal	DIP Switch
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					

1. In Common mode the field connection routes excitation voltage from the DI16 module to the field contacts and back to the positive terminal. The return path is made on the board through S2.
2. In Isolated mode excitation power is routed from the field contacts to the positive terminal, and the negative terminal is connected to the external voltage return.

4. Software Detailed Design Specification

The design descriptions of the common software modules are provided in MS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DI16I board.

4.1 Board Information

The HFC-DI16I board provides a total of sixteen channels that operate with either 48-vdc or 24-vdc interrogation voltage supplied from the board. In addition, the board provides the hardware and software necessary to support SOE logging. For the SOE logging function, the HFC-DI16I software includes a specific Interrupt Service Routine for external event interrupts.

4.2 Software Modules

4.2.1 I/O Scan Module

This I/O Scan Module performs the I/O scan for sixteen standard DI channels. It takes samples to read the status of four interrogation voltages and 16 digital inputs during each scan. The loss of interrogation voltages means that the DI images are not valid and the module will not update its DI images with new readings. If any interrogation voltage is false, the Interrogation Voltage Off error bit in the diagnostic byte will be set to indicate a hardware fault. This information will be reported to the controller in the response to a diagnostic request message.

Normally the DI images will be transferred to the Scan Working Buffer only when at least one of three interrogation voltages is present. However, to avoid missing information on the controller side, an interrogation voltage failure counter is used in the I/O scan process. This counter increments each time a scan cycle misses all interrogation voltage lines. When the accumulated count exceeds a predefined limit, the DI images will be updated to the Scan Working Buffer to be reported to the controller even though no interrogation voltage is present. This counter will be reset once any interrogation voltage line is present.

The first time the software performs I/O Scan, it sets up the interrupt vectors for Interrupt Service Routines.

4.2.2 SOE Interrupt Service Routine

When this routine is activated by an external interrupts, it reads digital inputs from the data port and writes the input data to the 8255 port. Then it reads the current time from the 8255 port. The I/O images with a time tag will be stored in an event queue buffer.

4.2.3 Process Command routine

Each time the board receives a poll from the controller, this routine checks the command code. If an SOE Synchronization command has been received, the software transfers the time code from the message data field to the onboard SOE clock. It also performs a date rollover every 24 hours and adds a date rollover entry in the event queue buffer.

If the command is an SOE event buffer request, the process command routine verifies that the code is the correct SOE task code (01_H). If the task code is not correct, the routine sends a NACK response and returns. If the task code is valid, the process command routine reads the SOE request code. Currently, only one type of buffer request is supported: Send Block of Event Records. The routine finds the starting record of events requested and builds an SOE response with the records in the event buffer queue.

For normal update messages, this routine has no function. For UCP diagnostics messages, common processing is used as described in document DS002-000-02.

4.3 Data Structure

4.3.1 Scan Data

The DI16I board has sixteen DI channels. For normal scan cycles, the sixteen DI images will be put into two bytes as follows:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1
1	PT16	PT15	PT14	PT13	PT12	PT11	PT10	PT9

For a report of SOE status, the data is formatted with the 16-bit data image followed by the time stamp.

4.3.2 SOE Event queue buffer

An event queue buffer is used for logging SOE events. Each queue entry has 6 bytes. A normal entry contains data as follows:

Byte	Description
0-1	I/O images
2-3	Second
4-5	Hour

A date roll over event entry contains data as follows:

Byte	Description
0-1	Second
2-3	Hour
4-5	Date Roll Over Entry Code (8000_H)

4.3.3 SOE Special Request Messages

4.3.3.1 SOE Synchronization Command

This command is used for synchronization of the SOE timer with the controller master timer. The message code is $9E_H$. The data field contains the current time sent by the controller as shown below. No response is returned for this command.

Byte	Description
0-1	Second
2-3	Hour

4.3.3.2 SOE Event Buffer Request Command

This command is used for requesting the records in the SOE Event Buffer maintained by the software. The message code is 90_H, and it is one of the special UCP message types. Refer to the ICL protocol document DS002-000-02 for more information on UCP messages.

The data field contains the UCP request codes as follows:

Byte	Value	Description
0-1		
2		
3		
4		

The response message data field will include a predefined number of records of contiguous block data starting from the buffer record number contained in the command message. The requested event records can be wrapped around the event buffer, i.e. if the records requested reaches the end of the buffer, the records at the beginning of the buffer will be added to the response.

4.3.4 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3-1 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 3. Programmable Ports Used for the HFC-DI16I Board

Port	Functions	Implementation
P1.0		
P1.1		
P1.2		
P1.3		
P1.4		
P1.7		
P2.1		
P2.3		
Port 1 Control Register		

5. Module Implementation Description

5.1 Hardware Schematics

The schematic for the HFC-DI16I board is drawing 400451-01.

5.2 Hardware Components – Bill of Materials

The part number of the HFC-DI16I board is 40045201, and its bill of materials is 400452-01p.

5.3 Software Source Code Listing

The HFC-DI16I board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

6. Design Safety

Refer to MS901-000-02 for a discussion of design safety considerations relating to the HFC-6000 I/O modules.

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HFC-6000 Product Line

HFC-DC33 Board
Module Detailed Design Specification

Digital Input/Output Controller Board
Specific for Motor Operated Valve (MOV)

DS901-000-05

Rev C

Effective Date	10/23/07
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3/3/07	B	J Taylor	SCR 1766.
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1. Introduction

The HFC-DC33 is a multi-channel Input/Output (I/O) buffer printed circuit board (PCB). It is used for control, interrogation, and monitoring of field devices in an HFC-6000 control system. The board receives digital messages from its controller, the HFC-SBC06, and sends the image of its 11 digital input (DI) channels.

Descriptions and discussions of the architectural and design descriptions of a standard HFC-6000 I/O board, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-DC33 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DC33 board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DC33 is a special purpose I/O buffer board designed for power plant applications. This buffer is specifically designed to meet the unique control requirements of a dual-coil Motor Operated Valve (MOV) starter. Typical applications include controlling dual coil motor starters while monitoring coil continuity, overloads and the position of the valve.

This board provides a 16-bit 80C188EB microprocessor, 11 DI channels, two 120-vac DO channels, and onboard status sensors. Major functions performed by the microprocessor during normal operation are as follows:

- Responds to data transmissions from the HFC-6000 controller.
- Controls the on/off state of the two DO channels.
- Reads the digital status of the onboard DI channels.
- Reads coil continuity and the presence of ac excitation signals for both DO channels.
- Stores the DI image and onboard status in local memory.
- Transmits the digital image of its 11 DI channels back to the HFC-6000 controller.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification.

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes
  - Temperature: 0° to 60 C° (operating)
    0° to 70 C° (storage)
  - Humidity: 5% to 95%, non-condensing

- Power Requirement — Note: AC signals are represented by their rms value.
  - Output Voltage: 60 to 140-vac, 47 to 63 Hz
  - Output Current: 110 amps: inrush, 5 amps continuous
  - External Source Power: 24-vdc at 0.3 A nominal current
  - Interrogation Voltage: 48-vdc

- Onboard Clock Rate
  - Microprocessor Clock: 22.1184 MHZ

- Mounting Requirements
  - The HFC-DC33 mounts vertically in an HFC-6000 card chassis.

3.2 Controls, Jumpers, and LED Indicators

3.2.1 Jumpers

E1-E2 Installed during calibration to disable the NMI signal. When the jumper is removed, the D-latch U41-A activates a high NMI signal.

3.2.2 Switches

SW1 Enables manual reset of the 80C188EB microprocessor.

S5 Permits manual configuration of DI channels 1-11 as isolated or common in any combination

S3 Enables/Disables the Seal-In circuitry for channel 0 output

S4 Enables/Disables the Seal-In circuitry for channel 1 output

3.2.3 Reset-able Fuses

RF1–RF3 Provide overload protection for the +48-vdc interrogation voltage supplied for the 11 DI channels.

3.2.4 LED Indicators

DS1-1 SYSA/B lights when receive function is enabled for port A; it is out when receive function is enabled for port B.
DS1-2 TX flashes during serial data transmission over ICL.
DS1-3 RX flashes during reception of serial data from ICL.
DS1-4 DMT lights while watchdog timer is being triggered.

DS2-1 CH0 RDY lights when 120- vac power is available, and CH0 is de-energized and connected to an operational coil.
DS2-2 CH1_RDY lights when 120- vac power is available, and CH1 is de-energized and connected to an operation coil.
DS2-3 PWR PRESENT0 lights when 120-vac power is available for CH0.

DS2-4	PWR PRESENT1 lights when 120-vac power is available for CH1.
DS3-1	SEAL IN CH0 lights when seal-in circuitry for CH0 is enabled.
DS3-2	SEAL IN CH1 lights when seal-in circuitry for CH1 is enabled.
DS3-3	CH0 OUT lights when output relay U27 is enabled.
DS3-4	CH1 OUT lights when output relay U13 is enabled.
DS4-1	Lights when the channel 1 is on
DS4-2	Lights when the channel 2 is on
DS4-3	Lights when the channel 3 is on
DS4-4	Lights when the channel 4 is on
DS5-1	Lights when input channel 5 is on.
DS5-2	Lights when input channel 6 is on.
DS5-3	Lights when input channel 7 is on.
DS5-4	Lights when input channel 8 is on.
DS6-1	Lights when input channel 9 is on.
DS6-2	Lights when input channel 10 is on.
DS6-3	Lights when input channel 11 is on.
DS6-4	No Connection will not illuminate.

3.3 Onboard Power Distribution

The board receives redundant 24-vdc power feeds from the backplane connector P1. The two power feeds are diode auctioneered, and an onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for components on the HFC-DC33 board.

Two +48-vdc interrogation power sources are fed through connector P1 and divided into three branches with each branch supplying power to four channels. A separate reset-able fuse provides overload protection for each branch, and three optocouplers permit the microprocessor to monitor status of the three power lines.

The board receives a nominal 120-vac (20 to 140-vac) power for the two solenoid output channels. When supply power is available, a bridge rectifier produces a dc status signal that forward biases an optocoupler, enabling the microprocessor to verify power status. The 120-vac power line is connected to a separate solid state relay for CH0 and CH1. The microprocessor can control these relays independently to enable power output to one or both channels.

120-VAC can be provided to the seal-in circuitry for CH0/CH1. When power is available, a bridge rectifier produces a dc signal that is supplied to a DC-DC converter. If S3 is in the enabled position a 5V signal is available to sustain the output of CH0 in case of controller failure or in loss of 24V power to the board. If S4 is in the enabled position a 5V signal is available to sustain the output of CH1 in case of controller failure or in the loss of 24V power to the board.

3.4 Microprocessor Peripheral Ports

The microprocessor controls the following peripheral ports:

- Two digital data input ports
- CH0/CH1 control output port
- Link address data input port
- Redundant serial ports

Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the I/O ports.

The board provides one output latch to control the status of the two 120-vac output channels (CH0 and CH1) and two input buffers to read 15 bits of input data. During an I/O scan, the microprocessor writes the ON/OFF image for CH0 and CH1 to the output latch. The resulting output signals control separate solid state relays. When the microprocessor enables one or both outputs, the corresponding relay becomes enabled and passes the 120-vac power to its output. Similarly, the microprocessor reads input status by running separate read cycles to the two input buffers. The low order byte contains the digital image of PT01/ through PT08/. The high order byte contains the digital image of PT09/ through PT11/, CH0_RDY/, CH1_RDY/, CH0_PWR/, CH1_PWR/, SICH0/, and SICH1/. In addition to the 17 bits of input data, the microprocessor also can read the status of the excitation voltage lines VSEN/, VSEN2/, and VSEN3/. These signals are routed directly to three pins of programmable I/O port P2 of the microprocessor.

The Link address data input port and Redundant serial ports are covered in document DS901-000-02 I/O Board Module Detailed Design Specification.

3.5 Input Channel Operation

The HFC-DC33 board contains 20 input channels composed of 11 general purpose DI channels, two coil continuity inputs, two power monitor inputs, two seal-in status inputs, and a separate status monitor for the three excitation voltage lines. Each of the DI channels is composed of a low-pass input filter and optocoupler. The input filter is designed to reject any input signal having a pulse width less than 10 ms in duration, and the optocoupler isolates the internal logic circuitry from the field wiring. When one of these channels receives an active input signal, the optocoupler becomes forward biased and produces a low active output. While any of these outputs is active, the corresponding LED lights. The input circuit for the three VSEN/ input signals is identical, except they do not have an LED indication.

The input circuit for the 120-vac power monitor consists of a bridge rectifier, a low pass filter, and an optocoupler. When the 120-vac power source is present, the rectifier produces a dc signal at the input of the low pass filter network, and the optocoupler activates the CH0_PWR/ status signal.

The circuit for the two coil continuity monitor inputs is similar to that of the power monitor circuit except for input biasing. When the 120-vac output is enabled, the circuit is always

enabled, so the status input is not meaningful. When one or both output channels are disabled, a small voltage bleeds through the biasing network to the input of the rectifier. If the external coil is present, this small voltage dissipates through the coil and the output from the optocoupler remains disabled. This output is inverted to produce a low active status input (CH0_RDY/ or CH1_RDY/) to the microprocessor. If the external coil is not present or open, the small voltage at the input of the rectifier is sufficient to forward bias the optocoupler, resulting in a high (false) indication for the CH_RDY/ input.

3.6 Hardware Connections

The HFC-DC33 board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Pin assignments for the P1 connector are identical for all I/O boards and can be found in document DS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each DI channel can be configured for either isolated or common mode operation on an individual basis. When operating in common mode, excitation voltage is supplied from this board to the field device being monitored. When operating in isolated mode, external equipment must supply the power to enable or disable the DI indication. Table 2 lists the DIP switch settings and signal assignments required to configure each channel for either mode of operation.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1		P2-C1	
P2-A2		P2-B2	
P2-C2		P2-A3	
P2-C3		P2-A4	
P2-C4		P2-A5	
P2-B5		P2-C5	
P2-A6		P2-C6	
P2-A7		P2-C7	
P2-A8		P2-B8	
P2-C8		P2-A9	
P2-C9		P2-A10	
P2-C10		P2-A11	
P2-B11		P2-C11	
P2-A12		P2-C12	
P2-A13		P2-C13	
P2-A14		P2-B14	
P2-C14		P2-A15	
P2-C15		P2-A16	
P2-C16		P2-A17	
P2-B17		P2-C17	
P2-A18		P2-C18	
P2-A19		P2-B19	
P2-C19		P2-A20	
P2-B20		P2-C20	
P2-A21		P2-B21	
P2-C21		P2-A22	
P2-B22		P2-C22	
P2-A23		P2-B23	
P2-C23		P2-A24	
P2-B24		P2-C24	
P2-A25		P2-B25	
P2-C25		P2-A26	

P2-B26		P2-C26	
P2-A27		P2-B27	
P2-C27		P2-A28	
P2-B28		P2-C28	
P2-A29		P2-B29	
P2-C29		P2-A30	
P2-B30		P2-C30	
P2-A31		P2-B31	
P2-C31		P2-A32	
P2-B32		P2-C32	

Table 2. Input Connection Summary

Channel No.	Type	Positive	Negative	Dipswitch
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				

4. Software Detailed Design Specification

The HFC-DC33 board monitors a total of 20 DI channels. The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DC33 board.

4.1 I/O Scan Module

This I/O Scan Module performs the I/O scan for 11 standard DI channels, two coil continuity status inputs, two power monitor status input, and two seal in status inputs. It takes samples to read the status of three interrogation voltages and two bytes of input data during each scan. The loss of any interrogation voltage means that four or more DI images may not be valid, so the module will not update DI images with new readings if no interrogation voltage is present. If any interrogation voltage is false, the Interrogation Voltage Off error bit in the diagnostic byte will be set to indicate a hardware fault. This information will be reported to the controller in the response to a diagnostic request message. However, in isolated mode, the interrogation voltages are not used and will not affect DI accuracy.

Normally the DI images will be transferred to the Scan Working Buffer only when at least one of three interrogation voltages is present. However, to avoid missing information on the

controller side, an interrogation voltage failure counter is used in the I/O scan process. This counter is incremented during each scan cycle where all interrogation voltages are missing. When the accumulated count exceeds a predefined limit, the DI images in the Scan Working Buffer will be updated and reported to the controller, even if no interrogation voltage is present. This counter will remain reset as long as any interrogation voltage line is present.

If a DO channel is set ON, the corresponding coil continuity status input is not meaningful. So the coil continuity status will be reported as "TRUE" to prevent spurious error indications. Only when the corresponding DO channel is not ON will the actual coil continuity status be reported back to the HFC-SBC06 controller.

4.2 Process Command routine

For normal update messages, this routine reads the one byte output image for two output channels from the command message and transfers that image to output data latch. UCP diagnostics messages are processed as described in HFC-6000 I/O Board Module Detailed Design Specification DS002-000-02.

4.3 Data Structure

This section describes the structure of the I/O data images and provides a list of the programmable ports controlled by the software.

4.3.1 I/O Scan Data

The HFC-DC33 board has two DO channels and 11 DI channels. The data field of poll messages received from the HFC-SBC06 controller has the following structure:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	PT2	PT1

The data field of the response message to the HFC-SBC06 Controller has the following structure:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1
2	Power Source 1	Power Source 0	Coil 1 Continuity	Coil 0 Continuity	Seal In CH 0	PT11	PT10	PT9

4.3.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 3. Programmable Ports Used for HFC-DC33 Board

Port	Description	Implementation
P1.0		
P1.1		
P1.2		
P1.3		
P1.5		
P1.6		
P1.7		
P2.1		
P2.3		
P2.4		
P2.5		
P2.6		
Port 1 Control Register		

5. Module Implementation Description

5.1 Hardware Schematics

The schematic for the HFC-DC33 board is drawing 400463-01.

5.2 Hardware Components – Bill of Materials

The part number of the HFC-DC33 board is 40046201, and its bill of materials is 400462-01 and 400462-81.

5.3 Software Source Code Listing

The HFC-*DC33* board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

6. Design Safety

Refer to MS901-000-02 for a discussion of design safety considerations for HFC-6000 I/O modules.

HF Controls

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HFC-6000 Product Line

HFC-DC34 Board
Module Detailed Design Specification

Digital Input/Output Controller Board
Specific for Electronically Operated Breakers (EOB)

DS901-000-06

Rev C

Effective Date	10/23/07
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Date	Revision	Author	Changes
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1. Introduction

The HFC-DC34 is a multi-channel Input/Output (I/O) buffer printed circuit board (PCB). It is used for control, interrogation, and monitoring of field devices in an HFC-6000 control system. Typical applications include monitoring Electrically Operated Breakers (EOB) for overloads. The board receives digital messages from its controller, the HFC-SBC06, and sends the image of its 11 digital input (DI) channels.

Descriptions and discussions of the architectural and design descriptions of a standard HFC-6000 I/O board, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-DC34 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-DC34 board will be presented using design, implementation, and configuration information.

2. Functional Description

The HFC-DC34 is a special purpose I/O buffer board designed for power plant applications. This board is designed to provide the specific combination of digital I/O channels needed to control motor starter or switchgear field equipment.

This board provides a 16-bit 80C188EB microprocessor, 11 DI channels, two 125-vdc DO channels, and onboard status sensors. Major functions performed by the microprocessor during normal operation are as follows:

- Responds to data transmissions from the HFC-6000 controller.
- Controls the on/off state of the two output channels.
- Reads the digital status of the onboard DI channels.
- Reads coil continuity and the presence of dc excitation signals.
- Stores the DI image and onboard status in local memory.
- Transmits the digital image of its 11 DI channels back to the HFC-6000 controller.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification.

3. Hardware Detailed Design Specification

3.1 Module Specification

- Environmental Extremes
  - Temperature: 0° to 60 C° (operating)
    0° to 70 C° (storage)
  - Humidity: 5% to 95%, non-condensing

- Power Requirement
  - Output Voltage: 100 to 150-vdc
  - Output Current: 25 amps: inrush
    10 amps, 250ms repeated once per 5 minutes
    2 amps continuous
  - External Source Power: 24-vdc at 0.3 A nominal current
  - Interrogation Voltage: 48-vdc
- Onboard Clock Rate 22.1184 MHZ
- Mounting Requirements
  - The HFC-DC34 mounts vertically in an HFC-6000 card chassis.

3.2 Controls, Jumpers, and LED Indicators

3.2.1 Jumpers

E1-E2 Installed during calibration to disable the NMI signal. When the jumper is removed, the D-latch U41-A activates a high NMI signal.

3.2.2 Switches

SW1 Enables manual reset of the 80C188EB microprocessor.

S1 Permits manual configuration of DI channels 1-11 as isolated or common in any combination

S3 Enables/Disables the Seal In mode for CH0

S4 Enables/Disables the Seal In mode for CH1

3.2.3 Reset-able Fuses

RF1–RF3 Provide overload protection for the +48-vdc interrogation voltage supplied for the 12 DI channels.

3.2.4 LED Indicators

DS1-1 SYSA/B lights when receive function is enabled for port A; it is out when receive function is enabled for port B.
DS1-2 TX flashes during serial data transmission over ICL.
DS1-3 RX flashes during reception of serial data from ICL.
DS1-4 DMT lights while watchdog timer is being triggered.

DS2-1 CH0 RDY lights when 125- vdc power is available, coil test mode is enabled, and the external coil on CH0 is operational.

DS2-2	CH1 RDY lights when 125- vdc power is available, coil test mode is enabled, and the external coil on CH1 is operational.
DS2-3	PWR PRESENT0 lights when 125-vdc power is available for CH0.
DS2-4	PWR PRESENT1 ligths when 125-vdc power is available for CH1.
DS3-1	SEAL IN CH0 lights when seal in circuitry for CH0 is enabled.
DS3-2	SEAL IN CH1 lights when seal in circuitry for CH1 is enabled.
DS3-3	CH1 OUT lights when the CH1 output is enabled.
DS3-4	CH0 OUT lights when the CH0 output is enabled.
DS4-1	Lights when the channel 1 is on
DS4-2	Lights when the channel 2 is on
DS4-3	Lights when the channel 3 is on
DS4-4	Lights when the channel 4 is on
DS5-1	Lights when input channel 5 is on.
DS5-2	Lights when input channel 6 is on.
DS5-3	Lights when input channel 7 is on.
DS5-4	Lights when input channel 8 is on.
DS6-1	Lights when input channel 9 is on.
DS6-2	Lights when input channel 10 is on.
DS6-3	Lights when input channel 11 is on.
DS6-4	No connection, will not illuminate.

3.3 Onboard Power Distribution

The board receives redundant 24-vdc power feeds from the backplane connector P1. The two power feeds are diode auctioneered, and an onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for components on the HFC-DC34 board.

Two +48-vdc interrogation power sources are fed through connector P1 and divided into three branches with each branch supplying power to four channels. A separate reset-able fuse provides overload protection for each branch, and three optocouplers permit the microprocessor to monitor status of the three power lines.

The board receives a nominal 125-vdc (100 to 150-vdc) power for the two solenoid output channels. When supply power is available, an input status signal forward biases a corresponding optocoupler, enabling the microprocessor to verify power status. The 125-vdc power line is connected to a separate FET switch for CH0 and CH1. The microprocessor can control these FETs independently to enable power output on one or both channels.

125-VDC can be provided to the seal-in circuitry for CH0/CH1. When power is available, a linear regulator converts 125-VDC to 48-VDC, then a DC-DC converter converts 48VDC to 5VDC. If S3 is in the enabled position and the 125-VDC is supplied to SEAL IN CH0, then a 5V signal is available to sustain the output of CH0 in case of controller failure or in loss of 24V power to the board. If S4 is in the enabled position and the 125-VDC is supplied to SEAL IN CH1, then a 5V signal is available to sustain the output of CH1 in case of controller failure or in loss of 24V power to the board.

3.4 Microprocessor Peripheral Ports

The microprocessor controls the following peripheral ports:

- Two digital data input ports
- CH0/CH1 control output port
- Link address data input port
- Redundant serial ports

Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the I/O ports.

The board provides one output latch to control the status of the two 125-vdc digital output channels (CH0_OUT/ and CH1_OUT/) and two coil monitoring circuits (CH0_TST/ and CH1_TST/). When one of the DO channels is set on, the corresponding CHx_OUT/ signal from the latch forward biases a solid-state switch, passing 125-vdc power from input source to the output port for that channel. When a DO channel is set off, the microprocessor can activate the CHx_TST/ output signal to energize the coil monitoring circuit. In order for the circuit to produce meaningful results, the onboard software prevents the DO channel and the coil monitoring circuit from being enabled at the same time.

The microprocessor reads input status by running separate read cycles to the two input buffers. The low order byte contains the digital image of PT01/ through PT08/. The high order byte contains the digital image of PT09/ through PT11/, CH0_RDY/, CH1_RDY/, CH0_PWR/, CH1_PWR/, SICH0/, AND SICH1/. In addition to the 17 bits of input data, the microprocessor also can read the status of the excitation voltage lines VSEN/, VSEN2/, and VSEN3/. These signals are routed directly to three pins of programmable I/O port P2 of the microprocessor.

The Link address data input port and Redundant serial ports are covered in document DS901-000-02 I/O Board Module Detailed Design Specification.

3.5 Input Channel Operation

The HFC-DC34 board contains 20 input channels composed of 11 general purpose DI channels, two coil continuity inputs, two power monitor inputs, two seal-in status inputs, and a separate status monitor for the three excitation voltage lines. Each of the DI channels is composed of a low-pass input filter and an optocoupler. The input filter is designed to reject any input signal having a pulse width less than 10 ms in duration, and the optocoupler isolates the internal logic circuitry from the field wiring. When one of these channels receives an active input signal, the optocoupler becomes forward biased and produces a low active output. While any of these outputs is active, the corresponding LED lights. The input circuit for the three VSEN/ input signals is identical, except they do not have an LED indication.

Each of the two input circuits for the 125-vdc power monitor consists of a low pass filter, and an optocoupler. When the 125-vdc power source is present for one or both input channels, the dc signal at the input of the low pass filter network activates a corresponding optocoupler

to produce a low active output (CH0_PWR/ and/or CH1_PWR/). If either the CH0_PWR/ or the CH1_PWR/ signal is active, the PWR PRESENT0 LED or PWR PRESENT1 LED lights respectively.

The coil monitor circuit consists of a voltage divider connected to the 125-vdc power source, a low pass filter, and two optocouplers. When the microprocessor activates the CHx_TST/ signal, one optocoupler passes the 125-vdc power source to the input of the voltage divider. This circuit then applies a significantly reduced voltage across the ports of the DO channel. If an external coil is present, a small current passes through the voltage divider network to forward bias the monitoring optocoupler, which then produces a low active CHx_RDY/ status output. If the external circuit is open, no current flows through the circuit, and the monitoring optocoupler remains cut off. If either the CH0_RDY/ or the CH1_RDY/ signal is active, the CH0/1 RDY LED lights.

3.6 Hardware Connections

The HFC-DC34 board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Pin assignments for the P1 connector are identical for all I/O boards and can be found in document DS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each DI channel can be configured for either isolated or common mode operation on an individual basis. When operating in common mode, excitation voltage is supplied from this board to the field device being monitored. When operating in isolated mode, external equipment must supply the power to enable or disable the DI input circuit. Table 2 lists the DIP switch settings and signal assignments required to configure each channel for either mode of operation.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1		P2-C1	
P2-A2		P2-B2	
P2-C2		P2-A3	
P2-C3		P2-A4	
P2-C4		P2-A5	
P2-B5		P2-C5	
P2-A6		P2-C6	
P2-A7		P2-C7	
P2-A8		P2-B8	
P2-C8		P2-A9	
P2-C9		P2-A10	
P2-C10		P2-A11	
P2-B11		P2-C11	
P2-A12		P2-C12	
P2-A13		P2-C13	
P2-A14		P2-B14	

Table 1(Continued). Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-C14		P2-A15	
P2-C15		P2-A16	
P2-C16		P2-A17	
P2-B17		P2-C17	
P2-A18		P2-C18	
P2-A23		P2-B23	
P2-C23		P2-A24	
P2-B24		P2-C24	
P2-A25		P2-B25	
P2-C25		P2-A26	
P2-B26		P2-C26	
P2-A27		P2-B27	
P2-C27		P2-A28	
P2-B28		P2-C28	
P2-A29		P2-B29	
P2-C29		P2-A30	
P2-B30		P2-C30	
P2-A31		P2-B31	
P2-C31		P2-A32	
P2-B32		P2-C32	

Table 2. Input Connection Summary

Channel No.	Type	Positive	Negative	Dipswitch
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				

4. Software Detailed Design Specification

The HFC-DC34 board monitors a total of 20 DI channels. The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-DC34 board.

4.1 I/O Scan Module

This I/O Scan Module performs the I/O scan for 11 standard DI channels, two coil continuity status inputs, 2 power monitor status inputs, and two seal in status inputs. It reads the status of three interrogation voltages and the two bytes of input data during each scan. The loss of any interrogation voltages means that four or more of the DI images may not be valid, so the module will not update DI images with new readings if no interrogation voltage is present. If any interrogation voltage input is false, the Interrogation Voltage Off error bit in the diagnostic byte will be set to indicate a hardware fault. This information will be reported to the controller in the response to a diagnostic request message. However, in isolated mode, the interrogation voltages are not used and will not affect DI accuracy.

Normally, the DI images are transferred to the Scan Working Buffer when at least one of three interrogation voltages is present. However, to avoid missing information on the controller side, an interrogation voltage failure counter is used in the I/O scan process. This

counter is incremented during each scan cycle where all interrogation voltages are missing. When the accumulated count exceeds a predefined limit, the DI images in the Scan Working Buffer will be updated and reported to the controller even if no interrogation voltage is present. This counter will remain reset as long as any interrogation voltage line is present.

If a DO channel is set ON, the corresponding coil continuity status input is not meaningful. So the coil continuity status will be reported as "TRUE" to prevent spurious error indications. Only when the corresponding DO channel is not ON will the actual coil continuity status be reported back to the HFC-SBC06 controller.

4.2 Process Command routine

For normal update messages, this routine reads the one byte output image for two output channels from command message and transfers that image to output data latch. UCP diagnostics messages are processed as described in HFC-6000 I/O Board Module Detailed Design Specification DS002-000-92.

4.3 Data Structure

This section describes the structure of the I/O data images and provides a list of the programmable ports controlled by the software.

4.3.1 I/O Scan Data

The HFC-DC34 board has 2 DO channels and 11 DI channels. The data field of poll messages received from the HFC-SBC06 controller has the following structure:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	CH1_OUT/	CH0_OUT/

The data byte transferred to the output data latch has the following structure:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	-	CH1_OUT/	CH0_OUT/

The data field of the response message to the HFC-SBC06 Controller has the following structure:

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1
2	Power Source 1	Power Source 0	Coil 1 Continuity	Coil 0 Continuity	Seal In CH0	PT11	PT10	PT9

4.3.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 3 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 3. Programmable Ports Used for HFC-DC34 Board

Port	Description	Implementation
P1.0		
P1.1		
P1.2		
P1.3		
P1.5		
P1.6		
P1.7		
P2.1		
P2.3		
P2.4		
P2.5		
P2.6		
Port 1 Control Register		

5. Module Implementation Description

5.1 Hardware Schematics

The schematic for the HFC-DC34 board is drawing 400468-01.

5.2 Hardware Components – Bill of Materials

The part number of the HFC-DC34 board is 40046701, and its bill of materials are 400467-01 and 400467-81.

5.3 Software Source Code Listing

The HFC-DC34 board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

6. Design Safety

Refer to MS901-000-02 for a discussion of design safety considerations for the HFC-6000 I/O Modules.

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HFC-6000 Product Line

HFC-AI16 Board
Detailed Design Specification

Sixteen Channel Analog Input Board

DS901-000-07

Rev C

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Author J. Taylor

Reviewer B. Cain

Approval D. Briner

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1. Introduction

The HFC-AI16 assembly is a 16-channel analog input board. This assembly operates as a standard AI board in an HFC-6000 control system. It receives analog input signals from field equipment at the plant and performs A/D conversion for each channel at regular intervals. The HFC-SBC06 controller initiates communication with a configured HFC-AI16 board during its regular scan cycles, and the HFC-AI16 board returns the current digital image for all input channels.

Descriptions and discussions of the architectural and design descriptions of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-AI16 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-AI16 board will be presented using design, implementation, and configuration information.

1.1 References

700901-06	HFC-6000 I/O Card Requirements Specification
MS901-000-02	HFC-6000 Product Line, I/O Module Design Specification
DS901-000-02	HFC-6000 Product Line, I/O Module Detailed Design Specification
RS901-000-40	HFC-6000 Product Line PCB Layout Requirements
40043301	HFC-AI16 Schematic
WI-ENG-106	Development of Hardware Design Specification

1.2 Special Terms and Abbreviations

I/O	Input/Output
LSB	Least Significant Bit
RAM	Random Access Memory
AI16F	0-20mA 16 Channel Analog Input
AI16E	0-10V 16 Channel Analog Input
AI16R	0-5V 16 Channel Analog Input
A/D	Analog to Digital Converter

2.0 Specifications

- Environmental Extremes

Temperature:	0° to 55° C (operating)
	0° to 70° C (storage)
Relative Humidity:	5% to 95%, non-condensing

- Power Requirements
  External Power Supply: +24 vdc, 0.3 A maximum load.
  Excitation voltage: +24 vdc with resetable fuse for each pair of channels and 0.5 A fuse for the combined load

- Onboard Clock Rate
  Microprocessor Clock: 22.1184 MHz

- Input Signal Requirements
  Signal:

AI16F	249Ω input resistor accepts 0 to 20mA.
AI16E	1 MΩ input resistor accepts 0 to 10V.
AI16R	1 MΩ input resistor accepts 0-5V.
Accuracy:	Designed to read input signals accurately to .1% of full scale.

3.0 Controls and Indicators

The firmware determines the overall operating characteristics of the hardware on the HFC-AI16 board. The HFC-AI16 board includes the set of four LEDs common to all I/O board types (DS901-000-02). In addition, the board also includes six jumpers, two potentiometers, three switches, and nine fuses. The function of these components is as follows:

Jumpers

W36 Installed to supply 24-vdc excitation power for common AI channels.

W37 Installed to make the analog return and digital return electrical common.

E1-E2 Installed during calibration to disable both the NMI signal. When this jumper is removed, the D-latch U41-A activates a high NMI signal.

E5-E6 Not currently defined.

Potentiometers

R97 Enables the manual adjustment of the ADC offset voltage.

R98 Enables the manual adjustment of the ADC gain.

Switches

SW1 Enables user to reset the 80C188EB microprocessor.

S1 8-position DIP switch enables the user to configure channels 1 through 8 for either common or isolated mode operation (SW ON = COMMON) in any combination.

S2 8-position DIP switch enables the user configure channels 8 through 16 for either common or isolated mode operation (SW ON = COMMON) in any combination.

Fuses

F1, F2, F4-F9 Provide separate overload protection on the 24-vdc excitation voltage line for each pair of input channels

F3 Provides common overload protection for the excitation power source supplied to all 16 input channels.

4.0 Functional Description

The HFC-AI16 AI board is controlled by an onboard 80C188EB microprocessor and provides an interface for up to 16 analog field inputs for an HFC-6000 control system. The analog inputs are converted into digital images and stored in onboard RAM. The system controller accesses these values from RAM by sending the appropriate message to the HFC-AI16 board.

4.1 Overview

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification. The major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Performs reset and initialization of onboard hardware.
- Responds to data transmissions from the HFC-6000 controller.
- Samples the analog data from each of the 16 AI channels.
- Performs the Analog-to-Digital (A/D) conversion of field inputs.
- Stores the digital image for each channel in onboard memory.

4.2 Onboard Power Distribution

The board receives redundant 24-vdc power feeds from the backplane connector J1. The two power feeds are diode auctioneered and routed to the following components:

- An onboard voltage regulator converts the 24-vdc source power to +5-vdc power required for logic components on the HFC-AI16 board.

- An onboard voltage regulator (PS1) converts the 24-vdc source power to ± 15-vdc non-isolated power. This supplies operating power for the non-isolated analog circuitry.

- An onboard voltage regulator (PS2) converts the 24-vdc source power to ± 15-vdc for the isolated analog circuitry.

When jumper W36 is installed, a 24-vdc power line is divided into 8 branches. Each branch includes a separate resetable line fuse and supplies excitation power for two AI channels.

4.3 Reset/Initialization

The Micro Monitor chip monitors the voltage level of the +5-vdc power rail, the state of the onboard reset switch (SW1), and normal operation of the microprocessor clock. When power is first applied to the board, the low state of the logic power rail causes the Micro Monitor chip to hold a /RESIN signal at a low level. After logic power increases above 4.5-vdc, the Micro Monitor chip keeps the /RESIN signal low for an additional 350 ms to ensure that all transient signals have dissipated before the microprocessor begins operation. During subsequent operation, the chip monitors its inputs for actuation of the RESET switch (SW1) or a significant drop in the voltage level of the onboard logic power rail.

When the microprocessor begins running, CLKOUT pulses are routed from the microprocessor to the Micro Monitor chip. If the microprocessor clock stops running for a period of 50 ms, the Micro Monitor chip automatically activates the /RESIN signal to reset the microprocessor. If the operator presses the SW1 RESET switch, circuitry on the board causes the Micro Monitor chip to activate the /RESIN signal. When the operator releases the RESET switch, the /RESIN signal remains low for an additional 350 ms before permitting the microprocessor to resume normal operation.

Watchdog Timer Functions

The HFC-AI16 board is equipped with a watchdog timer circuit composed of a one-shot (U40-A) and a D-latch (U41-A). During initial power-up or manual reset, the output from the Micro Monitor chip holds both the one-shot and D-latch in their reset state. When the /RESIN signal assumes a high state, the one-shot can respond to outputs from the microprocessor.

Programmable output from port P2.1 of the microprocessor is routed to the negative trigger input of the one-shot. During normal operation of the onboard software, the microprocessor must produce a low output pulse from this port once every 950 ms to keep the one-shot at a triggered state. While the one-shot remains triggered, the negative output keeps LED DS5-1 lit, and the positive output enables the transmission function of the redundant serial ports. If the microprocessor stops normally processing its software, the one-shot times out after a period of 950 ms. The resulting transition of the low active output clocks the D-latch, and the low state of the high active output disables transmission over the serial links.

If jumper E1-E2 is not installed, the U41-A D-latch activates a high NMI signal and low TIMEOUTA/ and TIMEOUTB/ signals. The two TIMEOUT/ signals can be used to notify external equipment that this board is not operating, and the NMI signal halts microprocessor operation. As a result, the operator must actuate the RESET switch to initiate hardware reset of the board. If the E1-E2 jumper is installed, the transition of the watchdog timer disables transmission over the serial links, but the NMI signal remains disabled.

4.4 Memory Structure

Memory on the HFC-AI16 board is organized into two banks of private memory for the microprocessor. Private memory for the 80C188EB microprocessor consists of one bank of EPROM and one bank of RAM. The private memory banks are connected directly to the address and data lines of the microprocessor.

80C188EB Microprocessor Upper Memory

The upper bank of local memory for the 80C188EB microprocessor provides up to 64K by 8 bits of EPROM storage ending with the address of $FFFFF_H$. Access to memory in this bank is enabled by the UCS/ chip-select and RD/ signals from the microprocessor. When the low active RESIN/ signal returns to a high level following power-up, the internal address pointer of the microprocessor begins operation by accessing the data stored at address $FFFF0_H$ in upper memory. As a result, the first instruction of the initialization code must be located at this address.

80C188EB Microprocessor Low Memory

The low memory bank provides up to 32K by 8 bits of static RAM for general data storage. Low memory begins at address 00000_H, and access to the memory in this range is enabled by the LCS/ signal. This portion of memory contains the data structures and temporary storage buffers defined by the functional code in upper memory.

4.5 Interrupt Processing

The 80C188EB microprocessor provides a modular core for processing interrupts and exception conditions. The chip architecture includes a port for an NMI input, ports for five maskable interrupts (INT0 through INT4), and a variety of internally generated interrupts. For this specific board four of the maskable interrupt inputs (INT0 through INT3) are disabled. The maskable interrupt input INT4 is configured to detect completion of the A/D cycle. By using INT4 in this way, the microprocessor can efficiently read the converted analog data at the appropriate time. The watchdog timer controls the NMI input.

4.6 Microprocessor Peripheral Ports

The microprocessor controls the following peripheral ports:

- Analog Input (AI) control output port
- A/D data input port
- Link address data input port
- Redundant serial port

The link address input port, and the redundant serial port are common to all I/O board types, and are described in document DS901-000-02. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the three I/O ports

4.6.1 Analog Input (AI) control output port

The interface between the microprocessor and the analog section of the board consists of a 16-bit A/D converter, an eight-bit latch, and two BCD-to-decimal decoders. Bits 4 through 7 (formatted as AD0 through AD3) of the data transferred to the latch contain a four-bit code for the AI channel to be read, and bit 1 (AD6) controls the R/C output to the A/D converter. The four-bit channel selection code is routed from the output ports of the latch to the input of both BCD-to-decimal decoders via the eight-bit buffer. The buffer has two output enable ports controlled by separate signals from the microprocessor. OE1 is controlled by the output from P1.6, and OE2 is controlled by the output from P1.5. When the microprocessor activates the output from P1.6, the channel select code controls selection of PT00 through

PT07; when the output from P1.5 is activated, the channel select code controls selection of PT08 through PT17. PT16 and PT17 control selection of zero and span voltage inputs for a calibration cycle. The active output signal then forward biases the optocoupler for the selected channel, and it passes the analog input from the field device to an input amplifier.

The input amplifier produces a gain of 1.909 (nominal) into the isolation amplifier. The input circuit for the AI16F is designed for a signal ranging from 0 to 20 mA across a 249Ω load. The input circuit for the AI16E is designed for 0 to 10V signal range across a 1MΩ resistor. Thus, the normal input to the isolation amplifier should range from 0 to 9.507 vdc. If the input signal from a field device is greater than 20.2 mA (9.601-vdc input to the isolation amplifier), an over-range condition exits. The software should detect any over-range condition. The microprocessor accomplishes over-range detection by monitoring the magnitude of the count value produced by the A/D converter. If the output of the A/D converter is greater than 31460 counts (which corresponds to 9.601-vdc), an over-range error condition exists.

Input channels PT16 and PT17 provide precision voltage levels to enable the microprocessor to evaluate the calibration of the analog circuitry. When PT16 is selected, the onboard circuitry supplies a fixed signal of 0.91-vdc to the input amplifier. When PT17 is selected, the circuitry supplies a fixed signal of 10-vdc to the input amplifier. The microprocessor reads the count values for these two inputs and compares them with expected values from memory. If the drift is less than a fixed tolerance value in memory, the software can calculate a correction factor for each of the field inputs. If the drift exceeds the tolerance value, the software can trigger a calibration error alarm.

4.6.2 A/D data input port

The microprocessor uses the following sequence to select an input channel, initiate A/D conversion, and read the resulting 16-bit digital image from the ADC.

1. The microprocessor writes the channel selected code and a high R/C signal to the output latch.

2. After completion of the write cycle, the microprocessor sets either programmable port P1.5 or P1.6 low to enable generation of the required port selection output signal.

3. The selected channel supplies its signal to the input of the analog circuitry. The high state of the R/C and CS/ signals enable internal sample-and-hold circuits in the ADC to acquire the input signal.

4. After a delay to allow signal stabilization, the microprocessor sets the R/C and CS/ signals low to start the conversion process. The sample-and-hold in the ADC retains the signal acquired during the previous interval.

5. The ADC sets the STS (BUSY/) signal low at the start of the conversion cycle. When the conversion cycle is complete, the STS signal returns to a high level.

6. The low-to-high transition of the STS signal triggers the INT4 input to the microprocessor.

7. The microprocessor sets the R/C signal high and then runs two read cycles to the A/D data input port with the CS/ signal low. The microprocessor sets the AD0 signal low to access the most significant byte of data and sets it high to access the least significant byte of data.

8. The microprocessor can repeat steps 4 through 7 to read the digital image from the sample-and-hold circuit without repeating the acquisition cycle.

4.7 I/O Ports

The HFC-AI16 board contains 16 input channels for analog input signals from external field equipment. Each channel includes a low-pass filter to block electrical noise and an optocoupler to isolate the onboard circuitry from the field circuitry. Each channel includes a connection to an onboard DIP switch that permits configuration for either common or isolated operation on a channel-by-channel basis. When a channel is configured for common mode operation, 24-vdc power is supplied from the board to the field transducer that produces the input signal. When a channel is configured for isolated operation, that channel is electrically isolated from all other components on the board, and the field transducer must provide the power source to drive the input signal.

5.0 Hardware Connections

The HFC-AI16 board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-AI16 and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 1. In addition, each AI channel can be configured for either isolated or common operation on an individual basis. Table 2 lists connection requirements for both isolated and common configurations for each channel.

6. Software Detailed Design Specification

The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AI16F board.

6.1 Board Information

The HFC-AI16F board has a total of 16 identical AI channels. Each channel will provides positive and negative terminal connections for a signal in the range of 0-20 mA. The board contains a single A/D converter that will be configured to produce a 16-bit digital image of the analog input for each channel.

Table 1. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1		P2-C1	
P2-A2		P2-C2	
P2-A3		P2-C3	
P2-A4		P2-C4	
P2-A5		P2-C5	
P2-A6		P2-C6	
P2-A7		P2-C7	
P2-A8		P2-C8	
P2-A9		P2-C9	
P2-A10		P2-C10	
P2-A11		P2-C11	
P2-A12		P2-C12	
P2-A13		P2-C13	
P2-A14		P2-C14	
P2-A15		P2-C15	
P2-A16		P2-C16	
P2-A17		P2-C17	
P2-A18		P2-C18	
P2-A19		P2-C19	
P2-A20		P2-C20	
P2-A21		P2-C21	
P2-A22		P2-C22	
P2-A23		P2-C23	
P2-A24		P2-C24	

Table 2. Input Connection Summary

Channel No.	Type	Positive	Negative	Dipswitch
1				
2				
3				
4				
5				
6				

Channel No.	Type	Positive	Negative	Dipswitch
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				

6.2 Analog Input Scan Algorithm

Every scan cycle, the scan module performs an AI calibration test, and then calculates the AI offset and gain. If any errors occur during the calibration test, the scan module sets an error bit in the diagnostics byte, marks the normal response as a bad response, and returns.

If no errors occur during the calibration test, the module reads the raw value of each analog input channel from the AD converter, and adjusts the raw value with AI offset and AI gain using the algorithm described in Section 4.2.3 "AI Algorithm."

After finishing with all channels, the module stores the adjusted raw value in a filter buffer, and calculates a moving average of all records of raw value in the buffer. The filter buffer's size is predefined. Every scan cycle, a new reading of raw value is added to the buffer, and the earliest reading in the buffer is pushed out.

There are two calibration parameters for each channel that are originally obtained from the EPROM. The software uses these parameters to adjust the filtered AI raw value of each channel for better accuracy. Then the adjusted input images will be saved in the scan work buffer. Refer to Section 4.3 "Single Channel Adjustment Algorithm" for the adjustment algorithm using calibration parameters.

6.2.1 Read Channel Raw Value

During each AI signal reading, control signals are used to initialize the A/D converter (ADC), and to sample the input signal from the selected channel. The output signal STS is linked with the interrupt signal INT4 to the microprocessor. This signal indicates the status of the ADC cycle. It goes low at the beginning of a conversion and returns high when the conversion cycle is complete. The interrupt request register REQST is used to check the ADC conversion complete bit (INT4).

The module takes predefined number of AI samples per channel and averages the raw count value. The main sequence to scan the image for one AI channel is as follows:

1. Initialize the AI image accumulator to 0
2. Initialize loop counter to sample numbers
3. Select the port for this AI channel
4. Then loop to initialize an A/D conversion, wait till the REQST indicates the completion of A/D conversion, then read data from the A/D converter, and add the sample data to the AI image accumulator
5. After the loop is finished, deselect the port
6. Average the AI image accumulator by sample numbers

6.2.2 Calibration Test Routine

This routine gets the raw values from the low calibration point and the high calibration point. If the low or high calibration point raw value is out of range, the routine will return with error. If there are no errors, the routine calculates AI offset and gain by using low and high calibration point raw values.

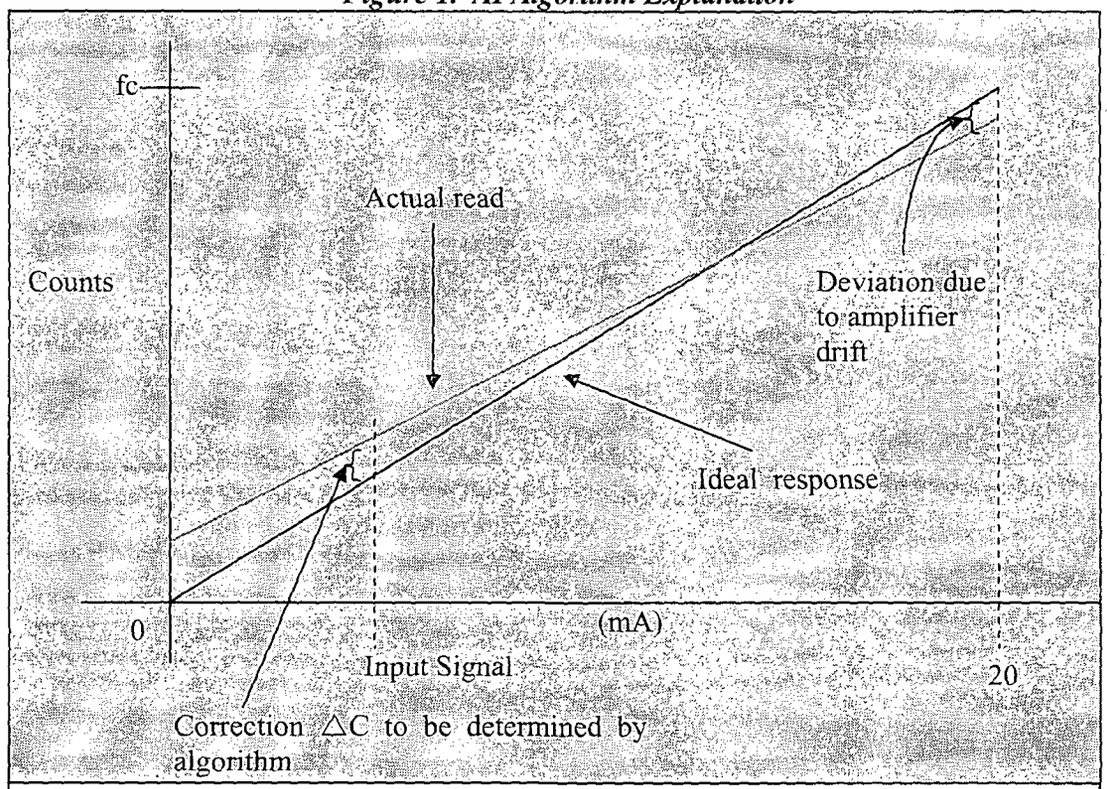
For 15-bit AD converter, the raw value of the low calibration point should be within 0B18H ± A0H counts, and the raw value of the high calibration point should be within 79E0H ± A0H counts. When the raw values are within the acceptable ranges, the calculation of AI offset and AI gain is as follows:

6.2.3 AI Algorithm

For 15-bit AD converter, the calculation of AI image is as follows:

Please see Figure 1 below for an explanation of what this AI Algorithm is accomplishing.

Figure 1. AI Algorithm Explanation



Using basic analytic geometry, the problem consists merely of calculating the value of △C based on the difference in the slope of the ideal response and the actual response. The algorithm accomplishes just this, but all calculations are based on integer count values. The ADC is capable of processing either + or – input signals, but this design only uses + inputs. The ADC produces a 16-bit image, but bit 16 is the sign bit. The software for the HFC-AI16F reserves this bit for channel status.

6.3 Single Channel Adjustment Algorithm

The single channel adjustment algorithm is used in the software of AI16I, AO8F, AC36 boards to achieve better accuracy. Offset and gain for each channel will be determined by testing or default to zero, and an EPROM file will be built incorporating the offset and gain parameters in a specific location of EPROM memory. First time the I/O software enters the scan module, the software obtains the offset and gain parameters from the specific memory location in EPROM to calculate actual raw value for 4 mA and 20 mA of each analog input or analog output channel and saves them in a buffer as two arrays: CALZERO and CALGAIN.

Both 12-bit and 15-bit adjustments shall be handled according to the board type. 15-bit AI requires over range and under range check. 12-bit AO doesn't have over range or under range, but needs to make sure that negative number set to 0 and over 0FFFH number clamped to 0FFFH to avoid overflow.

6.4 HFC-AI16F-board Specific Modules

6.4.1 I/O Scan Module

The SCAN module performs AI scan for sixteen channels

6.4.2 Process Command routine

For normal update messages, this routine doesn't do anything because there is no AO channel on card. For UCP diagnostics messages, are processed as described in document DS-002002-02.

6.5 Data Structure

6.5.1 Scan Data

The data field of the response message sent to the HFC-SBC06 controller contains AI images for sixteen channels as follows:

Table 3. Byte Assignments For Scan Data

Byte	AI	Byte	AI	Byte	AI	Byte	AI
0	CH1 (L)	8	CH5 (L)	16	CH9 (L)	24	CH13 (L)
1	CH1 (H)	9	CH5 (H)	17	CH9 (H)	25	CH13 (H)
2	CH2 (L)	10	CH6 (L)	18	CH10 (L)	26	CH14 (L)
3	CH2 (H)	11	CH6 (H)	19	CH10 (H)	27	CH14 (H)
4	CH3 (L)	12	CH7 (L)	20	CH11 (L)	28	CH15 (L)
5	CH3 (H)	13	CH7 (H)	21	CH11 (H)	29	CH15 (H)
6	CH4 (L)	14	CH8 (L)	22	CH12 (L)	30	CH16 (L)
7	CH4 (H)	15	CH8 (H)	23	CH12 (H)	31	CH16 (H)

7. Module Implementation Description

7.1 Hardware Schematics

The schematic for the HFC-AI16F board is drawing 400433-01.

7.2 Hardware Components – Bill of Materials

The part number of the HFC-AI16F board is 40043201, and its bill of materials is 400432-01.

7.3 Software Source Code Listing

The HFC-AI16F board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

8. Design Safety

Refer to MS901-000-02 for a discussion of design safety issues.

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HFC-6000 Product Line

HFC-AO8 Board
Module Detailed Design Specification

Eight Channel Analog Output Board

DS901-000-08

Rev C

NON-PROPRIETARY

Effective Date	3/12/07
Author	J. Taylor
Reviewer	B. Cain
Approval	D. Briner

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Revision History

Date	*Revision*	*Author*	*Changes*
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3/2/07	C	J Taylor	SCR 1766; restored software coverage to Rev B.

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1.0 INTRODUCTION

The HFC-AO8 assembly is an 8-channel analog output board. This assembly operates as a standard AO board in an HFC-6000 control system. It receives digital output images from the system controller and performs D/A conversion for each channel at regular intervals. The HFC-SBC06 controller initiates communication with a configured HFC-AO8 board during its regular scan cycles, and the HFC-AO8 board receives the current digital image for all output channels from the poll message and returns current status.

Descriptions and discussions of the architectural and design descriptions of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Card Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

This document describes the detailed structure and design of the HFC-AO8 board. The design descriptions of the common software modules and hardware functions of I/O boards are covered in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The description of the operation and function of an HFC-AO8 board will be presented using design, implementation, and configuration information.

1.1 REFERENCES

700901-06	HFC-6000 I/O Card Requirements Specification
400473-01	HFC-AI16 Schematic
400472-01	HFC-AO8F 8 channel, 4-20mA Assembly
400472-02	HFC-AO8E 8 channel, 0-10VAssembly
WI-ENG-106	Development of Hardware Design Specification
MS901-000-02	HFC-6000 Product Line, I/O Module Design Specification
DS901-000-02	HFC-6000 Product Line, I/O Module Detailed Design Specification
RS901-000-40	HFC-6000 Product Line, PCB Layout Requirements

1.2 SPECIAL TERMS AND ABBREVIATIONS

I/O	Input/Output
LSB	Least Significant Bit
RAM	Random Access Memory
AO8F	0-20mA 8 Channel Analog Output
AO8E	0-10V 8 Channel Analog Output
D/A	Digital to Analog Converter

2.0 SPECIFICATIONS

- Environmental Extremes

Temperature:	0° to 55° C (operating)
	0° to 70° C (storage)
Relative Humidity:	5% to 95%, non-condensing

- Power Requirements
  External Power Supply: +24 vdc, 0.4 A maximum load.

- Onboard Clock Rate
  Microprocessor Clock: 22.1184 MHz

Output Channel Rating: 0 to 20 mA (-01 assembly) or 0 to 10 V (-02 assembly) with 1/16-A line fuse for each channel and a 0.5-A line fuse for all eight channels

- Mounting Requirements: Mounts vertically in an HFC-6000 chassis

3.0 CONTROLS AND INDICATORS

The firmware determines the overall operating characteristics of the hardware on the HFC-AO8 board. The HFC-AO8 board only includes the set of four LEDs and one switch that are common to all I/O board types (DS901-000-02). However, the board does include eight jumpers and nine fuses. These devices and the functions that they control are as follows:

3.1 JUMPERS

W3-W5 Fail-state jumpers, refer to paragraph 4.6.2 in this document for more information on the fail-state jumpers.

W37 Installed to make analog return and digital return electrical common.

E1-E2 Installed during calibration only to disable the NMI signal. When this jumper is removed, the D-latch U41-A activates a high NMI signal. E1-E2 should be removed for normal operation.

E5-E6 Function not currently defined.

3.2 FUSES

F1, F2, F4-F9 Provide separate overload protection for each AO channel.

F3 Provides common overload protection for the 24-vdc power source to the eight output drivers.

4.0 FUNCTIONAL DESCRIPTION

The HFC-AO8 board is controlled by an onboard 80C188EB microprocessor and provides a hardware interface between an HFC-6000 control system and field equipment requiring analog control signals.

4.1 OVERVIEW

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Card Module Design Specification. The major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Performs reset and initialization of onboard hardware.
- Responds to data transmissions from the HFC-6000 controller.
- Receives AO images for each channel from the controller and store that data in local memory.
- Transfer AO images from memory to the Digital-to-Analog (D/A) converter for each channel.
- Control the D/A conversion process.

4.2 POWER DISTRIBUTION

The board receives redundant 24-vdc power feeds from the back plane connector J1. The two power feeds are diode auctioneered, and the combined 24-vdc power line is divided into four branches. One branch is routed to the input of an onboard voltage regulator. The second branch is routed through a 0.5-A onboard line fuse. The remaining two branches are routed to two ±15-vdc power supplies. These separate branches provide operating power for the following functions:

- The onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for logic components on the HFC-AO8 board.

- The fused 24-vdc-power trace is routed to the VCC port of the output driver for each Analog Output (AO) channel.

- The two +15 vdc supplies provide operating power to the DAC for each channel. One of the +15 supplies also provides power to a precision 2.5-vdc regulator that provides a reference voltage to all eight DACs.

4.3 RESET/INITIALIZATION

The Micro Monitor chip monitors the voltage level of the +5-vdc power rail, the state of the onboard reset switch (SW1), and normal operation of the microprocessor clock. When power is first applied to the board, the low state of the logic power rail causes the Micro Monitor chip to hold a /RESIN signal at a low level. After logic power increases above 4.5-vdc, the Micro Monitor chip keeps the /RESIN signal low for an additional 350 ms to ensure that all transient signals have dissipated before the microprocessor begins operation. During subsequent operation, the chip monitors its inputs for actuation of the RESET switch (SW1) or a significant drop in the voltage level of the onboard logic power rail.

When the microprocessor begins running, CLKOUT pulses are routed from the microprocessor to the Micro Monitor chip. If the microprocessor clock stops running for a period of 50 ms, the Micro Monitor chip automatically activates the /RESIN signal to reset

the microprocessor. If the operator presses the SW1 RESET switch, circuitry on the board causes the Micro Monitor chip to activate the /RESIN signal. When the operator releases the RESET switch, the /RESIN signal remains low for an additional 350 ms before permitting the microprocessor to resume normal operation.

4.4 MEMORY STRUCTURE

Memory on the HFC-AO8 board is organized into two banks of private memory for the microprocessor. Private memory for the 80C188EB microprocessor consists of one bank of EPROM and one bank of RAM. The private memory banks are connected directly to the address and data lines of the microprocessor.

4.5 INTERRUPT PROCESSING

The 80C188EB microprocessor provides a modular core for processing interrupts and exception conditions. The chip architecture includes an NMI input port, a variety of internally generated interrupts, and ports for five maskable interrupts (INT0 through INT4). For this application, the five maskable interrupt inputs are disabled. The NMI input is configured to halt the processor on a watchdog timeout.

4.6 MICROPROCESSOR PERIPHERAL PORTS

The microprocessor controls the following peripheral ports:

- Digital-to-Analog Converter (DAC) data output port
- Analog Output (AO) select output port
- Fail safe condition data input port
- Link address data input port
- Redundant serial port.

The Link Address input port, and the Redundant serial port are covered for the general case of I/O cards, therefore, they are not discussed here. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the three I/O ports

4.6.1 AO INTERFACE

The interface between the microprocessor and the analog outputs includes both the DAC data output port and the AO select output port. The interface between the microprocessor and each AO channel consists of an eight-bit latch, a one-of-eight demultiplexer, and a separate D/A converter for each channel. Because each AO image consists of 12 bits, the microprocessor must run two write cycles to each DAC. The hardware design for the card requires that the microprocessor transfer the most significant (high) byte of data to the DAC first and then the least significant (low) byte. During the second write cycle, the microprocessor transfers both bytes of data to the internal DAC register, enabling the DAC process to begin. The overall process required for data transfer to a single DAC is as follows:

1. The microprocessor runs an I/O write cycle with programmable output port P1.0 pulled low to transfer the high byte of the AO image to the eight-bit latch. The latch retains this data until it is overwritten by a subsequent write cycle. The output ports of the latch control an eight-bit data bus that is connected to each of the DAC chips.

2. The microprocessor pulls programmable port P1.1 low (CSMSB/) to transfer the high byte of the AO image from the eight-bit data bus into the input register of all DAC chips simultaneously.

3. The microprocessor runs a second write cycle to transfer the low byte of the AO image to the eight-bit latch.

4. The microprocessor places the binary code for the AO channel being processed on address lines A01, A02, and A03. The one-of-eight demultiplexer uses this code to activate the chip select signal (CS/) for the DAC associated with this AO channel.

5. The low active CS/ signal transfers the low byte from the eight-bit data bus into the DAC for the selected channel, and it also transfers the entire AO image into the DAC register.

6. When the CS/ signal returns to a high state, the DAC begins the conversion process.

Each DAC is set to operate in a voltage-switching mode. To ensure accuracy in the voltage-switching mode, the full-scale output of each converter is limited to 2.5-vdc. Therefore, the onboard circuitry provides the DAC with a precision 2.500-vdc reference voltage input.

Once the AO image has been loaded into the DAC register, DAC automatically uses that data to perform D/A conversion, unless overridden by a failsafe condition (controlled by the FH/L and FH/C signals). Of the 16-bits in the DAC register, only 12 bits are used to represent the channel output value; and these 12 bits are either right or left justified in the register, depending on the logic state of the FH/L and FH/C signals (Table 2). The DAC converts the AO image into a corresponding current value, and the current signal provides the input to an amplifier, which produces an output signal between 0-5 vdc. This voltage is supplied to the input of a precision voltage-to-current converter, which produces an output signal having a range of 0 to 20 mA.

The DAC produces an analog output that has a full-scale range of 0 to 2.5 vdc. The individual analog channels condition the output to provide 0-20 mA (-01 assembly). The –02 assembly has 499 Ω resistors on each output channel that convert the 0-20 mA signal into a 0- 10 V signal.

4.6.2 FAIL SAFE CONDITION DATA INPUT PORT

The design of the HFC-AO8 includes three jumpers that are used to configure the card for one of thee failsafe modes: fail high, fail low, hold last state. Each failsafe jumper (W3, W4, and W5) controls the logic state of a separate input to an eight-bit buffer. The microprocessor can read the status of these jumpers by running a bus read cycle with programmable output port P1.0 pulled low. These inputs enable the software to determine the failure state selected by the jumper strapping. If the card looses communication with the controller, the software can

initiate the transition to the fail high/low state for each channel by transferring the appropriate AO image (00_H or FF_H) to each DAC. However, if a watchdog timeout occurs, the microprocessor stops running. During a watchdog timeout, jumpers W4 and W5 control the failsafe function. These jumpers control the logic state of the FH/L and FH/C signals. If jumper E1-E2 is removed, the logic state of the FH/L and FH/C signals force the DAC into the desired failure state on watchdog timeout. The hard-wired failure state produced by jumpers W4 and W5 following watchdog timeout are defined in Table 1.

In addition to controlling the failsafe response of the DAC, the FH/L signal also determines the required justification of the AO image in the DAC register. The software must read the jumper status in order to provide the proper justification for the AO image before transferring that image to the DAC. Table 2 defines the required justification of the image data based on the status of W5 when the FH/C signal is high.

Table 1. AO Failsafe Control

Jumper	Status	Function
W4	Removed	On watchdog timeout the microprocessor stops operation, and each DAC retains the last AO image received .
W4	Installed	On watchdog timeout the microprocessor stops operation; the high state of the FH/L signal and the low state of the FH/C signal overwrite the AO image in each DAC with all 1s.
W5	Removed	
W4	Installed	On watchdog timeout the microprocessor stops operation; the low state of the FH/L and FH/C signals overwrite the AO image in each DAC with all 0s.
W5	Installed	

Table 2. Data Justification of AO Images

W5	Most Significant Byte								Least Significant Byte							
ON	MSB											LSB	x	x	x	x
OFF	x	x	x	X	MSB											LSB
	8	7	6	5	4	3	2	1	8	7	6	5	4	3	2	1

5.0 HARDWARE CONNECTIONS

The HFC-AO8 card contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-AO8 and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 3.

Table 3. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1		P2-C1	
P2-A3		P2-C3	
P2-A4		P2-C4	
P2-A6		P2-C6	
P2-A7		P2-C7	
P2-A9		P2-C9	
P2-A10		P2-C10	
P2-A12		P2-C12	

6.0 SOFTWARE DETAILED DESIGN SPECIFICATION

The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AO8F board.

6.1 BOARD INFORMATION

The AO8F card has a total of eight identical AO channels rated for 0-20 mA. Each channel includes a separate 12-bit D/A converter.

6.2 ANALOG OUTPUT SCAN ALGORITHM

An on-board fail-hi / fail-lo jumper provides option for using left justified or right justified output data for the D/A converter. Before writing analog output images to the D/A converters, the software checks if the jumper is installed. If it is installed, the software left-shifts each output image four bit positions to make it left-justified. (Each 12-bit image is stored as a single data byte.) If the jumper is not installed, the software leaves the AO images just as they are received from the controller.

There are two calibration parameters for each channel that were originally obtained from the EPROM. The software uses these parameters to adjust the output image of each channel for better accuracy. Then the software strobes the adjusted output image into D/A converter output for each channel. Refer to Section 4.3 for adjustment algorithm using calibration parameters.

6.3 SINGLE CHANNEL ADJUSTMENT ALGORITHM

The single channel adjustment algorithm is used in the software of AI16I, AO8F, AC36 cards to achieve better accuracy. Offset and gain for each channel will be determined by testing or default to zero, and an EPROM file will be built incorporating the offset and gain parameters in a specific location of EPROM memory. First time the I/O software enters scan module,

the software obtains the offset and gain parameters from the specific memory location in EPROM to calculate actual raw value for 4 mA and 20 mA of each analog input or analog output channel and saves them in a buffer as two arrays: CALZERO and CALGAIN.

The CALZERO array stores for each channel the actual value for 4 mA, i.e. STDZERO adjusted by offset parameter for that channel. The CALGAIN array stores for each channel the actual value for 20 mA, i.e. STDGAIN adjusted by gain parameter for that channel.

Let BX = channel number, then

Both 12-bit and 15-bit adjustments are handled according to the board type. The 15-bit AI image requires over range and under range checks. The 12-bit AO does not have over range or under range; however, the algorithm sets any negative value to 0 and changes any value above $0FFF_H$ to $0FFF_H$ to prevent overflow.

6.4 HFC-AO8F BOARD SPECIFIC MODULES

6.4.1 I/O SCAN MODULE

The HFC-AO8F board firmware has in I/O scan module like all other I/O boards, but because this board has no input channels, this module has no function.

6.4.2 PROCESS COMMAND ROUTINE

For normal update messages, this routine reads eight AO images and transfers them to the Scan Work Buffer. For UCP diagnostics messages, are processed as described in document DS-002002-02.

6.5 DATA STRUCTURE

6.5.1 SCAN DATA

The data field of the request message coming from the HFC-SBC06 controller contains AO images for eight channels as follows:

Table 4. Byte Assignments For Scan Data

Byte	AO	Byte	AO
0	CH1 (L)	8	CH5 (L)
1	CH1 (H)	9	CH5 (H)
2	CH2 (L)	10	CH6 (L)
3	CH2 (H)	11	CH6 (H)
4	CH3 (L)	12	CH7 (L)
5	CH3 (H)	13	CH7 (H)
6	CH4 (L)	14	CH8 (L)
7	CH4 (H)	15	CH8 (H)

7.0 MODULE IMPLEMENTATION DESCRIPTION

7.1 HARDWARE SCHEMATICS

The schematic for the HFC-AO8F board is drawing 400471-01.

7.2 HARDWARE COMPONENTS – BILL OF MATERIALS

The part number of the HFC-AO8F board is 40047201, and its bill of materials is 400472-01.

7.3 SOFTWARE SOURCE CODE LISTING

The HFC-AO8F board software consists of all common modules described in document DS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification and the following programs:

8.0 DESIGN SAFETY

Refer to MS901-000-02 for a discussion of design safety for HFC-6000 I/O modules.

HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-AI8M
Module Detailed Design Specification

Eight Channel RTD Input Board

NON-PROPRIETARY

DS901-000-11

Rev B

Effective Date	3/12/07
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Date	Revision	Author	Changes
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1. Introduction

The HFC-AI8M Resistance Temperature Detector (RTD) printed circuit board (PCB) is an input-conditioning device for an HFC-6000 control system. Current hardware design for the HFC-6000 product line supports 100-Ω and 200-Ω platinum RTDs only. Refer to Table 1. This assembly operates as a standard I/O board in an HFC-6000 control system. The HFC-AI8M PCB receives the voltage images of its isolated analog inputs from external RTDs and presents them for conversion into a digital count value image for each channel at regular time intervals.

Table 1. Input Device Table

Supported	Device ID	Device Type Description
Yes	0H	100 Ohm Platinum, DIN 43760 standard
Yes	1H	100 Ohm Platinum, SAMA standard
No	2H	10 Ohm Copper
No	3H	120 Ohm Nickel
Yes	4H	200 Ohm Platinum, DIN 43760 standard
Yes	5H	200 Ohm Platinum, SAMA standard
No	6H	2K Ohm Resistive Device
No	7H	5K Ohm Resistive Device

Descriptions and discussions of the architecture and design of a standard HFC-6000 I/O card, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Card Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01

Subsequent sections of this document provide detailed structure and design descriptions of the HFC-AI8M card, with concentration on the specific characteristics of an HFC-AI8M card. The design descriptions of the common software modules of I/O cards are covered in document DS901-000-02, HFC-6000 I/O Card Module Detailed Design Specification. The purpose of this document is to present a detailed description of the methods and strategies used to accomplish the specific operation and function of an HFC-AI8M card. The discussion of the operation and function of an HFC-AI8M card will be presented using design, implementation, and configuration information.

2. HFC-AI8M Functional Description

The HFC-AI8M (RTD) board includes one microprocessor with a local memory array, a serial port for communicating with the HFC-SBC06 controller board, and a 16-bit analog to digital converter for voltage to digital image conversion. The HFC-AI8M RTD board is designed to interface RTD field inputs to an HFC-6000 control system. The HFC-AI8M board is supervised with an 80C188EB microprocessor and accommodates connections for up to eight RTD inputs. Major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Control onboard reset and initialization functions.

- Respond to data transmissions from the HFC-6000 controller.
- Run regular automatic calibration cycles for onboard analog circuitry.
- Sample the input signals from each channel and control the ADC processing cycles.
- Convert raw count data into a 15-bit digital image for each input channel.
- Transfer the AI image for each channel into onboard memory.

3. Hardware Detailed Design Specifications

3.1 COMMON DESIGN ELEMENTS

The HFC-AI8M has the following areas of design that are common to HFC-6000 I/O cards. Descriptions and discussions of the architecture and design of these areas are provided in document MS901-000-02, HFC-6000 I/O Card Module Design Specification.

- Reset/Initialization of the Board.
- Hardware Reset Function.
- Watchdog Timer Functions.
- Microprocessor Type and Implementation Criteria.
- Link Address Data Input Port.
- Processor Serial I/O Ports (Note: Additional material in section 3.5)

3.2 MODULE SPECIFICATION

- Environmental mits
  Temperature: 0° to 55 C° (operating)
  0° to 70 C° (storage)
  Humidity: 5% to 95%, non-condensing

- Power Requirement
  External Input Power: +24-VDC , 0.4 A maximum load.

- Onboard Clock Rate
  Microprocessor Clock: 22.1184 MHz

- Devices Supported: 100-Ω two or three wire Platinum RTD, DIN 43760

- Input Image for 100-ohm RTD:
  AI Image 15-bit digital image for each input channel
  Accuracy ± 0.1% of Full Span
  Full Design Range 0° to 700° C

- Restricted Span Options 0° to 50° C with ±0.05° accuracy over entire span
  0° to 100° C with ±0.1° accuracy over entire span
  0° to 200° C with ±0.2° accuracy over entire span

- Mounting Requirements: Mounts vertically in HFC-6000 board chassis.

- The HFC-AI8M PCB meets the requirements of seismic category I.

- Onboard Power Regulation: A separate constant current source for each of the eight RTD channels is provided.

3.3 ONBOARD POWER DISTRIBUTION

The board receives redundant 24-VDC power feeds from the back plane connector P1. The two power feeds are diode auctioneered by CR1 and CR2, and the resulting output voltage is routed to the following components:

- An onboard voltage regulator (VR1) converts the 24-VDC source power to +5-VDC power required for onboard digital components.

- An onboard voltage regulator (PS1) converts the 24-VDC source power to ± 15-VDC non-isolated power. This supplies operating power for the non-isolated analog circuitry.

- An onboard voltage regulator (PS2) converts the 24-VDC source power to ± 15-VDC isolated power. This supplies operating power for isolated analog circuitry.

- The non-isolated +15-VDC power line also provides source power for a +5-VDC power supply. This power supply (Q13) provides operating power for the analog and digital circuits within the ADC chip.

- The ± 15-VDC isolated power supplies operating power for isolated reference voltage (Q2) of 10.00 VDC for calibration of the input amplifier circuitry.

- The isolated +15-VDC power line provides source power for precision voltage reference (U3) for eight constant current drivers (Q1 through Q8). Each constant current driver serves as an isolated current source for a single RTD channel.

- Fuses (F1-F8) provide overload protection for each RTD constant current source (PT1_RP through PT8_RP).

3.4 ONBOARD MEMORY CONFIGURATION

Memory on the HFC-AI8M board is organized into three banks of private memory for the microprocessor. Private memory for the 80C188EB microprocessor consists of one bank of EPROM, one bank of EEPROM, and one bank of RAM. The upper and low memories U5 and U43) are of common design as specified in MS901-000-02, HFC-6000 I/O Card Module Design Specification, and are connected directly to the address and data lines of the microprocessor.

The mid memory array consists of an 8K by 8-bit EEPROM (U23). The chip select signal for this bank of memory is controlled by programmable port P1.2 of the microprocessor, and its initial and final address are determined by software. The write enable line for the

EEPROM is controlled by jumper W5. During calibration, jumper W5 is installed so that zero and span count values for each channel can be written to this area of memory. After calibration is completed, jumper W5 should be removed to prevent overwriting the calibration data. Throughout normal operation, the count values in mid memory are used to calculate correction parameters for the raw count data received from the ADC.

3.5 INTERRUPT PROCESSING

The 80C188EB microprocessor uses the common interrupt processing as specified in MS901-000-02, HFC-6000 I/O Card Module Design Specification. For this application, three of the four maskable interrupt inputs are disabled. The NMI input is controlled by the watchdog timer, and the INT4 input is configured to detect completion of the A/D cycle. By using INT4, the microprocessor can read the converted analog data immediately after the AD conversion cycle is complete.

3.6 MICROPROCESSOR PERIPHERAL PORTS

The microprocessor controls the following peripheral ports:

3.6.1 Analog Input (AI) Point Select Output Port

The 80C188EB microprocessor uses a 4-bit code to control channel selection for analog input. This 4-bit code is transferred to a 4-to-10 binary-coded decimal (BCD) decoder that converts the code into a single channel select output signal. The channel select output from the BCD decoder activates one of the corresponding input RTD channel point 1 through point 10 (PT01 through PT10):

- Points 1 through 8 are the RTD analog field input channels. Each point includes two input signals designated channel A (CHA) and channel B (CHB).

- Point 9 is the zero reference. This input is selected once each scan and allows the board to automatically compensate for offset drift errors. When selected, this channel connects the isolated common to the input of the analog processing circuit. The resulting count value is compared with a value stored in memory. If the value read differs from the value in memory by less than a fixed tolerance, the software calculates a correction factor to adjust the raw count values for points 1 through 8.

- Point 10 is the auto-calibration reference voltage. The auto-calibration input voltage allows the board to automatically compensate for gain drift errors in both CHA and CHB. This fixed voltage level is read and compared to a value stored in memory. If the value read differs from the value in memory by less than a fixed tolerance, the software calculates a correction factor to adjust the raw count values for points 1 through 8.

When an RTD channel is selected, two photovoltaic relays become forward biased and pass two analog inputs to instrumentation amplifiers K24 and K27. The microprocessor enables corresponding sample/hold devices to receive the input and hold the voltage level until read.

Next, the microprocessor activates either the CHA/ or CHB/ signals to pass one of the analog inputs through the isolation amplifier K21, which supplies the input signal to the non-isolated circuitry associated with the A/D converter.

3.6.2 Analog-to-Digital (A/D) Select Output Port

The 80C188EB microprocessor can select one of ten analog input channels using the four input channels through latched output select lines at U27 and U18. These output select lines control which analog signal passes to the input of the A/D converter. The four select outputs from U27 and U18 control the following input signals to the A/D converter:

- CHA/ or CHB/, as described in paragraph 3.5, passes either the CHA or the CHB signal for the analog input points selected (PT01 through PT10) to the input of the amplifier K21.

- FIELD/ enables the output from the K21 amplifier to pass input to the A/D converter.

- The OFFSET/ signal passes the zero offset voltage of K21 to the input of the A/D converter. (The FIELD/ and OFFSET/ selection signals are mutually exclusive.)

- The A0 signal can be toggled to allow the A/D image to be read as two 8-bit bytes. During a conversion cycle setting this LOW will enable the low byte to be read. HIGH will enable the high byte to be read.

- /CS is used in combination with other signals to control the data conversion cycle. Tying it high will place the data bus interface of the ADC in Hi-Z state. Setting it LOW places the A/D converter chip in a hold state and starts the conversion.

- R/C is used to control read and convert modes. When /CS is LOW and Busy/HIGH, the High-to LOW transition of R/C starts the conversion process. With /CS Low, the Low-to High transition of R/C enables parallel output to the data bus.

3.6.3 A/D Converter Data Input Port

The 80C188EB microprocessor reads digital input from the A/D conversion cycles through an 8-bit buffer. In order to read a digital image of an input channel from the A/D converter, the microprocessor must perform the following operations:

1. Run a write cycle to the point select output port. This operation sets the levels of the AO, R/C, and /CS signals to enable an A/D conversion cycle. (When reading PT00 through PT08, it also selects the signal source.)

2. Run a write cycle to the VIN select port. The output signal from this port operation routes the selected signal to the input of the A/D converter.

3. Set the /CS input to the A/D converter low. This starts the A/D conversion cycle.

4. At the start of the A/D conversion cycle, the ADC sets its /BUSY signal low. The low -to-high transition of the /BUSY signal indicates completion of the conversion cycle and triggers INT4.

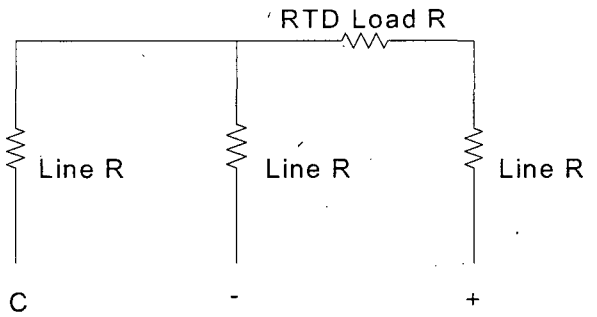
5. Run two read cycles to the input port. During these two read cycles, the logic level of the AO signal distinguishes between the low and high byte of the AI image.

6. Disable the /CS signal after start of conversion cycle.. Repeat this sequence for additional A/D cycles.

3.6.6 RTD Inputs

Each RTD channel is designed to accept either a two- or a three-wire RTD sensor (Figure 1.) The typical three-wire sensor requires connection for Signal+ (constant current supply), Signal- (constant current return), and common. The RTD algorithm measures the voltage difference between the Signal+ and the Signal- terminals and then uses the common input to compensate for the voltage drop in the field wires out to the RTD element.

Figure 1. Typical Three-Wire RTD



In order to reduce possible interference and signal coupling to a minimum, each channel provides the following features:

3.7 CONTROLS, JUMPERS, AND LED INDICATORS

The firmware determines the overall operating characteristics of the hardware on the HFC-AI8M board. However, the board contains eight jumpers, two potentiometers, one switch and eight fuses. These devices control the following functions.

3.7.1 Jumpers

W1 -- Function not currently defined.

W2 -- Passes the analog input signal to the A/D converter (ADC). This jumper is removed only to permit adjustment of the gain and offset for the ADC during calibration. It must be installed for all other phases of calibration and normal operation.

W3 -- Function not currently defined.

W4 -- Function not currently defined.

W5 -- Connects the WE/ signal to the IC socket for U23. This jumper is installed to enable transfer of calibration data to the EEPROM. It should be removed for normal operation.

W37 -- Installed to make analog and digital return electrically common.

E1-E2 -- Installed during calibration to disable the NMI signal. When this jumper is removed, D-latch U41-A activates a high NMI signal following watchdog timeout.

3.7.2 Potentiometers

R108 – Enables manual adjustment of the gain for the ADC during calibration.

R110 – Enables manual adjustment of the bipolar offset for the ADC during calibration.

3.7.3 Switches

SW1 – Used to reset the 80C188EB microprocessor.

3.7.4 LED Indicators

DS1-1 -- DMT (Dead Man Timer) is controlled by the watchdog timer. During normal operation the LED should remain constantly lit.

DS1-2 -- RX (Receive Data) The RX LED will light when the 80C188EB microprocessor is receiving data on the serial interface. This LED should flash on and off periodically throughout normal operation.

DS1-3 -- TX (Transmit Data) The TX LED will light when the 80C188EB microprocessor is transmitting data on the serial interface. This LED should flash on and off periodically throughout normal operation.

DS1-4 – SYS A/B LED lights when serial port A is enabled to receive data. When the LED is out, serial port B is enabled to receive data. During normal operation, the status of this LED identifies the primary ICL channel.

3.8 HARDWARE CONNECTIONS

The HFC-AI8M circuit card assembly contains board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 back plane. The pin assignments for P1 are listed in the common module description DS901-000-02. Table 2 lists the pin assignments for connector P2.

Table 2. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1		P2-C1	
P2-A2		P2-C2	
P2-A3		P2-C3	
P2-A4		P2-C4	
P2-A5		P2-C5	
P2-A6		P2-C6	
P2-A7		P2-C7	
P2-A8		P2-C8	
P2-A9		P2-C9	
P2-A10		P2-C10	
P2-A11		P2-C11	
P2-A12		P2-C12	

4. RTD ALGORITHM

RTD standards define platinum resistance vs. temperature behavior by the Callendar-Van Dusen equation, a non-linear mathematical model. These standards include the RTD value at 0° C, R(0), and equation coefficients. The Platinum RTD Callendar-Van Dusen non-linear model is a fourth order polynomial for negative temperatures and a quadric for positive temperatures. The HFC AI8M circuit is designed for positive temperatures of 0° C and above and uses the quadric model.

The Callendar-Van Dusen formula below defines the RTD in the general form of RX = R(0) + ΔR, where ΔR is the temperature dependent part of the RTD for T > 0;

$$RX = R(0) + \Delta R$$

$$RX = R(0) \times [1 + A \times T + B \times T^2]$$

Where:

RX = Resistance of the RTD sensor in Ohms at the current sensor temperature.
R (0) = Resistance of the RTD sensor at 0° C.
T = the current temperature of the sensor.
A = Callendar-Van Dusen coefficient furnished by the RTD manufacturer.
B = Callendar-Van Dusen coefficient furnished by the RTD manufacturer.

Coefficients A and B are defined by RTD standards and measured by RTD manufacturers as specified by ASTM 3711 and IEC 60751 standards.

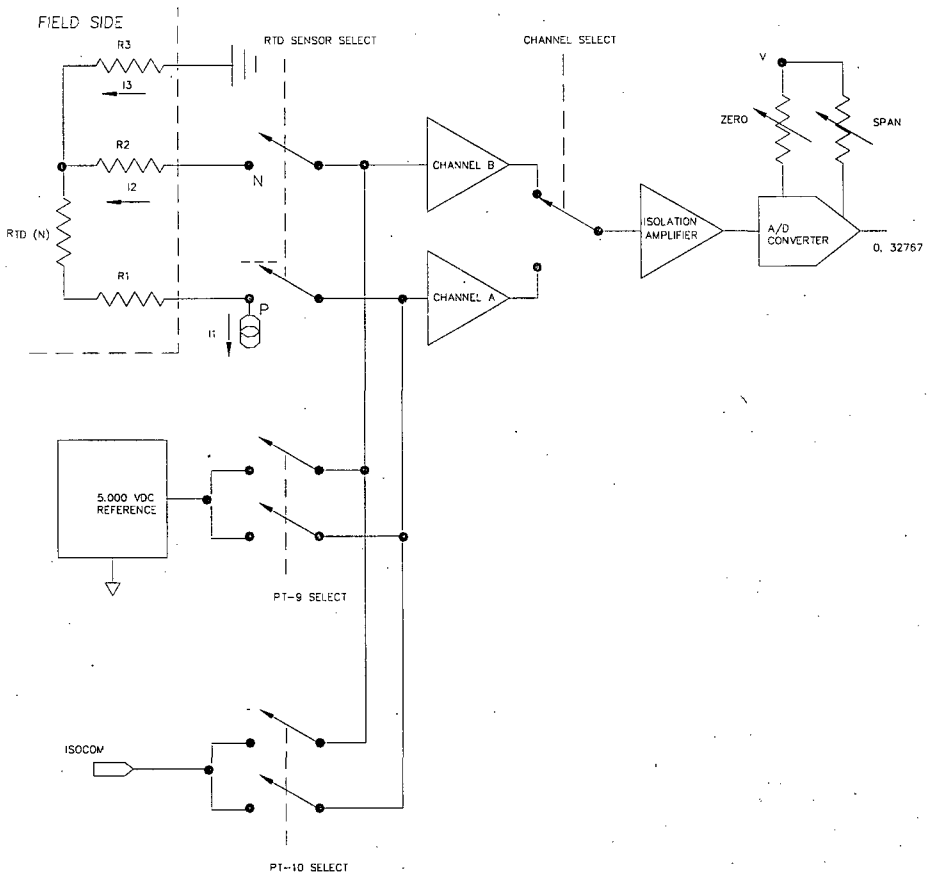
Solving this formula for T:

$$T=\frac{-A \pm \sqrt{A^2 - 4B(1-RX/R(0))}}{2B}$$

4.1 Resistance Measurement Method

Figure 2 illustrates the circuit technique utilized for measuring resistance of a RTD. The 3-wire configuration will be used in this illustration. This configuration has the advantage of compensating for the use of unmatched and long field cables. As outlined above the value of the resistance of the RTD is given as R (0) + ΔR. The circuit shown in the figure provides a current (I1) from a constant current source. Assuming equal line resistances for the three field wires this measurement technique eliminates their effect. Moreover, R (0), the temperature independent resistance part of the RTD is removed.

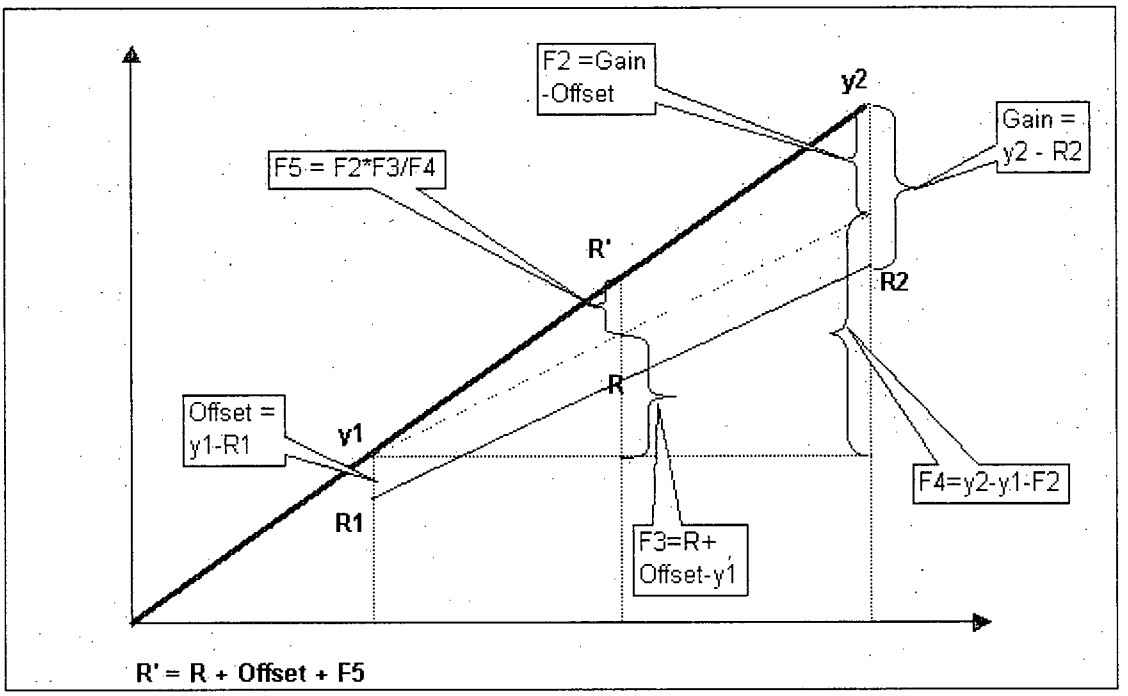
Figure 2. AI8M Simplified Circuit



4.2 A/D Image Compensation Methodology

This section uses an example to show the basic methodology employed in the A/D image compensation algorithm used by this assembly and software. Figure 3 illustrates the use of correction factors. The inputs are represented on the X axis and the corresponding A/D output image is shown on the Y axis. The line in bold *y1y2* represents the values of the A/D image count at the time of board calibration. The line *R1R2* represents the actual values of the A/D image count during normal operation. In order to correct a raw count value R, the value R' is calculated as it would appear on line y1y2, the calibration curve.

Figure 3. Compensation for A/D Images with Calibration Data



Offsets and gains are calculated as follows:

4.3 Operation

Before the initial use of each board, the A/D circuitry on board and the reference channels must be calibrated. During the calibration, the potentiometers are adjusted for the offset and gain channel of the ADC. Each of the reference channels and RTD channels is given a predefined resistance input and the raw count values from the ADC are saved in the onboard EEPROM. These calibration data will be used as correction factors for the actual raw count values during normal operation.

During normal operation, an RTD scan is performed at regular intervals. A calibration test is performed first to make sure that offset drifts and gain drifts are within acceptable ranges. Then offset and gain correction factors are calculated. Each RTD input channel is scanned and the A/D raw count image is compensated using the formulas as described in Section 4.2. Normalization is performed on the corrected value to get the final RTD image.

4.3.1 A/D Calibration

The A/D calibration is facilitated by isolating the A/D circuitry and using a Beta Calibrator to apply a zero voltage and a reference voltage of 5.000 volts to the inputs of the A/D. The calibration sequence is as follows:

4.3.2 Normal Operation

4.3.2.1 Calibration Test and A & B Channel Compensation

During each RTD scan cycle, a calibration test is performed first. Scan in turn point 9 channel A, point 10 channel A, point 9 channel B and point 10 channel B. Compare the raw count value obtained with the corresponding calibration data stored in the EEPROM. If the raw count values are within range (±120 counts of the stored value), calculate offset drift and gain drift of the A/D images for compensating the actual RTD raw count values. The calculations are performed using the formulas in Section 4.2.

4.3.2.2 RTD Input Channel Scan and Compensation Factors

Each RTD channel is scanned and then corrected for offset drifts and gain drifts. The algorithm is as described in Section 4.2. Point 1 through 8 are RTD inputs channels. Point 9 is the zero reference channel and the point 10 is the gain reference channel.

4.3.2.3 Normalization and Linearization

5. Software Functional Design Descriptions

The design descriptions of the common software modules are provided in MS901-000-02, HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AI8M board.

5.1 Board Information

HFC-AI8M card provides eight identical input channels from RTD elements (point 1 through 8) and two input channels that provide precision inputs for zero voltage (point 9) and span voltage (point 10) references. There are also a set of potentiometers and jumpers to support calibration of the analog section of the board. Calibration of these components must be accomplished before channel-by-channel calibration can be accomplished. The calibration data is stored in the onboard EEPROM. The board includes one 16-bit A/D converter that produces the raw digital image for each channel. The ADC was designed to accept both positive and negative input signals. Because this application requires only positive inputs, the sign bit of the digital image is reserved to represent status data.

5.2 Board Specific Modules

5.2.1 I/O Scan Module

Every scan cycle, this routine executes an RTD calibration test first. If the test fails, the software skips the AI scan, marks response message for a bad response, sets the calibration error bit in the diagnostic byte, and holds all AI images at their last valid value (if any). If the calibration test passes, the module automatically scales the input count values using the algorithm described in Section 4. The software scans the eight AI channels, applies the compensation factors, and tests the result for over range status. Any out of range input will cause the software to set an error bit in the diagnostic byte. A moving average will be taken over the current point data and previous data. The final AI images will be transferred to the response buffer.

5.2.2 RTD Calibration Test Routine

5.2.3 Scan RTD Channels Routine

5.2.4 Process Command Routine

5.3 Data Structure

5.3.1 Scan Data

The data field of the response message to the HFC-SBC06 controller contains AI images for eight channels as follows:

Table 3. AI Image

Byte	AI	Byte	AI
0	CH1 (L)	8	CH5 (L)
1	CH1 (H)	9	CH5 (H)
2	CH2 (L)	10	CH6 (L)
3	CH2 (H)	11	CH6 (H)
4	CH3 (L)	12	CH7 (L)
5	CH3 (H)	13	CH7 (H)
6	CH4 (L)	14	CH8 (L)
7	CH4 (H)	15	CH8 (H)

The request message from the SBC06 controller doesn't have a data field.

5.3.2 UCP Special Messages

The RTD card software handles two UCP special messages. One is a diagnostic message. The request message is same as to other I/O cards but the RTD diagnostics response has different content and size, as shown below.

The other UCP message is a UCP download message. The data field has the structure as shown in the **EEPROM Calibration Data** section in the table below. This section also lists the EEPROM offsets for the final storage of the download data.

Table 4. UCP Message Image

Byte	**Description**							
	Standard Diagnostic Response Header							
0								
1								
2-9								
10-25								
26-29								
30-31								
	Standard Diagnostic Area							
32	Diagnostics Status Byte							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
33	Spare							
34	Spare							
35	Failure mode jumper status							
36-39	Spare							
	EEPROM Calibration Data						EEPROM Offset	
40								
41								
42								
43-44								
45-46								
47-48								
49-50								
51-52								
53-54								
55-56								

Byte	Description	
57-58		
59-60		
61-62		
63-64		
65-66		
67-68		
69-70		
71-72		
73-74		
75-76		
77-78		
79-80		
81-82		
83		
84		
85		
86		
87		
Offset and Gain Data		
88		
89		
90		
91		
92		
93		
94-95		
96-97		
98-99		
100-101		
102-103		
104-105		
106-107		
108-109		
110-111		
112-113		
114-115		
116-117		
118-119		
120-121		
122-123		

Byte	Description
124-125	
126-127	
128-129	
130-131	
132-133	
Response Data	
134-135	
136-137	
138-139	
140-141	
142-143	
144-145	
146-147	
148-149	
150-153	
154-155	
156-157	
158-159	
160-161	
162-163	
164-165	
166-167	
168-169	
170-171	
172-173	
174-175	
176-177	
178-179	
180-181	
182-183	
184-185	

6. Module Implementation Descriptions

6.1 HARDWARE SCHEMATICS

The schematic for the HFC-AI8M card is in drawing 400443-01.

6.2 HARDWARE COMPONENTS – BILL OF MATERIALS

The part number of the HFC-AI8M card is 40044201 and its bill of materials is in file 40044201.txt.

6.3 SOFTWARE SOURCE CODE LISTING

Besides the common software sources for software common modules listed in the HFC-6000 I/O Card Module Detailed Design Specification, the HFC-AI8M card software also includes the following programs:

7. Design Safety

Refer to 700901-06 and MS901-000-02 for a discussion of safety consideration for the HFC-6000 I/O modules.

HF Controls

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NON-PROPRIETARY

HFC-6000 Product Line

HFC-AI4K
Module Detailed Design Specification

Pulse Input Board

DS901-000-12

Rev A

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Author	ANGELA HAN
Reviewer	JONATHON TAYLOR
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1.0 Introduction

The HFC-AI4K pulse input printed circuit board (PCB) provides four pulse input channels for an HFC-6000 control system. This assembly operates as a standard I/O board in an HFC-6000 control system. The four input channels of AI4K can be configured to either rate mode or accumulate mode. The rate mode is used to monitor input pulse rate and each input is reported as a standard 12-bit AI point. Accumulate mode is used to maintain a cumulative count of pulses being received and the values are reported as two consecutive AI points.

Descriptions and discussions of the architectural and design descriptions of standard HFC-6000 I/O boards, from an overview perspective, are provided in document MS901-000-02, HFC-6000 I/O Board Module Design Specification. Definitions of terms and acronyms are provided in HFC Common Glossary, document DS004-000-01.

Subsequent sections of this document provide detailed structure and design descriptions of the HFC-AI4K board, with concentration on the specific characteristics of an HFC-AI4K board. The design descriptions of the common software modules of I/O cards are covered in document DS901-000-02, HFC-6000 I/O Card Module Detailed Design Specification.

2.0 HFC-AI4K Functional Description

The HFC-AI4K board is controlled by an onboard 80C188EB microprocessor and provides an interface for up to four analog field inputs and four analog field outputs for an HFC-6000 control system. The AI4K board has onboard switches for manual configuration and status monitoring for each channel. It has an eight-character alphanumeric display to provide a visual indication of operating status.

It also has all standard functions of an HFC-6000 I/O board described in the HFC-6000 I/O Board Module Design Specification. Major functions performed by the 80C188EB microprocessor during normal operation are as follows:

- Controls reset and initialization functions.
- Supports channel configuration.
- Samples the pulse input data from each of the input channels.
- Stores the input data image for each channel in local memory.
- Respond to data transmissions from the HFC-6000 controller.

3.0 Hardware Detailed Design Specifications

3.1 Module Specification

- Environmental Extremes

Temperature:	0° to 55° C (operating)
	0° to 70° C (storage)
Relative Humidity:	5% to 95%, noncondensing

- Power Requirement
  External Power Supply: +24-vdc, 0.4 A maximum load.
  Interrogation Voltage: +48-vdc

- Onboard Clock Rate
  Microprocessor clock 22.1184 MHz

- Mounting Requirements: Mounts vertically in HFC-6000 board chassis.

- The HFC-AI8M PCB meets the requirements of seismic category I.

- Low memory provides 32K by 8-bits of nonvolatile RAM for temporary storage of message data being processed. Nonvolatile RAM is used to ensure that channel configuration parameters will be preserved when power is removed from the system.

- Pulse Input Channel Operating Limits

  Pulse rate: 0 Hz through 20 kHz
  Peak voltage level: 12-vdc to 150-vdc
  Peak input current: 10 ma (nominal)

3.2 ONBOARD POWER DISTRIBUTION

The board receives redundant 24-vdc power feeds from the backplane connector P1. The two power feeds are diode auctioneered, and an onboard voltage regulator converts the 24-vdc source power to 5-vdc power required for components on the HFC-AI4K board.

The board receives interrogation power (nominally 48-vdc) from the backplane. Proper field input wiring permit the user to configure one or more channels to operate with this interrogation power source. Overload protection is provided by a common line fuse, and an optocoupler permits the microprocessor to monitor status of the power line.

3.3 INTERRUPT PROCESSING

The 80C188EB microprocessor provides a modular core for processing interrupts and exception conditions. The chip architecture includes an NMI input port, a variety of internally generated interrupts, and ports for five maskable interrupts (INT0 through INT4). For this application, all of the maskable interrupt inputs are disabled. The NMI input is controlled by the watchdog timer.

3.4 MICROPROCESSOR PERIPHERAL PORTS

The microprocessor controls the following peripheral ports:

- Link address data input port

- Redundant serial port.
- Switch status input
- Counter status input
- Programmable counter I/O
- Display control
- Status input from each pulse input channel.

The link address input port, and the redundant serial port are common to all I/O board types, and are described in document DS901-000-02. Individual outputs from the programmable port P1 of the microprocessor control the chip enable signals for the six I/O ports

3.4.1 Counter Status Port

The board contains a separately addressable input port for reading the following status input signals:

- CT_EN1 – High state indicates that the counter function for input channels 1 and 2 is enabled.
- CT_EN2 – High state indicates that the counter function for input channels 3 and 4 is enabled.
- RATE0/ - High state indicates that rate mode is selected for input channels 1 and 2.
- RATE1/ - High state indicates that rate mode is selected for input channels 3 and 4.

When rate mode is selected for a particular pair of input channels, the microprocessor uses the CT_EN status input to determine when the sampling period is complete. If rate mode is disabled, the CT_EN status is not meaningful.

3.4.2 Port Addressing and Control

The hardware design of the HFC-AI4K card uses direct addressing to access the remaining hardware ports on the board as well as specific registers within the intelligent devices associated with those ports. When the microprocessor requires access to one of these ports, it sets programmable output P1.0 low and places the address for the desired port on address lines A12, A13, and A14. A demultiplexer decodes the address code to activate one of eight output chip select signals. These signals control access to the following I/O ports:

- Address code 000 is assigned to the onboard eight-character alphanumeric display. When this device is selected, address signals A00 through A05 are used to access internal data and control registers. The microprocessor can then read status data from the internal registers or transfer data to the device for display.

- Address code 001 is assigned to an onboard 82C54 interval counter, and address signals A00 and A01 control access to three eight-bit counters and one control register. The microprocessor can read the current value of a selected counter, set the operating mode for a selected counter, or set a selected counter to a starting value.

- Address code 010 is assigned to the control function for the four pulse input channels. When this code is selected, address signals A00, A01, and A02 are decoded to produce a single output signal (CLR0/, CLR1/, SET0, or SET1/). The CLR0/ output clears the counters for pulse input channels 1 and 2, and the SET0/ output signal enables the count function for these two channels to start. The CLR1/ and SET1/ signals control the corresponding functions for pulse input channels 3 and 4. These output signals are used to start the sampling interval during rate mode operation.

- Address code 011 is assigned to the switch input port. When this address is selected, the microprocessor can read the status of switches S1, S2, S3, and the rotary switch connected at J5. The status of the excitation voltage is also included with this input data byte. The software uses the switch inputs to control configuration of the pulse input channels and as well as the specific data sent to the onboard display.

Address codes 100 through 111 each enable access to a single 82C55A port controller, and address signals A00 and A01 control access to internal registers of the selected port controller. Each port controller is associated with one of the pulse input channels. An 82C55A port controller includes 24 I/O pins that can be programmed to operate in one of three operating modes. For the present application, all 24 I/O pins are programmed to receive input data from the two 12-bit counters for a particular pulse channel. The microprocessor can read the current count of one or both 12-bit counters by running consecutive read cycles to the internal registers and incrementing address signals A00 and A01 with each read.

3.4.3 Input Channel Configuration

Each input channel consists of a voltage biasing network with a simple RC low-pass filter, an optocoupler, a second low-pass filtering network, a signal conditioning network, and two cascaded 12-bit counters. The 24 output signals from the two counters are routed to one of the programmable port controllers, and a slide switch controls selection of either the accumulate or the rate mode of operation.

3.4.3.1 Input Signal Conditioning

The input network monitors digital pulse (nominally 48-vdc) input signals. These signals are applied across RC low-pass filters (34 kHz shoulder frequency) to the input of transistor switches. When no signal is present, the low-pass filter shunts high frequency noise to ground, and the transistor switch remains cut off. When a positive input is present, the transistor becomes forward biased and passes an output through the base-emitter junction. A Zener diode in the base circuit limits the output voltage to the TTL range upstream from the optocoupler.

The final stage of signal conditioning consists of a second low-pass filter, a voltage comparator configured as a high speed switch, and a NAND gate. The low-pass filter is configured in parallel with the input of the voltage comparator to block any residual signal noise that could produce invalid pulse inputs to the counters. However, because the shoulder frequency of this filter is relatively low (63 Hz to 63 kHz), it also distorts the input

waveform. In order to produce a signal having well defined leading and trailing edges, the output from the low-pass filter is connected to the non inverting input of the voltage comparator. The biasing network connected to the inverting input comparator controls the voltage level at which the device switches its output signal. This network is configured to switch from OFF to ON when the input signal increases above 3.33 volts, and it switches from ON to OFF when the signal decreases below 1.67 volts. The resulting output is connected to a NAND gate and controls the clock input to the first of the two 12-bit counters. The NAND gate inverts the signal so that the trailing edge of each pulse increments the count.

3.4.3.2 Pulse Channel Operation

Selection of rate mode operation for each pair of pulse input channels is controlled by a slide switch. When the slide switch for channels 1 and 2 is in the rate position, switch contacts produce the following control circuits:

- The CT_EN1 signal is NANDed with the input pulse train for channel 1 and channel 2. When the CT_EN1 signal is low, the NAND gate blocks the pulse input, and the counters stop incrementing.

- The CLR0/ signal is routed to the reset port of all four 12-bit counters for these two input channels.

- A high RATE0/ signal is routed to the counter status input port.

When the RATE0/ signal is high, the microprocessor selects tuning parameters for the rate mode from memory. The operator must enter these tuning parameters manually from the rotary switch and the three pushbutton switches during hardware configuration of the card. The tuning parameters control selection between 8-bit and 12-bit resolution, a preset count value, and the maximum pulse rate. The microprocessor controls rate mode operation by configuring the programmable counter for a sampling interval determined by the tuning parameters, and then it clears the 12-bit counters. Once the counters have been cleared, the microprocessor activates the SET1 output. This signal sets a latch that activates the CNT_EN1 output signal. While this signal is high, the interval counter is enabled, and the 12-bit counters increment with each pulse received from the field. When the sampling interval expires, the interval counter produces an output pulse that clears the latch, forcing the CNT_EN1 signal low. The low state of the CNT_EN1 signal blocks further input to the 12-bit counters and notifies the microprocessor that the sampling period is complete. The microprocessor then reads the accumulated count from the port controllers for channels 1 and 2.

When the slide switch for channels 1 and 2 is in the accumulate position, the RATE0/ signal assumes a low level, and the reset input to the 12-bit counters is disabled. While accumulate mode is enabled, all pulses received from the field pass to the clock input port of the first 12-bit counter. When this counter reaches full count, the high-to-low transition of the MSB increments the second 12-bit counter. While accumulate mode is enabled, the counters

continue incrementing, and the microprocessor reads the total 24-bit accumulated count at periodic intervals.

3.5 CONTROLS, JUMPERS, AND INDICATORS

The firmware determines the overall operating characteristics of the hardware on the HFC-AI4K board. The HFC-AI4K board includes the set of four LEDs and a RESET pushbutton common to all I/O board types (DS901-000-02). In addition, the board includes jumpers, switches, and onboard indicators. These devices and the functions that they control are as follows:

3.5.1 Switches

The HFC-AI4K pulse input board includes a set of switches that enable configuration of operating parameters.

S1 INC Actuating this switch when tuning mode is enabled increments the value of the tuning parameter currently being displayed.

S2 DEC Actuating this switch when tuning mode is enabled decrements the value of the tuning parameter currently being displayed.

S3 SEL Actuating this switch during normal operating mode displays the value of the indicated parameter. Actuating the SEL switch during tuning mode steps through the tuning parameters in sequence and then saves the new parameter in memory.

S4 ACCUMULATE/RATE two-position slide-switch selects either the accumulate or the rate modes of operation for input channels 1 and 2.

S5 ACCUMULATE/RATE two-position slide-switch selects either the accumulate or the rate modes of operation for input channels 3 and 4.

S6 Four-position DIP switch. Closing a particular switch position configures the corresponding channel for common mode operation. Opening a particular switch position configures the corresponding channel for isolated mode operation.

Inputs from a 17-position rotary switch (J5) control alphanumeric displays presented on U23 and programming functions of the board. The function defined for each switch position is defined in Table 1.

Table 3-1. Rotary Switch Functions

Position	Function
0	Display off
1	CHANNEL 1. Displays the current value for input channel 1 in either the accumulate or the rate mode of operation.
2	CHANNEL 2. Displays the current value for input channel 2 in either the accumulate or the rate mode of operation.
3	CHANNEL 3. Displays the current value for input channel 3 in either the accumulate or the rate mode of operation.
4	CHANNEL 4. Displays the current value for input channel 4 in either the accumulate or the rate mode of operation.
5	1 & 2 ACCUM/RATE. Displays the current operating mode selected for channels 1 and 2.
6	1 & 2 PRESCALE/RATE. When ACCUMULATE mode is selected for channels 1 and 2, the display indicates the number of pulses that must be received before the accumulator is incremented. When RATE mode is selected, the display indicates the counter resolution (8-bit or 12-bit) and maximum pulse rate selection.
7	3 & 4 ACCUM/RATE. Displays the current operating mode selected for channels 3 and 4.
8	3 & 4 PRESCALE/RATE. Presents the same display as switch position 6 for channels 3 and 4.
9	PRESET CH 1. Actuating the INC/DEC switches enables the user to enter a preset count value for channel 1. Actuating the SEL switch causes the board to display the SAVE TUN prompt. Actuating the SEL switch a second time saves this value in memory.
A	PRESET CH 2. Enables the same tuning function as switch position 9 for input channel 2.
B	PRESET CH 3. Enables the same tuning function as switch position 9 for input channel 3.
C	PRESET CH 4. Enables the same tuning function as switch position 9 for input channel 4.
D	1 & 2 ACCU/RATE. When ACCUMULATE mode is selected for channels 1 and 2, actuating the SEL switch enables the user enter a single prescaler value for the two channels. When RATE mode is selected, the user can enter two tuning parameters. The first time the SEL switch is actuated, the user can select between 8-bit and 12-bit (either 8B or 12B) counter resolution. Actuating the SEL switch again permits the user to select the maximum pulse rate (from 512 up to 20 K for 12-bit or from 50 to 10 K for 8-bit) for channels 1 and 2. Actuating the SEL switch again prompts the user to save the new tuning parameter in memory.
E	3 & 4 ACCU/RATE. Provides the same tuning function as switch position D for channels 3 and 4.
F	Functional test. Actuating the RESET switch and then the SEL switch causes the firmware to step through an internal diagnostic routine. This test displays the current operating mode and the values of the tuning parameters.

3.5.2 Jumpers

E58-E57 Function not currently defined.

E100-E101 Installed during calibration to disable both the NMI signal. When this jumper is removed, the D-latch U4-A activates a high NMI.

The channel input interfaces have four RC low-pass filters whose shoulder frequency is determined by a jumper strap. The jumper position typically installed at the factory selects a filter frequency of 1590 Hz. This filter frequency can be changed in the field as necessary to provide greater attenuation of signal noise. The input channels one through four jumper functions are defined in Table 2.

Table 3-2. **Jumper Configuration**

Input Channel 1
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: • E102-E103 1590 Hz • E104-E105 159 Hz • E106-E107 15.9 Hz • E108-E109 1.59 Hz
Input Channel 2
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: • E110-E111 1590 Hz • E112-E113 159 Hz • E114-E115 15.9 Hz • E116-E117 1.59 Hz
Input Channel 3
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: • E118-E119 1590 Hz • E120-E121 159 Hz • E122-E123 15.9 Hz • E124-E125 1.59 Hz
Input Channel 4
Selects an R-C low-pass filter for input channel 1 following four shoulder frequencies: • E126-E127 1590 Hz • E128-E129 159 Hz • E130-E131 15.9 Hz • E132-E133 1.59 Hz

3.5.3 Onboard Status Indicators

The HFC-AI4K provides an eight-character alphanumeric display (U23) that indicates current operating status of the board. During board configuration, the display operates in conjunction with switches S1 through S3 and J5 to enter and save operating parameters. During normal operation, the display operates with the programmable switch (J5) to provide a readout of current values for operating parameters.

3.6 CONFIGURATION PROCEDURE

3.6.1 Hardware Setup Requirements

Before a new HFC-AI4K card can be placed into a system, onboard jumpers and switches must be set to match the specific operating environment that will be required.

1. Each input interface can be configured for isolated or common mode operation. Set each position of DIP switch to select either common mode (switch closed) or isolated mode (switch open) for the corresponding input channel.

2. The input interfaces have four RC low-pass filters whose shoulder frequency is determined by jumper straps (Table 2). The jumper position typically installed at the factory selects a filter frequency of 62.8 kHz. This filter frequency can be changed in the field as necessary to provide greater attenuation of signal noise.

3. Position switches S4 and S5 to select either rate or accumulate mode for the input channels.

4. Insert the board into the selected I/O board slot and power up the chassis.

3.6.1.1 Point Type Configuration

The pulse board reports its data to the controller either as a 12-bit or a 24-bit image. In order to allocate adequate memory in the controller for the input data, the user must configure a pulse input card as an AI8 board type in the I/O configuration table. However, the specific channel and AI point assignments depend on the operating mode selected for each input channel indicated in Table 3-3.

Table 3-3. Input Channel Assignments

Input Channel	Rate Mode	Accumulate Mode
1	AI1	AI1 and AI2
2	AI2	AI3 and AI4
3	AI5	AI5 and AI6
4	AI6	AI7 and AI8

3.6.1.2 Input Channel Tuning Parameters

The operator must enter tuning parameters directly into the pulse board using rotary switch (J5) and pushbutton switches (S1 through S3) mounted on the edge of the board. The rotary switch permits the user to read the current values of the data in memory and to revise the tuning parameters for each channel. The following steps outline the process for updating the values of the tuning parameters in memory.

1. Rotary switch positions 9 through C enable the user to update a preset parameter for each channel. This value determines the starting count for the corresponding channel when that channel is in the accumulate mode. The preset value is not used for the rate mode.

2. Rotary switch positions D and E enable the user to enter either a prescaler value (accumulate mode) or a maximum input pulse rate (rate mode).

   - For accumulate mode, the firmware accepts a single prescaler value for each pair of input channels (1 and 2 or 3 and 4). When the prescaler value is either 0 or 1, the counter increments with each input pulse. For any number greater than 1, the prescaler value determines the number of input pulses that must be received before the counter is incremented by 1. Actuating the SEL switch after setting the desired prescaler value saves the tuning parameter in memory.

   - For rate mode, the firmware accepts a separate parameter for counter size and for maximum pulse rate. The first time the SEL switch is incremented, the default counter size is displayed. Actuating the UP or DN switch causes this value to toggle between 8B (8-bit) and 12B (12-bit). Actuating the SEL switch again causes the firmware to display the default maximum pulse rate of 512 Hz. The user can increment this parameter in steps from 512 Hz up to 20,000 Hz for 12 bit by actuating the UP switch. Range for 8 bit is from 50 HZ to 10 KHZ. Actuating the SEL switch after setting both values saves those parameters to memory.

3.7 HARDWARE CONNECTIONS

The HFC-AI4K board contains two board-edge connectors (P1 and P2) that mate with corresponding connectors on the HFC-6000 backplane. Connector P1 provides the electrical interface between the HFC-AC36 and the HFC-SBC06, and connector P2 provides the electrical interface with the external field hardware. Pin assignments for the P1 connector are identical for all I/O boards and are covered in document MS901-000-02. Pin assignments for the P2 connector are covered in Table 4.

Table 3-4. Connector P2 Pinout Summary

Pin	Mnemonic	Pin	Mnemonic
P2-A1		P2-C1	
P2-A3		P2-C3	
P2-A4		P2-C4	
P2-A6		P2-C6	
P2-A2 P2-C2 P2-A5 P2-C5			

4.0 Software Functional Design Descriptions

The design descriptions of the common software modules are provided in HFC-6000 I/O Board Module Detailed Design Specification. The following subsections provide detailed design descriptions for the software routines specific to the HFC-AI4K board.

4.1 Board Specific Modules

4.1.1 I/O Scan Module

If it is the first time that the software enters I/O Scan Module after power up or rest, the software runs a tuning test first to compare the mode parameters in memory with mode switch settings. If the parameters match the switch settings, the software can enter the Normal Operation stage for I/O scan. Otherwise, the software enters Tuning Mode to set up all configuration parameters. Refer to Section 4.1.2 for detailed Tuning Process. After tuning, the software go back to Initialization module to set up interrupt vectors and memory buffers before it re-enters the operating system main routine.

Every scan cycle, a Tuning Test is performed to check if the status of any mode switch has been changed. If there are changes in the mode switch status, the routine will set diagnostic error bit in the diagnostic byte, mark the current normal response as a bad response, and return without performing an I/O scan. Otherwise, the routine proceeds to perform an I/O scan.

It starts reading function switch and command switches and updates display if there are any changes. Refer to Section 4.1.3 for details about the display functions. It reads mode switches settings to decide how to scan the four input channels: Rate mode or Accumulate mode for every two channels, and scans them accordingly.

For rate mode, raw count reading is 8 bit data. If the channel is set for 12-bit rate mode, the raw count is left shift 4 bits to make itself 12 bit. For accumulate mode, the reading result is divided by prescaler setting. The final channel data will be stored in the Scan Working buffer and the routine returns to the operating system main routine.

4.1.2 Display Functions During Normal Operation

During normal operation, the rotary switch J5 can be used to display data currently stored in memory. Refer to position 0 to 8 in Table 3-1.

4.1.3 Tuning Process

During tuning mode operation, the software will go through different tuning steps depending on mode selected and the configuration parameters entered. Basically, the Tuning Process has the main functions listed in position 9 to F in Table 3-1. The Switches SEL, INC and DEC are used to make selections for configuration parameters.

4.1.4 Process Command Routine

For normal update requests, this routine has no function. For UCP diagnostics messages, it uses the common processing as described in DS002-000-02 to process UCP request received on the ICL.

4.2 Data Structure

4.2.1 Scan Data

The data field of the response message to the HFC-SBC06 controller contains AI images for eight channels as follows:

Table 4-1. AI Image

Byte	AI
0	CH1 (L)
1	CH1 (H)
2	CH2 (L)
3	CH2 (H)
4	CH3 (L)
5	CH3 (H)
6	CH4 (L)
7	CH4 (H)

The request message from the SBC06 controller doesn't have a data field.

4.2.2 Microprocessor Programmable Ports

The microprocessor uses certain programmable ports of P1 and P2 to control specific hardware functions. Table 8 lists the specific ports that are used, their function, their active state, and the mask required to implement that state in the program.

Table 4-2. Programmable Ports Used for the Card

Port	Description	Implementation
P1.0		
P1.1		
P1.3		
P1.7		
P2.1		
P2.3		
Port 1 Control		

Table 4-3. On-Board I/O Ports

Addr	On-Board I/O Ports
000	
001	
010	
011	
100-111	
1000	

4.2.3 Counter Status/Mode Port

Two-position slide-switches S4 and S5 control the operation mode of the input channels. S4 selects either the Accumulate or the Rate mode of operation for input channels 1 and 2. S5 selects either the Accumulate or the Rate mode for input channels 3 and 4.

The mode port permits the microprocessor to read the counter status input signals. These inputs indicate which modes are selected for the input channels.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Spare	Spare	Spare	Spare	RATE1	RATE0	CT_EN2	CT_EN1

CT_EN1 – High state indicates that the counter function for input channels 1 and 2 is enabled.
CT_EN2 – High state indicates that the counter function for input channels 3 and 4 is enabled.
RATE0/ - High state indicates that rate mode is selected for input channels 1 and 2.
RATE1/ - High state indicates that rate mode is selected for input channels 3 and 4.

When rate mode is selected for a particular pair of input channels, the CT_EN status input is used to determine when the sampling period is complete. If rate mode is disabled, the CT_EN status is not meaningful.

4.2.4 Input Channels

The AI4K card reports the data for its four pulse input channels as eight AI points to the SBC06 controller. The specific channel and AI point assignments depend on the operating mode of the card.

Table 4-4. AI Point Assignments to Pulse Input Channels

Mode 1&2	AI 1	AI 2	AI 3	AI 4	**Mode 3&4**	AI 5	AI 6	AI 7	AI 8
RATE	Ch. 1	Ch. 2	Spare	Spare	**RATE**	Ch. 3	Ch. 4	Spare	Spare
ACCU	Channel 1		Channel 2		**ACCU**	Channel 3		Channel 4	

4.2.5 Switch Input Port

Besides the two switches S4 and S5 mentioned above, the card includes four additional switches:

- J5 - 16-position rotary switch controls alphanumeric displays and programming functions of the card. This switch permits the operator to read the current values of the data in memory during normal operation and to enter or revise the configuration parameters for each channel while in tuning mode.
- S1 – INC. Actuating this switch during tuning increments the value of the tuning parameter currently being displayed.
- S2 - DEC. Actuating this switch during tuning decrements the value of the tuning parameter currently being displayed.
- S3 – SEL. Actuating this switch during normal operating mode displays the value of the indicated parameter. Actuating the SEL switch during tuning mode steps through the tuning parameters in sequence and then saves the new parameter in memory.

The switch input port provides the switch status input signals.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
J5 – Rotary Switch				S1-INC	S2-DEC	S3-SEL	Power

4.2.6 Alphanumeric Display Messages

The AI4K provides an eight-character alphanumeric display (U23) that indicates current operating status of the board. During board configuration, the display operates in conjunction with switches S1 through S3 and J5 to enter and save configuration parameters. During normal operation, the display operates with the J5 rotary switch to provide a read-out of current values for operating parameters.

The messages listed in the table below are designed for the display purpose of AI4K card.

Table 4-5. Display Messages

Message No	Display String
0	ROM ERR
8	RAM ERR
16	BRCH ERR
24	MATH ERR
32	LOG ERR
40	TUNE ERR
48	EPROM OK
56	SUM=
64	CPU ERR
72	CPU OK
80	J3 ON
88	REC. OK
96	REC. ERR
104	XMT 55?
112	XMT AA?
120	J4 ON?
128	COMPLETE
136	TUNE OK
144	TUNE?
152	1&2 RATE
160	3&4 RATE
168	1&2 ACCU
176	3&4 ACCU
184	8B
192	12B
200	‘ ‘
208	MOVE SW1
216	MOVE SW2
224	SAVE TUN
232	SAVED
240	HUNTING
248	‘ ‘

5.0 Module Implementation Descriptions

5.1 HARDWARE SCHEMATICS

The schematic for the HFC-AI4K card is in drawing 400448-01.

5.2 HARDWARE COMPONENTS – BILL OF MATERIALS

The part number of the HFC-AI4K card is 40044701 and its bill of materials is in file 40044701.txt.

5.3 SOFTWARE SOURCE CODE LISTING

Besides the common software sources for software common modules listed in the HFC-6000 I/O Card Module Detailed Design Specification, the HFC-AI4K card software also includes the following programs:

HF Controls

NON-PROPRIETARY

HF CONTROLS CONTROL SYSTEM

HFC-6000 Product Line Components

HFC-BPC01-08

Hardware Design Specification

DS901-000-14

Rev B

Effective Date 9/16/2005

Author/Title Eric Schirmer

Reviewer/Title Rob Lovgren

Approval/Title David Briner

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Revision History

Date	Revision	Author	Changes
01/09/04	A0	R Lovgren	Initial Draft: Based on HFC_BPC01-19 Design
06/29/05	B	E Schirmer	SCR869 – Added power pins to carry current

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1.0 GENERAL

The HFC-BPC01-08 card is a single-loop backplane designed for use in an HFC-6000 control system. Major features of the card are as follows:

- The card serves as a controller chassis backplane for an 8-inch card rack assembly.
- The HFC-BPC01-08 backplane provides two slots for HFC-SBC06 controllers, one slot for an HFC-DPM06, and a maximum of 3 HFC-6000 I/O cards.
- The backplane can receive operating power from redundant power cables that attach to a connector on the back of the card or from a power supply module installed in one of the I/O slots.
- The loop controller(s) plugged into this backplane communicates with I/O cards via redundant serial Intercommunication Link (ICL) traces on the backplane.
- Redundant ICL connectors on the rear of the backplane card enable connection of the ICL with an expansion card chassis.
- The structure of the HFC-6000 card chassis is designed to meet category 1 seismic requirements.

1.1 REFERENCES

400517-01	HFC-BPC01-08 Assembly Diagram
400518-01	HFC-BPC01-08 Schematic Diagram
700918-01	Single Loop Hoffman Cabinet
RS901-000-02	Single Loop Controller System Requirements Specification
RS901-000-01	HFC-6000 Product Line Specification

1.2 SPECIAL TERMS AND ABBREVIATIONS

DPM	Dual-Ported Memory
ICL	Intercommunication Link
I/O	Input/Output

2.0 SPECIFICATIONS

Environmental Extremes

Temperature	0° to 55° C (operating)
	0° to 70° C (storage)
Humidity	5% to 95% RH, noncondensing

Power	Power requirements are provided from a connector on the back of the backplane.
Operating Power	Redundant +24 vdc power at 8 A maximum combined load
Aux Power	Redundant 48 vdc (nominal) at 5 A maximum combined load.
Connectors	6 rows of DIN 41612-type connectors with 1.20-in. center-to-center spacing
Controller	DIN 120 Pin connector
DPM	DIN 120 Pin connector
I/O Cards	DIN 96 and 48 Pin connectors.

Card Slot Assignments

Controller	Slots 4 and 6 are reserved for the HFC-SBC06 controller.
DPM	Slot 5 is reserved for the HFC-DPM06.
I/O Cards	Slots 1 through 3 will accept HFC-6000 I/O cards in any combination.

3.0 CONTROLS AND INDICATORS

None

4.0 FUNCTIONAL DESCRIPTION

The HFC-BPC01-08 backplane is designed to mount on the rear flanges of a HFC-6000 Single Loop chassis assembly 700918-01. This version of the card chassis is designed for installation in a standard 8-inch equipment cabinet. The overall design of the chassis assembly was developed to meet category 1 seismic qualification requirements for structural integrity.

The HFC-BPC01-08 assembly provides connectors and electrical traces necessary for a single loop controller rack. The backplane accepts either a single HFC-6000 controller or a redundant pair of controllers, a dual-ported memory (DPM) card, and up to 3 I/O cards. Different backplane connectors prevent installation of I/O cards in the slots reserved for the controller and DPM hardware.

The backplane card may receive redundant +24-vdc power at a connector (PT) located on the left rear of the card, or a power module may be installed in one of the I/O card slots. In

either case, traces on the backplane route two sets of power supply lines (+24 V and AUX) to every card slot. Each card plugged into the backplane performs diode auctioneering and voltage level conversion to obtain the operating power needed for onboard hardware.

The communication link between the controller and I/O cards is provided by a redundant serial communication bus (ICL). For I/O cards installed in the controller chassis, the ICL consists of traces that run from the controller slots to each of the I/O card slots. Communication with I/O cards installed in an adjacent expansion card chassis is provided by a twisted pair ICL cable that mates with a connector on the back of the HFC-BPC01-08 assembly and extends to a corresponding connector on the back of the expansion backplane. Addressing for card slots in both the controller chassis and expansion chassis is provided by a 7-bit address code.

The HFC-BPC01-08 backplane has connectors for 6 cards equally spaced across the backplane. Connector P4 is reserved for controller CPU A, and connector P6 is reserved for CPU B. The DPM card is installed in P5 between the two controller cards. Each I/O card installed in the rack has two connectors (PnA and PnB) that mate with connectors mounted on the backplane. The PnA connectors mate with connectors P1A through P3A that are soldiered to the backplane. Traces on the backplane connect power, data, and control signals from the controller slots to the I/O card slots. The PnB connectors of each I/O card mate with connectors P1B through P3B that are attached to the backplane by means of mechanical mounting hardware. Connectors P1B through P3B provide the ability to connect external signals to each I/O card as required.

Conductor traces on the backplane connect the controller slot P4 (CPU A) and P6 (CPU B) to the DPM slot P5. If the control loop requires more than 3 I/O cards, connectors LNK_0, LNK_1, and XEN can be used to connect the ICL from this card chassis to the ICL traces of other HFC-6000 card racks. Each expansion rack can hold up to 14 I/O cards.

5.0 HARDWARE CONNECTIONS

Table 1 lists the pin assignments for the controller connectors P4 & P6. Table 2 lists the pin assignments for the DPM connector P5. Table 3 lists the pin assignments for the I/O card connectors (P1 through P3). Table 4 lists the pin assignments for the power module connector PT. Tables 5 and 6 list the pin assignments for connectors LNK_0 and LNK_1, respectively for the ICL. Table 7 lists the pin assignments for connector XEN.

Table 1. Controller (P4 & P6) Pin Assignments

Category	Pin	Mnemonic	Pin	Mnemonic
	A1 C1 B3		B1 A3 C3	
	A5 C5 B6		B5 A6 C6	
	A7 C7 A8 A9 C9 A10		B9 B10 B11 B12 B13 B14	
	A11 C11 A12 A13 C13 A14 A15 C15 A16 A17 C17 A18 A19 C19 A20		B15 B16 B17 B18 B19 B20 B21 B22 B23 B24 B25 B26 B27 B28 B29	
	A21 C21 A22 A23 C23 A24 A25 C25 A26 A27 C27 A28 A29 C29 A30 A31		B30 B31 B32 B33 B34 B35 B36	
	C31 A32 A33			

Table 1. Controller (P4 & P6) Pin Assignments (Cont)

Category	Pin	Mnemonic	Pin	Mnemonic
	C33 A34 A35 C35 A36 A37 C37 A38			
	A39 A40 B7 C39 B40		C8 B37 B8 C40 B39	

Table 2. DPM (P5) Pin Assignments

Category	Pin	Mnemonic	Pin	Mnemonic
	A1 C1 B3		B1 A3 C3	
	A4 C4		B4	
	A7 B7 A8 A9 B9 A10		C7 B8 C8 C9 B10 C10	
	A11 B11 A12 A13 B13 A14 A15 B15 A16 A17 B17 A18 A19 B19 A20		C11 B12 C12 C13 B14 C14 C15 B16 C16 C17 B18 C18 C19 B20 C20	

Table 2. DPM (P5) Pin Assignments (Cont)

Category	Pin	Mnemonic	Pin	Mnemonic
	A21 B21 A22 A23 B23 A24 A25 B25 A26 A27 B27 A28 A29 B29 A30 A31		C21 B22 C22 C23 B24 C24 C25 B26 C26 C27 B28 C28 C29 B30 C30 C31	
	B31 A32 A33		B32 C32 C33	
	B33 A34 A35 B35 A36 A37 B37 A38		B34 C34 C35 B36 C36 C37 B38 C38	
	A39 A40 A5 B39 A6		C39 C40 B5 B40 C6	

Table 3. Connector P1-P3 Pinout Summary

Category	Pin	Mnemonic	Pin	Mnemonic
	A1 C1 B2 A3 C3 B4 A5 C5 B12 A14 C14 B16 B15		B1 A2 C2 B3 A4 C4 B5 A12 C12 B14 A16 C16	
	A9 B8 C10		C9 A10 C8	
	A6 C6 B7 A8		B6 A7 C7	

Table 4. Power Bus Connector (PT)

Pin	Mnemonic	Description
1		
2		
3		
4		
5		
6		

Table 5. Link 0 ICL Connector (LNK_0)

Pin	Mnemonic	Description
1		
2		
3		
4		
5		
6		

Table 6. Link 1 ICL Connector (LNK_1)

Pin	Mnemonic	Description
1		
2		
3		
4		
5		
6		

Table 7. Com Link Enable Connector (XEN)

Pin	Description
1	
2	
3	
4	
5	
6	

HF Controls

HF Controls Corporation

HFC-6000 Product Line

HFC-SBC06-DPM06 Boards
Module Design Specification

System Controller

MS901-000-01

Rev C

NON-PROPRIETARY

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Author/Title	J. Taylor
Reviewer/Title	J. Stevens
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1. Introduction

The HFC-6000 distributed control system provides plant monitoring and control capabilities, with monitoring and control responsibilities spread over multiple remote control units. The HFC-SBC06 System Controller is the primary board used for implementing plant control functions. This HFC-SBC06-DPM06 Module Design Specification describes the HFC-SBC06 System Controller board and HFC-DPM06 Dual Ported Memory board.

As shown in Figure 1, the HFC-SBC06 System Controller board is positioned in the HFC-6000 system hierarchy between the Operator Station(s), which provides the direct Human Machine Interface to the plant operators, and the I/O boards which provide the signal-level interface to the equipment and devices in the plant.

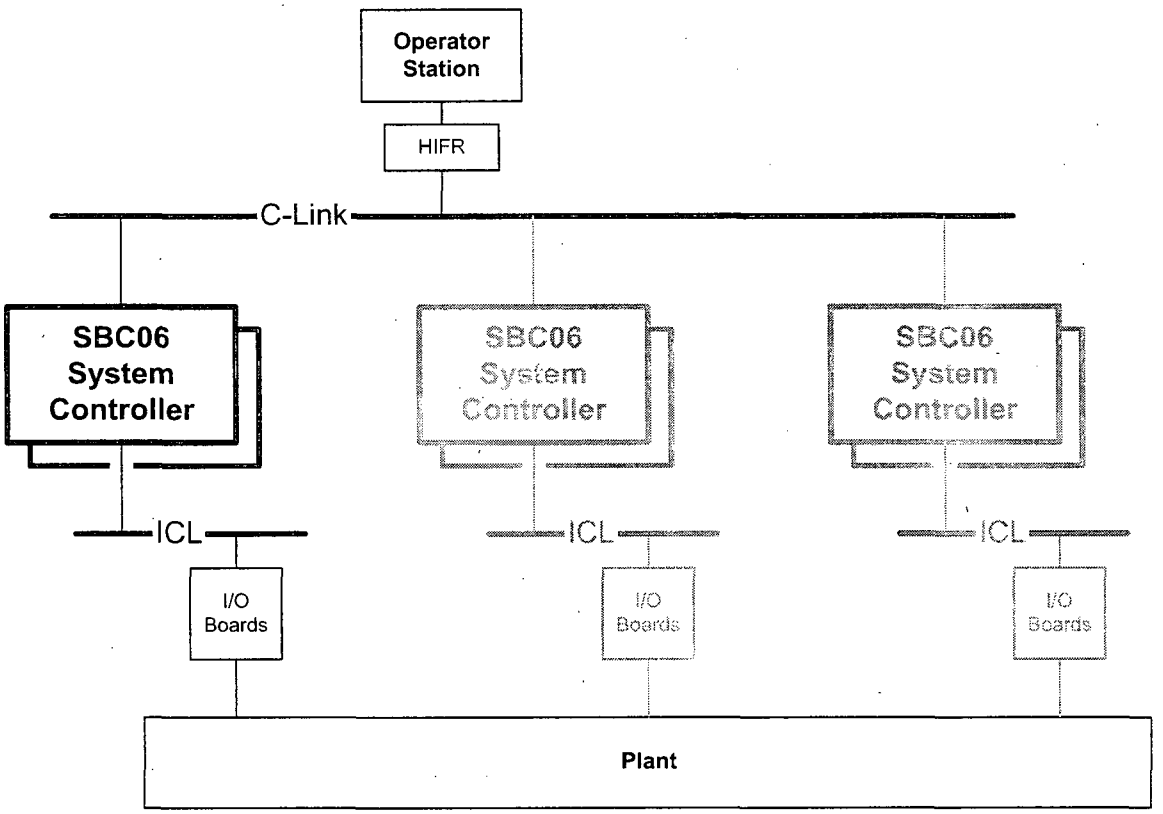

Figure 1. HFC-6000 System Hierarchy

Descriptions of the functional requirements of the HFC-SBC06 System Controller board and HFC-DPM06 board, from an external perspective, are provided in the HFC-6000 Product Line Requirements Specification, RS901-000-01. The design of the HFC-SBC06 and HFC-DPM06

also complies with the detailed requirements spelled out in 700901-04, 700901-05, and RS901-000-37.

The purpose of this document is to describe the operation and functions of the HFC-SBC06 and HFC-DPM06 boards. The discussion of the operation and function of the HFC-SBC06 and HFC-DPM06 will be presented using architectural, design, and implementation information.

Subsequent sections of this document provide architectural and design descriptions of the HFC-SBC06 board. Lower level descriptions of the HFC-SBC06 and HFC-DPM06 are contained in the HFC-SBC06-DPM06 System Controller Module Detailed Design Specification, DS901-000-01. The major functions performed by the HFC-SBC06 and HFC-DPM06 are listed in the next section which contains brief descriptions of the functions and how the HFC-SBC06 or HFC-DPM06 performs the functions.

2. Functional Description

The functions described in this section are the major functions performed by the HFC-SBC06 System Controller. The functional descriptions are presented so as to provide a context for understanding the operation of the HFC-SBC06 and a description of how the functions performed by the HFC-SBC06 System Controller work within the overall architecture of the HFC-6000 distributed control system.

The major functions performed by the HFC-SBC06 System Controller are:

- Communication with other system controllers and workstation PCs connected to the same redundant C-Link (Communication Link), an HFC proprietary network; Broadcasting plant status information;

- Communication with modules connected to the same ICL (Intercommunication Link), another HFC proprietary network; Collecting plant status information and sending plant operation commands;

- Redundant controller operation, System Controller failure detection, failover of the control function to the Secondary System Controller on failure of the Primary System Controller, and maintenance failover.

- Execution of application control programs for the specific control logic;

The following sections supply descriptions of the HFC-SBC06 functional requirements and identify aspects of the HFC-SBC06 that perform functions satisfying the requirements.

2.1 External Communication

Two communication interfaces connect the HFC-SBC06 to other boards and devices in the HFC-6000 system. Two identical 10BaseT interfaces connect the HFC-SBC06 to the redundant fiber optic Communication Link (C-Link) network, an HFC proprietary Ethernet-based network that the HFC-SBC06 uses to transfer data to and from the Operator Stations. Typical data transfers between the Operator Station and a System Controller are operator commands from an Operating Station to the System Controller and plant operation data to the Operator Station. The HFC-SBC06 also uses the C-Link to broadcast its status to other remotes attached to the C-Link.

The other HFC-SBC06 communication interface connects the HFC-SBC06 to the Intercommunication Link (ICL), which is an RS-485 serial network connecting the HFC-SBC06 to its I/O boards. Each HFC-SBC06 has two serial channels (ICL0 and ICL1) with each connecting to different I/O boards. Each serial channel can be linked to up to 32 I/O boards. Input values from plant field devices and output values to plant actuators are transferred between the HFC-SBC06 and I/O boards over the ICL serial network. The ICL network implements a master/slave communication protocol. Only the master can initiate communication, and the slave devices only respond to the master's poll. HFC-SBC06 serves as the master for all communication transfers with its configured ICL stations. Each I/O board operates as a slave node on the ICL network. The HFC-SBC06 polls each configured slave device at regular intervals, and the slave devices receive operation commands in the communication messages and respond with plant status information. Although each HFC-SBC06 board has two physical serial channels connected to different I/O boards, these two physical channels are on one logical link under the ICL protocol, either ICL A or ICL B for the I/O boards. Therefore, each ICL can be linked to up to 64 I/O boards.

Refer to DS002-000-01, C-Link Protocol Component Design Specification, and DS002-000-02, ICL Protocol Component Design Specification for details.

2.2 Redundant System Controllers

The HFC-SBC06 System Controller board is designed to operate in a redundant controller configuration. As shown in Figure 2, a redundant configuration consists of two System Controller boards (HFC-SBC06 A and HFC-SBC06 B) and a HFC-DPM06 dual ported memory board with the DPM06 board installed in between of the two SBC06 boards. Each HFC-SBC06 board in the redundant pair operates in one of two different modes: one board operates in a Primary controller mode, and the other board operates in a Secondary controller mode. Controller mode operation is determined at controller board start-up, with the first HFC-SBC06 to complete its initialization routine becoming the Primary, and the other HFC-SBC06 board defaults to Secondary controller mode.

Each HFC-SBC06 in a redundant pair is connected to redundant C-Link networks for communication with the Operating Station and one of two ICL serial networks that provides communication between the HFC-SBC06 and to each of its I/O boards. Each I/O board connects

with two system controllers via its dual serial ports as shown in Figure 2. The mode (Primary or Secondary) in which the HFC-SBC06 is operating determines how the HFC-SBC06 will use C-Link (Ethernet) and ICL (serial) networks.

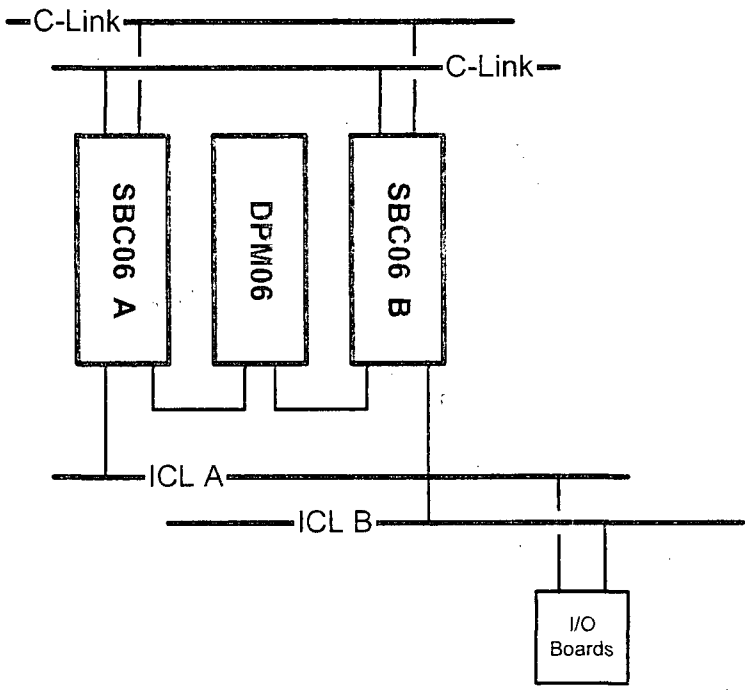

Figure 2. Redundant HFC-SBC06 Boards with DPM06 Board

During redundant operation, the Primary controller periodically copies application and system status data to dual ported memory (DPM) contained on the DPM06 board. The Secondary controller, on the other hand, periodically validates the status data in the DPM and updates its own record of status data if the data is valid. This DPM Transferring Mechanism keeps the secondary controller updated with a current copy of the primary running status and ensures a smooth transition from one controller to the other in the case of failover. During a failover event when control responsibility switches from the Primary to the Secondary, the Secondary uses the most recent application and system status data as an initial state for starting its control of the system. Starting with an initial state that is one second old or less minimizes disturbances to the plant induced by the controller switch over, and prevents potentially hazardous bumping caused by transfer of control. After switch over is complete, the Secondary, which is now the controlling the plant, switches to operation in the Primary control mode. Additional discussion of the failover mechanism is listed DS001-000-08, Failover Mechanism Component Design Specification.

A Maintenance Failover function is supported to perform regular check on the working status of the secondary controller to make sure it will be able to take over the control when the primary controller fails. A pushbutton on the HFC-DPM06 allows failover to be triggered manually.

As shown in Figure 3, the ICL network for a redundant controller configuration includes four physical serial channels for the redundant controllers: ICL A includes ICL A0 and ICL A1 for controller A; ICL B includes ICL B0 and ICL B1 for controller B. A single controller can have up to 64 I/O boards under its control.

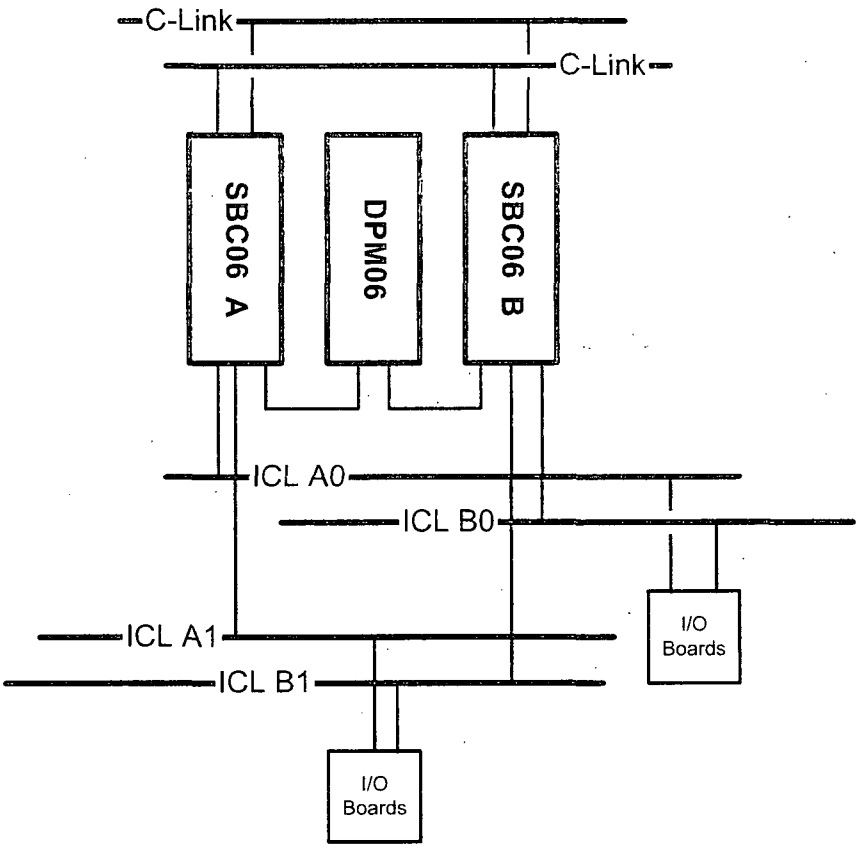

Figure 3. ICL Network for Redundant Controller Configuration

The HFC-SBC06 board may also be configured as a non-redundant System Controller. In a non-redundant of configuration, a single HFC-SBC06 is installed in slot 12 or 14 of a 19-inch HFC-6000 controller rack, and a DPM06 is installed in slot 13. (If the system uses 23-inch racks, the controller may be in slot 16 or 18, and the DPM 06 must be installed in slot 17.) Configuration switches located on the front edge of the DPM06 board are used to setup a number of system configuration parameters. The HFC-SBC06 must access a DPM06 to read the configuration settings as part of its initialization process.

Another difference between a redundant and non-redundant configuration is that a non-redundant HFC-SBC06 configuration only supports a non-redundant ICL network, as shown in Figure 4 instead of the redundant ICL network shown in Figure 3.

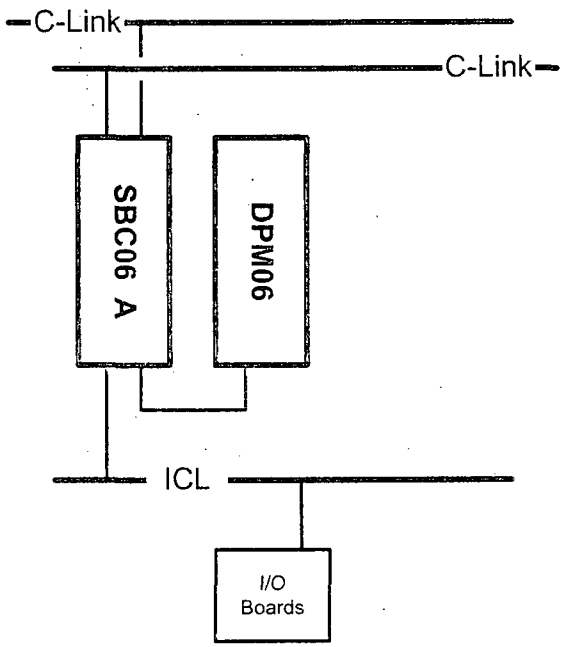

Figure 4. Non-Redundant HFC-SBC06 Board and DPM06 Board

2.3 Execution of Application Programs

The primary function of the HFC-SBC06 System Controller board is to provide control of the plant system actuators based upon the values of system inputs collected from plant field sensors. Control logics, such as arithmetic calculations and logical operations, operate upon field input values to provide control output values that drive plant actuators, operator status displays, and alarm indicators. These control logics are defined in an Application Program, which is installed in the PROM or flash memory in the HFC-SBC06 System Controller. It is transferred to the RAM during power up initialization, and the program is executed during operation of the controller.

Refer to DS001-000-002, Equation Interpreter Component Design Specification, and DS001-000-003, CQ4 Blocks Component Design Specification, for detailed descriptions of control logic algorithms. Refer to UG004-000-01, EWS User's Guide for detailed information about the structure of application program code.

3. Module Architecture

The architecture and design of the HFC-SBC06 board is based upon a partitioning of the module functions between three separate microprocessor sections: the SYS microprocessor section, the ICL microprocessor section, and the CPC microprocessor section. Each microprocessor section is dedicated to a specific set of functional responsibilities, with the SYS processor being the main

processor or system processor for the whole controller and the other two processors being subordinate processors.

The three independent microprocessors uses Public Memory to communicate and coordinate their individual operations. Public Memory is a shared onboard memory (RAM) section that may be accessed by the three microprocessors over a Shared Bus. As shown in Figure 5, the three microprocessors connect to the Public Memory address and data bus (Shared Bus) on the board, with each microprocessor's access to Public Memory controlled by a bus arbitration circuit. Public Memory contains data that is shared by the microprocessors and data that must be transferred between the microprocessors.

In addition to available use of Public Memory, each microprocessor is configured with Private Memory with separate PROM, Flash, and RAM sections. System firmware codes are installed in the PROM or flash memory. Private Memory is accessible only to the microprocessor in that circuit section.

The CPC Section has two RJ45 10BASET ports for the redundant C-Link interface. The ICL Section includes two RS-485 communication links for the ICL.

There is an onboard Sanity circuit for detection of controller failure. The SANE status and PRI (Primary) status signals from the Sanity circuit are routed to the Failover circuit on the HFC-DPM06 board. The Failover circuit supports failover on failure of Primary controller and maintenance failover.

There is a dual-ported memory on the HFC-DPM06 board which is accessible to both the primary and secondary controllers. The three processors connect to the DPM address and data bus, with each processor's access to the DPM controlled by a bus arbitration circuit. Software arrangements coordinate Read and Write to the DPM by the primary and secondary controllers to avoid conflicts or corrupted data.

The System Controller provides Sequence of Events (SOE) master clock with 1 ms resolution over 24 consecutive hours of operation.

Both the HFC-SBC06 and HFC-DPM06 board have DIP switches for controller configuration. These switch settings are accessible to the SYS processor on board.

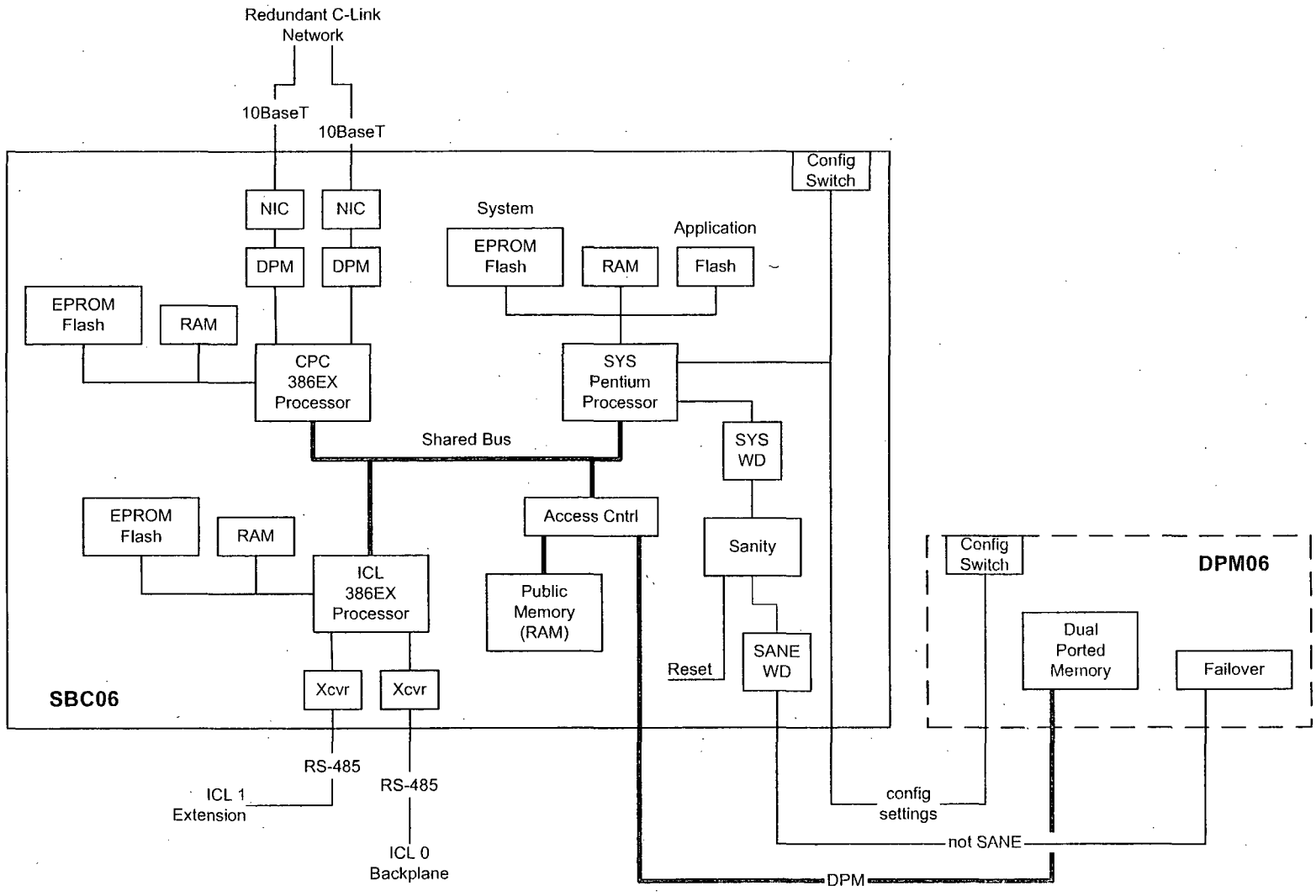

Figure 5. HFC-SBC06 / DPM06 Module Architectures

3.1 Memory Mapping Structure

The individual memory address spaces for the three microprocessors on the HFC-SBC06 board have the same basic structure, with each address space including both Public and Private Memory areas. As shown in Figure 6, the top range of the address space (PROM / Flash) contains executable code. The microprocessor data area (RAM) is mapped to the bottom range of the address space. Public Memory is mapped to the center range of the microprocessor address space.

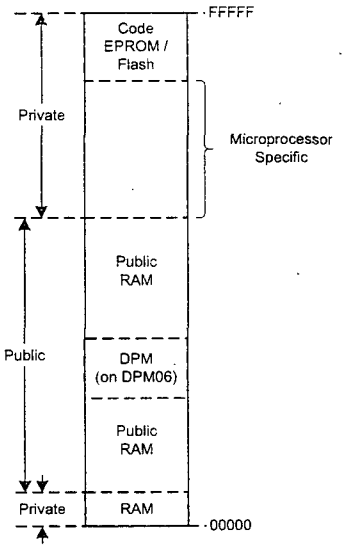

Figure 6. Microprocessor Address Space

The DPM memory area located in Public Memory address space shown in Figure 6 is dual ported memory residing on the DPM06 board installed in the slot next to the HFC-SBC06 board. DPM memory is used by two HFC-SBC06 boards operating as a redundant pair for transferring data between Primary and Secondary.

The Private Memory area shown in Figure 6 labeled **Microprocessor Specific** has different uses within the three processor sections. In the SYS processor section, this area of Private Memory contains the Application Program instructions. In the CPC processor section, this area is mapped to a dual ported memory part that is used to interface the CPC microprocessor to the Ethernet controllers managing low-level communication functions on the C-Link network. In the ICL processor section, this area of Private Memory is not used and contains no RAM, PROM, or Flash memory.

3.2 *Public Memory Data*

The design of the HFC-SBC06 board uses a Public Memory Data area to allow the three microprocessors to share and transfer data during operation. Public Memory contains a number of data stores used by the microprocessors with the main data stores holding I/O and UCP message data.

The I/O data stores hold data that is accessed and shared by all three microprocessors. As an example of shared data, Public Memory contains three main shared data areas: IO Point Image, Internal Point Image, and DDB Image. These data image areas are used by all three processors on the System Controller board. The data stores shown in Figure 7 are three of the main data items in Public Memory, and these data stores will be encountered a number times during discussion concerning aspects of the software architectures of the three microprocessor sections on the HFC-SBC06 System Controller board.

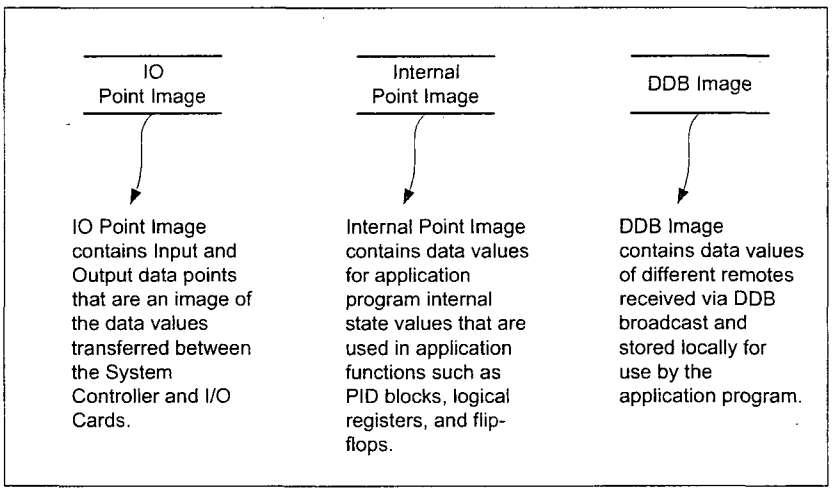

Figure 7. Public Memory Data Stores

The IO Point Image data area holds Input and Output data values that are accessed by:

- the SYS processor during execution of the application program. The SYS processor uses the input data values as the inputs to the application programs and results of execution will be used to update the output data values.
- the ICL processor for storing Input values read from the I/O boards and retrieving Output values that need to be sent to the I/O boards over the ICL serial link;
- the CPC processor for DDB data broadcasts on the C-Link network.

The UCP message data stores hold UCP messages that need to be transferred between the microprocessors. UCP messages are point-to-point communication messages used in HFC control systems. The next section, Section 3.3 provides more descriptions of UCP messages. The UCP messages stored in the Public Memory are mainly operator commands or inquiries from operator workstations and responses from the SBC06 System Controller to the operator workstations. A UCP message is normally processed in the following sequences:

- The CPC processor receives a UCP message from the C-Link and stores it in the Public Memory if the message is not addressed to itself
- The SYS processor retrieves any UCP message addressed to itself from the Public Memory, executes the command and stores the UCP response messages in the Public Memory.
- The ICL processor retrieves any UCP message addressed to itself or ICL I/O boards in the Public Memory, and stores the UCP response message in the Public Memory
- The CPC processor retrieves any UCP response message from the Public Memory and transmits it to the C-Link

3.3 Remote Communication Architecture

Remote communication is used when an HFC-SBC06 System Controller exchanges data with another System Controller, Operator Station, or Engineering Workstation. The HFC-SBC06 supports remote communication over the Communication Link (C-Link) network and provides dual network ports for connection to a redundant C-Link network. Two protocols are used to carry data over the C-Link network. These two protocols are:

- Dynamic Database (DDB) protocol. Refer to DS002-000-001, C-Link Protocol Component Design Specification for detailed descriptions of DDB protocol.
- Universal Communication Packet (UCP) protocol. Refer to DS002-000-003, UCP Protocol Component Design Specification for detailed descriptions of UCP protocol.

The use of one protocol versus the other depends upon whether the data being carried is information that is transferred on a regularly scheduled basis or whether the information is being transferred due to a system event. The DDB protocol is designed to carry data traffic occurring on a regularly scheduled basis, and the UCP protocol is designed to carry a periodic traffic such as operator commands and controller status inquiries.

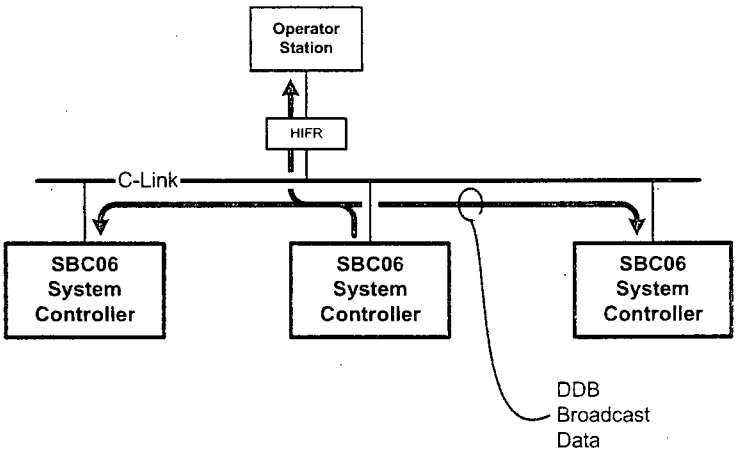

Figure 8. DDB Broadcast Data Paths

The Dynamic Database protocol is a broadcast protocol in which a transmitting node on the C-Link network broadcasts data packets to all nodes on the network. As shown in Figure 8, one network node, the HFC-SBC06 System Controller in center, is broadcasting DDB data while all other nodes are receiving DDB data. The DDB protocol is the method used for transferring system operating data, such as field input values, actuator output values, and control state values, among System Controllers and Operator Workstations. In the HFC-6000 system, DDB data is broadcast from each System Controller in a round-robin sequence.

The Universal Communication Packet protocol is designed as a point-to-point protocol for transferring data that is not sent on a regular basis during system operation.

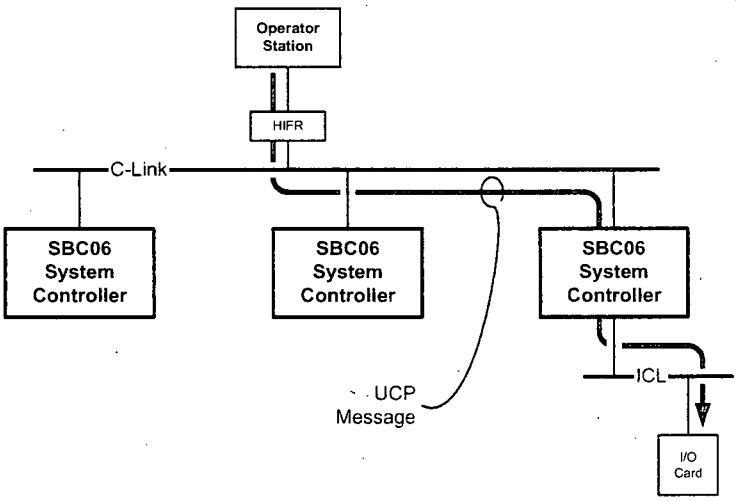

Figure 9. UCP Point-to-Point Message Path

An example of a typical UCP message is an operator query for the status of a device in the plant. As shown in Figure 9, the UCP message originates at the Operator Station and travels to the I/O board connected to the plant device for which the status is being queried.

The complete transaction for this UCP example message actually would consist of two UCP messages. The first message in the transaction would be a UCP request message sent from the Operator Station to the I/O board responsible for the operation of the device. The point-to-point message would be a request for the value control state. The second UCP message in the transaction would also be a UCP response message providing the device control state and going point-to-point from the I/O board to the Operator Station.

Network transmission control for the C-Link network uses a token passing mechanism. In a token passing transmission control scheme, a single node within the network holds the token, and the node with the token is the only one that is allowed to **transmit** data on the C-Link network at a given point in time. While the transmitting node has the token, all other nodes on the network can only receive data. Error detecting functions and mechanisms use network error timers running at each node that are designed to detect token passing errors such as "Lost Token", "Fail to Pass Token", "Fail to Claim Token", and "Token Claim Collision".

Remote communication for the HFC-SBC06 is handled by the CPC processor. However, data for remote communication may be produced or consumed by any of the three microprocessors on the HFC-SBC06 board. The next two sections describe the CPC processors handling of the data sent and received via remote communication.

3.3.1 HFC-SBC06 Handling of DDB Data

As explained previously, the DDB protocol uses a broadcast of data for transferring information from one node to all other nodes on the network. Each HFC-SBC06 System Controller on the network must be able to both broadcast DDB data and receive DDB data. The specific information that the HFC-SBC06 broadcasts when it has possession of the token is specified in the DDB Broadcast Table. The actual data that is broadcast by the HFC-SBC06 is contained in the IO Point Image and Internal Point Image data stores, as shown in Figure 10. During a DDB broadcast, the CPC processor uses the Broadcast table to determine which data in the two Point Image data stores to select and broadcast on the C-Link.

Not all DDB data broadcast on the C-Link will typically be needed by an HFC-SBC06 for performing its required operations. When the HFC-SBC06 is receiving DDB data from the C-Link, a filter is applied to the data, and only the DDB data specified by the filter is processed CPC processor. As shown in Figure 10, the DDB Filter Table, which lists the DDB data that is needed by the particular HFC-SBC06, is used by the CPC processor to determine which incoming DDB data is to be processed and stored by the CPC processor in the DDB Image data store. DDB data from the C-Link that is **not** listed in the Filter is skipped by the CPC processor.

The I/O Scan Table lists all the configured I/O boards on the ICL for the SBC06 and board information, such as type of I/O points on board, number of points, and assigned point numbers.

The ICL processor uses the I/O Scan Table to determine which I/O board to scan, how to scan it, and where the I/O point values should be stored in the Public Memory.

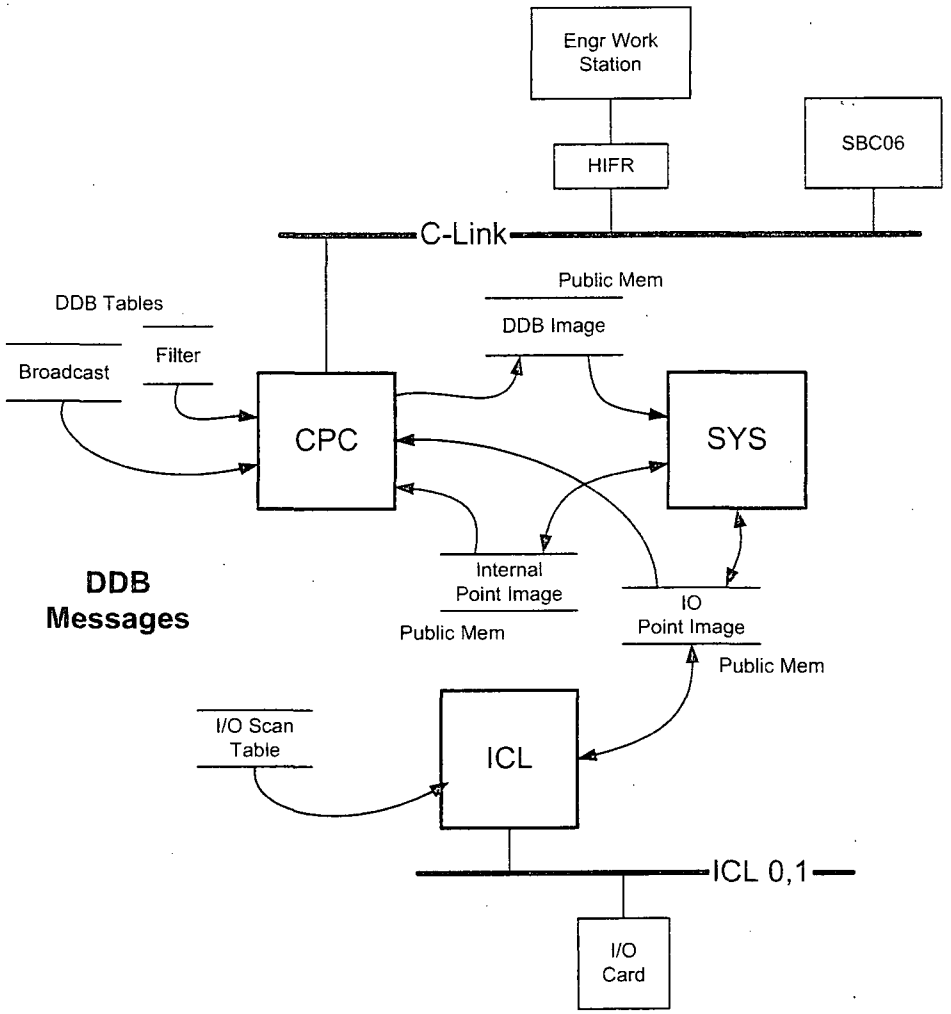

Figure 10. Broadcasting and Filtering of DDB Data

3.3.2 HFC-SBC06 Handling of UCP Messages

UCP messages are designed to be transferred on a point-to-point basis, and as such, any UCP message received by the HFC-SBC06 will either end up being processed by a task running on one of the three HFC-SBC06 processors, or will end up being passed to an I/O board attached to the HFC-SBC06 via the ICL serial network. UCP messages are received from the C-Link network by the CPC processor, which processes the message header to determine where to post the message. If the UCP message is destined for a task running on the CPC processor, the message is stored in a CPC data store for processing by the specific CPC task.

If the UCP message is not addressed to a CPC task, the message will be stored in message data store in Public Memory. As shown in Figure 11, a UCP message addressed to a task running on the SYS processor is stored in the SYS message data store in Public Memory. A UCP message that is addressed to a task running on the ICL processor, or a UCP message addressed to an I/O board, is stored in the ICL message data store in Public Memory.

UCP messages sent from a task running on either the SYS processor or the ICL processor, or a UCP response message received from an I/O board attached to the HFC-SBC06, is stored in respective message data store (SYS messages or ICL messages) in Public Memory.

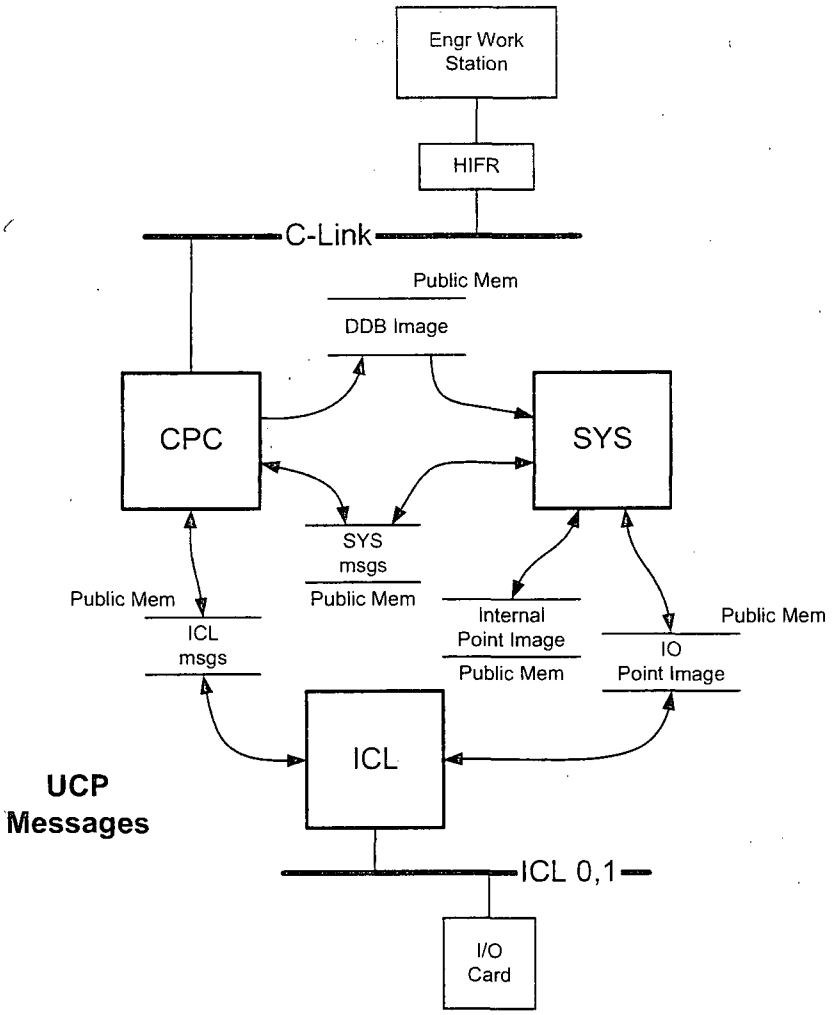

Figure 11. UCP Message Processing

A message event mechanism, with events passed between processors using Public Memory, is used by a processor in the HFC-SBC06 to notify another processor in the HFC-SBC06 that a UCP message has been placed in its respective message data store. Refer to DS001-000-001,

Operating System Component Design Specification for details of the UCP message event mechanism.

3.4 SYS Processor Section

The SYS processor section is based on an Intel Pentium processor. Figure 12 shows the architecture of the SYS Processor section. The major functions of the SYS Processor section are as follows:

- Execution of application programs on I/O point images
- Coordination of the other two processors on board
- Monitoring overall controller status

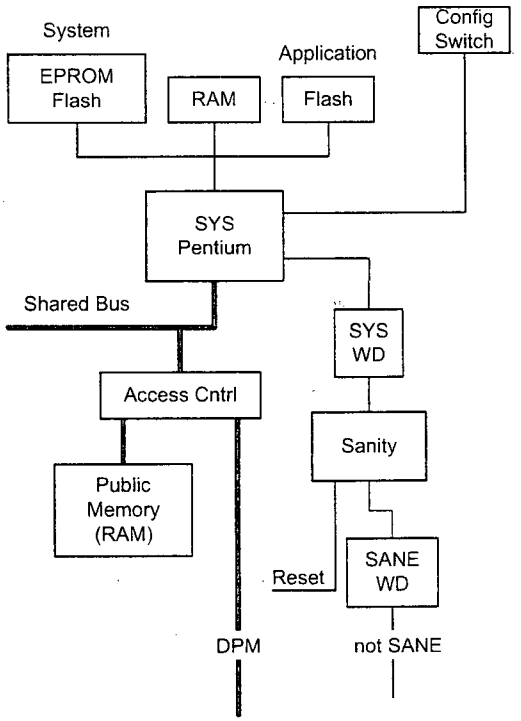

Figure 12. System Processor Architecture

The SYS processor has access to the flash memory that has application programs installed. The application program consists of a sequential set of instructions that are executed by the Equation Interpreter software task. The Equation Interpreter processes the instructions from the application program to generate digital and analog output values using input values currently in

memory. The descriptions of architecture, interface and design of Equation Interpreter component are provided in DS001-000-002, Equation Interpreter Component Design Specification.

The application program in the SYS processor's flash memory also contains DDB Filter Table, DDB Broadcast Table, and I/O Scan Table. During controller initialization, the SYS processor copies these tables from its flash memory to the Public Memory for the use by the CPC Processor and the ICL Processor.

On the HFC-SBC06 board and HFC-DPM06 board, there are DIP switches for controller configuration. The SYS processor reads the switch settings and stores the configuration data in the Public Memory.

As the system processor, the SYS Processor performs initialization for the Public Memory during controller initialization. It configures the Public Memory according to the predefined structure. After the Public Memory Initialization is done, the SYS processor sets a READY flag in the Public Memory to inform the other two subordinate processors that the Public Memory is ready for use.

The other two subordinate processors report to the SYS Processor after they finish initialization successfully and wait for the SYS processor's indication as when to start operating. The SYS Processor, after verifying that all the processors on board have finished initialization, sets a System_Go flag in the public memory, enabling normal operation to begin. The subordinate processors start normal operation after the System_Go flag is set. Thus, the whole controller enters normal operation mode.

Each of the subordinate processor has a "Mailbox" in the Public Memory to report the status of the processor. During normal operation, the subordinate processor periodically updates its mailbox by loading a preset value into it. As a parallel process, the SYS processor monitors subordinate processor running status by decrementing the mailbox at preprogrammed intervals. The setting of mailbox preset value and mailbox decrementing amount and intervals determine how soon a failure of the subordinate processor can be detected.

The SYS processor also maintains the system watchdog timer (a MicroMonitor chip) by strobing the timer periodically. If the SYS processor fails to strobe the watchdog timer, the timer will time out and trigger a failover if the controller is in Primary mode. Refer to details of controller failure detection and failover mechanism in Section 3.7.

The SYS processor maintains a controller status flag in the Public Memory. In case of a status change, the SYS processor updates the controller status flag, so that the two subordinate processors will change their running mode from primary to secondary, or vice versa. This mechanism ensures that the whole controller operates in the same mode: either primary or secondary.

The SYS Processor is also responsible for transferring system status data between the Public Memory and the DPM periodically. If the SYS Processor is in primary mode, it transfers data from the Public Memory to the DPM. If the SYS Processor is in secondary mode, it transfers data from the DPM to the Public Memory. This mechanism keeps the secondary controller updated with system status data and ensures a smooth transition of control in case of a failover from primary controller to secondary controller.

3.4.1 SYS Processor Software Architecture

The SYS Processor software consists of the following routines:

- Initialization
  - Power up/Reset Initialization
  - Controller Configuration
  - Processor Specific Initialization
    - Memory Initialization for Public Memory
    - Task Initialization
- Operating System Component
- Processor Specific Tasks
  - System Tasks
    - DBM Tasks and System Database Manager
    - Equalization Task for DPM
    - Processor Status Monitor Task
  - Equation Applications
    - Equation Interpreter Task
    - Logic Algorithms
    - Analog Processing Algorithms - CQ4 Block Algorithms
  - Timer Interrupt Service Routines
- UCP Utility Component
  - UCP Memory Manager
  - Network Manager for Path Element
  - Network Message Routine
  - UCP Message Handling Tasks

The SYS Processor software is designed based on an operating system common to all processors on the HFC-SBC06 board and a set of configurable tasks that will be run by the operating system. Figure 13 provides an overview of the SYS Processor Software Architecture. The Operating System is mainly a task scheduler, which executes the configured tasks one after another according to a task control block (TCB) list.

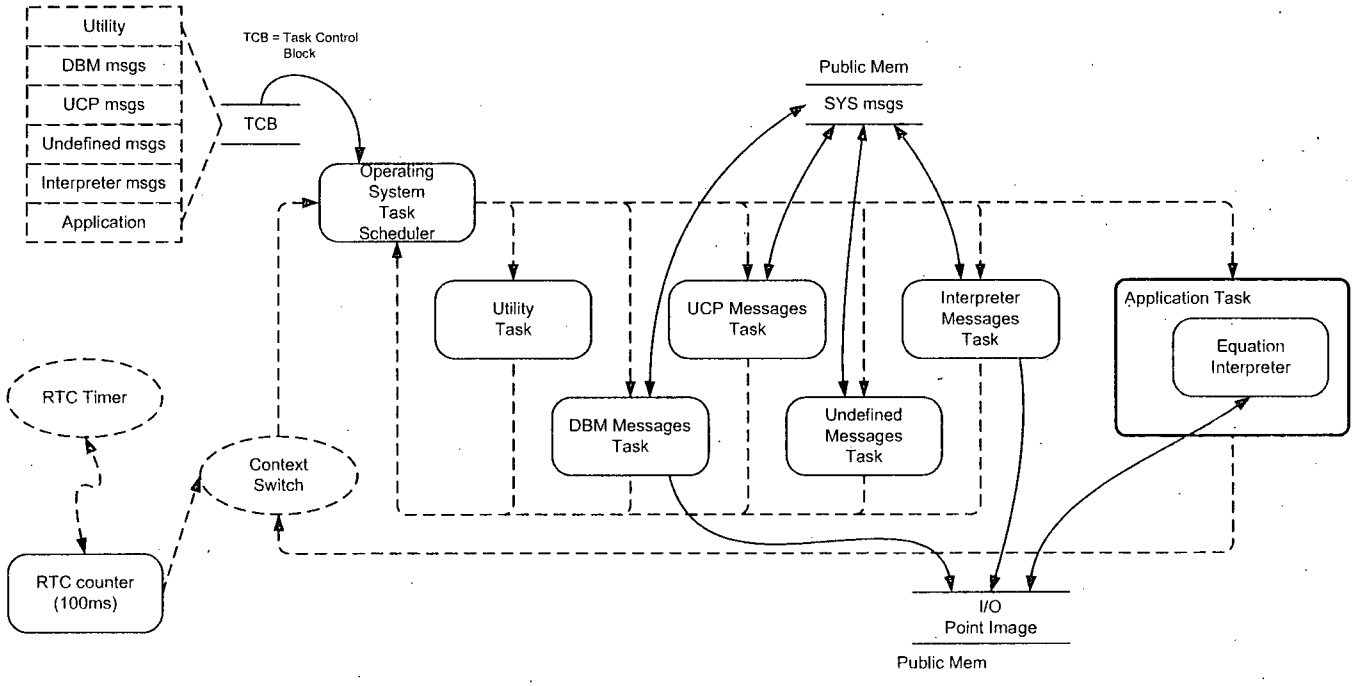

Figure 13. System Software Architecture

The tasks running on the SYS processor are:

- Equation Interpreter Task for running the application program on I/O point images. This is implemented by individual logic subroutines and analog processing algorithms.
  - IOSS_TSK

- UCP Message Handling Tasks which will process the UCP message and call the appropriate routines to provide service to the UCP requests. The services requested include:
  - CQ4INT - CQ4 block update
  - PIDTSK – PID block task,
  - DBMTSK - DBM Task for I/O point images in the Public Memory
  - XEQUAL - Equalization Task for DPM
  - EQMSGTSK - Equation Interpreter service
  - PKTXHG – Packet exchange service
  - UNDEFTSK – handling undefined UCP messages
  - OFFLINETSK – handling UCP messages from EWS workstation intended for offline controllers for updating various controller configuration information. The Equation Interpreter will be stopped so that the application programs will not be executed.

- Operating System tasks:
  - UTILTSK – Performs configured initialization and utility functions
  - UCPTSK - UCP message activity monitoring task

- System processor tasks, such as
  - STATSK - Processor Status Monitor Task
  - IOSTSK - I/O Simulation Task for simulation of the operation of control system like I/O image changes without the presence of real field devices.
  - BLRQ - Build DDB Filter Task, etc.

During initialization, the SYS processor configures several Mailbox utility functions for the OS Utility Task. These mailbox functions are essential to determine the System Controller's Sanity. During every Operating System task scan cycle, these functions will be executed by the Utility Task according to the operation mode of the controller: Primary or Secondary. Refer to Section 3.7.2 for detailed descriptions.

Existing software components will be used to build the SYS Processor software. All of the above tasks, the Operating System and UCP Network Utilities are covered by Component Design Specifications. Refer to Section 5 for the reference document numbers.

The descriptions of Initialization Process are provided in the DS901-000-001, HFC-SBC06 Module Detailed Design Specification.

3.5 ICL Processor Section

The ICL Processor section is based on an Intel 386 processor. Figure 14 shows the architecture of the ICL Processor section. The major function of the ICL Processor section is to handle communication on the ICL to obtain current plant status information from the I/O boards and to send operation commands to the I/O boards.

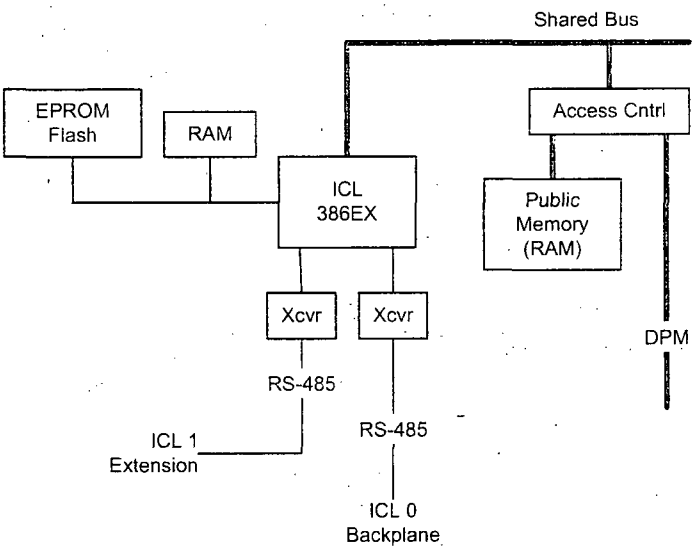

Figure 14. ICL Processor Architecture

The control system interface to field devices in the plant, such as process input sensors and output actuators, is handled by I/O boards mounted in the HFC-6000 board rack. The I/O boards measure signals from field device inputs, convert the measurements to digital images, and control output drive-level signals to plant actuators. The output drive-level signals are the converted values of output images sent to the I/O board from the HFC-SBC06.

The digital images the HFC-SBC06 receives from and sends to the I/O boards are carried by the ICL network that connects the HFC-SBC06 System Controller to its I/O boards. The ICL is structured as an RS-485 network implementing a master/slave communication control protocol. The HFC-SBC06 System Controller board provides the network master function and controls communication on the connected ICL network connected to it. Each I/O board operates as a slave node on the ICL network to which it is attached. The System Controller polls each I/O board, requesting data values for field inputs connected to the I/O board and sending data values for field outputs connected to the I/O board. Only the HFC-SBC06 board will initiate a communication on the ICL with a request message.

The HFC-SBC06 System Controller board has two serial channels: ICL0 and ICL1. ICL0 is on the controller backplane, but it has a connector on the backplane so that it can access boards in

expander chassis. ICL1 only goes to expander chassis. Both channels can communicate with boards in up to two chassis. ICL0 and ICL1 will be connected to different I/O boards but they are logically one ICL. In a redundant configuration, each of the dual serial ports of an I/O board is connected to one of the redundant controllers via an ICL.

The ICL Processor has access to the DPM. This capability is used in a redundant configuration for the secondary ICL Processor to takes over the scan task of an I/O board if the primary ICL does not function well with a particular I/O board. If an I/O board does not respond to a regular poll message from the primary ICL Processor, the primary ICL Processor transfers the request message to a dedicated area in the DPM for the secondary ICL Processor to poll that particular I/O board. If the secondary ICL is functional, the secondary ICL processor takes over the scan task for that I/O board and uses the DPM to pass the response data to the primary ICL Processor. Periodically, the secondary ICL Processor performs a loopback test for that I/O board to determine if the primary link is functioning. If the loop test results show that the primary ICL is functioning properly with that I/O board, the primary ICL resumes polling this I/O in its normal sequence.

3.5.1 ICL Software Architecture

The SYS Processor software consists of the following routines:

- Initialization
  - Power up/Reset Initialization
  - Controller Configuration
  - Processor Specific Initialization
    - ICL Communication Initialization
- Operating System Component
- Processor Specific Tasks
  - ICL Scan Task
    - ICL Download Table Routine
    - ICL Scan Routine
      - Primary Mode Routine
        - Build ICL Command
        - Perform Transaction Routine
        - Process Response Routines
      - Secondary Mode Routine
  - Communication Utility Routines
    - Send Message Routine
    - Receive Message Routine
  - ICL Utilities
  - Timer Interrupt Service Routines
- UCP Utilities
  - UCP Memory Manager
  - Network Manager for Path Element
  - Network Message Routine

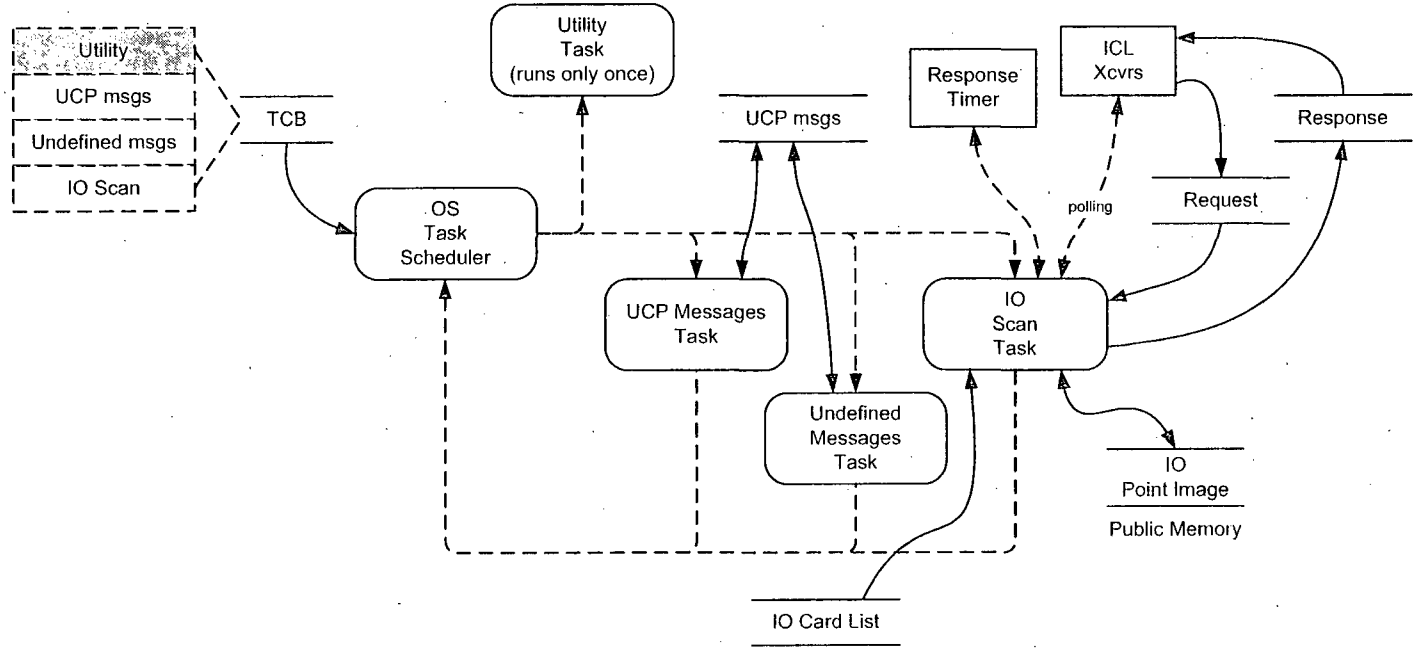

Figure 15. ICL Software Architecture

The ICL Processor software is also designed based on the operating system component common to all processors on the HFC-SBC06 board and a set of configurable tasks that will be run by the operating system. Figure 15 provides an overview of the ICL Processor Software Architecture.

The tasks running on the ICL Processor are:

- ICL I/O Scan Task:
  - IOFSCN

- UCP Message Handling Tasks which will process the UCP message and call the appropriate routines to provide service to the UCP requests. The services requested include:
  - UNDEFTSK – handling undefined UCP messages
  - OFFLINETSK – handling UCP messages intended for offline controllers for updating various controller configuration information

- Operating System tasks:
  - UTILTSK – No utility routines configured
  - UCPTSK - UCP message activity monitoring task

The ICL Processor software does not have any special utility functions configured for the OS Utility Task. So after finishing the initialization part of functions, the OS Utility Task will remove its self from the OS task control block list and will not be executed again.

The existing software components will be used to build the ICL Processor software. All of the above tasks, the Operating System and UCP Network Utilities will be described in Component Design Specifications. Refer to Section 5 for the reference document numbers.

The descriptions of Initialization Process are provided in the DS901-000-001, HFC-SBC06 Module Detailed Design Specification.

3.6 CPC Processor Section

The CPC Processor section is based on an Intel 386 processor. Figure 16 shows the architecture of the CPC Processor section. The CPC Processor section includes hardware for two identical Ethernet channels with twisted pair 10BaseT configuration. The Ethernet interface is implemented with two serial interface network controller chips (NIC). The 10BaseT interface to the C-Link functions in accordance with IEEE 803.2 standards.

The NICs incorporate receiver, transmitter, collision detection, heartbeat, jabber timer, and link integrity test functions. There is one DPM between each NIC and the CPC processor. This DPM provides the memory buffer for the messages received and to be transmitted by the NIC.

The CPC processor controls overall operation of the Ethernet interface to the C-Link, transfer of data to or from the NIC via the DPM, and transfer of data to and from the Public Memory.

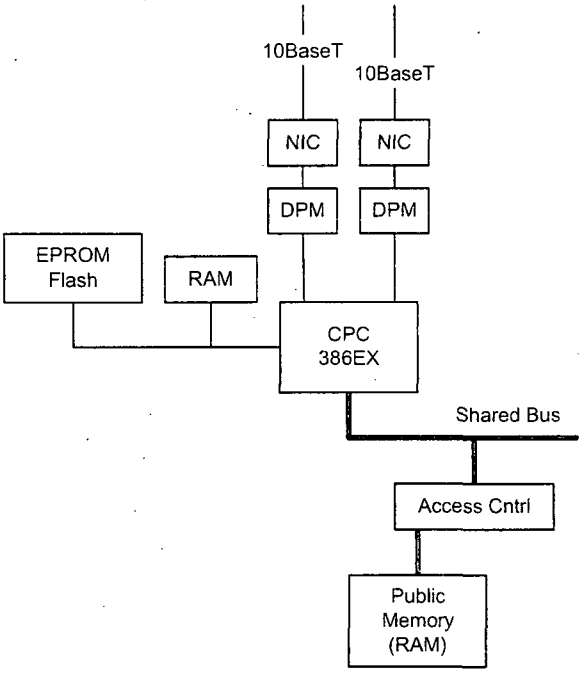

Figure 16. CPC Processor Architecture

3.6.1 CPC Processor Software Architecture

The CPC Processor Software consists of the following routines:

- Initialization
  - Power up/Reset Initialization
  - Controller Configuration
  - Processor Specific Initialization
    - NIC Initialization
    - Tasks Initialization
    - Data Initialization
    - Interrupt Vectors Initialization
- Operating System Component
- Processor Specific Tasks – Communication Tasks
  - Transmit Tasks
    - Interface Transmit Task
    - LLC Transmit Task

        - NIC Transmit Driver
    - Receive Tasks
        - Receive ISR
        - LLC Receive Task
        - Interface Receive Task
    - Timer Interrupt Service Routines
        - Timer 0 ISR
        - Timer 1 ISR
        - Timer 2 ISR
    - DDB Process Routine
        - Get DDB Routine
        - Put DDB Routine
        - Save DDB Routine
- UCP Utilities
    - UCP Memory Manager
    - Network Manager for Path Element
    - Network Message Routine

The CPC Processor software is also designed based on the operating system component common to all processors on the HFC-SBC06 board and a set of configurable tasks that will be run by the operating system. Figure 17 provides an overview of the CPC Processor Software Architecture.

The tasks running on the ICL Processor are:

- C-Link Communication Tasks:
    - LLCRCV – LLC layer receive task
    - LLCTRN – LLC layer transmit task
    - ITFRCV – Interface layer receive task
    - ITFTRN – Interface layer transmit task

- UCP Message Handling Tasks which will process the UCP message and call the appropriate routines to provide service to the UCP requests. The services requested include:
    - UNDEFTSK – handling undefined UCP messages
    - OFFLINETSK – handling UCP messages intended for offline controllers for updating various controller configuration information

- Operating System tasks:
    - UTILTSK – No utility routines configured
    - UCPTSK - UCP message activity monitoring task

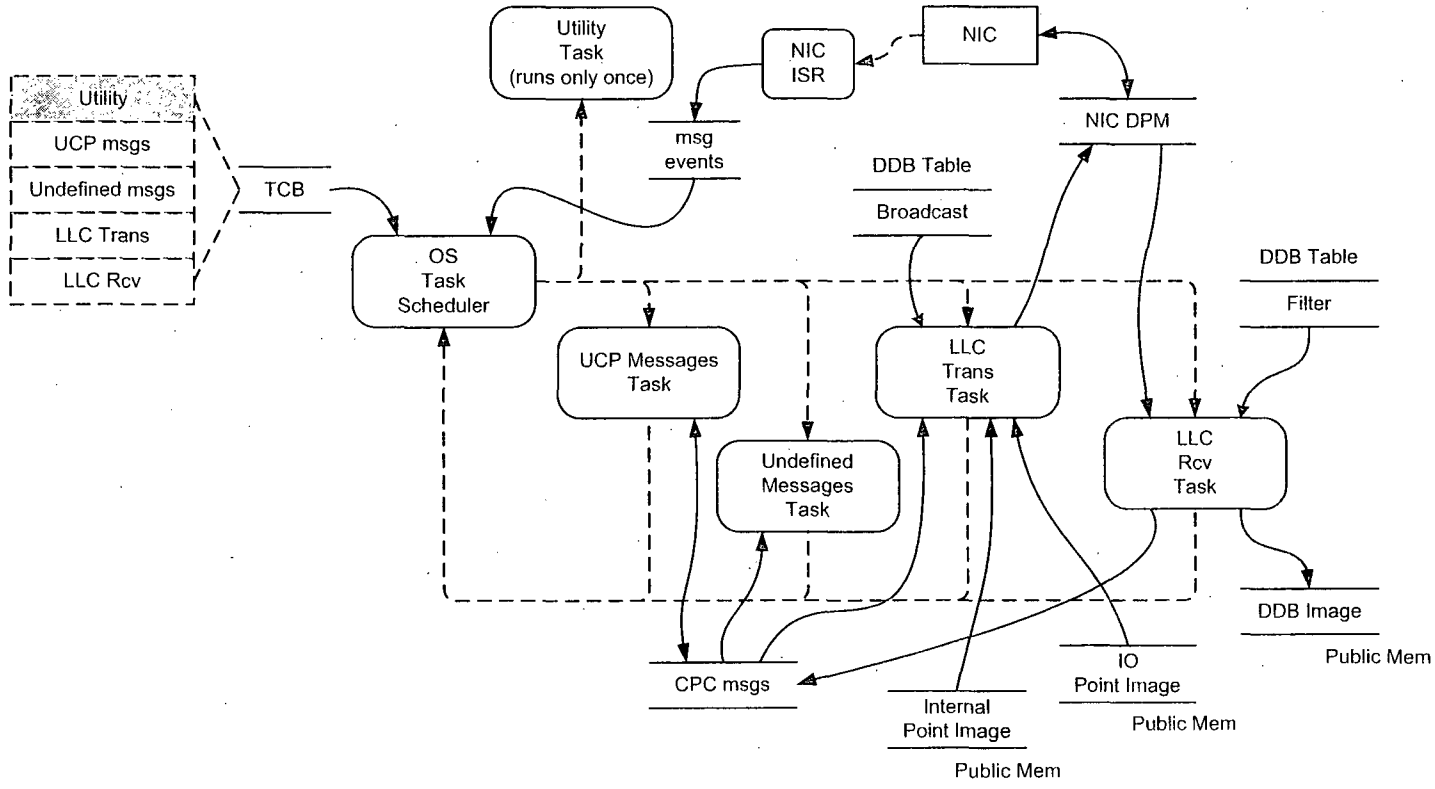

Figure 17. CPC Software Architecture

The CPC Processor software does not have any special utility functions configured for the OS Utility Task. So after finishing the initialization part of functions, the OS Utility Task will remove its self from the OS task control block list and will not be executed again.

The existing software components will be used to build the CPC Processor software. All of the above tasks, the Operating System and UCP Network Utilities will be described in Component Design Specifications. Refer to Section 5 for the reference document numbers.

The descriptions of Initialization Process are provided in the DS901-000-001, HFC-SBC06 Module Detailed Design Specification.

3.7 HFC-SBC06 and HFC-DPM06 Redundancy Architecture

Refer to Section 2.2 for descriptions of Redundant System Controllers. Two HFC-SBC06 boards and a HFC-DPM06 board in the redundant configuration are installed in the three leftmost slots of the HFC-6000 controller rack, with the DPM06 board installed between the two HFC-SBC06 boards. The three boards include hardware and software designed to support redundant controller operation. The main functions of the redundant architecture are as follows:

- Logic to determine controller operation mode: Primary or Secondary
- Failover mechanism on failure of primary controller
- Manual maintenance failover
- Controller failure detection mechanism
- Mechanism to ensure a smooth transition of control during failover

Figure 18 shows the redundancy architecture. Each of the HFC-SBC06 System Controller has a Sanity circuit consisting of mainly a CPLD. This circuit provides a SANE signal and a PRI (primary) signal to indicate the sanity and primary status of the system controller board. These signals are routed to the backplane as inputs to the failover circuit on the HFC-DPM06 board. This failover circuit is implemented mainly by a CPLD, a maintenance failover push button and board edge LEDs.

The Sanity circuit determines the sanity of the controller by the action that the SYS Processor strobes the watchdog timer before it times out. The SYS processor periodically initiates a strobe to the watchdog timer to keep the Sane signal in its active state. If the PRI signal from the other controller is false, the Sanity circuit will produce a true PRI signal. The failover circuit on the DPM06 board activates corresponding output signals to board edge LEDs to indicate that status. However, the Sanity circuit will not make the PRI signal true if the PRI signal from the other controller is already true, which means that the other controller is running in primary mode. This condition causes the controller to operate in secondary mode.

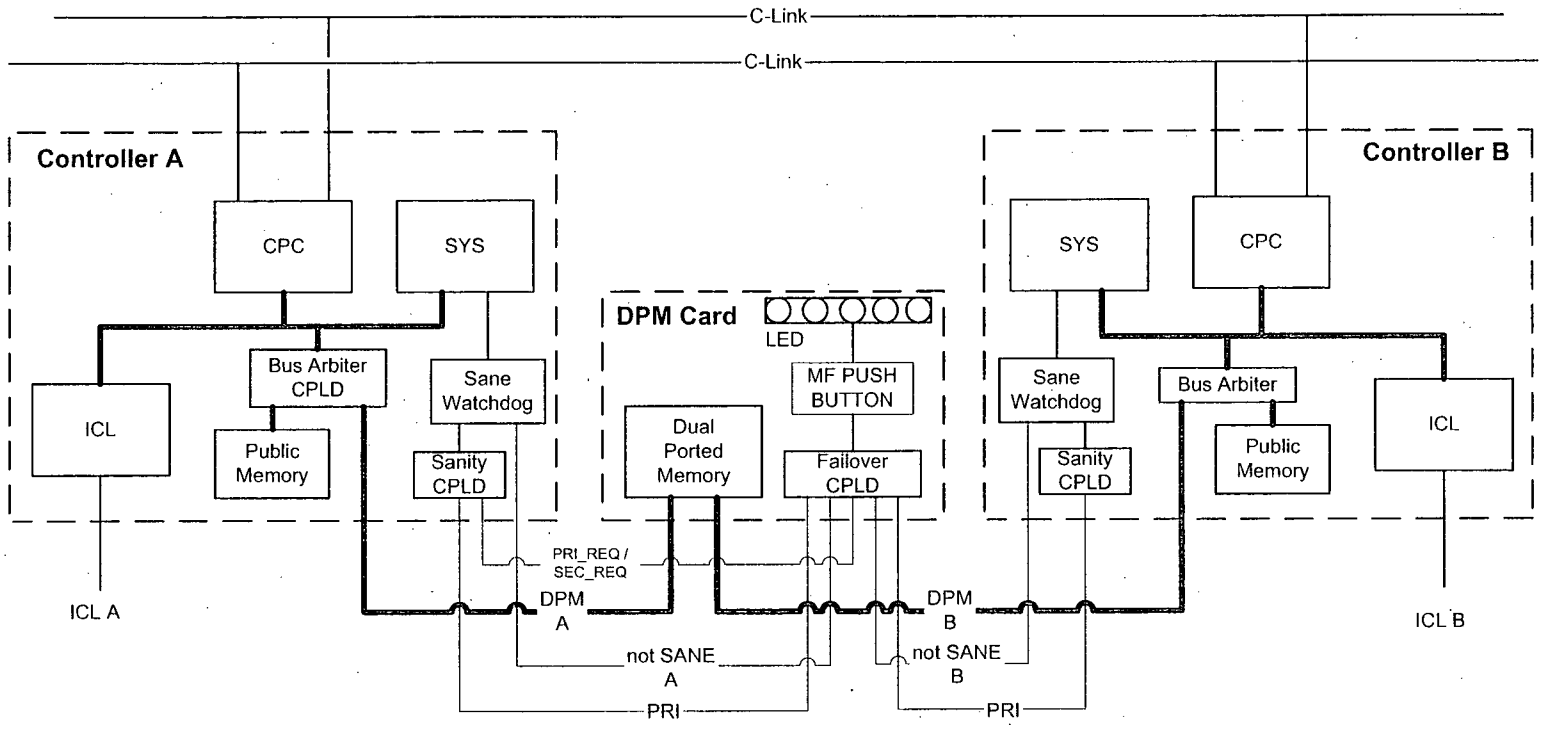

Figure 18. HFC-SBC06 Redundancy and Failover

During the start up of redundant controllers, the SANE signals in both controllers are inactive, and so are the PRI signals. The controller that finishes initialization first sends a strobe to its watchdog timer first. The Sanity circuit sets both the SANE and PRI signals true. The SYS Processor software of this controller reads the PRI signal to determine its operation mode, sets a remote operation status flag to Primary in the Public Memory, and starts operating in Primary mode. The other two subordinate processors of this controller read the operation mode flag in the Public Memory and start operating in Primary mode too. On a parallel process, the other controller finishes initialization, strobes its watchdog timer and becomes sane, but its Sanity circuit can not set the PRI signal to true, because the PRI signal from this controller is already true. So every processor on the other controller will operate in Secondary mode.

The SYS Processor software strobes the Watchdog Timer periodically, so that the SANE signal from the Sanity circuit will remain true. If the software fails to strobe the Watchdog Timer, the watchdog timer will time out. The SANE status signal will then be disabled. The change in SANE signal from true to false will cause the PRI signal to become false. If the controller is currently in secondary mode, the maintenance failover function will be disabled to prevent manual activation of failover while the secondary controller is not functioning properly. If the controller is currently in primary mode, a failover will be triggered. The current primary controller will become secondary, and the current secondary controller will become primary. During the failover process, the SYS Processor detects the need for an operation mode change first by comparing the hardware PRI signal with its current remote operation status. It changes its remote operation status flag in the Public Memory and sets the Synchronization flag to Not_In_Sync. The Operating System on each processor detects that a synchronization of operation status is needed for all tasks running on that processor. After each processor is synchronized, the Operating System on the SYS Processor will clear the Synchronization flag.

As long as both controllers are operating normally (SANE and all applications data validated), the failover circuit on the DPM06 board activates an output to the LED DS1. This display indicates that the maintenance failover function is available. If the user presses the maintenance failover button on the DPM06 board, the failover circuit activates a SEC_REQ signal for controller A if it is currently the Primary controller, or a PRI_REQ signal if it is currently the Secondary controller. This signal causes controller A to initiate failover to controller B by setting its PRI status from Primary to Secondary (with SEC_REQ signal) or from Secondary to Primary (with PRI_REQ signal). Assuming that controller A is the current primary controller, the change of its PRI status will cause the current secondary controller to change its PRI from Secondary to Primary. However, if one of the two controllers loses SANE status, the DS1 LED goes out, and the maintenance failover function is disabled.

Additional information of the Failover Mechanism and DPM Transfer is provided in DS001-000-08, Failover Mechanism Component Design Specification.

3.8 HFC-SBC06 CPLD Design

The HFC-SBC06 utilizes four Xilinx CPLDs and the HFC-DPM06 utilizes one Xilinx CPLD to implement most of the required miscellaneous "hardwired" digital logic functions. These CPLDs, when programmed, function as though they were a matrix of individual logic gates. The algorithms contained within these devices are defined in VHDL source codes.

- PBUSIF - This CPLD provides logic necessary to interface the SYS processor's local bus with the other components on board, such as flash memory access, .

- SBC6_CHSEL – This CPLD provides the logic necessary to perform such functions as chip selects, interrupt controller,, I/O ports, timer and processor reset for the SYS processor.

- SBC6_386C – This CPLD provides the chip selects, memory read, and memory write control both of the 386EX processors, i.e. CPC processor and ICL processor. It also provides reset logic and public memory access control for these two processors.

- SBC6_SHARB – This CPLD defines the address range of the public memory and the DPM as well as providing the SOE (sequence of events) timer.

Details of the data lines defined by these CPLDs are provides in the DS901-000-01, HFC-SBC06 Module Detailed Design Specification.

3.9 Sequence of Events Timer

The HFC-SBC06 system controller maintains a Sequence of Events (SOE) timer over 24 consecutive hours of operations. The SOE timer is used for "time tagging" events that occur system wide. This timer can be synchronized by some master SOE timer located elsewhere in the system, or can be the master timer itself. The SOE timer provides a resolution of 100 μS for synchronizing similar SOE timers on each I/O boards.

The timer is implemented by a timer with 100 μS resolution contained in the SBC6_SHARB CPLD. The SOE timer is a 45-bit counter capable of counting 100 μS intervals for over 100 years. By convention, software algorithms assume some base date and time, such as midnight, Jan. 1, 1980, which corresponds to a counter value of zero. This initial date and time, expressed in seconds, is called the base time. The counter value corresponding to the current time can then be calculated by multiplying the number of seconds that have elapsed since the base by 10,000. Proceeding in this manner, the SOE timer can be loaded with the current time value at initialization.

When the system controller is configured for SOE logging, the SYS processor communicates with configured buffers within the CPLD to transfer commands, the timer preset value, and to read the current timer count. The SYS processor can transfer data to the buffers or read the current count value without disrupting operation of the counter.

3.10 HFC-DPM06 Board

The HFC-DPM06 board provides three onboard DIP switches for the configuration settings of the HFC-SBC06 System Controller board. It also provides a dual ported memory, a failover circuit, LEDs, four bus driver chips, and a maintenance failover push button for redundant controller configuration.

There is a CPLD on the HFC-DPM06 board. This CPLD supports arbitration and bus control functions and maintenance failover. It receives a set of status and control signals from both the redundant System Controller boards. The resulting outputs from the CPLD control operation of the four onboard bus drivers and status displays on the board edge LEDs. The same CPLD also provides logic to support the failover mechanism for redundant system controller configuration.

4. Configuration Setup and LED Displays

The HFC-SBC06 board contains one 8-position DIP switch, two toggle switches and nine jumpers. The switches and jumpers enable manual control of reset, hardware configuration, and programming of the board. Additional configuration switches are physically located on the HFC-DPM06 common board.

4.1 HFC-SBC06 Onboard Switch Functions

SW1 Power on/off, RESET

SW2 Positioned down (toward the board) permits write cycles to onboard flash memory chips. The switch is placed in this position to program flash memory for the ICL and CPC processors and to download the application program to the flash memory of the SYS processor.

Positioned away from the board enables a write-protect function for flash memory. For safety-related applications, the switch should remain in this position for normal operation.

SW4 8-position DIP switch defines operating modes and control parameters as indicated in Table 1.

Table 1. SYS Processor Configuration Switches

Switch	Function
SW4-1 SW4-2	
SW4-3	
SW4-4	
SW4-5	
SW4-6	
SW4-7	
SW4-8	

4.2 HFC-DPM06 Onboard Switch Functions

Three eight-position DIP switches on the DPM common board control values for the following parameters:

4.3 HFC-SBC06 Onboard Jumper Options

Table 2 defines the function of each jumper included on the HFC-SBC06 controller.

Table 2. Jumper Options

Jumper	Function
J1	
J8	
W2	
W3	
W5	
W6	
J5	
E1, E2	

4.4 LEDs

The HFC-SBC06 board contains eight board-edge LEDs, which provide a visual indication of functional status of the controller hardware and software. The HFC-DPM06 board contains five board-edge LEDs, which provide a visual indication of functional status of the controller.

4.4.1 HFC-SBC06 LED Functions

DS1 Includes four LEDs to indicate hardware status of the Ethernet interface as follows:

- DS1-1 flashes on for approximately 50 ms when C-Link channel 1 transmits in TPI mode.
- DS1-2 flashes on for approximately 50 ms when receive data is detected for C-Link channel 1 in TPI mode.
- DS1-3 flashes on for approximately 50 ms when C-Link channel 0 transmits in TPI mode.
- DS1-4 flashes on for approximately 50 ms when receive data is detected for C-Link channel 0 in TPI mode.

DS2 Includes four LEDs . Two LEDs are controlled directly by the P1.6 and P1.7 ports of the ICL microprocessor, and two are controlled by the corresponding ports of the CPC microprocessor.

DS3 and DS4 Includes 8 LEDs controlled by the SYS Processor. Refer to Section 4.4.1.1.

4.4.1.1 DS3 and DS4 LEDs

If the SYS processor detects a failure condition during system initialization/reset, the display freezes with the LEDs displaying a binary code for that fault. Table 3 lists the defined error codes and the error conditions that they represent. Throughout normal operation, the LED display represents a binary code for different processor tasks, and the LED code for a particular task lights while it is running. As a result, all 16 LEDs flicker constantly during this phase of operation. The bottom LED is always on when the board is running normally. Table 4 lists the defined task LED code. If the board detects a failure condition during normal operation, the display freezes with the LEDs displaying a binary code for that fault. Table 5 lists the defined error codes and the error conditions they represent.

Table 3. DS3 and DS4 LED Indications for Initialization Failure

Code	Error Condition
01_H	
02_H	
03_H	
04_H	
05_H	
06_H	
07_H	
08_H	
09_H	
$0A_H$	
$0B_H$	
$0C_H$	
$0D_H$	
$0E_H$	
$0F_H$	
10_H	
11_H	
12_H	
13_H	
14_H	
15_H	
16_H	
17_H	
18_H	
19_H	
$1A_H$	

Table 4. DS3 and DS4 LED Indications for Individual Tasks

Bit	Hex	Task
0	1_H	
2	4_H	
3	8_H	
5	20_H	
6	40_H	
7	80_H	
9	200_H	
10	400_H	
11	800_H	
15	8000_H	
Other	Other	

Table 5. DS3 and DS4 LED Failure Indications During Normal Operation

Code	Error Condition
01_H	
02_H	
03_H	
04_H -10_H	
11_H	
12_H	
13_H	
14_H	
15_H	
Note: All processor failure codes are defined, but they are functional only if that processor is configured for the control system.	

4.4.2 HFC-DPM06 LED Functions

DS1 Lights when the maintenance failover function is available (controller A and controller B both sane).

DS2 Lights when controller A is primary.
DS3 Lights when controller A is sane.

DS4 Lights when controller B is primary.
DS5 Lights when controller B is sane.

4.5 Installation of System Software and Application Programs

Each of the three onboard processors has a dedicated flash memory and a dedicated PROM for system software. SYS processor also has a dedicated flash memory for its application program code. Switch and jumper selections on the board cause the processor to boot from either the PROM or the flash memory.

At the present time, the system software normally is burned into a separate PROM for each processor, and then each PROM is installed in the PROM sockets associated with the appropriate private memory array. The code is then copied from PROM to flash memory during the initialization sequence. During system development, the application code can either be downloaded to flash or installed in PROM for transfer to flash. Once system development and tuning has been completed, the download function should be disabled to prevent inadvertent alteration of the application code. Throughout the normal operating life of a system, all application code should be transferred to flash from PROM to ensure proper configuration management.

4.5.1 System Code Transfer to Flash

Initially, the flash memory chips are blank. The following steps describe the procedural sequence required to transfer system software code to each of the onboard flash memory chips.

1. Install jumper J1 to enable the SYS processor to boot from its system code PROM.

2. Install the PROM containing system software for the SYS processor in socket U52.

3. Set DIP switch SW4-8 in the ON (toward the board) position.

4. Install jumper J8 to enable the ICL and CPC processors to boot from their system code PROMs.

5. Install the PROM containing the system software for the ICL processor in socket U7.

6. Install the PROM containing the system software for the CPC processor in socket U8.

CAUTION

Make sure that S1 is positioned toward the board before installing it in the board rack. If SW1 is positioned away from the board and power is applied to the rack, power transients could damage components on the board.

7. Mount the board in a controller slot of the HFC-6000 controller board rack.

8. Ensure that power is applied to the board rack, and position S2 toward the board to enable write cycles to flash memory.

9. Ensure that power is applied to the board rack, and position SW1 away from the board.

10. Following application of operating power, the system software will be transferred from U52 to the flash memory for the SYS processor. Successful transfer will be indicated by the following:

    - LED01 lights for several seconds and then goes out.
    - LED00 through LED07 light in sequence.

11. The system software for the ICL and CPC processors should be transferred to flash memory.

NOTE

> As long as J1 remains installed, the SYS processor will boot from the PROM installed in socket U52. That code will be compared with the code currently in flash memory; and if it is different, the contents of PROM will be transferred to flash memory and the processor will operate from that code. If J1 is removed, the SYS processor will boot from the flash memory without examining the contents of its PROM.
>
> As long as J8 remains installed, the ICL and CPC processors will boot from their respective PROMs. If SW2 is positioned as write enable, the contents of the PROMs will also be transferred to the flash memories for the two processors.

12. After the installation of the system software to flash, do the following:

    - Remove jumper J1.
    - Set DIP switch SW4-8 OFF (away from the board).
    - Leave jumper J8 installed (for current software design).

4.5.2 Application Code Download

The application program codes can be compiled by an EWS workstation software and downloaded to the controller over the C-Link. This download can be repeated following any modification or update to the application code during application development; however, the download function should be disabled during normal operation to prevent inadvertent changes to the application.

1. Set S1 toward the board to remove power from the board.

2. DIP SW4 can be set to place the software in offline mode (SW4-1 ON and SW4-2 OFF). While operating in this mode, the system software runs normally, but the equation interpreter task does not run.

3. Set S2 toward the board to enable flash write cycles.

4. For redundant controllers, set SW4-5 ON.

5. For redundant controllers, repeat steps *1* through *4* for the second controller.

6. Set S1 away from the board to enable distribution of operating power on the board (both controllers for redundant configurations).

7. At the EWS workstation, compile the final application code for the controller.

8. Download the equations, RQ file, and CQ4 blocks, as applicable.

9. For redundant controllers, initiate failover to the secondary controller.

10. Download the equations, RQ file, and CQ4 blocks as applicable.

11. Set S2 away from the board to disable flash memory write cycles.

12. If the controller was placed in offline mode, power down the controller and set both SW4-1 and SW4-2 OFF to enable normal operation. Power the controller up to enable controller operation to begin.

4.5.3 System Software Updates

If an upgrade is provided for the system software of one or more processors on the controller board following installation, repeat the procedure described ion paragraph 4.5.1. Direct download of system programs code to flash memory is not presently supported.

4.6 Hardware Configuration

Refer to Tables 1 and 2 for a general definition of functions controlled by the onboard switches and jumpers. The following steps identify typical switch and jumper settings required for normal operation. Record the specific DIP switch settings required for each controller to be used in the system.

CAUTION

Make sure that S1 is positioned toward the board before removing or installing the board in the board rack. If SW1 is positioned away from the board and power is applied to the rack, power transients could result in damage to components on the board.

1. Set SW4-1 and SW4-2 on the HFC-SBC06 board both in the open position. This configuration enables normal run mode for the system software.

2. If the controller is used as part of a redundant pair, set SW4-5 closed. This enables regular transfers of status from the primary to the secondary via the HFC-DPM06 array.

3. Set SW4-6 closed. This enables the sanity function.

4. Set SW4-7 and SW4-8 both open. This disables software downloads from the EWS workstation.

5. Set DIP switches on the HFC-DPM06 board to provide the following configuration parameters:

   - Set SW2 to the binary value for the remote number assigned to this controller. The valid range is from 0 to 255.

   - Set SW4 to the binary value for the total number of remotes configured for this system (up to 255).

   - Set SW1 to the binary value for the sequence number of this remote on the C-Link. The valid range is from 0 to 31.

CAUTION

The remotes must be configured on the C-Link in numeric sequence with the HIFR assigned the sequence number of 0. If any remote is installed out of sequence, reliable communication with that remote over the C-Link could be disrupted.

6. When the HFC-SBC06 board is used as a redundant controller, a jumper should be installed from node J5–1 to J5–2. This hardware interlock requires the controller chassis to complete its power up initialization sequence successfully (SANE status TRUE) and become the primary controller before the ICL processor can begin transmitting over its serial link. Removing all jumpers results in a configuration in which the transmit interface remains enabled as long as logic power is present.

5. Module Design Constraints

The following is a list of specifications that constraint the design of an HFC-SBC06 board module.

5.1 Communication Interface Specifications

- Document DS002-000-01, C-Link Protocol Component Specification
- Document DS002-000-02, ICL Protocol Component Specification
- Document DS002-000-03, UCP Protocol Component Specification

5.2 Operating System Specification

- Document DS001-000-01, Operating System Component Design Specification
- Document DS001-000-02, Equation Interpreter Component Design specification
- Document DS001-000-03, CQ4 Component Design Specification
- Document DS001-000-06, System Component Design Specification
- Document DS001-000-07, Job Component Design Specification
- Document DS001-000-08, Failover Mechanism Component Design Specification

5.3 Hardware Interface Specifications

- Document 40040901, HFC-BPC01-19 Backplane Specification
- Document 40041401, HFC-BPE01-19 Backplane Specification
- Document DS901-000-34, HFC-BPC01-23 Backplane Specification
- Document DS-901-000-35, HFC-BPE0-23 Backplane Specification
- Document DS-901-000-36, HFC-BPC02-23 Backplane Specification
- Document DS-901-000-37, HFC-BPC02A-23 Backplane Specification
- Document DS901-000-38, HFC-BPC03-23 Backplane Specification

2.4 Design Safety

5.4.1 Main Processor – SC Code

5.4.1.1 Criticality

5.4.1.2 Hazard

5.4.1.3 Security

5.4.1.4 Risk

5.4.2 ICL Processor – SAP Code

5.4.2.1 Criticality

5.4.2.2 Hazard

5.4.2.3 Security

5.4.2.4 Risk

5.4.3 C-Link Processor – SEP Code

5.4.3.5 Criticality

5.4.3.6 Hazard

5.4.3.7 Security

5.4.3.8 Risk

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HFC-6000 Product Line

HFC-6000 I/O Board
Module Design Specification

NON-PROPRIETARY

MS901-000-02

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1. Introduction

The HFC-6000 distributed control system provides plant monitoring and control capabilities with monitoring and control responsibilities spread over multiple remote control units. The I/O boards are sensors and drivers for implementing plant control functions. They provide signal-level interfaces to the equipment and devices in the plant. As shown in Figure 1, an HFC-6000 I/O board is positioned in the HFC-6000 system hierarchy between the HFC-SBC06 System Controller(s), which is the CPU of HFC-6000 system, and the equipments and devices in the plant.

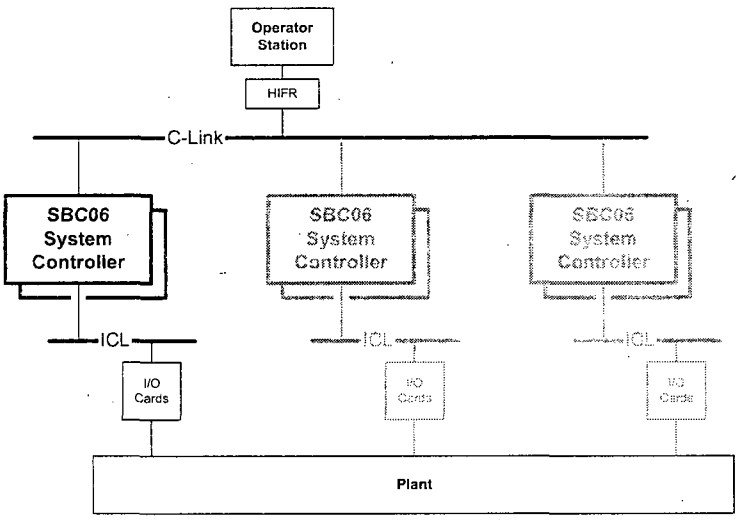

Figure 1. HFC-6000 System Hierarchy

Descriptions and discussions of the functional requirements of the HFC-6000 I/O boards from an external perspective are provided in Appendix C-N of the HFC-6000 Product Line Requirements. The design of the HFC I/O boards complies with the generic HFC-6000 Product Line Requirements and with specific module requirements defined in Appendix C-N of the HFC-6000 Product Line Requirements.

Subsequent sections of this document provide architectural and design descriptions of a typical HFC-6000 I/O board. The HFC-6000 I/O boards use the same architectural and design concept, and share many common software modules. Lower level descriptions of each I/O board are contained in a separate Module Detailed Design Specification for each board type. The design descriptions of the common software modules and the common hardware characteristics are covered in the HFC-6000 I/O Board Module Detailed Design Specifications. The purpose of this document is to present the methods and strategies used to accomplish the operation and functions required of an HFC-6000 I/O board. The discussion of the operation and function of an HFC-6000 I/O board are presented using architectural, design, and implementation information.

2. Functional Description

This section describes the major functions performed by an HFC-6000 I/O board. The functional descriptions are presented to provide a context for understanding the internal operation of an HFC-6000 I/O board and how the functions performed by an HFC-6000 I/O board work within the overall architecture of the HFC-6000 distributed control system.

The major functions performed by an HFC-6000 I/O Board are:

- Initialization
- Communication with system controller connected to an HFC proprietary network, ICL (Inter-Communication Link);
- Setting each digital/analog output channel using digital output images, and/or getting digital input images from each digital/analog input channel
- Self diagnostics functions

An I/O board generally has two operation stages: Initialization state and Normal Operation state. Upon power up or reset, the processor firmware will accomplish initialization for hardware, software, and communication set up. During initialization, some self diagnostics tests will be performed, such as RAM Write/Read test and EPROM test. Any error detected at this state is fatal and will cause the software to halt execution.

After completing initialization, the board will enter the Normal Operation stage. During normal operation, the I/O board handles communication with the HFC-SBC06 controller and performs an I/O scan at regular intervals to set digital/analog output channels and/or read digital/analog input channels. An HFC-6000 I/O Board can have digital input channels, digital output channels, analog input channels, and/or analog output channels connected to the field devices and equipments. An I/O board having output channels receives digital images for output channels from an HFC-SBC06 system controller at regular intervals, and uses this data to set each output channel. An I/O board with input channels reads the input image for each channel and sends the images of the digital or analog inputs to the HFC-SBC06 system controller at regular intervals.

A communication interface connects an I/O board to the ICL, which is an HFC proprietary, RS-485 serial network connecting the I/O boards to the HFC-SBC06 controller. Input values from plant field devices and output values for plant actuators are transferred between the HFC-SBC06 and I/O boards over the ICL. In addition, each HFC-6000 I/O board maintains internal diagnostic status and can report that status to the HFC-SBC06 controller.

During the time between successive I/O scans, the I/O board performs its self-diagnostics functions, which are mainly RAM tests. If any error is detected by the self-diagnostics tests, the I/O board will re-enter initialization stage to perform a restart.

How an I/O board scans its I/O channels and what is the content in its communication messages with the HFC-SBC06 vary with board type and channel configuration. Table 1

provides a list of the current HFC-6000 I/O Board types and a description of the I/O channels for each board type.

Table 1. List of HFC-6000 I/O Boards

Name	I/O Channels
DO8J	8 digital relay output
DI16I	16 digital input
DC33	2 120-vac digital output and 12 digital input
DC34	2 125-vdc digital output and 12 digital input
AI16F	16 analog input
AO8F	8 analog output
AC36	4 analog input, 4 analog output
AI8L	8 channel E-type thermocouple input
AI8M	8 channel 100Ω RTD input
AI4K	4 channel pulse input

The architecture of each HFC-6000 I/O board has been developed to support the functions that the board is required to perform. The following sections provide descriptions of the architecture and design of an HFC I/O board and discuss details of the functions performed by an HFC-6000 I/O board.

3. Module Architecture

3.1 I/O Board Architecture

Figure 2 provides an overview of the architecture of an HFC-6000 I/O board. Major features of an HFC-6000 I/O board are as follows:

- An on-board 16-bit Intel 80C188EB microprocessor
- Two banks of memory:
  - Upper memory provides up to 64K by 8-bits of EPROM for functional program code storage.
  - Lower memory provides 32K by 8-bit of RAM for temporary storage of data being processed, such as I/O images, ICL messages, diagnostic data, etc.
- Two independent RS-485 serial interfaces for communication with the HFC-SBC06 system controller
- Onboard LEDs to provide a visual indication of board status
- Onboard jumpers and switches to control configuration options
- I/O digital/analog input/output channels
- Each I/O channel includes the circuitry to measure its input signal or to control its output signal. Each analog output channel includes a digital analog converter (DAC)

in its I/O circuitry to convert digital images into analog signals. AI channels are configured with a single ADC per board to convert analog signals into digital images.

- An onboard dc-to-dc converter provides regulated +5-vdc logic power
- An onboard switch permits manual reset of the microprocessor
- Two card-edge connectors (P1 and P2) mate with corresponding backplane connectors. Signal assignments for P1 are identical for all I/O boards, so that any board can be inserted in any I/O slot of an HFC-6000 chassis. The P2 connector for each I/O board uses the same hardware, but signal assignment are unique for each board type.

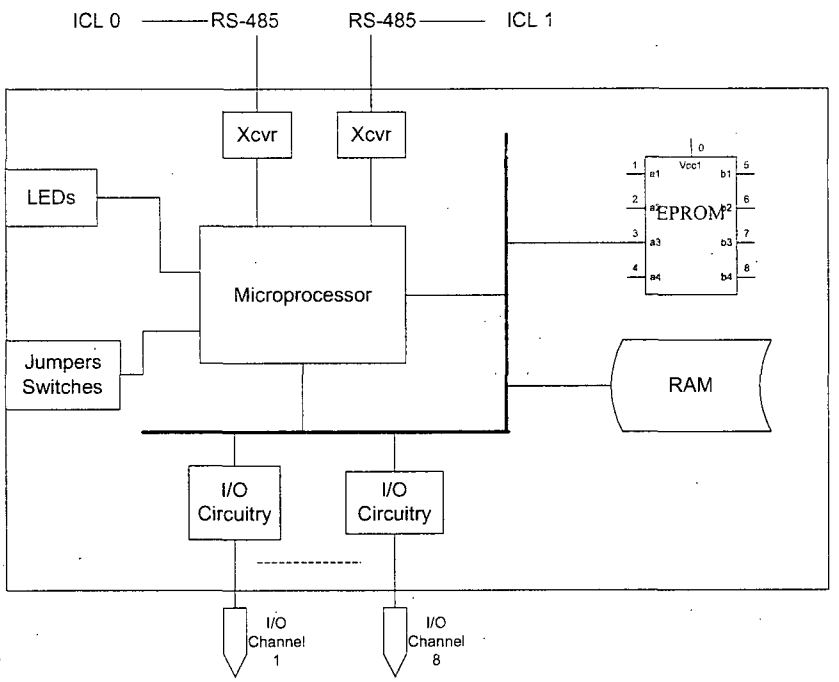

Figure 2. HFC I/O Board Module Architecture

3.2 Communication Architecture

Each HFC-6000 I/O board supports communication with the HFC-SBC06 controller via the ICL. The ICL is structured as an RS-485 network implementing a master/slave communication control protocol. The HFC-SBC06 System Controller board serves as the network master for all communication transfers with its configured ICL stations. Each I/O board operates as a slave node on the ICL network to which it is attached. The system controller polls each I/O board in station address sequence, requesting data values for input channels and sending data values for output channels. Each I/O board can transmit over the ICL only after it has been polled by the HFC-SBC06 System Controller board.

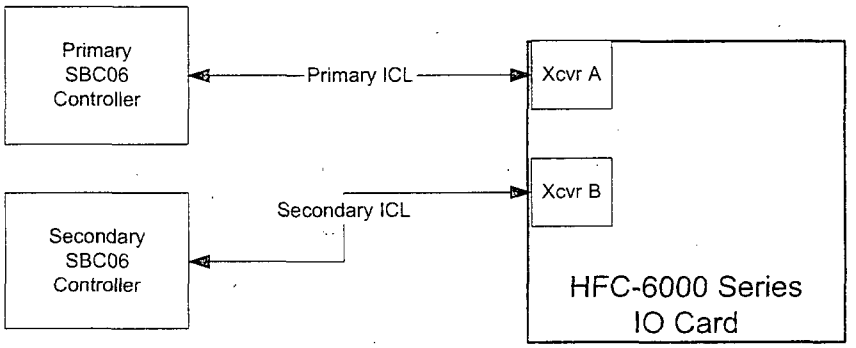

Figure 3. ICL Communication Architecture

As shown in Figure 3, each I/O board has two transceivers that are connected to the redundant ICL channels. Each ICL is connected to a separate HFC-SBC06 controller. The I/O board identifies which link has active communication during initialization and monitors that link as primary. Throughout normal operation of the HFC-6000 control system, one SBC-06 controller functions as primary and controls ICL scans; the other HFC-SBC06 is secondary and serves as a hot spare.

All polling messages from the HFC-SBC06 will be broadcast to every node on the same ICL. However, an I/O board will process only those messages that have its station address. The response messages from an I/O board will be sent to the HFC-SBC06 controller only.

The messages carried over the ICL network can be categorized into two types:

- Normal Data Update messages
- Special Request messages using Universal Communication Packet (UCP) protocol

The normal exchange between the master HFC-SBC06 and an ICL station consists of a poll message to that station followed by a poll response from that station. This exchange provides the mechanism for regular I/O data transfer. The ICL protocol also supports several types of special messages that support specific functions. Two major special message types are:

- Diagnostic request message causes the I/O board to return the image of its diagnostic status data in its response message.
- Loopback request message permits the controller to verify normal operation of the secondary ICL.

3.3 Address Space Architecture

Memory on an HFC-6000 I/O board is organized into two banks of memory, one bank of EPROM and one bank of RAM. The memory banks are connected directly to the address and data lines of the microprocessor.

The upper bank of local memory for the microprocessor provides up to 64K by 8 bits of EPROM storage ending with the address of $FFFFF_H$. Upon power-up or reset, the internal address pointer of the microprocessor begins operation by accessing the data stored at

address $FFFF0_H$ in upper memory. Therefore, the first instruction of the initialization code must be located at this address.

The low memory bank provides up to 32K by 8 bits of static RAM for general data storage. Low memory begins at address 00000_H. This portion of memory contains the data and temporary storage buffers defined by the functional code in upper memory.

3.4 Software Architecture

Each HFC-6000 I/O board's software will be composed of a set of x86 programs that will handle hardware and software initialization, I/O scan process, communication with the HFC-HFC-SBC06 controllers, and self-diagnostic tests functions.

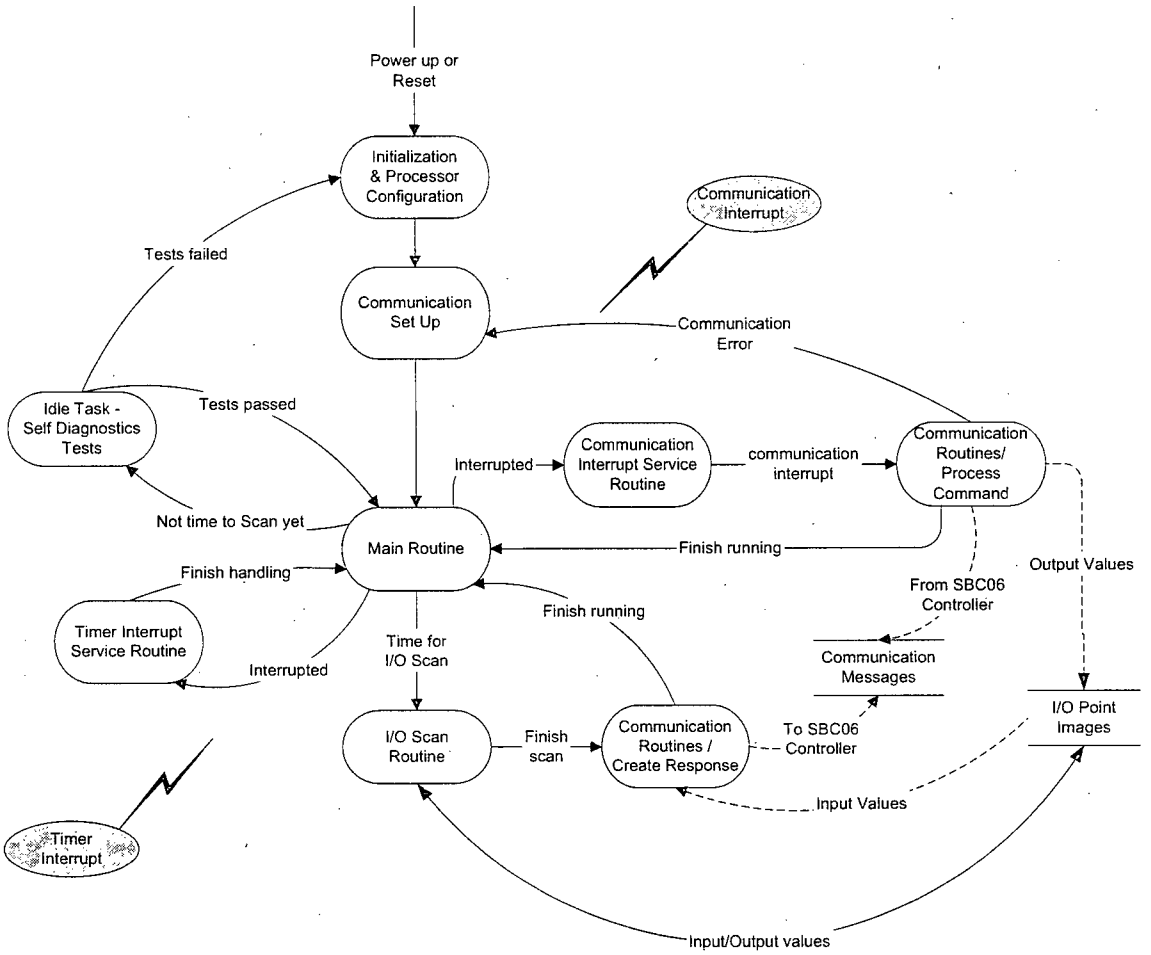

Figure 4. I/O Board Software Architecture

The I/O board software consists of the following modules:

- Initialization
  - PCB/Reset Initialization
  - Communication Set Up
- Main Routine

- I/O Scan Routine
- Idle Task – Self Diagnostic Tests
  - RAM Write/Read Test
  - EPROM Test
- Communication Routines
  - Receive Interrupt Service Routine
  - Process Command Routine
  - Create Response Routine
- Timer Interrupt Service Routines

Most of these software modules are common to all I/O boards, except those routines that are specific to each board's functions and I/O channels, such as I/O Scan Routine and Process Command Routine.

Upon power up or reset, the I/O firmware becomes activated. It runs an Initialization Routine to perform hardware and software initialization, processor configuration, and communication set up. During initialization, the RAM read/write and EPROM diagnostics tests are performed. Any error detected at this stage is fatal, and firmware execution will stop.

After initialization, the firmware enters a Main Routine which runs continuously throughout the normal operation. This Main Routine is an infinite loop. It calls an I/O Scan routine at regular intervals to perform the I/O Scan function. Between successive I/O scans, the Main Routine runs an idle task to perform self diagnostics RAM tests. If any failure is detected during self diagnostics tests, the Main Routine will transfer program control to the Initialization Routine to restart the firmware.

All I/O images will be stored in an I/O image buffer in RAM. The I/O Scan Routine will perform an I/O scan by either setting digital/analog output channel using digital output images from the I/O image buffer, and/or reading digital images from each digital/analog input channel and storing them in the I/O image buffer. How the I/O scan are performed varies with the specific type of I/O channels. Therefore, the I/O scan routine is specific to each type of I/O board.

At the end of the I/O Scan routine, a Create Response routine is called to build a response message using the new I/O scan data and to store them in the Communication Message buffer in RAM. This area contains the command message received from the controller and the response message to be transmitted to the controller.

The software is interrupt-driven and handles three type of interrupts: timer interrupt, receive interrupt on the serial communication port, and transmit interrupt on the serial communication port. When an interrupts occurs, the program control is transferred to the configured Interrupt Service Routine. After the interrupt is handled, program control is transferred back to the routine that was running when the interrupt occurred.

When a receive interrupt occurs, indicating that a message is received from the ICL, the Receive Interrupt Service Routine will validate the message and call a Process Command

Routine to process the message and to store any output images contained in the message in the I/O image buffer in RAM. Then a communication routine fetches the response message from the Communication Message buffer and transmits it to the HFC-SBC06 controller via the ICL.

Timers are used to control I/O scan intervals, communication response time out, etc. When a timer interrupt occurs, the configured Timer Interrupt Service Routine handles the interrupt.

3.4.1 Fault Detection and Processing

During Initialization, the software performs the RAM read/write test and EPROM test to detect any hardware errors in the RAM or EPROM. Any failure of these tests is fatal and will cause the program to halt execution.

Throughout normal operation, the software performs a RAM read/write self diagnostics test during the idle time between successive I/O scans. Any failure of these tests will cause the program to return to the initialization stage to perform a restart of software.

During communication with the HFC-SBC06 controller, hardware timers will be used to control the communication response time. Any communication timeout will cause the program to go to Communication Setup stage to reconfigure hardware communication channel and re-establish communication with the HFC-SBC06 controller.

3.5 Onboard Switches, Jumpers, and LEDs

This section lists the typical switches and board-edge LEDs for a standard HFC-6000 I/O board. An I/O board may include additional switches, jumpers and LEDs depending on board type. The descriptions of specific switches, jumpers, and LEDs for each particular HFC-6000 I/O board are provided in each board's Module Detailed Design Specification.

- Switch
  - SW1 Used to reset the microprocessor

- Each HFC-6000 I/O board has the following 4 LEDs
  - DS5-1 SYS A/B LED lights when serial port A is enabled to receive data; the LED is out when serial port B is enabled to receive data.

  - DS5-2 TX (Transmit Data) The TX LED lights when the microprocessor is transmitting data on the serial interface. This LED flashes periodically, except during a reset condition.

  - DS5-3 RX (Receive Data) The RX LED lights when the microprocessor is receiving data on the serial interface. This LED flashes periodically, except during a reset condition.

  - DS5-4 DMT (Dead Man Timer) The DMT LED lights when the microprocessor is running normally. This LED should remain lit continuously during normal operation.

4. Module Design Constraints

The following is a list a specifications that constraint the design of an HFC-6000 I/O board module.

4.1 Communication Interface Specifications

- Document DS002-000-02 ICL Protocol Component Specification.

4.2 Hardware Interface Specifications

- Document DS003-000-01, HFC-6000 Backplane Specification.

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HFC-6000 Product Line

Document Map

PP901-000-02

Rev A

NON-PROPRIETARY

Effective Date 11/17/04

Author/Title Angela Han

Reviewer/Title Steve Yang

Approval/Title Allen Hsu

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1. Purpose and Scope

This document defines the required documentation for the HFC-6000 product line and the documentation layer that is used. This document also provides guidance on how to go through HFC-6000 product line documentation.

The documents mentioned in this document include documentation specific to HFC-6000 product line as well as documentation for standard products or software modules, which are referred as components.

2. Conventions

Figure 1 shows the basic documentation layer for HFC-6000 documents. At the top level, there is Product Line Requirements Specification, which provides product line concept, architecture overview, list of modules included in the product line, and the requirements specification for each module.

Each module will have a Module Design Specification, which provides functional, architectural, and design descriptions of the module. According to the complexity of the module, a module detailed design specification may be required to provide more detailed design descriptions.

Each module will also have a test procedure for prototype testing and a test procedure for functional testing.

Each independent component has a Component Design Specification. A component is a software or hardware component that makes a part of a module, but the same component can be used in different modules, systems or product lines.

User's guides will also be included in the product line documentation to provide user interface, system installation and maintenance information.

Appendix A provides a list of all documents planned for the HFC-6000 documentation.

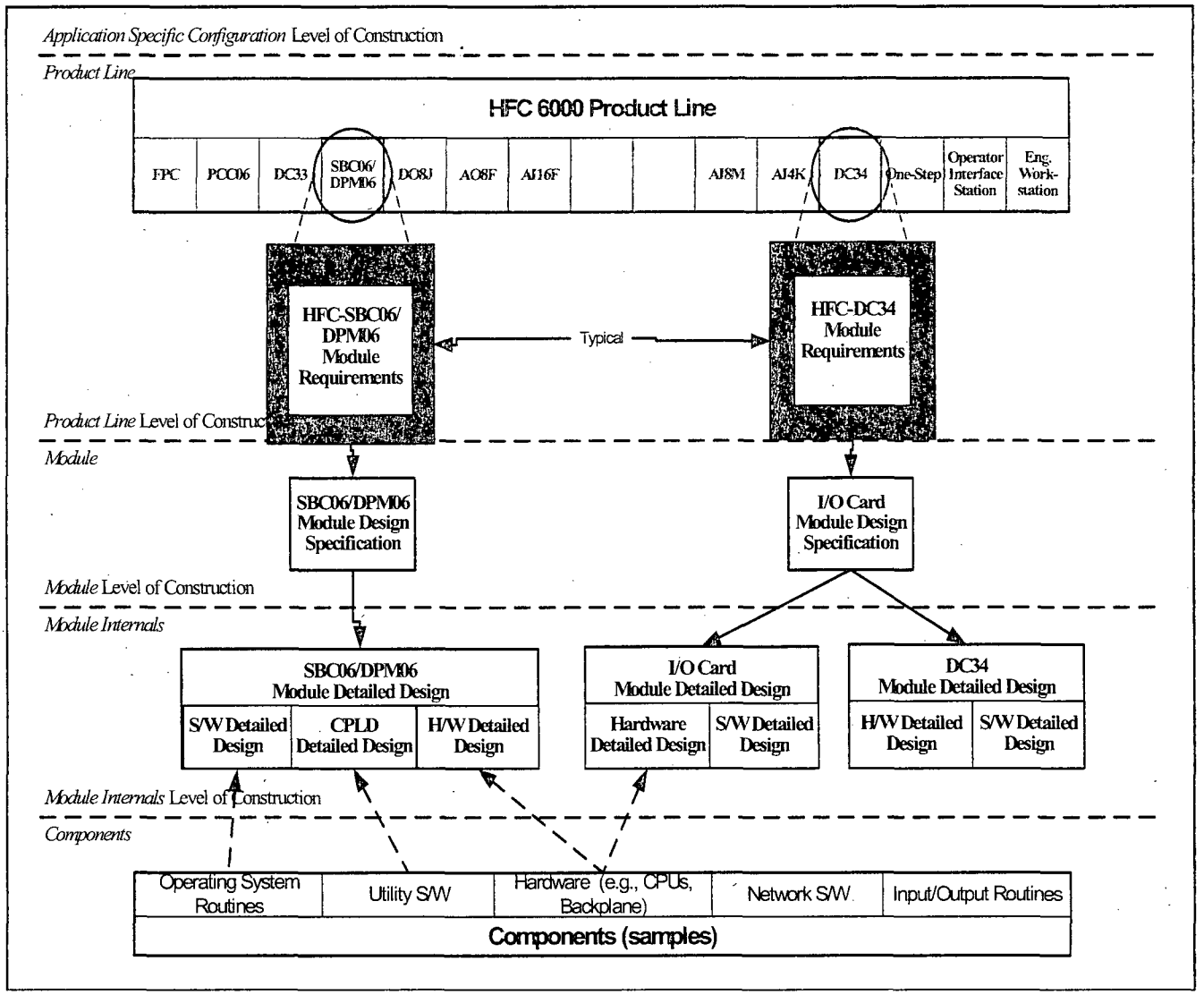

Figure 1 - HFC-6000 Documentation Layers

3. Product Line Requirements Specification

The Product Line Requirements Specification is the top level documentation for the HFC-6000 product line. It provides descriptions of product concept based on marketing and engineering input, requirements that apply to all modules or class of modules and product architecture overview with modules shown in block diagram. It also include an appendix with each defining requirements for a single module.

4. Module Design Specifications

The Module Design Specifications provides descriptions of architecture and overview information of an HFC module, from hardware, software or logic aspects. It also includes functional description and module constraints. Since all the I/O modules share the same hardware and software architecture and have many similar functions and designs, only one Module Design Document is provided for all the I/O modules.

5. Module Detailed Design Specifications

The Module Detailed Design Specification provides descriptions of detailed design and implementation information. A Module Detailed Design Document of HFC-6000 I/O Modules covers the common detailed features and implementation methods of all I/O modules. The descriptions of specific I/O function and implementation of each individual I/O module are provided in a Module Detailed Design Document for each I/O module.

6. Component Design Specification

Component Design Specifications provides descriptions of architecture, interface and implementation information of independent HFC components, such as hardware component, communication protocol, software library, common glossary, etc.

7. Test Procedures

Test Procedures provide detailed descriptions of test environment set up information, test sequences and acceptance criteria from test results. For each module, there should be a separate test procedure for prototype testing and production functional testing. The prototype testing tries to validate the functionality and performance of different component and circuitry of the module in details. The production functional testing aims at validating the basic functions of the module.

8. User's Guide

User's Guides are provided for user interface modules, system installation, maintenance and trouble shooting, etc. Some of the User's Guides are standard for different HFC systems and some are specific to HFC-6000 product line.

Appendix A. List of Documents for HFC-6000 Product Line

No.	Level	Document No	Name
1-1	Map	PP901-000-02	HFC-6000 Product Line Document Map
1-2	Marketing	ML901-000-01	HFC-6000 Control System Catalogue
1-3	Top	RS901-000-01	HFC-6000 Product Line Requirements Specification
2-1	Module	MS901-000-01	HFC-SBC06 Module Design Specification
2-2		MS901-000-02	HFC-6000 I/O Card Module Design Specification
2-3		MS901-000-03	HFC-PCC06 Card Module Design Specification
3-1	Module Details	DS901-000-01	HFC-SBC06 Module Detailed Design Specification
3-2		DS901-000-02	HFC-6000 I/O Card Module Detailed Design Specification
3-3		DS901-000-03	HFC-DO8J Card Module Detailed Design Specification
3-4		DS901-000-04	HFC-DI16I Module Detailed Design Specification
3-5		DS901-000-05	HFC-DC33 Module Detailed Design Specification
3-6		DS901-000-06	HFC-DC34 Module Detailed Design Specification
3-7		DS901-000-07	HFC-AI16F Module Detailed Design Specification
3-8		DS901-000-08	HFC-AO8F Module Detailed Design Specification
3-9		DS901-000-11	HFC-AI8M Module Detailed Design Specification
3-10		DS901-000-12	HFC-AI4K Module Detailed Design Specification
3-11		DS901-000-21	FPC Module Software Design Specification
4-1	Components	DS001-000-01	Operating System Component Design Specification
4-2		DS001-000-02	Equation Interpreter Component Design specification
4-3		DS001-000-03	CQ4 Component Design Specification
4-4		DS001-000-06	System Component Design Specification
4-5		DS001-000-07	Job Component Design Specification
4-6		DS001-000-08	Failover Mechanism Component Design Specification
4-7		DS002-000-01	C-Link Protocol Component Design Specification
4-8		DS002-000-02	ICL Protocol Component Design Specification
4-9		DS002-000-03	UCP Protocol Component Design Specification
4-10		DS004-000-01	HFC Common Glossary
5-1	Test Procedure	TS001-000-01	Component Test Procedure
5-2		TS901-000-01	HFC-PCC06 Detailed Prototype Test Procedure
5-3		TS901-000-02	HFC-SBC06/HFC-DPM06 Detailed Prototype Test Procedure
5-4		TS901-000-04	HFC-AI16F Detailed Prototype Test Procedure
5-5		TS901-000-05	HFC-AI4K Detailed Prototype Test Procedure
5-6		TS901-000-07	HFC-AI8M Detailed Prototype Test Procedure
5-7		TS901-000-08	HFC-AO8F Detailed Prototype Test Procedure

No.	Level	Document No	Name
5-8		TS901-000-09	HFC-DC33 Detailed Prototype Test Procedure
5-9		TS901-000-10	HFC-DC34 Detailed Prototype Test Procedure
5-10		TS901-000-11	HFC-DI16I Detailed Prototype Test Procedure
5-11		TS901-000-12	HFC-DO8J Detailed Prototype Test Procedure
5-12		TS901-000-14	HFC-PCC06 Detailed Test Procedure
5-13		TS901-000-16	HFC-BPC01-08 Prototype Test Procedure
5-14		TS901-000-17	HFC-BPC01-08 Test Procedure
6-1	User Manual	UG004-000-01	EWS User's Guide
6-2		UG004-000-02	CRT User's Guide
6-3		UG004-000-03	HAS User's Guide
6-4		UG004-000-04	One-Step Software User's Guide
6-5		UG004-000-05	Software Installation User's Guide
6-6		UG004-000-06	HIFR User's Guide
6-7		UG004-000-07	Site Planning and Installation Guide
6-8		UG004-000-08	Control System Maintenance Manual
6-9		UG004-000-09	I/O Simulation Manual
7-1	Review Report	RR901-000-01	HFC-6000 Failure Modes and Effects Analysis
7-2		RR901-000-04	HFC-6000 Availability and Reliability Analysis Report
7-3		RR901-000-10	HFC-6000 EPRI 107330 Requirements Compliance Traceability Matrix

ATTACHMENT 7.1

Project Quality Plan

HF Controls, Corporation			
Client: **HFC**	Project No.: **ERD-111**	No.: **N/A**	PQP. No.: **2003-005** / Rev.: **D**
Purchase Spec. No. / Description: **N/A** Rev.: **0**			

NON-PROPRIETARY

Project Quality Plan

HFC-6000 Product Line Qualification Testing

Consisting of:

Item 1- System Chassis

Item 2 - Control Switch Modules

Item 3 - M/A Stations

Item 4 - Prefabricated Cable

Item 5 -Quadruplex Fiber Optic Cables and Connectors

Item 6 – Operator Interface Subsystem (OIS), Maintenance Subsystem (MSS), Color Printer for OIS and MSS and Other Components or Equipment Necessary to Complete the System

Item 7 – Seismic Testing

Item 8 – Environmental Testing

Item 9 – EMI/RFI Testing

Item 10 – ESD testing

Item 11 – Component Classification

Rev	Date	Revision Description	Prepared By	Reviewed By	Approved By
D	10/28/03	Updated Component Classification	John Stevens	Jonathan Taylor	C.E. Fisher
C	10/7/03	Updated per actual functions	John Stevens	Jonathan Taylor	C.E. Fisher
1	7/23/03	2nd Submittal Added item 11	John Stevens	Jonathan Taylor	C.E. Fisher
0	7/15/03	1st Submittal	John Stevens	Jonathan Taylor	C.E. Fisher

Control Copy Distribution:

QA Manager
Manufacturing Manager
Project Manager

PQP: **2003-005** / Rev.: **D**

1. **Project Definition/Technical Requirements (Describe the work that is to be done identifying, where applicable, the following elements):**

   1) Project objectives – HFC's product developed from the AFS and ECS lines is called HFC-6000. HFC's new product will be manufactured and qualification tests will be performed for use in safety related applications in the US and globally.

   2) Major tasks – Manufacture four chassis for qualification testing, and four spare chassis as a backup for extra hardware.

   3) Major deliverables – System chassis, control switch modules, M/A station, cables, OIS, FPD, and miscellaneous hardware.

   4) Customer specific requirements – N/A

   5) Project schedule with anticipated end date – Testing dates are the beginning of September 2003.

2. **Quality Requirements (Check each item that is applicable)**

   ☒ NQA-1 ☐ ISO 9001 ☒ 10CFR21 (Nuclear Safety Related)

   ☒ All project activities must comply with quality system requirements

   ☐ The following tasks must comply with quality system requirements

   a. N/A

   ☐ Customer specific quality requirements
   a. N/A

3. **HFC Quality System Applicability**

•Mark QA Manual Sections Applicable to Project:

☒ **Section 1.0**	☒ **Section 6.0**	☒ **Section 11.0**	☒ **Section 16.0**	☐ **Section 21.1**
☒ **Section 2.0**	☒ **Section 7.0**	☒ **Section 12.0**	☒ **Section 17.0**	
☒ **Section 3.0**	☒ **Section 8.0**	☒ **Section 13.0**	☒ **Section 18.0**	
☒ **Section 4.0**	☒ **Section 9.0**	☒ **Section 14.0**	☐ **Section 19.0**	
☒ **Section 5.0**	☒ **Section 10.0**	☒ **Section 15.0**	☐ **Section 20.0**	

•Mark QA Procedures to be implemented by Project Team:

☒ **QPP 1.2**	☒ **QPP 5.2**	☒ **QPP 11.1**	☒ **QPP 16.3**	☐ **Section 21.1**
☒ **QPP 2.1**	☒ **QPP 6.1**	☒ **QPP 12.1**	☒ **QPP 17.1**	
☒ **QPP 2.2**	☒ **QPP 7.1**	☒ **QPP 13.1**	☒ **QPP 17.2**	
☒ **QPP 3.1**	☒ **QPP 7.2**	☒ **QPP 14.1**	☒ **QPP 18.1**	
☒ **QPP 4.1**	☒ **QPP 8.1**	☒ **QPP 16.1**	☒ **QPP 19.1**	
☒ **QPP 5.1**	☒ **QPP 10.1**	☒ **QPP 16.2**	☐ **QPP 20.1**	

4. **Work Instructions: (Identify work instructions required to support work performed under HFC's Quality Program)**
   a. **Project work will comply with all Work Instructions that implement the above referenced QPPs.**

5. **Project Team: (Identify project team members by name and title or role; use asterisk to show individuals authorized to do document review and approval. Project specific training identified.)**
   a. **See Product Development Plan (VV0401)**

6. **Vendors: (If applicable, list vendors supporting project activities, or expected recipients of a procurement document.)**
   a. **Weschler**
   b. **SVTronics**
   c. **AssembleTech**
   (For More complete list see QSL)

7. **HFC Assigned Hold Points; Source, Receipt, In-Process and Final Inspections: (If applicable, include hold points at key milestones in the project needing Project Manager approval. Project Manager should consider the cost of source inspections when budgeting project costs.)**

8. **Other Items to be considered:**

9. **HFC Project Quality Documents and Records: Identify the types of quality records that will be generated by the project, which quality records require QA Manager review and approval, and which records require customer approval.**

See next page:

Project Record	Applicable to Project		Review, Approval of Vendor Docs		QA Manager Review and Approval		Customer Approval		Retention Time
	Yes	No	Yes	No	Yes	No	Yes	No	
Drawings	X		X		X			X	Permanent
Bill of Materials	X				X			X	Permanent
Design Specifications	X		X			X		X	7 years
Software Requirements Specification	X					X		X	7 years
Software V & V Reports	X				X			X	Permanent
Software V & V Plans	X				X			X	7 years
Software Requirements Specification	X				X			X	Permanent
User Manual	X		X			X		X	Permanent
Analysis Package Documentation	X					X		X	7 years
Receipt, In-process and/or Final Inspections	X		X		X			X	Permanent
Commercial Grade Dedication Plans	X		X			X		X	Permanent
Test Documentation	X		X		X			X	Permanent
Project Training Records	X					X		X	7 years
Project Quality Plan	X				X			X	Permanent
M&TE Calibration Records	X					X		X	7 years
HFC Hold Point Releases	X				X			X	7 years
Vendor Supplied Documentation/HFC Acceptances	X				X			X	7 years
System Configuration Management Plan:	X				X			X	

(Boxes left blank means it is not applicable)

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 1 - System Chassis		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	HFC Inspection Point		Buyer Inspection Point		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Dimensional / Visual Inspection	Eng. Dwg. 700709-Series	H				Receiving Inspection Report	
2.	In-Process Inspection	Eng. Dwg. 700709-Series	W				Process Control Sheet	
3.	Surface Preparation and Coating:	Eng. Spec. N/A					Receiving Inspection Report	
4.	Assemble & Install Components	Eng. Dwg. 700709-Series	W				Process Control Sheet	
5.	Terminate Internal Wiring	Eng. Dwg. 700916-01	W				Process Control Sheet	
6.	Pre-Test Inspection	Eng. Dwg. 700909-01	H				Process Control Sheet	
7.	Burn-in Test	TP0410	W				Test Report	
8.	Application Object Test	TN0402	W				Test Report	
9.	Setup and Checkout Test	TP0401	W				Test Report	
10.	Operability Test	TP0402	W				Test Report	
11.	Prudence Test	TP0403	W				Test Report	
12.	Isolation Test	TP0411	W				Test Report	
13.								
14.								

Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 1 - System Chassis		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	HFC Inspection Point	Buyer Inspection Point	Quality Verification Document	Remarks
15.	Final Inspection	Eng. Dwg. 700700 Series	R		Inspection Report	
16.	Review and Sign-off of QVDL		H		QVDL	
17.	Release For Shipment		R			
18.	Packing & Crating Inspection (Shipment to testing Lab.)		W			
Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:				

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 2 - Control Switch Modules		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	Seller Inspection Point		Buyer Inspection Point (N/A)		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Receiving Inspection	Eng. Dwg. Later	W				Receiving Inspection Report	
2.	In-Process Inspection	Eng. Dwg. Later	W				Process Control Sheet	
3.	Surface Preparation and Coating:	Eng. Spec. 700040-03, 04	W				Receiving Inspection Report	
4.	Assemble & Install Components	Eng. Dwg. 700500 series	W				Process Control Sheet	
5.	Terminate Internal Wiring	Eng. Dwg. 700500 Series	W				Process Control Sheet	
6.	Pre-Test Inspection	Eng. Dwg. 700500 Series	W				Process Control Sheet	
7.	Final Inspection	Eng. Dwg. 700500 Series	H				Process Control Sheet	
8.	Review and Sign-off of QVDL		H				QVDL	
9.	Release For Shipment		W					
10.	Packing & Crating Inspection		W					

Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 3 - M/A Stations		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	Seller Inspection Point		Buyer Inspection Point (N/A)		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Receiving Inspection	Eng. Dwg. Later	W				Receiving Inspection Report	
2.	In-Process Inspection	Eng. Dwg. Later						
3.	Final Inspection	Eng. Dwg. 700530-00	H				Receiving Inspection Report	
4.	Review and Sign-off of QVDL		H				QVDL	
5.	Release For Shipment		H					
6.	Packing & Crating Inspection		W					

Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: QPP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 4 - Prefabricated Cable		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	Seller Inspection Point		Buyer Inspection Point (N/A)		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Receiving Inspection	Eng. Dwg. Later	W				Receiving Inspection Report	
2.	In-Process Inspection	Eng. Dwg. Later	R					
3.	Continuity Test	Eng. Dwg. Later	W				Test Report	
4.	Final Inspection	Eng. Dwg. 700530-00	H				Receiving Inspection Report	
5.	Review and Sign-off of QVD		H				QVDL	
6.	Release For Shipment		W					
7.	Packing Inspection		W					

Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 5 - Quadruplex Fiber Optic Cables and Connectors		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	Seller Inspection Point		Buyer Inspection Point (N/A)		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Receiving Inspection	Eng. Dwg. Later	W				Receiving Inspection Report	
2.	In-Process Inspection	Eng. Dwg. Later						
3.	Final Inspection	Eng. Dwg. 700530-00	H				Receiving Inspection Report	
4.	Review and Sign-off of QVDL		H				QVDL	
5.	Release For Shipment		W					
6.	Packing Crating Inspection		W					

Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 6 – Operator Interface Subsystem (OIS), Maintenance Subsystem (MSS), Color Printer for OIS and MSS and Other Components or Equipment		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	HFC Inspection Point		Buyer Inspection Point (N/A)		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Receiving Inspection	Eng. Dwg. Later	W				Receiving Inspection Report	
2.	In-Process Inspection	Eng. Dwg. Later						
3.	Final Inspection	Eng. Dwg. 700530-00	H				Receiving Inspection Report	
4.	Review and Sign-off of QVDL		H				QVDL	
5.	Release For Shipment		W					
6.	Packing & Crating Inspection		W					
Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:						

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 7 – Seismic Testing		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	HFC Inspection Point		Buyer Inspection Point (N/A)		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Receiving Inspection	Eng. Dwg. Later	W				Receiving Inspection Report	
2.	Installation Process	Eng. Dwg. 700912-01	W					
3.	Pre-Test Process	TP0405	H				Test Report	
4.	Environmental Testing	TP0405	W				Test Report	
5.	Post-Test Process	TP0405	W				Test Report	
6.	Last Test Return to HFC		W					
Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:						

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 8 – Environmental Testing		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	HFC Inspection Point		Buyer Inspection Point (N/A)		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Receiving Inspection	Eng. Dwg. Later	W				Receiving Inspection Report	
2.	Installation Process	Eng. Dwg. 700912-01	W					
3.	Pre-Test Process	TP0404	H				Test Report	
4.	Environmental Testing	TP0404	W				Test Report	
5.	Post-Test Process	TP0404	W				Test Report	
6.	Last Test Return to HFC		W					

Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 9 – EMI/RFI Testing		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	HFC Inspection Point		Buyer Inspection Point (N/A)		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Receiving Inspection	Eng. Dwg. Later	W				Receiving Inspection Report	
2.	Installation Process	Eng. Dwg. 700912-01	W					
3.	Pre-Test Process	TP0407	H				Test Report	
4.	EMI/RFI Testing	TP0407	W				Test Report	
5.	Post-Test Process	TP0407	W				Test Report	
6.	Last Test Return to HFC		W					

Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 10 – ESD Testing		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	HFC Inspection Point		Buyer Inspection Point (N/A)		Quality Verification Document	Remarks
			Point	Verify	Point	Verify		
1.	Receiving Inspection	Eng. Dwg. Later	W				Receiving Inspection Report	
2.	Installation Process	Eng. Dwg. 700912-01	W					
3.	Pre-Test Process	TP0409	H				Test Report	
4.	ESD Testing	TP0409	W				Test Report	
5.	Post-Test Process	TP0409	W				Test Report	
6.	Last Test Return to HFC		W					

Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:

Client: HFC	Job No: ERD-111	PQP. No. / Rev.: PQP – 2003-005, Rev D
Purchase Spec. No./Description: N/A		
Component: Item 11 – Component Classification		Sequence of Fabrication

No.	Description of Operation	Ref. Doc.	HFC Inspection Point		Buyer Inspection Point (N/A)		CGE Verification Plan	Remarks
			Point	Verify	Point	Verify		
	Safety Related Items							
1.	Power Supplies	90445-10 90445-11	R				CGE-00056	
2.	Connector DIN 41612	69900-22	R				CGE-00057	
3.	Fastener	91505-07	R				CGE-00058	
4.	PCB Cards	700912-02	R				CGE-00046	
5.	Chassis	700709-01 700709-02	R				TBD	
6.	Staco Switch	78907-10 78907-11	R				CGE-00002	
7.	Connector F/O	88431-53	R				CGE-00005	
8.	Connector DB9	77025-14	R				CGE-00009	
9.	F/O Cable	89647-12 thru -17	R				CGE-00012	
10.	6 Cond. Cable	89647-03 thru -07	R				CGE-00013	
11.	Connector DB9 45 deg angle	74784-04	R				CGE-00019	
12	M/A Station	77752-00	R				CGE-00047	
13	Terminal Strips	6990067, 6990062, 6990085 & 6990089	R				CGE-00040	
	Non-Safety Related Items							
1.	All remaining items	N/A					N/A	

Insp. Pts.	W: Witness Pt. H: Hold Pt. R: Doc. Rev.	Notes: Project Manager:

DOOSAN

HF Controls

NON-PROPRIETARY

QUALITY ASSURANCE PROGRAM MANUAL

Revision: **G**

Effective Date: **10/3/07**

Prepared By: P. Evans

Reviewed By: J. Stevens

Reviewed By: J. Ingram

Reviewed By: G. Reding

Approved By: A. Hsu

HFC QUALITY ASSURANCE PROGRAM MANUAL

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Policy Statement

This Quality Assurance Program Manual (QAPM) describes the Quality Assurance Program at HF Controls (HFC). The program is designed to provide administrative measures and procedures necessary for assuring that all HFC hardware and software products as well as any services meet or exceed customer requirements and applicable industry codes and standards. This Quality Program is designed to comply with ANSI/ASME NQA-1 2004; *Quality Assurance Requirements for Nuclear Facilities Applications*, ANSI/ASME NQA-1 - 2000 *Quality Assurance Requirements for Nuclear Facility* Applications with Addenda, 10 CFR 50 Appendix B; "Quality Assurance Criteria for Nuclear Power Plants and Fuel Reprocessing Plants", ISO 9001:2000, and 10CFR Part 21.

HFC's specific goals and objectives are to provide to our customers: 1) Quality products with no defects or failures, 2) Products delivered on or prior to the promised date. HFC also commits to continually broaden the knowledge base of our employees and services within a safe work environment.

The requirements of this manual shall apply to all activities affecting the quality of products and services provided and performed by HFC. HFC personnel at every level of the organization are required to fully support HFC's QA Program, achieve a high level of excellence through the application of proven technology in their respective areas of responsibility, and promote an atmosphere of continuous improvement.

See Original in File

Allen Hsu
President

See Original in File

Jame F. Ingram
QA Director

Section 1.0 - Organization

HF Controls (HFC) Corporation designs controls systems for customers in the form of Projects, provides warranty and non-warranty work on nonfunctioning items, on site service and provides spare parts when requested. See Attachment 1 for a flow chart description of the interaction between the processes of the quality management system. HFC has established and is maintaining a Quality Program for products delivered to our customers and services performed for our customers. Although authority for development and execution of the program may, on occasion, be delegated to other parties, such as consultants or contractors, HFC retains overall program responsibility. Internal and external interface responsibilities have been established in implementing procedures.

The HFC QA Director has the responsibility for establishing the Quality Program and verifying that activities affecting the quality of deliverables are performed in accordance with this program. By reporting directly to the President, HFC, the QA Director is afforded sufficient authority and organizational freedom, including independence from the cost and schedule impacts of required quality assurance actions, to identify quality problems; to initiate, recommend, or provide solutions to quality problems; and to verify implementation of solutions to quality problems. The QA Director has the ability to stop work if deemed necessary. All employees share the same responsibility and authority as the QA Manager to identify quality problems; to initiate and provide solutions to quality problems; to verify implementation; and to resolve deficiencies that affect quality.

The QA Director is the HFC Management Representative and is responsible for ensuring that this quality system is maintained, understood and implemented at all levels of the organization. The Management Representative is also responsible for reporting on the performance of the Quality System to executive management for review and improvement.

The HFC Quality Policy is affirmed in a statement at the front of this document. All HFC personnel have been made aware of this policy and annually the Policy Statement shall be reviewed by management and disseminated throughout the organization.

The organizational structure, functional responsibilities, level of authority and lines of communication for activities affecting quality are defined in an implementing procedure. In the event that any individual in the organization is absent or otherwise unavailable to perform functions or responsibilities, those functions and responsibilities may be performed by a superior or delegated to a qualified subordinate within the organization.

The President of HFC, has assigned trained personnel to manage, perform and verify activities affecting quality. Personnel assigned these tasks are qualified on the basis of experience and/or training. All employees are responsible for the quality of the products and services under their control and for following procedural requirements during all processes in which they are involved.

A formal management review of the quality system will be performed annually, at a minimum, to ensure its continuing suitability and effectiveness in satisfying HFC's business policies and objectives. This management review shall evaluate, as a minimum, the results of internal and applicable external audits, corrective and preventive actions status, customer feedback, product nonconformances, Returned Material Authorizations (RMA), follow-up actions from previous meetings, changes that could effect the quality management system, training requirements, recommendation for improvement and resource needs. Records of the management review meeting and associated completed action items shall be maintained in accordance with documented procedures.

Where more than one organization is involved in execution of the section, the responsibility and authority of each organization shall be clearly established and documented.

HFC management shall insure that adequate facilities necessary for employees to perform their assigned tasks are provided. Test equipment and software used shall be appropriately certified and identified as appropriate. Services necessary to meet contract requirements shall be provided.

Implementing Procedures

QPP 1.1, "Management Review"

QPP 1.2, "Organizational Responsibilities"

QPP 17.1, "Quality Records"

Section 2.0 - Quality Assurance Program

Policy statements that define and establish the HFC Quality Assurance Program are in each section of this manual.

The HFC Quality Assurance Program shall apply to all related activities as specifically defined in the applicable Quality Plan (Project or Nuclear Spare Parts). Both plans define the scope and implementation of the HFC Quality Assurance Program to satisfy specific customer requirements.

The HFC Quality Assurance Program is implemented through Quality Procedures, Quality Plans, Process Control Sheets and Work Instructions. Quality Assurance Forms are used to capture objective evidence to demonstrate effective implementation.

The HFC Quality Assurance Program provides assurance that activities affecting quality are documented within controlled systems, and accomplished in accordance with written procedures, instructions and/or drawings.

The HFC Quality Assurance Program provides for indoctrination, training, and qualification (when required) of personnel who manage, test, perform or verify activities affecting quality as necessary to assure that suitable proficiency is achieved and maintained. Methods are in place for the qualification of Inspection and Test and Auditor personnel. Training needs other than those defined herein shall be identified and documented during the annual management review of the quality system. Appropriate records of training shall be maintained as quality records.

The status, adequacy, and effectiveness of this Quality Assurance Program in meeting HFC business and quality objectives, as well as compliance to the aforementioned requirements shall be audited annually with the results reported to HFC management.

The HFC Quality Assurance Program shall be reviewed annually by the President of HFC, and his staff, and revised as necessary in order to ensure continuing compliance with applicable codes, standards, regulations and customer requirements. The review should include how to improve the Quality Assurance Program and its influence on organizational effectiveness and efficiency.

Implementing Procedures

QPP 1.1, "Management Review"

QPP 2.1, "Quality Plans"

QPP 2.2, "General Indoctrination and Training"

QPP 16.1, "Corrective Action Program"

QPP 16.2, "Customer Feedback"

QPP 17.1, "Quality Records"

QPP 18.1, "Audits"

Section 3.0 - Design Control

HFC shall establish and maintain documented procedures to ensure that applicable regulations, codes, standards, and customer requirements are translated into design documents, procedures, and/or instructions. These documents shall include provisions to assure that appropriate quality standards are specified and included in design documents and that deviations from defined requirements are controlled.

Product Development Plans shall be initiated for each new product design and development activity and shall describe these activities as well as the responsibility for their implementation. The design and development activities shall be assigned to qualified personnel equipped with adequate resources. The Product Development Plan and associated design documents shall be updated as the design evolves.

Organizational and technical interfaces between different groups that input into the design process are defined in the Product Development Plan. All design information necessary to ensure satisfaction of customer requirements shall be documented, transmitted, when applicable, and regularly reviewed.

The design control program is established and implemented to assure that the activities associated with the design of systems, components, structures, and equipment and modifications thereto, are executed in a planned, controlled, and orderly manner. The program includes provisions to control design inputs, processes, outputs, changes, interfaces, records, and organizational interfaces.

Design input requirements, relating to our products, shall be established, documented and their selection reviewed and approved for adequacy. Design input shall take into account the requirements in customer orders. Design requirements shall be objective, quantitative, or capable of unambiguous determination of implementation. Incomplete, ambiguous, or conflicting requirements shall be resolved with those responsible for imposing the requirements. Changes from approved design inputs, including the reasons for the changes, shall be identified, approved, documented and controlled.

Design output shall be documented and expressed in terms that can be verified against design input requirements and validated. Individuals or groups other than those that performed the original design shall review design output documents. Design output shall contain or make reference to acceptance criteria.

Independent design reviews shall occur at prescribed stages within the design process. Participants at each design review shall include, when necessary, representatives of all functions concerned with the design stage being reviewed. Records of design reviews shall be maintained.

Design verifications shall include design reviews, alternate calculations, qualification tests or a combination of methods in accordance with approved procedures. Design verifications shall be performed in accordance with approved procedures, performed prior to release for procurement, manufacturing, or to another organization for use, to ensure that the design output meets the design input requirements. Records of design verifications shall be maintained. In cases where this timing cannot be met, the unverified portion of the design shall be identified and controlled.

Independent design validations shall be performed to ensure that products conform to user needs and/or requirements. Records of design validations shall be maintained.

Design Analyses shall be performed in a planned controlled and documented manner. They shall be sufficiently detailed as to purpose, method, assumptions, design input, references and units. Methods such as computer programs and calculations are described and controlled. Qualification testing shall demonstrate adequacy of performance under conditions that simulate the most adverse design conditions.

Design changes, shop changes, modifications and nonconforming items dispositioned use-as-is or repair shall be justified and shall be subject to design control measures commensurate with those applied to the original design. Measures have been established to ensure that design changes are reviewed by the same affected group or organization that reviewed and approved the original design.

Design documents, including revisions, shall be reviewed, approved, released, distributed, and controlled in accordance with prescribed procedures and/or instructions.

Procedures have been established to identify critical characteristics, dedicate and utilize a Commercial Grade Item or Software in nuclear projects.

Implementing Procedures

QPP 3.1, "Design Control"

QPP 3.2, "System Lifecycle and Verification and Validation Program"

QPP 5.1, "Review and Approval of Documents"

QPP 6.1, "Control and Distribution of Documents"

QPP 17.1, "Quality Records"

QPP 7.2, "Commercial Grade Item Evaluation"

QPP 7.3, "Commercial Grade Software Evaluation"

Section 4.0 - Procurement Document Control

HFC shall establish and maintain documented procedures to ensure that purchased products and services conform to specified requirements.

Applicable technical, regulatory, administrative, reporting and quality requirements (e.g., specifications, codes, standards, tests, inspections, special processes, and 10CFR Part 21) are invoked for procurement of items and services, as applicable.

Review of procurement document requirements has been specified in procedures. Responsible organizations shall review the procurement documents to ensure conformance and inclusion of applicable technical and quality requirements prior to release.

The Quality Assurance Program includes provision for ensuring that documented evidence of an item's conformance to procurement requirements is available before the item is placed in service or used, unless otherwise specified in procedures.

The Quality Assurance Program ensures that changes to procurement documents receive the same level of control as the original document.

The Quality Assurance Program ensures that procurement documents provide for defining the scope work, technical requirements, quality assurance program requirements required by the supplier, the right to access a supplier's facility and their records for the purpose of inspection and audits by HFControls, HFC's customers, or a designated representative, documentation to be submitted, reporting and approving a nonconformance and identification of spare parts.

When contractually specified, HFC customers, or their agents, shall be afforded the right to verify, at HFC's facility or HFC's suppliers facilities, that subcontracted product conforms to specified requirements.

HFC shall not use customer verification as a means of assuring supplier conformance to procurement requirements nor shall it absolve our responsibility to provide acceptable product to our customers.

Implementing Procedures

QPP 4.1, "Review, Approval, and Issuance of Purchase Orders"

QPP 10.1, "Receipt, In-process, and Final Inspections"

QPP 17.1, "Quality Records"

Section 5.0 - Instruction, Procedures, and Drawings

HFC shall establish and maintain a quality system that assures activities that affect quality are prescribed by documented procedures, instructions, and drawings and shall be accomplished in accordance with these procedures, instructions, and drawings.

Procedures, instructions, and drawings shall include, as appropriate, quantitative or qualitative acceptance criteria for determining that activities affecting quality have been satisfactorily accomplished.

Procedures, instructions, and drawings shall be reviewed and approved for adequacy by authorized personnel prior to use. Changes to these documents shall be reviewed and approved by the same organization that performed the original review and approval. The designated organization shall have access to pertinent background information upon which to base their review and approval.

Changes to quality documents shall be identified in the document or the appropriate attachments.

Implementing Procedures

QPP 5.1, "Review and Approval of Quality Documents"

QPP 5.2, "Preparation of Procedures and Instructions"

Section 6.0 - Document Control

Procedures are established by HFC to control the issuance of documents, such as instructions, procedures, drawings, and data, including changes thereto, which prescribe activities affecting quality.

These procedures are established to identify documents and data, including changes that are be controlled along with their specified distribution, the identification of assignment of responsibility for preparing, reviewing, approving and issuing of these documents and data, and for the review of these documents and data for adequacy, completeness, and correctness prior to approved and issuance.

Measures are established requiring the same organizations that performed the original review and approval to review and approve changes to documents unless another responsible organization is designated.

New and revised controlled documents are distributed in accordance with approved procedures. Superseded documents are removed from the work area. Any obsolete documents retained for legal and/or knowledge-preservation shall be suitably identified.

Methods have been established to ensure that the current revision status of documents is identified and readily available to preclude the use of invalid and/or obsolete documents.

Documents of external origin, such as standards and customer documents, shall be controlled.

Implementing Procedures

QPP 5.1, "Review and Approval of Documents"

QPP 6.1, "Control and Distribution of Documents"

Section 7.0 - Control of Purchased Items and Services

HFC shall establish and maintain documented procedures and processes to ensure that the purchased product conforms to procurement document requirements. A product may include a service, hardware, spare parts, software, or a combination thereof.

The quality assurance programs of NQA-1 vendors shall be evaluated by audit. Audits are performed in accordance with approved procedures. ISO 9000 vendors may be evaluated by obtaining a copy of their ISO Certificate. Vendors providing commercial grade products/services used in safety-related applications shall be evaluated, when applicable, in accordance with approved procedures. Vendors listed on the HFC Qualified Suppliers List (QSL) shall be evaluated at intervals consistent with the importance and complexity of the product. The use of customer-approved vendors is allowable. Documented evidence of customer-designated use shall be maintained in accordance with approved procedures.

Procedures have been established noting the requirements for procurement, inspection, and acceptance of commercial grade products that may be used by HFC.

Procedures have been established to define the processes for accepting product through source verification. Source verification arrangements and the method of product release shall be defined in procurement documents.

Methods have been established and documented for the disposition of item(s) that do not conform to the procurement document.

For products provided directly to HFC, implementing procedures shall define requirements for receipt inspection to assure that purchased items or services conform to procurement documents. Drop shipment from HFC's vendor directly to HFC's customer must be evaluated and authorized by the HFC QA Manager / Designee.

Procedures have been established to perform Bid evaluations to determine the extent of conformance to the procurement document.

Measures have been established to ensure that supplier generated documents are controlled, handled, and approved.

Methods have been established for the acceptance of services such as third party inspection, engineering and consulting services etc. These methods include a) technical verification of data produced, b) surveillance or audit of the activity c) review of objective evidence for conformance to the procurement document requirements.

Measures have been established to control changes to procurement documents.

When required by procurement documents, HFC, or a designated agent, shall verify the purchased product at the vendor's facility.

Records of acceptable suppliers shall be maintained as quality records.

HFC has established documented methods with applicable suppliers for the disposition of items and services that do not conform to procurement documentation requirements.

Implementing Procedures

QPP 7.1, "Supplier Selection, Qualification and Re-Evaluation"

QPP 7.2, "Commercial Grade Item Evaluation"

QPP 7.3, "Commercial Grade Software Evaluation"

QPP 17.1, "Quality Records"

QPP 4.1, "Review, Approval and Issuance of Purchase Orders"

Section 8.0 - Identification and Control of Items

HFC shall establish and maintain documented procedures to ensure that materials, parts, and components used in quality-affecting activities, including those items supplied by HFC customers or returned for rework, are properly identified and controlled.

These procedures shall ensure that applicable materials, parts, and components, including partially fabricated assemblies, maintain their identification from initial receipt and fabrication up to installation and use. Materials, parts, and components are controlled to prevent loss, damage, or deterioration, and to prevent the inadvertent use of incorrect or defective materials, parts, and components.

Physical marking shall be utilized to the maximum extent possible; however if it is not impractical then physical separation, procedural controls or other appropriate means shall be employed. When specified, specific identification and traceability requirements will be controlled. All products procured or assembled by HFC shall have their identification and traceability documented. Records of this activity shall be maintained as quality records.

Markings used for identification are clear and legible when utilized and do not detrimentally effect the function of the material, part, and component. If required, markings shall be transferred to each part of the identified material, part, and component when subdivided. The identification shall be readable upon surface treatment or coating unless other means of identification are substituted.

HFC does not produce or assemble materials, parts, and components that required traceability from codes, standards, or specifications.

Material or equipment purchased by HFC shall be inspected per applicable procedures or instructions. Inspection results are documented and acceptable material is appropriately marked.

Items having limited shelf life are controlled to prevent their inadvertent use or installation.

Methods have been established to control material, part, and component identification and marking consistent with planned duration and conditions of storage. These methods shall ensure that material, part, and component identification and marking are placed if damaged, deteriorated, aged or mishandled.

Implementing Procedures

QPP 8.1, "Identification and Control of Materials, Parts, and Components"

QPP 16.1, "Corrective Action Program"

QPP 20.1, "Servicing and Customer Supplied Products"

Section 9.0 - Control of Processes

HFC shall establish and maintain documented procedures to ensure processes that directly affect quality are carried out under controlled conditions.

The Quality Plan (QP) is the mechanism in which all quality-affecting project activities or nuclear spare parts orders are described and controlled. The QP defines the quality assurance program controls applicable to the project work scope, and identifies the project team, deliverables, applicable quality records that are created by the project, and QA and customer witness and hold points. The QP is reviewed, approved, and controlled in accordance with approved procedures.

HFC does not use or maintain any quality-affecting equipment that requires periodic preventive maintenance nor does HFC perform special processes such as welding and heat-treating etcetera that requires qualified personnel using qualified procedure.

A Shop Floor Order or Process Control Sheet shall be utilized for any internal assembly activities or work scope activities outsourced under the direct control of the HFC QA Program Manual. The Shop Floor Order or the Process Control Sheet is utilized to approve processes and equipment, as appropriate.

Records of qualification shall be maintained as appropriate.

Implementing Procedures

QPP 2.1, "Quality Plans"

QPP 9.1, "Process Control Sheets and Shop Floor Order Routing"

QPP 17.1, "Quality Records"

Section 10.0 - Inspection

HFC shall establish and maintain documented procedures for inspection activities in order to verify that the specified requirements in the Quality Plan, or implementing procedures, are met. The Quality Plan, or implementing procedures, shall define the inspections required and the inspection records to be established.

Receipt inspection shall be performed as described in implementing procedures. HFC shall ensure that incoming items are not used or processed until they have been inspected or otherwise verified as conforming to procurement documents. Items that have not been subject to receipt inspection shall not be released for use.

The Quality Plan, or implementing procedures, shall define all in-process and / or final inspection attributes. Witness and hold points applied in the project documents shall be verified, and accepted, by personnel qualified in accordance with approved procedures. Final inspection shall verify that the finished item conforms to requirements, all nonconformances are resolved and that all previous defined inspections have been carried out. No item may be released until all inspections that have been defined in the Quality Plan, or implementing procedures, have been satisfactorily completed and the data, documentation, and records associated with these inspections are available and completed. Product failing inspection shall be subject to controls defined in the Corrective Action Program.

In-process inspections shall be identified in the Shop Floor Order for items where the quality cannot be verified once completely assembled or manufactured.

Modifications, repairs, or replacements of items performed subsequent to Final Inspections shall require re-inspection and retest as appropriate to verify acceptability.

Inspection personnel report directly to the QA Director and are independent of the work being inspected. Personnel performing inspections shall be trained and/or qualified in accordance with approved procedures.

Records of inspection activities shall be maintained in accordance with approved procedures. Records shall identify the inspection authority responsible for release of inspected items, the item inspected, inspection date, inspector, type of observation, results and disposition.

Implementing Procedures

QPP 2.2, "General Indoctrination and Training"

QPP 2.5, "Qualification of Inspection Personnel"

QPP 10.1, "Receipt, In-Process, and Final Inspection"

QPP 16.1, "Corrective Action Program"

QPP 15.1, "Nonconformance Control Program"

QPP 17.1, "Quality Records"

QPP 20.1, "Servicing and Customer Supplied Products"

Section 11.0 - Test Control

HFC shall establish and maintain documented procedures for acceptance test activities in order to ensure requirements specified in approved test procedures are met. Test procedures shall define the required tests and the test records to be established.

Test procedures shall have provisions for assuring that test prerequisites have been met, that adequate test instrumentation is available and used, and that the test is performed under suitable environmental conditions. Assigned witness and hold points shall be verified, and accepted, by trained and/or qualified personnel in accordance with approved procedures.

Test results shall be documented and evaluated by responsible individuals to assure that acceptance test requirements have been satisfied. Test activities failing established acceptance criteria shall be subject to the controls defined in the Corrective Action Program. Records shall identify the item tested, date of test, personnel performing the test, test results, actions taken in connection with deviations, and the personnel evaluating the test results. Records of test activities shall be maintained in accordance with approved procedures.

Tests required to collect data, such as for design input, shall be planned, executed, documented, and evaluated.

Procedures are in place for developing test requirements and acceptance criteria for computer programs and associated computer systems. Test requirements and acceptance criteria for verification and In-Use tests are provided and approved. Procedures contain applicable requirements and applicable results shall be documented.

Implementing Procedures

QPP 2.2, "General Indoctrination and Training"

QPP 2.4, "Qualification of Inspection Personnel"

QPP 11.1, "Test Control"

QPP 11.2, "Product Development Test Control"

QPP 17.1, "Quality Records"

Section 12.0 - Control of Measuring and Test Equipment

HFC shall establish and maintain documented procedures to ensure that measuring and test equipment (M&TE) and inspection hardware (e.g., templates, test fixtures, etc.) used in quality affecting activities are properly identified, calibrated, and controlled.

Measuring and test equipment shall be marked or labeled such that the current status of each instrument is readily discernible. As described in implementing procedures, a master list or database is maintained to identify each piece of measuring and test equipment, their location, manufacturer, model number, calibration date, serial number, accuracy and tolerance ranges, calibration due date and calibration intervals.

Measuring and test equipment shall be calibrated against standards that have an accuracy of at least four times the required accuracy of the equipment being calibrated. If this is not possible, the standard used and its measurement uncertainty shall ensure that the equipment being calibrated is consistent with its measurement capability. Measuring and test equipment shall be calibrated using reference standards traceable to national standards (e.g., National Institute of Standards and Technology, "NIST"), where such standards exist. If no national standards exist, the basis for calibration shall be documented.

Measuring and test equipment calibration intervals shall be identified or the measuring and test equipment shall be calibrated prior to each use.

Measuring and test equipment, which are not calibrated to full capability or which have limitations on their use shall be labeled or otherwise identified as to their limitations.

Environmental conditions (e.g., temperature, humidity, static electricity) in which M&TE are calibrated shall be controlled and shall be appropriate for the calibration being performed. As required, M&TE and test software shall be guarded against adjustments that would invalidate the calibration or test results.

Handling, preservation and storage of M&TE shall be prescribed in approved procedures.

Measuring and test equipment found to be beyond calibration limits at the time of re-calibration shall be identified and evaluated on a Condition Report and a use history review conducted to ascertain the identity of components inspected with the M&TE since their last calibration.

Commercial measuring devices (rulers, tape measures, levels, etc.) will not be required to be calibrated if such commercial equipment provides adequate accuracy for the tests or inspections indicated.

Calibration service providers employed to calibrate M&TE for activities affecting quality shall be selected and qualified in accordance with approved procedures.

Records of calibration activities shall be maintained in accordance with approved procedures.

Test software shall be reviewed, approved and controlled in accordance with approved procedures.

When contractually required, technical data pertaining to the M&TE shall be made available to our customers, or their agents, to enable them to verify the functionability and adequacy of the M&TE.

Implementing Procedures

QPP 12.1, "Control of Measuring and Test Equipment"

QPP 16.1, "Corrective Action Program"

QPP 17.1, "Quality Records"

Section 13.0 - Handling, Shipping, Storage and Preservation of Items

HFC shall establish and maintain documented procedures for ensuring that the handling, packaging, shipping, storage, and preservation of items affecting quality satisfy requirements specified in the customer procurement document.

Items shall be handled in a manner not to cause them excessive vibration or damage. Carts may be used to move items around the HFC facility. Lighter items can be hand carried to points of destination.

Special handling requirements, when required, shall be defined in the Quality Plan or approved procedure.

Equipment is staged on shelves, carts, or on the floor in the original container until receipt inspection is completed. In-process items shall be staged on pallets or shelves in a manner not to cause damage or deterioration. Items shall be stored in a manner to prevent damage, deterioration and loss. Appropriate methods for authorizing receipt to and dispatch from these areas have been defined in implementing procedures. As defined in implementing procedures, the condition of product in stock is assessed at least annually to detect deterioration. Documentation of these checks is maintained.

Methods have been established when required for particular items, special equipment (such as containers, shock absorbers, and accelerometers) and special protective environment including atmosphere, moisture, and temperature parameters shall be established, as applicable and verified.

Packaging shall be performed using standard commercial practices in a manner that prevents damage or deterioration to the item shipped or packaged as specified by the customer. Critical, sensitive, perishable, or high-value articles, specific procedure for handling, storage, packaging, shipping, and preservation shall be used. Special handling tools and equipment are typically out-sourced.

Delivery shall be performed using commercial carriers or customer designated carriers. Delivery of product is not considered a critical attribute to product quality unless contractually specified. Commercial carriers do not require approval for placement on the Qualified Suppliers List.

Controls have been established to ensure that unauthorized personnel have limited access to HFC facilities.

Items are marked and/or labeled during packaging, handling, and storage to ensure that the integrity of the units is preserved (e.g., carts, tables, shelves, etc.).

Personnel performing activities affecting quality shall be trained in accordance with approved procedures.

Implementing Procedures

QPP 2.2, "General Indoctrination and Training"

QPP 2.4, "Qualification of Inspection Personnel"

QPP 13.1, "Handling, Shipping, Storage, and Preservation of Materials, Parts, and Components"

QPP 17.1, "Quality Records"

QPP 20.1, "Servicing and Customer Supplied Products"

Section 14.0 - Inspection, Test and Operating Status

HFC shall establish and maintain documented procedures to indicate, by the use of markings, such as stamps, tags, labels, routing cards, or other suitable means, the status of inspections and tests performed upon individual items.

Measures shall be established to provide for the identification of items that have satisfactorily passed required inspections and tests, where necessary to preclude inadvertent bypassing of such inspections and tests. Unsatisfactory inspection or test results are processed in accordance with Section 15.0.

Measures shall be established for indicating the operating status of structures, systems, and components to prevent inadvertent use or operation.

The identification of inspection and test status shall be maintained throughout fabrication, assembly, installation, and testing.

The authority for application and removal of tags, markings, labels and stamps shall be specified.

Implementing Procedures

QPP 8.1, "Identification and Control of Materials, Parts, and Components"

QPP 10.1, "Receipt, In-Process, and Final Inspection"

QPP 11.1, "Test Control"

QPP 13.1, "Handling, Shipping, Storage, and Preservation of Materials, Parts, and Components"

QPP 14.1, "Inspection and Test Status"

QPP 17.1, "Quality Records"

QPP 20.1, "Servicing and Customer Supplied Products"

Section 15.0 - Control of Nonconforming Items

HFC shall establish and maintain documented procedures to ensure that materials, parts, or components that do not conform to requirements are prevented from use or installation. Identification of any of these items not conforming to requirements will require generation of a Condition Report. The responsibility for review and authority for the disposition of nonconforming items shall be defined.

Procedures for nonconforming items shall address identification, documentation, evaluation, segregation, disposition, and notification to affected organizations, including the customer, when required.

Nonconforming items shall be reviewed and accepted, rejected, repaired or reworked in accordance with documented procedures. Disposition and or cause of the nonconforming items shall be documented on the Condition Report.

The description of repairs, and of any nonconformity that has been accepted under authorized concession, shall be recorded to denote the actual condition. Repaired, reworked, and replacement items shall be re-inspected in accordance with documented procedures.

Measures have been established to ensure that personnel performing evaluations to determine a disposition have demonstrated competence in the specific area. The engineering department shall provide a technical justification for repair and use-as-is dispositions. Nonconformances to design requirements dispositioned use-as-is or repair shall be subject to design control measures commensurate with those applied to the original design.

Implementing Procedures

QPP 15.1, "Nonconformance Control Program"

QPP 16.1, "Corrective Action Program"

QPP 17.1, "Quality Records"

QPP 20.1, "Servicing and Customer Supplied Products"

Section 16.0 - Corrective Action

HFC shall establish and maintain documented procedures to ensure that conditions adverse to quality such as inadequate processes, procedures, adverse quality trends, audit findings, deviations from the quality system and/or project requirements, and customer feedback are promptly identified and resolved.

Procedures for corrective action shall require identification of the root cause, the actions taken to resolve significant conditions adverse to quality, to prevent recurrence of the adverse condition, and for the evaluation and documentation of the effectiveness of the corrective actions taken to eliminate the significant conditions adverse to quality.

The investigation, corrective and preventive actions shall be documented on the Condition Report and shall be commensurate with the severity of the condition adverse to quality. Relevant information regarding corrective and preventive conditions shall be reported to, and evaluated by, HFC management during the annual management review of the quality system. HFC shall implement and record any changes to documented procedures resulting from corrective and preventive actions.

Reports of conditions that are adverse to quality are analyzed to identify trends in quality performance. Significant trends are reported to, and evaluated by, HFC management during the annual management review of the quality system.

A process for identifying, documenting, and resolving customer feedback shall be established.

Significant conditions (10CFR Part 21) adverse to quality shall be documented in accordance with established procedures.

Preventative Actions resulting for data analysis and Management review shall be identified and reported in the Corrective Action Program.

Implementing Procedures

QPP 1.1, "Management Review"

QPP 16.1, "Corrective Action Program"

QPP 16.2, "Customer Feedback"

QPP 16.3, "10CFR Part 21 Reporting"

QPP 17.1, "Quality Records"

Section 17.0 - Quality Assurance Records

Sufficient records are maintained by HFC to demonstrate conformance to specified requirements and the effective operation of the quality system.

Procedures are established for classification and identification, collecting, indexing, accessing, filing, storage, maintenance, legibility and disposition of quality records. Records shall be protected against damage, deterioration, or loss. Records shall be bound or placed in folders for storage in steel file cabinets or in containers on shelving. Electronic media shall be stored in appropriate containers.

Records are established and maintained that provide evidence that the product has been inspected and/or tested. These records identify the inspector or data recorder, the type of observation, the results, the acceptability, and the action taken in connection with any deficiencies noted. Pertinent quality records from subcontractors are included.

Requirements concerning record retention, including duration, location, transmittal, and assigned responsibility are established.

Records shall be made accessible to the Purchaser or his designated alternate, e.g. the Owner for an agreed to period of time.

Provisions have been established to ensure that records are stored in facilities or locations constructed and maintained which minimizes the risk of damage or destruction. Nuclear quality records shall be stored in 2-hour fire rated Class B containers meeting NFPA 232-2007 or at a dual storage approved facility.

Implementing Procedures

QPP 17.1, "Quality Records"

Section 18.0 – Audits

HFC shall establish and maintain documented procedures to ensure that a comprehensive system of planned and periodic audits is established and effectively implemented.

Audits shall be scheduled on the basis of the status and importance of the activity to be audited, performed in accordance with written procedures or checklists, and shall be carried out by qualified personnel independent of those having direct responsibility for the activity being audited. Each section of the manual shall be audited annually.

Measures are established to ensure that audits plans are developed and documented, reported, authenticated and contain appropriate information.

Results of audits shall be documented and brought to the attention of the personnel having responsibility in the area audited. Management personnel for the area shall take timely corrective action on deficiencies found during the audit.

Follow-up audit activities shall verify and record the implementation and effectiveness of the corrective action taken.

Relevant results of the audits shall be reported and provided to HFC Management for review during the annual management review of the quality system. Adverse finding shall be investigated and actions taken to correct the finding including measures to prevent recurrence.

Audit records shall include audit plans / checklists, audit reports, written replies and record of corrective action completion.

Implementing Procedures

QPP 1.1, "Management Review"

QPP 2.3, "Lead Auditor Qualification"

QPP 2.4, "Auditor Qualification"

QPP 16.1, "Corrective Action Program"

QPP 17.1, "Quality Records"

QPP 18.1, "Audits"

Section 19.0 - Contract Review

HFC shall establish and maintain documented procedures to ensure that customer orders are reviewed and accepted prior to order release to engineering or production.

Implementing procedures shall assure that customer requirements are reviewed and accepted by authorized HFC personnel to ensure that HFC has the capability to perform the stated scope of work. HFC normally receives customer requirements in the form of purchase orders and contracts.

Differences between HFC proposals and customer authorizing documents shall be reconciled prior to acceptance of the order. Verbal authorizations are not accepted by HFC.

Amendments to customer authorizing documents must be reviewed and accepted in the same manner as the original document.

Records of contract review shall be maintained.

Implementing Procedures

QPP 17.1, "Quality Records"

QPP 19.1, "Contract Review"

Section 20.0 – Servicing and Customer Supplied Products

Servicing activities may include: warranty issues, service contract activities, RMAs, training, application engineering and or field design changes.

Procedures are developed to process Customer Supplied Products in the form of Returned Material Authorizations.

HFC shall establish and maintain documented procedures to ensure that trained and/or qualified personnel perform, verify and report these functions under controlled conditions. For service activities covered by an open project, the Quality Plan shall define the scope of HFC field services required by the customer.

Methods have been established for performing, verifying and reporting the servicing meets specified requirements when contractually specified.

Implementing Procedures

QPP 2.1, "Quality Plans"

QPP 17.1, "Quality Records"

QPP 20.1, "Servicing and Customer Supplied Products"

QPP 10.1, "Receipt, In-Process, and Final Inspection"

QPP 8.1, "Identification and Control of Materials, Parts, and Components"

QPP 15.1, "Nonconformance Control Program"

QPP 13.1, "Handling, Shipping, Storage, and Preservation of Materials, Parts, and Components"

Section 21.0 - Statistical Techniques

Current statistical data, process data, variations, supplier issues and trends are identified for management review. Graphical techniques such as bar charts, tables etc. are used as necessary to depict trends. Applicable managers control the areas for statistical techniques.

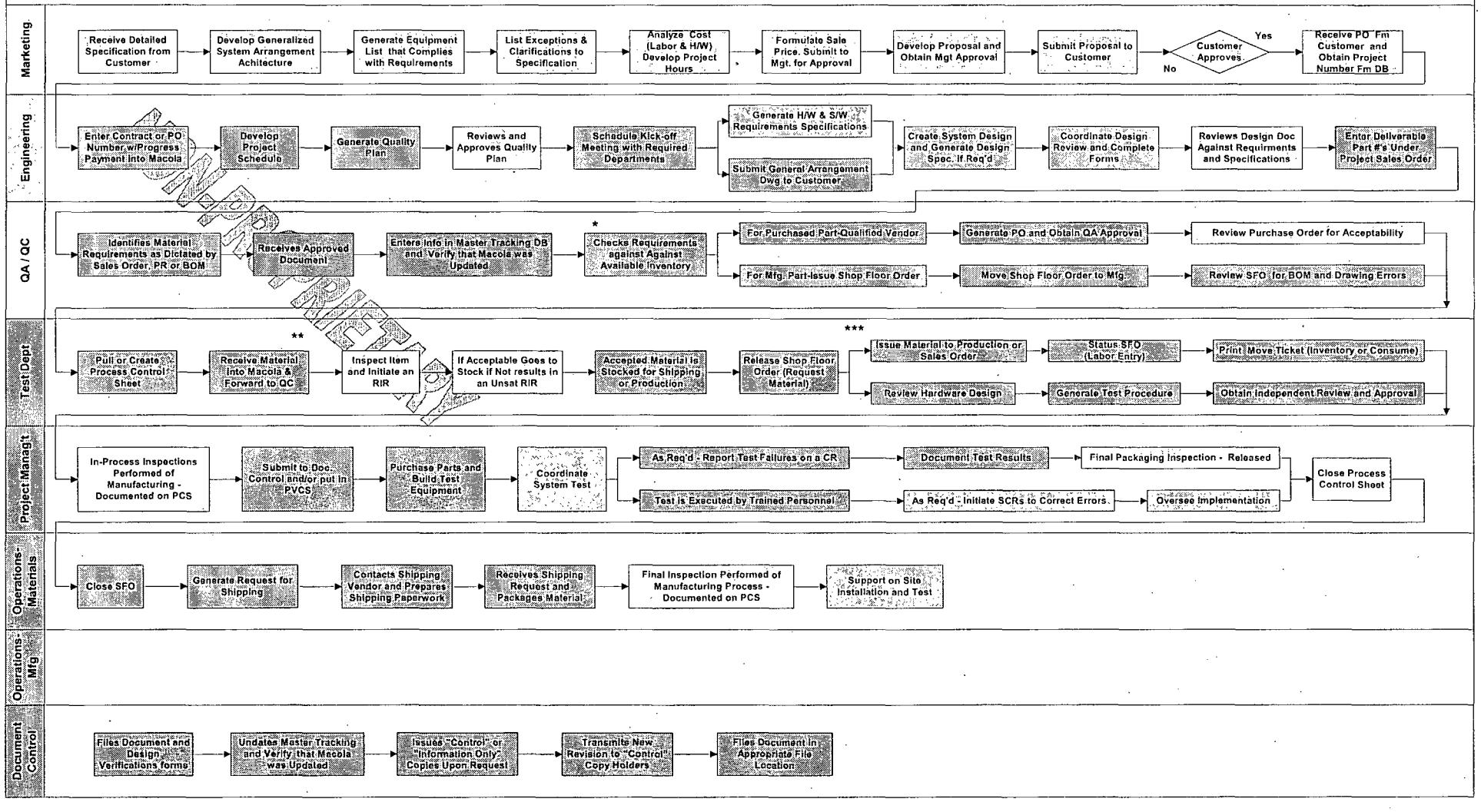
The areas that are targeted for data analysis and used for process improvement are as a minimum the following:

- Customer satisfaction
- Conformance to product and service requirements
- Trends
- Opportunities for preventative actions
- Suppliers.

Implementing Procedures

QPP 21.1, "Statistical Techniques"

ATTACHMENT 1 "Quality Management Process for Projects"



DOOSAN

HF Controls

NON-PROPRIETARY

MANAGEMENT REVIEW

QUALITY PROCESS PROCEDURE

Procedure No. **QPP 1.1** Revision: **C**

Effective Date: **2/2/04**

Prepared By: John Kim

Reviewed By: Jonathan Taylor

Approved By: C.E. Fisher

Management Review

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Management Review

1.0 PURPOSE AND SCOPE

1.1. The purpose of this procedure is to define the process, in which the periodic management review of the HF Controls (HFC) Quality Program is planned, performed, and documented.

2.0 ORGANIZATIONAL RESPONSIBILITIES

2.1. The President of HF Controls is responsible for ensuring that the annual review of the quality program is performed as described in this procedure.

2.2. The Quality Assurance Manager / Designee is responsible for assembling quality system measurable data to be evaluated during the management review meeting, establishing the meeting agenda, and retaining a meeting summary as a quality record.

3.0 REFERENCES

3.1 QPP 17.1, "Quality Records"

3.2 ISO 9001:2000

3.3 CR 2003-0502

4.0 GENERAL INFORMATION

4.1. None

5.0 PROCEDURE

5.1. Planning

5.1.1. The Quality Assurance Manager / Designee shall collect measurable data relating to the following quality system attributes and prepare an agenda for the annual management review of the quality system. Suggested sources of this data are as follows:

1. Condition Report Status (Corrective and Preventive Actions)
2. Internal and applicable External Audit results.
3. Customer Feedback.
4. Documented adverse trends.
5. Returned Material Authorizations (RMA)

6. Training needs for HFC personnel.

7. Process performance.

8. Follow-up actions from previous Management Review Meeting.

9. Recommendations for Improvement.

10. Results of the QA Program review for continual conformance to applicable codes and standards and its influence on the effectiveness and efficiency of the HFC organization.

11. System Change Request (SCR) Status.

12. Changes that could affect the Quality Management System.

13. Resource needs.

5.2. Management Review Meeting

5.2.1. The President, HF Controls, shall chair the management review meeting. Attendees shall include all direct reports and other staff personnel, as necessary.

5.2.2. The attendees shall review the measurable data presented to ensure the quality system's continuing suitability and effectiveness in satisfying HFC's business goals and objectives.

5.2.3. The results of the meeting shall be summarized and shall identify the following:

1. Attendees.

2. Quality Assurance Manager presentation materials of issues discussed.

3. Statement of the effectiveness of the quality system in meeting business goals and objectives.

4. Assigned action items and proposed completion dates, if any.

5. Improvements resulting from the presented data.

6. Additional resources needed.

7. Improvements to products resulting from customer requirements.

5.2.4 The President, HF Controls, shall sign feedback documentation thus attesting to the statement of effectiveness in the presentation materials and may add personal comments or action items to the record regarding but not limited to its effectiveness or conduct.

5.2.5 The meeting summary, and all completed action items are considered quality records and shall be maintained by the Quality Assurance Manager.

5.3. Action items resulting from the meeting shall be identified to allow follow-up.

5.3.1 The Quality Assurance Manager / Designee is responsible for follow-up on action assignments to verify adequate closure. Open actions shall be reported to the President, HFControls.

5.3.1. Results of all completed action assignments shall be disseminated to all attendees and a copy shall be maintained as described in paragraph 5.2.4.

6.0 QA RECORDS

6.1. The following records shall be maintained in accordance with QPP 17.1, "Quality Records".

6.1.1. Management Review Meeting Summary.

6.1.2. Completed action items.

7.0 ATTACHMENTS

7.1. Attachment 7.1, "Management Review Meeting Summary"

MANAGEMENT REVIEW MEETING SUMMARY

Attachment 7.1

DATE: _____

AGENDA:

- Determine which processes or what parts of the business do we want to obtain measurable data on and what is that data as it relates to the following:

  Condition Report Status (Corrective and Preventive)

  Internal and applicable External Audit Results.

  Customer Feedback.

  Documented adverse trends.

  Returned Material Authorizations (RMA)

  Training needs for HFC personnel.

  Process performance.

  Follow-up actions from previous Management Review Meeting

  Recommendations for Improvement.

  Results of the QA Program review for continual conformance to applicable codes and standards and its influence on the effectiveness and efficiency of the HFC organization.

  System Change Request

- Review the effectiveness of the Quality System and provide a statement.

  Previous Internal Audits

  Improvement related to Customer requirements

  Additional resource needs.

SUMMARY OF RESULTS:

_____
_____
_____
_____
_____
_____
_____(Use Addition Pages if necessary)

ATTENDEES SIGNATURE:

_____
_____

DOOSAN

HF Controls

NON-PROPRIETARY

ORGANIZATIONAL RESPONSIBILITIES

QUALITY PROCESS PROCEDURE

Procedure No. **QPP 1.2** Revision: **C**

Effective Date: 10/12/07

Prepared By: P. Mikes

Reviewed By: G. Reding

Approved By: J.F. Ingram

ORGANIZATIONAL RESPONSIBILITIES

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ORGANIZATIONAL RESPONSIBILITIES

1.0 PURPOSE AND SCOPE

1.1. The purpose of this procedure is to delineate the organizational structure, functional responsibilities, levels of authority and lines of communication within HF Controls (HFC).

1.2. These responsibilities apply to product development, and projects performed by HFC, unless specifically delineated in an approved Project Quality Plan.

2.0 ORGANIZATIONAL RESPONSIBILITIES

2.1. The Quality Assurance Manager/Designee is responsible for maintaining and revising this procedure.

3.0 REFERENCES

3.1. HFC Quality Assurance Program Manual

3.2. QPP 16.1, Corrective Action Program

3.3. QPP 17.1, Quality Records

4.0 GENERAL INFORMATION

4.1. The Quality Assurance Department has sufficient authority, access to work areas, and organizational freedom to report quality problems, initiate, recommend, or provide solution to quality problems through designated channels, verify implementation of solutions and assure that further processing, delivery, installation, or use is controlled until proper disposition of a nonconformance, deficiency, or unsatisfactory condition has occurred.

5.0 PROCEDURE

5.1. President, HF Controls

5.1.1. The President of HF Controls is responsible for:

1. Ensuring that the overall quality of the services performed, and products produced by HF Controls, meets or exceeds customer expectations.

2. Promoting an environment of continuous improvement.

3. Communicating company policies, goals and objectives.

4. Performing and documenting the annual review of the Quality Assurance Program.

5. Chairing the meeting for the annual review of the quality program and ensuring that follow-up actions are completed in a timely manner.

5.2. Quality Assurance Department

5.2.1. The Quality Assurance Manager reports directly to the President and is responsible for the following:

1. Providing measurable data relating to the effectiveness of HFC's QA program to the President for evaluation during the annual management review of the quality program.

2. Scheduling and ensuring the execution of all internal audits of activities affecting quality.

3. Evaluating suppliers for compliance with procurement document requirements and license agreements.

4. Reviewing procurement documents and license agreements for inclusion of proper QA requirements.

5. Communicating directly with HFC senior management.

6. Overseeing the control of quality assurance records such as procedures, drawing, specifications, etc.

5.2.2. Quality Control Inspector(s) are responsible for the following:

1. Inspecting and segregating, if required, all parts and products received.

2. Maintaining and executing the HFC quality assurance program.

3. Performing and/or witnessing testing as delineated in test procedures and plans.

4. Reporting nonconformances as appropriate.

5. Verifying any corrective action resulting from a Significant Condition Report.

6. Ensuring that the product delivered meets the Customer requirements.

5.2.3. The Document Control Coordinator is responsible for the following:

1. Ensuring that only the latest revision of documents are distributed or given out for information.

2. Maintaining satellite document stations and ensuring that only the latest revisions are kept in the stations.

3. Maintaining the Document Tracking database.

5.2.4 The V&V Team reports to the director of QA and is responsible for the following:

1. A full independent evaluation of a nuclear safety system's documentation and test results by reviewing for omissions, inconsistencies, inaccuracies and errors of omission/irrelevant requirements with emphasis on the system performance requirements and design specifications.

5.3. Engineering Department

5.3.1. The Vice President of Engineering reports directly to the President and is responsible for the following:

1. Building and providing leadership for a first class product development and project execution team, creating an organization that teams with sales, marketing and aftermarket services, creating trust and credibility throughout the company.

2. Supervising all engineering activities all projects of HFC product lines. Ensuring that all engineering efforts are delivered on time, on budget and in proper working order in accordance with the functionality identified in the requirements documents and project development plan. He is also responsible for providing technical

guidelines and engineering design directions.

3. Protecting HFC intellectual property by designing and enforcing security systems. Developing the process and maintenance tracking system for HFC patents.

4. Acting as technical liaison with parent company to identify, jointly develop new projects and new sources of product development funding.

5.3.2. The Hardware and Software Development Engineering section is responsible for the following:

1. The Development Engineering Section has a Senior Manager to lead overall system development activities and handle quality and schedule for all system hardware/software design projects. A Manager of H/W development supervises the H/W development activities and a Manager of S/W development supervises the S/W development activities.

2. Designing and testing system hardware/software for HFC product lines for both nuclear safety related and non-safety/commercial related applications.

3. Supporting the technical service for all HFC's existing installed control systems.

4. Designing test procedures and performing test process and reports for all development activities of HFC control systems.

5. Publishing technical manuals for HFC product lines.

6. The H/W and S/W Engineers in Development Engineering section handle system development projects to extend the scope of supply for an HFC control system.

5.3.3 The Project Engineering section is responsible for the following:

1. The Project Engineering section has a Director to manage overall project engineering activities and handle quality and schedule for all HFC projects. A Senior Project Manager manages projects in a special market

and territory. A Project Engineer supervises the project engineering activities.

2. Ensuring the management of the total engineering and technical content on a project from receipt of contract to customer acceptance.

3. Coordinating the total project engineering efforts with the rest of engineering sections. Project Engineer/Manager is responsible for the project schedule and cost issues related to engineering exercise.

4. Coordinating with the Procurement Department for the schedule and cost issues related to material purchasing.

5. Coordinating with the Manufacture Department for the schedule and cost issues related to manufacturing.

6. Monitoring project's engineering status and report as necessary.

7. Developing Project Quality Plans and Process Control Sheets, when applicable.

8. Acting as the primary technical contact with customer for Nuclear and Non Nuclear Safety related contracts.

9. For application engineering activities, designing the loop schematic drawing, control logics, database and system graphics.

10. Developing bills of materials and documentation to include dimensions, part numbers, wiring and assembly diagrams, standard products, logic drawings and graphics.

11. Designing the arrangement drawing, specifying equipment, power distribution drawings, assembly drawings, address tables and field installation drawings.

5.3.4 System Test Technician reports to the Director of Engineering and is responsible for the following:

1. Performing system level testing activities in accordance with documented engineering procedures and project requirements.

2. Supporting Integration and Test/Repair activities when workload permits.

3. Ensuring that system test activities comply with quality requirements.

5.4. Operations Department

5.4.1. The Director of Operations reports directly to the President and is responsible for the following:

1. Procuring of all products and services necessary for business operations in a manner that maximizes value to HFC.

2. Developing and managing the supply chain to deliver value to both internal and external customers.

3. Reviewing purchase orders to ensure their quality.

5.4.2. The Integration Manager reports directly to the Director of Operations and is responsible for the following:

1. Ensuring that all assembly work is performed in accordance with approved and current engineering drawings.

2. Ensuring that every aspect of the manufacturing process complies with quality requirements.

3. Establishing and maintaining calibrated measuring and testing equipment.

5.4.3 The Test / Repair Manager reports directly to the Director of Operations and is responsible for the following:

1. Ensuring that all product testing and rework / repair activities are performed in accordance with approved and current engineering design documentation.

2. Ensuring that every aspect of the product testing and rework / repair process complies with quality requirements.

5.4.4 The Buyer / Planner reports to the Director of Operations and is responsible for the following:

1. Procuring materials, both production and non-production in accordance with established quality procedures and work instructions.

2. Creating Shop Floor Orders, including routings and material plans, in support of Project material requirements and deadlines.

3. Maintaining critical planning data in an ERP environment.

4. Ensuring that all procurement and production control activities comply with quality requirements.

5.5. Sales and Marketing Department

5.5.1 The Director of Sales and Marketing reports directly to the President and is responsible for the following:

1. Supervising all HFC sales support staff both in-house and at regional offices.

2. Establishing and managing a sales representative organization to cover both domestic and international sales.

3. Participating in contract negotiations as the lead negotiator for HFC.

5.5.2 The Customer Care Manager reports directly to the Director of Sales and Marketing and is responsible for the following:

1. Supervising all after-market services (service, spare parts, and customer training) for all HFC control systems.

2. Reviewing all customer purchase orders to ensure that pricing policies established for after-market services are correct based on the proposals or quotations before the order is accepted at HFC.

5.5.3 The National Sales Manager reports directly to the Director of Sales and Marketing and is responsible for the following:

1. Participating in contract negotiations as the lead negotiator for HFC for North American Projects.

2. Coordinating and scheduling of all Proposal personnel for work performed to support the sales effort.

3. Establishing and managing a sales representative organization to cover both domestic and international sales.

4. Developing and maintaining company product literature.

5. Developing and maintaining existing customer base and developing new business opportunities for the North American Markets.

5.6. Finance

5.6.1 The Chief Financial Officer reports to the President and is responsible for the following:

1. Represent the organization's financial operations and financial condition to the parent company, board of directors, and other outside contacts.

2. Coordinates finance and accounting activities of the organization.

5.6.2 The Controller reports to the Chief Financial Officer and is responsible for the following:

1. Directs the financial and accounting activities of an organization by performing the following duties personally or through subordinates:

   a. General and subsidiary ledgers, accounts receivable, accounts payable, revenue distribution, depreciation, cost, property, and operating expenses.

   b. Prepares budgets, statements and reports which summarize and forecast company business activity and financial position in areas of orders, income, expenses, and earnings based on past, present, and expected operations.

   c. Directs the installation and maintenance of new accounting, timekeeping, payroll, inventory,

property, and other related procedures and controls.

5.6.3 The HR Generalist/Payroll Generalist reports to the Controller and is responsible for the following:

1. To complete all aspects of the Human Resource and Payroll functions including new employee orientation, benefits, payroll, and compliance to applicable local, state, and federal laws and third party reporting requirements relating to these activities.

5.7 Organizational Interface

5.8.1 The responsibilities between organizations shall be delineated in the Quality Process Procedure and the Work Instructions.

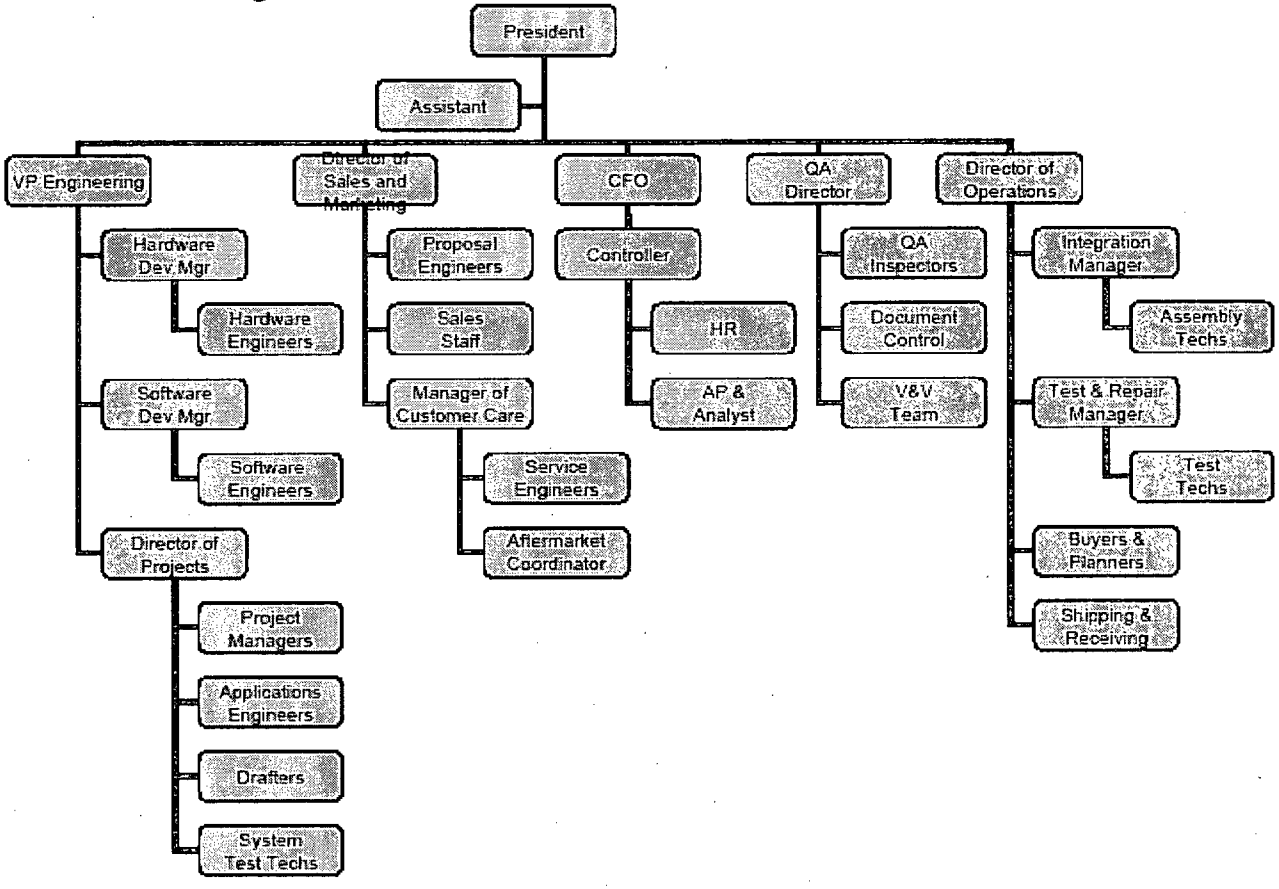
6.0 QA RECORDS

6.1. None

7.0 ATTACHMENTS

7.1. Organizational Chart

HF Controls Organization Chart



DOOSAN

HF Controls

NON-PROPRIETARY

QUALITY PLANS

QUALITY PROCESS PROCEDURE

Procedure No. **QPP 2.1** Revision: **D**

Effective Date: **07/07/06**

Prepared By: Teryl Rogers

Reviewed By: John Stevens

Approved By: C.E. Fisher Jr.

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1.0 PURPOSE AND SCOPE

1.1. The purpose of this procedure is to define the process to be followed by the Project Manager in initiating, managing, and closing out a project or a spare parts order that endorses the requirements of NQA-1 or ISO 9001.

2.0 ORGANIZATIONAL RESPONSIBILITIES

2.1. The Quality Assurance Manager is responsible for reviewing and approving the Project Quality Plan (PQP) and the Spares Quality Plan (SQP).

2.2. The Project Manager is responsible for planning, initiating, managing, and closing the project or spare parts order in accordance with the requirements identified within this procedure.

3.0 REFERENCES

3.1. QPP 2.1, "General Indoctrination and Training"

3.2. QPP 7.2, "Commercial Grade Dedication"

3.3. QPP 10.1, "Receipt, In-Process and Final Inspections"

3.4. QPP 16.1, "Corrective Action Program"

3.5. QPP 17.1, "Quality Records"

3.6. QPP 19.1, "Contract Review"

3.7 2002-0531

4.0 GENERAL INFORMATION

4.1 Definitions

4.1.1 A "<u>project</u>" supports the development, maintenance and/or implementation of a product. The project may be executed by HFC staff performing various activities or through one or more contracts with suppliers. The result of project efforts consists of the direct delivery of a product to the customer.

4.1.2 A "<u>product</u>" is a service, hardware, processed materials, software, or a combination thereof, developed by HFC for its customers.

4.1.3 A "spare" is a part ordered after delivery and may include the assembly of products. An order is considered a "spare" when no engineering work is required.

4.2 A Project Quality Plan shall be developed for all projects that have product deliverables to HFC customers. The Project Quality Plan need not be used for fabrication and assembly of inventory stock items performed by HFC.

4.3 A Spares Quality Plan shall be developed for only nuclear spare parts orders.

5.0 PROCEDURE

5.1. Project Initiation

5.1.1 A quality project may be initiated as the result of:

1. A customer order, as documented on an Order Entry Review form in accordance with QPP 19.1, "Contract Review".

2. A decision by HFC Management to perform work meeting either NQA-1 or ISO 9001 requirements in order to meet customer, policy or business needs.

5.1.2 Each Project Manager planning a project or spare order shall have access to the latest approved version of the HFC Quality Manual and Procedures on the HFC LAN. The Project Manager shall develop a Project Quality Plan (PQP) as described in Paragraph 5.2 of this procedure or a Spares Quality Plan (SQP) as described in Paragraph 5.3 using the latest version of the form attached to this procedure.

5.1.3 While the PQP or the SQP is required at the initiation of the project or order; any changes in the information contained in the document require a revision with approval of the QA Manager. A revision of the PQP or SQP may use the version used in the original submission, with the approval of the QA Manager.

5.2 Project Quality Plan (PQP):

5.2.1 The Project Manager shall address the following elements in the PQP using Attachment 7.1 to this QPP:

5.2.2 The **Project Definition** shall reflect the customer requirements and identify, where applicable, the project objectives, major tasks, major deliverables, customer-specific requirements, and project schedule with anticipated project end date.

5.2.3 **Quality Requirements** shall identify which quality standard(s) are to be passed down to the supplier, and which portions of the project are to be conducted under this quality program. If Commercial Grade Dedication is used to bring a product under this quality program, this quality program's requirements will apply with the initiation of the Commercial Grade Dedication in accordance with QPP 7.2, "Commercial Grade Dedication".

5.2.4 **HFC Quality System Applicability** identifies which sections of the HFC QA Manual apply to this project and which Quality Process Procedures (QPP) are to be implemented by the Project Team. Those sections of the QA Manual and those QPPs that apply to all projects under a quality program have been pre-checked as mandatory in Section 3 of the form. The remaining sections and procedures shall be selected by the Project Manager, as appropriate for the work to be performed.

1. It is the Project Manager's responsibility to review new or revised QPPs issued after the approval date of the project's PQP, for applicability to the project's activities.

2. The PQP shall be revised whenever a new or revised QPP is considered applicable to the project.

5.2.5 This project may require specific **Work Instructions** to execute project-specific processes or provide alternatives to existing QPPs. These instructions may be required to support work done at HFC or by HFC suppliers. These special instructions shall be identified in the PQP or, if specific instructions cannot be identified at this time, the need to identify them early in the project shall be specified.

5.2.6 Members of the **Project Team** that will implement this PQP shall be identified by name and title or role. The Project Manager shall ensure that all team members have been trained in accordance with QPP 2.2, "General

Indoctrination and Training." Design interfaces (internal/external to HFC) shall be identified.

5.2.7 HFC may elect to subcontract to **Qualified Suppliers,** some or all of the work identified in the project. This may be to provide technical support, or to supply software, material, or parts for the project. Suppliers expected to be used for the work shall be identified.

1. If a proposed supplier is not on the QSL, the Project Manager should request the QA Manager to evaluate the Supplier for inclusion on the QSL. (Making the request early will minimize delay in issuing the procurement document.)

2. If the proposed supplier's quality program is not suitable for inclusion on the QSL, the Project Manager may propose to the QA Manager that the suppliers products be evaluated in accordance with QPP 7.2, "Commercial Grade Dedication" in order to use the services of the proposed Supplier.

3. If none of these approaches is deemed workable, the Project Manager shall select a different Supplier.

5.2.8 **HFC Hold Points/Source/Receipt, In-process and Final Inspections** shall be identified in order to assure that the Project Manager has approved results at key milestones of the project. Inspection requirements are described in QPP 10.1, "Receipt, In-Process and Final Inspections."

5.2.9 **Project Quality Documents and Records** that will be maintained during the project shall be identified. The project quality records will usually include those documents identified below.

1. The Project Manager shall identify **Supplier Documents that are required to be Submitted to HFC for Review and Approval**. The requirement to review and approve these documents shall be identified in the procurement document issued to the supplier.

2. **Documents that require customer approval** shall be identified by the Project Manager. These could include drawings of a part or component being

produced for the customer, nonconformance reports, supplier documents.

3. The Project Manager shall identify **Project-Specific Documents Affecting Product Quality to be Developed by the HFC Project Team**. These documents shall include, where applicable, technical specifications, design review plans, supplier work scope, fabrication specifications, software V&V, test plans, process control forms and travelers, criteria for satisfactory conclusion of the project, etc.

4. The Project Manager shall indicate in the PQP **any User or Software Setup Documentation or Manuals** required for the project. The PQP shall indicate the schedule for submittal of such documents or manuals.

5.2.10 Any **Other Items** unique to this project affecting product quality that is not addressed above shall be identified.

5.3 Spares Quality Plans:

5.3.1 The Project Manager shall address the following elements in the SQP using Attachment 7.2 to this QPP:

5.3.2 The **Spares Definition** shall reflect the customer requirements and identify, where applicable, major tasks, major deliverables, customer-specific requirements, and shipment schedule.

5.3.3 The **Quality Requirements** shall identify which quality standard(s) are to be passed down to the supplier, and which portions of the order are to be conducted under this quality program. If Commercial Grade Dedication is used to bring a product under this quality program, this quality program's requirements will apply with the initiation of the Commercial Grade Dedication in accordance with QPP 7.2, "Commercial Grade Dedication".

5.3.4 **HFC Quality System Applicability** identifies which sections of the HFC QA Manual apply to this order and which Quality Process Procedures (QPP) governs.

1. It is the Project Manager's responsibility to review new or revised QPPs issued after the approval date of the SQP, for applicability.

2. The Process Control Sheets for HFC assemble products placed in inventory to be sold as "spare" shall be retrieved and evaluated. This evaluation shall determine if the previous completed hold and witness points meet customer requirements of the current order. This evaluation is performed and documented by the QA Manager/Designee in the SQP.

5.3.5 The SQP shall be revised whenever a new or revised QPP is considered applicable to the order.

5.3.6 This order may require specific **Work Instructions** to execute product-specific processes or provide alternatives to existing QPPs. These instructions may be required to support work done at HFC or by HFC suppliers. These special instructions shall be identified in the SQP or, if specific instructions cannot be identified at this time, the need to identify them early in the completion of the order shall be specified.

5.3.7 HFC may elect to subcontract to **Qualified Suppliers,** some or all of the work identified in the order. This may be to provide technical support, or to supply software, material, or parts. Suppliers expected to be used to fulfill the order shall be identified.

1. If a proposed supplier is not on the QSL, the Project Manager should request the QA Manager to evaluate the Supplier for inclusion on the QSL. (Making the request early will minimize delay in issuing the procurement document.)

2. If the proposed supplier's quality program is not suitable for inclusion on the QSL, the Project Manager may propose to the QA Manager that the suppliers products be evaluated in accordance with QPP 7.2, "Commercial Grade Dedication" in order to use the services of the proposed Supplier.

5.3.8 If none of these approaches is deemed workable, the Project Manager shall select a different Supplier.

5.4 Project Management

5.4.1 The Project Manager shall submit the completed PQP or the SQP to the QA Manager for his review and approval. If required by the customer-authorizing document, the

Project Manager shall submit the PQP to the customer for his/her approval. Revisions to the PQP or SQP shall follow the same review and approval process as the original.

5.4.2 The Project Manager shall establish a Project Record File for managing the Project Quality Records in accordance with QPP 17.1, "Quality Records."

5.4.3 Specific Work Instructions may be developed as specified in the PQP or SQP.

5.4.4 The Project Manager and the Quality Assurance Manager shall ensure that controlled copies of the PQP or SQP and specific work instructions are available to the appropriate members of the project team who will perform the QA tasks for the projects and indoctrinate them in the contents of the PQP or SQP and those work instructions which govern the work each team member performs. Objective evidence of this training shall be recorded per QPP 2.2, "General Indoctrination and Training".

5.4.5 For work to be performed by a supplier, the Project Manager shall prepare a procurement document, which shall include, where applicable, the following information:

1. Engineering documents (e.g., specifications, drawings, bill of materials, etc)

2. Hold points, including those requiring HFC acceptance before proceeding

3. Documents required from the supplier for HFC review and approval

4. Customer or other special requirements

5. Specification of which tasks are to be performed under the supplier's quality program.

6. Product or service acceptance criteria.

5.4.6 The Project Manager shall review and approve supplier documents as specified in the PQP and the procurement document. The Project Manager shall record his/her approval on the document.

5.4.7 The Project Manager shall submit project documents to the customer for approval as specified in the PQP.

5.4.8 The Quality Assurance Manager shall document any Nonconformances or Corrective Actions in accordance with QPP 16.1, "Corrective Action Program".

5.5 Project and Spares Order Close-Out

5.5.1 Projects and Spares Orders will be closed out and be considered inactive when all activities for that project or orders have been completed.

5.5.2 Quality records associated with the activity shall be transmitted to Record Retention for archival within one (1) year after work has ceased on that contract or activity.

6.0 QA RECORDS

6.1 The following records shall be maintained in accordance with QPP 17.1, "Quality Records".

6.1.1 Project and Spares Quality Plan

Retention Time: Nuclear – Lifetime, Commercial – 7 yrs.
Location: Record Retention File.
Authorized Access: HFC Personnel.
Method of Filing: Project Number.
Dispositioned By: QA Manager

7.0 ATTACHMENTS

Attachments 7.1 and 7.2 are forms that are related to this procedure. These forms shall carry the same revision as this procedure. To access them, click on the link provided.

7.1 Project Quality Plan..\Forms\QPP 2.1, Attachment 7.1, Project Quality Plan, Rev D.doc

7.2 Spares Quality Plan..\Forms\QPP 2.1, Attachment 7.2, Spares Quality Plan, Rev D.doc

DOOSAN

HF Controls

NON-PROPRIETARY

GENERAL INDOCTRINATION AND TRAINING

QUALITY PROCESS PROCEDURE

Procedure No. **QPP 2.2** Revision: **D**

Effective Date: 10/12/07

Prepared By: B. Cain

Reviewed By: J. Stevens

Approved By: J. Ingram

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GENERAL INDOCTRINATION AND TRAINING

1.0 PURPOSE AND SCOPE

1.1. The purpose of this procedure is to describe the requirements for general indoctrination and training of HF Controls (HFC) personnel who manage, perform, or verify activities affecting quality.

2.0 ORGANIZATIONAL RESPONSIBILITIES

2.1. Executive management, as defined in Quality Process Procedure (QPP) 1.2, "Organizational Responsibilities" shall determine appropriate training needs during the annual management review of the Quality Program.

2.2. The QA Director is responsible for accomplishing general Quality Assurance training of HFC personnel, who manage, perform, or verify activities affecting quality, in the requirements of the Quality Program. The QA Director shall maintain the applicable records documenting performance of this indoctrination and training.

2.3. Human Resources are responsible for providing new employee orientation and for maintaining records documenting performance of this activity.

2.4. Department Managers are responsible for training their personnel in their roles as established by the QA Program and or the Project Quality Plan.

3.0 REFERENCES

3.1. QPP 1.1, "Management Review"

3.2. QPP 1.2, "Organizational Responsibilities"

3.3. QPP 2.1, "Quality Plans"

3.4. QPP 2.3, "Lead Auditor Qualification"

3.5. QPP 2.4, "Auditor Qualification"

3.6. QPP 2.5, "Qualification of Inspection Personnel"

3.7. Deleted

3.8. QPP 17.1, "Quality Records"

3.9. WI-ENG-005, "Certifying Engineering Activities"

3.10. WI-OP-004, "Declaration of Manufacturing Competency"

4.0 GENERAL INFORMATION

4.1. General

4.1.1. All personnel who manage, perform and verify activities affecting quality must be *trained* in the requirements of the Quality Program to enable them to fully participate in the operation of that Program.

4.1.2. All management, technical, and administrative support personnel employed as of April 20, 2001 are qualified to perform their current job function based on their training, education, and/or experience as of that date. Records of previous training and/or qualification for personnel who performed and verified work affecting quality may be available. All new or transferred, management, technical, and support personnel must be trained to perform their assigned functions under this program.

5.0 PROCEDURE

5.1. Employee and Contract Personnel Training

5.1.1. Training (job task specific) for all new or transferred, management, technical, and support personnel working on or supervising projects, must be performed by his or her manager. This training shall assure that each employee or contractor is capable of performing his or her assigned functions under this program. Attestation of successful completion of this training, or its equivalent, will be an appropriately signed document from their immediate manager. This document is forwarded to the QA Director to be maintained as a quality record in accordance with QPP 17.1, "Quality Records".

5.1.2. Lead Auditors, auditors, and inspection personnel shall be qualified and certified to perform their assigned tasks in accordance with procedures referenced in Section 3.0.

5.2. New Employee Orientation

5.2.1. All new HFC employees who play a role in HFC's Quality Program shall receive new employee orientation in HFC Corporate Policies, applicable Quality Process Procedures and applicable Work Instructions (WI).

5.3. Quality Program Training

5.3.1. Managers of all new HFC personnel, whose assigned activities may affect quality, shall assure that their

employees are trained in the requirements of the quality system and their specific job task. Contractor personnel who could manage, perform or verify activities affecting quality shall be trained in the quality system and job specific tasks. This training shall occur within six months of their employment but prior to assignment to a project. This training shall include:

1. HFC's Quality Policy.

2. Overview of the HFC Quality Program (Quality Manual, Quality Process Procedures, and Work Instructions).

3. Job Specific Competency Requirements.

5.3.2. As an alternate to classroom or one-on-one training, staff personnel may be given a required reading list to complete. This required reading list must be completed within the time constraints defined in paragraph 5.4.1.

5.3.3. The QA Director shall maintain a Training Attendance Sheet (Attachment 7.1) as a quality record in accordance with QPP 17.1, "Quality Records". A training log or matrix may be developed from the attendance sheet at which time attendance sheets may be discarded. The Training Log or Matrix should have as a minimum the trainee's name, the date of training and the training course title (content). The reading list shall serve as a Training Attendance Sheet in the event it is used according to paragraph 5.4.2.

5.3.4. Refresher training in the Quality Program shall occur every two years. All HFC personnel, who manage, perform, or verify activities affecting quality under this Program, shall attend this training. As discussed in paragraph 5.4.2 a reading list may be optioned for this one-on-one or classroom training.

5.4. Required Project or Job Specific Training

5.4.1. Project or job specific training on their roles as defined in the PQP and Work Instructions, which the PQP calls for the project team to use, will be conducted by the Project Manager / Designee or the individual department Manager / Designee. Attachment 7.1 or the forms required from Reference 3.9 and 3.10 shall be used to document this training / competency requirements. Training records shall be maintained in accordance with QPP 17.1, "Quality Records".

5.4.2. Required reading lists, which include the QA Program Manual, applicable QPPs and WIs, are found in the Attachments. The manager may use any of these, based on the departmental need, to select and record the employee's proficiency and awareness maintenance of the Quality Program as required in Section 5.3.

5.5. HFC Training Needs

5.5.1. Training needs for affected HFC personnel shall be discussed, identified, and documented during the annual management review of the Quality Program as required by QPP 1.1, "Management Review".

6.0 QA RECORDS

6.1. The following records shall be maintained in accordance with QPP 17.1, "Quality Records".

6.1.1. Training Attendance Sheet.

6.1.2. Management validation of employee training – Reference 3.9 and 3.10 Forms.

6.1.3. Deleted

6.1.4. Deleted

6.1.5. Project training records.

6.1.6. Required Reading List.

Retention Time: Nuclear – Lifetime.
Location: Record Retention File.
Authorized Access: HFC Personnel.
Method of Filing: Employee Name or by Year.
Dispositioned By: QA Director

7.0 ATTACHMENTS

7.1. Training Attendance Sheet *
7.2 Required Reading
7.3 Required Reading QAPM and QPP
7.4 Required Reading WI
7.5 Required Reading WI for QC Inspector

* HYPERLINKED TO: KEPCODATA \ HFC_DOC_CNTL \ FORMS

HFC

NON-PROPRIETARY

LEAD AUDITOR QUALIFICATION

QUALITY PROCESS PROCEDURE

Procedure No. **QPP 2.3** Revision: **0**

Effective Date: **7/23/2001**

Prepared By: P. Mikes

Reviewed By: B. Cain

Approved By: J.F. Ingram

Lead Auditor Qualification

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Lead Auditor Qualification

1.0 PURPOSE AND SCOPE

1.1. The purpose of this procedure is to define the requirements for qualifying and certifying Lead Auditors.

2.0 ORGANIZATIONAL RESPONSIBILITIES

2.1. The Quality Assurance Manager, or a qualified Lead Auditor, is responsible for qualifying and certifying Lead Auditors in accordance with this procedure.

3.0 REFERENCES

3.1. QPP 17.1, "Quality Records"

4.0 GENERAL INFORMATION

4.1. None.

5.0 PROCEDURE

5.1. General

5.1.1. The prospective Lead Auditor shall have verifiable evidence that a minimum of ten (10) credits under the following system have been accumulated.

5.1.2. Education and Experience (Four credits maximum)

1. Associate degree from an accredited institution: score one credit or if the degree is in engineering, physical sciences, mathematics, or quality assurance, score two credits; or

2. A bachelor's degree from an accredited institution: score two credits, or if the degree is in engineering, physical sciences, mathematics, or quality assurance, score three credits; in addition score one credit for a master's degree in engineering, physical sciences, mathematics, or quality assurance from an accredited institution.

5.1.3. Experience (Nine credits maximum)

1. Technical experience in engineering, manufacturing, construction, operation, or maintenance: score one (1) credit for each full year with a maximum of five (5) credits for this aspect of experience.

2. If two (2) years of this experience have been in the nuclear field, score one additional credit; or

3. If two (2) years of this experience have been in quality assurance, score two (2) additional credits; or

4. If two (2) years of this experience have been in auditing, score three (3) additional credits; or

5. If two years of this experience have been in nuclear quality assurance, score three (3) additional credits; or

6. If two (2) years of this experience have been in nuclear quality assurance auditing, score four (4) additional credits.

5.1.4. Other Credentials of Professional Competence (Two [2] credits maximum)

1. For certification of competency in engineering, science, or quality assurance specialties issued and approved by a State Agency or National Professional or Technical Society: score two (2) credits.

5.1.5. Rights of Management (Two [2] credits maximum)

1. HFC may grant up to two (2) credits for other performance factors applicable to auditing which may not be explicitly called out in this practice. Examples of these factors are leadership, sound judgment, maturity, analytical ability, tenacity, past performance, and quality assurance training courses.

5.1.6. Communication Skills

1. Prospective Lead Auditors shall have the capability to communicate effectively, both in writing and orally. This shall be attested to in writing on the Lead Auditor Qualification Form (Attachment 7.1).

5.1.7. Training

The prospective Lead Auditor shall receive training to the extent necessary to assure competence in auditing skills. Training in the following areas shall be given based upon management evaluation of the particular needs of each prospective Lead Auditor:

1. Knowledge and understanding of applicable codes, standards, regulations, and regulatory guides.

2. General structure of quality assurance programs as whole and applicable elements.

3. Auditing techniques of examining, questioning, evaluating, and reporting, methods of identifying and following up on corrective action items, and closing out audit findings.

4. Audit planning in the quality related functions for the following activities: design, purchasing, fabrication, handling, shipping, storage, cleaning, erection, installation, inspection, testing, statistics, nondestructive examination, maintenance, repair, operation, modification of nuclear facilities or associated components, and safety aspects of the nuclear facility.

5. On-the-job training to include applicable elements of the audit program.

5.1.8. Audit Participation

1. The prospective Lead Auditor shall have participated in a minimum of five (5) quality assurance audits within a period of time not to exceed three (3) years prior to the date of qualification, one audit of which shall be a nuclear quality assurance audit within the year prior to his qualification.

5.1.9. Examination

1. The prospective Lead Auditor shall pass an examination that shall evaluate his comprehension of and ability to apply the body of knowledge identified in 5.1.7 above. The test may be oral, written, practical, or any combination of the three types. The development and administration of the examination shall be in accordance with Section 5.3.1 of this procedure.

5.2. Maintenance of Qualification

5.2.1. Maintenance of Proficiency

1. Lead Auditors shall maintain their proficiency through: regular and active participation in the audit process, review and study of codes, standards, procedures, instructions, and other documents related to quality assurance programs and program auditing, and participation in training programs. Based on annual assessment, management may extend the qualification, require retraining, or require requalification. These evaluations shall be documented on the Lead Auditor Qualification Form (Attachment 7.1) and/or a memo attesting to the results of the annual assessment.

5.2.2. Requalification

1. Lead Auditors who fail to maintain their proficiency for a period of two years or more shall require requalification. Requalification shall include retraining in accordance with the requirements of 5.1.7 above, and participation as an Auditor in at least one nuclear quality assurance audit.

5.3. Qualification Examination

5.3.1. The development and administration of the Lead Auditor examination is the responsibility of the Quality Assurance Manager. This activity may be delegated to an independent testing agency or contractor, but the Quality Assurance Manager shall retain responsibility for conformance of the examination and its administration. Integrity of the examination shall be maintained by the employer or certifying agency through appropriate confidentiality of files and, where applicable, proctoring of examinations. Copies of the objective evidence regarding the type(s) and content of the examination(s) shall be retained by HFC.

5.4. Certification of Qualification

5.4.1. Each Lead Auditor shall be certified as being qualified to lead audits. This certification shall be documented on the Lead Auditor Qualification Form (Attachment 7.1) to this procedure and shall, as a minimum, reflect the following information:

1. HFC as the certifying agent.
2. Lead Auditor's name and employer.
3. Date of certification or recertification.
4. Basis of qualification (i.e. education, experience, communication skills, training, examination, etc.).
5. Signature of the HFC individual who is responsible for certification of qualification for Lead Auditors.

6.0 QA RECORDS

6.1. The Record of Lead Auditor Qualification Form shall be retained on file in accordance with QPP 17.1, "Quality Records":

7.0 ATTACHMENTS

7.1. Attachment 7.1, Record of Lead Auditor Qualification Form

Lead Auditor Qualification

ATTACHMENT 7.1

HFC

RECORD OF LEAD AUDITOR QUALIFICATION FORM

HFC RECORD OF LEAD AUDITOR QUALIFICATION	Name	Date
EMPLOYER:		
QUALIFICATION POINT REQUIREMENTS		CREDITS
Education - University/Degree Date	4 Credits Max.	_____
1. Undergraduate Level 2. Graduate Level		
Experience - Company/Dates	9 Credits Max.	_____
Nuclear Industry (0-1 credit), or Quality Assurance (0-2 credits), or Auditing (0-4 credits)		
Professional Accomplishment - Certificate/Date	2 Credits Max.	_____
1. P.E. 2. Society		
Management - Justification/Evaluator/Date	2 Credits Max.	_____
Explain: Evaluated by: (Name and Title)	Date:	
	Total Credits:	_____
AUDIT COMMUNICATION SKILLS		
Evaluated by: (Name and Title)	Date:	
AUDIT TRAINING COURSES		
Course Title or Topic: 1. 2.	Date:	
AUDIT PARTICIPATION		

	Location	Audit	Date
	1.		
	2.		
	3.		
	4.		
	5.		

EXAMINATION:	PASSED:	DATE:
AUDITOR QUALIFICATION CERTIFIED BY: (Signature and Title)		Date Certified

ANNUAL EVALUATION (Signature and Date)					

HFC

NON-PROPRIETARY

AUDITOR QUALIFICATION

QUALITY PROCESS PROCEDURE

Procedure No. **QPP 2.4** Revision: **0**

Effective Date: **5/11/2001**

Prepared By: P. Mikes

Reviewed By: Jonathan Taylor

Approved By: J.F. Ingram

Auditor Qualification

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Auditor Qualification

1.0 PURPOSE AND SCOPE

1.1. The purpose of this procedure is to define the requirements for qualifying and certifying auditors. (For qualifying lead auditors see QPP 2.3)

1.2. This procedure applies to the personnel who will participate as auditors in HFC quality assurance audits. Activities in such audits include planning, conducting, documenting, and closing audits.

2.0 ORGANIZATIONAL RESPONSIBILITIES

2.1. The Quality Assurance Manager is responsible for assuring the qualification and certification of Auditors in accordance with this procedure.

3.0 REFERENCES

3.1. QPP 2.3, "Lead Auditor Qualification"

3.2. QPP 17.1, "Quality Records"

4.0 GENERAL INFORMATION

4.1. None

5.0 PROCEDURE

5.1. Qualifications of Audit Personnel

5.1.1. The Quality Assurance Manager, or designated Lead Auditor, shall assign auditors or Technical Specialists to assist in HFC audits. The qualifications for these individuals shall be based on comparing the individual's education, experience, and level of competence as evidenced by oral examination during interview, references from previous or present employers, and certificates of training in the audit area. A resume or an Experience/Education form (Attachment 7.1) shall be used to substantiate these qualifications.

5.1.2. Personnel selected for auditing assignments must possess educational experience and training qualifications commensurate with the scope, complexity, or special nature of the activities to be audited.

5.1.3. The documentation of qualifications of Auditors assisting HFC from another company shall be evaluated. This evaluation will

be made by the Quality Assurance Manager or his designee to determine which qualifications are acceptable and what additional training is required, if any, to achieve the required level of competence for auditing activities.

5.2. Record of Auditor Evaluation

5.2.1. To assist in determining the qualifications of prospective Auditors, the Record of Evaluation (Attachment 7.2) shall be used. The record shall be filed in the individual's certification file after being completed.

5.2.2. The prospective Auditor shall have verifiable evidence that a minimum of ten (ten) points under the following scoring system have been accumulated. Personnel failing to achieve ten (10) points will be considered Auditors-in-Training.

1. Education (Maximum five (5) points)

High school graduate (GED), score one (1) point. Associate degree from an accredited institution, score two (2) points, or if the degree is in engineering, physical sciences, mathematics, or quality assurance, score three (3) points. Bachelors degree from an accredited institution, score three (3) points; if the degree is in engineering, physical sciences, mathematics, or quality assurance, score one (1) additional point. Masters degree, score four points; if the degree is in engineering, physical sciences, business management, or quality assurance, score one (1) additional point.

2. Experience (Maximum nine (9) points)

Technical experience in construction, engineering, manufacturing, operations, or maintenance, score <u>one</u> (1) point for each full year with a maximum of three (3) points for this aspect of experience.

Technical experience in quality assurance inspection, test or examination for manufacturing, construction, or operations, score one (1) point plus one (1) additional point for each full year of experience with a maximum of three (3) points.

If one (1) or more years of this experience has been in nuclear quality assurance inspection, test, or

examination, score one point for each year with a maximum of four (4) points, or

If one (1) or more years of this experience has been in quality assurance auditing for manufacturing, construction, or operations, score three (3) points plus one (1) point for each year with a maximum of five (5) points, or

If the individual has verifiable evidence of experience in nuclear quality assurance auditing, but does not qualify for Lead Auditor status, score four (4) points plus one point for each year in this capacity.

3. Other Credentials of Professional Competence (Maximum two (2) points)

   Certification of competency in engineering, science, quality assurance specialties, or auditing issued and approved by a state agency or national professional society, score two (2) points.

4. Capability Testing (Maximum two (2) points)

   For each examination successfully completed within the HFC quality program pertinent to audit activities, score one (1) point.

5. Specialized Training (Maximum two (2) points)

   For each special quality assurance training course pertinent to the audit activity, score one-half point.

6. Rights of Management (Maximum two (2) points)

   The Quality Assurance Manager or Lead Auditor may grant up to two (2) points for other performance factors applicable to quality assurance auditing which may not be explicitly delineated in this practice. Examples of these factors are leadership, sound judgment, maturity, analytical ability, past performance, communication skills (oral and written), etc.

5.3. Training

5.3.1. Audit personnel shall receive appropriate orientation or training to ensure their competence in performing audits. The extent of orientation or training will be determined by the Quality Assurance Manager or Lead Auditor through personal interview and documented evidence of the Auditor's education and experience as indicated on his/her resume.

5.3.2. Training shall consist of formal and/or informal (on-the-job and/or home study) training. The applicability of formal versus informal training is determined through comparing the individual's experience and his/her level of competence, as evidenced through testing and demonstrated knowledge, references from previous employers, or certificates of training from educational institutions pertinent to auditing activities.

5.3.3. Auditors-in-training shall receive sufficient on-the-job training, guidance, and counseling under the direct supervision of a Lead Auditor until a satisfactory level of competence in auditing activities has been achieved.

5.3.4. All audit personnel shall receive formal or informal orientation and/or training so as to achieve a working knowledge and understanding of applicable codes, standards, and regulations, and the applicable auditing procedure before being assigned to an audit team.

5.3.5. Attendance records shall support all training and/or orientation sessions, number of hours, dates, lesson outline, and scope.

5.3.6. A training course outline should be developed to specify the topics in the auditing body of knowledge that will be addressed during the training of audit personnel.

5.4. Examination

5.4.1. All auditors-in-training shall successfully complete a written examination to evaluate their comprehension of, and ability to apply, the body of knowledge pertinent to quality assurance auditing.

5.5. Certification

5.5.1. Upon completion of the training and qualification process, the Auditor's qualification shall be documented on the Record of Auditor Evaluation (Attachment 7.2). This document shall serve as permanent documentation of the Auditor's certification.

5.6. Maintenance of Qualification

5.6.1. Auditors shall maintain their qualifications through participation in audits, review and study of codes, standards, procedures, instructions, and other documents related to quality assurance programs and program auditing, formal and informal training on subjects pertinent to quality assurance programs, and review of the Auditor's training course.

6.0 QA RECORDS

6.1. The following records shall be maintained in accordance with QPP 17.1, "Quality Records":

6.1.1. Experience/Education Summary

6.1.2. Record of Evaluation

7.0 ATTACHMENTS

7.1. Experience/Education Summary

7.2. Record of Evaluation

Auditor Qualification

ATTACHMENT 7.1

HFC

QUALITY ASSURANCE

EXPERIENCE/EDUCATION SUMMARY FORM

Name _____ Group _____

Discipline _____ Date _____

EXPERIENCE

Employer	Project Description	Level	Time Period

TRAINING COURSES

Employer	Description	Length

Auditor Qualification

ATTACHMENT 7.2

RECORD OF EVALUATION

Name: _____ Discipline/Level: _____

SECTION	QUALIFICATION POINTS	CREDIT
I. Education (Select Highest Level Attained – Five Points Maximum)		
1. High School or GED	One Point	_____
2. Associate Degree	Two Points	_____
3. Associate Degree (Eng., Science, Math, Physics, QA)	Three Points	_____
4. Bachelors Degree	Three Points	_____
5. Bachelors Degree (Eng., Science, Math, Physics, QA)	Four Points	_____
6. Masters Degree	Four Points	_____
7. Masters Degree (Eng., Science, Math, Physics, QA)	Five Points	_____
		Sub-total _____
II. Experience (Engineering, Manufacturing, Construction, Operation, or Maintenance - 9 Points Maximum)		
1. Non-QA General	One Point Per Year – Four Points Maximum	_____
2. Non-QA Nuclear	One Point + One Point/Year – Six Points Maximum	_____
3. QA General	Two Points + One Point/Year	_____
4. QA Nuclear	Three Points + One Point/Year	_____
		Sub-total _____
III. Credentials of Professional Competence (Two Points Maximum)		
1. P.E. _____	Two Points	_____
2. Society _____	Two Points	_____
		Sub-total _____
IV. Capability Testing (Two Points Maximum)		
1. _____	2. _____	
3. _____	4. _____	Subtotal _____
V. Specialized Training (.5 Points Course – Two Points Maximum)		
1. _____	2. _____	
3. _____	4. _____	Subtotal _____
VI. Management Option (Explain)	Points (Two Points Maximum)	Subtotal _____

Evaluated By: Date:

VII. Total Points Awarded _____ Points

Qualification Evaluated By: _____ Date: _____

(Comments)

HFC

NON-PROPRIETARY

QUALIFICATION OF INSPECTION PERSONNEL

QUALITY PROCESS PROCEDURE

Procedure No. **QPP 2.5** Revision: **B**

Effective Date: **7/27/04**

Prepared By: TODD LEFFINGWELL

Reviewed By: JONATHAN TAYLOR

Approved By: C.E. FISHER

Qualification of Inspection Personnel

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Qualification of Inspection Personnel

1.0 PURPOSE AND SCOPE

1.1. The purpose of this procedure is to define the requirements for training, qualification, and certification of personnel who perform inspections, examinations, and tests that verify quality.

1.2. This section applies to HFC personnel who will be assigned to perform inspections, examinations, and tests as a part of a quality related activity undertaken by HFC in accordance with the HFC Quality Assurance Program, and who are required by contract, code, specification, or program to be qualified and certified to perform such inspections, examinations, and tests.

2.0 ORGANIZATIONAL RESPONSIBILITIES

2.1. The Quality Assurance Manager / Designee is responsible for training, qualification, and certification of Quality Control personnel in accordance with the requirements of this procedure.

3.0 REFERENCES

3.1. QPP 17.1, "Quality Records"

4.0 GENERAL INFORMATION

4.1. The contractual or technical requirements of some HFC projects may require that a specific work instruction be developed to address project requirements. The Project Quality Plan shall identify project unique instructions.

4.2. Quality Control Inspectors are qualified as Electro-Mechanical Inspectors and their training allows them to perform Receipt, In-Process, and Final Inspections of electrical and mechanical parts and assemblies.

5.0 PROCEDURE

5.1. Levels of Capability

5.1.1. The minimum capabilities that qualify personnel to perform receipt, in-process, and final inspections and acceptance tests are divided into three basic levels. The requirements for each level are not limited with regard to organizational position, or professional status, but are limited with regard to functional activities as defined on the Minimum Levels of Capability Chart (Attachment 7.1).

1. Level I - A Level I person shall be capable of performing the inspections, examinations, and tests that are required to be performed in accordance with documented procedures and/or industry practice. The individual must be capable of

interpreting technical documents (drawings, specifications, etc.) and shall have demonstrated proficiency in the use of the tools and equipment to be employed in accomplishing the assigned tasks. The Level I individual shall be capable of determining that the calibration status of inspection and measuring equipment is current, in proper condition for use, and that the inspection, examination, and test procedures are approved. (See Practical Test for specifics) The Level I individual shall report to a Level II or Level III inspector, qualified during the course of inspections and tests. All inspections performed and signed off by a Level I person shall be reviewed and signed by at least a Level II individual.

2. Level II - A Level II person shall have all the capabilities of a Level I person for the inspection, examination, and test category or class in question. The individual shall have demonstrated capabilities in setting up inspections and tests with the necessary equipment, planning, supervising, or maintaining surveillance over the inspections, examinations, and tests together with reporting and evaluating the validity and acceptability of the results. The Level II shall be capable of supervising lower level personnel and be responsible to a Level III individual.

3. Level III - A Level III person shall have all of the capabilities of a Level II person for the inspection, examination, or test discipline, class, or category applicable to the work. The individual shall also be capable of evaluating the adequacy of specific programs used to train, test and qualify inspection, examination, and test personnel for certification to the indicated level. The Level III shall be proficient in: establishing and approving test, examination, and inspection procedures; interpreting specifications, standards, and codes; designating proper techniques for specific tests and inspections. The individual shall be responsible for supervising and certifying lower level personnel.

4. Trainees - Trainees may be used for a project as determined by the HFC Quality Assurance Manager or Level III for inspection, examination, and test. Specific limitations governing the use of the trainees will be defined in the Project Quality Plan or specific Work Instructions. A trainee shall receive the required amount of classroom and on-the-job training and successfully pass the required examination(s) for the test or inspection method to which he/she is to be assigned. In the performance of his/her assigned duties, the trainee is directly responsible to a cognizant Level II or III, and shall not perform final acceptance test, examination, or inspection.

5.2. Limited Certification

5.2.1. Persons may be certified to perform limited work functions for which they are qualified. The training, experience, and certification requirements for limited certification by specific function and level will be specified in the Project Quality Plan or specific Work Instructions. Examples of limited certifications could be Receiving Inspection limited to hardware, but excluding document review. Personnel qualified as Level I, II, or III inspection, examination, and test personnel shall have education and experience requirements commensurate with their specific level. The education and experience requirements specified herein, for the various levels should not be treated as absolute, when other factors provide reasonable assurance that a person can competently perform a particular task. Other factors may be a demonstrated capability in a given job through previous performance or satisfactory completion of proficiency testing. The HFC Quality Assurance Manager or the responsible Level III on the Record of Evaluation shall document these other factors when the education and experience factors are waived for a particular individual.

5.3. Education, Experience, and Training

5.3.1. Level I Personnel

1. Completion of college work leading to an Associate Degree in a related discipline plus three (3) months of related experience in equivalent inspection, examination or testing activities, or;

2. High school graduate, plus six (6) months of experience in quality assurance, including testing and/or inspection of equivalent construction and/or installation activities, or;

3. Two (2) years of related experience in equivalent inspection, examination, or testing, and;

4. Completion of formal classroom training, when required, and successfully passing Level I examinations.

5.3.2. Level II Personnel

1. Graduate of a four-year accredited college or university, plus six (6) months experience in quality assurance/quality control including inspection, examination or testing activities, or;

2. Completion of college level work leading to an Associate Degree in a related discipline plus one (1) year related experience in equivalent inspection, examination, or test activities, or;

3. One (1) year satisfactory performance as Level I in the corresponding inspection, examination, or test category or class, and

4. Completion of formal classroom training, as required, and successfully passing Level II examination(s).

5.3.3. Level III Personnel

1. Graduate of a four-year accredited college or university, plus five (5) years experience in quality assurance/quality control including inspection, examination, and testing. At least two years of this experience should be associated with nuclear facilities, or if not, the individual shall receive sufficient training in the relevant quality assurance aspects of safety-related work, or;

2. Completion of college level work leading to an Associate Degree and seven (7) years of related experience in equivalent inspection, examination, and testing activities, with at least two (2) years experience associated with nuclear facilities, or, if not, sufficient training to be acquainted with the relevant quality assurance aspects of a nuclear facility, or;

3. High school graduate plus ten (10) years related experience in equivalent inspection, examination, and testing activities, or high school graduate plus eight (8) years experience in equivalent activities, with at least two (2) years associated with nuclear activities, or, if not, at least sufficient training to be acquainted with the relevant quality assurance aspects of a nuclear facility, or;

4. Six (6) years of satisfactory performance as a Level II in the corresponding inspection, examination, or test category or class.

5.4. Training

5.4.1. Personnel to be certified in a particular method, or advancing to a higher certification level shall receive sufficient formal and on-the-job training in that method. The presentation of training may be accomplished either as formal (classroom) or informal (home study) training. The applicability of formal versus informal training is determined through comparing the individual's previous education, experience, and level of competence, as evidenced through a demonstrated knowledge of the activity, references from previous or present employers, or certificates from training or educational institutions with the requirements of the position.

5.4.2. Formal training course(s) shall be of duration consistent with the complexity and importance of the method. The training course(s) may be presented in multiple sessions. Training course(s) shall be based on:

1. The job description (functional) of the position performing the method.

2. The objective of the course.

3. The probable entry level of the participants

4. A course outline provides the means of fulfilling the stated objectives.

5.4.3. Training may be administered by organizations outside of HFC such as: universities, colleges, technical associations, and consultants, trade associations, professional technical societies, or electric utilities. Copies of training outlines, course schedules, or course material shall be supplied to indicate the basis and level of material presented.

5.4.4. Informal training shall consist of either home study and/or on-the-job training. Home study consists of providing the individual with sufficient materials or references to read or review at home or at work when time permits. Programmed home study courses or computer-based home study may also be employed to provide informal training. On-the-job training shall consist of first hand experience gained through actual performance under the observation and instruction of a Level II or III. If necessary, a review should be held at the end of the informal training prior to examination.

5.4.5. For newly hired individuals, whose previous experience in performance of inspections, examinations, and/or tests can be substantiated and documented, formal training may be waived. These personnel may be required to pass an examination as specified in this program.

5.4.6. When training is used as a basis for certification, records of training will be maintained.

5.5. Evaluation and Certification of Personnel

5.5.1. When an individual is hired or a current inspection, examination, and test quality person is to be evaluated for advancement to a higher qualification level, a Qualification Evaluation Form (Attachment 7.2) will be completed. This form will document the current qualifications of the individual for assessment in accordance with the following:

1. Level I - The candidate shall have Quality Assurance Inspection/Test experience and present evidence that a minimum of five (5) points under the scoring system shown in the Instructions for Completing Qualification Evaluation Form for Inspection, Examination, and Test Personnel, (Attachment 7.3). A minimum of one (1) point must come from Section I and a minimum of two (2) points must come from Section II.

2. Level II - The candidate shall have Quality Assurance Inspection/Test experience and present viable evidence for an accumulation of a minimum of ten (10) points under the scoring system shown on the Instructions for Completing Qualification Evaluation Form for Inspection, Examination, and Test Personnel, (Attachment 7.3). A minimum of one (1) point must come from Section I and a minimum of four (4) points must come from Section II.

3. Level III - The candidate shall have Quality Assurance Inspection/Test experience and present viable evidence for an accumulation of a minimum of fifteen (15) points under the scoring system shown on the Instructions for Completing Qualification Evaluation Form for Inspection, Examination, and Test Personnel, (Attachment 7.3). A minimum of one (1) point must come from Section I and a minimum of eight (8) points must come from Section II.

4. The evaluation, including Section VI, "Rights of Management" shall be performed by the Quality Assurance Manager or by a person with written authorization from the Quality Assurance Manager.

5.6. Examination

5.6.1. After completion (or waiving) of training, personnel may be tested to demonstrate their knowledge and competence in a particular method.

5.6.2. This testing includes a "General" test which covers fundamentals, practices, codes, and standards which are generally related to the respective method; a "Specific" test which can be administered open book and covers the specific codes, standards, and specifications to be used to accomplish a particular project; and a "Practical" test shall be given for a practical demonstration of proficiency. The "Practical" shall specify the types of inspections necessary to perform a receipt, in-process, and a final inspection.

5.6.3. The testing shall be administered and graded by a qualified individual (Quality Assurance Manager, Level III or other designated person appointed by the Quality Assurance Manager).

5.6.4. Personnel, other than those performing inspection and/or testing functions may be tested to demonstrate their capability in particular methods. This testing need not be comprised of "General", "Specific", and "Practical" sections, but may consist of a single, one part test developed from the applicable work instruction.

5.6.5. Grading of the tests shall be accomplished by the use of percentile weights, as defined for each test for a Level. These weights are as follows:

1. Level I: General 0.4, Specific 0.3, Practical 0.3
2. Level II: General 0.4, Specific 0.3, Practical 0.3
3. Level III: General 0.4, Specific 0.6,

5.6.6. The composite grade is determined as follows:

1. Gc = (Gg x Wg) + (Gs x Ws) + (Gp x Wp) Where:
2. Gc = Composite Grade
3. Gg = Actual General Examination Grade
4. Wg = Assigned Percentile Weight for General
5. Gs = Actual Specific Examination Grade
6. Ws = Assigned Percentile Weight for Specific
7. Gp = Actual Practical Examination Grade
8. Wp = Assigned Percentile Weight for Practical

5.6.7. For Levels I and II, a composite grade of 80 or better is required for passing. No grade of the test(s) given shall be less than 70 percent. For Level III, a composite grade of 85 or better is required with no individual grade below 80 percent.

5.6.8. Personnel who fail to pass any test may be re-examined after waiting at least thirty (30) days. Re-examination may occur sooner than thirty days if the candidate receives additional training and/or classroom instruction. Approval for waiver of the thirty-day waiting period shall be made by the Quality Assurance Manager, the responsible Level III, or an individual authorized to do so by the either of the two individuals named previously.

5.7. Physical Capabilities Examination

5.7.1. An examination shall be given to assure natural and near

distance visual acuity such that the individual is capable of reading a minimum of Jaeger Number 1 letters at a distance of not less than twelve (12) inches (30.5 cm) on a standard Jaeger/Snellen Reading Card. The ability to read an Ortho-Rater minimum of 10 or equivalent tests is also acceptable.

5.7.2. The individual shall be capable of distinguishing and differentiating contrast between colors as demonstrated by a practical examination (i.e.: Ishihara 25 Plate Practical Test for Color Blindness), or other test performed for the method for which the individual is to be qualified.

5.7.3. An individual certified in accordance with this program shall possess adequate health and physical mobility to perform the assigned tasks.

5.7.4. Eye examinations (visual acuity and color blindness) shall be administered at the time of initial certification and annually thereafter by qualified personnel trained to perform such tests. The results of the annual eye examinations shall be documented on an eye examination form supplied by the eye care professional or on Attachment 7.5.

5.8. Certification

5.8.1. After completion of training and examination for a method, certification shall be documented using a Certification Record Form (Attachment 7.4). A personal resume or experience / education summary shall be prepared and available for each individual.

5.8.2. Certifications shall be terminated when an individual leaves HFC for any reason other than lack of work. Certifications for individuals laid-off shall remain valid for 180 days from their transfer/separation date.

5.9. Performance

5.9.1. Personnel who are assigned the responsibility and authority to perform functions covered by this section shall have as a minimum the level of capability shown on the Minimum Levels of Capability Chart (Attachment 7.1).

5.9.2. When a single inspection or test requires implementation by a team or group, personnel not meeting the requirements of Level I may be used in data-taking assignments or in equipment operation, provided they are supervised or overseen by a qualified individual participating in the inspection, examination, or tests.

5.9.3. Whenever a certified individual's performance is unsatisfactory,

the Quality Assurance Manager shall remove that individual from that activity until such time as the required capability has been demonstrated followed by re-examination and re-certification.

5.9.4. The performance of certified personnel shall be re-evaluated every three (3) years. The personnel shall be re-certified based on this evaluation. Those personnel who demonstrate continuous satisfactory performance may be re-certified with no training or examination.

5.9.5. Any certified individual who has not performed inspection, examination, or testing activities in their qualified area for a period of one (1) year shall be re-evaluated by a re-determination of required capability. The Quality Assurance Manager will document this re-evaluation.

6.0 QA RECORDS

6.1. The following records shall be maintained in accordance with QPP 17.1, Quality Records:

6.1.1. Record of Evaluation and Certification.

6.1.2. Basic education, training, and experience records.

6.1.3. Copies of examinations taken for respective methods.

6.1.4. Reports of required physical examinations.

6.1.5. Records of periodic evaluations.

6.1.6. Records of retraining, re-examination, and/or recertification.

7.0 ATTACHMENTS

7.1. Minimum Levels of Capability for Inspection, Examination, and Test Personnel (General Functions)

7.2. Record of Evaluation

7.3. Instructions for Completing Record of Evaluation Form

7.4. Certification Record, Inspection Personnel

ATTACHMENT 7.1

Minimum Levels of Capability for Inspection, Examination, and Test Personnel (General Functions)

General Function	Level I	Level II	Level III
Recording Inspection, Examination and Testing Data	X	X	X
Implementing Inspection, Examination, and Testing Procedures	X	X	X
Interpret Drawings and Specifications	X	X	X
Planning Inspections, Examinations, and Tests		X	X
Setting up Tests and Tests Equipment		X	X
Evaluating the Validity and Acceptability of Inspection, Examination, and Testing Results		X	X
Reporting Inspection, Examination, and Testing Results		X	X
Supervising Equivalent or Lower Level Personnel		X	X
Qualifying Lower Level Personnel			X
Evaluating the Adequacy of Specific Programs Used To Train and Test Inspection, Examination, and Testing Personnel			X
Qualifying Same Level Personnel			X

Qualification of Inspection Personnel

ATTACHMENT 7.2

RECORD OF EVALUATION

Name: _____ **Level:** _____

SECTION	QUALIFICATION POINTS	CREDIT
I. Education (Select Highest Level Attained – Five Points Maximum)		
1. High School or GED	One Point	_____
2. Associate Degree	Two Points	_____
3. Associate Degree (Eng., Science, Math, Physics, QA)	Three Points	_____
4. Bachelors Degree	Three Points	_____
5. Bachelors Degree (Eng., Science, Math, Physics, QA)	Four Points	_____
6. Masters Degree	Four Points	_____
7. Masters Degree (Eng., Science, Math, Physics, QA)	Five Points	_____
		Sub-total _____
II. Experience (Engineering, Manufacturing, Construction, Operation, or Maintenance - 9 Points Maximum)		
1. Non-QA General	One Point Per Year – Four Points Maximum	_____
2. Non-QA Nuclear	One Point + One Point/Year – Six Points Maximum	_____
3. QA General	Two Points + One Point/Year	_____
4. QA Nuclear	Three Points + One Point/Year	_____
		Sub-total _____
III. Credentials of Professional Competence (Two Points Maximum)		
1. P.E. _____	Two Points	_____
2. Society _____	Two Points	_____
		Sub-total _____
IV. Capability Testing (Two Points Maximum)		
1. _____ 2. _____		
3. _____ 4. _____		Subtotal _____
V. Specialized Training (.5 Points Course – Two Points Maximum)		
1. _____ 2. _____		
3. _____ 4. _____		Subtotal _____
VI. Management Option (Explain)	**Points (Two Points Maximum)**	**Subtotal** _____

Evaluated By: **Date:**

VII. Total Points Awarded _____

Qualification Evaluated By: _____ **Date:**_____

(Comments)

ATTACHMENT 7.3

Instructions for Completing Record of Evaluation Form

The following are instructions for completing the Record of Evaluation form used to document the evaluation of a candidate's education, experience, credentials of professional competence, and the results of capability testing, specialized training, and management assessment of factors not specified in the Record of Evaluation form.

SECTION I

Education – (Maximum five points)

High School Graduate or GED – Score one point. Score two points for an Associate degree; or, three points if the Associate degree is in engineering, physical sciences, mathematics, or quality assurance. Score three points for a Bachelors degree or four points if the degree is in engineering, physical sciences, mathematics, or quality assurance. Score four points for a Masters degree or five points if the Masters degree is in engineering, physical sciences, mathematics, or quality assurance.

SECTION II

Experience – (Maximum nine points)

Technical experience in engineering, manufacturing, construction, operation, or maintenance score one point for each full year with a maximum of four points for experience, or;

If one or more years of this experience have been in the nuclear profession, score one additional point plus one additional point for each additional year of nuclear experience with a maximum of six points, or;

If one or more years of this experience have been in quality assurance inspection and testing for manufacturing or construction, score two additional point plus one additional point for each additional year, or;

If one or more years of this experience have been in nuclear quality assurance inspection and testing for manufacturing or construction, score three additional points plus one additional point for each additional year.

SECTION III

Other Credentials of Professional Competence – (Maximum two points)

Certification of competency in engineering, physical science, or quality assurance specialties, including nondestructive testing, issued and approved by a Level III and/or state agency or National Professional Society, score two points.

ATTACHMENT 7.3

Instructions for Completing Record of Evaluation Form (Con't)

SECTION IV

Capability Testing – (Maximum two points)

For each examination successfully completed within the HFC NDE Center Certification
Program scores one point. For more than one successfully completed examination, score two points.

SECTION V

Specialized Training – (.5 point per course – Maximum two points)

For each specialized Quality Assurance training course completed score .5 points.

SECTION VI

Rights of Management – (Maximum two points)

The Quality Assurance Manager, or designee, may grant up to two points for other performance factors applicable to Quality Assurance Engineering or Inspection that may not be explicitly called out in this procedure.

Qualification Evaluation – The completed evaluation form shall be evaluated by the Quality Assurance Manager, responsible Level III, or other individual(s) authorized by the Quality Assurance Manager.

ATTACHMENT 7.4

Certification Record
Inspection Personnel

Name of Certified Individual:_____

Level of Certification:_____

Examination	Exam Date	Grade	Weight	Weighted Grade	Examiner
Written - General					
Written - Specific					
Practical					
Composite Grade					

Certification Notes:

☐ In accordance with the requirements of the HFC Quality Assurance Program, the above-named individual has satisfactorily completed the required training and passed the examinations for the level of certification listed above.

☐ The above named individual was examined as noted on the attached document(s) and was found to meet the physical requirements for certification.

Training:

Course	Company	Date	Hours	Instructor

Certification By:_____ **Date:**_____

Re-certification:

Re-certify By / Date:					
Initials:					
Date:					

ATTACHMENT 7.5

VISUAL ACUITY RECORD

NAME:	**SSN**:	:

A. NEAR VISION ACUITY

1. ☐ JAEGER J-1 SCALE L ____ R ____ ☐ OTHER (Specify) _____
2. ☐ UNCORRECTED ☐ CORRECTED (Specify) Contacts ☐ Glasses ☐
3. ☐ PASSED ☐ FAILED*

B. DISTANT VISION ACUITY

1. ☐ SNELLEN L ____ R ____ ☐ OTHER (Specify) _____
2. ☐ UNCORRECTED ☐ CORRECTED (Specify) Contacts ☐ Glasses ☐
3. ☐ PASSED ☐ FAILED*

C. COLOR VISION

1. ☐ ISHIHARA ☐ OTHER (Specify) _____
2. NUMBER OF PLATES TESTED ____ NUMBER CORRECTLY READ ___
3. ☐ PASSED ☐ FAILED*

RECOMMENDATION ☐ PASSED ☐ FAILED

***EXPLAIN ITEM CHECKED**:

_____

_____

VISION TESTS MAY BE CONDUCTED BY ONE OF THE FOLLOWING: QUALIFI4ED OPTOMETRIST, MEDICAL DOCTOR, REGISTERED NURSE (RN/LPN), NDT LEVEL III, ANSI LEVEL III

NAME OF EXAMINER _____ TITLE _____

SIGNATURE _____ DATE OF EXAMINATION _____

LOCATION OF EXAMINATION _____