

Toshiba Corporation

Topical Report of NRW-FPGA- Based I&C System Design Process

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TOSHIBA CORPORATION
NUCLEAR ENERGY SYSTEMS & SERVICES DIV.

September, 2007

Meeting Objectives

- Provide overview and background of Toshiba's **Generic Topical Report** for the Toshiba Non-Rewritable (NRW) Field Programmable Gate Array (FPGA)-Based Instrumentation and Control (I&C) System Design Process.
- Explain technical topics of the FPGA-based systems and Toshiba's process to facilitate USNRC acceptance review of the TR.
- Discuss TR submittal and USNRC Review Process.

Table of Contents

1. Introduction
2. Project Schedule and Project Management
3. Description of Topical Report of NRW-FPGA-Based I&C System Design Process
4. Toshiba's Quality Assurance Process
5. Vendor Evaluations
6. FPGA-Based System Description
7. FPGA Logic Development Lifecycle
8. FPGA Logic Development
9. System Design
10. Verification and Validation Process
11. Hardware Qualification Process
12. Implementing Toshiba's Generic Qualification Process for Application-Specific Equipment
13. Conclusions
14. Questions
15. Discuss USNRC Review Process and Schedule

1. Introduction

Toshiba's Goal

Toshiba FPGA-based I&C Systems are designed as a replacement for the existing analog and microprocessor-based I&C systems in use in safety-related US nuclear applications.

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Toshiba Experience

- Toshiba has extensive Quality Assurance (QA) experience in designing and supplying safety grade systems to Japanese Nuclear Power Plants (NPP).
 - Toshiba has supplied FPGA-based equipment to Japanese Nuclear Power Plants for years. For example,
 - Supplied Process Radiation Monitor* including safety-related system:
 - Fukushima daiichi-2
 - Fukushima daini-1
 - Fukushima daini-3
 - Kashiwazaki Kariwa-1
 - Tsuruga-1
 - Supplied safety-related Power Range Monitor system: Kashiwazaki Kariwa-2
- *This developed qualification process was not applied to safety-related Process Radiation Monitor

These plants are currently in operation.

Project Background

- Original Toshiba plan was to submit TR for the Power Range Monitoring (PRM) System in 2004 and receive USNRC safety evaluation report (SER) in 2005. Toshiba had two review meetings with USNRC on August 20, 2003 and March 1, 2004.
- In Fall 2004 Toshiba reorganized and rescheduled the project. Toshiba requested the USNRC to stop the review process.
- In 2005 Toshiba restarted the qualification project for the FPGA-based PRM system.
- Toshiba had a meeting with USNRC Research Group in July 2006. Based on comments received during this meeting, Toshiba reorganized and divided the TR for the PRM system into generic and specific TRs.
- Toshiba is finalizing the Generic Topical Report (G-TR).
- PRM System qualification testing is in progress.

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2. Project Schedule and Project Management

Project Schedule and Project Management

- **Project Schedule**

- Submittal of G-TR: Toshiba will submit the G-TR to the USNRC for review and approval in October 2007.

- **Project Management**

- Toshiba Design/Engineering Manager: Naotaka Oda
- Toshiba Contact with NRC: Ryuji Iwasaki
- Contact Support : Rossnyev Alvarado
- NRC Project Manager : Vanice Perin

Status of PRM System Qualification

- **PRM System Validation Test Completed in 2006.**
- **PRM System Qualification Testing at Wyle is ongoing.**
Expected completion by end of 2007.
- **Preparation of PRM System Topical Report.**
Fall 2007 / Winter 2008.
- **Submittal of S-TR for PRM System.**
Spring 2008.

3. Description of Topical Report of NRW-FPGA-Based I&C System Design Process

Purpose of Generic Topical Report

Describe Toshiba's lifecycle process for developing FPGA-based I&C systems, and to explain how this process is suitable for US nuclear safety-related applications.

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4. Toshiba's Quality Assurance Process

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Lifecycle Process

- Toshiba's lifecycle process formalizes the interaction between the two organizations for FPGA-based systems by integrating these different QA programs.
- The NED and Fuchu Complex lifecycle is analogous to a software lifecycle and includes the normal features and design outputs of a software lifecycle, including design documentation, verification and validation (V&V) records, change control, and configuration management.

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FPGA System Development Process

- The V&V activities are performed by both NED and Fuchu Complex.
- Fuchu Complex's scope and responsibility for V&V activities are specified in the NED procurement documents.
- NED controls and accepts Fuchu Complex's activities and work products into the NED quality assurance 10 CFR 50 Appendix B process, in accordance with NED's procedures for procurement and commercial grade dedication.

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5. Vendor Evaluations

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6. FPGA-Based System Description

Definition of FPGA

- **FPGA: Field Programmable Gate Array**
 - An FPGA is an integrated circuit that can be logic-implemented.
- **NRW-FPGA: Non-Rewritable FPGA**
 - A type of FPGA that can not be rewritten once logic is implemented.
- **VHDL : Very High Speed Integrated Circuit Hardware Definition Language**

Signal processing functions embedded in an FPGA are composed of physical circuits.

Toshiba uses VHDL to develop the logic for the FPGA.

VHDL is a development language which is similar to conventional programming languages.

Features of FPGA-based I&C System

- Conventional systems have some issues
- FPGA-based systems can resolve these issues

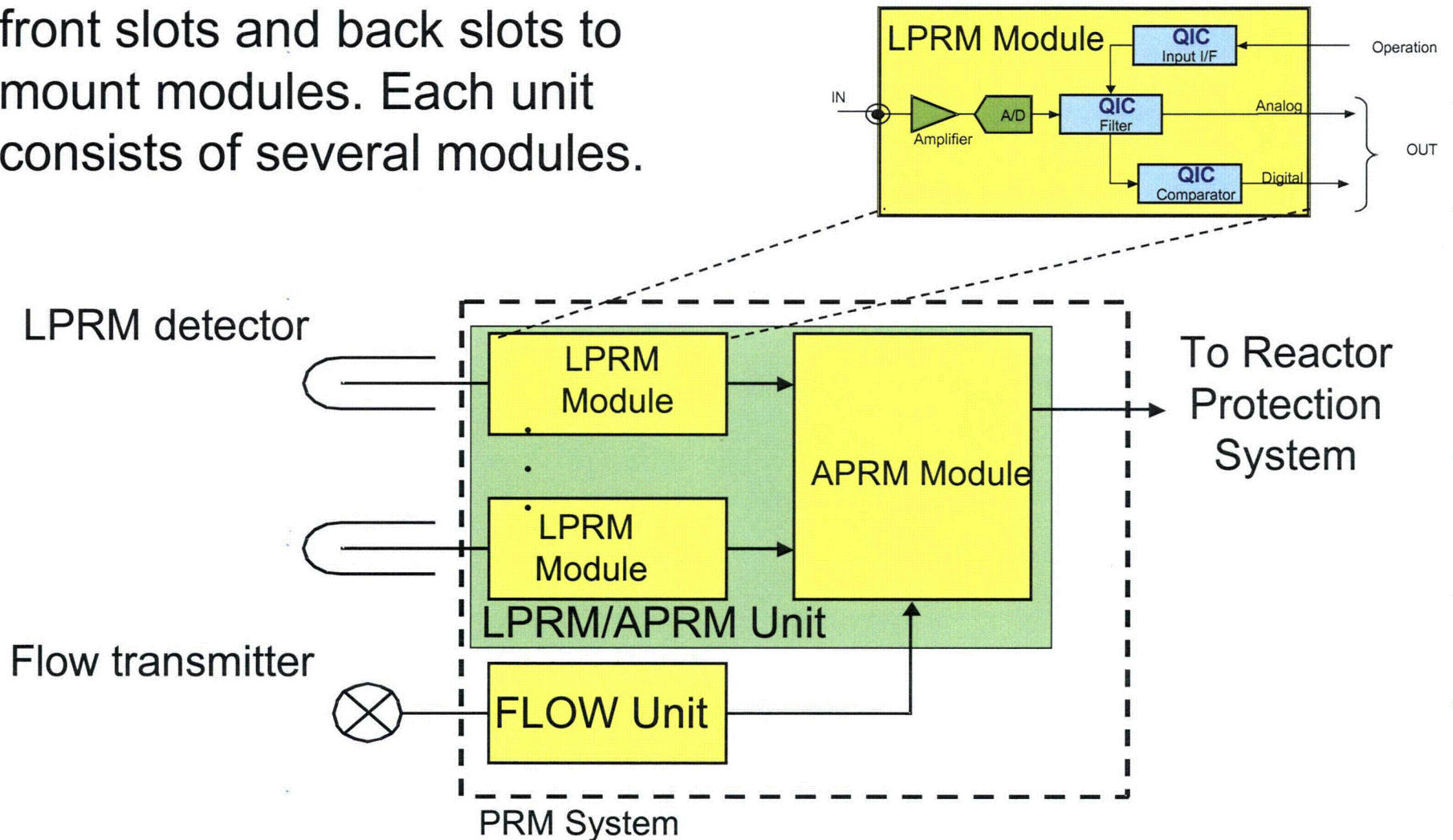
Hardware for I&C	Product Life Cycle	Testability	Operation
Analog-based	Parts obsolescence	OK	Drift
CPU-based	Short life cycle	Complete verification is difficult	OK
FPGA-based	OK Long life support	OK Functional & 100% toggle coverage test	OK Fewer parts, lower temperature

Architecture of FPGA-Based Systems

- FPGA-based systems are constituted of units, which are made from a combination of modules.
- A module, such as a Local Power Range Neutron Monitor (LPRM) module, is constructed of one or more printed circuit boards, which include the FPGAs.
- The FPGAs are built from logical blocks, which are referred to as Functional Elements (FEs).

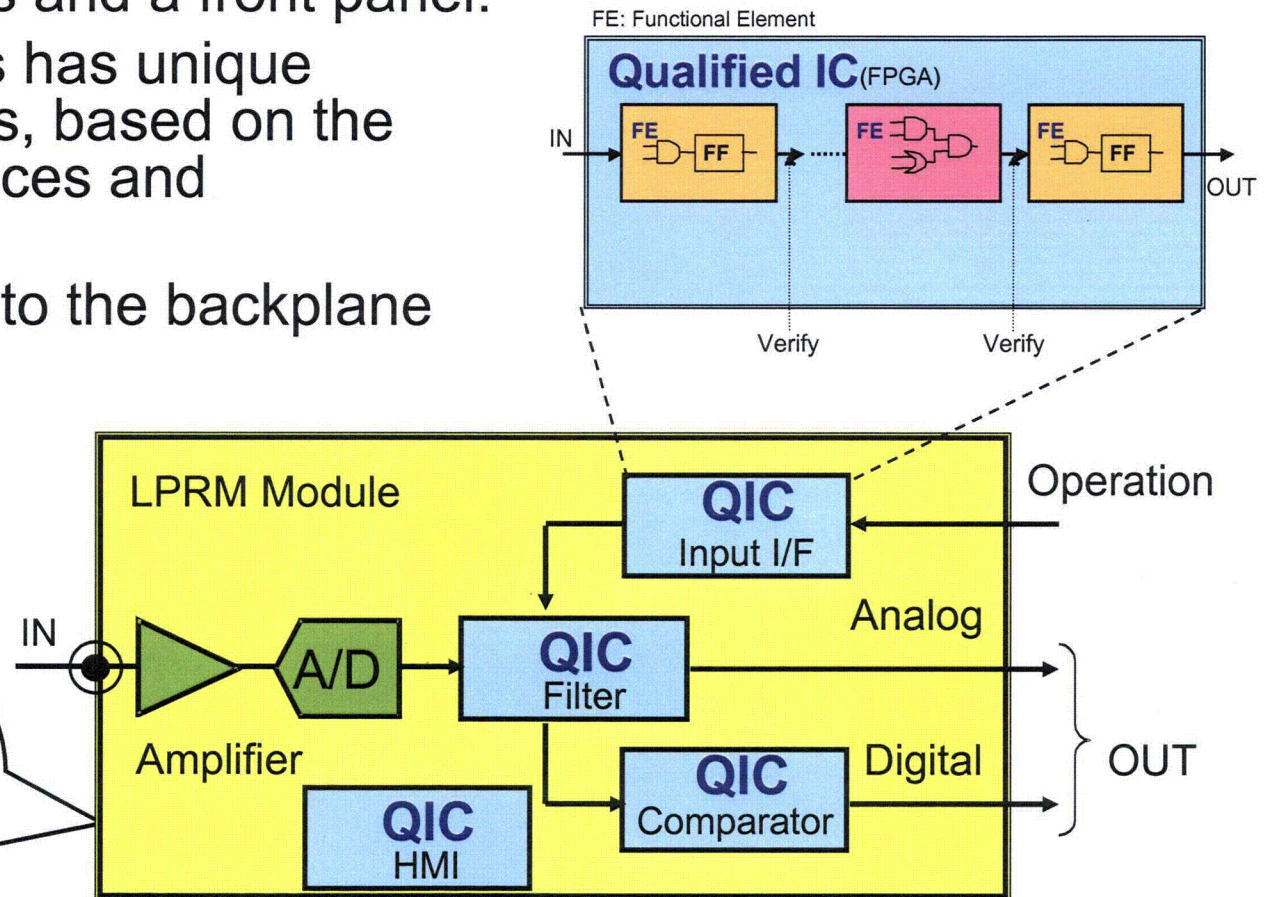
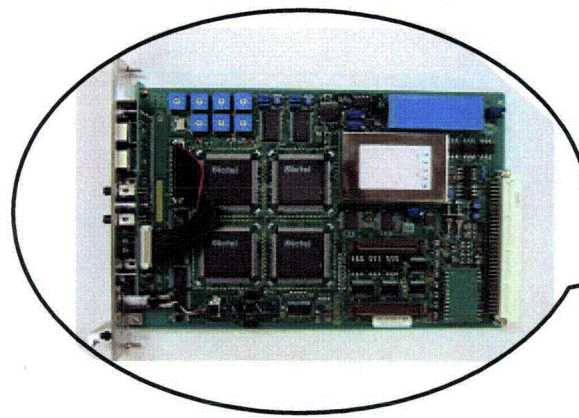
Systems

- The unit is a chassis that has front slots and back slots to mount modules. Each unit consists of several modules.



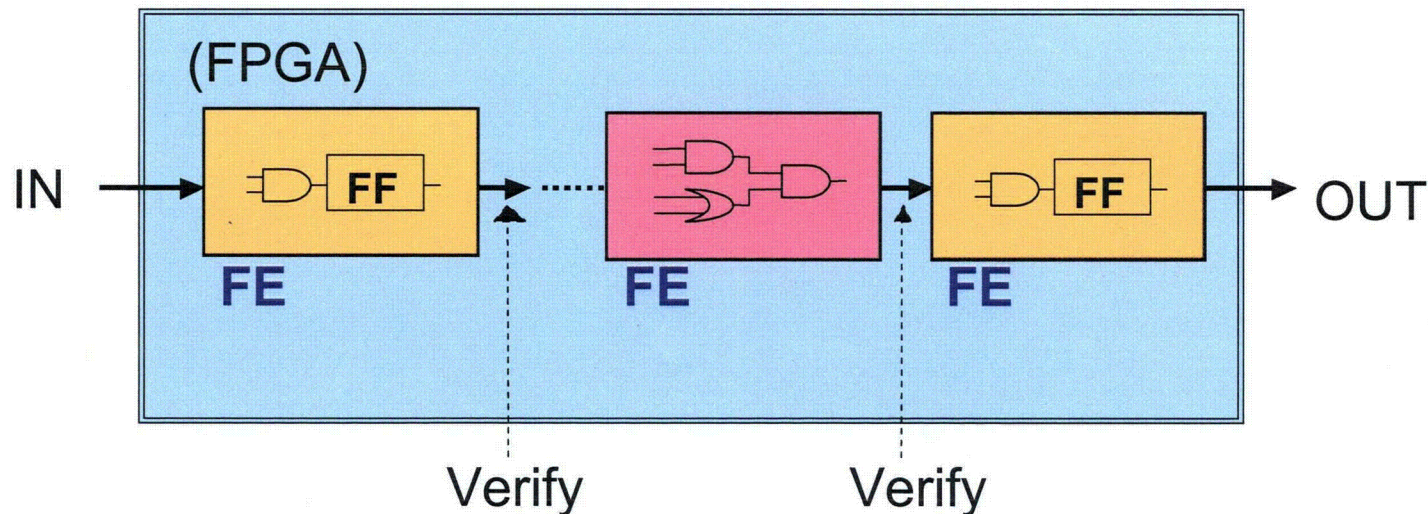
Modules

- Each module consists of one or more printed circuit boards and a front panel.
- Each of the modules has unique architectural features, based on the differences in interfaces and requirements.
- The module plugs into the backplane through connectors.



FPGAs

- An FPGA is a type of logic chip that can be programmed.
- The FEs are connected by logic paths, linked with antifuses, in the circuit diagram. FEs are completely verified by exhaustive pattern tests.
- The FPGAs are non-rewritable, which prevents configuration control problems at the utility.



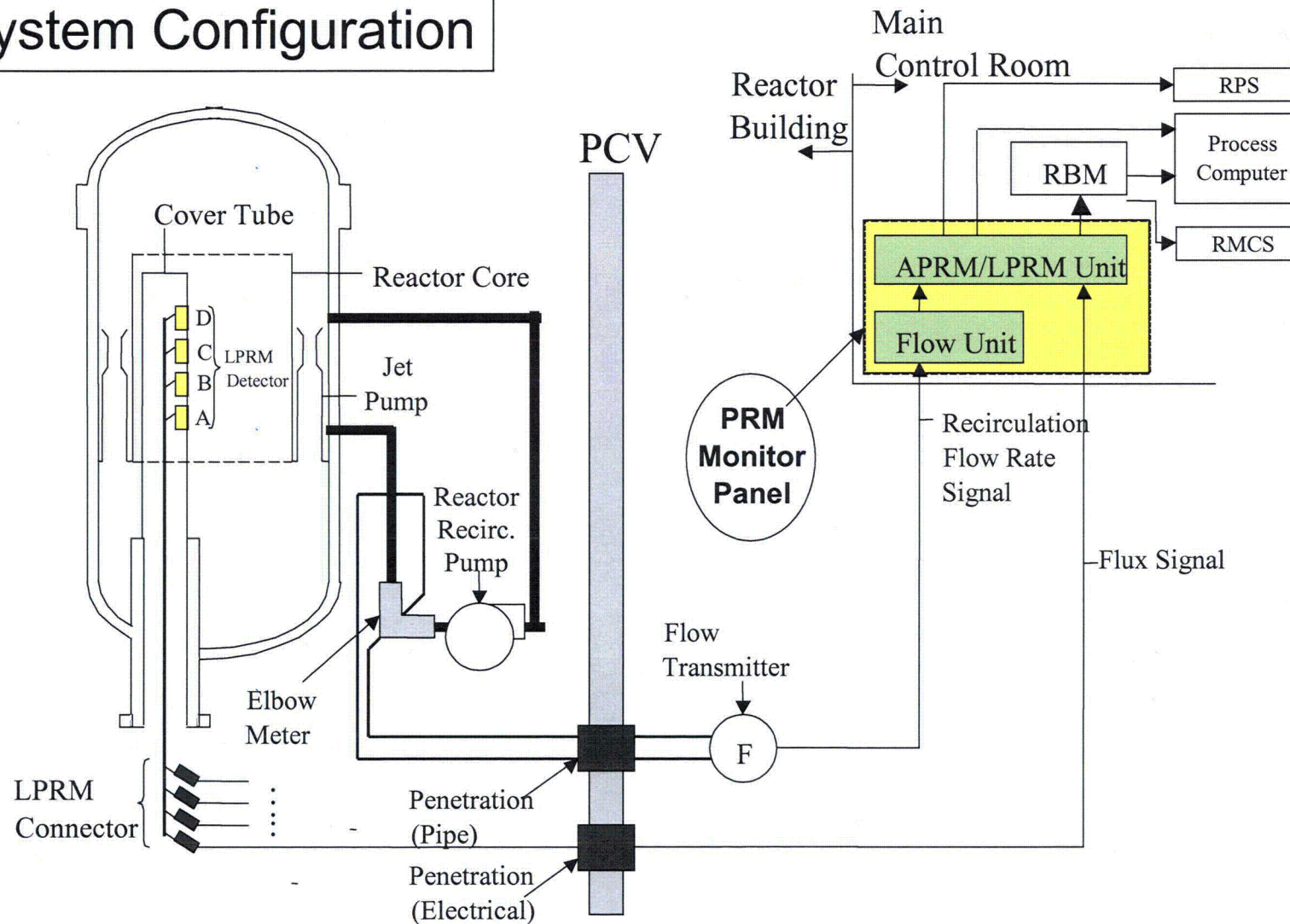
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Example: Power Range Monitor

System Configuration



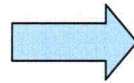
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NRW FPGA Features

- Toshiba uses Actel FPGAs models A54SX72A and A54SX32A
- The FPGAs are one-time programmable devices with antifuse technology.
- Features of the antifuse type FPGA include:
 - Non-volatile
 - Non-rewritable
 - High-speed operation
 - Highly reliable



NRW-FPGA
(Non Re-Writable FPGA)

- Actel FPGA models can only implement digital logic. Therefore, all analog processing and conversion between analog and digital representations occurs in devices attached to the FPGA.
- FPGAs provide stable technology to minimize the risk of technological obsolescence.
- Applications where NRW-FPGAs are used:
 - Satellites, military, aerospace, aircraft, etc.



7. FPGA Logic Development Lifecycle


Development Process

- FPGA-based I&C systems do not use application software
- Toshiba uses VHDL for designing and implementing FPGA circuits



- Toshiba uses a modified software lifecycle approach to logic design

Qualification Approach and Criteria

- **Fundamental Basis for qualification**  **Standard Review Plan (SRP)**
- **Regulations and industry standards to be applied for the qualification process:**
 - EPRI TR-107330
 - EPRI TR-106439
 - IEEE Standard 7-4.3.2
 - BTP HICB-14 and HICB-18
 - USNRC Regulatory Guide (RG) 1.152
 - IEEE Standard 1012
- **Cyber Security**

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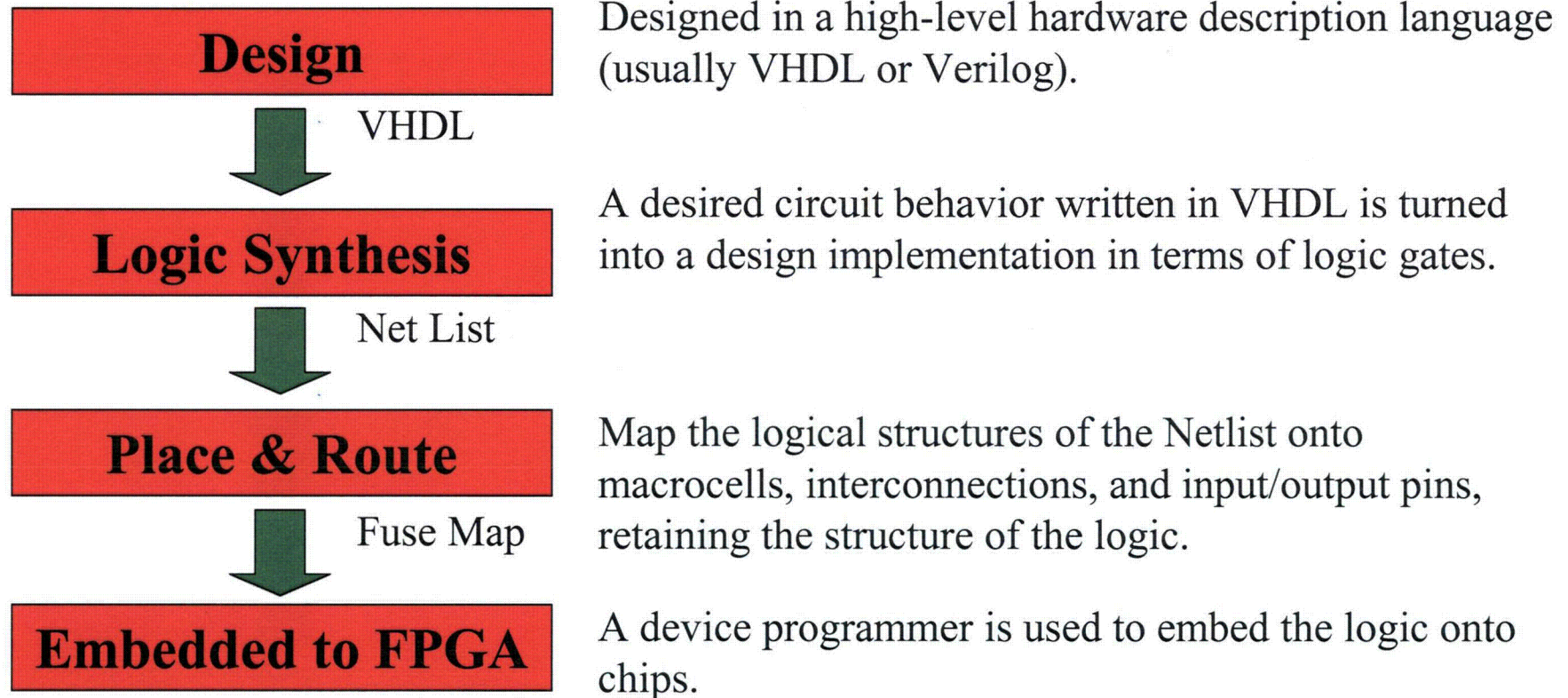
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8. FPGA Logic Development

Developing FPGAs

- For each module, NICSD prepares Design Specifications for the FPGAs to be included in the module.
- NICSD uses the Actel Libero® IDE software tools.
- FPGAs are created using a combination of verified and registered FEs.

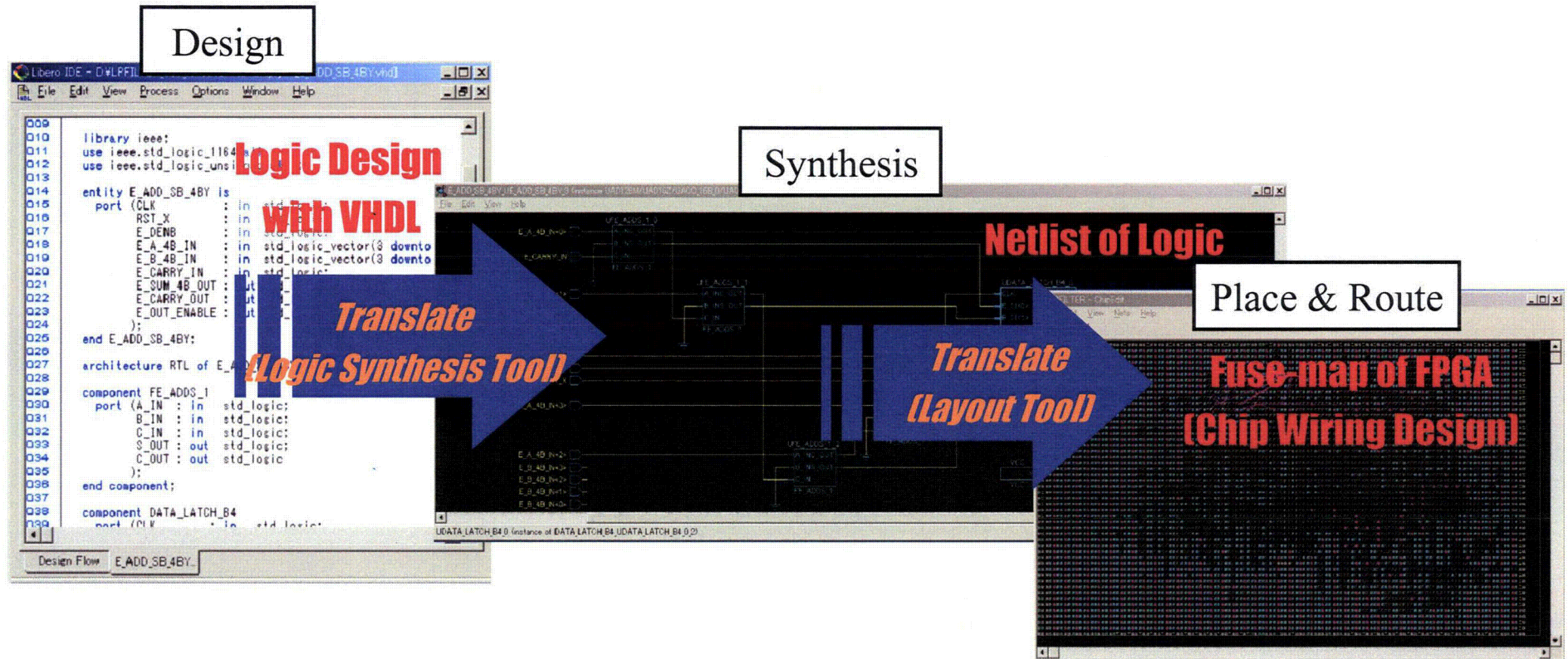
Logic Design Process for FPGA



FPGA Application Tools

- Configuration control of the application tools is conducted based on the configuration management process.
- Each FPGA Application Tool is controlled based on the tool's version.
- NICSD evaluates and accepts new tool versions, and verifies that the new version does not create issues with the existing products.

Logic Design Process for FPGAs



Similar to CPU-based System compile and link.

V&V is performed in compliance with IEEE 1012.

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9. System Design

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Integrating a Unit

- Modules are installed in a chassis.
- Each unit consists of several modules.
- The unit includes front slots and back slots to mount modules.
- Once the unit is assembled, the unit is tested.
- Units are accepted.



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10. Verification and Validation Process

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Validation Tests

1. FPGA Testing
2. Unit/Module Validation Testing
3. System Validation Testing

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11. Hardware Qualification Process

Hardware Qualification - Overview

- Purpose is to demonstrate that the system meets those requirements that can be demonstrated by test and analysis.
- EPRI TR-107330 describes the hardware qualification tests to demonstrate hardware acceptability for safety-related applications. Qualification analyses are also performed.
- For specific applications, NED will confirm that the customer's requirements are bounded by the qualification envelope established by the qualification.

Qualification Tests

- Qualification testing is performed on a Test System which contains a Test Specimen and Test Equipment.
- The test specimen is composed of all the units needed to recreate a typical FPGA-based system.
- The test equipment is used to generate input signals and to monitor the output signals of the test specimen during the qualification type testing.
- Test acceptance criteria are based on the expectations provided in EPRI TR-107330.
- NED prepares a Master Test Plan (MTP). This document identifies the test activities and testing sequence and acceptance criteria.

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12. Implementing Toshiba's Generic Qualification Process for Application-Specific Equipment

Implementation of G-TR

- Toshiba intends to provide NRW-FPGA-based I&C products for safety-related systems in US nuclear power plants.
- Toshiba will use the process specified in this Topical Report to develop and qualify products for new applications or for enhancements to existing products.
- Toshiba will manufacture the equipment for sale to their customers using the same manufacturing, test, and integration methods documented in this Topical Report.
- The G-TR process is implemented when:
 - Toshiba wants to qualify a system.
 - Toshiba wants to manufacture application-specific equipment.
 - Toshiba wants to modify an existing application.

13. Conclusions

Conclusions

- The G-TR describes Toshiba's design, development, test, qualification, and manufacturing processes for NRW-FPGA-based systems for US nuclear safety-related applications.
- Toshiba will submit the G-TR to the USNRC for review and approval in October 2007.
- Toshiba is currently qualifying the PRM system using the description contained in the G-TR.

14. Questions

15. Discuss USNRC Review Process and Schedule

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