# Attachment 1

## 13-JC-ZZ-0204

**Uncertainty of Analog-to-Digital and Digital-to-Analog Converters for Computer Input in ERFDADS, PMS, CPC, and QSPDS, Revision 3**

| PALO VERDE NUCLEAR GENERATING STATION | Calculation | Calculation Number 13-JC-ZZ-0204 | Rev. 3 |
|---|---|---|---|
| | Quality Class Q [X] QAG [ ] NQR [ ] | Pages Affected by Revision 5-6, 10-11, 14-20 | |

Title

# Uncertainty of Analog-to-Digital and Digital-to-Analog Converters for Computer Input in ERFDADS, PMS, CPC, and QSPDS

| Initiating Document(s) | Pending Plant Modifications |
|---|---|
| EDC 2002-00390 | Addendum A - CPC Replacement DMWO 223535 |

Reason for and Description of Revision

DMWO 223535 changes the CPC hardware. The uncertainty of the new hardware is determined in Addendum A of this revision.

There is an input buffer card before the A/D converter for QSPDS. For completeness the uncertainty of this card is included.

Some assumptions or references have slightly added information for improved clarity.

The values supporting the final uncertainty have changed, but the end result, the output of the Calculation has not, therefore there is no impact to other Calculations or documents.

EDC Incorporation: [ ] Direct Revision: [ ] No SWMS Associations Changes: [ ] Category B Software: [ ]

| | |
|---|---|
| Preparer: Kent R. Bjornn — Digitally signed by: Bjornn, Kent R(Z11671) Date: 12/17/2002 15:23:36 Reason: Preparer Location: PVNGS | Mechanical Reviewer: NA |
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| Electrical Reviewer: NA | Independent Verifier: Roxton E. Baker — Digitally signed by: Baker, Roxton E(Z99675) Date: 12/17/2002 15:28:00 Reason: Independent Verification Location: PVNGS |
| I&C Reviewer: NA | Approver: Panos Paramithas — Digitally signed by: Paramithas, Panos (V72983) Date: 12/17/2002 16:18:19 Reason: I am approving this document Location: PVNGS |

*Cross-Discipline or Other, specify organization

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## Revision History

| Rev. | Responsible Engineer<br>Independent Verifier<br>Other Reviewers, Dept.<br>Approver | Approval Date | Reason for and Description of Change |
|---|---|---|---|
| 3 | Kent R. Bjornn<br>Roxton E. Baker<br>Pano Paramithas | | DMWO 223535 changes the CPC hardware. The uncertainty of the new hardware is determined in Addendum A of this revision.<br>There is an input buffer card before the A/D converter for QSPDS. For completeness the uncertainty of this card is included.<br>Some assumptions or references have slightly added information for improved clarity.<br>The values supporting the final uncertainty have changed, but the end result, the output of the Calculation has not, therefore there is no impact to other Calculations or documents. |
| 2 | Adrian Abbate<br>Kent Bjornn<br>Panos Paramithas | 16 Nov 00 | The ERFDADS discussion is expanded to discuss additional ERFDADS uncertainty experienced under certain conditions. |
| 1 | Kent R. Bjornn<br>Jim Sim - I&C Maint Engr<br>Stewart L. Hall<br>Panos Paramithas | 21 Apr 99 | Provided additional information about ERFDADS, CPC and QSPDS converters, updated references, provided slightly more conservative environment for PMS, CPC, and QSPDS converters, added digital-to-analog converter in QSPDS, reformatted for electronic control. Changes have been so extensive that no change bars are used. |
| 0 | Kent Bjornn<br>George Wilkenson<br>M. S. Burns | 04 Dec 92 | Initial Issue |

# 1 PURPOSE

This calculation determines an overall uncertainty for analog-to-digital converters used to provide input to ERFDADS [Ref. 6.5], PMS (which consists of two computers: plant computer and core monitoring computer, which runs COLSS) [Ref. 6.7], CPC [Ref. 6.9], and QSPDS [Ref. 6.18] for calculations prepared in accordance with the "Design Guide for Instrument Uncertainty and Setpoint Determination" [Ref. 6.1]. This is to be a single value which can be used for any of the A/D or D/A converters.

# 2 SUMMARY and CONCLUSIONS

The uncertainty of the analog-to-digital and digital-to-analog converters in ERFDADS, PMS, CPC, and QSPDS to be used for calculations prepared in accordance with Ref. 6.1 is 0.10% CS. This is inclusive of all effects which need to be considered for the control room and the upper and lower cable spreading room. For some of the A/D converters this is very conservative; however, the difference between the actual uncertainty and the single bounding value is very small compared to the other uncertainties of the loops in which these instruments are used.

Note: If the conditions described in section 4.2 exist, ERFDADS uncertainty may be increased to 0.30% CS.

# 3 CRITERIA and ASSUMPTIONS

3.1 **Design and Licensing Criteria**: This Calculation is an input to other Calculations and does not address any particular instrument channel; therefore, there are no specific criteria associated with this Calculation. Whatever design or licensing criteria that exist for a given channel would be applicable to the Calculations which use the results of this Calculation as one of the inputs.

3.2 The single largest uncertainty of each of the A/D converters will be used as representative of all of them.

3.3 All effects are treated as random. The information provided by the vendor is described as random in the design guide [Ref. 6.1]. This allows effects to be combined SRSS.

3.4 The temperature range for environmental conditions for all except ERFDADS will be 10°C even though the range provided in plant documents is 10°F (see Table 4-1). This will provide a measure of conservatism. The temperature variation within a cabinet is considered to be the same as the variation of the room in which it is located. This assumes that the temperature difference between the room and the cabinet is constant and that final calibrations are performed (or checked) with the equipment at the operating temperature of the cabinet. Using the 10°C range instead of the 10°F will compensate if the variation is wider.

3.5 The A/D converters are not exposed to the process. Therefore process pressure effects are not included.

3.6 Resolution (or sensitivity) for A/D converters is the quantizing error, and is related to the least-significant-bit (LSB). The significance of the LSB is determined using the relation $s = 1/(2^n - 1)$, where n is the number of bits of data. If the error is equal to the $\pm 1/2$ LSB and there are 12 bits, then R = 0.0122% CS. (See Ref. 6.4)

3.7 Seismic effects are not considered. The effect of shaking on the accuracy of an electronic instrument is assumed negligible. Similarly, post seismic effects are not considered.

3.8 Radiation is less than $10^4$ rads TID in the control building. Therefore, radiation effect is not applicable and vendor information is not needed for devices in the control building.

3.9 None of the vendors for the A/D converters provide a specification for humidity effect. The effect is considered negligible for electronic equipment in the control room environment. The operating range of humidity as stated by the vendors for the A/D converters is generally much wider than the expected actual humidity range.

3.10 The A/D converters are not affected by ambient pressure; therefore, barometric pressure effect is not applicable.

3.11 Generally the vendors do not specify drift. Unless provided by the vendor otherwise, this calculation will assume that drift is included in the accuracy.

## 4 INPUT DATA

Five different types of A/D converters are used to provide input to the computers. The ModComp converters are used in ERFDADS. The Analogic converters are used as inputs to the CPC [Ref. 6.10.1]. The Honeywell converters are used in the Plant Monitoring computer [Ref. 6.8.1]. The Data Translation and Datel converters are used in the QSPDS [Ref. 6.19.1 & Ref. 6.20.1].

### 4.1 Environmental Conditions

The A/D converters for PMS, CPC, and QSPDS are located in the control instrumentation room, which is part of the control room for environmental conditions. The A/D converters for ERFDADS are located in the cable spreading rooms (elevations 120' and 160'). Six operating conditions for uncertainties could exist for an instrument loop: accident, post-accident, seismic event, post-seismic, normal, and testing. However, because of the controlled environment for the control building, the temperature and pressure are the same for normal, accident, and post-accident [Ref. 6.3]. Seismic and post-seismic are not considered for A/D converters, since the shaking is assumed to have negligible effect on electronic instruments like these [Sect. 3.7]. Any testing of the instruments will occur during normal operations. Therefore, only one set of environmental parameters for a given type of A/D converter need be considered.

**Table 4-1. Environmental Conditions for Control Instrumentation Room**

| PMS (PC & CMC), CPC, and QSPDS | | | |
|---|---|---|---|
| | **Description** | **Data** | **Basis** |
| **Normal** | Temperature Range | 70-80°F | Ref. 6.2<br>Ref. 6.3 |
| | Pressure Range | Atm. | |
| | Humidity Range | 40 - 60% RH | |
| | Radiation | $< 10^3$ rad | |

**Table 4-2. Environmental Conditions for Cable Spreading Rooms**

| ERFDADS | | | |
|---|---|---|---|
| | **Description** | **Data** | **Basis** |
| **Normal** | Temperature Range | 40 - 120°F | Ref. 6.2<br>Ref. 6.3 |
| | Pressure Range | Atm. | |
| | Humidity Range | < 90% RH | |
| | Radiation | $< 10^3$ rad | |

## 4.2 ERFDADS (ModComp)

ERFDADS cards are autoranging. The autoranging allows for greater accuracy of small signals considering that 11 bits are used to describe the magnitude of the signal. Autoranging is explained in Ref. 6.6. The worst case condition occurs for a signal greater than approximately 50% span. In this case bits 1 - 11, as shown in Figure 12-3 of Ref. 6.6, are used to represent the signal. The least-significant-bit (LSB) is bit 11 which represents 5 mV. The quantizing error is given as $\pm^1/_2$ LSB. Therefore, the error is 2.5 mV and the nominal span is 10 Vdc. This is 0.025% CS, which is slightly larger than the 0.0244%CS expected from expression $1/(2^{11} - 1)$ (see Sect. 3.6), because the voltage range is slightly larger than 10 Vdc. Signals which are smaller than approximately 50% span use bits 2 - 12, 3 - 13, or 4 - 14, and have correspondingly smaller quantization error (error is still $\pm^1/_2$ LSB, but the LSB now represents a smaller voltage, and therefore, smaller error in %CS). The worst case error will be used.

**Table 4-3. ModComp 1860-X and 1861-X A/D Converter Vendor Data**

| Type | Description | Data | Basis |
|---|---|---|---|
| Random Effects | Accuracy (A) | 0.035% full scale | Ref. 6.6[a] |
| | Humidity Effect (HE) | NA | Sect. 3.9 |
| | Radiation Effect (RE) | NA | Sect. 3.8 |
| | Resolution (R) | 11 bits → 0.025%CS | Ref. 6.6[b] |
| | Drift (tD) | not available | —— |
| | Temperature Effect (TE) | —— | —— |
| | Voltage Stability Effect (VE) | not available | —— |

a. Accuracy above is the SRSS of offset setability (0.01%), gain accuracy setability (0.01%), linearity error (0.025%), and noise (0.02%).

b. The ModComp card has 12 bit resolution including the sign bit. Therefore, only 11 bits are available for describing the magnitude of the signal, and they are autoranged as described above.

Note that there is an additional error that may not be included in instrument loops utilizing ERFDADS outputs. ERFDADS testing (PM task# 286648) is performed with a signal injection to the ERFDADS backplane (essentially directly into the A/D converter). However, during the ERFDADS upgrade installation (DCPs 1,2,3,-PJ-038/37), functional end-to-end testing was performed with signal injections into the termination rails/cabinets upstream of the ERFDADS backplane. Where the typical measured accuracy of signals injected into the ERFDADS backplane is less than ±0.10% CS, some signals injected upstream at the termination cabinets experienced measured accuracies of up to ±0.30% CS. During this installation end-to-end testing, most of the measured accuracies were closer to ±0.10% CS with a smaller minority in the range of ±0.10% CS to ±0.30% CS. There are no additional components between these points; however, there is the normal wiring, terminal rail connectors, plugs, etc. Normally, any uncertainty due to these intermediate connections can be ignored as insignificant compared to the remaining loop uncertainty components. However, in the case where the remaining loop components add little or no instrument uncertianty, these intermediate connection uncertainties can take on more significance.

In the development of typical instrument loop uncertainties and as-found/as-left tolerances, use of the normal calculated uncertainty of ±0.10% CS for ERFDADS outputs will produce satisfactory results. This value will encompass the vast majority of actual ERFDADS signal paths. Years of established routine as-found/as-left testing shows that the existing ERFDADS "group" testing values are adequate when using an ERFDADS uncertainty value of ±0.10%CS (Note that most all ERFDADS points are calibrated as part of a "group" which typi-

cally includes at least an I/V converter and possiblty other components). For these "group" tests, the other components in the group are significantly larger than the ERFDADS uncertainties, thus even if the actual ERFDADS uncertainty were as large as ±0.30% CS, there would not be a significant increase in the calculated tolerances or loop uncertainties. However, in cases where are no additional "group" components or the additional "group" components are very accurate, additional uncertainty considerations may be needed.

To summarize, when standard additional "group" components are included in an instrument loop (such as an I/V converter) it is appropriate to consider the ERFDADS uncertainty as ±0.10% CS. When only an ERFDADS components exists as the "group" or the other "group" components are extremely accurate, it may be necessary to expand the ERFDADS tolerance to ±0.30% CS to account for potential errors present in the intermediate termination wiring. This increase in tolerance should be applied on a case by case basis based on current or past operating experience.

## 4.3 PMS (Honeywell)

There are two types of A/D converters used in the Honeywell system: Hi level and Lo level Process Interface Units [Ref. 6.8.1].

**Table 4-4. Honeywell High Level Process Interface Units A/D Converter Vendor Data**

| Type | Description | Data | Basis |
|---|---|---|---|
| Random Effects | Accuracy (A) | gain error: 0.05%FS<br>repeatability: 0.05%FS<br>total (SRSS): 0.071%FS | Ref. 6.8.3 |
| | Humidity Effect (HE) | NA | Sect. 3.9 |
| | Radiation Effect (RE) | NA | Sect. 3.8 |
| | Resolution (R) | 12 bits → 0.0122% of full scale | Ref. 6.8.3<br>Sect. 3.6 |
| | Drift (tD) | not available | —— |
| | Temperature Effect (TE) | Gain: 50 ppm/°C → 0.0050%CS/°C<br>Offest: 50 ppm/°C → 0.0050%CS/°C<br>Total (SRSS): 0.0071%CS/°C | Ref. 6.8.3 |
| | Voltage Stability Effect (VE) | not available | —— |

**Table 4-5. Honeywell Low Level Process Interface Units A/D Converter Vendor Data**

| Type | Description | Data | Basis |
|---|---|---|---|
| Random Effects | Accuracy (A) | gain error: 0.025%FS<br>repeatability: 0.025%FS<br>total (SRSS): 0.035%FS | Ref. 6.8.2 |
| | Humidity Effect (HE) | NA | Sect. 3.9 |
| | Radiation Effect (RE) | NA | Sect. 3.8 |
| | Resolution (R) | 12 bits → 0.0122% of full scale | Ref. 6.8.2<br>Sect. 3.6 |
| | Drift (tD) | not available | —— |
| | Temperature Effect (TE) | Gain: 40 ppm/°C → 0.0040%CS/°C | Ref. 6.8.2 |
| | Voltage Stability Effect (VE) | not available | —— |

## 4.4 CPC (Analogic)

There are four aspects to be considered: the uncertainty of each of the three cards (multiplexer, signal processor, and A/D converter) and the reference voltage error.

**Table 4-6. Analogic AC4730 High Level Filter Multiplexer Card Vendor Data**

| Description | Data | Basis |
|---|---|---|
| Transfer Accuracy (A) | 0.01% @ DC | Ref. 6.10.3 |
| Humidity Effect (HE) | NA | Sect. 3.9 |
| Radiation Effect (RE) | NA | Sect. 3.8 |
| Resolution (R) | Not provided | Ref. 6.10.3 |
| Drift (tD) | | |
| Temperature Effect (TE) | | |
| Voltage Stability Effect (VE) | | |

**Table 4-7. Analogic AC262/AC265 Signal Processor Card Vendor Data**

| Description | | Data | Basis |
|---|---|---|---|
| Gain Accuracy (A) | | 0.01% FSR | Ref. 6.10.4 |
| Humidity Effect (HE) | | NA | Sect. 3.9 |
| Radiation Effect (RE) | | NA | Sect. 3.8 |
| Linearity (L) | | ±0.003% FSR | Ref. 6.10.4[a] |
| Noise (N) | | <0.5mV p-p = 0.0025% CS[b] | |
| Drift (tD) | | not available | |
| Temperature Effect (TE) | gain | <20 ppm/°C → 0.0020%CS/°C | |
| | offset | <50 µV/°C → 0.0005%CS/°C | |
| Voltage Stability Effect (VE) | | not available | —— |

a. Uncertainties in absolute volts are converted to %CS using a full scale input voltage of 10 Vdc.
b. Half of the peak-to-peak noise is used.

**Table 4-8. Analogic MP2712C A/D Converter Vendor Data**

| Description | | Data | Basis |
|---|---|---|---|
| Accuracy (A) | | 0.015% full scale (absolute) | Ref. 6.10.2 |
| Humidity Effect (HE) | | NA | Sect. 3.9 |
| Radiation Effect (RE) | | NA | Sect. 3.8 |
| Resolution (R) | | 12 bits → 0.0122%CS | Ref. 6.10.2, Sect. 3.6 |
| Drift (tD) | | not available | —— |
| Temperature Effect (TE) | linearity | ±3 ppm/°C → 0.0003%CS/°C | Ref. 6.10.2 |
| | gain | ±12 ppm/°C → 0.0012%CS/°C | |
| | offset | ±12 ppm/°C → 0.0012%CS/°C | |
| Voltage Stability Effect (VE) | | ±0.0012%/%change in supply → ±0.0036%CS | Ref. 6.10.2[a] |
| Voltage Stability | | ±3% | |

a. The power supply requirements for 15 V supplies allow a 3% variation. This calculation will assume that the full allowed variation does occur.

The uncertainty of the reference voltage and its interaction with the CPC software is discussed in Ref. 6.11 and Ref. 6.12. There was a hardware and an intended software change which would improve the accuracy of the reference voltage. The expected improvement in accuracy is given in Ref. 6.13. However, there was a question whether the software change actually occurred and if it made the intended improvements. This was discussed in CRDR 9-4-0464 [Ref. 6.14]. The conclusion from CE is provided in Ref. 6.15. The results of PVNGS testing and review of the CE evaluation is given in Ref. 6.16. A chronology of major events in this process is provided in Ref. 6.17. The end result seems to be that hardware and software changes that have been made to date (March 1999) are at least as accurate as the original proposal, the accuracy of which was given in Ref. 6.13. Therefore, the accuracy of **0.033%CS** given in Ref. 6.13 will be used.

## 4.5 QSPDS

### 4.5.1 Input Buffer Card

The non-thermocouple inputs to QSPDS also have a buffer or filter board before the A/D converter [Ref. 6.22]. This board isolates the input from the A/D card. The component which does the buffering is a National Semiconductor model LM308A operational amplifier [Ref. 6.23].

**Table 4-9. National Semiconductor LM308A Op Amp/Buffer Vendor Data [a]**

| Description | Data | Basis |
|---|---|---|
| Input Offset Voltage | 0.73 mV | Ref. 6.21 |
| Temperature Coefficient of Input Offset Voltage | 5.0 µV/°C | |
| Temperature Coefficient of Input Offset Current | 10 pA/°C | |
| Input Bias Current | 10 nA | |
| Resistance in the input path | 124 kΩ | Ref. 6.23[b] |

a. The maximum values are used, and where there are model variations, the larger values are used.
b. This is the sum of 62kΩ and 62kΩ for resistors labeled as "R1-R32" and "R35-R64" in the figure in the reference.

### 4.5.2 Data Translation DT 1748 A/D Converter

This converter is used for thermocouple inputs to QSPDS [Ref. 6.20.2 & Ref. 6.20.3].

**Table 4-10. Data Translation A/D Converter Vendor Data**

| Description | Data | Basis |
|---|---|---|
| Accuracy (A) | 0.03% CS[a] | Ref. 6.19.2 |
| Humidity Effect (HE) | NA | Sect. 3.9 |
| Radiation Effect (RE) | NA | Sect. 3.8 |
| Resolution (R) | 12 bits → 0.0122%CS | Ref. 6.19.2<br>Sect. 3.6 |
| Drift (tD) | not available | —— |
| Temperature Effect (TE) | For Amplifier<br>offset: ±3µV/°C = 0.00003% CS<br>gain: ±10ppm/°C = 0.0010%CS/°C<br>For A/D converter<br>zero: ±20µV/°C = 0.0002% CS<br>full span ±30ppm/°C = 0.0030%CS/°C | Ref. 6.19.2[b] |
| Voltage Stability Effect (VE) | not available | —— |

a. The system accuracy is given as 0.03% FSR. Linearity of $\pm^1/_2$ LSB and quantization error of $\pm^1/_2$ LSB are also provided. Linearity will be considered as already included in system accuracy, but quantization error will be treated separaetely under resolution.
b. Uncertainties in absolute volts are converted to %CS using a full scale input voltage of 10 Vdc.

### 4.5.3 Datel ST-732 A/D and D/A Converter

The A/D function of this card is used for all analog inputs to QSPDS except the thermocouples. The D/A function is used for output from QSPDS to analog recorders used to track subcooled margin [Ref. 6.20.1].

**Table 4-11. Datel ST-732 A/D Converter Vendor Data**

| Description | Data | Basis |
|---|---|---|
| Accuracy (A) | ±0.07% FSR ±1/2 LSB[a] | Ref. 6.19.3 |
| Humidity Effect (HE) | NA | Sect. 3.9 |
| Radiation Effect (RE) | NA | Sect. 3.8 |
| Resolution (R) | 12 bits → 0.0122%CS - included in accuracy | Ref. 6.19.3<br>Sect. 3.6 |
| Drift (tD) | not available | —— |
| Temperature Effect (TE) | zero: ±20μV/°C = 0.0002% CS/°C[b]<br>full span ±30ppm of FSR /°C = 0.0030%CS/°C | Ref. 6.19.3 |
| Voltage Stability Effect (VE) | not available | —— |

a. The input voltage is 10 Vdc therefore the gain is "X1"; however, for conservatism the accuracy for higher gains will be used.
b. For a full scale input voltage of 10 Vdc an error of 20 μV is 0.0002% CS

**Table 4-12. Datel ST-732 D/A Converter Vendor Data**

| Description | Data | Basis |
|---|---|---|
| Accuracy (A) | 0.05% FSR | Ref. 6.19.4 |
| Humidity Effect (HE) | NA | Sect. 3.9 |
| Radiation Effect (RE) | NA | Sect. 3.8 |
| Resolution (R) | 12 bits → ±0.0122%CS | Ref. 6.19.3<br>Sect. 3.6 |
| Drift (tD) | not available | —— |
| Temperature Effect (TE) | ±50 ppm of FSR/°C = 0.0050% CS/°C | Ref. 6.19.3 |
| Voltage Stability Effect (VE) | not available | —— |

# 5 CALCULATION and RESULTS

## 5.1 ERFDADS (ModComp)

Ussing SRSS of accuracy and resolution results in an overall uncertainty of 0.0430%CS.

$$U_{ERF,1860} = \sqrt{A^2 + R^2}$$

$$U_{ERF,1860} = \sqrt{0.035^2 + 0.025^2} = 0.0430\%CS$$

Note: This is the accuracy of the A/D converter. See section 4.2 for other ERFDADS channel error consider

## 5.2 PMS (Honeywell)

The Honeywell has both high and low level process interface units. The terms are combined using SRSS and using a temperature variation of 10°C (Sect. 3.4) for temperature effect.

$$U_{PMS} = \sqrt{A^2 + R^2 + TE^2}$$

For the high level PIU this results in an overall uncertainty of 0.1011% CS.

$$U_{PMS,hi} = \sqrt{0.071^2 + 0.0122^2 + (0.0071(10))^2} = 0.1011\%CS$$

For the low level PIU the overall uncertainty is 0.0545% CS.

$$U_{PMS,lo} = \sqrt{0.035^2 + 0.0122^2 + (0.0040(10))^2} = 0.0545\%CS$$

## 5.3 CPC (Analogic)

The uncertainty for the CPC overall analog-to-digital conversion process is determined below. Uncertainty values for the CPC input cards have been previously calculated by CE [Ref. 6.12]. The methods below are similar to the CE results except for use of SRSS to combine individual effects and a different temperature range (38°C for CE and 10°C for this calculation).

- **Multiplexer Card**

Only transfer accuracy need be considered.

$$U_m = A = 0.01\%CS$$

- **Signal Processor Card**

The terms to be combined are shown in the equation below. A temperature variation of 10°C (Sect. 3.4) is used for temperature effects.

$$U_{sp} = \sqrt{EA^2 + L^2 + N^2 + TE_{gain}^2 + TE_{off}^2}$$

$$U_{sp} = \sqrt{0.01^2 + 0.003^2 + 0.0025^2 + (0.0020(10))^2 + (0.0005(10))^2}$$

$$U_{sp} = 0.0232\%CS$$

- **Analog-to-Digital Converter Card**

The terms to be combined are shown in the equation below. A temperature variation of 10°C (Sect. 3.4) is used for temperature effects.

$$U_{ad} = \sqrt{A^2 + R^2 + TE_{lin}^2 + TE_{gain}^2 + TE_{off}^2 + VE^2}$$

$$U_{ad} = \sqrt{0.015^2 + 0.0122^2 + (0.0003(10))^2 + (0.0012(10))^2 + (0.0012(10))^2 + 0.0036^2}$$

$$U_{ad} = 0.0261\%CS$$

- **Reference Voltage Error**

$$U_{rv} = 0.033\%CS$$

- **Total**

The uncertainty of the overall analog-to-digital conversion process for CPCs is the SRSS of the four uncertainties above and results in an uncertainty of 0.0491% CS.

$$U_{CPC} = \sqrt{0.01^2 + 0.0232^2 + 0.0261^2 + 0.033^2} = 0.0491\%CS$$

## 5.4 QSPDS

### 5.4.1 Input Buffer Card

There are four terms to be considered: the input offset voltage, the temperature effect on the input offset voltage, the input bias current, and the temperature effect on the input bias current (the last two are multiplied by the resistance on the input path to obtain a voltage error)[1]. These are all combined SRSS.

$$U_B = \sqrt{V_{offset}^2 + TE_{volt\text{-}offset}^2 + R^2(I_{bias}^2 + TE_{current\text{-}bias}^2)}$$

For additional conservatism a temperature variation of 15°C is used instead of the 10°C (Sect. 3.4) used for other devices.

$$U_B = \sqrt{(0.73mV)^2 + \left(\frac{5\mu V}{°C}15°C\right)^2 + (124k\Omega)^2\left((10nA)^2 + \left(\frac{10pA}{°C}15°C\right)^2\right)}$$

$$U_B = \sqrt{(0.73mV)^2 + (0.075mV)^2 + (124k\Omega)^2((10nA)^2 + (0.150nA)^2)}$$

$$U_B = \sqrt{(0.73mV)^2 + (0.075mV)^2 + 124^2(10^2 + 0.150^2)(\mu V)^2}$$

$$U_B = \sqrt{(0.73mV)^2 + (0.075mV)^2 + 1.53795(mV)^2}$$

$$U_B = \sqrt{0.5329 + 0.005625 + 1.53795}(mV) = 1.441mV$$

1. The input bias current is not compensated so using the input offset is not needed. The input offset is in effect the difference in the bias current, but since the entire bias is used, an offset is not needed. The leakage currents through the two diodes on the input are assumed to be equal, and therfore cancel.

Converting this uncertainty from mV to %CS for a 10V input span results in an uncertainty of 0.01441% CS.

### 5.4.2 Data Translation DT 1748 A/D Converter

Combining the terms using SRSS and using a temperature variation of 10°C (Sect. 3.4) for temperature effect results in an overall uncertainty of 0.0453% CS.

$$U = \sqrt{A^2 + R^2 + TE_{AD}^2 + TE_A^2}$$

$$U = \sqrt{0.03^2 + 0.0122^2 + [(0.0002(10))^2 + (0.003(10))^2] + [(0.00003(10))^2 + (0.001(10))^2]} = 0.0453\%CS$$

### 5.4.3 Datel ST-732 A/D Convter

Combining the terms using SRSS and using a temperature variation of 10°C (Sect. 3.4) for temperature effect results in an uncertainty of 0.0772% CS for the A/D converter.

$$U = \sqrt{A^2 + R^2 + TE^2_{AD}}$$

$$U = \sqrt{0.07^2 + 0.0122^2 + [(0.0002(10))^2 + (0.0030(10))^2]} = 0.0772\%CS$$

Combining this with the uncertainty of the input buffer results in the uncertaint of the conversion process. this is combined using SRSS.

$$U = \sqrt{0.0772^2 + 0.01441^2} = 0.0785\%CS$$

### 5.4.4 Datel ST-732 Converter - D/A Function

Combining the terms using SRSS and using a temperature variation of 10°C (Sect. 3.4) for accuracy (expressed as a temperature effect by vendor) results in an overall uncertainty of 0.0718% CS.

$$U = \sqrt{A^2 + R^2 + TE_{DA}^2}$$

$$U = \sqrt{0.05^2 + 0.0122^2 + (0.005(10))^2} = 0.0718\%CS$$

## 5.5 Overall Uncertainty

The least accurate A/D converter appears to be the Honeywell high level PIU, the overall uncertainty being 0.1011% CS. All other A/D and D/A converters have a much lower uncertainty. A value of 0.10% CS will be used as the overall accuracy of all of the A/D and D/A converters, which includes all effects.

Note: This is the overall uncertainty to be used for most all cases. However, see section 4.2 for some exceptions to ERFDADS.

# 6 REFERENCES

## • General References

6.1 "Design Guide for Instrument Uncertainty and Setpoint Determination", Palo Verde Nuclear Generating Station, Nuclear I&C Department, DSG IC-0205, Rev. 8.

6.2 "HVAC Environmental Design Parameters", PVNGS Study 13-MS-A82. Rev. 0.

6.3 PVNGS Environmental Qualification Program Manual (EQDF EQ-PM), Rev. 9, Sections 2.3.4.5, 2.3.2.1.

6.4 "Terms, Definitions, and Letter Symbols for Analog-to-Digital and Digital-to-Analog Converters", Electronic Industries Association, JEDEC Standard Number 99, Addendum 1, July 1989, e.g. pages 11,15. (available from Information Handling Service (http://www.ihserc.com) with subscription. Search for document number "EIA JESD99-1", leave other fields blank or default)

## • Emergency ResponseFacilities Data Acquisition and Display System

6.5 ERFDADs Information Manuals

6.5.1 "PVNGS System Training Manual: Emergency Response Facilities Data Acquisition and Display System (SD)", PVNGS, Rev. 1.

6.5.2 Design Basis Manual - Emergency ResponseFacilities Data Acquisition and Display System (ERFDADS (SD)), Rev. 3.

6.6 Technical Manual MODACS III Part 1 of 2, MODCOMP Inc., J106-00051-6, pages 1-2, high level cards: 12-1, 12-2, (figure 12-3); low level cards: 13-1 & 13-2.

## • Plant Monitoring System and Core Monitoring Computer

6.7 "PVNGS System Training Manual: Plant Monitoring System (RJ)", PVNGS, Rev. 1

6.8 Honeywell Plant Monitoring System, Vendor Technical Manual, VTM-H260-0003.

6.8.1 "TDC-2000 Process Interface Unit Site Planning/Installation Manual", Honeywell, VTD-H260-0098-1 (Honeywell publication PTH-022 (R320), 12/81 and AR1 dated 29 Aug 86, VTM-H260-0003 tab 2), page 6 (provides information about which PIU are applicable to PVNGS, Note that Honeywell publication PCRH-S "HL PIU Specifications and Technical Data" should be VTD-H260-0175 rather than 0094 as shown).

6.8.2 "Honeywell Specification and Technical Data for Low Level Process Interface Unit", VTD-H260-0235-1 (Honeywell publication PCRL-S (Rel. 320), VTM-H260-0003 tab 14), pages 7 & 9.

6.8.3 "Honeywell Specification and Technical Data for High Level Process Interface Unit", VTD-H260-0175-1 (Honeywell publication PCRH-S(B) 7/89 and AR1 dated 29 Aug 86, VTM-H260-0003 tab 7), pages 8 & 9.

## • Core Protection Calculator

6.9 CPC Information Manuals

6.9.1 "PVNGS System Training Manual: Core Protection Calculator (CPC)", PVNGS, Rev. 2.

6.9.2 Design Basis Manual - Core Protection Calculator System / Core Operating Limit Supervisory System (CPCS/COLSS (CA)), Rev. 2

6.10 Simmonds Precision Products Inc. VTM-S204-0001

6.10.1 "System Operation and Maintenance Instructions for Departure from Nucleate Boiling Ratio/Local Power Density (DNBR/LPD) Calculator System", Simmonds Precision Products Inc., VTD-S204-

0001-4, (VTM-S204-0001 tab 1), section 2.5 and Table 2-5, Table 2-5 (shows Analogic part numbers which are used in this calculation, A/D converter (AC2712-1A), signal processor (AC262), multiplexer (AC4730)).

6.10.2 "Analogic Corporation Specifications for Series 2700 A/D Converters", VTD-A389-0003-1 (VTM-S204-0001 tab 4) pages 2 & 3.

6.10.3 "Analogic Corporation Specifications for AC4730 Series High Level Filter Multiplexer for AN5400", VTD-A389-0004-2 (VTM-S204-0001 tab 5) page 1.

6.10.4 "Analogic Corporation Data Sheet for Analog Signal Processor AC262/AC265 for AN5400", VTD-A389-0005-1 (VTM-S204-0001 tab 6) page 1.

6.11 "SYS80 Core Protection Calculator (CPC) Input Hardware Error Analysis", CE, CE Analysis SYS80-ICE-3626 Rev. 02, PVNGS nmbr N001-1304-238-2.

6.12 "PVNGS Core Protection Calculator (CPC) System Input Software Error Analysis", CE, CE Analysis 14273-ICE-3629 Rev. 02, PVNGS nmbr N001-1304-239-2, section 2.3.

6.13 "PVNGS CPC/CEAC DAS Reference Voltage Uncertainty (725721)", CE memorandum from W.B. Parsons and J.E. Burns to P.L. Hung, 25 February 1987, CE letter number TIC-87-147 and V-IC-665. (CDCC number 61369)

6.14 CRDR 9-4-0464, 30 June 1994.

6.15 "APS CPC Analog to Digital Measurement Channel Uncertainties", CE memorandum from Jeffrey Arpin to Paul F. Crawley (APS), 18 May 1995, CE letter number TIC-95-537. This is part of the closure of CRDR 9-4-0464.

6.16 "Summary of CPC Reference Voltage Evaluation", PVNGS memorandum from J.J. Valerio to R.J. Logue, 24 Oct 1995, PVNGS letter number 104-00247-RJL/JJV, Conclusion 1.

6.17 "Proposed CPCS Software Revision - Final Recommendation", PVNGS memorandum from P.M. Clifford, M.J. Chernick, and J.J. Valerio to File, 22 Sep 1995, PVNGS letter number 162-06964-PMC, pages A2-A3.

- **Qualified Safety Parameters Display System**

6.18 QSPDS Information Manuals

6.18.1 "PVNGS System Training Manual: Qualified Safety Parameter Display System (SH)", PVNGS, Rev. 1.

6.18.2 Design Basis Manual - Qualified Safety Parameter Display System (SH), Rev. 3.

6.19 Qualified Safety Parameter Display System, Vendor Technical Manual, VTM-C490-0010

6.19.1 "Combustion Engineering Qualified Safety Parameter Display System Instruction Manual", CE, VTD-C490-0074-2 (CE document 14273-ICE-0505, Rev 00, VTM-C490-0010 tab 1) figures 6.2 and 6.3 (pages 86-87) show the I/O boards as ST-732 and DT1748), section 6.3 (provides information about calibration of the I/O cards), page 5 (or ii) indicates user manual for ST-732 and DT1748 applicable to this system.

6.19.2 "User Manual for DT1748, DT1759 Isolated Input Data Acquisition and Control System", Data Translation Inc., VTD-D960-0003-1, page 14 (Data Translation number: UM-00050-0, page 2-2; VTM-C490-0010 tab 13).

6.19.3 "Datel ST-711/732 Product Data Sheet", Datel, VTD-D033-0009-2 (VTM-C490-0010 tab 14)

6.19.4 "Datel User Manual for ST-711/732 Multibus A/D Microcomputer Board", Datel, VTD-D033-0012-1, page 26 (1-8) (VTM-C490-0010 tab 31).

6.20 QSPDS Drawer #x Schematics

6.20.1 "QSPDS Drawer #1 Schematic", CE, N001-13.10-54-2.

6.20.2 "QSPDS Drawer #2 Schematic", CE, N001-13.10-82-2.

6.20.3 "QSPDS Drawer #3 Schematic", CE, N001-13.10-61-3.

6.21 "Linear Databook", National Semicondutor Corp., 1982 edition, pages 3-149 and 3-151, section for LM108A/LM208A/LM308A/LM308A-1/LM308A-2 Operational Amplifiers/Buffers. Attached. Note that the uncertainty information is the same as for the May 19898 edition of the datasheet for LM108A/LM208A/LM308A Operational Amplifiers available from www.national.com, which is also included in the attachment.

6.22 "QSPDS Schematics Drawer #1", N001-1310-00054-4.

6.23 "Electro-Mechanics QSPDS Analog Input Filter Board Schematics and Parts List", VTD-C490-00083-1, pages 2 and 3. Note that resistors R65-96 are optional and may not be present.

## Addendum A - CPC Replacement

Contingencies
None

### A-1 Purpose

See calculation section 1.

### A-2 Summary and Conclusions

See calculation section 2. Note that the conclusion and output of the Calculation is unchanged.

### A-3 Criteria and Assumptions

See calculation section 3.

### A-4 Input Data

Five different types of A/D converters are used to provide input to the computers. The ModComp converters are used in ERFDADS [Ref. 6.6]. The ABB/Westinghouse converters are used as inputs to the CPC [Ref. A-6.1]. The Honeywell converters are used in the Plant Monitoring computer [Ref. 6.8.1]. The Data Translation and Datel converters are used in the QSPDS [Ref. 6.19.1 & Ref. 6.20.1].

See calculation section 4 for all subsections except section 4.4 (CPC); for that see section A-4.1 below.

#### A-4.1 CPC (Westinghouse & ABB Advent)

The AI 685 analog input card receives a voltage signal directly; there are no other devices associated with preparing the signal for input to the AI685 (i.e. no multiplexer or signal processor) [Ref. A-6.2]. Any devices in the signal path before the AI685 (e.g. I/V converter) are considered in the individual channel calculation.

**Table A4-1. Westinghouse AI685 Analog Input Card (A/D converter) Vendor Data**

| Description | Data | Basis |
|---|---|---|
| Accuracy (A) | 0.05% of range | Ref. A-6.2[a] |
| Humidity Effect (HE) | NA | Sect. 3.9 |
| Radiation Effect (RE) | NA | Sect. 3.8 |
| Resolution (R) | 16 bits → 0.00076%CS | Ref. A-6.2, Sect. 3.6 |
| Drift (tD) | 0.01% FS/year | Ref. A-6.2 |
| Temperature Effect (TE) | 0.006%FS/°C → 0.0003%CS/°C | Ref. A-6.2 |
| Voltage Stability Effect (VE) | negligible | Ref. A-6.2[b] |

a. Includes combined effects of linearity, repeatability, and hysteresis.

b. Ref. A-6.2 provides an example overall accuracy determination (using a different calibration tolerance and temperature range), but does not include a power supply effect, indicating that the power supply effect is negligible.

## A-5 Calculation and Results

See calculation section 5 for all except section 5.3 (CPC); for that see section A-5.1 below. Note that the overall uncertainty (section 5.5) is the same for the body of the Calculation and for this addendum.

### A-5.1 CPC (Westinghouse & ABB Advent)

The uncertainty for the CPC overall analog-to-digital conversion process is determined below. Uncertainty values for the CPC input cards have been previously calculated by Westinghouse [Ref. A-6.3]. The methods below are similar to the Westinghouse results except for inclusion of resolution, R, (a negligble term) and a different temperature range: (Westinghouse used ~32°C for what they considered to be an accident condition; this calculation uses 10°C since accident and normal are the same (see section 3.4 and section 4.1)).

The terms to be combined are shown in the equation below. The effective accuracy, EA, is the vendor stated accuracy. A calibration interval of 18 months, plus 25% or 22.5 months is used.

$$U_{CPC} = \sqrt{EA^2 + R^2 + TE^2 + tD^2}$$

$$U_{CPC} = \sqrt{0.05^2 + 0.00076^2 + (0.006(10))^2 + \left(0.01\left(\frac{22.5}{12}\right)\right)^2}$$

$$U_{CPC} = 0.0803\%CS$$

## A-6 References

Except as noted below, the references remain unchanged.

- **Core Protection Calculator**

Add the following references

A-6.1 "Hardware Design Description for the Common Q Core Protection Calculator", PVNGS number JN1000-A00028-0 (Westinghouse number 0000-ICE-30164 Rev 1), Figures 2.1-1 and 2.1-2x.

A-6.2 "S600 I/O Hardware Advent Controller 160 Reference Manual" PVNGS number JN1000-A00082-0, (ABB Advent document number 3BDS 005 558R301). Section 3.1 AI685; Section 3.1.8 Technical Data; Section 3.1.11 Process Connections

A-6.3 "PVNGS Core Protection Calculator (CPC) System Input Processing Uncertainty Calculation" PVNGS number JN1000-A00029-0, (Westinghouse number 14273-ICE-36363 Rev 0).

Delete the following references: Ref. 6.10 through Ref. 6.17 (all except the general CPC references).

National Semiconductor

Operational Amplifiers/Buffers

# LM108A/LM208A/LM308A, LM308A-1, LM308A-2 Operational Amplifiers

## General Description

The LM108/LM108A series are precision operational amplifiers having specifications about a factor of ten better than FET amplifiers over their operating temperature range. In addition to low input currents, these devices have extremely low offset voltage, making it possible to eliminate offset adjustments, in most cases, and obtain performance approaching chopper stabilized amplifiers.

The devices operate with supply voltages from ±2V to ±18V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary. Outstanding characteristics include:

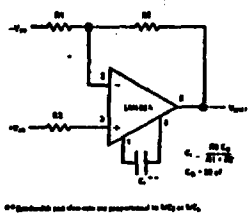
- Offset voltage guaranteed less than 0.5 mV
- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed 5 μV/°C drift.
- Guaranteed 1 μV/°C for LM308A-1

The low current error of the LM108A series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

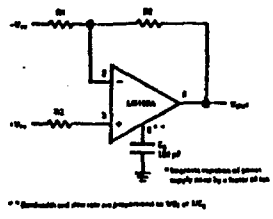
The LM208A is identical to the LM108A, except that the LM208A has its performance guaranteed over a −25°C to 85°C temperature range, instead of −55°C to 125°C. The LM308A devices have slightly-relaxed specifications and performance guaranteed over a 0°C to 70°C temperature range.

## Compensation Circuits

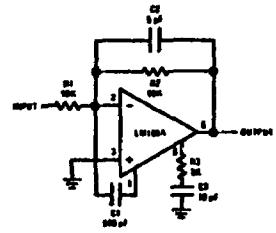
Standard Compensation Circuit



Alternate* Frequency Compensation

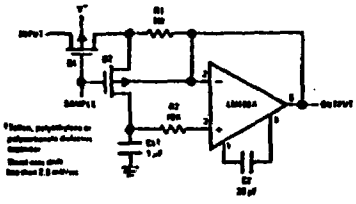


Feedforward Compensation

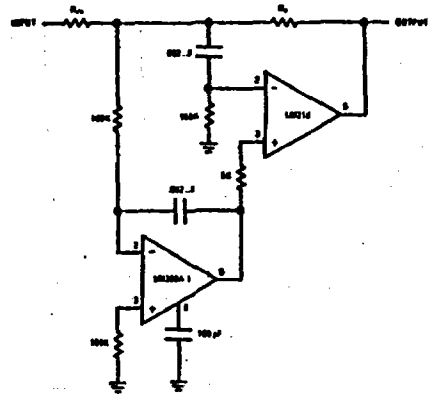


## Typical Applications

Sample and Hold



High Speed Amplifier with Low Drift and Low Input Current



## LM308A, LM308A-1, LM308A-2

### Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Current (Note 2) | ±10 mA |
| Input Voltage (Note 3) | ±15V |
| Output Short-Circuit Duration | Indefinite |
| Operating Temperature Range | 0°C to 70°C |
| Storage Temperature Range | −65°C to 150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

### Electrical Characteristics (Note 4)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Offset Voltage | $T_A = 25°C$ | | 0.3 | 0.5 | mV |
| Input Offset Current | $T_A = 25°C$ | | 0.2 | 1 | nA |
| Input Bias Current | $T_A = 25°C$ | | 1.5 | 7 | nA |
| Input Resistance | $T_A = 25°C$ | 10 | 40 | | MΩ |
| Supply Current | $T_A = 25°C$, $V_S = ±15V$ | | 0.3 | 0.8 | mA |
| Large Signal Voltage Gain | $T_A = 25°C$, $V_S = ±15V$, $V_{OUT} = ±10V$, $R_L \geq 10\ k\Omega$ | 80 | 300 | | V/mV |
| Input Offset Voltage | $V_S = ±15V$, $R_S = 100\Omega$ | | | | |
| LM308A | | | | 0.73 | mV |
| LM308A-1 | | | | 0.54 | mV |
| LM308A-2 | | | | 0.59 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $V_S = ±15V$, $R_S = 100\Omega$ | | | | |
| LM308A | | | 2.0 | 5.0 | μV/°C |
| LM308A-1 | | | 0.6 | 1.0 | μV/°C |
| LM308A-2 | | | 1.3 | 2.0 | μV/°C |
| Input Offset Current | | | | 1.5 | nA |
| Average Temperature Coefficient of Input Offset Current | | | 2.0 | 10 | pA/°C |
| Input Bias Current | | | | 10 | nA |
| Large Signal Voltage Gain | $V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 10\ k\Omega$ | 60 | | | V/mV |
| Output Voltage Swing | $V_S = ±15V$, $R_L = 10\ k\Omega$ | ±13 | ±14 | | V |
| Input Voltage Range | $V_S = ±15V$ | ±14 | | | V |
| Common-Mode Rejection Ratio | | 96 | 110 | | dB |
| Supply Voltage Rejection Ratio | | 96 | 110 | | dB |

Note 1: The maximum junction temperature of the LM308A, LM308-1 and LM308-2 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $±5V \leq V_S \leq ±15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified.

National Semiconductor

May 1989

# LM108A/LM208A/LM308A Operational Amplifiers

## General Description

The LM108/LM108A series are precision operational amplifiers having specifications about a factor of ten better than FET amplifiers over their operating temperature range. In addition to low input currents, these devices have extremely low offset voltage, making it possible to eliminate offset adjustments, in most cases, and obtain performance approaching chopper stabilized amplifiers.

The devices operate with supply voltages from ±2V to ±18V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108A series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

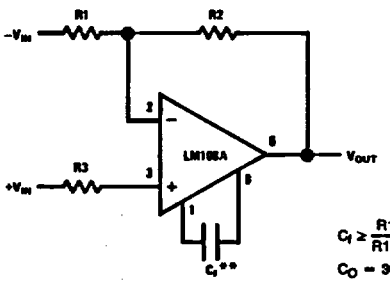
The LM208A is identical to the LM108A, except that the LM208A has its performance guaranteed over a −25°C to +85°C temperature range, instead of −55°C to +125°C. The LM308A devices have slightly-relaxed specifications and performances over a 0°C to +70°C temperature range.

## Features

- Offset voltage guaranteed less than 0.5 mV
- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed 5 μV/°C drift

## Compensation Circuits

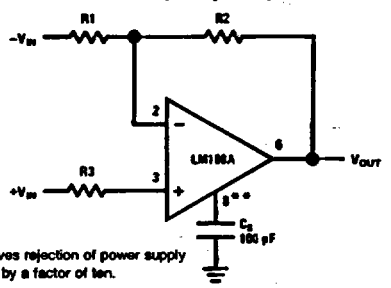
**Standard Compensation Circuit**




TL/H/7759–1

**Bandwidth and slew rate are proportional to $1/C_f$.

**Alternate* Frequency Compensation**

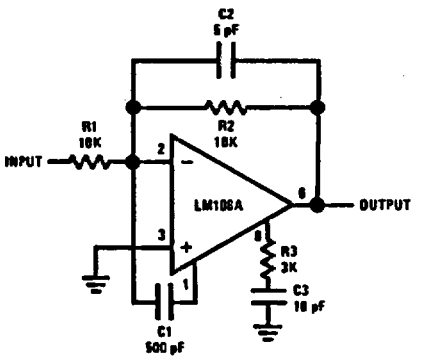



*Improves rejection of power supply noise by a factor of ten.

TL/H/7759–2

**Bandwidth and slew rate are proportional to $1/C_s$.

**Feedforward Compensation**




TL/H/7759–3

RRD-B30M115/Printed in U. S. A.

## LM108A/LM208A Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)**

| | |
|---|---|
| Supply Voltage | ±20V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Current (Note 2) | ±10 mA |
| Input Voltage (Note 3) | ±15V |
| Output Short-Circuit Duration | Continuous |
| Operating Free Air Temperature Range | |
| LM108A | −55°C to +125°C |
| LM208A | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) (DIP) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See An-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

| | |
|---|---|
| ESD Tolerance (Note 6) | 2000V |

## Electrical Characteristics (Note 4)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage | $T_A$ = 25°C | | 0.3 | 0.5 | mV |
| Input Offset Current | $T_A$ = 25°C | | 0.05 | 0.2 | nA |
| Input Bias Current | $T_A$ = 25°C | | 0.8 | 2.0 | nA |
| Input Resistance | $T_A$ = 25°C | 30 | 70 | | MΩ |
| Supply Current | $T_A$ = 25°C | | 0.3 | 0.6 | mA |
| Large Signal Voltage Gain | $T_A$ = 25°C, $V_S$ = ±15V, $V_{OUT}$ = ±10V, $R_L \geq 10\ k\Omega$ | 80 | 300 | | V/mV |
| Input Offset Voltage | | | | 1.0 | mV |
| Average Temperature Coefficient of Input Offset Voltage | | | 1.0 | 5.0 | μV/°C |
| Input Offset Current | | | | 0.4 | nA |
| Average Temperature Coefficient of Input Offset Current | | | 0.5 | 2.5 | pA/°C |
| Input Bias Current | | | | 3.0 | nA |
| Supply Current | $T_A$ = 125°C | | 0.15 | 0.4 | mA |
| Large Signal Voltage Gain | $V_S$ = ±15V, $V_{OUT}$ = ±10V, $R_L \geq 10\ k\Omega$ | 40 | | | V/mV |
| Output Voltage Swing | $V_S$ = ±15V, $R_L$ = 10 kΩ | ±13 | ±14 | | V |
| Input Voltage Range | $V_S$ = ±15V | ±13.5 | | | V |
| Common Mode Rejection Ratio | | 96 | 110 | | dB |
| Supply Voltage Rejection Ratio | | 96 | 110 | | dB |

**Note 1:** The maximum junction temperature of the LM108A is 150°C, while that of the LM208A is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

**Note 2:** The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 4:** These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM208A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$.

**Note 5:** Refer to RETS108AX for LM108AH and LM108AJ-8 military specifications.

**Note 6:** Human body model, 1.5 kΩ in series with 100 pF.

## LM308A Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | ±18V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Current (Note 2) | ±10 mA |
| Input Voltage (Note 3) | ±15V |
| Output Short-Circuit Duration | Continuous |
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| H-Package Lead Temperature (Soldering, 10 sec.) | 300°C |
| Lead Temperature (Soldering, 10 sec.) (DIP) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See An-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

## Electrical Characteristics (Note 4)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Offset Voltage | $T_A$ = 25°C | | 0.3 | 0.5 | mV |
| Input Offset Current | $T_A$ = 25°C | | 0.2 | 1 | nA |
| Input Bias Current | $T_A$ = 25°C | | 1.5 | 7 | nA |
| Input Resistance | $T_A$ = 25°C | 10 | 40 | | MΩ |
| Supply Current | $T_A$ = 25°C, $V_S$ = ±15V | | 0.3 | 0.8 | mA |
| Large Signal Voltage Gain | $T_A$ = 25°C, $V_S$ = ±15V, $V_{OUT}$ = ±10V, $R_L \geq 10\ k\Omega$ | 80 | 300 | | V/mV |
| Input Offset Voltage | $V_S$ = ±15V, $R_S$ = 100Ω | | | 0.73 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $V_S$ = ±15V, $R_S$ = 100Ω | | 2.0 | 5.0 | µV/°C |
| Input Offset Current | | | | 1.5 | nA |
| Average Temperature Coefficient of Input Offset Current | | | 2.0 | 10 | pA/°C |
| Input Bias Current | | | | 10 | nA |
| Large Signal Voltage Gain | $V_S$ = ±15V, $V_{OUT}$ = ±10V, $R_L \geq 10\ k\Omega$ | 60 | | | V/mV |
| Output Voltage Swing | $V_S$ = ±15V, $R_L$ = 10 kΩ | ±13 | ±14 | | V |
| Input Voltage Range | $V_S$ = ±15V | ±14 | | | V |
| Common Mode Rejection Ratio | | 96 | 110 | | dB |
| Supply Voltage Rejection Ratio | | 96 | 110 | | dB |

**Note 1:** The maximum junction temperature of the LM308A is 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

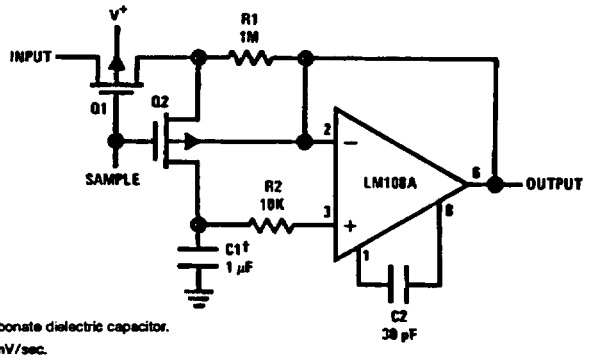
**Note 2:** The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

**Note 3:** For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

**Note 4:** These specifications apply for ±5V ≤ $V_S$ ≤ ±15V and 0°C ≤ $T_A$ ≤ +70°C, unless otherwise specified.

## Typical Applications

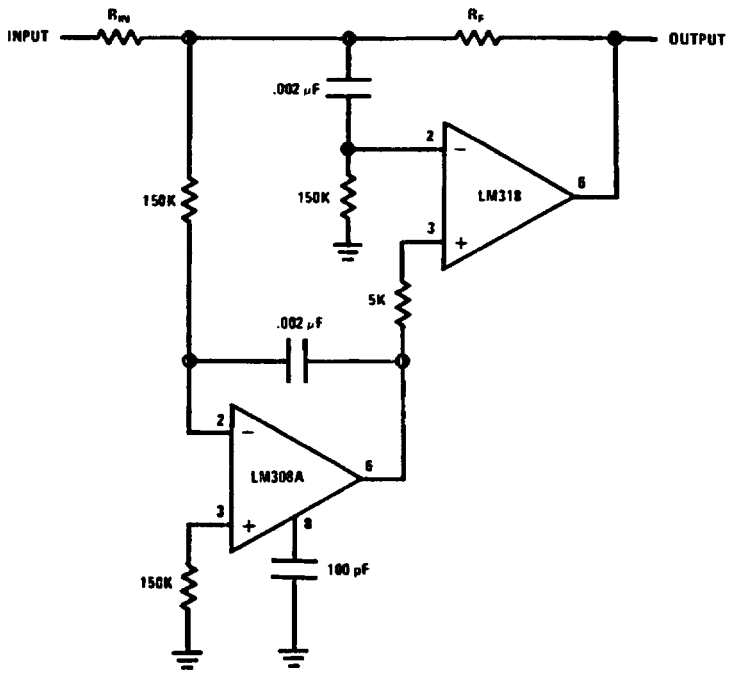
### Sample and Hold




†Teflon, polyethylene or polycarbonate dielectric capacitor.
Worst case drift less than 2.5 mV/sec.

TL/H/7759–4

### High Speed Amplifier with Low Drift and Low Input Current




TL/H/7759–5

## Application Hints

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted.

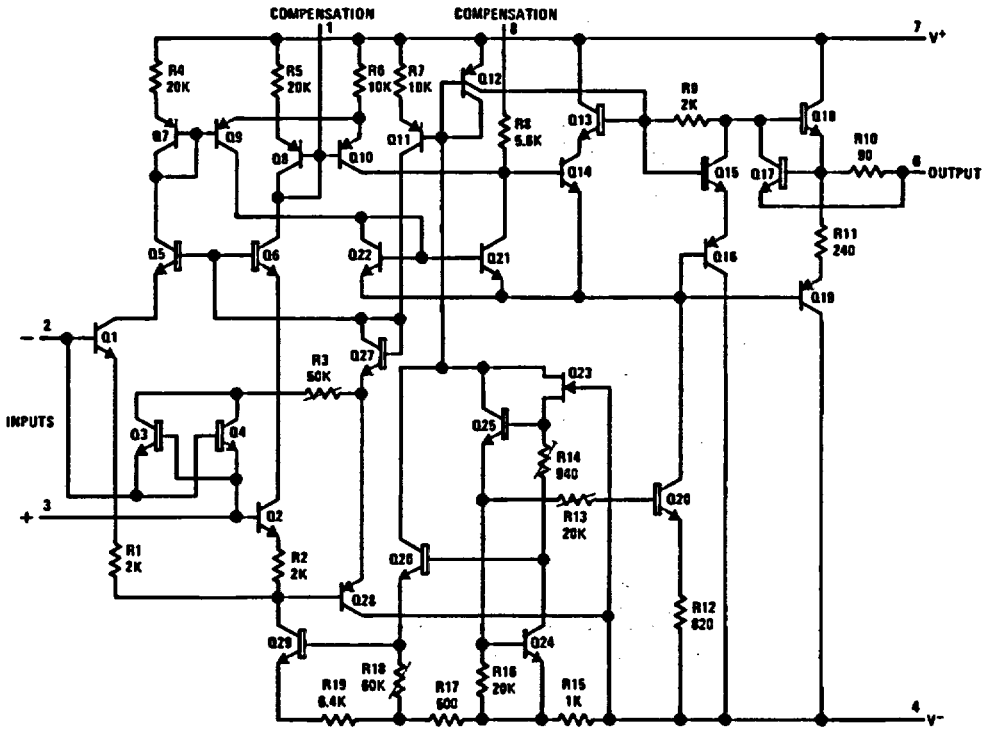
Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Only a few degrees gradient can cause hundreds of microvolts of error. The two places this shows up, generally, are the package-to-printed circuit board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together helps greatly.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evanohm or manganin are best since they only generate about 2 $\mu$V/°C referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low drift stage electrically and thermally will yield good results.

Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature a gain error will result. For example, a gain of 1000 amplifier with a constant 10 mV input will have a 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a 50 $\mu$V error. All of the gain fixing resistor should be the same material.

Testing low drift amplifiers is also difficult. Standard drift testing technique such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method—do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signal through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test along with the gain setting resistor should be isothermal.

## Schematic Diagram

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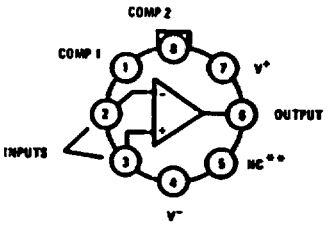
## Connection Diagrams

**Metal Can Package**

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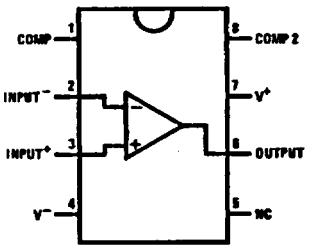
Pin 4 is connected to the case.

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

**Order Number LM108AH, LM208AH or LM208AH**
**See NS Package Number H08C**

**Dual-In-Line Package**

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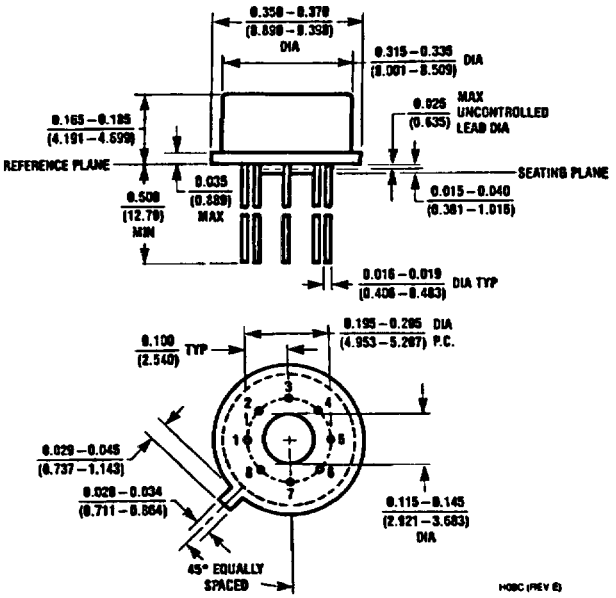
**Top View**

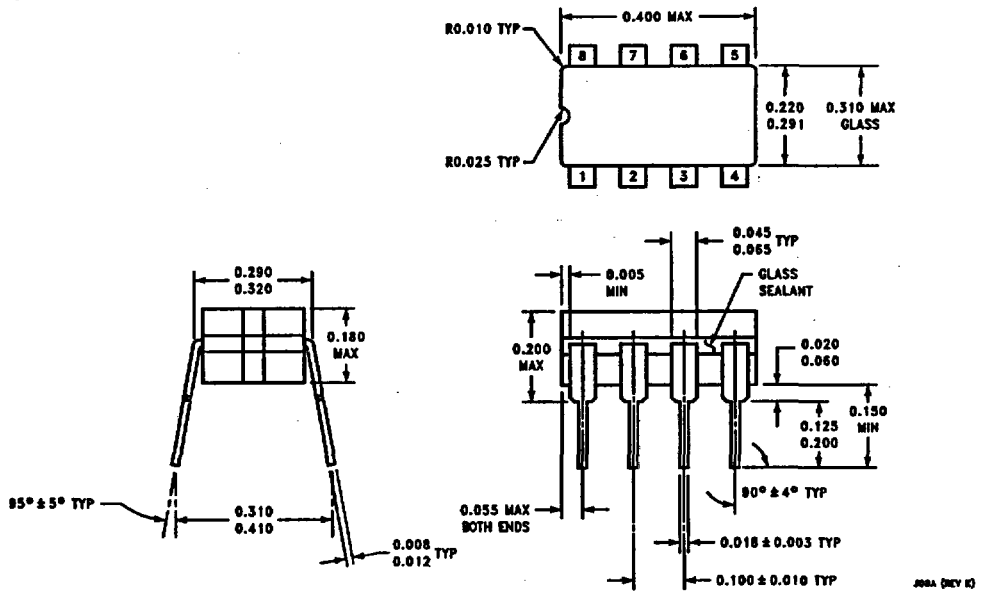
**Order Number LM108AJ-8, LM208AJ-8, LM308AJ-8, LM308AM or LM308AN**
**See NS Package Number J08A, M08A or N08E**

## Physical Dimensions inches (millimeters)

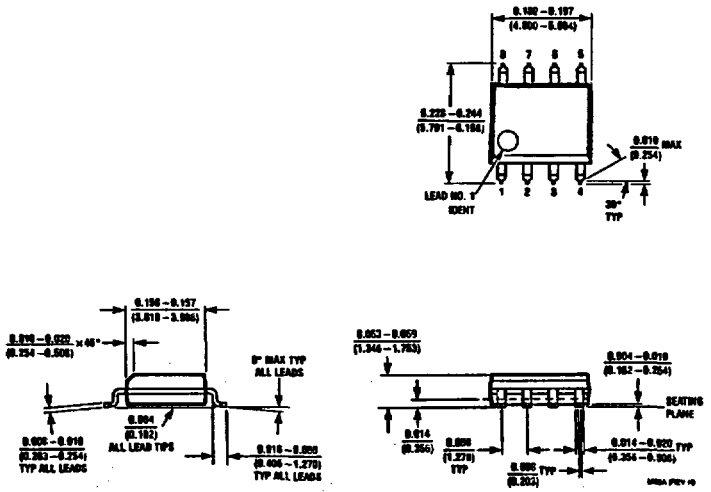



**Metal Can Package (H)**
**Order Number LM108AH, LM208AH or LM308AH**
**NS Package Number H08C**

## Physical Dimensions inches (millimeters) (Continued)

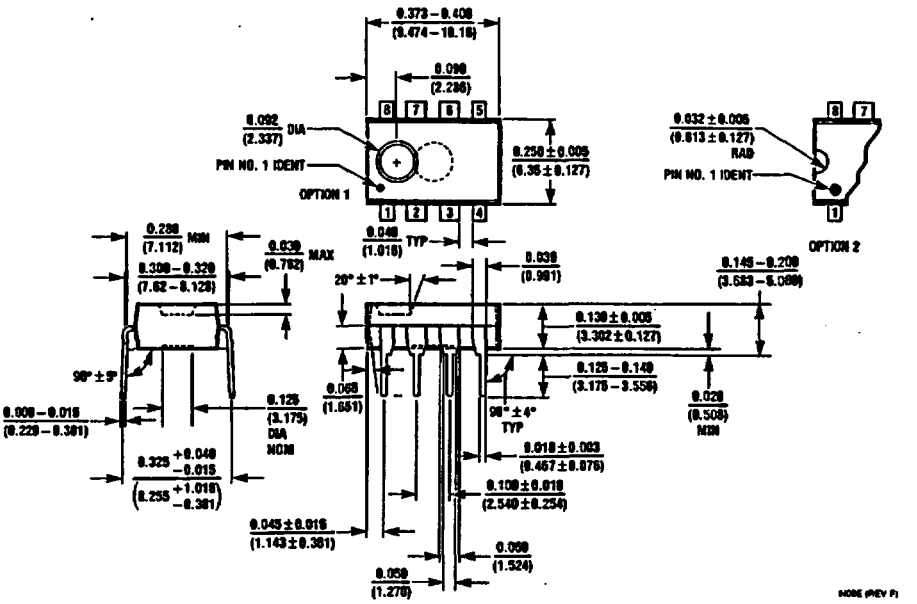



**Ceramic Dual-In-Line Package (J)**
**Order Number LM108AJ-8, LM208AJ-8 or LM308AJ-8**
**NS Package Number J08A**




**S.O. Package (M)**
**Order Number LM308AM**
**NS Package Number M08A**

## Physical Dimensions inches (millimeters) (Continued)




**Molded Dual-In-Line Package (N)**
**Order Number LM308AN**
**NS Package Number N08E**

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